



**1990
Linear
Databook
Volume I**

**1990 Linear Databook
Volume I**



QUICK REFERENCE INDEX

LF155	2-271	LM336-2.5	3-101	LT1008	2-73
LF156	2-271	LM337	4-157	LT1009 Series	3-27
LF198	9-97	LM337HV	4-165	LT1009S8	3-31
LF355	2-271	LM338	4-169	LT1010	2-85
LF356	2-271	LM350	4-177	LT1011	6-9
LF398	9-97	LM385-1.2	3-105	LT1012	2-105
LF398S8	9-113	LM385-2.5	3-109	LT1012S8	2-117
LF412A	2-275	LM385S8-1.2	3-113	LT1013	'92DB 2-19
LH0070	3-65	LM385S8-2.5	3-113	LT1013DS8	'92DB 2-19
LH2108A	2-279	LM399	3-115	LT1014	'92DB 2-19
LM10	2-281	LM399A	3-115	LT1015	'92DB 10-4
LM101A	2-297	LT111A	6-85	LT1016	6-25
LM107	2-297	LT117A	4-137	LT1016CS8	6-41
LM108	2-303	LT117AHV	4-145	LT1017	'94DB 10-4
LM108A	2-303	LT118A	2-311	LT1018	'94DB 10-4
LM111	6-85	LT119A	6-93	LT1019	3-33
LM117	4-137	LT123A	4-149	LT1020	4-29
LM117HV	4-145	LT137A	4-157	LT1020CS	4-45
LM118	2-311	LT137AHV	4-165	LT1021	3-41
LM119	6-93	LT138A	4-169	LT1021DCS8	3-57
LM123	4-149	LT150A	4-177	LT1022	2-145
LM129	3-83	LT311A	6-85	LT1024	2-153
LM134 Series	3-87	LT317A	4-137	LT1025	11-7
LM136-2.5	3-101	LT317AHV	4-145	LT1026	5-3
LM137	4-157	LT318A	2-311	LT1027	'92DB 7-6
LM137HV	4-165	LT319A	6-93	LT1028	'94DB 2-12
LM138	4-169	LT323A	4-149	LT1028CS	'94DB 2-12
LM150	4-177	LT337A	4-157	LT1029	3-61
LM185-1.2	3-105	LT337AHV	4-165	LT1030	10-5
LM185-2.5	3-109	LT338A	4-169	LT1030CS	10-9
LM199	3-115	LT350A	4-177	LT1031	3-65
LM199A	3-115	LT580	3-121	LT1032	10-11
LM234	3-87	LT581	3-121	LT1033	4-49
LM301A	2-297	LT685	6-5	LT1034-1.2	'94DB 7-5
LM307	2-297	LT1001	2-11	LT1034-2.5	'94DB 7-5
LM308	2-303	LT1001CS8	2-23	LT1034CS8-1.2	'94DB 7-5
LM308A	2-303	LT1002	2-25	LT1034CS8-2.5	'94DB 7-5
LM311	6-85	LT1003	4-9	LT1035	4-57
LM317	4-137	LT1004	3-17	LT1036	4-69
LM317HV	4-145	LT1004CS8-1.2	3-25	LT1037	2-57
LM318	2-311	LT1004CS8-2.5	3-25	LT1037CS	2-69
LM318S8	2-319	LT1005	4-17	LT1038	4-77
LM319	6-93	LT1006	2-41	LT1039	10-19
LM323	4-149	LT1006S8	2-53	LT1054	'94DB 4-26
LM329	3-83	LT1007	2-57	LT1055	2-219
LM334S8	3-99	LT1007CS	2-69	LT1055S8	2-231

Note: '92DB = LTC's 1992 Databook Supplement and '94DB = LTC's 1994 Databook Volume III. Quick Reference Index continues on inside back cover.

QUICK REFERENCE INDEX (Continued from inside front cover)

LT1056	2-219	LT1170	'94DB 4-433	LTC1064-1	7-89
LT1056S8	2-231	LT1171	'94DB 4-433	LTC1064-2	'92DB 8-5
LT1057	2-235	LT1172	'94DB 4-433	LTC1064-3	'92DB 8-13
LT1058	2-235	LT1178	'92DB 2-112	LTC1064-4	'92DB 8-21
LT1070	5-37	LT1179	'92DB 2-112	LTC1090	9-5
LT1071	5-37	LT1180 .. See LT1180A	'94DB 5-27	LTC1091	9-29
LT1072	'94DB 4-232	LT1181 .. See LT1181A	'94DB 5-27	LTC1092	9-29
LT1074	'94DB 4-243	LT1188	'92DB 4-48	LTC1093	9-29
LT1077	'92DB 2-45	LT1280 .. See LT1280A	'94DB 5-41	LTC1094	9-29
LT1078	'92DB 2-56	LT1281 .. See LT1281A	'94DB 5-41	LTC1095	9-57
LT1079	'92DB 2-56	LT1431	92DB 7-13	LTC1099	9-81
LT1080 .. See LT1180A	'94DB 5-27	LT1524	5-85	LTC1100	'92DB 3-4
LT1081 .. See LT1181A	'94DB 5-27	LT1525A	5-97	LTC1150	'92DB 2-321
LT1083	'94DB 4-48	LT1526	5-105	LTC1290	'92DB 6-67
LT1083 Fixed	'94DB 4-61	LT1527A	5-97	LTC1291	'94DB 6-163
LT1083-5	'94DB 4-61	LT1846	5-113	LTC1292	'94DB 6-182
LT1083-12	'94DB 4-61	LT1847	5-113	LTC1293	'92DB 6-113
LT1084	'94DB 4-48	LT3524	5-85	LTC1294	'92DB 6-113
LT1084 Fixed	'94DB 4-61	LT3525A	5-97	LTC7652	2-197
LT1084-5	'94DB 4-61	LT3526	5-105	LTC7660	5-9
LT1084-12	'94DB 4-61	LT3527A	5-97	LTk001	11-3
LT1085	'94DB 4-48	LT3846	5-113	LTZ1000	3-9
LT1085 Fixed	'94DB 4-61	LT3847	5-113	LTZ1000A	3-9
LT1085-5	'94DB 4-61	LTC201 .. See LTC201A	'92DB 11-4	OP-05	2-321
LT1085-12	'94DB 4-61	LTC1040	6-57	OP-07	2-329
LT1086 Series	'94DB 4-72	LTC1041	6-69	OP-07CS8	2-337
LT1086-5	'94DB 4-72	LTC1042	6-77	OP-15	2-341
LT1086-12	'94DB 4-72	LTC1043	11-15	OP-16	2-341
LT1087	'92DB 4-56	LTC1043CS	11-31	OP-27	2-345
LT1088	11-33	LTC1044	5-9	OP-37	2-345
LT1089	11-45	LTC1044CS8	5-21	OP-215	2-275
LT1101	'92DB 3-11	LTC1045	10-27	OP-227	2-357
LT1102	'92DB 3-23	LTC1049	'92DB 2-299	OP-237	2-357
LT1120	'94DB 4-96	LTC1050	2-181	REF-01	3-125
LT1130 .. See LT1130A	'94DB 5-10	LTC1051	'92DB 2-306	REF-02	3-125
LT1131 .. See LT1131A	'94DB 5-10	LTC1052	2-197	SG1524	5-85
LT1132 .. See LT1132A	'94DB 5-10	LTC1052CS	2-217	SG1525A	5-97
LT1133 .. See LT1133A	'94DB 5-10	LTC1059	7-3	SG1527A	5-97
LT1134 .. See LT1134A	'94DB 5-10	LTC1059CS	7-11	SG3524	5-85
LT1135 .. See LT1135A	'94DB 5-10	LTC1060	7-15	SG3524S	5-93
LT1136 .. See LT1136A	'94DB 5-10	LTC1060CS	7-35	SG3525A	5-97
LT1137 .. See LT1137A	'94DB 5-20	LTC1061	7-39	SG3527A	5-97
LT1138 .. See LT1138A	'94DB 5-10	LTC1061CS	7-55		
LT1139 .. See LT1139A	'94DB 5-10	LTC1062	'94DB 8-5		
LT1140 .. See LT1140A	'94DB 5-10	LTC1062CS	'94DB 8-5		
LT1141 .. See LT1141A	'94DB 5-10	LTC1064	7-73		

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Linear Technology Corporation
1990 Linear Databook
Volume I

Note: The 1990 Databook is the first volume in our series of databooks. Since its creation some of the products have had some changes made to the data sheets due to additional package types such as surface mount, extended temperature ranges and parametric changes. We have cross referenced these products to the current revised data sheet contained in the 1992 and the 1994 Databooks.

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**1990
Linear
Databook
Volume I**

GENERAL INFORMATION	1
OPERATIONAL AMPLIFIERS	2
VOLTAGE REFERENCES	3
VOLTAGE REGULATORS	4
SWITCHING REGULATORS/VOLTAGE CONVERTERS	5
COMPARATORS	6
FILTERS	7
INSTRUMENTATION AMPLIFIERS	8
DATA CONVERSION	9
RS232 INTERFACE	10
SPECIAL FUNCTION	11
MILITARY PRODUCTS	12
NEW PRODUCTS	13
PACKAGE DIMENSIONS	14
APPENDICES	15

NOTES

TABLE OF CONTENTS

SECTION 1—GENERAL INFORMATION

INDEX	1-2
GENERAL ORDERING INFORMATION	1-3
ALTERNATE SOURCE CROSS REFERENCE GUIDE	1-4

SECTION 2—OPERATIONAL AMPLIFIERS

INDEX	2-2
SELECTION GUIDE	'94DB 2-3
PROPRIETARY PRODUCTS	
LT1001, Precision Op Amp	2-11
LT1001CS8, Precision Op Amp	2-23
LT1002, Dual, Matched Precision Op Amp	2-25
LT1006, Precision, Single Supply Op Amp	2-41
LT1006S8, Precision, Single Supply Op Amp	2-53
LT1007, Low Noise, High Speed Precision Op Amp	2-57
LT1007CS/LT1037CS, Low Noise, High Speed Precision Op Amps	2-69
LT1008, Picoamp Input Current, Microvolt Offset, Low Noise Op Amp	2-73
LT1010, Fast $\pm 150\text{mA}$ Power Buffer	2-85
LT1012, Picoamp Input Current, Microvolt Offset, Low Noise Op Amp	2-105
LT1012S8, Picoamp Input Current, Microvolt Offset, Low Noise Op Amp	2-117
LT1013, Dual Precision Op Amp	'92DB 2-19
LT1013DS8, Dual Precision Op Amp	'92DB 2-19
LT1014, Quad Precision Op Amp	'92DB 2-19
LT1022, High Speed, Precision JFET Input Op Amp	2-145
LT1024, Dual, Matched Picoampere, Microvolt Input, Low Noise Op Amp	2-153
LT1028, Ultra-Low Noise Precision High Speed Op Amp	'94DB 2-12
LT1028CS, Ultra-Low Noise Precision High Speed Op Amp	'94DB 2-12
LT1037, Low Noise, High Speed Precision Op Amp	2-57
LTC1049, Low Power Zero Drift Operational Amplifier with Internal Capacitors	'92DB 2-299
LTC1050, Precision Zero Drift Op Amp with Internal Capacitors	2-181
LTC1051/LTC1053, Dual/Quad Precision Zero Drift Operational Amplifiers with Internal Capacitors	'92DB 2-306
LTC1052, Zero Drift Op Amp	2-197
LTC1052CS, Zero Drift Op Amp	2-217
LT1055, Precision, High Speed, JFET Input Op Amp	2-219
LT1056, Precision, High Speed, JFET Input Op Amp	2-219
LT1055S8/LT1056S8, Precision, High Speed, JFET Input Op Amps	2-231
LT1057, Dual JFET Input Precision, High Speed Op Amp	2-235
LT1057S/LT1057IS, Dual JFET Input Precision, High Speed Op Amps	'92DB 2-41
LT1058, Quad JFET Input Precision, High Speed Op Amp	2-235
LT1077, Micropower, Single Supply, Precision Operational Amplifier	'92DB 2-45
LT1078, Micropower, Dual, Single Supply, Precision Op Amp	'92DB 2-56
LT1079, Micropower, Quad, Single Supply, Precision Op Amp	'92DB 2-56
LTC1100, Precision, Zero Drift Instrumentation Amplifier	'92DB 3-4
LT1101, Precision, Micropower, Single Supply Instrumentation Amplifier (Fixed Gain = 10 or 100)	'92DB 3-11
LT1102, High Speed, Precision, JFET Input Instrumentation Amplifier (Fixed Gain = 10 or 100)	'92DB 3-23
LTC1150, $\pm 15\text{V}$ Zero-Drift Operational Amplifier with Internal Capacitors	'92DB 2-321
LT1178, $17\mu\text{A}$ Max, Dual, Single Supply, Precision Op Amp	'92DB 2-112
LT1179, $17\mu\text{A}$ Max, Quad, Single Supply, Precision Op Amp	'92DB 2-112
ENHANCED AND SECOND SOURCE PRODUCTS	
LF155/LF355, JFET Input Op Amp, Low Supply Current	2-271

Note: '92DB = LTC's 1992 Databook Supplement and '94DB = LTC's 1994 Databook Volume III.

TABLE OF CONTENTS

LF155A/LF355A, JFET Input Op Amp, Low Supply Current	2-271
LF156/LF356, JFET Input Op Amp, High Speed	2-271
LF156A/LF356A, JFET Input Op Amp, High Speed	2-271
LF412A, Dual Precision JFET Input Op Amp	2-275
LH2108A, Dual LM108 Op Amp	2-279
LM10/B(L)/C(L), Low Power Op Amp and Reference	2-281
LM101A/LM301A, Uncompensated General Purpose Op Amp	2-297
LM107/LM307, Compensated General Purpose Op Amp	2-297
LM108/LM308, Super Gain Op Amp	2-303
LM108A/LM308A, Super Gain Op Amp	2-303
LM118/LM318, High Slew Rate Op Amp	2-311
LM318S8, High Speed Op Amp	2-319
LT118A/LT318A, Improved LM118 Op Amp	2-311
LTC7652, Chopper Stabilized Op Amp	2-197
OP-05, OP-05A, OP-05C, OP-05E, Internally Compensated Op Amp	2-321
OP-07, OP-07A, OP-07C, OP-07E, Precision Op Amp	2-329
OP-07CS8, Precision Op Amp	2-337
OP-15A, OP-15B, OP-15C, OP-15E, OP-15F, OP-15G, Precision, High Speed JFET Input Op Amp	2-341
OP-16A, OP-16B, OP-16C, OP-16E, OP-16F, OP-16G, Precision, High Speed JFET Input Op Amp	2-341
OP-27A, OP-27C, OP-27E, OP-27G, Low Noise, Precision Op Amp	2-345
OP-37A, OP-37C, OP-37E, OP-37G, Low Noise, High Speed Op Amp	2-345
OP-215, Dual Precision JFET Input Op Amp	2-275
OP-227A, OP-227C, OP-227E, OP-227G, Dual Matched, Low Noise Op Amp	2-357
OP-237A, OP-237C, OP-237E, OP-237G, Dual High Speed, Low Noise Op Amp	2-357

SECTION 3—VOLTAGE REFERENCES

INDEX	3-2
SELECTION GUIDE	'94DB 7-3
PROPRIETARY PRODUCTS	
LTZ1000, Ultra Precision Reference	3-9
LTZ1000A, Ultra Precision Reference	3-9
LT1004, Micropower Voltage Reference	3-17
LT1004CS8-1.2/LT1004CS8-2.5, Micropower Voltage References	3-25
LT1009 Series, 2.5 Volt Reference	3-27
LT1009S8, 2.5 Volt Reference	3-31
LT1019, Precision References	3-33
LT1021, Precision References	3-41
LT1021DCS8, Precision References	3-57
LT1027, Precision 5V Reference	'92DB 7-6
LT1029, 5V Bandgap Reference	3-61
LT1031, Precision 10V Reference	3-65
LT1034-1.2/LT1034-2.5, Micropower Dual Reference	'94DB 7-5
LT1034CS8-1.2/LT1034CS8-2.5, Micropower Dual Reference	'94DB 7-5
LT1431, Programmable Reference	'92DB 7-13
ENHANCED AND SECOND SOURCE PRODUCTS	
LH0070, Precision 10V Reference	3-65
LM129/LM329, 6.9V Precision Voltage Reference	3-83
LM134 Series, Constant Current Source and Temperature Sensor	3-87
LM334S8, Constant Current Source and Temperature Sensor	3-99
LM136-2.5/LM336-2.5, 2.5 Volt Reference	3-101

Note: '92DB = LTC's 1992 Databook Supplement and '94DB = LTC's 1994 Databook Volume III.

TABLE OF CONTENTS

LM185-1.2/LM385-1.2, Micropower Voltage Reference	3-105
LM185-2.5/LM385-2.5, Micropower Voltage Reference	3-109
LM385S8-1.2/LM385S8-2.5, Micropower Voltage Reference	3-113
LM199/LM399/LM199A/LM399A, Precision Reference	3-115
LT580, Precision Reference	3-121
LT581, Precision Reference	3-121
REF-01/REF-02, Precision Voltage References	3-125

SECTION 4—VOLTAGE REGULATORS

INDEX	4-2
SELECTION GUIDE	'94DB 4-4
PROPRIETARY PRODUCTS	
<i>LT1003, 5 Volt, 5 Amp Voltage Regulator</i>	4-9
<i>LT1005, Logic Controlled Regulator</i>	4-17
<i>LT1020, Micropower Regulator and Comparator</i>	4-29
<i>LT1020CS, Micropower Regulator and Comparator</i>	4-45
<i>LT1033, 3A Negative Adjustable Regulator</i>	4-49
<i>LT1035, Logic Controlled Regulator</i>	4-57
<i>LT1036, Logic Controlled Regulator</i>	4-69
<i>LT1038, 10 Amp Positive Adjustable Voltage Regulator</i>	4-77
<i>LT1083, 7.5A Low Dropout Positive Adjustable Regulator</i>	'94DB 4-48
<i>LT1083-5, 7.5A Low Dropout Positive Fixed 5V Regulator</i>	'94DB 4-61
<i>LT1083-12, 7.5A Low Dropout Positive Fixed 12V Regulator</i>	'94DB 4-61
<i>LT1084, 5A Low Dropout Positive Adjustable Regulator</i>	'94DB 4-48
<i>LT1084-5, 5A Low Dropout Positive Fixed 5V Regulator</i>	'94DB 4-61
<i>LT1084-12, 5A Low Dropout Positive Fixed 12V Regulator</i>	'94DB 4-61
<i>LT1085, 3A Low Dropout Positive Adjustable Regulator</i>	'94DB 4-48
<i>LT1085-5, 3A Low Dropout Positive Fixed 5V Regulator</i>	'94DB 4-61
<i>LT1085-12, 3A, Low Dropout Positive Fixed 12V Regulator</i>	'94DB 4-61
<i>LT1086, 1.5A Low Dropout Positive Adjustable Regulator</i>	'94DB 4-72
<i>LT1086-5, 1.5A Low Dropout Positive Fixed 5V Regulator</i>	'94DB 4-72
<i>LT1086-12, 1.5A Low Dropout Positive Fixed 12V Regulator</i>	'94DB 4-72
<i>LT1087, Adjustable Low Dropout Regulator with Kelvin-Sense Inputs</i>	'92DB 4-56
<i>LT1120, Micropower Regulator with Comparator and Shutdown</i>	'94DB 4-96
ENHANCED AND SECOND SOURCE PRODUCTS	
<i>LM117/LM317, Positive Adjustable Regulator</i>	4-137
<i>LT117A/LT317A, Improved LM117</i>	4-137
<i>LM117HV/LM317HV, High Voltage Positive Adjustable Regulator</i>	4-145
<i>LT117AHV/LT317AHV, Improved LM117HV</i>	4-145
<i>LM123/LM323, 5 Volt, 3 Amp Regulator</i>	4-149
<i>LT123A/LT323A, Improved LM123</i>	4-149
<i>LM137/LM337, Negative Adjustable Regulator</i>	4-157
<i>LT137A/LT337A, Improved LM137</i>	4-157
<i>LM137HV/LM337HV, High Voltage Negative Adjustable Regulator</i>	4-165
<i>LT137AHV/LT337AHV, Improved LM137HV</i>	4-165
<i>LM138/LM338, 5 Amp Positive Adjustable Regulator</i>	4-169
<i>LT138A/LT338A, Improved LM138</i>	4-169
<i>LM150/LM350, 3 Amp Positive Adjustable Regulator</i>	4-177
<i>LT150A/LT350A, Improved LM150</i>	4-177

Note: '92DB = LTC's 1992 Databook Supplement and '94DB = LTC's 1994 Databook Volume III.

TABLE OF CONTENTS

SECTION 5—SWITCHING REGULATORS AND VOLTAGE CONVERTERS

INDEX	5-2
PROPRIETARY PRODUCTS	
<i>LT1026, Voltage Converter</i>	5-3
<i>LTC1044/7660, Switched Capacitor Voltage Converter</i>	5-9
<i>LTC1044CS8, Switched Capacitor Voltage Converter</i>	5-21
<i>LT1054, Switched Capacitor Voltage Converter with Regulator</i>	'94DB 4-26
<i>LT1054CS/LT1054IS, Switched Capacitor Voltage Converter with Regulator</i>	'94DB 4-26
<i>LT1070, 5A High Efficiency Switching Regulator</i>	5-37
<i>LT1071, 2.5A High Efficiency Switching Regulator</i>	5-37
<i>LT1072, 1.25A High Efficiency Switching Regulator</i>	'94DB 4-232
<i>LT1074, Switching Regulator</i>	'94DB 4-243
<i>LT1170, 100kHz, 5A, High Efficiency 100kHz Switching Regulators</i>	'94DB 4-433
<i>LT1171, 100kHz, 2.5A High Efficiency 100kHz Switching Regulators</i>	'94DB 4-433
<i>LT1172, 100kHz, 1.25A High Efficiency 100kHz Switching Regulators</i>	'94DB 4-433
ENHANCED AND SECOND SOURCE PRODUCTS	
<i>SG1524/SG3524, Regulating Pulse Width Modulators</i>	5-85
<i>SG3524S, Regulating Pulse Width Modulator</i>	5-93
<i>LT1524/LT3524, Regulating Pulse Width Modulators</i>	5-85
<i>SG1525A/SG3525A, Regulating Pulse Width Modulators</i>	5-97
<i>LT1525A/LT3525A, Regulating Pulse Width Modulators</i>	5-97
<i>LT1526/LT3526, Regulating Pulse Width Modulators</i>	5-105
<i>SG1527A/SG3527A, Regulating Pulse Width Modulators</i>	5-97
<i>LT1527A/LT3527A, Regulating Pulse Width Modulators</i>	5-97
<i>LT1846/LT1847, Current Mode PWM Controller</i>	5-113
<i>LT3846/LT3847, Current Mode PWM Controller</i>	5-113

SECTION 6—COMPARATORS

INDEX	6-2
SELECTION GUIDE	'94DB 10-3
PROPRIETARY PRODUCTS	
<i>LT685, High Speed Comparator</i>	6-5
<i>LT1011, Voltage Comparator</i>	6-9
<i>LT1015, High Speed Dual Line Receiver</i>	'92DB 10-4
<i>LT1016, Ultra Fast Precision Comparator</i>	6-25
<i>LT1016CS8, Ultra Fast Precision Comparator</i>	6-41
<i>LT1017, Micropower Dual Comparator</i>	'94DB 10-4
<i>LT1018, Micropower Dual Comparator</i>	'94DB 10-4
<i>LT1017CS/LT1018CS, Micropower Dual Comparator</i>	'94DB 10-4
<i>LTC1040, Dual Micropower Comparator</i>	6-57
<i>LTC1041, BANG-BANG Controller</i>	6-69
<i>LTC1042, Window Comparator</i>	6-77
ENHANCED AND SECOND SOURCE PRODUCTS	
<i>LM111/LM311, Voltage Comparator</i>	6-85
<i>LT111A/LT311A, Improved LM111</i>	6-85
<i>LM119/LM319, Dual Comparator</i>	6-93
<i>LT119A/LT319A, Improved LM119</i>	6-93

Note: '92DB = LTC's 1992 Databook Supplement and '94DB = LTC's 1994 Databook Volume III.

TABLE OF CONTENTS

SECTION 7—FILTERS

INDEX	7-2
PROPRIETARY PRODUCTS	
LTC1059, High Performance Switched Capacitor Universal Filter	7-3
LTC1059CS, High Performance Switched Capacitor Universal Filter	7-11
LTC1060, Universal Dual Filter Building Block	7-15
LTC1060CS, Universal Dual Filter Building Block	7-35
LTC1061, High Performance Triple Universal Filter Building Block	7-39
LTC1061CS, High Performance Triple Universal Filter Building Block	7-55
LTC1062, 5th Order Lowpass Filter	'94DB 8-5
LTC1062CS, 5th Order Lowpass Filter	'94DB 8-5
LTC1064, Low Noise, Fast, Quad Universal Filter Building Block	7-73
LTC1064-1, Low Noise, 8th Order, Clock Sweeplable Elliptic Lowpass Filter	7-89
LTC1064-2, Low Noise, High Frequency, 8th Order Butterworth Lowpass Filter	'92DB 8-5
LTC1064-3, Low Noise, High Frequency, 8th Order Linear Phase Lowpass Filter	'92DB 8-13
LTC1064-4, Low Noise, 8th Order, Clock Sweeplable Cauer Lowpass Filter	'92DB 8-21

SECTION 8—INSTRUMENTATION AMPLIFIERS

INDEX	8-2
PROPRIETARY PRODUCTS	
LTC1043, Dual Instrumentation Switched Capacitor Building Block	11-15
LTC1100, Precision, Zero-Drift, Instrumentation Amplifier (Fixed Gain = 100)	'92DB 3-4
LT1101, Precision, Micropower, Single Supply Instrumentation Amplifier (Fixed Gain = 10 or 100)	'92DB 3-11
LT1102, High Speed, Precision, JFET Input Instrumentation Amplifier (Fixed Gain = 10 or 100)	'92DB 3-23

SECTION 9—DATA CONVERSION

INDEX	9-2
SELECTION GUIDE	'94DB 6-3
PROPRIETARY PRODUCTS	
LTC1090, Single Chip 10-Bit Data Acquisition System	9-5
LTC1091, 1-Channel, 10-Bit Serial I/O Data Acquisition System	9-29
LTC1092, 2-Channel, 10-Bit Serial I/O Data Acquisition System	9-29
LTC1093, 6-Channel, 10-Bit Serial I/O Data Acquisition System	9-29
LTC1094, 8-Channel, 10-Bit Serial I/O Data Acquisition System	9-29
LTC1095, Complete 10-Bit Data Acquisition System with On Board Reference	9-57
LTC1099, High Speed 8-Bit A/D Converter with Built-In Sample-and-Hold	9-81
LTC1290, Single Chip 12-Bit Data Acquisition System	'92DB 6-67
LTC1291, 1-Channel, 12-Bit Serial I/O Data Acquisition System	'94DB 6-163
LTC1292, 2-Channel, 12-Bit Serial I/O Data Acquisition System	'94DB 6-182
LTC1293, 6-Channel, 12-Bit Serial I/O Data Acquisition System	'92DB 6-113
LTC1294, 8-Channel, 12-Bit Serial I/O Data Acquisition System	'92DB 6-113
SECOND SOURCE PRODUCTS	
LF198A/LF398A, Precision Sample and Hold Amplifier	9-97
LF198/LF398, Precision Sample and Hold Amplifier	9-97
LF398S8, Precision Sample and Hold Amplifier	9-113

Note: '92DB = LTC's 1992 Databook Supplement and '94DB = LTC's 1994 Databook Volume III.

TABLE OF CONTENTS

SECTION 10—RS232 INTERFACE

INDEX		10-2
SELECTION GUIDE		'94DB 5-3
PROPRIETARY PRODUCTS		
<i>LT1015, High Speed Dual Line Receiver</i>	'92DB	10-4
<i>LT1030, Quad Low Power Line Driver</i>		10-5
<i>LT1030CS, Quad Low Power Line Driver</i>		10-9
<i>LT1032, Quad Low Power Line Driver</i>		10-11
<i>LT1039, RS232 Driver/Receiver with Shutdown</i>		10-19
<i>LT1045, Programmable Micropower Hex Translator/Receiver/Driver</i>		10-27
<i>LT1080, Advanced Low Power 5V RS232 Dual Driver/Receiver</i>	Refer to LT1180A	'94DB 5-27
<i>LT1081, Advanced Low Power 5V RS232 Dual Driver/Receiver</i>	Refer to LT1181A	'94DB 5-27
<i>LT1080CS/LT1081CS, 5V Powered RS232 Driver/Receiver with Shutdown</i>	Refer to LT1180A/LT1181A	'94DB 5-27
<i>LT1130, 5-Driver/5-Receiver RS232 Transceiver</i>	Refer to LT1130A	'94DB 5-10
<i>LT1131, 5-Driver/4-Receiver RS232 Transceiver with Shutdown</i>	Refer to LT1131A	'94DB 5-10
<i>LT1132, 5-Driver/3-Receiver RS232 Transceiver</i>	Refer to LT1132A	'94DB 5-10
<i>LT1133, 3-Driver/5-Receiver RS232 Transceiver</i>	Refer to LT1133A	'94DB 5-10
<i>LT1134, 4-Driver/4-Receiver RS232 Transceiver</i>	Refer to LT1134A	'94DB 5-10
<i>LT1135, 5-Driver/3-Receiver RS232 Transceiver without Charge Pump</i>	Refer to LT1135A	'94DB 5-10
<i>LT1136, 4-Driver/5-Receiver RS232 Transceiver with Shutdown</i>	Refer to LT1136A	'94DB 5-10
<i>LT1137, 3-Driver/5-Receiver RS232 Transceiver with Shutdown</i>	Refer to LT1137A	'94DB 5-20
<i>LT1138, 5-Driver/3-Receiver RS232 Transceiver with Shutdown</i>	Refer to LT1138A	'94DB 5-10
<i>LT1139, 4-Driver/4-Receiver RS232 Transceiver with Shutdown</i>	Refer to LT1139A	'94DB 5-10
<i>LT1140, 5-Driver/3-Receiver RS232 Transceiver without Charge Pump</i>	Refer to LT1140A	'94DB 5-10
<i>LT1141, 3-Driver/5-Receiver RS232 Transceiver without Charge Pump</i>	Refer to LT1141A	'94DB 5-10
<i>LT1180, Advanced Low Power RS232 Dual Driver/Receiver with Small Capacitors</i>	Refer to LT1180A	'94DB 5-27
<i>LT1181, Advanced Low Power RS232 Dual Driver/Receiver with Small Capacitors</i>	Refer to LT1181A	'94DB 5-27
<i>LT1280, Advanced Low Power 5V RS232 Dual Driver/Receiver</i>	Refer to LT1280A	'94DB 5-41
<i>LT1281, Advanced Low Power 5V RS232 Dual Driver/Receiver</i>	Refer to LT1281A	'94DB 5-41

SECTION 11—SPECIAL FUNCTION

INDEX		11-2
PROPRIETARY PRODUCTS		
<i>LTK001, Thermocouple Cold Junction Compensator and Matched Amplifier</i>		11-3
<i>LTC201, Quad CMOS SPST Low Charge Injection Analog Switch</i>	Refer to LTC201A	'92DB 11-4
<i>LT1025, Micropower Thermocouple Cold Junction Compensator</i>		11-7
<i>LTC1043, Dual Precision Instrumentation Switched Capacitor Building Block</i>		11-15
<i>LTC1043CS, Dual Precision Instrumentation Switched Capacitor Building Block</i>		11-31
<i>LT1088, Wideband RMS-DC Converter Building Block</i>		11-33
<i>LT1089, High Side Switch</i>		11-45
<i>LT1188, 1.5A High Side Switch</i>	'92DB	4-48

SECTION 12—MILITARY PRODUCTS

INDEX		'94DB 12-2
MIL/JAN Products		'94DB 12-3
Standard Military Drawings		'94DB 12-4
Hi-Rel		'94DB 12-7
MIL-STD-883 Product		'94DB 12-7
MIL-M-38510 Class B Flow		'94DB 12-4

Note: '92DB = LTC's 1992 Databook Supplement and '94DB = LTC's 1994 Databook Volume III.

TABLE OF CONTENTS

MIL-M-38510 Class S Flow	'94DB	12-5
Military Sampling Plan	'94DB	12-7
MIL-STD-883 Test Methods	'94DB	12-9
Military Parts List	'94DB	12-13

SECTION 13—NEW PRODUCTS

INDEX		13-2
PROPRIETARY PRODUCTS		
<i>LTC201, Quad CMOS SPST Low Charge Injection Analog Switch</i>	Refer to LTC201A	'92DB 11-4
<i>LT1015, High Speed Dual Line Receiver</i>		'92DB 10-4
<i>LT1027, Precision 5V Reference</i>		'92DB 7-6
<i>LTC1049, Low Power Chopper Stabilized Op Amp with Internal Capacitor</i>		'92DB 2-299
<i>LTC1051, Dual Precision Chopper Stabilized Op Amp with Internal Capacitors</i>		'92DB 2-306
<i>LTC1064-2, Low Noise, High Frequency 8th Order Butterworth Lowpass Filter</i>		'92DB 8-5
<i>LTC1064-3, Low Noise, High Frequency 8th Order Linear Phase Lowpass Filter</i>		'92DB 8-13
<i>LTC1064-4, Low Noise, 8th Order, Clock Sweepable Cauer Lowpass Filter</i>		'92DB 8-21
<i>LT1074, Switching Regulator</i>		'94DB 4-243
<i>LT1077, Micropower, Single Supply, Precision Op Amp</i>		'92DB 2-45
<i>LT1087, Adjustable Low Dropout Regulator with Kelvin-Sense Inputs</i>		'92DB 4-56
<i>LTC1100, Precision, Single Supply, Instrumentation Amplifier (Fixed Gain = 100)</i>		'92DB 3-4
<i>LT1101, Precision, Micropower, Single Supply Instrumentation Amplifier (Fixed Gain = 10 or 100)</i>		'92DB 3-11
<i>LT1102, High Speed, Precision, JFET Input Instrumentation Amplifier (Fixed Gain = 10 or 100)</i>		'92DB 3-23
<i>LTC1150, ±15V Chopper Stabilized Op Amp with Internal Capacitors</i>		'92DB 2-321
<i>LT1188, 1.5A High Side Switch</i>		'92DB 4-48
<i>LTC1290, Single Chip 12-Bit Data Acquisition System</i>		'92DB 6-67
<i>LTC1291, 1-Channel, 12-Bit Serial I/O Data Acquisition System</i>		'94DB 6-163
<i>LTC1292, 2-Channel, 12-Bit Serial I/O Data Acquisition System</i>		'92DB 6-182
<i>LTC1293, 6-Channel, 12-Bit Serial I/O Data Acquisition System</i>		'92DB 6-113
<i>LTC1294, 8-Channel, 12-Bit Serial I/O Data Acquisition System</i>		'92DB 6-113
<i>LT1431, Programmable Reference</i>		'92DB 7-13

SECTION 14—PACKAGE DIMENSIONS

INDEX	'94DB	14-2
Package Cross Reference	'94DB	14-3
Package Dimensions	'94DB	14-5

SECTION 15—APPENDICES

INDEX	'94DB	15-2
Introduction to Quality and Reliability Assurance Programs	'94DB	15-3
Reliability Assurance Program	'94DB	15-4
Quality Assurance Program	'94DB	15-20
R-Flow	'94DB	15-34
ESD Protection Program	'94DB	15-35
Surface Mount Products	'94DB	15-49
Surface Mount Parts List	'94DB	15-58
Dice Products	'94DB	15-62
Application Notes Index	'94DB	15-64

ALPHANUMERIC INDEX

Extended Temperature Range–200°C Products	13-74
JM38510/10104BCA, LM108AJ Super Gain Op Amp	2-303
JM38510/10104BGA, LM108AH Super Gain Op Amp	2-303
JM38510/10104BGC, LM108AH Super Gain Op Amp	2-303
JM38510/10104BPA, LM108AJ8 Super Gain Op Amp	2-303
JM38510/10106BEA, LH2108AD Super Gain Op Amp	2-279
JM38510/10107BGA, LM118H High Slew Rate Op Amp	2-311
JM38510/10107BGC, LM118H High Slew Rate Op Amp	2-311
JM38510/10107BPA, LM118J8 High Slew Rate Op Amp	2-311
JM38510/11401BGA, LF155H High Performance JFET Input Op Amp	2-271
JM38510/11401BGC, LF155H High Performance JFET Input Op Amp	2-271
JM38510/11401BPA, LF155J8 High Performance JFET Input Op Amp	2-271
JM38510/11402BGA, LF156H High Speed JFET Input Op Amp	2-271
JM38510/11402BGC, LF156H High Speed JFET Input Op Amp	2-271
JM38510/11402BPA, LF156J8 High Speed JFET Input Op Amp	2-271
JM38510/11404BGA, LF155AH High Performance JFET Input Op Amp	2-271
JM38510/11404BGC, LF155AH High Performance JFET Input Op Amp	2-271
JM38510/11405BGA, LF156AH High Speed JFET Input Op Amp	2-271
JM38510/11405BGC, LF156AH High Speed JFET Input Op Amp	2-271
JM38510/11405BPA, LF156AJ8 High Speed JFET Input Op Amp	2-271
JM38510/11703BXA, LM117H Adjustable Positive Voltage Regulator	4-137
JM38510/11703BXC, LM117H Adjustable Positive Voltage Regulator	4-137
JM38510/11704BYA, LM117K Adjustable Positive Voltage Regulator	4-137
JM38510/11706BYA, LM138K Adjustable Positive Voltage Regulator	4-169
JM38510/11803BXA, LM137H Adjustable Negative Voltage Regulator	4-157
JM38510/11803BXC, LM137H Adjustable Negative Voltage Regulator	4-157
JM38510/11804BYA, LM137K Adjustable Negative Voltage Regulator	4-157
JM38510/12501BGA, LF198H Sample and Hold Amplifier	9-97
JM38510/12501BGC, LF198H Sample and Hold Amplifier	9-97
JM38510/13501BGA, OP07AH Precision Op Amp	2-329
JM38510/13501BGC, OP07AH Precision Op Amp	2-329
JM38510/13501BPA, OP07AJ8 Precision Op Amp	2-329
JM38510/13502BGA, OP07H Precision Op Amp	2-329
JM38510/13502BGC, OP07H Precision Op Amp	2-329
JM38510/13502BPA, OP07J8 Precision Op Amp	2-329
JM38510/13503BGA, OP27AH Low Noise, Precision Op Amp	2-345
JM38510/13503BGC, OP27AH Low NOise, Precision Op Amp	2-345
JM38510/13503BPA, OP27AJ8 Low Noise, Precision Op Amp	2-345
LF155, JFET Input Op Amp, Low Supply Current	2-271
LF155A, JFET Input Op Amp, Low Supply Current	2-271
LF156, JFET Input Op Amp, High Speed	2-271
LF156A, JFET Input Op Amp, High Speed	2-271
LF198, Precision Sample and Hold Amplifier	9-97
LF198A, Precision Sample and Hold Amplifier	9-97
LF355, JFET Input Op Amp, Low Supply Current	2-271

Note: '92DB = LTC's 1992 Databook Supplement and '94DB = LTC's 1994 Databook Volume III.

ALPHANUMERIC INDEX

LF355A, JFET Input Op Amp, Low Supply Current	2-271
LF356, JFET Input Op Amp, High Speed	2-271
LF356A, JFET Input Op Amp, High Speed	2-271
LF398, Precision Sample and Hold Amplifier	9-97
LF398A, Precision Sample and Hold Amplifier	9-97
LF398S8, Precision Sample and Hold Amplifier	9-113
LF412C, Dual Precision JFET Input Op Amp	2-275
LF412M, Dual Precision JFET Input Op Amp	2-275
LF412AC, Dual Precision JFET Input Op Amp	2-275
LF412AM, Dual Precision JFET Input Op Amp	2-275
LH0070-0, 10V, 3-Lead Trimmed Reference	3-65
LH0070-1, 10V, 3-Lead Trimmed Reference	3-65
LH0070-2, 10V, 3-Lead Trimmed Reference	3-65
LH2108, Dual Super Beta Op Amp	2-279
LH2108A, Dual Super Beta Op Amp	2-279
LM10, Low Power Op Amp and Reference	2-281
LM10B, Low Power Op Amp and Reference	2-281
LM10BL, Low Power Op Amp and Reference	2-281
LM10C, Low Power Op Amp and Reference	2-281
LM10CL, Low Power Op Amp and Reference	2-281
LM101A, Uncompensated General Purpose Op Amp	2-297
LM107, Compensated General Purpose Op Amp	2-297
LM108, Super Gain Op Amp	2-303
LM108A, Super Gain Op Amp	2-303
LM111, Voltage Comparator	6-85
LM117, Positive Adjustable Regulator	4-137
LM117HV, High Voltage Positive Adjustable Regulator	4-145
LM118, High Slew Rate Op Amp	2-311
LM119, Dual Comparator	6-93
LM123, 5 Volt, 3 Amp Regulator	4-149
LM129A, 6.9 Volt Precision Voltage Reference	3-83
LM129B, 6.9 Volt Precision Voltage Reference	3-83
LM129C, 6.9 Volt Precision Voltage Reference	3-83
LM134, Constant Current Source and Temperature Sensor	3-87
LM136, 2.5 Volt Voltage Reference	3-101
LM136A, 2.5 Volt Voltage Reference	3-101
LM137, Negative Adjustable Regulator	4-157
LM137HV, High Voltage Negative Adjustable Regulator	4-165
LM138, 5 Amp Positive Adjustable Regulator	4-169
LM150, 3 Amp Positive Adjustable Regulator	4-177
LM185-1.2, Micropower Voltage Reference	3-105
LM185-2.5, Micropower Voltage Reference	3-109
LM199, Precision Reference	3-115
LM199A, Precision Reference	3-115
LM234, Constant Current Source and Temperature Sensor	3-87

Note: '92DB = LTC's 1992 Databook Supplement and '940B = LTC's 1994 Databook Volume III.

ALPHANUMERIC INDEX

LM301A, Uncompensated General Purpose Op Amp	2-297
LM307, Compensated General Purpose Op Amp	2-297
LM308, Super Gain Op Amp	2-303
LM308A, Super Gain Op Amp	2-303
LM311A, Voltage Comparator	6-85
LM317, Positive Adjustable Regulator	4-137
LM317HV, High Voltage Positive Adjustable Regulator	4-145
LM318, High Slew Rate Op Amp	2-311
LM318S8, High Speed Op Amp	2-319
LM319, Dual Comparator	6-93
LM323, 5 Volt, 3 Amp Regulator	4-149
LM329A, 6.9V Precision Voltage Reference	3-83
LM329B, 6.9V Precision Voltage Reference	3-83
LM329C, 6.9V Precision Voltage Reference	3-83
LM329D, 6.9V Precision Voltage Reference	3-83
LM334, Constant Current Source and Temperature Sensor	3-87
LM334S8, Constant Current Source and Temperature Sensor	3-99
LM336-2.5, 2.5 Volt Reference	3-101
LM336B, 2.5 Volt Reference	3-101
LM337, Negative Adjustable Regulator	4-157
LM337HV, High Voltage Negative Adjustable Regulator	4-165
LM338, 5 Amp Positive Adjustable Regulator	4-169
LM350, 3 Amp Positive Adjustable Regulator	4-177
LM385-1.2, Micropower Voltage Reference	3-105
LM385-2.5, Micropower Voltage Reference	3-109
LM385S8-1.2, Micropower Voltage Reference	3-113
LM385S8-2.5, Micropower Voltage Reference	3-113
LM399, Precision Reference	3-115
LM399A, Precision Reference	3-115
LT111A, High Performance Voltage Comparator	6-85
LT117A, Positive Adjustable Regulator	4-137
LT117AHV, High Voltage Positive Adjustable Regulator	4-145
LT118A, High Slew Rate Op Amp	2-311
LT119A, High Speed Dual Comparator	6-93
LT123A, 5 Volt, 3 Amp Regulator	4-149
LT137A, Negative Adjustable Regulator	4-157
LT137AHV, High Voltage Negative Adjustable Regulator	4-165
LT138A, 5 Amp Positive Adjustable Regulator	4-169
LT150A, 3 Amp Positive Adjustable Regulator	4-177
LT311A, High Performance Voltage Comparator	6-85
LT317A, Positive Adjustable Regulator	4-137
LT317AHV, High Voltage Positive Adjustable Regulator	4-145
LT318A, High Slew Rate Op Amp	2-311
LT319A, High Speed Dual Comparator	6-93
LT323A, 5 Volt, 3 Amp Regulator	4-149

Note: '92DB = LTC's 1992 Databook Supplement and '94DB = LTC's 1994 Databook Volume III.

ALPHANUMERIC INDEX

LT337A, Negative Adjustable Regulator	4-157
LT337AHV, High Voltage Negative Adjustable Regulator	4-165
LT338A, 5Amp Positive Adjustable Regulator	4-169
LT350A, 3 Amp Positive Adjustable Regulator	4-177
LT580J, Precision 2.5V 3 Terminal Reference	3-121
LT580K, Precision 2.5V 3 Terminal Reference	3-121
LT580L, Precision 2.5V 3 Terminal Reference	3-121
LT580M, Precision 2.5V 3 Terminal Reference	3-121
LT580S, Precision 2.5V 3 Terminal Reference	3-121
LT580T, Precision 2.5V 3 Terminal Reference	3-121
LT580U, Precision 2.5V 3 Terminal Reference	3-121
LT581J, Precision 10V 3 Terminal Reference	3-121
LT581K, Precision 10V 3 Terminal Reference	3-121
LT581S, Precision 10V 3 Terminal Reference	3-121
LT581T, Precision 10V 3 Terminal Reference	3-121
LT581U, Precision 10V 3 Terminal Reference	3-121
LT685C, High Speed Comparator	6-5
LT685M, High Speed Comparator	6-5
LT1001AC, Precision Op Amp	2-11
LT1001AM, Precision Op Amp	2-11
LT1001C, Precision Op Amp	2-11
LT1001CS8, Precision Op Amp	2-23
LT1001M, Precision Op Amp	2-11
LT1002AC, Dual, Matched Precision Op Amp	2-25
LT1002AM, Dual, Matched Precision Op Amp	2-25
LT1002C, Dual, Matched Precision Op Amp	2-25
LT1002M, Dual, Matched Precision Op Amp	2-25
LT1003C, 5 Volt, 5 Amp Voltage Regulator	4-9
LT1003M, 5 Volt, 5 Amp Voltage Regulator	4-9
LT1004C, Micropower Voltage Reference	3-17
LT1004CS8-1.2, Micropower Voltage Reference	3-25
LT1004CS8-2.5, Micropower Voltage Reference	3-25
LT1004M, Micropower Voltage Reference	3-17
LT1005C, Logic Controlled Regulator	4-17
LT1005M, Logic Controlled Regulator	4-17
LT1006AC, Precision, Single Supply Op Amp	2-41
LT1006AM, Precision, Single Supply Op Amp	2-41
LT1006C, Precision, Single Supply Op Amp	2-41
LT1006M, Precision, Single Supply Op Amp	2-41
LT1006S8, Precision, Single Supply Op Amp	2-53
LT1007AC, Low Noise, High Speed Precision Op Amp	2-57
LT1007AM, Low Noise, High Speed Precision Op Amp	2-57
LT1007C, Low Noise, High Speed Precision Op Amp	2-57
LT1007CS, Low Noise, High Speed Precision Op Amp	2-69
LT1007M, Low Noise, High Speed Precision Op Amp	2-57

Note: '92DB = LTC's 1992 Databook Supplement and '94DB = LTC's 1994 Databook Volume III.

ALPHANUMERIC INDEX

LT1008C, Picoamp Input Current, Microvolt Offset Low Noise Op Amp	2-73
LT1008M, Picoamp Input Current, Microvolt Offset Low Noise Op Amp	2-73
LT1009C, 2.5 Volt Reference	3-27
LT1009M, 2.5 Volt Reference	3-27
LT1009S8, 2.5 Volt Reference	3-31
LT1010C, Fast $\pm 150\text{mA}$ Power Buffer	2-85
LT1010M, Fast $\pm 150\text{mA}$ Power Buffer	2-85
LT1011AC, Voltage Comparator	6-9
LT1011AM, Voltage Comparator	6-9
LT1011C, Voltage Comparator	6-9
LT1011M, Voltage Comparator	6-9
LT1012AC, Picoamp Input Current, Microvolt Offset Low Noise Op Amp	2-105
LT1012AM, Picoamp Input Current, Microvolt Offset Low Noise Op Amp	2-105
LT1012C, Picoamp Input Current, Microvolt Offset Low Noise Op Amp	2-105
LT1012M, Picoamp Input Current, Microvolt Offset Low Noise Op Amp	2-105
LT1012S8, Picoamp Input Current, Microvolt Offset Low Noise Op Amp	2-117
LT1013AC, Dual Precision Operational Amplifier	'92DB 2-19
LT1013AM, Dual Precision Operational Amplifier	'92DB 2-19
LT1013C, Dual Precision Operational Amplifier	'92DB 2-19
LT1013D, Dual Precision Operational Amplifier	'92DB 2-19
LT1013M, Dual Precision Operational Amplifier	'92DB 2-19
LT1013DS8, Dual Precision Operational Amplifier	'92DB 2-19
LT1014AC, Quad Precision Operational Amplifier	'92DB 2-19
LT1014AM, Quad Precision Operational Amplifier	'92DB 2-19
LT1014C, Quad Precision Operational Amplifier	'92DB 2-19
LT1014D, Quad Precision Operational Amplifier	'92DB 2-19
LT1014M, Quad Precision Operational Amplifier	'92DB 2-19
LT1015C, High Speed Dual Line Receiver	'92DB 10-4
LT1015M, High Speed Dual Line Receiver	'92DB 10-4
LT1016C, Ultra Fast Precision Comparator	6-25
LT1016M, Ultra Fast Precision Comparator	6-25
LT1016CS8, Ultra Fast Precision Comparator	6-41
LT1017C, Micropower Dual Comparator	'94DB 10-4
LT1017M, Micropower Dual Comparator	'94DB 10-4
LT1018C, Micropower Dual Comparator	'94DB 10-4
LT1018M, Micropower Dual Comparator	'94DB 10-4
LT1019AC, Precision Reference	3-33
LT1019AM, Precision Reference	3-33
LT1019C, Precision Reference	3-33
LT1019M, Precision Reference	3-33
LT1020C, Micropower Regulator and Comparator	4-29
LT1020M, Micropower Regulator and Comparator	4-29
LT1020CS, Micropower Regulator and Comparator	4-45
LT1021BC, Precision Reference	3-41
LT1021BM, Precision Reference	3-41

Note: '92DB = LTC's 1992 Databook Supplement and '94DB = LTC's 1994 Databook Volume III.

ALPHANUMERIC INDEX

LT1021CC, Precision Reference	3-41
LT1021CM, Precision Reference	3-41
LT1021DC, Precision Reference	3-41
LT1021DM, Precision Reference	3-41
LT1021DCS8, Precision Reference	3-57
LT1022AC, High Speed, Precision JFET Input Op Amp	2-145
LT1022AM, High Speed, Precision JFET Input Op Amp	2-145
LT1022C, High Speed, Precision JFET Input Op Amp	2-145
LT1022M, High Speed, Precision JFET Input Op Amp	2-145
LT1024AC, Dual, Matched Picoampere, Microvolt Input, Low Noise Op Amp	2-153
LT1024AM, Dual, Matched Picoampere, Microvolt Input, Low Noise Op Amp	2-153
LT1024C, Dual, Matched Picoampere, Microvolt Input, Low Noise Op Amp	2-153
LT1024M, Dual, Matched Picoampere, Microvolt Input, Low Noise Op Amp	2-153
LT1025AC, Micropower Thermocouple Cold Junction Compensator	11-7
LT1025AM, Micropower Thermocouple Cold Junction Compensator	11-7
LT1025C, Micropower Thermocouple Cold Junction Compensator	11-7
LT1025M, Micropower Thermocouple Cold Junction Compensator	11-7
LT1026C, Voltage Converter	5-3
LT1026M, Voltage Converter	5-3
LT1027BC, Precision 5V Reference	'92DB 7-6
LT1027BM, Precision 5V Reference	'92DB 7-6
LT1027CC, Precision 5V Reference	'92DB 7-6
LT1027CM, Precision 5V Reference	'92DB 7-6
LT1028AC, Ultra-Low Noise Precision High Speed Op Amp	'94DB 2-12
LT1028AM, Ultra-Low Noise Precision High Speed Op Amp	'94DB 2-12
LT1028C, Ultra-Low Noise Precision High Speed Op Amp	'94DB 2-12
LT1028M, Ultra-Low Noise Precision High Speed Op Amp	'94DB 2-12
LT1029AC, 5 Volt Bandgap Reference	3-61
LT1029AM, 5 Volt Bandgap Reference	3-61
LT1029C, 5 Volt Bandgap Reference	3-61
LT1029M, 5 Volt Bandgap Reference	3-61
LT1030C, Quad Low Power Line Driver	10-5
LT1030M, Quad Low Power Line Driver	10-5
LT1030CS, Quad Low Power Line Driver	10-9
LT1031BC, Precision 10 Volt Reference	3-65
LT1031BM, Precision 10 Volt Reference	3-65
LT1031CC, Precision 10 Volt Reference	3-65
LT1031CM, Precision 10 Volt Reference	3-65
LT1031DC, Precision 10 Volt Reference	3-65
LT1031DM, Precision 10 Volt Reference	3-65
LT1032C, Quad Low Power Line Driver	10-11
LT1032M, Quad Low Power Line Driver	10-11
LT1033C, 3 Amp Negative Adjustable Regulator	4-49
LT1033M, 3 Amp Negative Adjustable Regulator	4-49
LT1034BC, Micropower Dual Reference	'94DB 7-5

Note: '92DB = LTC's 1992 Databook Supplement and '94DB = LTC's 1994 Databook Volume III.

ALPHANUMERIC INDEX

LT1034BM, Micropower Dual Reference	'94DB	7-5
LT1034C, Micropower Dual Reference	'94DB	7-5
LT1034M, Micropower Dual Reference	'94DB	7-5
LT1035C, Logic Controlled Regulator		4-57
LT1035M, Logic Controlled Regulator		4-57
LT1036C, Logic Controlled Regulator		4-69
LT1036M, Logic Controlled Regulator		4-69
LT1037AC, Low Noise, High Speed Precision Op Amp		2-57
LT1037AM, Low Noise, High Speed Precision Op Amp		2-57
LT1037C, Low Noise, High Speed Precision Op Amp		2-57
LT1037M, Low Noise, High Speed Precision Op Amp		2-57
LT1037CS, Low Noise, High Speed Precision Op Amp		2-69
LT1038C, 10 Amp Positive Adjustable Voltage Regulator		4-77
LT1038M, 10 Amp Positive Adjustable Voltage Regulator		4-77
LT1039C, RS232 Driver/Receiver with Shutdown		10-19
LT1039M, RS232 Driver/Receiver with Shutdown		10-19
LT1054C, Switched Capacitor Voltage Converter with Regulator	'94DB	4-26
LT1054M, Switched Capacitor Voltage Converter with Regulator	'94DB	4-26
LT1055AC, Precision, High Speed, JFET Input Op Amp		2-219
LT1055AM, Precision, High Speed, JFET Input Op Amp		2-219
LT1055C, Precision, High Speed, JFET Input Op Amp		2-219
LT1055M, Precision, High Speed, JFET Input Op Amp		2-219
LT1055S8, Precision, High Speed, JFET Input Op Amp		2-231
LT1056AC, Precision, High Speed, JFET Input Op Amp		2-219
LT1056AM, Precision, High Speed, JFET Input Op Amp		2-219
LT1056C, Precision, High Speed, JFET Input Op Amp		2-219
LT1056M, Precision, High Speed, JFET Input Op Amp		2-219
LT1056S8, Precision, High Speed, JFET Input Op Amp		2-231
LT1057AC, Dual JFET Input Precision, High Speed Op Amp		2-235
LT1057AM, Dual JFET Input Precision, High Speed Op Amp		2-235
LT1057C, Dual JFET Input Precision, High Speed Op Amp		2-235
LT1057M, Dual JFET Input Precision, High Speed Op Amp		2-235
LT1058AC, Quad JFET Input Precision, High Speed Op Amp		2-235
LT1058AM, Quad JFET Input Precision, High Speed Op Amp		2-235
LT1058C, Quad JFET Input Precision, High Speed Op Amp		2-235
LT1058M, Quad JFET Input Precision, High Speed Op Amp		2-235
LT1070C, 5A High Efficiency Switching Regulator		5-37
LT1070HVC, 5A High Efficiency Switching Regulator		5-37
LT1070HVM, 5A High Efficiency Switching Regulator		5-37
LT1070M, 5A High Efficiency Switching Regulator		5-37
LT1071C, 2.5A High Efficiency Switching Regulator		5-37
LT1071HVC, 2.5A High Efficiency Switching Regulator		5-37
LT1071HVM, 2.5A High Efficiency Switching Regulator		5-37
LT1071M, 2.5A High Efficiency Switching Regulator		5-37
LT1072C, 1.25A High Efficiency Switching Regulator	'94DB	4-232

Note: '92DB = LTC's 1992 Databook Supplement and '94DB = LTC's 1994 Databook Volume III.

ALPHANUMERIC INDEX

LT1072HVC, 1.25A High Efficiency Switching Regulator	'94DB	4-232
LT1072HVM, 1.25A High Efficiency Switching Regulator	'94DB	4-232
LT1072M, 1.25A High Efficiency Switching Regulator	'94DB	4-232
LT1074C, Switching Regulator	'94DB	4-243
LT1074HVC, Switching Regulator	'94DB	4-243
LT1074HVM, Switching Regulator	'94DB	4-243
LT1074M, Switching Regulator	'94DB	4-243
LT1077, Micropower, Single Supply, Precision Operational Amplifier	'92DB	2-45
LT1078AC, Micropower, Dual, Single Supply, Precision Operational Amplifier	'92DB	2-56
LT1078AM, Micropower, Dual, Single Supply, Precision Operational Amplifier	'92DB	2-56
LT1078C, Micropower, Dual, Single Supply, Precision Operational Amplifier	'92DB	2-56
LT1078M, Micropower, Dual, Single Supply, Precision Operational Amplifier	'92DB	2-56
LT1079AC, Micropower, Quad, Single Supply, Precision Operational Amplifier	'92DB	2-56
LT1079AM, Micropower, Quad, Single Supply, Precision Operational Amplifier	'92DB	2-56
LT1079C, Micropower, Quad, Single Supply, Precision Operational Amplifier	'92DB	2-56
LT1079M, Micropower, Quad, Single Supply, Precision Operational Amplifier	'92DB	2-56
LT1080C, Advanced Low Power 5V RS232 Dual Driver/Receiver	Refer to LT1180A	'94DB 5-27
LT1080CS, Advanced Low Power 5V RS232 Dual Driver/Receiver	Refer to LT1180A	'94DB 5-27
LT1080M, Advanced Low Power 5V RS232 Dual Driver/Receiver	Refer to LT1180A	'94DB 5-27
LT1081C, Advanced Low Power 5V RS232 Dual Driver/Receiver	Refer to LT1181A	'94DB 5-27
LT1081CS, Advanced Low Power 5V RS232 Dual Driver/Receiver	Refer to LT1181A	'94DB 5-27
LT1081M, Advanced Low Power 5V RS232 Dual Driver/Receiver	Refer to LT1181A	'94DB 5-27
LT1083C, 7.5A Low Dropout Positive Adjustable Regulator	'94DB	4-48
LT1083M, 7.5A Low Dropout Positive Adjustable Regulator	'94DB	4-48
LT1083-5, 7.5A Low Dropout Positive Fixed 5V Regulator	'94DB	4-61
LT1083-12, 7.5A Low Dropout Positive Fixed 12V Regulator	'94DB	4-61
LT1084C, 5A Low Dropout Positive Adjustable Regulator	'94DB	4-48
LT1084M, 5A Low Dropout Positive Adjustable Regulator	'94DB	4-48
LT1084-5, 5A Low Dropout Positive Fixed 5V Regulator	'94DB	4-61
LT1084-12, 5A Low Dropout Positive Fixed 12V Regulator	'94DB	4-61
LT1085C, 3A Low Dropout Positive Adjustable Regulator	'94DB	4-48
LT1085M, 3A Low Dropout Positive Adjustable Regulator	'94DB	4-48
LT1085-5, 3A Low Dropout Positive Fixed 5V Regulator	'94DB	4-61
LT1085-12, 3A Low Dropout Positive Fixed 12V Regulator	'94DB	4-61
LT1086C, 1.5A Low Dropout Positive Adjustable Regulator	'94DB	4-72
LT1086M, 1.5A Low Dropout Positive Adjustable Regulator	'94DB	4-72
LT1086-5, 1.5A Low Dropout Positive Fixed 5V Regulator	'94DB	4-72
LT1086-12, 1.5A Low Dropout Positive Fixed 12V Regulator	'94DB	4-72
LT1087C, Adjustable Low Dropout Regulator with Kelvin-Sense Inputs	'92DB	4-56
LT1087M, Adjustable Low Dropout Regulator with Kelvin-Sense Inputs	'92DB	4-56
LT1088C, Wideband RMS-DC Converter Building Block		11-33
LT1089C, High Side Switch		11-45
LT1089M, High Side Switch		11-45
LT1101AC, Precision, Micropower, Single Supply Instrumentation Amplifier (Fixed Gain = 10 or 100)	'92DB	3-11
LT1101AM, Precision, Micropower, Single Supply Instrumentation Amplifier (Fixed Gain = 10 or 100)	'92DB	3-11

Note: '92DB = LTC's 1992 Databook Supplement and '94DB = LTC's 1994 Databook Volume III.

ALPHANUMERIC INDEX

LT1101C, Precision, Micropower, Single Supply Instrumentation Amplifier (Fixed Gain = 10 or 100)	'92DB	3-11
LT1101M, Precision, Micropower, Single Supply Instrumentation Amplifier (Fixed Gain = 10 or 100)	'92DB	3-11
LT1102, High Speed, Precision, JFET Input Instrumentation Amplifier (Fixed Gain = 10 or 100)	'92DB	3-23
LT1120C, Micropower Regulator with Comparator and Shutdown	'94DB	4-96
LT1130C, 5-Driver/5-Receiver RS232 Transceiver	Refer to LT1130A	'94DB 5-10
LT1130M, 5-Driver/5-Receiver RS232 Transceiver	Refer to LT1130A	'94DB 5-10
LT1131C, 5-Driver/4-Receiver RS232 Transceiver with Shutdown	Refer to LT1131A	'94DB 5-10
LT1131M, 5-Driver/4-Receiver RS232 Transceiver with Shutdown	Refer to LT1131A	'94DB 5-10
LT1132C, 5-Driver/3-Receiver RS232 Transceiver	Refer to LT1132A	'94DB 5-10
LT1132M, 5-Driver/3-Receiver RS232 Transceiver	Refer to LT1132A	'94DB 5-10
LT1133C, 3-Driver/5-Receiver RS232 Transceiver	Refer to LT1133A	'94DB 5-10
LT1133M, 3-Driver/5-Receiver RS232 Transceiver	Refer to LT1133A	'94DB 5-10
LT1134C, 4-Driver/4-Receiver RS232 Transceiver	Refer to LT1134A	'94DB 5-10
LT1134M, 4-Driver/4-Receiver RS232 Transceiver	Refer to LT1134A	'94DB 5-10
LT1135C, 5-Driver/3-Receiver RS232 Transceiver without Charge Pump	Refer to LT1135A	'94DB 5-10
LT1135M, 5-Driver/3-Receiver RS232 Transceiver without Charge Pump	Refer to LT1135A	'94DB 5-10
LT1136C, 4-Driver/5-Receiver RS232 Transceiver with Shutdown	Refer to LT1136A	'94DB 5-10
LT1136M, 4-Driver/5-Receiver RS232 Transceiver with Shutdown	Refer to LT1136A	'94DB 5-10
LT1137C, 3-Driver/5-Receiver RS232 Transceiver with Shutdown	Refer to LT1137A	'94DB 5-20
LT1137M, 3-Driver/5-Receiver RS232 Transceiver with Shutdown	Refer to LT1137A	'94DB 5-20
LT1138C, 5-Driver/3-Receiver RS232 Transceiver with Shutdown	Refer to LT1138A	'94DB 5-10
LT1138M, 5-Driver/3-Receiver RS232 Transceiver with Shutdown	Refer to LT1138A	'94DB 5-10
LT1139C, 4-Driver/4-Receiver RS232 Transceiver with Shutdown	Refer to LT1139A	'94DB 5-10
LT1139M, 4-Driver/4-Receiver RS232 Transceiver with Shutdown	Refer to LT1139A	'94DB 5-10
LT1140C, 5-Driver/3-Receiver RS232 Transceiver without Charge Pump	Refer to LT1140A	'94DB 5-10
LT1140M, 5-Driver/3-Receiver RS232 Transceiver without Charge Pump	Refer to LT1140A	'94DB 5-10
LT1141C, 3-Driver/5-Receiver RS232 Transceiver without Charge Pump	Refer to LT1141A	'94DB 5-10
LT1141M, 3-Driver/5-Receiver RS232 Transceiver without Charge Pump	Refer to LT1141A	'94DB 5-10
LT1170C, 100kHz, 5A High Efficiency Switching Regulator	'94DB	4-433
LT1170HVC, 5A High Efficiency 100kHz Switching Regulator	'94DB	4-433
LT1170HVM, 5A High Efficiency 100kHz Switching Regulator	'94DB	4-433
LT1170M, 5A High Efficiency 100kHz Switching Regulator	'94DB	4-433
LT1171C, 2.5A High Efficiency 100kHz Switching Regulator	'94DB	4-433
LT1171HVC, 2.5A High Efficiency 100kHz Switching Regulator	'94DB	4-433
LT1171HVM, 2.5A High Efficiency 100kHz Switching Regulator	'94DB	4-433
LT1171M, 2.5A High Efficiency 100kHz Switching Regulator	'94DB	4-433
LT1172C, 1.25A High Efficiency 100KHZ Switching Regulator	'94DB	4-433
LT1172HVC, 1.25A High Efficiency 100KHZ Switching Regulator	'94DB	4-433
LT1172HVM, 1.25A High Efficiency 100KHZ Switching Regulator	'94DB	4-433
LT1172M, 1.25A High Efficiency 100KHZ Switching Regulator	'94DB	4-433
LT1178AC, 17 μ A Max, Dual, Single Supply, Precision Operational Amplifier	'92DB	2-112
LT1178AM, 17 μ A Max, Dual, Single Supply, Precision Operational Amplifier	'92DB	2-112
LT1178C, 17 μ A Max, Dual, Single Supply, Precision Operational Amplifier	'92DB	2-112
LT1178M, 17 μ A Max, Dual, Single Supply, Precision Operational Amplifier	'92DB	2-112
LT1179AC, 17 μ A Max, Quad, Single Supply, Precision Operational Amplifier	'92DB	2-112

Note: '92DB = LTC's 1992 Databook Supplement and '94DB = LTC's 1994 Databook Volume III.

ALPHANUMERIC INDEX

LT1179AM, 17 μ A Max, Quad, Single Supply, Precision Operational Amplifier	'92DB	2-112
LT1179C, 17 μ A Max, Quad, Single Supply, Precision Operational Amplifier	'92DB	2-112
LT1179M, 17 μ A Max, Quad, Single Supply, Precision Operational Amplifier	'92DB	2-112
LT1180C, Advanced Low Power 5V RS232 Dual Driver/Receiver with Small Capacitors	Refer to LT1180A	'94DB 5-27
LT1180M, Advanced Low Power 5V RS232 Dual Driver/Receiver with Small Capacitors	Refer to LT1180A	'94DB 5-27
LT1181C, Advanced Low Power 5V RS232 Dual Driver/Receiver with Small Capacitors	Refer to LT1181A	'94DB 5-27
LT1181M, Advanced Low Power 5V RS232 Dual Driver/Receiver with Small Capacitors	Refer to LT1181A	'94DB 5-27
LT1188C, 1.5A High Side Switch	'92DB	4-48
LT1188M, 1.5A High Side Switch	'92DB	4-48
LT1280C, Advanced Low Power 5V RS232 Dual Driver/Receiver	Refer to LT1280A	'94DB 5-41
LT1280M, Advanced Low Power 5V RS232 Dual Driver/Receiver	Refer to LT1280A	'94DB 5-41
LT1281C, Advanced Low Power 5V RS232 Dual Driver/Receiver	Refer to LT1281A	'94DB 5-41
LT1281M, Advanced Low Power 5V RS232 Dual Driver/Receiver	Refer to LT1281A	'94DB 5-41
LT1431C, Programmable Reference	'92DB	7-13
LT1431M, Programmable Reference	'92DB	7-13
LT1524, Regulating Pulse Width Modulator		5-85
LT1525A, Regulating Pulse Width Modulator		5-97
LT1526, Regulating Pulse Width Modulator		5-105
LT1527A, Regulating Pulse Width Modulator		5-97
LT1846, Current Mode PWM Controller		5-113
LT1847, Current Mode PWM Controller		5-113
LT3524, Regulating Pulse Width Modulator		5-85
LT3525A, Regulating Pulse Width Modulator		5-97
LT3526, Regulating Pulse Width Modulator		5-105
LT3527A, Regulating Pulse Width Modulator		5-97
LT3846, Current Mode PWM Controller		5-113
LT3847, Current Mode PWM Controller		5-113
LTC201AC, Quad CMOS SPST Low Charge Injection Analog Switch	'92DB	11-4
LTC201AM, Quad CMOS SPST Low Charge Injection Analog Switch	'92DB	11-4
LTC201C, Quad CMOS SPST Low Charge Injection Analog Switch	'92DB	11-4
LTC201M, Quad CMOS SPST Low Charge Injection Analog Switch	'92DB	11-4
LTC1040C, Dual Micropower Comparator		6-57
LTC1040M, Dual Micropower Comparator		6-57
LTC1041C, BANG-BANG Controller		6-69
LTC1041M, BANG-BANG Controller		6-69
LTC1042C, Window Comparator		6-77
LTC1042M, Window Comparator		6-77
LTC1043C, Dual Precision Instrumentation Switched Capacitor Building Block		11-15
LTC1043M, Dual Precision Instrumentation Switched Capacitor Building Block		11-15
LTC1043CS, Dual Precision Instrumentation Switched Capacitor Building Block		11-31
LTC1044C, Switched Capacitor Voltage Converter		5-9
LTC1044CS8, Switched Capacitor Voltage Converter		5-21
LTC1044M, Switched Capacitor Voltage Converter		5-9
LTC1045C, Programmable Micropower Hex Translator/Receiver/Driver		10-27
LTC1045M, Programmable Micropower Hex Translator/Receiver/Driver		10-27

Note: '92DB = LTC's 1992 Databook Supplement and '94DB = LTC's 1994 Databook Volume III.

ALPHANUMERIC INDEX

LTC1049C, Low Power Zero Drift Operational Amplifier with Internal Capacitors	'92DB	2-299
LTC1049M, Low Power Zero Drift Operational Amplifier with Internal Capacitors	'92DB	2-299
LTC1050AC, Precision Zero Drift Op Amp with Internal Capacitors		2-181
LTC1050AM, Precision Zero Drift Op Amp with Internal Capacitors		2-181
LTC1050C, Precision Zero Drift Op Amp with Internal Capacitors		2-181
LTC1050M, Precision Zero Drift Op Amp with Internal Capacitors		2-181
LTC1051C, Dual Precision Zero Drift Operational Amplifier with Internal Capacitors	'92DB	2-306
LTC1051M, Dual Precision Zero Drift Operational Amplifier with Internal Capacitors	'92DB	2-306
LTC1052C, Chopper Stabilized Op Amp		2-197
LTC1052CS, Chopper Stabilized Op Amp		2-217
LTC1052M, Chopper Stabilized Op Amp		2-197
LTC1059AC, High Performance Switched Capacitor Universal Filter		7-3
LTC1059AM, High Performance Switched Capacitor Universal Filter		7-3
LTC1059C, High Performance Switched Capacitor Universal Filter		7-3
LTC1059CS, High Performance Switched Capacitor Universal Filter		7-11
LTC1059M, High Performance Switched Capacitor Universal Filter		7-3
LTC1060AC, Universal Dual Filter Building Block		7-15
LTC1060AM, Universal Dual Filter Building Block		7-15
LTC1060C, Universal Dual Filter Building Block		7-15
LTC1060CS, Universal Dual Filter Building Block		7-35
LTC1060M, Universal Dual Filter Building Block		7-15
LTC1061AC, High Performance Triple Universal Filter Building Block		7-39
LTC1061AM, High Performance Triple Universal Filter Building Block		7-39
LTC1061C, High Performance Triple Universal Filter Building Block		7-39
LTC1061CS, High Performance Triple Universal Filter Building Block		7-55
LTC1061M, High Performance Triple Universal Filter Building Block		7-39
LTC1062C, 5th Order Lowpass Filter	'94DB	8-5
LTC1062CS, 5th Order Lowpass Filter	'94DB	8-5
LTC1062M, 5th Order Lowpass Filter	'94DB	8-5
LTC1064C, Low Noise, Fast, Quad Universal Filter Building Block		7-73
LTC1064M, Low Noise, Fast, Quad Universal Filter Building Block		7-73
LTC1064-1C, Low Noise, 8th Order, Clock Sweepable Elliptic Lowpass Filter		7-89
LTC1064-1M, Low Noise, 8th Order, Clock Sweepable Elliptic Lowpass Filter		7-89
LTC1064-2C, Low Noise, High Frequency, 8th Order Butterworth Lowpass Filter	'92DB	8-5
LTC1064-2M, Low Noise, High Frequency, 8th Order Butterworth Lowpass Filter	'92DB	8-5
LTC1064-3, Low Noise, High Frequency, 8th Order Linear Phase Lowpass Filter	'92DB	8-13
LTC1064-4, Low Noise, 8th Order, Clock Sweepable Cauer Lowpass Filter	'92DB	8-21
LTC1090AC, Single Chip 10-Bit Data Acquisition System		9-5
LTC1090AM, Single Chip 10-Bit Data Acquisition System		9-5
LTC1090C, Single Chip 10-Bit Data Acquisition System		9-5
LTC1090M, Single Chip 10-Bit Data Acquisition System		9-5
LTC1091AC, 1-Channel, 10-Bit Serial I/O Data Acquisition System		9-29
LTC1091AM, 1-Channel, 10-Bit Serial I/O Data Acquisition System		9-29
LTC1091C, 1-Channel, 10-Bit Serial I/O Data Acquisition System		9-29
LTC1091M, 1-Channel, 10-Bit Serial I/O Data Acquisition System		9-29

Note: '92DB = LTC's 1992 Databook Supplement and '94DB = LTC's 1994 Databook Volume III.

LTC1092AC, 2-Channel, 10-Bit Serial I/O Data Acquisition System	9-29
LTC1092AM, 2-Channel, 10-Bit Serial I/O Data Acquisition System	9-29
LTC1092C, 2-Channel, 10-Bit Serial I/O Data Acquisition System	9-29
LTC1092M, 2-Channel, 10-Bit Serial I/O Data Acquisition System	9-29
LTC1093AC, 6-Channel, 10-Bit Serial I/O Data Acquisition System	9-29
LTC1093AM, 6-Channel, 10-Bit Serial I/O Data Acquisition System	9-29
LTC1093C, 6-Channel, 10-Bit Serial I/O Data Acquisition System	9-29
LTC1093M, 6-Channel, 10-Bit Serial I/O Data Acquisition System	9-29
LTC1094AC, 8-Channel, 10-Bit Serial I/O Data Acquisition System	9-29
LTC1094AM, 8-Channel, 10-Bit Serial I/O Data Acquisition System	9-29
LTC1094C, 8-Channel, 10-Bit Serial I/O Data Acquisition System	9-29
LTC1094M, 8-Channel, 10-Bit Serial I/O Data Acquisition System	9-29
LTC1095BC, Complete 10-Bit Data Acquisition System with On Board Reference	9-57
LTC1095BM, Complete 10-Bit Data Acquisition System with On Board Reference	9-57
LTC1095CC, Complete 10-Bit Data Acquisition System with On Board Reference	9-57
LTC1095CM, Complete 10-Bit Data Acquisition System with On Board Reference	9-57
LTC1099AC, High Speed 8-Bit A/D Converter with Built-In Sample-and-Hold	9-81
LTC1099AM, High Speed 8-Bit A/D Converter with Built-In Sample-and-Hold	9-81
LTC1099C, High Speed 8-Bit A/D Converter with Built-In Sample-and-Hold	9-81
LTC1099M, High Speed 8-Bit A/D Converter with Built-In Sample-and-Hold	9-81
LTC1100, Precision, Zero-Drift, Instrumentation Amplifier	'92DB 3-4
LTC1150C, $\pm 15V$ Chopper Stabilized Op Amp with Internal Capacitors	'92DB 2-32
LTC1150M, $\pm 15V$ Chopper Stabilized Op Amp with Internal Capacitors	'92DB 2-32
LTC1290BC, Single Chip 12-Bit Data Acquisition System	'92DB 6-67
LTC1290BM, Single Chip 12-Bit Data Acquisition System	'92DB 6-67
LTC1290CC, Single Chip 12-Bit Data Acquisition System	'92DB 6-67
LTC1290CM, Single Chip 12-Bit Data Acquisition System	'92DB 6-67
LTC1291, 1-Channel, 12-Bit Serial I/O Data Acquisition System	'94DB 6-163
LTC1292, 2-Channel, 12-Bit Serial I/O Data Acquisition System	'94DB 6-182
LTC1293, 6-Channel, 12-Bit Serial I/O 12-Bit Data Acquisition System	'92DB 6-113
LTC1294, 8-Channel, 12-Bit Serial I/O 12-Bit Data Acquisition System	'92DB 6-113
LTC7652C, Chopper Stabilized Op Amp	2-197
LTC7660, Switched Capacitor Voltage Converter	5-9
LTKA00C, Thermocouple Cold Junction Compensator and Matched Amplifier	11-3
LTKA00M, Thermocouple Cold Junction Compensator and Matched Amplifier	11-3
LTKA01C, Thermocouple Cold Junction Compensator and Matched Amplifier	11-3
LTKA01M, Thermocouple Cold Junction Compensator and Matched Amplifier	11-3
LTk001AC, Thermocouple Cold Junction Compensator and Matched Amplifier	11-3
LTk001AM, Thermocouple Cold Junction Compensator and Matched Amplifier	11-3
LTk001C, Thermocouple Cold Junction Compensator and Matched Amplifier	11-3
LTk001M, Thermocouple Cold Junction Compensator and Matched Amplifier	11-3
LTZ1000AC, Ultra Precision Reference	3-9
LTZ1000C, Ultra Precision Reference	3-9
OP-05, Internally Compensated Op Amp	2-321
OP-05A, Internally Compensated Op Amp	2-321

Note: '92DB = LTC's 1992 Databook Supplement and '94DB = LTC's 1994 Databook Volume III.

ALPHANUMERIC INDEX

OP-05C, Internally Compensated Op Amp	2-321
OP-05E, Internally Compensated Op Amp	2-321
OP-07, Precision Op Amp	2-329
OP-07A, Precision Op Amp	2-329
OP-07C, Precision Op Amp	2-329
OP-07CS8, Precision Op Amp	2-337
OP-07D, Precision Op Amp	2-329
OP-07E, Precision Op Amp	2-329
OP-15A, Precision, High Speed JFET Input Op Amp	2-341
OP-15B, Precision, High Speed JFET Input Op Amp	2-341
OP-15C, Precision, High Speed JFET Input Op Amp	2-341
OP-15E, Precision, High Speed JFET Input Op Amp	2-341
OP-15F, Precision, High Speed JFET Input Op Amp	2-341
OP-15G, Precision, High Speed JFET Input Op Amp	2-341
OP-16A, Precision, High Speed JFET Input Op Amp	2-341
OP-16B, Precision, High Speed JFET Input Op Amp	2-341
OP-16C, Precision, High Speed JFET Input Op Amp	2-341
OP-16E, Precision, High Speed JFET Input Op Amp	2-341
OP-16F, Precision, High Speed JFET Input Op Amp	2-341
OP-16G, Precision, High Speed JFET Input Op Amp	2-341
OP-27A, Low Noise, Precision Op Amp	2-345
OP-27C, Low Noise, Precision Op Amp	2-345
OP-27E, Low Noise, Precision Op Amp	2-345
OP-27G, Low Noise, Precision Op Amp	2-345
OP-37A, Low Noise, High Speed Op Amp	2-345
OP-37C, Low Noise, High Speed Op Amp	2-345
OP-37E, Low Noise, High Speed Op Amp	2-345
OP-37G, Low Noise, High Speed Op Amp	2-345
OP-215A, Dual Precision JFET Input Op Amp	2-275
OP-215C, Dual Precision JFET Input Op Amp	2-275
OP-215E, Dual Precision JFET Input Op Amp	2-275
OP-215G, Dual Precision JFET Input Op Amp	2-275
OP-227A, Dual Matched, Low Noise Op Amp	2-357
OP-227C, Dual Matched, Low Noise Op Amp	2-357
OP-227E, Dual Matched, Low Noise Op Amp	2-357
OP-227G, Dual Matched, Low Noise Op Amp	2-357
OP-237A, Dual High Speed, Low Noise Op Amp	2-357
OP-237C, Dual High Speed, Low Noise Op Amp	2-357
OP-237E, Dual High Speed, Low Noise Op Amp	2-357
OP-237G, Dual High Speed, Low Noise Op Amp	2-357
REF-01, Precision Voltage Reference	3-125
REF-01A, Precision Voltage Reference	3-125
REF-01C, Precision Voltage Reference	3-125
REF-01E, Precision Voltage Reference	3-125
REF-01H, Precision Voltage Reference	3-125

Note: '92DB = LTC's 1992 Databook Supplement and '94DB = LTC's 1994 Databook Volume III.

REF-02, Precision Voltage Reference	3-125
REF-02A, Precision Voltage Reference	3-125
REF-02C, Precision Voltage Reference	3-125
REF-02D, Precision Voltage Reference	3-125
REF-02E, Precision Voltage Reference	3-125
REF-02H, Precision Voltage Reference	3-125
SG1524, Regulating Pulse Width Modulator	5-85
SG1525A, Regulating Pulse Width Modulator	5-97
SG1527A, Regulating Pulse Width Modulator	5-97
SG3524, Regulating Pulse Width Modulator	5-85
SG3524S, Regulating Pulse Width Modulator	5-93
SG3525A, Regulating Pulse Width Modulator	5-97
SG3527A, Regulating Pulse Width Modulator	5-97

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ALPHANUMERIC INDEX

SURFACE MOUNT PRODUCTS

LF398S8, Precision Sample and Hold Amplifier	9-113
LM318S8, High Speed Op Amp	2-319
LM334S8, Constant Current Source and Temperature Sensor	3-99
LM385S8-1.2, Micropower Voltage Reference	3-113
LM385S8-2.5, Micropower Voltage Reference	3-113
LT1001CS8, Precision Op Amp	2-23
LT1004CS8-1.2, Micropower Voltage Reference	3-25
LT1004CS8-2.5, Micropower Voltage Reference	3-25
LT1006S8, Precision Single Supply Op Amp	2-53
LT1007CS, Low Noise, High Speed Precision Op Amp	2-69
LT1009S8, 2.5 Volt Reference	3-31
LT1012S8, Picoamp Input Current, Microvolt Offset, Low Noise Op Amp	2-117
LT1013DS8, Dual Precision Op Amp	2-141
LT1016CS8, Ultra Fast Precision Comparator	6-41
LT1017CS, Micropower Dual Comparator	6-53
LT1018CS, Micropower Dual Comparator	6-53
LT1020CS, Micropower Regulator and Comparator	4-45
LT1021DCS8, Precision Reference	3-57
LT1028CS, Ultra-Low Noise Precision High Speed Op Amp	2-177
LT1030CS, Quad Low Power Line Driver	10-9
LT1034CS8-1.2, Micropower Dual Reference	3-81
LT1034CS8-2.5, Micropower Dual Reference	3-81
LT1037CS, Low Noise, High Speed Precision Op Amp	2-69
LT1054CS, Switched Capacitor Voltage Converter with Regulator	5-35
LT1054IS, Switched Capacitor Voltage Converter with Regulator	5-35
LT1055S8, Precision, High Speed, JFET Input Op Amp	2-231
LT1056S8, Precision, High Speed, JFET Input Op Amp	2-231
LT1057S, Dual JFET Input Precision High Speed Op Amp	2-247
LT1057IS, Dual JFET Input Precision High Speed Op Amp	2-247
LT1080CS, 5V Powered RS232 Driver/Receiver with Shutdown	10-51
LT1081CS, 5V Powered RS232 Driver/Receiver with Shutdown	10-51
LTC1043CS, Dual Precision Instrumentation Switched-Capacitor Building Block	11-31
LTC1044CS8, Switched Capacitor Voltage Converter	5-21
LTC1052CS, Chopper-Stabilized Op Amp (CSOA™)	2-217
LTC1059CS, High Performance Switched Capacitor Universal Filter	7-11
LTC1060CS, Universal Dual Filter Building Block	7-35
LTC1061CS, High Performance Triple Universal Filter Building Block	7-55
LTC1062CS, 5th Order Low Pass Filter	7-71
OP-07CS8, Precision Op Amp	2-337
SG3524S, Regulating Pulse Width Modulator	5-93

SECTION 1—GENERAL INFORMATION

1

SECTION 1—GENERAL INFORMATION

INDEX	1-2
GENERAL ORDERING INFORMATION	1-3
ALTERNATE SOURCE CROSS REFERENCE GUIDE	1-4

I. ORDER ENTRY

Orders for products contained herein should be directed to: LINEAR TECHNOLOGY CORPORATION, 1630 McCarthy Boulevard, Milpitas, California 95035. Phone: 408-432-1900.

II. ORDERING INFORMATION

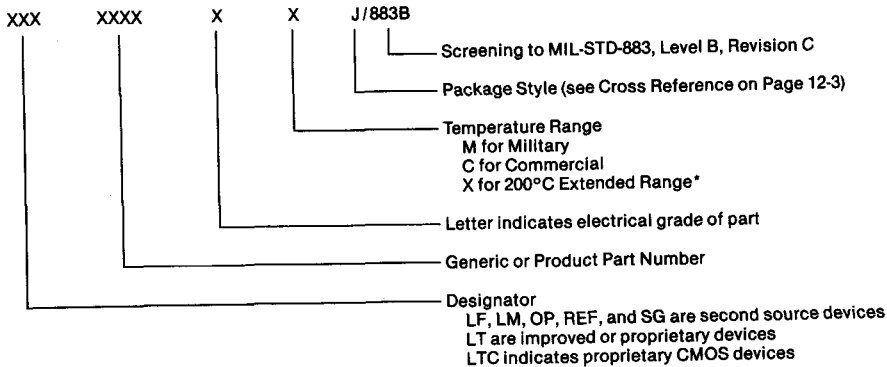
Minimum order value is \$2000.00 per order; minimum value per line item is \$500.00.
 Each item must be ordered using the complete part number exactly as listed on the datasheet.
 F.O.B.: Milpitas, California.

III. RELIABILITY PROGRAMS

Linear Technology Corporation currently offers the following Reliability Programs:

- A. JAN QPL devices.
- B. DESC drawings.
- C. MIL-STD-883, Level B, Revision C for all military temperature range devices.
- D. "R-Flow" Burn-In Program for commercial temperature range devices. Consult Factory regarding burn-in program.

IV. PART NUMBER EXPLANATION



V. PACKAGE SUFFIX EXPLANATION

Letter Designator	Description
D	14, 16, 18 and 20 Pin Side Brazed Hermetic DIP
D8	8 Pin Side Brazed Hermetic DIP
H	Multi Lead Metal Can
J	14, 16, 18 and 20 Pin Ceramic DIP
J8	8 Pin Ceramic DIP
K	TO-3 Metal Can (Steel)
N	14, 16, 18 and 20 Pin Molded DIP
N8	8 Pin Molded DIP
P	TO-3P Molded (3 lead)
S8	8 Lead Small Outline (SO) package (Note 1)
S	16, 18, 20 Pin Small Outline (SO) package (Note 1, 2)
T	TO-220 Molded (3 lead, 5 lead)
V	11 Pin Molded SIP
W	10 Pin Flatpack (Cerpak)
Z	TO-92 Molded (3 lead)

Note 1: Pin-out and electrical specifications may differ from standard commercial grade N8 package. See SO datasheet for specific information.

Note 2: These devices are delivered in either 150 MIL (SO) or 300 MIL (SO-L) wide packages depending on device die size. See specific SO datasheet for pin counts and package dimensions.

AMD		FSC P/N	LTC DIRECT REPL	INTERSIL P/N	LTC DIRECT REPL	MOTO P/N	LTC DIRECT REPL
AMD P/N	LTC DIRECT REPL						
AM685	LT685	μA108	LM108	LM111	LM111	MC1558	LT1013M*
AM686	LT1016	μA108A	LM1008M*		LT111A*	MC78T05	LM323T
LF155	LT155	μA111	LM108A	LM124	LT1011M*		LT323AT*
	LT1055M*		LT1008M*		LT1014M*	OP27A	OP27A
LF155A	LT155A		LM111				LT1007AM*
	LT1055AM*	μA117	LT111A*	MAXIM		OP27B	LT1007M*
LF156	LT156		LT1011M*			OP27C	OP27C
	LT1056M*		LT117A*				LT1007M
LF156A	LT156A	μA124	LT1014M*	AD7820	LTC1099*	OP27E	OP27E
	LT1056AM*	μA148	LT1014M*	ICL7850	LTC1052**	OP27F	LT1007AC*
LF198	LT198	μA308A	LM308A*	ICL7852	LTC7852	OP27G	LT1007C*
LF355A	LT355A		LM1008C**	MAX232	LTC1044**		LT1007C*
	LT1055AC*	μA311	LM311	MAX235	LT1081*	OP37A	OP37A
LF356A	LT356A		LT311A*	MAX237	LT1132**		LT1037AM*
	LT1056AC*		LT1011C*	MAX238	LT1134**	OP37B	LT1037M*
LF398	LT398	μA317	LM317	MAX239	LT1133**	OP37C	OP37C
LM108	LT108		LT317A*	MAX400	LT1001		LT1037M*
	LT1008M*	μA318	LM318	MAX430	LTC1050	OP37E	OP37E
LM108A	LT108A		LT318A*	MAX432	LTC1050		LT1037AC*
	LT1008M*	μA714	OP07	MAX680	LTC1026**	OP37F	LT1037C*
LM111	LT111		LT1001M*	MF10	LTC1060	OP37G	OP37G
	LT111A*	μA714C	OP07C	OP07			LT1037C*
	LT1011M*		LT1001C*	OP27	OP27	SG1524	SG1524
LM118	LT118	μA714E	OP07E	MOTOROLA			LT1524*
	LT118A*		LT1001C*			SG1525A	SG1525A
LM119	LT119	μA714L	OP07D	MOTO P/N	LTC DIRECT REPL		LT1525A*
	LT119A*		LT1001C*	LF155	LF155		LT1527A*
LM148	LT148	μA1558M	LT1013M*	LF155A	LT1055M	SG3524	SG3524
LM308A	LT308A				LT1055AM	SG3525A	SG3525A
	LM1008C*			LF156	LT1056M		LT3524*
LM311	LM311	HARRIS		LF156A	LT1056AM	SG3527A	SG3527A
	LT311A*	HARRIS P/N	LTC DIRECT REPL		LT156		LT3527A*
	LT1011C*	HA2510	LT118A**		LT1056M		
LM318	LM318		LM118**	LF156A	LT1056AM		
	LT318A*	HA2512	LT118A**		LT1056AM		
LM319	LM319		LM118A**	LF355A	LF355A	NATIONAL SEMICONDUCTOR	
	LT319A*	HA2515	LT318A**	LF356A	LF356A	NSC P/N	LTC DIRECT REPL
			LM318**	LM101A	LM101A		
		HA5130-2	OP07A	LM107	LM107	ADC032	LTC1091
			LT1001AM*	LM108	LM108	ADC0820	LTC1099*
		HA5130-5	OP07E	LM108	LM108M*	LF155	LF155
			LT1001C*	LM108A	LM108A	LF155A	LT1055M*
		HA5135-2	OP07		LT1008M*	LF156	LT1055AM*
			LT1001M*	LM111	LM111		LT1056M*
		HA5135-5	OP07C	LM117	LT111A*	LF156A	LT1022M*
			LT1001C*		LT1011M*		LT156A
		HAOP07	OP07	LM117	LM117		LT1056AM*
			LT1001M*	LM123	LT117A*		LT1056AM*
		HAOP07A	OP07A		LM123*		LT1022AM*
			LT1001AM*	LM124	LT1003M**	LF198	LF198
		HAOP07C	OP07C	LM137	LT1014M*	LF198A	LF198A
			LT1001C*		LT137A*	LF355A	LF355A
		HAOP07E	OP07E		LT1033M**		LT1055AC*
			LT1001C*	LM148	LT1033M**	LF356A	LF356A
				LM150	LT1014M*		LT1056AC*
		INTERSIL			LM150		LT1022AC*
		INTERSIL P/N	LTC DIRECT REPL	LM158	LT150A*	LF398	LF398
		ICL232	LT1081	LM158	LT1013M*	LF398A	LF398A
		ICL7650 8-Pin	LTC1050*	LM308A	LM308A	LF412A	LF412A
		ICL7652 8-Pin	LTC7852		LT1008C*	LH0002	LT1010M**
		ICL7660	LTC1044*	LM311	LM311	LH0044	LT1001M*
		ICL8069C	LM385-1.2		LT311A*	LH0070	LH0070
			LT1004C-1.2*	LM317	LT1011C*		LT1031M*
		ICL8069M	LM185-1.2		LM317	LH2108	LH2108
			LT1004M-1.2*	LM323	LT317A*	LH2108A	LH2108A
					LM323*	LM10	LM10
					LM323*	LM10B	LM10B
		LF155	LF155		LT323A**	LM10C	LM10C
		LF155A	LF155A	LM337	LT1003C**	LM101A	LM101A
		LF156	LF156		LM337*	LM107	LM107
		LF156A	LF156A		LM337*	LM108	LM108
		LF355A	LF355A	LM350	LT1033C**		
		LF356A	LF356A		LM350	LM108A	LM108A
		LH2108	LH2108		LT350A*		LT1008M*
		LH2108A	LH2108A		LT350A*		LT1008M*
		LM101A	LM101A	MC1400U2	LT1019CN8-2.5*		LT1008M*
		LM107	LM107	MC1400AU2	LT1019CN8-2.5**	LM111	LM111
		LM108	LM108	MC1400U5	LT1019CN8-5*		LT111A*
			LT1008M*	MC1400A5	LT1019CN8-5**	LM112	LT1011M*
		LM108A	LT1008M*	MC1400U10	LT1019CN8-10*	LM113	LT1012M*
				MC1400AU10	LT1019CN8-10**	LM117	LT1004M-1.2*
				MC145406	LT1039-16*	LM117	LM117
							LT117A*

*LTC Improved Replacement: 100% Pin-for-pin compatible with better electrical specifications.
 **Similar Device: Please consult the data sheet to determine the suitability of the replacement for specific applications.
 †Consult factory for guaranteed TC devices.

ALTERNATE SOURCE CROSS REFERENCE GUIDE

N5C P/N	LTC DIRECT REPL	N5C P/N	LTC DIRECT REPL	PMI P/N	LTC DIRECT REPL	PMI P/N	LTC DIRECT REPL
LM117HV	LM117HV LT117AHV*	LM338	LM338 LT338A*	OP16G	OP16G LT1056C*	PM2108A	LM2108A
LM118	LM118 LT118A*	LM350	LM350 LT350A*	OP27A	OP27A LT1007AM*	REF01	REF01 LT1019M-10*
LM119	LM119 LT119A*	LM368-5.0	LM368-5.0 LT1019AC-5*	OP27B	OP27B LT1007M*	REF01A	REF01A LT1021-10**
LM123	LM123 LT123A*	LM368Y-5.0	LM368Y-5.0 LT1019C-5**	OP27C	OP27C LT1007M*	REF01C	REF01C LT1019C-10*
LM124	LM124 LT1003M*	LM368Y-10.0	LM368Y-10.0 LT1019C-10**	OP27E	OP27E LT1007AC*	REF01E	REF01E LT1021-10**
LM129A	LM129A LM129B	LM385-1.2	LM385-1.2 LT1004C-1.2*	OP27F	OP27F LT1007C*	REF01H	REF01H LT1021-10**
LM129C	LM129C LM129M*	LM385-2.5	LM385-2.5 LT1004C-2.5*	OP27G	OP27G LT1007C*	REF01H	REF01H LT1019C-10*
LM133	LM133 LM134	LM385BX-1.2	LM385BX-1.2 LT1034BC-1.2*	OP37A	OP37A LT1037AM*	REF02	REF02 LT1019M-5*
LM134-3	LM134-3 LM134-6	LM385BY-1.2	LM385BY-1.2 LT1034C-1.2*	OP37B	OP37B LT1037M*	REF02A	REF02A LT1021-5**
LM136A	LM136A LT1009M*	LM385BY-2.5	LM385BY-2.5 LT1034BC-2.5*	OP37C	OP37C LT1037M*	REF02C	REF02C LT1021-5**
LM136-2.5	LM136-2.5 LT1009M*	LM396	LM396 LT1038C**	OP37E	OP37E LT1037AC*	REF02E	REF02E LT1021-5**
LM136-5	LM136-5 LT1029M**	LM399	LM399 LM399A	OP37F	OP37F LT1037AC*	REF02H	REF02H LT1019C-5*
LM137	LM137 LT1033M**	LM399A-20	LM399A-20 LM399A-50	OP37G	OP37G LT1037C*	REF03	REF03 LT1021-5**
LM137HV	LM137HV LT137AHV*	LM1524	LM1524 SG1524	OP77A	OP77A LT1011AM**		
LM138	LM138 LT138A*	LM2935	LM2935 LT1005**	OP77B	OP77B LT1001M**		
LM148	LM148 LT1014M*	LM3524	LM3524 SG3524	OP77C	OP77C LT1001AC**		
LM150	LM150 LT150A*	MF5	MF5 LTC1059*	OP77D	OP77D LT1001C**		
LM158	LM158 LT1013M*	MF10	MF10 LTC1060*	OP77E	OP77E LT1002M*		
LM188BY-5.0	LM188BY-5.0 LT1019M-5**	PMI		OP207A	OP207A LT1002M*	RAYTHEON	
LM188BY-10.0	LM188BY-10.0 LT1019M-10**	PMI P/N	LTC DIRECT REPL	OP207B	OP207B LT1002C*	RAYTH P/N	LTC DIRECT REPL
LM185-1.2	LM185-1.2 LT1004M-1.2*	CMP01	CMP01 LT1011**	OP207E	OP207E LT1002C*	LM101A	LM101A
LM185-2.5	LM185-2.5 LT1004M-2.5*	CMP02	CMP02 LT1011**	OP215A	OP215A LT1002C*	LM107	LM107
LM185BX-1.2	LM185BX-1.2 LT1034BM-1.2*	OP04	OP04 LT1013*	OP215B	OP215B LT1007AM*	LM111	LM111
LM185BY-1.2	LM185BY-1.2 LT1034M-1.2*	OP05	OP05 LT1001M*	OP215C	OP215C LT1007AM*	LM124	LM124
LM185BY-2.5	LM185BY-2.5 LT1034M-2.5*	OP05A	OP05A LT1001M*	OP215E	OP215E LT1007M*	LM148	LM148
LM196	LM196 LT1038M**	OP05C	OP05C LT1001M*	OP215F	OP215F LT1007M*	LM311	LM311
LM199	LM199 LT1008C*	OP05E	OP05E LT1001C*	OP215G	OP215G LT1007C*		
LM199A	LM199A LT1008C*	OP07	OP07 LT1001M*	OP220	OP220 LT1078**	OP05	OP05 LT1001M*
LM199A-20	LM199A-20 LT1008C*	OP07A	OP07A LT1001M*	OP221	OP221 LT1013*	OP05A	OP05A LT1001AM*
LM234-3	LM234-3 LT1008C*	OP07C	OP07C LT1001M*	OP222A	OP222A LT1013*	OP05C	OP05C LT1001C*
LM234-6	LM234-6 LT1008C*	OP07E	OP07E LT1001M*	OP222B	OP222B LT1013*	OP05E	OP05E LT1001C*
LM308A	LM308A LT1008C*	OP10	OP10 LT1002AM*	OP222C	OP222C LT1013*	OP07	OP07 LT1001M*
LM311	LM311 LT1011C*	OP10A	OP10A LT1002AM*	OP222D	OP222D LT1013*	OP07A	OP07A LT1001AM*
LM317	LM317 LT317A*	OP10C	OP10C LT1002C*	OP222E	OP222E LT1013*	OP07C	OP07C LT1001C*
LM317HV	LM317HV LT317AHV*	OP10E	OP10E LT1002C*	OP222F	OP222F LT1013*	OP07E	OP07E LT1001C*
LM318	LM318 LT318A*	OP11	OP11 LT1014*	OP222G	OP222G LT1013*	OP27A	OP27A LT1007AM*
LM319	LM319 LT319A*	OP12A	OP12A LT1012M*	OP222H	OP222H LT1013*	OP27B	OP27B LT1007M*
LM323	LM323 LT323A**	OP12B	OP12B LT1012M*	OP222I	OP222I LT1013*	OP27C	OP27C LT1007M*
LM329A	LM329A LT1003M**	OP12C	OP12C LT1012M*	OP222J	OP222J LT1013*	OP27E	OP27E LT1007AC*
LM329B	LM329B LT1003M**	OP12E	OP12E LT1012C*	OP222K	OP222K LT1013*	OP27F	OP27F LT1007C*
LM329C	LM329C LT1003M**	OP12F	OP12F LT1012C*	OP222L	OP222L LT1013*	OP27G	OP27G LT1007C*
LM329D	LM329D LT1003M**	OP12G	OP12G LT1012C*	OP222M	OP222M LT1013*	OP37A	OP37A LT1037AM*
LM333	LM333 LT1033C*	OP15A	OP15A LT1055AM*	OP222N	OP222N LT1013*	OP37B	OP37B LT1037M*
LM333A	LM333A LT1033C*	OP15B	OP15B LT1055M*	OP222O	OP222O LT1013*	OP37C	OP37C LT1037M*
LM334	LM334 LT1033C*	OP15C	OP15C LT1055M*	OP222P	OP222P LT1013*	OP37E	OP37E LT1037M*
LM336-2.5	LM336-2.5 LT1009C*	OP15E	OP15E LT1055M*	OP222Q	OP222Q LT1013*	OP37F	OP37F LT1037M*
LM336B-2.5	LM336B-2.5 LT1009C*	OP15F	OP15F LT1055AC*	OP222R	OP222R LT1013*		
LM336-5	LM336-5 LT1029C*	OP15G	OP15G LT1055C*	OP222S	OP222S LT1013*		
LM337	LM337 LT337A*	OP16A	OP16A LT1056AM*	OP222T	OP222T LT1013*		
LM337HV	LM337HV LT337AHV*	OP16B	OP16B LT1056M*	OP222U	OP222U LT1013*		
		OP16C	OP16C LT1056M*	OP222V	OP222V LT1013*		
		OP16E	OP16E LT1056AC*	OP222W	OP222W LT1013*		
		OP16F	OP16F LT1056C*	OP222X	OP222X LT1013*		

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 †Consult factory for guaranteed TC devices.

ALTERNATE SOURCE CROSS REFERENCE GUIDE

RAYTH P/N	LTC DIRECT REPL	SIL GEN P/N	LTC DIRECT REPL	TI P/N	LTC DIRECT REPL
OP37G	OP37G	SG1526	LT1526	OP27B	LT1007M*
RC714CH	LT1037C*	SG1527A	SG1527A	OP27C	OP27C
	OP07C		LT1527A*		LT1007M
RC714EH	LT1001C*	SG1558	LT1013M*	OP27E	OP27E
	OP07E	SG3524	SG3524		LT1007AC*
	LT1001C**		LT3524*	OP27F	LT1007C*
RM714H	OP07	SG3525A	SG3525A	OP27G	OP27G
	LT1001M*		LT3525A		LT1007C*
RM1558	LT1013M*	SG3526	LT3526	OP37A	OP37A
		SG3527A	SG3527A*		LT1037AM*
			LT3527A*	OP37B	LT1037M*
				OP37C	OP37C
SIGNETICS		TELEDYNE SEMICONDUCTOR			LT1037M*
SIGNETICS P/N LTC DIRECT REPL		TSC P/N LTC DIRECT REPL		OP37E	OP37E
LF398	LF398	TSC04	LM385-1.2		LT1037AC*
LF398A	LF398A	TSC05	LM385-2.5	OP37F	LT1037C*
LM101A	LM101A	TSC232	LT1080**	OP37G	OP37G
LM111	LM111		LT1081**		LT1037C*
	LT111A*	TSC911	LTC1050	SG1524	SG1524
	LT1011M*	TSC913	LT1078**		LT1524*
LM119	LM119	TSC914	LT1079**	SG1525A	SG1525A
	LT119A*	TSC918	LTC7652**		LT1525A*
LM124	LT1014M*	TSC7650	LTC1050	SG3524	SG3524
LM158	LT1013M*	TSC7652	LTC7652	SG3525A	SG3525A
LM311	LT311A*		LTC1052		LT3525A*
	LT1011C*	TSC7660	LTC1044*	UNITRODE	
MC1558	LT1013M*	TSC9491	LM385-1.2	UNITRODE P/N LTC DIRECT REPL	
NE1037	LT1037		REF02	UC117	LM117
NE5534	OP37*	TSC9495	LT1004C-1.2	UC137	LM137
	LT1037*		REF02		LM137*
NE5534A	OP37*		LT1019M-5		LT137A*
	LT1037*	TSC9496	LT1021-5**	UC150	LT1033M**
SE5534	OP37*		REF01E		LM150
	LT1037*		LT1021-10**	UC317	LM317
SE5534A	OP37*	TEXAS INSTRUMENTS		UC337	LM337
	LT1037*	TI P/N	LTC DIRECT REPL		LT337A*
SG3524	SG3524	LM101A	LM101A	UC350	LM350
	LT3524*	LM107	LM107	UC1524	SG1524
		LM108A	LM108A	UC1525A	SG1525A
		LM111	LM111	UC1527A	SG1527A
			LT111A*	UC1846	LT1846
			LT1011M*	UC1847	LT1847
			LT1014M*	UC3524	SG3524
			LT1014M*		LT3524*
			LT1013M*	UC3525A	SG3525A
			LM185-2.5	UC3527A	SG3527A
			LM311		LT3527A*
			LT311A*	UC3846	LT3846
			LT1011C*	UC3847	LT3847
			LM317KC		
			LM317T*		
			LM317AT*		
			LM318		
			LM318*		
			LM323		
			LM323*		
			LM350		
			LM350		
			LT1004		
			LT1007		
			LT1008		
			LT1008		
			LT1009		
			LT1009		
			LT1011		
			LT1011		
			LT1013		
			LT1016		
			LT1016		
			LT1028		
			LT1028		
			LT1037		
			LT1037		
			LT1070		
			LT1070		
			LTC1044		
			LTC1052		
			LTC1052		
			MC1558		
			LT1013M*		
			OP07C		
			OP077/14C		
			LT1001C*		
			OP077/14D		
			OP07D		
			LT1001C*		
			OP07E		
			OP077/14E		
			LT1001C*		
			OP27A		
			LT1007AM*		
SILICON GENERAL					
SIL GEN P/N	LTC DIRECT REPL				
SG101A	LM101A				
SG108	LM108				
	LT1008M*				
SG108A	LM108A				
	LT1008M*				
SG111	LM111				
	LT111A*				
	LT1011M*				
SG117	LM117				
SG117A	LT117A				
SG123	LM123				
SG123A	LT123A				
	LT1003M**				
SG124	LT1014M*				
SG137	LM137				
SG137A	LT137A				
	LT1033M**				
SG138	LM138				
SG138A	LT138A				
SG150	LM150				
SG150A	LT150A				
SG311	LM311				
	LT311A*				
	LT1011C*				
SG317	LM317				
SG317A	LT317A				
SG323	LM323				
SG323A	LT323A				
	LT1003C**				
SG337	LM337				
SG337A	LT337A				
	LT1033C**				
SG338	LM338				
SG338A	LT338A				
SG350	LM350				
SG350A	LT350A				
SG1524	SG1524				
	LT1524*				
SG1525A	SG1525A				
	LT1525A*				

*LTC Improved Replacement: 100% Pin-for-pin compatible with better electrical specifications.
 **Similar Device: Please consult the data sheet to determine the suitability of the replacement for specific applications.
 †Consult factory for guaranteed TC devices.

SECTION 2—OPERATIONAL AMPLIFIERS

2

SECTION 2—OPERATIONAL AMPLIFIERS

INDEX	2-2
SELECTION GUIDE	2-4
PROPRIETARY PRODUCTS	
LT1001, Precision Op Amp	2-11
LT1001CS8, Precision Op Amp	2-23
LT1002, Dual, Matched Precision Op Amp	2-25
LT1006, Precision, Single Supply Op Amp	2-41
LT1006S8, Precision, Single Supply Op Amp	2-53
LT1007, Low Noise, High Speed Precision Op Amp	2-57
LT1007CS/LT1037CS, Low Noise, High Speed Precision Op Amps	2-69
LT1008, Picoamp Input Current, Microvolt Offset, Low Noise Op Amp	2-73
LT1010, Fast $\pm 150\text{mA}$ Power Buffer	2-85
LT1012, Picoamp Input Current, Microvolt Offset, Low Noise Op Amp	2-105
LT1012S8, Picoamp Input Current, Microvolt Offset, Low Noise Op Amp	2-117
LT1013, Dual Precision Op Amp	2-121
LT1013DS8, Dual Precision Op Amp	2-141
LT1014, Quad Precision Op Amp	2-121
LT1022, High Speed, Precision JFET Input Op Amp	2-145
LT1024, Dual, Matched Picoampere, Microvolt Input, Low Noise Op Amp	2-153
LT1028, Ultra-Low Noise Precision High Speed Op Amp	2-161
LT1028CS, Ultra-Low Noise Precision High Speed Op Amp	2-177
LT1037, Low Noise, High Speed Precision Op Amp	2-57
LTC1049, Low Power Chopper Stabilized Op Amp with Internal Capacitors	13-10
LTC1050, Precision Chopper Stabilized Op Amp with Internal Capacitors	2-181
LTC1051, Dual Precision Chopper Stabilized Op Amp with Internal Capacitors	13-13
LTC1052, Chopper Stabilized Op Amp	2-197
LTC1052CS, Chopper Stabilized Op Amp (CSOA™)	2-217
LT1055, Precision, High Speed, JFET Input Op Amp	2-219
LT1056, Precision, High Speed, JFET Input Op Amp	2-219
LT1055S8/LT1056S8, Precision, High Speed, JFET Input Op Amps	2-231
LT1057, Dual JFET Input Precision, High Speed Op Amp	2-235
LT1057S/LT1057IS, Dual JFET Input Precision, High Speed Op Amp	2-247
LT1058, Quad JFET Input Precision, High Speed Op Amp	2-235
LT1077, Micropower, Single Supply, Precision Op Amp	13-27
LT1078, Micropower, Dual, Single Supply, Precision Op Amp	2-251
LT1079, Micropower, Quad, Single Supply, Precision Op Amp	2-251
LTC1100, Precision, Single Supply, Instrumentation Amplifier (Fixed Gain = 100)	13-35
LT1101, Precision, Micropower, Single Supply Instrumentation Amplifier (Fixed Gain = 10 or 100)	13-36
LT1102, High Speed, Precision, JFET Input Instrumentation Amplifier (Fixed Gain = 10 or 100)	13-48
LTC1150, $\pm 15\text{V}$ Chopper Stabilized Op Amp with Internal Capacitor	13-49
LT1178, 17 μA Max, Dual Single Supply, Precision Op Amp	2-267
LT1179, 17 μA Max, Quad Single Supply, Precision Op Amp	2-267

ENHANCED AND SECOND SOURCE PRODUCTS

LF155/LF355, JFET Input Op Amp, Low Supply Current	2-271
LF155A/LF355A, JFET Input Op Amp, Low Supply Current	2-271
LF156/LF356, JFET Input Op Amp, High Speed	2-271
LF156A/LF356A, JFET Input Op Amp, High Speed	2-271
LF412A, Dual Precision JFET Input Op Amp	2-275
LH2108A, Dual LM108 Op Amp	2-279
LM10/B(L)/C(L), Low Power Op Amp and Reference	2-281
LM101A/LM301A, Uncompensated General Purpose Op Amp	2-297
LM107/LM307, Compensated General Purpose Op Amp	2-297
LM108/LM308, Super Gain Op Amp	2-303
LM108A/LM308A, Super Gain Op Amp	2-303
LM118/LM318, High Slew Rate Op Amp	2-311
LM318S8, High Speed Op Amp	2-319
LT118A/LT318A, Improved LM118 Op Amp	2-311
LTC7652, Chopper-Stabilized Op Amp	2-197
OP-05, OP-05A, OP-05C, OP-05E, Internally Compensated Op Amp	2-321
OP-07, OP-07A, OP-07C, OP-07E, Precision Op Amp	2-329
OP-07CS8, Precision Op Amp	2-337
OP-15A, OP-15B, OP-15C, OP-15E, OP-15F, OP-15G, Precision, High Speed JFET Input Op Amp	2-341
OP-16A, OP-16B, OP-16C, OP-16E, OP-16F, OP-16G, Precision, High Speed JFET Input Op Amp	2-341
OP-27A, OP-27C, OP-27E, OP-27G, Low Noise, Precision Op Amp	2-345
OP-37A, OP-37C, OP-37E, OP-37G, Low Noise, High Speed Op Amp	2-345
OP-215, Dual Precision JFET Input Op Amp	2-275
OP-227A, OP-227C, OP-227E, OP-227G, Dual Matched, Low Noise Op Amp	2-357
OP-237A, OP-237C, OP-237E, OP-237G, Dual High Speed, Low Noise Op Amp	2-357

MILITARY

PART NUMBER	ELECTRICAL CHARACTERISTICS							IMPORTANT FEATURES
	V _{OS} MAX (μV)	TC V _{OS} (μV/°C)	I _B MAX (nA)	A _{VOL} MIN (V/mV)	SLEW RATE MIN (V/μs)	NOISE MAX 10Hz (nV/√Hz)	PACKAGES AVAILABLE	
SINGLE								
LT1001AM	15	0.6	2.0	450	0.15	18	H, J8	Extremely Low Offset Voltage Low Noise, Low Drift
LT1001M	60	1.0	3.8	400	0.15	18	H, J8	
LT1006AM	50	1.3	15	1000	0.25	24†	H, J8	Single Supply Operation, Fully Specified for +5V Supply
LT1006M	80	1.8	25	700	0.25	24†	H, J8	
LT1007AM	25	0.6	35	7000	1.7	4.5	H, J8	Extremely Low Noise, Low Drift
LT1007M	60	1.0	55	5000	1.7	4.5	H, J8	
LT1008M	120	1.5	0.1	200	0.1	30	H	Low Bias Current, Low Power
LT1010M	90mV	0.6mV/°C†	150μA	0.995	75	90†	H, K	High Speed Buffer, Drives ±10V into 75Ω
LT1012M	35	1.5	0.1	200	0.1	30	H	Low V _{OS} , Low Power
LT1022AM	250	5.0	0.05	150	23	50	H	Very High Speed JFET Input Op Amp with Very Good DC Spec
LT1022M	600	9.0	0.05	120	18	60	H	
LT1028AM	40	0.8	90	7000	11	1.7	H, J8	Low Noise, High Speed, Low Drift
LT1028M	80	1.0	180	5000	11	1.9	H, J8	
LT1037AM	25	0.6	35	7000	11	4.5	H, J8	Extremely Low Noise, High Speed
LT1037M	60	1.0	55	5000	11	4.5	H, J8	
LT1055AM	150	4	0.05	150	10	60	H	Low Offset, JFET Input Op Amp Combines High Speed and Precision
LT1055M	400	8	0.05	120	7	60	H	
LT1056AM	180	4	0.05	120	12	60	H	
LT1056M	450	8	0.05	100	9	60	H	
LT1077AM	40	0.4	9	250	0.1	40	H, J8	Micropower, Single Supply, Precision, Low Noise
LT1077M	60	0.4	11	200	0.1	29†	H, J8	
LTC1050AM	0.05	0.035	0.035	1000	4†	0.6μVp-p**	H, J8	No External Caps Required, Chopper Stabilized
LTC1050M	0.05	0.035	0.035	1000	4†	0.6μVp-p**	H, J8	
LTC1052M	5	0.05	0.03	1000	3†	0.5μVp-p**	H, J, J8	Chopper Stabilized Low Noise
LF155A	2000	15	0.05	75	5	25†*	H	JFET Inputs, Low I Bias, No Phase Reversal, Guaranteed TC V _{OS} on all Grades
LF155	2000	15	0.10	50	5	25†*	H	
LF156A	2000	5	0.05	75	10	15†*	H	
LF156	3500	15	0.10	50	9	15†*	H	
LM10	2000	2†	20	120		50†	H, J8	On-Chip Reference Operates with +1.2V Single Battery
LM101A	2000	15	75	25	0.3	28†	H, J8	Uncompensated Gen. Purp.
LM107	2000	15	75	25	0.3	28†	H, J8	Compensated Gen. Purp.
LM108A	500	5	2	40	0.1	30†	H	Low Bias Current, Low Supply Current
LM108	2000	15	3	25	0.1	30†	H	
LM118	4000		250	25	50	42†	H	High Speed, 15MHz
LT118A	1000		250	200	50	42†	H, J8	High Speed, 15MHz
OP-05A	150	0.9	2	300	0.1	18	H, J8	Low Noise, Low Offset Drift with Time
OP-05	500	2.0	3	200	0.1	18	H, J8	
OP-07A	25	0.6	2	300	0.1	18	H, J8	Low Initial Offset, Low Noise, Low Drift
OP-07	75	1.3	3	200	0.1	18	H, J8	
OP-15A	500	5	0.05	100	10	20†*	H	Precision JFET Input, Low I Bias, No Phase Reversal
OP-15B	1000	10	0.1	75	7.5	20†*	H	
OP-15C	3000	15	0.2	50	5	20†*	H	
OP-16A	500	5	0.5	100	18	20†*	H	Precision JFET Input, High Speed, No Phase Reversal
OP-16B	1000	10	0.1	75	12	20†*	H	
OP-16C	3000	15	0.2	50	9	20†*	H	
OP-27A	25	0.6	40	1000	1.7	5.5	H, J8	Very Low Noise, Unity Gain Stable
OP-27C	100	1.8	80	700	1.7	8.0	H, J8	
OP-37A	25	0.6	40	1000	11	5.5	H, J8	Very Low Noise, Stable for Gains ≥ 5
OP-37C	100	1.8	80	700	11	8.0	H, J8	

REFER TO TABLE OF CONTENTS FOR REVISED DATA LOCATION

OP AMP SELECTION GUIDE

MILITARY

PART NUMBER	ELECTRICAL CHARACTERISTICS							IMPORTANT FEATURES
	V _{os} MAX (μV)	TC V _{os} (μV/°C)	I _b MAX (nA)	A _{vol} MIN (V/mV)	SLEW RATE MIN (V/μs)	NOISE MAX 10Hz (nV/√Hz)	PACKAGES AVAILABLE	
DUAL								
LT1002AM	60	0.9	3.0	400	0.15	20	J	Dual, Matched LT1001 High CMRR, PSRR Matching
LT1002M	100	1.3	4.5	350	0.15	20	J	
LT1013AM	150	2.0	20	1500	0.2	24†	H, J8	Precision Dual Op Amp in 8-Pin Package
LT1013M	300	2.5	30	1200	0.2	24†	H, J8	
LT1024AM	50	1.5	0.12	250	0.1	33	D	Low V _{os} , Low Power, Matching Specs
LT1024M	100	2.0	0.20	180	0.1	33	D	
LT1057AM	450	7	0.05	150	10	75	H, J8	Low Offset, JFET Input Multiple Op Amps Combine High Speed and Excellent DC Specs
LT1057M	800	12	0.075	100	8	80	H, J8	
LT1078AM	70	2.0	0.25	250	0.07†	40	H, J8	Micropower, Precision, Single Supply, Low Noise Dual
LT1078M	120	2.5	0.35	200	0.07†	29†	H, J8	
LT1178AM	70	2.2	5	140	0.013	75	H, J8	17μA Max, Single Supply, Precision Dual
LT1178M	120	3.0	6	110	0.013	50†	J, N	
LF412AM	1000	10	0.1	100	10	20†*	H, J8	High Performance Dual JFET Input Op Amp
LH2108A	500	5.0	2	40	0.1	30†	D	Dual, Low Bias Current, Side Pin Package
LH2108	2000	15.0	2	25	0.1	29†	D	
OP-215A	1000	10	0.1	150	10	20†*	H, J8	High Performance Dual JFET Input Op Amp
OP-215C	3000	20	0.2	50	8	20†*	J	
OP-227A	80	1.0	40	40	1.7	6	J	Dual Matched OP-27
OP-227C	180	1.8	80	80	1.7	6	J	
OP-237A	80	1.0	40	3000	1.7	6	J	Dual Matched OP-37
OP-237C	180	1.8	80	2000	1.7	9	J	
QUAD								
LT1014AM	150	2.0	20	1500	0.2	24†	J	Precision Quad Op Amp in 14-Pin Package
LT1014M	300	2.5	30	1200	0.2	24†	J	
LT1058AM	600	15	0.05	150	10	75	J	Low Offset JFET Input Multiple Op Amps Combine High Speed and Excellent DC Specs
LT1058M	1200	15	0.075	100	8	80	J	
LT1079AM	120	2.0	0.25	250	0.07†	40	J	Micropower, Precision, Single Supply, Low Noise Quad
LT1079M	150	2.5	0.35	200	0.07†	29†	J	
LT1179AM	100	2.2	3	140	0.013	75	J	17μA Max, Single Supply, Precision Quad
LT1179M	150	3.0	6	110	0.013	50†	J	

† Typical Spec

* 100Hz Noise

** DC to 1Hz Noise

REFER TO TABLE OF CONTENTS FOR REVISED DATA LOCATION

2

COMMERCIAL

PART NUMBER	ELECTRICAL CHARACTERISTICS							IMPORTANT FEATURES
	V _{os} MAX (μV)	TC V _{os} (μV/°C)	I _b MAX (nA)	A _{vol} MIN (V/mV)	SLEW RATE MIN (V/μs)	NOISE MAX 10Hz (nV/√Hz)	PACKAGES AVAILABLE	
SINGLE								
LT1001AC	25	0.6	2.0	450	0.15	18	H, J8, N8	Extremely Low Offset Voltage Low Noise, Low Drift
LT1001C	60	1.0	3.8	400	0.15	18	H, J8, N8, S8	
LT1006AC	50	1.3	15	1000	0.25	24†	H, J8	Single Supply Operation, Fully Specified for +5V Supply
LT1006C	80	1.8	25	700	0.25	24†	H, J8, N8	
LT1006S8	400	3.5	25	700	0.25	25	S8	Extremely Low Noise, Low Drift
LT1007AC	25	0.6	35	7000	1.7	4.5	H, J8, N8	
LT1007C	60	1.0	55	5000	1.7	4.5	H, J8, N8, S	
LT1008C	120	1.5	0.1	200	0.1	30	H, N8	

OP AMP SELECTION GUIDE

COMMERCIAL

PART NUMBER	ELECTRICAL CHARACTERISTICS							IMPORTANT FEATURES
	V _{OS} MAX (μV)	TC V _{OS} (μV/°C)	I _B MAX (nA)	A _{VOL} MIN (V/mV)	SLEW RATE MIN (V/μs)	NOISE MAX 10Hz (nV/√Hz)	PACKAGES AVAILABLE	
SINGLE								
LT1010C	100mV	0.6mV/°C†	250μA	0.995	75	90†	H, K, T	High Speed Buffer, Drives ±10V into 75Ω
LT1012A	25	0.6	100	300	0.1	30	H, N8	Low V _{OS} , Low Power
LT1012C	50	1.5	0.15	200	0.1	30	H, N8	
LT1012D	60	1.7	150	200	0.1	30	H, N8	
LT1012S8	120	1.8	0.28	200	0.1	30	S8	
LT1022AC	250	5.0	0.05	150	23	50	H	Very High Speed JFET Input Op Amp with Very Good DC Specs
LT1022CH	600	9.0	0.05	120	18	60	H	
LT1022CN8	1000	15.0	0.05	100	18	60	N8	Lowest Noise, High Speed, Low Drift
LT1028AC	40	0.8	90	7000	11	1.7	H, J8, N8	
LT1028C	80	1.0	180	5000	11	1.9	H, J8, N8, S	Extremely Low Noise, High Speed
LT1037AC	25	0.6	35	7000	11	4.5	H, J8, N8	
LT1037C	60	1.0	55	5000	11	4.5	H, J8, N8, S	Lowest Offset, JFET Input Op Amp Combines High Speed and Precision
LT1055AC	150	4	0.05	150	10	50	H	
LT1055C	400	8	0.05	120	7.5	60	H	Lowest Offset, JFET Input Op Amp Combines High Speed and Precision
LT1055CN8	700	12	0.05	120	7.5	60	N8	
LT1055S8	1500	15	0.1	120	7.5	70	S8	Lowest Offset, JFET Input Op Amp Combines High Speed and Precision
LT1056AC	180	4	0.05	150	12	50	H	
LT1056C	450	8	0.05	120	9	60	H	Lowest Offset, JFET Input Op Amp Combines High Speed and Precision
LT1056CN8	800	12	0.05	120	9	60	N8	
LT1056S8	1500	15	0.1	120	9.0	70	S8	Lowest Offset, JFET Input Op Amp Combines High Speed and Precision
LT1077AC	40	0.4	9	200	0.12	20	H, J8, N8, S8	
LT1077C	60	0.4	11	200	0.12	20	H, J8, N8, S8	Micropower, Single Supply, Precision, Low Noise
LTC1050AC	5	0.05	0.035	3162	3†	0.6μVp-p**	H, J8, N8, S8	
LTC1050C	5	0.05	0.050	3162	4†	0.6μVp-p**	H, J8, N8, S8	No External Caps Required, Chopper Stabilized
LTC1052C	5	0.05	0.050	3162	3†	0.5μVp-p**	H, N8, N	Chopper Stabilized, Low Noise
LTC7652C	5	0.05	0.050	1000	3†	0.5μVp-p**	H, N8	
LF355A	2000	5	0.05	75	5	25†*	H, N8	JFET Inputs, Low I Bias, No Phase Reversal
LF356A	2000	5	0.05	75	10	15†*	H, N8	
LM10B	2000	2†	20	120	—	50†	H, J8	On-Chip Reference, Operates with +1.2V Single Battery
LM10BL	2000	2†	20	60	—	50†	H, J8	
LM10C	4000	5†	30	80	—	50†	H, J8, N8	
LM10CL	4000	5†	30	40	—	50†	H, J8, N8	
LM308A	500	5	7	60	0.1	30†	H, N8	Low Bias, Supply Current
LT318A	1000	—	250	200	50	42†	H, J8, N8	High Speed, 15MHz
LM318	10000	—	500	25	50	42†	H, J8, N8, S8	High Speed, 15MHz
OP-05C	1300	4.5	7	120	0.1	20	H, J8, N8	Low Noise, Low Offset Drift with Time
OP-05E	500	2.0	4	200	0.1	18	H, J8, N8	
OP-07C	150	1.8	7	120	0.1	20	H, J8, N8, S8	Low Initial Offset, Low Noise, Low Drift
OP-07E	75	1.3	4	200	0.1	18	H, J8, N8	
OP-15E	500	5	0.05	100	10	20†*	H, N8	Precision JFET Input, Low I Bias, No Phase Reversal
OP-15F	1000	10	0.1	75	7.5	20†*	H, N8	
OP-15G	3000	15	0.2	50	5	20†*	H, N8	Precision JFET Input, High Speed, No Phase Reversal
OP-16E	500	5	0.05	100	18	20†*	H, N8	
OP-16F	1000	10	0.1	75	12	20†*	H, N8	
OP-16G	3000	15	0.2	50	9	20†*	H, N8	
OP-27E	25	0.6	40	1000	1.7	5.5	H, J8, N8	Very Low Noise, Unity Gain Stable
OP-27G	100	1.8	80	700	1.7	8.0	H, N8	
OP-37E	25	0.6	40	1000	11	5.5	H, J8, N8	Very Low Noise, Stable for Gains ≥5
OP-37G	100	1.8	80	700	11	8.0	H, N8	
DUAL								
LT1002AC	60	0.9	3.0	400	0.15	20	J, N	Dual, Matched LT1001 High CMRR, PSRR Matching
LT1002C	100	1.3	4.5	350	0.15	20	J, N	

REFER TO TABLE OF CONTENTS FOR REVISED DATA LOCATION

OP AMP SELECTION GUIDE

COMMERCIAL

PART NUMBER	ELECTRICAL CHARACTERISTICS							IMPORTANT FEATURES
	V _{OS} MAX (μV)	TC V _{OS} (μV/°C)	I _B MAX (nA)	A _{VOL} MIN (V/mV)	SLEW RATE MIN (V/μs)	NOISE MAX 10Hz (nV/√Hz)	PACKAGES AVAILABLE	
DUAL								
LT1013AC	150	2.0	20	1500	0.2	24†	H, J8	Precision Dual Op Amp in 8-Pin Package
LT1013C	300	2.5	30	1200	0.2	24†	H, J8, N8	
LT1013D	800	5.0	30	1200	0.2	24†	N8, S8	Low V _{OS} , Low Power, Matching Specs
LT1024AC	50	1.5	0.12	250	0.1	33	N	
LT1024C	100	2.0	0.20	180	0.1	33	N	Low Offset JFET Input Multiple Op Amps Combine High Speed and Excellent DC Specs
LT1057AC	450	7	0.05	150	10	75	H, J8	
LT1057ACN8	450	10	0.05	150	10	75	N8	
LT1057C	800	12	0.075	100	8	80	H, J8	
LT1057CN8	800	16	0.075	100	8	80	N8	
LT1057S	2000	5†	0.1	100	8	13	S	
LT1057S	2000	5†	0.1	100	8	13	S	
LT1078AC	70	2.0	8	250	0.07†	40	H, J8, N8	Micropower, Precision, Single Supply, Low Noise Dual
LT1078C	120	2.5	10	200	0.07†	29†	H, J8, N8	
LT1178AC	70	2.2	5	140	0.013	75	H, J8, N8	17μA Max, Single Supply, Precision Dual
LT1178C	120	3.0	6	110	0.013	50†	H, J8, N8	
LF412AC	1000	10	0.1	100	10	20†*	H, J8, N8	High Performance Dual JFET Input Op Amp
OP-215E	1000	10	0.1	150	10	20†*	H, J8, N8	
OP-215G	3000	20	0.2	50	8	20†*	H, J8, N8	Matched OP-27
OP-227E	80	1.0	40	3000	1.7	9	J, N	
OP-227G	180	1.8	80	2000	1.7	9	J, N	Dual Matched OP-37
OP-237E	80	1.0	40	3000	1.7	6	J, N	
OP-237G	180	1.8	80	2000	1.7	6	J, N	
QUAD								
LT1014AC	180	2.0	20	1500	0.2	24†	J	Precision Quad Op Amp in 14-Pin Package
LT1014C	300	2.5	30	1200	0.2	24†	J, N	
LT1014D	800	5.0	30	1200	0.2	24†	N	Low Offset JFET Input Multiple Op Amps Combine High Speed and Excellent DC Specs
LT1058AC	50	1.0	0.05	150	10	75	J	
LT1058ACN	600	3.0	0.05	150	10	75	N	
LT1058C	1000	5.0	0.075	100	8	80	J	
LT1058CN	1000	22	0.075	100	8	80	N	
LT1079AC	120	2.0	8	250	0.07†	40	J, N	
LT1079C	150	2.5	10	200	0.07†	29†	J, N	
LT1179AC	100	2.2	5	140	0.013	75	J, N	17μA Max, Single Supply, Precision Quad
LT1179C	150	3.0	6	110	0.013	50†	J, N	

† Typical Spec
 * 100Hz Noise
 ** DC to 1Hz Noise

REFER TO TABLE OF CONTENTS FOR REVISED DATA LOCATION

2

OP AMP SELECTION GUIDE

SELECTION BY DESIGN PARAMETER

LOW OFFSET VOLTAGE

Max Input Offset Voltage ($T_A = 25^\circ\text{C}$)

$\leq 15\mu\text{V}$	$\leq 25\mu\text{V}$	$\leq 75\mu\text{V}$	$\leq 150\mu\text{V}$	$\leq 1\text{mV}$
LT1001AM LTC1050A LTC1050 LTC1052 LTC7652	LT1001AC LT1007A LT1012A LT1037A OP-07A OP-27A OP-27E OP-37A OP-37E	LT1001 LT1002A (D) LT1006A LT1007 LT1012 LT1012D LT1012S8 LT1012S8 LT1024A (D) LT1037 LT1077 LT1078A (D) LT1178A (D) OP-07E OP-07	LT1002 LT1006 LT1008 LT1012S8 LT1013A (D) LT1024 (D) LT1028 LT1055AM LT1055AC LT1079A (Q) LT1178 (D) LT1179A (Q) LT1179 (Q) OP-05A OP-07C, D OP-27C OP-37C OP-227A, E (D) OP-237A, E (D)	LT1013 (D) LT1014 (Q) LT1014A (Q) LT1022 ALL LT1055C LT1055M LT1056AM LT1056AC LT1056M LT1056C LT1057 ALL (D) LT1058 ALL (Q) LT1078 (D) LT1079 (Q) LF412A LH2108A (D) LM108A LM108B OP-05E OP-15A, E OP-15B, F OP-16A OP-16B, F OP-215A, E (D)

REFER TO TABLE OF CONTENTS
FOR REVISED DATA LOCATION

LOW BIAS CURRENT

Max Input Bias Current ($T_j = 25^\circ\text{C}$)

$\leq 0.2\text{nA}$	$\leq 3\text{nA}$	$\leq 5\text{nA}$	$\leq 10\text{nA}$
LT1008 LT1012 ALL LT1022 ALL LT1024 ALL (D) LT1055 ALL LT1056 ALL LT1057 ALL (D) LT1058 ALL (Q) LF155 ALL LF156 ALL LF412A ALL LTC7652 LTC1050 LTC1052 OP-15 ALL OP-16 ALL OP-215 ALL (D)	LT1001A LT1002A (D) LT1006 ALL LM108 LM108A OP-05A OP-05 OP-07A OP-07	LT1001 LT1002 (D) LT1178A (D) LT1179A (Q) OP-05E OP-07E	LT1077A LT1078A (D) LT1079A (Q) LT1078 (D) LT1079 (Q) LT1178 (D) LT1179 (Q) OP-05C LM308A

(D)—Dual Op Amp

(Q)—Quad Op Amp

OP AMP SELECTION GUIDE

SELECTION BY DESIGN PARAMETER

LOW NOISE

Typ Equivalent Input Noise Voltage
per $\sqrt{\text{Hz}}$, $f = 10\text{Hz}$, $R_S = 100\Omega$

$\leq 1\text{nV}/\sqrt{\text{Hz}}$	$\leq 25\text{nV}/\sqrt{\text{Hz}}$
LT1028 ALL	LT1001 ALL LT1002 ALL (D) LT1006 ALL LT1008 LT1012 LT1013 ALL (D) LT1014 ALL (D) LT1022 ALL LTC1050 LTC1052 *LT1055 ALL *LT1056 ALL LTC7652 *LF155 ALL *LF365 ALL *LF156 ALL OP-05 ALL OP-07 ALL *OP-15 ALL *OP-16 ALL
$\leq 5\text{nV}/\sqrt{\text{Hz}}$	
LT1007 ALL LT1037 ALL OP-27 ALL OP-37 ALL OP-227 ALL (D) OP-237 ALL (D)	

* 100Hz Noise

HIGH SLEW RATE

Typ Slew Rate

$\geq 10\text{V}/\mu\text{s}$	$\geq 50\text{V}/\mu\text{s}$
LT1022 ALL LT1028 ALL LT1037 ALL LT1055 ALL LT1056A OP-37 ALL OP-16A, B OP-16E, F OP-237 ALL (D) LF412A (D) OP-215A, E (D) LT1057A (D) LT1058A (Q)	LT118A/318A LM118/318 LM108/318

LOW POWER

Maximum Supply Current (per Amplifier)

$\leq 50\mu\text{A}$	$\leq 60\mu\text{A}$	$\leq 1\text{mA}$
LT1078A (D) LT1079A (Q) LT1178A (D) LT1178 (D) LT1179A (Q) LT1179 (Q)	LT1077 LT1078 (D) LT1079 (Q)	LT1006 LT1008 LT1012 ALL LT1013 (D) LT1014 (Q) LT1024 (D) LM108A LH2108A (D)

HIGH GAIN

Typ Open Loop Gain

$\geq 200 \frac{\text{V}}{\text{mV}}$	$\geq 100 \frac{\text{V}}{\text{mV}}$
LT1001 LT1002 (D) LT1003 LT1008 LT1012 ALL LT118A LT118A (Q) OP-05 OP-07 LT1077 LT1078 (D) LT1079 (Q) LT1178 (D) LT1179 (Q)	LT1006A LT1007 LT1009 LT1028 (Q) LT1028 LT1037 OP-27 OP-37 OP-227 (D) OP-237 (D) LTC1050 LTC1052 LTC7652


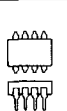
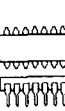
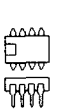
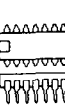
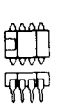
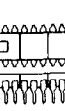
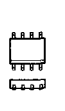
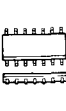
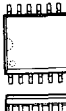
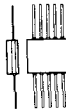
(D)—Dual Op Amp

(Q)—Quad Op Amp

REFER TO TABLE OF CONTENTS FOR REVISED DATA LOCATION

2

PACKAGES

										
H TO-5 8 LEAD 10 LEAD	J8 HERMETIC DIP 8 LEAD	J HERMETIC DIP 14 LEAD 16 LEAD 18 LEAD 20 LEAD 24 LEAD	N8 PLASTIC DIP 8 LEAD	N PLASTIC DIP 14 LEAD 16 LEAD 18 LEAD 20 LEAD 24 LEAD	D8 HERMETIC DIP 8 LEAD	D HERMETIC DIP 14 LEAD 16 LEAD 18 LEAD	S8 PLASTIC SO 8 LEAD	S PLASTIC SO 14 LEAD 16 LEAD	S PLASTIC SOL 16 LEAD 18 LEAD 20 LEAD 24 LEAD 28 LEAD	W CERPak 10 LEAD

NOTES

FEATURES

- **Guaranteed Low Offset Voltage**

LT1001AM	15 μ V max
LT1001C	60 μ V max
- **Guaranteed Low Drift**

LT1001AM	0.6 μ V/ $^{\circ}$ C max
LT1001C	1.0 μ V/ $^{\circ}$ C max
- **Guaranteed Low Bias Current**

LT1001AM	2nA max
LT1001C	4nA max
- **Guaranteed CMRR**

LT1001AM	114dB min
LT1001C	110dB min
- **Guaranteed PSRR**

LT1001AM	110dB min
LT1001C	106dB min
- **Low Power Dissipation**

LT1001AM	75mW max
LT1001C	80mW max
- **Low Noise 0.3 μ V_{p-p}**

APPLICATIONS

- Thermocouple amplifiers
- Strain gauge amplifiers
- Low level signal processing
- High accuracy data acquisition

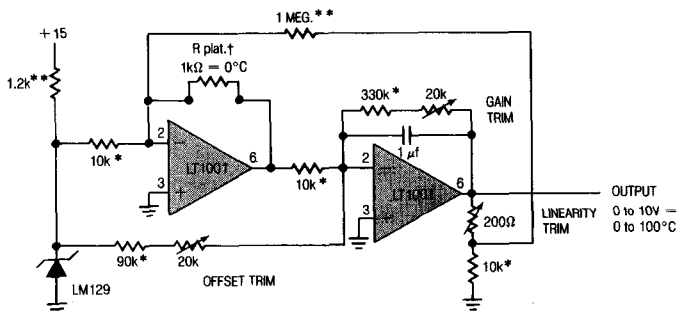
DESCRIPTION

The LT1001 significantly advances the state-of-the-art of precision operational amplifiers. In the design, processing, and testing of the device, particular attention has been paid to the optimization of the entire distribution of several key parameters. Consequently, the specifications of the lowest cost, commercial temperature device, the LT1001C, have been dramatically improved when compared to equivalent grades of competing precision amplifiers.

Essentially, the input offset voltage of all units is less than 50 μ V (see distribution plot below). This allows the LT1001AM/883 to be specified at 15 μ V. Input bias and offset currents, common-mode and power supply rejection of the LT1001C offer guaranteed performance which were previously attainable only with expensive, selected grades of other devices. Power dissipation is nearly halved compared to the most popular precision op amps, without adversely affecting noise or speed performance. A beneficial by-product of lower dissipation is decreased warm-up drift. Output drive capability of the LT1001 is also enhanced with voltage gain guaranteed at 10 mA of load current. For similar performance in a dual precision op amp, with guaranteed matching specifications, see the LT1002. Shown below is a platinum resistance thermometer application.

2

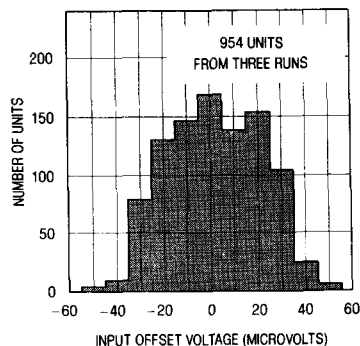
**Linearized Platinum Resistance Thermometer
 with $\pm 0.025^{\circ}$ C Accuracy Over 0 to 100 $^{\circ}$ C**



* ULTRONIX 105A WIREWOUND
 † 1% FILM
 ‡ PLATINUM RTD
 118MF (ROSEMOUNT, INC.)

‡ Trim sequence: trim offset (0 $^{\circ}$ C = 1000.0),
 trim linearity (35 $^{\circ}$ C = 1138.7), trim gain
 (100 $^{\circ}$ C = 1392.6). Repeat until all three
 points are fixed with $\pm 0.025^{\circ}$ C.

**Typical Distribution
 of Offset Voltage
 $V_S = \pm 15V, T_A = 25^{\circ}C$**



ABSOLUTE MAXIMUM RATINGS

Supply Voltage $\pm 22V$
 Differential Input Voltage $\pm 30V$
 Input Voltage $\pm 22V$
 Output Short Circuit Duration Indefinite
 Operating Temperature Range
 LT1001AM/LT1001M $-55^{\circ}C$ to $150^{\circ}C$
 LT1001AC/LT1001C $0^{\circ}C$ to $125^{\circ}C$
 Storage: All Devices $-65^{\circ}C$ to $150^{\circ}C$
 Lead Temperature (Soldering, 10 sec.) $300^{\circ}C$

PACKAGE/ORDER INFORMATION

<p>TOP VIEW OFFSET ADJUST</p> <p>H PACKAGE METAL CAN</p>	<p>ORDER PART NUMBER</p> <p>LT 1001AMH/883 LT 1001MH LT 1001ACH LT 1001CH</p>
<p>TOP VIEW</p> <p>J8 PACKAGE 8 PIN HERMETIC DIP</p> <p>NB PACKAGE 8 PIN PLASTIC DIP</p>	<p>LT 1001AMJ8/883 LT 1001MJ8 LT 1001ACJ8 LT 1001CJ8</p> <p>LT 1001ACN8 LT 1001CN8</p>

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V, T_A = 25^{\circ}C$, unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS	LT1001AM/883 LT1001AC			LT1001M/LT1001C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	Note 1 LT 1001AM/883 LT 1001AC		7	15		18	60	μV
$\frac{\Delta V_{OS}}{\Delta \text{Time}}$	Long Term Input Offset Voltage Stability	Notes 2 and 3		0.2	1.0		0.3	1.5	$\mu V/\text{month}$
I_{OS}	Input Offset Current			0.3	2.0		0.4	3.8	nA
I_b	Input Bias Current			± 0.5	± 2.0		± 0.7	± 4.0	nA
e_n	Input Noise Voltage	0.1Hz to 10Hz (Note 2)		0.3	0.6		0.3	0.6	μV_{RMS}
e_n	Input Noise Voltage Density	$f_o = 10\text{Hz}$ (Note 5) $f_o = 1000\text{Hz}$ (Note 2)		10.3	18.0		10.5	18.0	nV/\sqrt{Hz}
A_{VOL}	Large Signal Voltage Gain	$R_L \geq 2k\Omega, V_o = \pm 12V$ $R_L \geq 1k\Omega, V_o = \pm 10V$	450 300	800 500		400 250	800 500		V/mV
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 13V$	114	126		110	126		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 3V$ to $\pm 18V$	110	123		106	123		dB
R_{in}	Input Resistance Differential Mode	(Note 4)	30	100		15	80		$M\Omega$
	Input Voltage Range		± 13	± 14		± 13	± 14		V
V_{OUT}	Maximum Output Voltage Swing	$R_L \geq 2k\Omega$ $R_L \geq 1k\Omega$	± 13 ± 12	± 14 ± 13.5		± 13 ± 12	± 14 ± 13.5		V
S_R	Slew Rate	$R_L \geq 2k\Omega$ (Note 4)	0.1	0.25		0.1	0.25		V/ μs
GBW	Gain-Bandwidth Product	(Note 4)	0.4	0.8		0.4	0.8		MHz
P_d	Power Dissipation	No load No load, $V_o = \pm 3V$		46 4	75 6		48 4	80 8	mW

See Notes on page 3.

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V, -55^\circ C \leq T_A \leq 125^\circ C$, unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS	LT1001AM/883			LT1001M			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage		●	30	60	45	160	μV	
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Offset Voltage Drift		●	0.2	0.6	0.3	1.0	$\mu V/^\circ C$	
I_{OS}	Input Offset Current		●	0.8	4.0	1.2	7.6	nA	
I_B	Input Bias Current		●	± 1.0	± 4.0	± 1.5	± 8.0	nA	
A_{VOL}	Large Signal Voltage Gain	$R_L \geq 2k\Omega, V_0 = \pm 10V$	●	300	700	200	700	V/mV	
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 13V$	●	110	122	106	120	dB	
PSRR	Power Supply Rejection Ratio	$V_S = \pm 3$ to $\pm 18V$	●	104	117	100	117	dB	
	Input Voltage Range		●	± 13	± 14	± 13	± 14	V	
V_{OUT}	Output Voltage Swing	$R_L \geq 2k\Omega$	●	± 12.5	± 13.5	± 12.0	± 13.5	V	
P_d	Power Dissipation	No load	●	55	90	60	100	mW	

2

$V_S = \pm 15V, 0^\circ C \leq T_A \leq 70^\circ C$, unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS	LT1001AC			LT1001C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage		●	20	60	30	110	μV	
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Offset Voltage Drift		●	0.2	0.6	0.3	1.0	$\mu V/^\circ C$	
I_{OS}	Input Offset Current		●	0.5	3.5	0.6	5.3	nA	
I_B	Input Bias Current		●	± 0.7	± 3.5	± 1.0	± 5.5	nA	
A_{VOL}	Large Signal Voltage Gain	$R_L \geq 2k\Omega, V_0 = \pm 10V$	●	350	750	250	750	V/mV	
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 13V$	●	110	124	106	123	dB	
PSRR	Power Supply Rejection Ratio	$V_S = \pm 3V$ to $\pm 18V$	●	106	120	103	120	dB	
	Input Voltage Range		●	± 13	± 14	± 13	± 14	V	
V_{OUT}	Output Voltage Swing	$R_L \geq 2k\Omega$	●	± 12.5	± 13.8	± 12.5	± 13.8	V	
P_d	Power Dissipation	No load	●	50	85	55	90	mW	

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: Offset voltage for the LT1001AM/883 and LT1001AC are measured after power is applied and the device is fully warmed up. All other grades are measured with high speed test equipment, approximately 1 second after power is applied. The LT1001AM/883 receives 168 hr. burn-in at 125°C. or equivalent.

Note 2: This parameter is tested on a sample basis only.

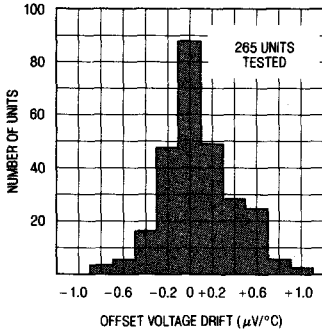
Note 3: Long Term Input Offset Voltage Stability refers to the averaged trend line of V_{OS} versus Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 days are typically 2.5 μV .

Note 4: Parameter is guaranteed by design.

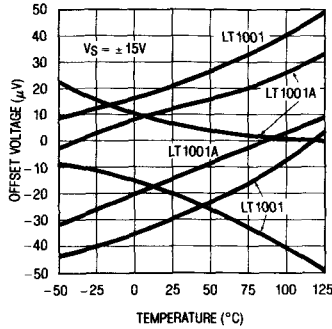
Note 5: 10Hz noise voltage density is sample tested on every lot. Devices 100% tested at 10Hz are available on request.

TYPICAL PERFORMANCE CHARACTERISTICS

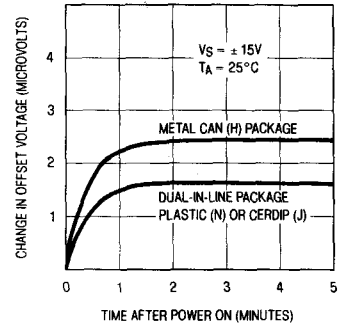
Typical Distribution of Offset Voltage Drift with Temperature



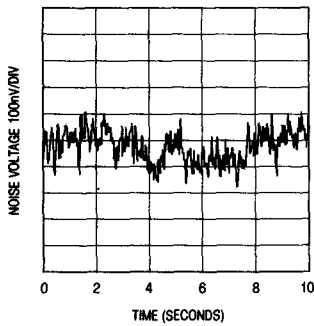
Offset Voltage Drift with Temperature of Representative Units



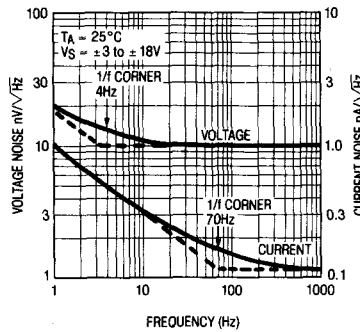
Warm-Up Drift



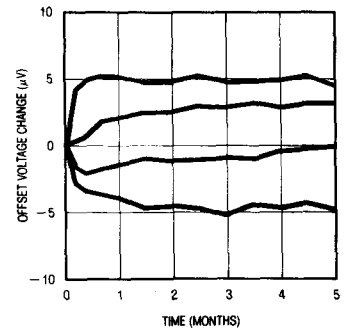
0.1Hz to 10Hz Noise



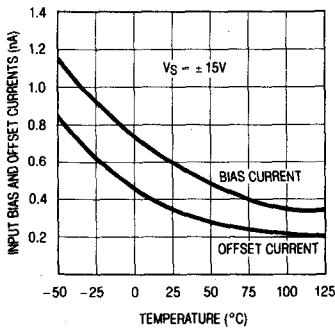
Noise Spectrum



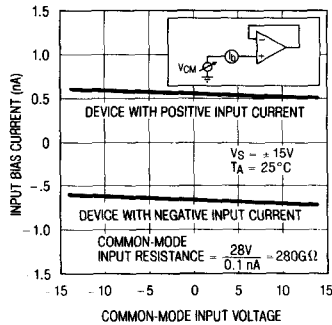
Long Term Stability of Four Representative Units



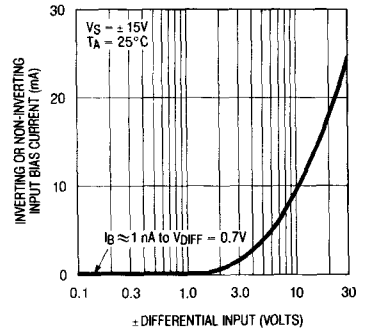
Input Bias and Offset Current vs Temperature



Input Bias Current Over the Common Mode Range

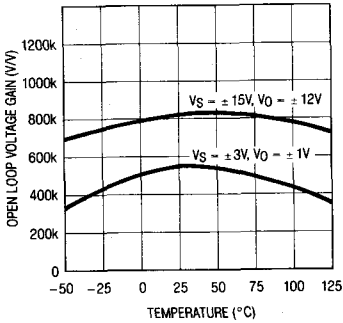


Input Bias Current vs. Differential Input Voltage

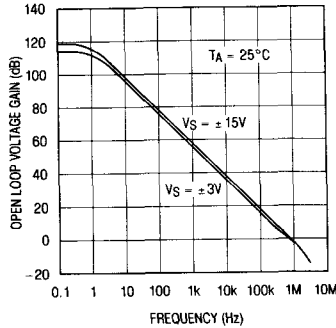


TYPICAL PERFORMANCE CHARACTERISTICS

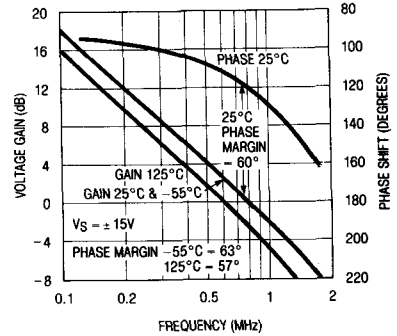
Open Loop Voltage Gain vs Temperature



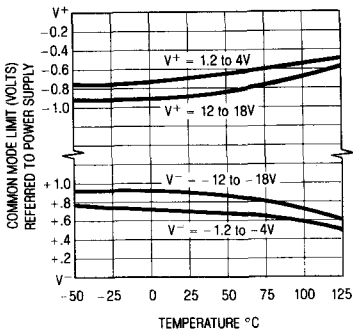
Open Loop Voltage Gain Frequency Response



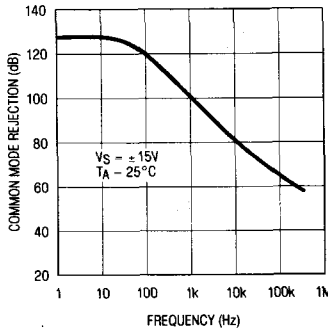
Gain, Phase Shift vs. Frequency



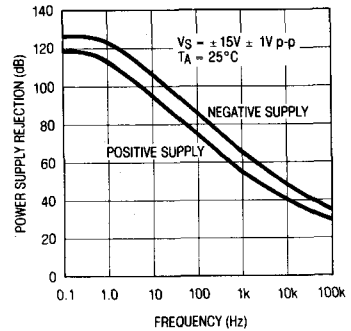
Common Mode Limit vs Temperature



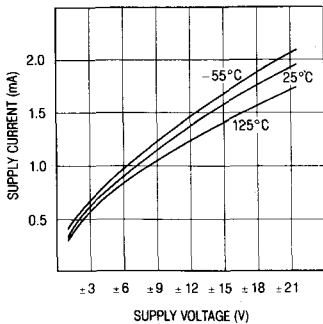
Common Mode Rejection Ratio vs Frequency



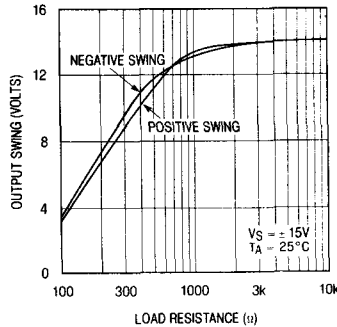
Power Supply Rejection Ratio vs Frequency



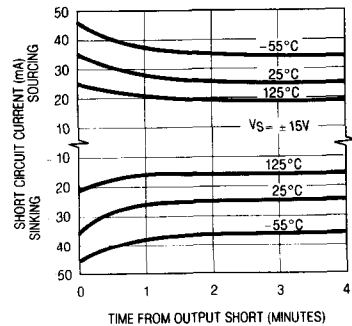
Supply Current vs Supply Voltage



Output Swing vs. Load Resistance



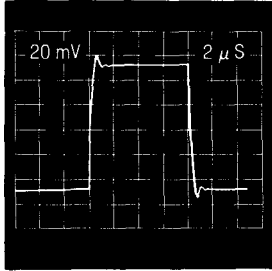
Output Short Circuit Current vs Time



2

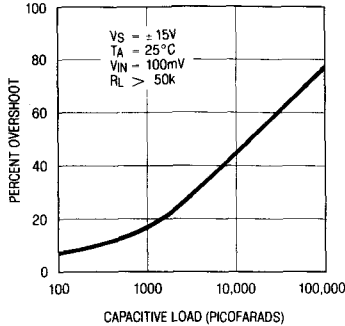
TYPICAL PERFORMANCE CHARACTERISTICS

Small Signal Transient Response

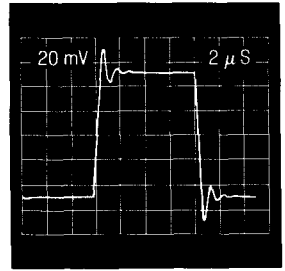


$A_v = +1, C_L = 50\text{pF}$

Voltage Follower Overshoot vs Capacitive Load

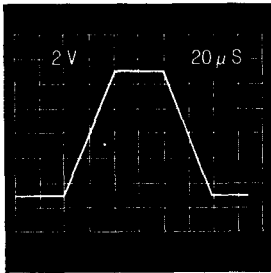


Small Signal Transient Response

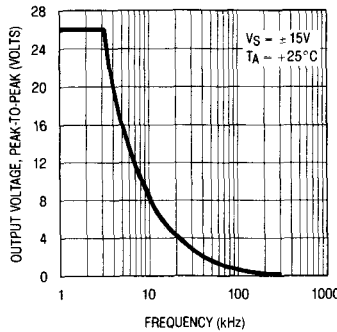


$A_v = +1, C_L = 1000\text{pF}$

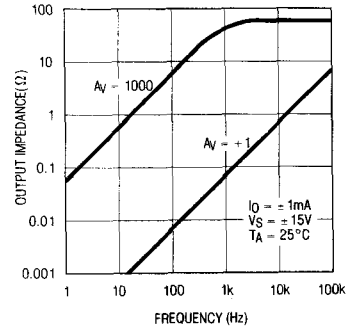
Large Signal Transient Response



Maximum Undistorted Output vs. Frequency



Closed Loop Output Impedance



APPLICATIONS INFORMATION

Application Notes and Test Circuits

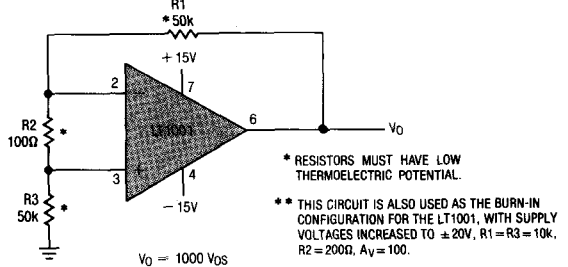
The LT1001 series units may be inserted directly into OP-07, OP-05, 725, 108A or 101A sockets with or without removal of external frequency compensation or nulling components. The LT1001 can also be used in 741, LF156 or OP-15 applications provided that the nulling circuitry is removed.

The LT1001 is specified over a wide range of power supply voltages from $\pm 3\text{V}$ to $\pm 18\text{V}$. Operation with lower supplies is possible down to $\pm 1.2\text{V}$ (two Ni-Cad batteries). However, with $\pm 1.2\text{V}$ supplies, the device is stable only in closed loop gains of +2 or higher (or inverting gain of one or higher).

Unless proper care is exercised, thermocouple effects caused by temperature gradients across dissimilar

metals at the contacts to the input terminals, can exceed the inherent drift of the amplifier. Air currents over device leads should be minimized, package leads should be short, and the two input leads should be as close together as possible and maintained at the same temperature.

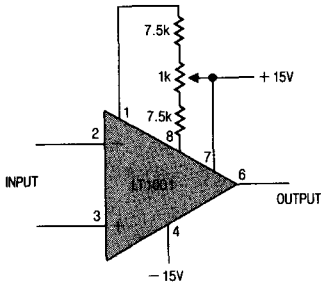
Test Circuit for Offset Voltage and its Drift with Temperature



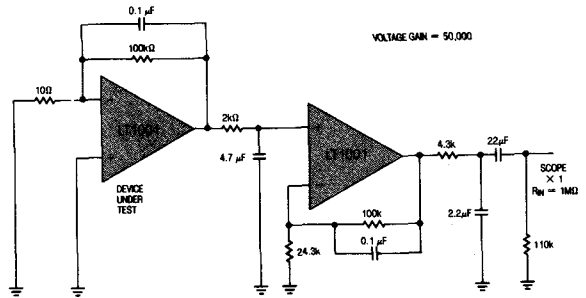
Offset Voltage Adjustment

The input offset voltage of the LT1001, and its drift with temperature, are permanently trimmed at wafer test to a low level. However, if further adjustment of Vos is necessary, nulling with a 10k or 20k potentiometer will not degrade drift with temperature. Trimming to a value other than zero creates a drift of (Vos/300) $\mu\text{V}/^\circ\text{C}$, e.g. if Vos is adjusted to 300 μV , the change in drift will be 1 $\mu\text{V}/^\circ\text{C}$. The adjustment range with a 10k or 20k pot is approximately $\pm 2.5\text{mV}$. If less adjustment range is needed, the sensitivity and resolution of the nulling can be improved by using a smaller pot in conjunction with fixed resistors. The example below has an approximate null range of $\pm 100 \mu\text{V}$.

Improved Sensitivity Adjustment



0.1Hz to 10Hz Noise Test Circuit

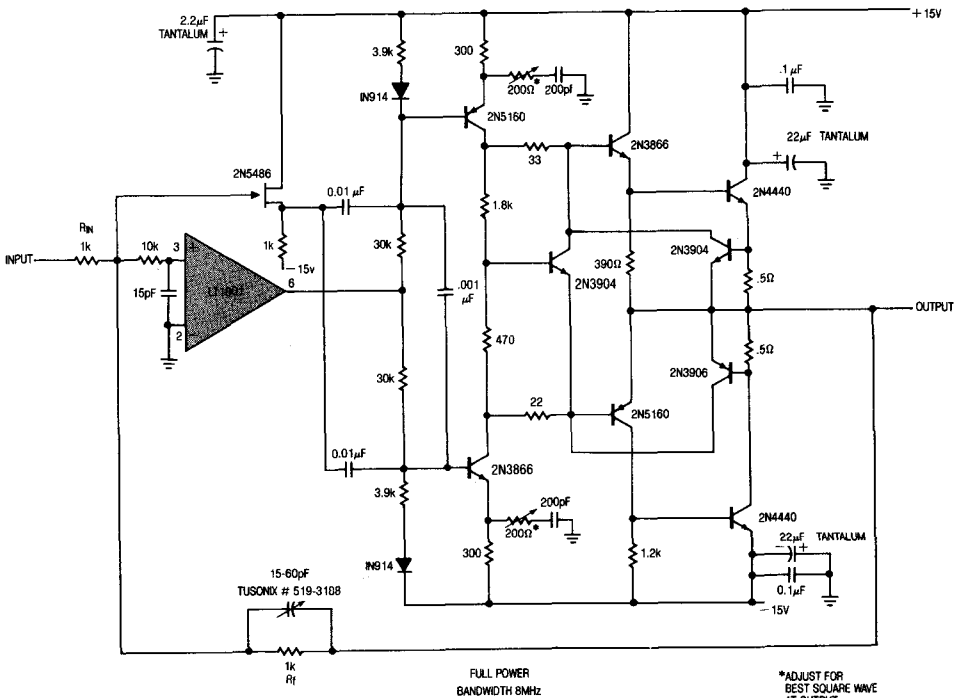


(Peak to Peak noise measured in 10 Sec interval)

The device under test should be warmed up for three minutes and shielded from air currents.

2

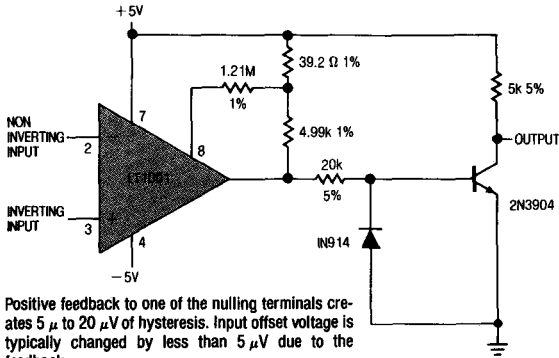
**DC Stabilized
1000v/ μsec Op Amp**



*ADJUST FOR BEST SQUARE WAVE AT OUTPUT

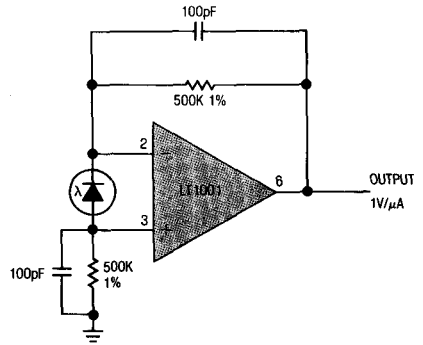
TYPICAL APPLICATIONS

Microvolt Comparator with TTL Output

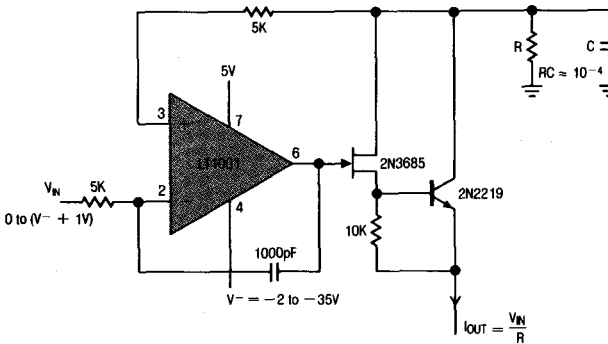


Positive feedback to one of the nulling terminals creates $5\mu\text{V}$ to $20\mu\text{V}$ of hysteresis. Input offset voltage is typically changed by less than $5\mu\text{V}$ due to the feedback.

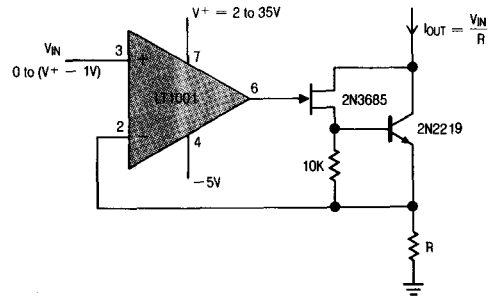
Photodiode Amplifier



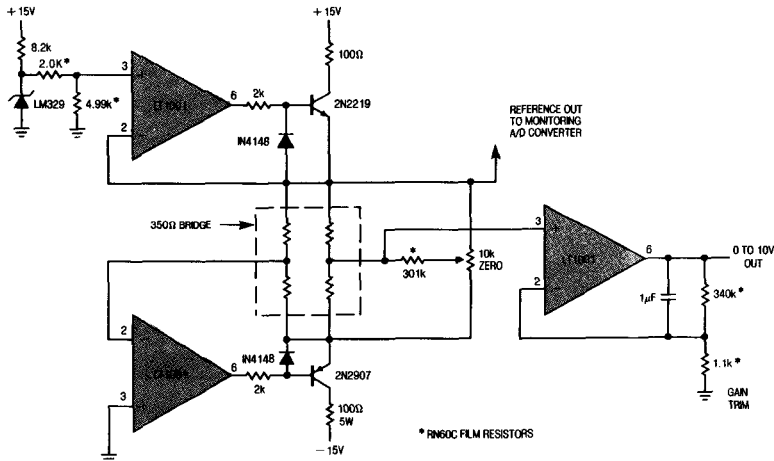
Precision Current Source



Precision Current Sink

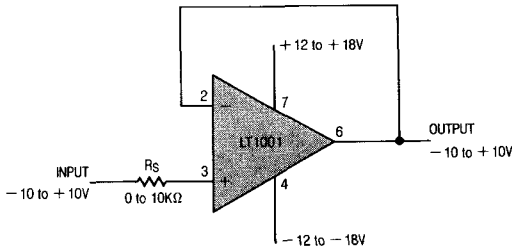


Strain Gauge Signal Conditioner with Bridge Excitation



* FM60C FILM RESISTORS

**Large Signal Voltage Follower
With 0.001% Worst-Case Accuracy**



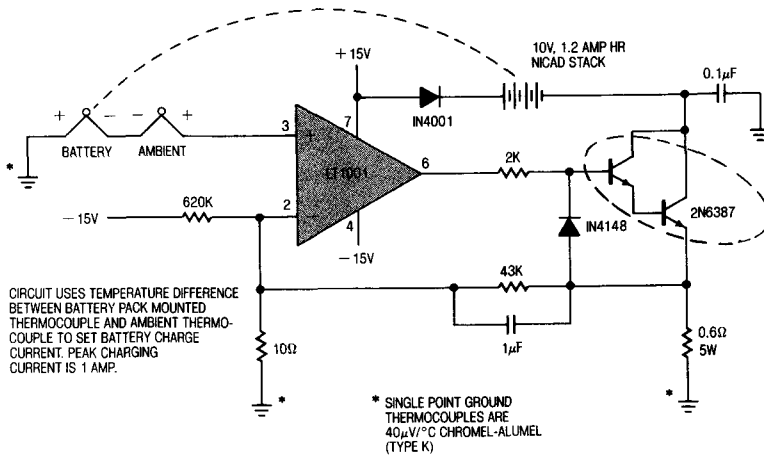
The voltage follower is an ideal example illustrating the overall excellence of the LT1001. The contributing error terms are due to offset voltage, input bias current, voltage gain, common-mode and power-supply

rejections. Worst-case summation of guaranteed specifications is tabulated below.

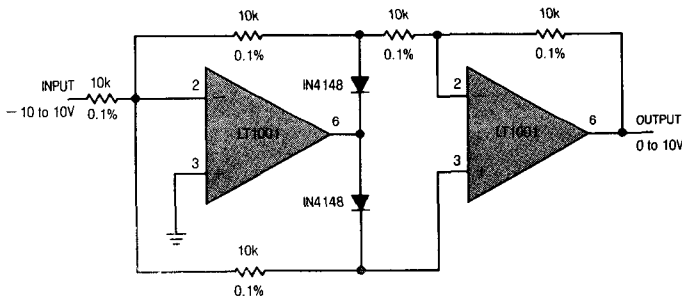
Error	OUTPUT ACCURACY			
	LT1001AM /883	LT1001C	LT1001AM /883	LT1001C
	25°C Max.	25°C Max.	-55 to 125°C Max.	0 to 70°C Max.
Offset Voltage	15μV	60μV	60μV	110μV
Bias Current	20μA	40μA	40μA	55μA
Common-Mode Rejection	20μV	30μV	30μV	50μV
Power Supply Rejection	18μV	30μV	36μV	42μV
Voltage Gain	22μV	25μV	33μV	40μV
Worst-case Sum	95μV	185μV	199μV	297μV
Percent of Full Scale (=20V)	0.0005%	0.0009%	0.0010%	0.0015%

2

Thermally Controlled Nicad Charger

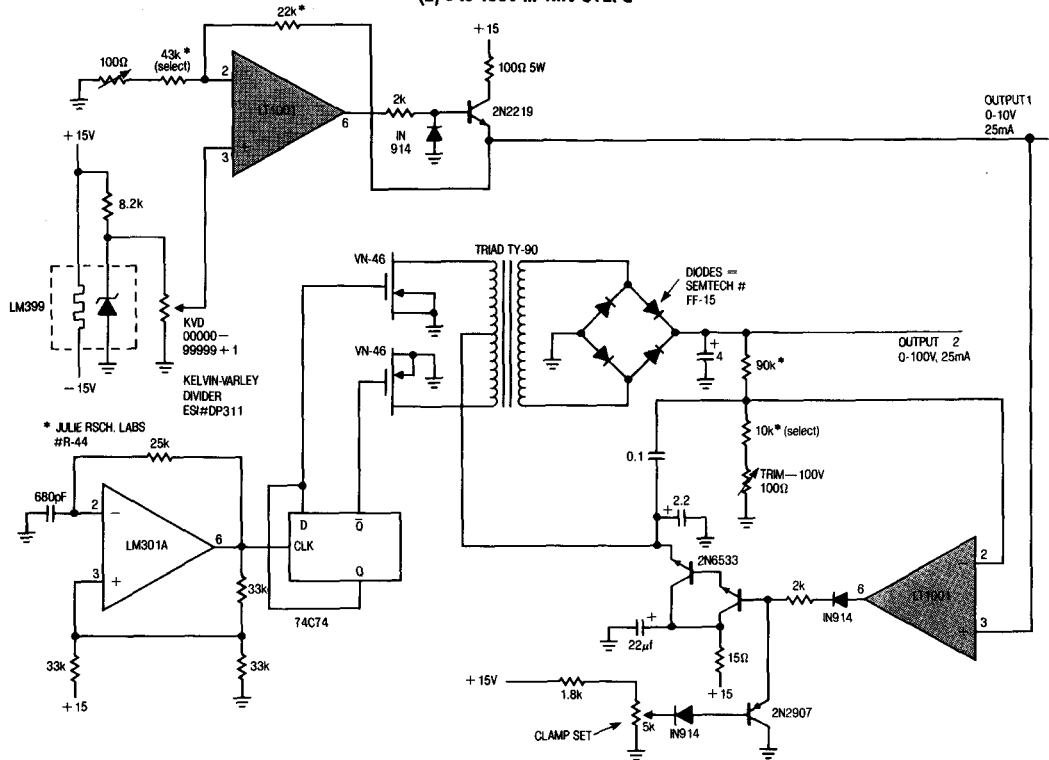


Precision Absolute Value Circuit



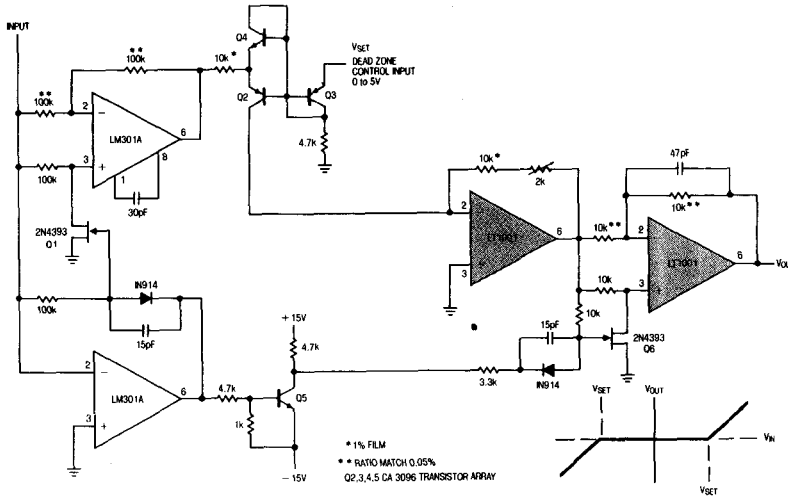
Precision Power Supply with Two Outputs

- (1) 0 to 10V in 100 μ V STEPS
- (2) 0 to 100V in 1mV STEPS



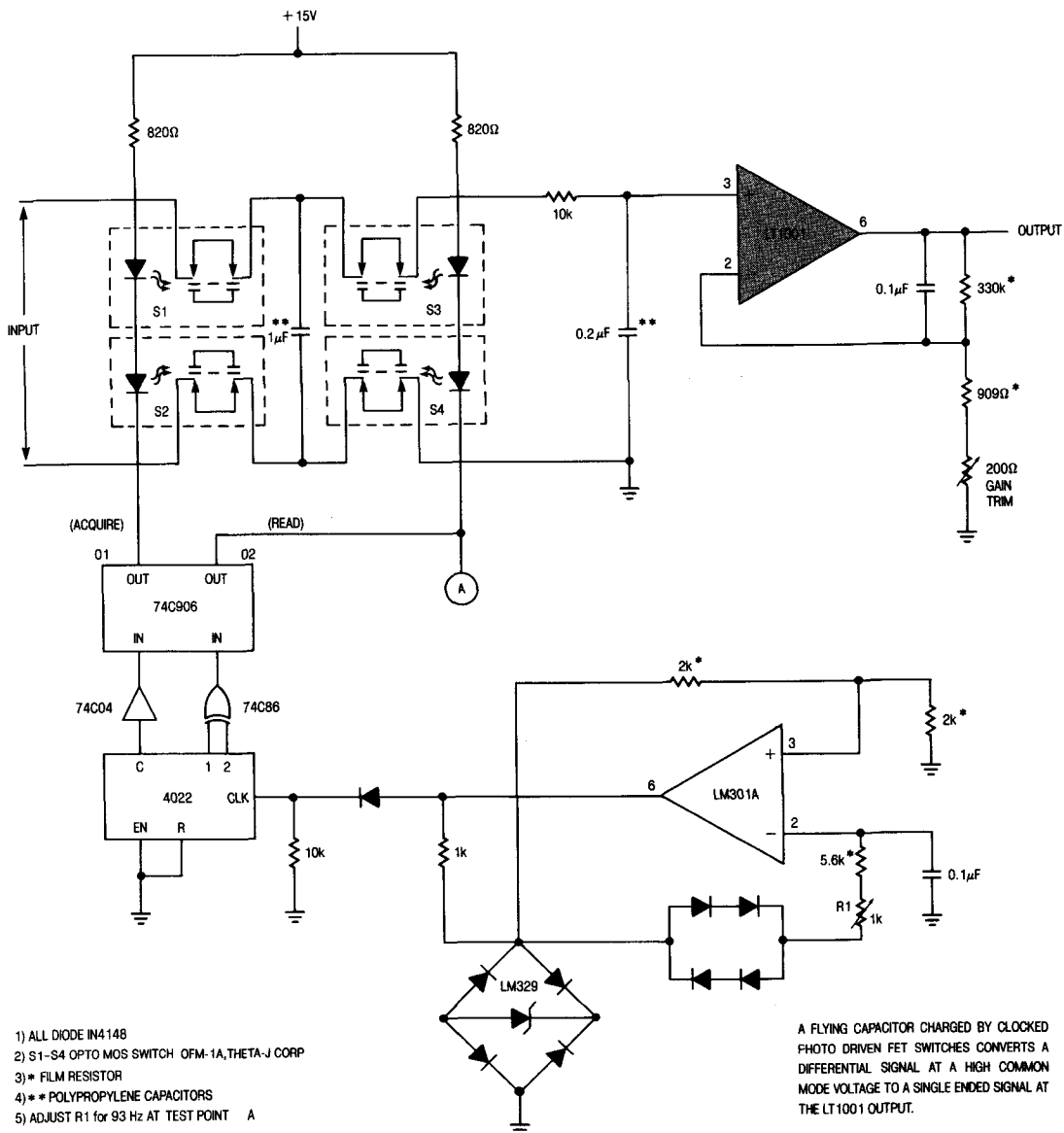
Dead Zone Generator

BIPOLAR SYMMETRY IS EXCELLENT BECAUSE ONE DEVICE, Q2, SETS BOTH LIMITS



* 1% FILM
 ** RATIO MATCH 0.05%
 Q2,3,4,5 CA 3096 TRANSISTOR ARRAY

**Instrumentation Amplifier with $\pm 300V$
Common Mode Range and CMRR > 150dB**



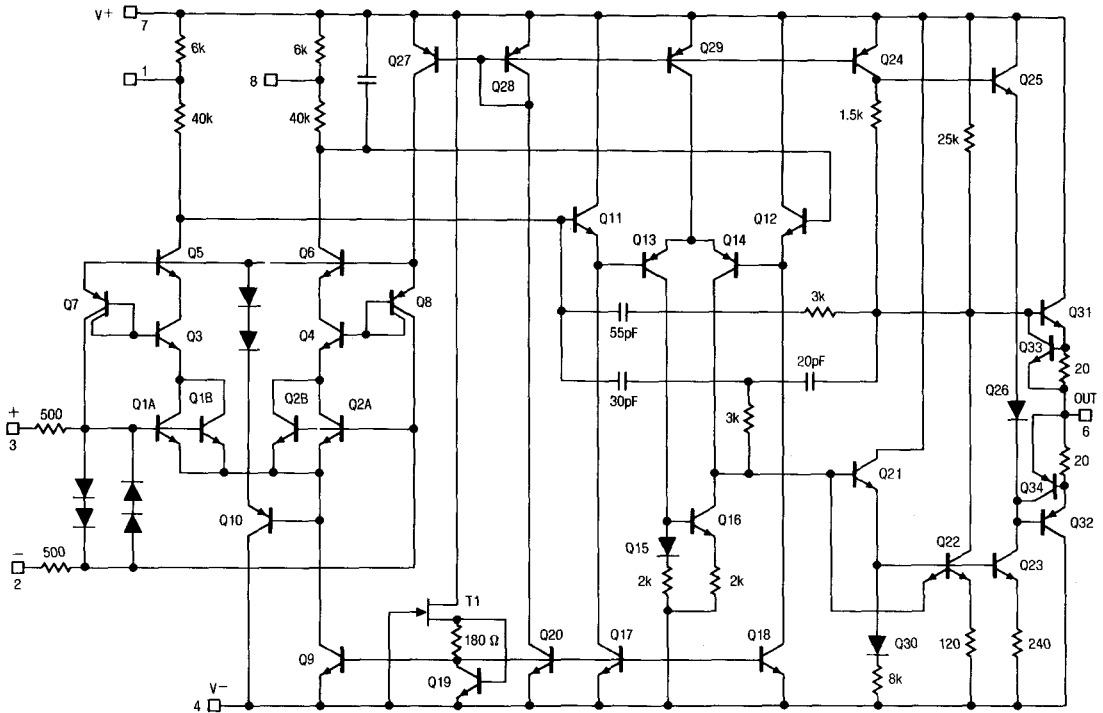
2

- 1) ALL DIODE IN4148
- 2) S1-S4 OPTO MOS SWITCH OFM-1A, THETA-J CORP
- 3) * FILM RESISTOR
- 4) ** POLYPROPYLENE CAPACITORS
- 5) ADJUST R1 for 93 Hz AT TEST POINT A

A FLYING CAPACITOR CHARGED BY CLOCKED PHOTO DRIVEN FET SWITCHES CONVERTS A DIFFERENTIAL SIGNAL AT A HIGH COMMON MODE VOLTAGE TO A SINGLE ENDED SIGNAL AT THE LT1001 OUTPUT.

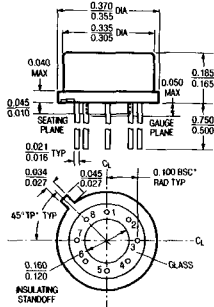
SCHEMATIC DIAGRAM

LT1001 Schematic Diagram



PACKAGE DESCRIPTION

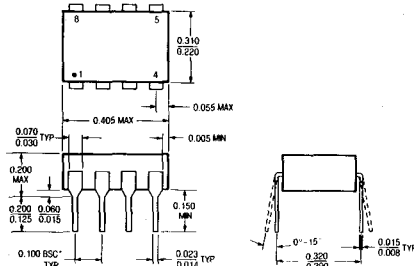
H Package
Metal Can



NOTE: DIMENSIONS IN INCHES

T_{jmax}	θ_{ja}	θ_{jc}
150°C	150°C/W	45°C/W

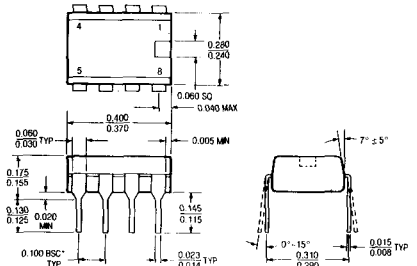
J8 Package
8 Lead Hermetic Dip



NOTE: DIMENSIONS IN INCHES UNLESS OTHERWISE NOTED.
*LEADS WITHIN 0.007 OF TRUE POSITION (TYP) AT GAUGE PLANE

T_{jmax}	θ_{ja}
150°C	100°C/W

N8 Package
8 Lead Plastic



NOTE: DIMENSIONS IN INCHES UNLESS OTHERWISE NOTED.
*LEADS WITHIN 0.007 OF TRUE POSITION (TYP) AT GAUGE PLANE

T_{jmax}	θ_{ja}
100°C	130°C/W

FEATURES

- *Guaranteed* Low Offset Voltage 60 μ V Max.
- *Guaranteed* Low Drift 1.0 μ V/ $^{\circ}$ C Max.
- *Guaranteed* Low Bias Current 4nA Max.
- *Guaranteed* CMRR 110dB Min.
- *Guaranteed* PSRR 106dB Min.
- Low Power Dissipation 80mW Max.
- Low Noise 0.3 μ Vp-p

DESCRIPTION

The LT1001 significantly advances the state-of-the-art of precision operational amplifiers. In the design, processing, and testing of the device, particular attention has been paid to the optimization of the entire distribution of several key parameters. Consequently, the specifications of the lowest cost, commercial temperature device, the LT1001C, have been dramatically improved when compared to equivalent grades of competing precision amplifiers.

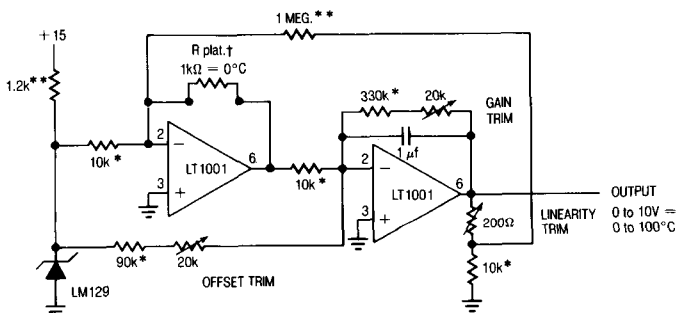
Essentially, the input offset voltage of all units is less than 50 μ V (see distribution plot below). Input bias and offset currents, common-mode and power supply rejection of the LT1001C offer guaranteed performance which were previously attainable only with expensive, selected grades of other devices. Power dissipation is nearly halved compared to the most popular precision op amps, without adversely affecting noise or speed performance. A beneficial by-product of lower dissipation is decreased warm-up drift. Output drive capability of the LT1001 is also enhanced with voltage gain guaranteed at 10mA of load current.

2

APPLICATIONS

- Thermocouple Amplifiers
- Strain Gauge Amplifiers
- Low Level Signal Processing
- High Accuracy Data Acquisition

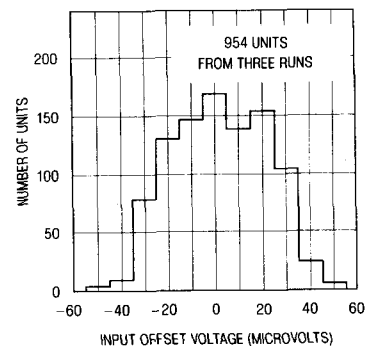
Linearized Platinum Resistance Thermometer
 with $\pm 0.025^{\circ}$ C Accuracy Over 0 to 100 $^{\circ}$ C



* ULTRONIX 105A WIREWOUND
 ** 1% FILM
 † PLATINUM RTD
 118MF (ROSEMOUNT, INC.)

‡ Trim sequence: trim offset (0 $^{\circ}$ C = 1000.0 Ω),
 trim linearity (35 $^{\circ}$ C = 1138.7 Ω), trim gain
 (100 $^{\circ}$ C = 1392.6 Ω). Repeat until all three
 points are fixed with $\pm 0.025^{\circ}$ C.

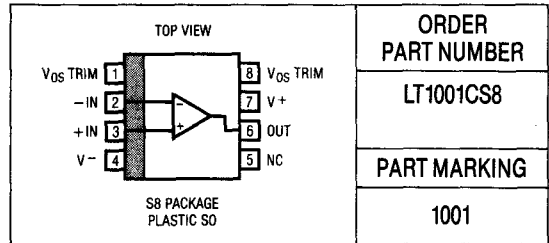
Typical Distribution
 of Offset Voltage
 $V_S = \pm 15V, T_A = 25^{\circ}C$



ABSOLUTE MAXIMUM RATINGS

Supply Voltage ± 22V
 Differential Input Voltage ± 30V
 Input Voltage ± 22V
 Output Short Circuit Duration Indefinite
 Operating Temperature Range 0°C to 70°C
 Storage Temperature Range - 65°C to 150°C
 Lead Temperature (Soldering, 10 sec.) 300°C

PACKAGE/ORDER INFORMATION



ORDER PART NUMBER	LT1001CS8
PART MARKING	1001

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V, T_A \leq 25^\circ C$, unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS	LT1001C			UNITS
			MIN	TYP	MAX	
V_{OS}	Input Offset Voltage			18	60	μV
$\frac{\Delta V_{OS}}{\Delta Time}$	Long Term Input Offset Voltage Stability	Note 1 and Note 2		0.3	1.5	$\mu V/month$
I_{OS}	Input Offset Current			0.4	3.8	nA
I_b	Input Bias Current			± 0.7	± 4.0	nA
e_n	Input Noise Voltage	0.1Hz to 10Hz (Note 1)		0.3	0.6	μV_{p-p}
e_n	Input Noise Voltage Density	$f_o = 10Hz$ (Note 1) $f_o = 1000Hz$ (Note 1)		10.5 9.8	18.0 11.0	nV/\sqrt{Hz}
A_{VOL}	Large Signal Voltage Gain	$R_L \geq 2k\Omega, V_o = \pm 12V$ $R_L \geq 1k\Omega, V_o = \pm 10V$	400 250	800 500		V/mV V/mV
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm 13V$	110	126		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 3V$ to ± 18V	106	123		dB
R_{in}	Input Resistance Differential Mode		15	80		M Ω
	Input Voltage Range		± 13	± 14		V
V_{OUT}	Maximum Output Voltage Swing	$R_L \geq 2k\Omega$ $R_L \geq 1k\Omega$	± 13 ± 12	± 14 ± 13.5		V V
S_R	Slew Rate	$R_L \geq 2k\Omega$ (Note 3)	0.1	0.25		V/ μs
GBW	Gain-Bandwidth Product	(Note 3)	0.4	0.8		MHz
P_d	Power Dissipation	No Load		48	80	mW
		No Load, $V_S = \pm 3V$		4	8	mW

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V, 0^\circ C \leq T_A \leq 70^\circ C$, unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS	LT1001C			UNITS
			MIN	TYP	MAX	
V_{OS}	Input Offset Voltage		●	30	110	μV
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Offset Voltage Drift		●	0.3	1.0	$\mu V/^\circ C$
I_{OS}	Input Offset Current		●	0.6	5.3	nA
I_b	Input Bias Current		●	± 1.0	± 5.5	nA
A_{VOL}	Large Signal Voltage Gain	$R_L \geq 2k\Omega, V_o = \pm 10V$	●	250	750	V/mV
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm 13V$	●	106	123	dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 3V$ to ± 18V	●	103	120	dB
	Input Voltage Range		●	± 13	± 14	V
V_{OUT}	Output Voltage Swing	$R_L \geq 2k\Omega$	●	± 12.5	± 13.8	V
P_d	Power Dissipation	No Load	●	55	90	mW

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: This parameter is tested on a sample basis only.

Note 2: Long Term Input Offset Voltage Stability refers to the averaged trend line of V_{OS} versus Time over extended periods after the first 30 days of

operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 days are typically 2.5 μV .

Note 3: Parameter is guaranteed by design.

FEATURES

- **Guaranteed low offset voltage**
 - LT1002A 60 μ V max
 - LT1002 100 μ V max
- **Guaranteed offset voltage match**
 - LT1002A 40 μ V max
 - LT1002 80 μ V max
- **Guaranteed low drift**
 - LT1002A 0.9 μ V/ $^{\circ}$ C max
 - LT1002 1.3 μ V/ $^{\circ}$ C max
- **Guaranteed CMRR**
 - LT1002A 110dB min
 - LT1002 110dB min
- **Guaranteed channel separation**
 - LT1002A 132dB min
 - LT1002 130dB min
- **Guaranteed matching characteristics**
- **Low noise 0.35 μ V p-p**

APPLICATIONS

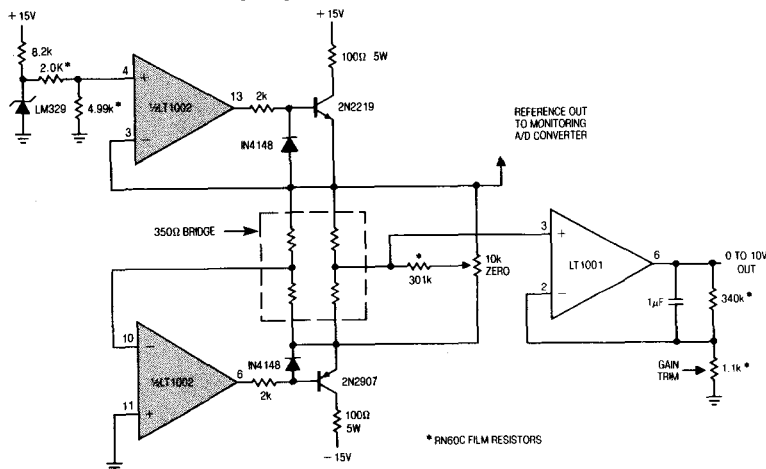
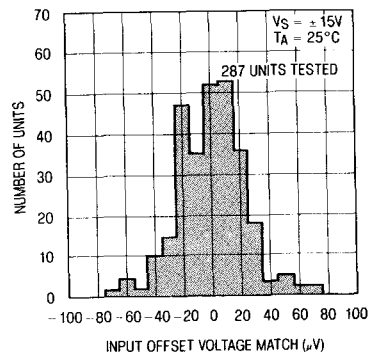
- Thermocouple Amplifiers
- Strain Gauge Amplifiers
- Low level signal processing
- Medical instrumentation
- Precision dual limit threshold detection
- Instrumentation amplifiers

DESCRIPTION

The LT1002 dual, matched precision operational amplifiers combine excellent individual amplifier performance with tight matching and temperature tracking between amplifiers.

In the design, processing, and testing of the device, particular attention has been paid to the optimization of the entire distribution of several key parameters and their matching. Consequently, the specifications of even the low cost commercial grade (the LT1002C) have been spectacularly improved compared to presently available devices.

Essentially, the input offset voltage of all units is less than 80 μ V, and matching between amplifiers is consistently better than 60 μ V (see distribution plot below). Input bias and offset currents, channel separation, common mode and power supply rejections of the LT1002C are all specified at levels which were previously attainable only on very expensive, selected grades of other dual devices. Power dissipation is nearly halved compared to the most popular precision duals, without adversely affecting noise or speed performance. A by-product of lower dissipation is decreased warm-up drift. For even better performance in a single precision op amp, refer to the LT1001 data sheet. A bridge signal conditioning application is shown below. This circuit illustrates the requirement for both excellent matching and individual amplifier specifications.

2
Strain Gauge Signal Conditioner With Bridge Excitation

Distribution of Offset Voltage Match


ABSOLUTE MAXIMUM RATINGS

Supply Voltage (Note 6) $\pm 22V$
 Differential Input Voltage $\pm 30V$
 Input Voltage Equal to Supply Voltage
 Output Short Circuit Duration Indefinite
 Operating Temperature Range
 LT1002AM/LT1002M $-55^{\circ}C$ to $125^{\circ}C$
 LT1002AC/LT1002C $0^{\circ}C$ to $70^{\circ}C$
 Storage Temperature Range
 All Grades $-65^{\circ}C$ to $150^{\circ}C$
 Lead Temperature (Soldering, 10 sec.) $300^{\circ}C$

PACKAGE/ORDER INFORMATION

ORDER PART NO.	OFFSET VOLTAGE MAX at 25°C
LT1002AMJ	60 μV
LT1002MJ	100 μV
LT1002ACJ	60 μV
LT1002CJ	100 μV
LT1002ACN	60 μV
LT1002CN	100 μV

NOTE: Device may be operated even if insertion is reversed; this is due to inherent symmetry of pin locations of amplifiers A and B. (Note 6)

ELECTRICAL CHARACTERISTICS, INDIVIDUAL AMPLIFIERS

$V_S = \pm 15V$, $T_A = 25^{\circ}C$, unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS	LT1002AM/LT1002AC		LT1002M/LT1002C		UNITS	
			MIN	TYP	MAX	MIN		TYP
V_{OS}	Input Offset Voltage	Note 1		20	60	25	100	μV
$\frac{\Delta V_{OS}}{\Delta \text{Time}}$	Long Term Input Offset Voltage Stability	Notes 2 and 3		0.3	1.5	0.4	2.0	$\mu V/\text{month}$
I_{OS}	Input Offset Current			0.3	2.8	0.4	4.2	nA
I_B	Input Bias Current		± 0.6	± 3.0		± 0.7	± 4.5	nA
e_n	Input Noise Voltage	0.1Hz to 10Hz (Note 2)		0.35	0.7	0.38	0.75	μV_{p-p}
e_n	Input Noise Voltage Density	$f_o = 10\text{Hz}$ (Note 5) $f_o = 1000\text{Hz}$ (Note 2)		10.3 9.6	20.0 11.5	10.5 9.8	20.0 12.0	$nV\sqrt{\text{Hz}}$
A_{VOL}	Large Signal Voltage Gain	$R_L \geq 2k\Omega$, $V_o = \pm 12V$ $R_L \geq 1k\Omega$, $V_o = \pm 10V$	400 250	800 500		350 220	800 500	V/mV
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 13V$	110	126		110	126	dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 3V$ to $\pm 18V$	108	123		105	123	dB
R_{in}	Input Resistance Differential Mode	Note 4	20	100		13	80	M Ω
	Input Voltage Range		± 13	± 14		± 13	± 14	V
V_{OUT}	Maximum Output Voltage Swing	$R_L \geq 2k\Omega$ $R_L \geq 1k\Omega$	± 13 ± 12	± 14 ± 13.5		± 13 ± 12	± 14 ± 13.5	V
SR	Slew Rate	$R_L \geq 2k\Omega$ (Note 4)	0.1	0.25		0.1	0.25	V/ μs
GBW	Gain Bandwidth Product	Note 4	0.4	0.8		0.4	0.8	MHz
P_o	Power Dissipation per amplifier	No load No load, $V_S = \pm 3V$	46 4	75 7		48 4	85 8	mW

ELECTRICAL CHARACTERISTICS, INDIVIDUAL AMPLIFIERS

$V_S = \pm 15V$, $-55^\circ C \leq T_A \leq 125^\circ C$, unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS	LT1002AM			LT1002M			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	Note 1	●	30	150		45	230	μV
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Input Offset Voltage Drift		●	0.2	0.9		0.3	1.3	$\mu V/^\circ C$
I_{OS}	Input Offset Current		●	0.8	5.6		1.2	8.5	nA
I_B	Input Bias Current		●	± 1.0	± 6.0		± 1.5	± 9.0	nA
A_{VOL}	Large Signal Voltage Gain	$R_L \geq 2k\Omega$, $V_o = \pm 10V$	●	300	700		200	700	V/mV
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 13V$	●	106	122		104	120	dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 3V$ to $\pm 18V$	●	102	117		96	117	dB
	Input Voltage Range		●	± 13	± 14		± 13	± 14	V
V_{OUT}	Output Voltage Swing	$R_L \geq 2k\Omega$	●	± 12.5	± 13.5		± 12.0	± 13.5	V
P_d	Power Dissipation per amplifier	No load	●	55	90		60	100	mW

2

$V_S = \pm 15V$, $0^\circ C \leq T_A \leq 70^\circ C$, unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS	LT1002AC			LT1002C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	Note 1	●	20	100		30	160	μV
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Input Offset Voltage Drift		●	0.2	0.9		0.3	1.3	$\mu V/^\circ C$
I_{OS}	Input Offset Current		●	0.5	4.2		0.6	5.7	nA
I_B	Input Bias Current		●	± 0.7	± 4.5		± 1.0	± 6.0	nA
A_{VOL}	Large Signal Voltage Gain	$R_L \geq 2k\Omega$, $V_o = \pm 10V$	●	350	750		250	750	V/mV
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 13V$	●	108	124		106	123	dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 3V$ to $\pm 18V$	●	105	120		100	120	dB
	Input Voltage Range		●	± 13	± 14		± 13	± 14	V
V_{OUT}	Output Voltage Swing	$R_L \geq 2k\Omega$	●	± 12.5	± 13.8		± 12.5	± 13.8	V
P_d	Power Dissipation per amplifier	No load	●	50	85		55	90	mW

The ● denotes the specifications which apply over the full operating temperature range.

For MIL-STD components, please refer to LTC 883C data sheet for test listing and parameters.

Note 1: Offset voltage measured with high speed test equipment, approximately 1 second after power is applied.

Note 2: This parameter is tested on a sample basis only.

Note 3: Long Term Input Offset Voltage Stability refers to the averaged trend line of V_{OS} versus Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically $2.5\mu V$.

Note 4: Parameter is guaranteed by design.

Note 5: 10Hz noise voltage density is sample tested on every lot. Devices 100% tested at 10Hz are available on request.

Note 6: The $V+$ supply terminals are completely independent and may be powered by separate supplies if desired (this approach, however, would sacrifice the advantages of the power supply rejection ratio matching). The $V-$ supply terminals are both connected to the common substrate and must be tied to the same voltage. Both $V-$ pins should be used.

MATCHING CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25^\circ C$, unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS	LT1002AM/AC			LT1002M/C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
I_{b^+}	Input Offset Voltage Match		—	15	40	—	25	80	μV
	Average Non-Inverting Bias Current		—	± 0.6	± 3.5	—	± 0.7	± 4.8	nA
I_{os^+}	Non-Inverting Offset Current		—	0.6	3.5	—	0.7	6.0	nA
I_{os^-}	Inverting Offset Current		—	0.6	3.5	—	0.7	6.0	nA
$\Delta CMRR$	Common Mode Rejection Ratio Match	$V_{CM} = \pm 13V$	110	132	—	108	132	—	dB
$\Delta PSRR$	Power Supply Rejection Ratio Match	$V_S = \pm 3V$ to $\pm 18V$	108	130	—	102	128	—	dB
	Channel Separation	$f \leq 10Hz$ (Note 4)	132	148	—	130	146	—	dB

MATCHING CHARACTERISTICS at $V_S = \pm 15V$, $-55^\circ C \leq T_A \leq 125^\circ C$, unless otherwise noted

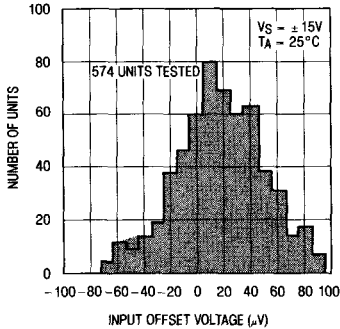
SYMBOL	PARAMETER	CONDITIONS	LT1002AM			LT1002M			UNITS	
			MIN	TYP	MAX	MIN	TYP	MAX		
I_{b^+}	Input Offset Voltage Match		●	—	50	140	—	60	230	μV
	Input Offset Voltage Tracking		●	—	0.3	1.0	—	0.4	1.5	$\mu V/^\circ C$
I_{os^+}	Average Non-Inverting Bias Current		●	—	± 1.5	± 6.0	—	± 1.8	± 10.0	nA
	Non-Inverting Offset Current		●	—	1.5	6.5	—	1.8	12.0	nA
I_{os^-}	Inverting Offset Current		●	—	1.5	6.5	—	1.8	12.0	nA
$\Delta CMRR$	Common Mode Rejection Ratio Match	$V_{CM} = \pm 13V$	●	106	126	—	102	124	—	dB
$\Delta PSRR$	Power Supply Rejection Ratio Match	$V_S = \pm 3V$ to $\pm 18V$	●	102	122	—	94	120	—	dB

MATCHING CHARACTERISTICS at $V_S = \pm 15V$, $0^\circ C \leq T_A \leq 70^\circ C$, unless otherwise noted

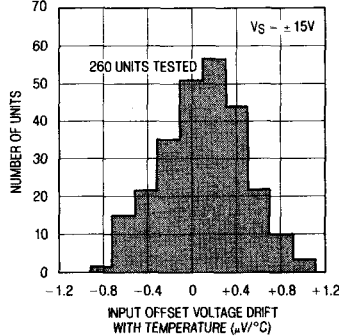
SYMBOL	PARAMETER	CONDITIONS	LT1002AC			LT1002C			UNITS	
			MIN	TYP	MAX	MIN	TYP	MAX		
I_{b^+}	Input Offset Voltage Match		●	—	30	85	—	45	150	μV
	Input Offset Voltage Tracking		●	—	0.3	1.0	—	0.4	1.5	$\mu V/^\circ C$
I_{os^+}	Average Non-Inverting Bias Current		●	—	± 1.0	± 4.5	—	± 1.2	± 7.0	nA
	Non-Inverting Offset Current		●	—	1.0	5.0	—	1.2	8.5	nA
I_{os^-}	Inverting Offset Current		●	—	1.0	5.0	—	1.2	8.5	nA
$\Delta CMRR$	Common Mode Rejection Ratio Match	$V_{CM} = \pm 13V$	●	108	130	—	105	128	—	dB
$\Delta PSRR$	Power Supply Rejection Ratio Match	$V_S = \pm 3V$ to $\pm 18V$	●	105	126	—	98	124	—	dB

TYPICAL PERFORMANCE CHARACTERISTICS

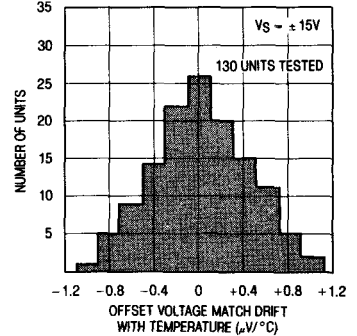
Distribution of Offset Voltage of Individual Amplifiers



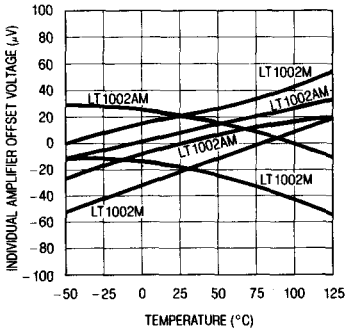
Distribution of Offset Voltage Drift with Temperature (Individual Amplifiers)



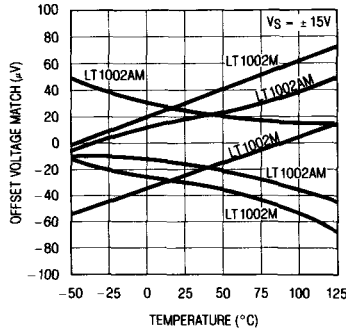
Distribution of Offset Voltage Match Drift with Temperature



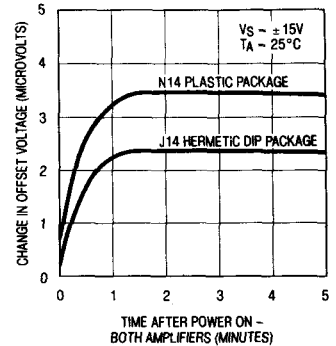
Offset Voltage Drift with Temperature of Six Representative Units



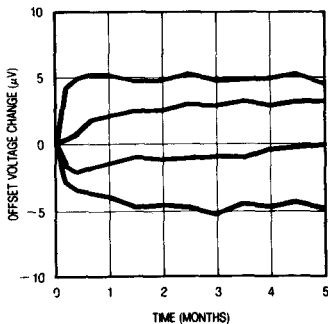
Offset Voltage Tracking with Temperature of Six Representative Units



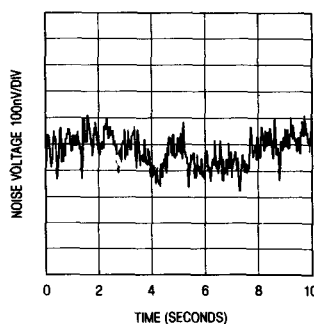
Warm-Up Drift



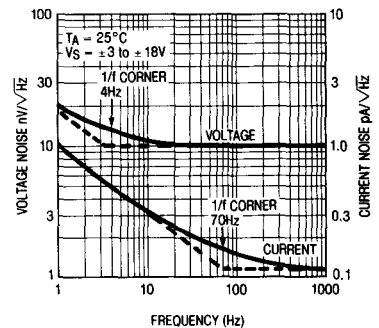
Long Term Stability of Four Representative Units



0.1Hz to 10Hz Noise

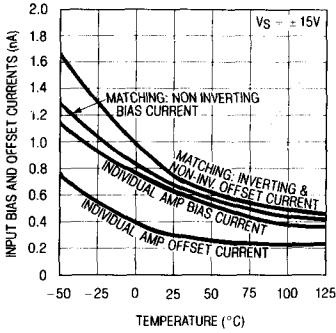


Noise Spectrum

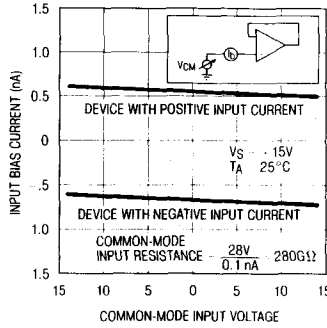


TYPICAL PERFORMANCE CHARACTERISTICS

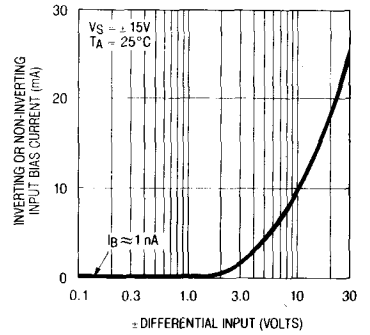
Matching and Individual Amplifier Bias and Offset Currents vs Temperature



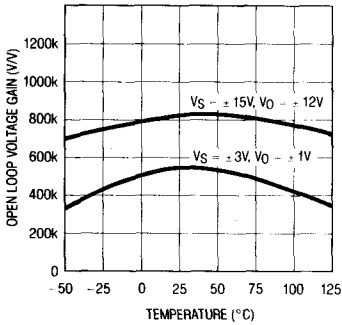
Input Bias Current Over the Common Mode Range



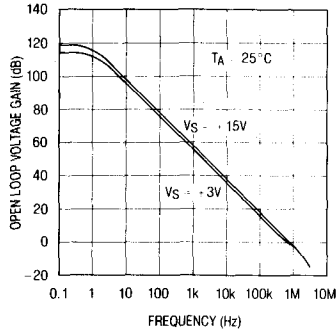
Input Bias Current vs. Differential Input Voltage



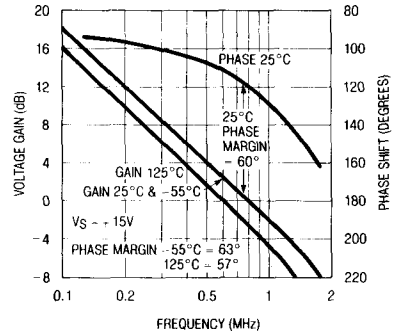
Open Loop Voltage Gain vs Temperature



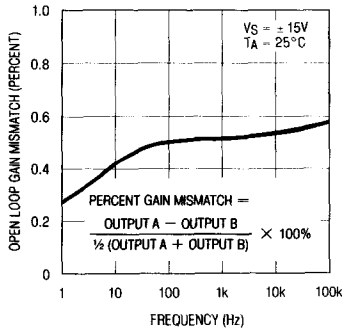
Open Loop Voltage Gain Frequency Response



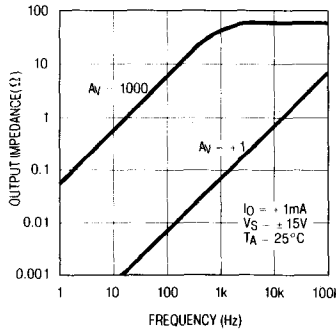
Gain, Phase Shift vs. Frequency



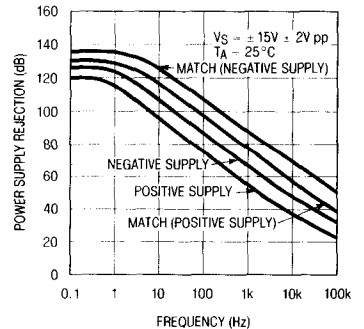
Open Loop Gain Mismatch vs Frequency



Closed Loop Output Impedance

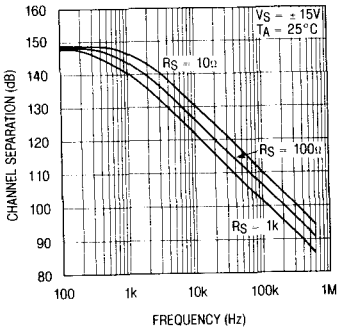


Power Supply Rejection and PSRR Match vs Frequency

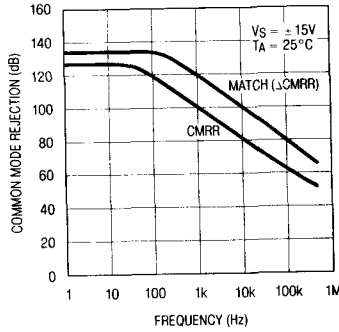


TYPICAL PERFORMANCE CHARACTERISTICS

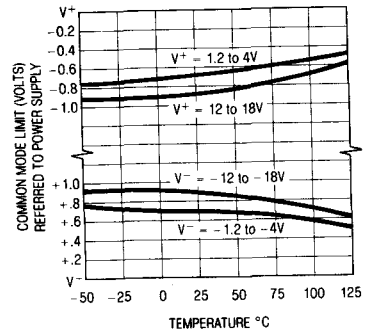
Channel Separation vs Frequency



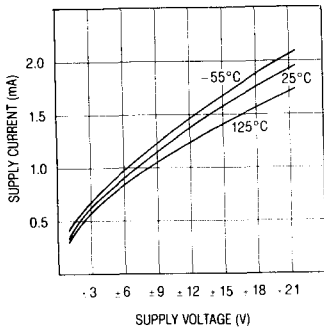
Common Mode Rejection and CMRR Match vs Frequency



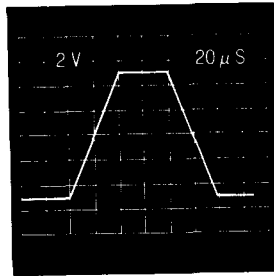
Common Mode Limit vs Temperature



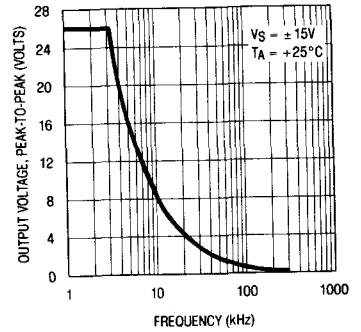
Supply Current vs. Supply Voltage For Each Amplifier



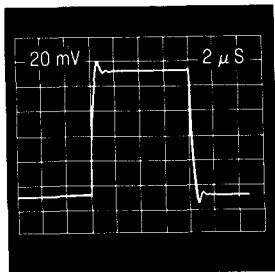
Large Signal Transient Response



Maximum Undistorted Output vs. Frequency

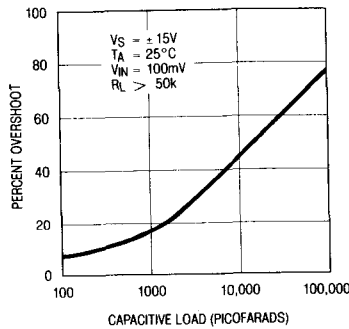


Small Signal Transient Response

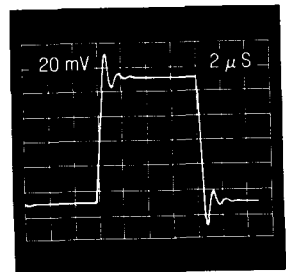


$A_V = +1, C_L = 50\text{pF}$

Voltage Follower Overshoot vs Capacitive Load



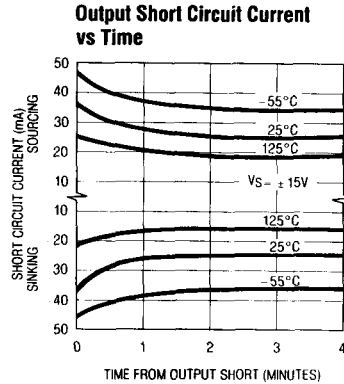
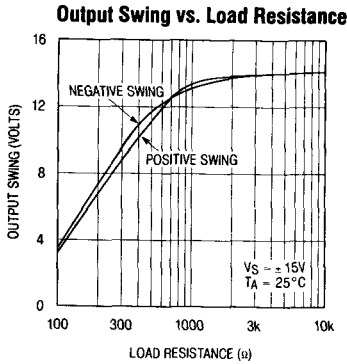
Small Signal Transient Response



$A_V = +1, C_L = 1000\text{pF}$

2

TYPICAL PERFORMANCE CHARACTERISTICS



APPLICATIONS INFORMATION

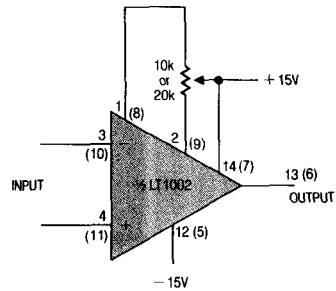
The LT1002 dual amplifier may be inserted directly into OP-10, OP207, OP227 sockets with or without removal of external nulling potentiometers.

Offset Voltage Adjustment The input offset voltage of the LT1002, and its drift with temperature, are permanently trimmed at wafer testing to a low level. However, if further adjustment of V_{OS} is necessary, nulling with a 10k or 20k potentiometer will not degrade drift with temperature. Trimming to a value other than zero creates a drift of $(V_{OS}/300) \mu V/^\circ C$, e.g. if V_{OS} is adjusted to $300 \mu V$, the change in drift will be $1 \mu V/^\circ C$. The adjustment range with a 10k or 20k pot is approximately $\pm 2.5mV$. If less adjustment range is needed, the sensitivity and resolution of the nulling can be improved by using a smaller pot in conjunction with fixed resistors. The example has an approximate null range of $\pm 100 \mu V$.

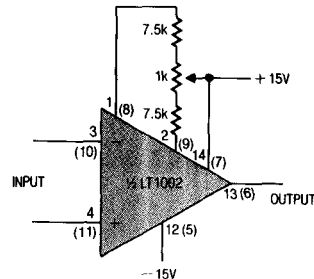
In matching applications, both amplifiers can be trimmed to zero, or the offset of one amplifier can be trimmed to match the offset of the other. Offset adjustment, however, slightly degrades the gain, common-mode and power-supply rejection match between the

two op amps. Fortunately, the guaranteed offset voltage match of the LT1002 is very low, in most applications offset adjustment will be unnecessary.

Standard Adjustment

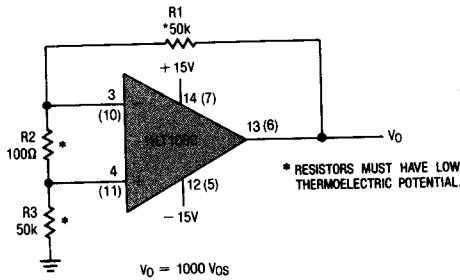


Improved Sensitivity Adjustment



APPLICATIONS INFORMATION

Test Circuit for Offset Voltage and its Drift with Temperature



This circuit is also used as the burn-in configuration for the LT1002, with supply voltages increased to $\pm 20V$, $R1 = R3 = 20k$, $R2 = 200\Omega$, $A_V = 100$.

Unless proper care is exercised, thermocouple effects, caused by temperature gradients across dissimilar metals at the contacts to the input terminals, can exceed the inherent drift of the amplifier. Air currents should be minimized, package leads should be short, the two input leads should be as close together as possible and maintained at the same temperature.

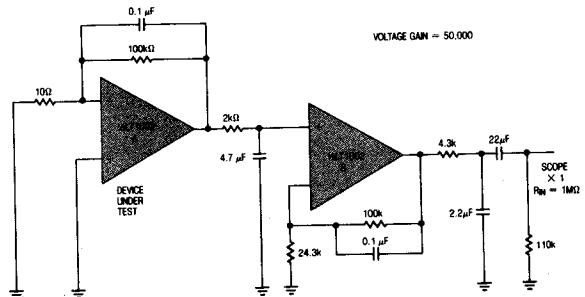
Channel Separation

This parameter is defined as the ratio of the change in input offset voltage of one amplifier to the change in output voltage of the other amplifier causing the offset change.

At low frequencies the LT1002's channel separation is an almost unmeasurable 148dB. As frequency increases, pin to pin capacitance of the package, between the output of one amplifier and the inputs of the other, becomes dominant. Since these pins are non-adjacent, the capacitance is only 0.02pF. To maintain the LT1002's excellent channel separation at higher frequencies, the socket and PC board capacitances should be minimized.

0.1Hz to 10Hz Noise Test Circuit

The device under test should be warmed up for three minutes and shielded from air currents. Turn the device 180° to measure the noise of side B.



(Peak to Peak noise measured in 10 Sec interval)

2

Power supplies

The LT1002 is specified over a wide range of power supply voltages from $\pm 3V$ to $\pm 18V$. Operation with lower supplies is possible, down to $\pm 1.2V$ (two Ni-Cad batteries). However, with $\pm 1.2V$ supplies, the device is stable only in closed loop gains of +2 or higher (or inverting gain of one or higher).

The $V+$ supply terminals are completely independent and may be powered by separate supplies if desired (this approach, however, would sacrifice the advantages of the power supply rejection ratio matching). The $V-$ supply terminals are both connected to the common substrate and must be tied to the same voltage. Both $V-$ pins should be used.

APPLICATIONS INFORMATION

Advantages of Matched Dual Op Amps In many applications the performance of a system depends on the matching between two operational amplifiers rather than the individual characteristics of the two op amps. Two or three op amp instrumentation amplifiers, tracking voltage references and low drift active filters are some of the circuits requiring matching between two op amps.

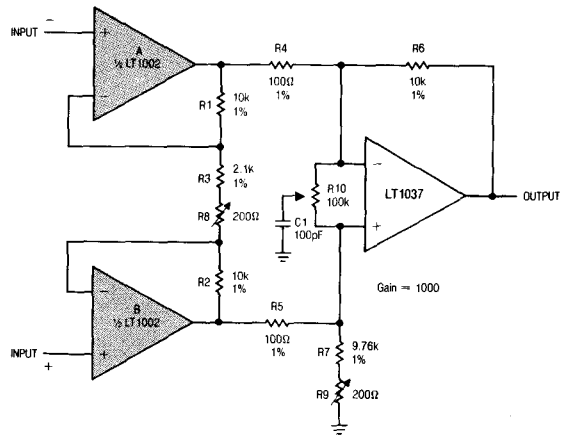
The well-known triple op amp configuration illustrates these concepts. Output offset is a function of the difference between the offsets of the two halves of the LT1002. This error cancellation principle holds for a considerable number of input referred parameters in addition to offset voltage and its drift with temperature. Input bias current will be the average of the two non-inverting input currents (I_{B^+}). The difference between these two currents (I_{OS^+}) is the offset current of the instrumentation amplifier. The difference between the inverting input currents (I_{OS^-}) will cause errors flowing through R1, R2, and R3. Common-mode and power supply rejections will be dependent only on the match between the two amplifiers (assuming perfect resistor matching).

The concepts of common mode and power supply rejection ratio match ($\Delta CMRR$ and $\Delta PSRR$) are best demonstrated with a numerical example:

Assume $CMRR_A = +1.0\mu V/V$ or 120dB,
and $CMRR_B = +0.75\mu V/V$ or 122.5dB,
then $\Delta CMRR = 0.25\mu V/V$ or 132dB;
if $CMRR_B = -0.75\mu V/V$ which is still 122.5dB,
then $\Delta CMRR = 1.75\mu V/V$ or 115dB.

Clearly, the LT1002, by specifying and guaranteeing all of these matching parameters, can significantly improve the performance of matching dependent circuits.

Three Op Amp Instrumentation Amplifier



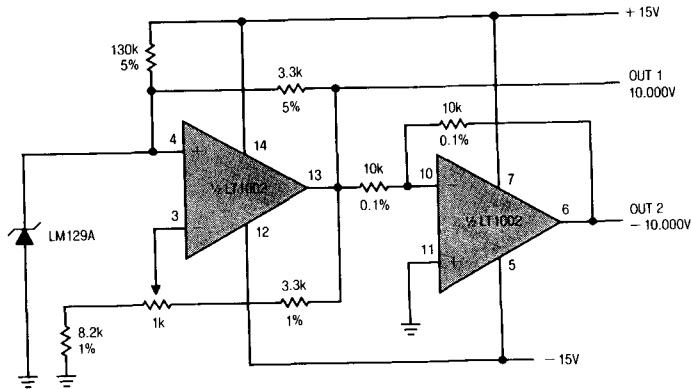
- Trim R8 for gain
- Trim R9 for DC common mode rejection
- Trim R10 for AC common mode rejection

Typical performance of the instrumentation amplifier:

- Input offset voltage = $25\mu V$
- Input bias current = $0.7nA$
- Input resistance = $200 G\Omega$
- Input offset current = $0.6nA$
- Input noise = $0.5\mu V$ p-p
- Power bandwidth ($V_0 = \pm 10V$) = 80kHz

APPLICATIONS INFORMATION

Precision $\pm 10V$ Reference

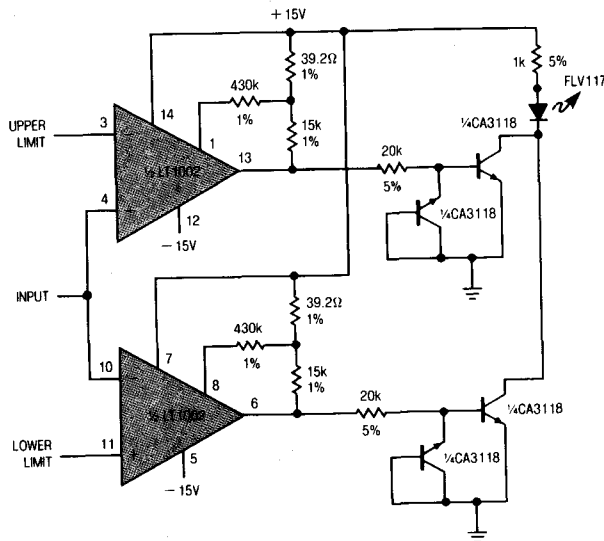


2

The LT1002 contributes less than 5% of the total drift with temperature, noise and long term drift of the ref-

erence. The accuracy of the $-10V$ output is limited by the matching of the two 10k resistors.

Dual Limit Microvolt Comparator

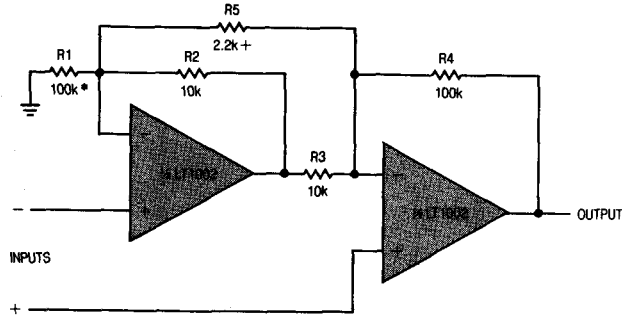


When the upper or lower limit is exceeded the LED lights up. Positive feedback to one of the nulling terminals creates 5 to 20 μV of hysteresis on both amplifiers. This feedback changes the offset voltage of the

LT1002 by less than 5 μV . Therefore, the basic accuracy of the comparator is limited only by the low offset voltage of the LT1002.

APPLICATIONS INFORMATION

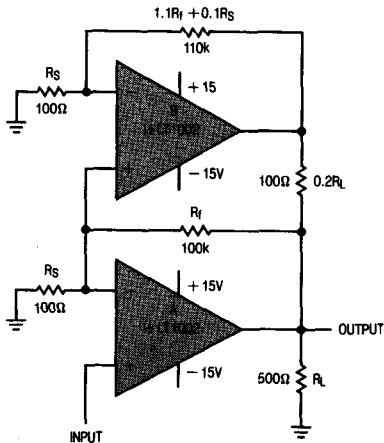
Two Op Amp Instrumentation Amplifier



* TRIM FOR COMMON-MODE REJECTION
 + TRIM FOR GAIN

$$\text{Gain} = \frac{R_4}{R_3} \left[1 + \frac{1}{2} \left(\frac{R_2}{R_1} + \frac{R_3}{R_4} \right) + \frac{R_2 + R_3}{R_5} \right] \approx 100$$

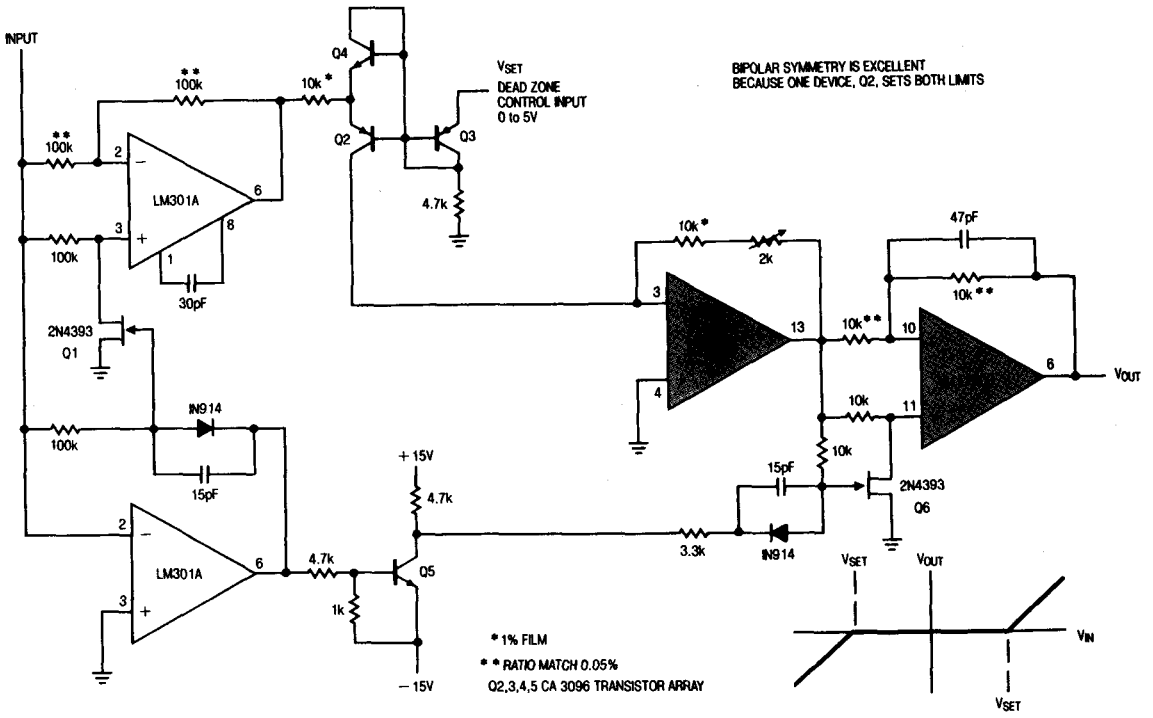
Precision Amplifier Drives 500Ω Load to ±10V



This application utilizes the guaranteed 10mA load driving capability of the LT1002. The offset voltage of amplifier A is the offset of the configuration. Amplifier B provides the additional 10mA load current. When load resistor R_L is removed, amplifier A sinks this current without affecting accuracy. In the gain of 1000 configuration shown, approximately 0.3% gain accuracy can be realized.

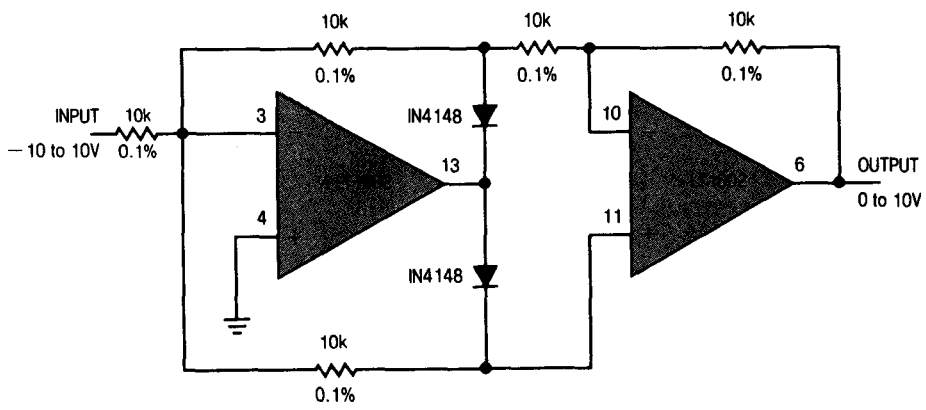
APPLICATIONS INFORMATION

Dead Zone Generator



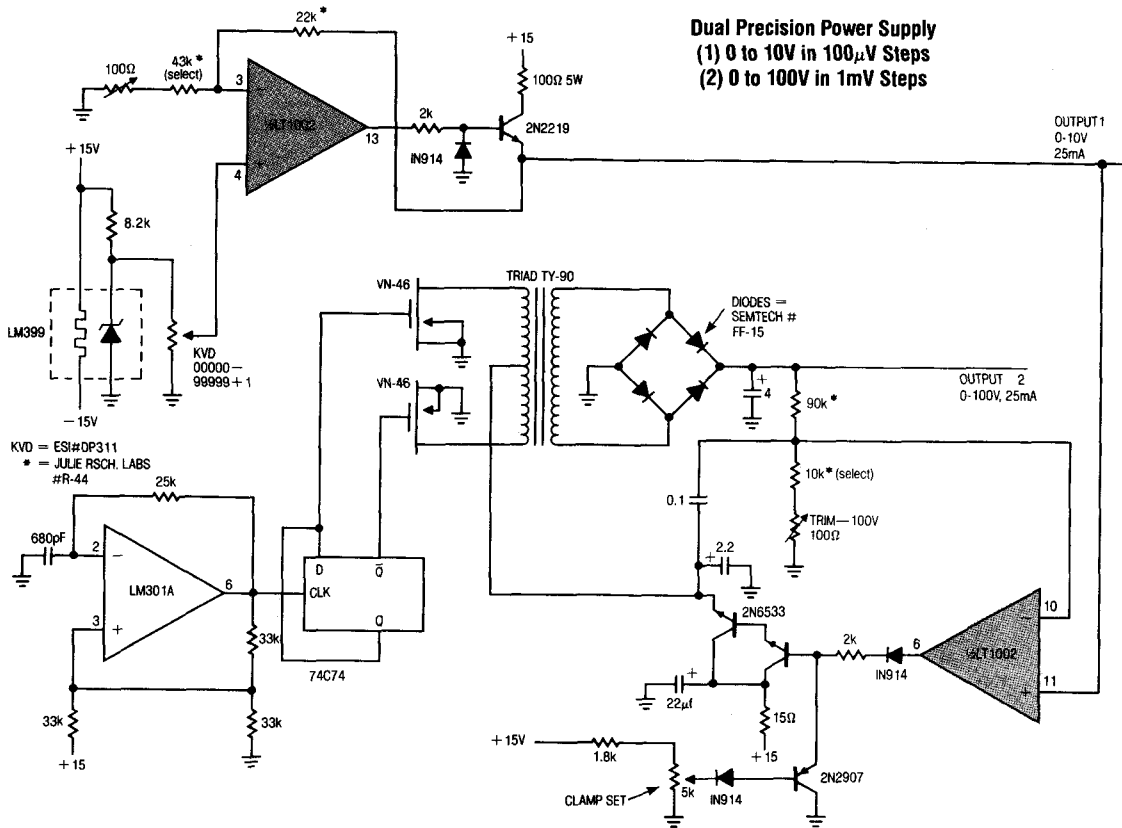
2

Precision Absolute Value Circuit



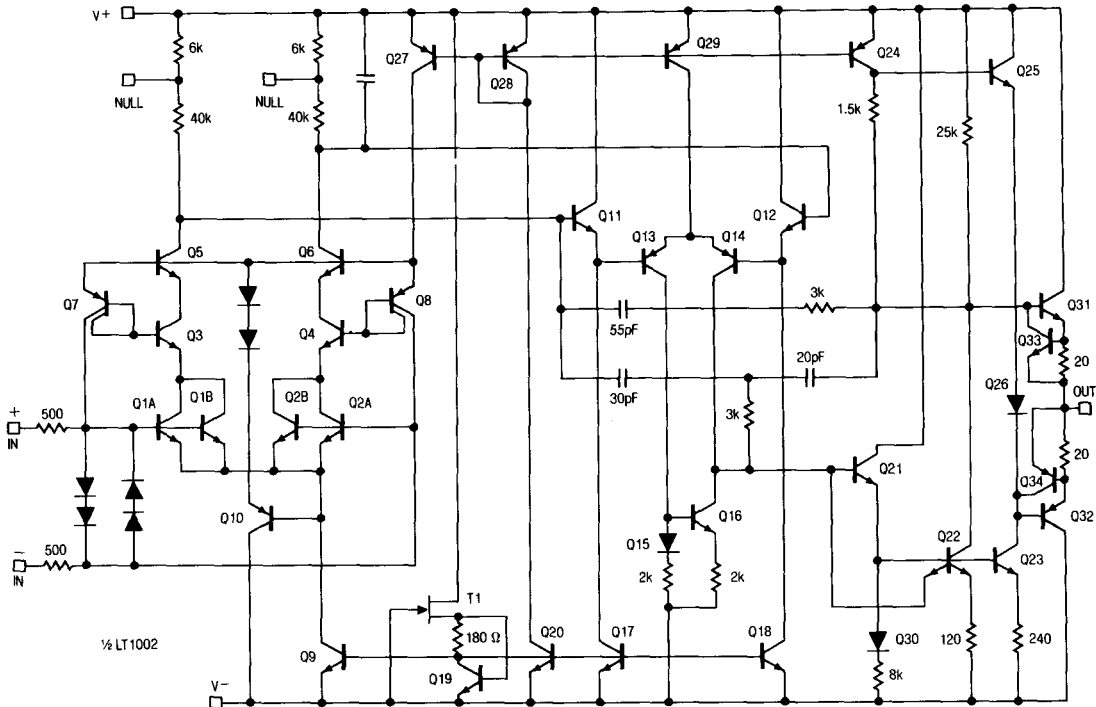
APPLICATIONS INFORMATION

Dual Precision Power Supply
 (1) 0 to 10V in 100 μ V Steps
 (2) 0 to 100V in 1mV Steps



KVD = ESI#DP311
 * = JULIE ROSCH LABS #R-44

SCHEMATIC DIAGRAM

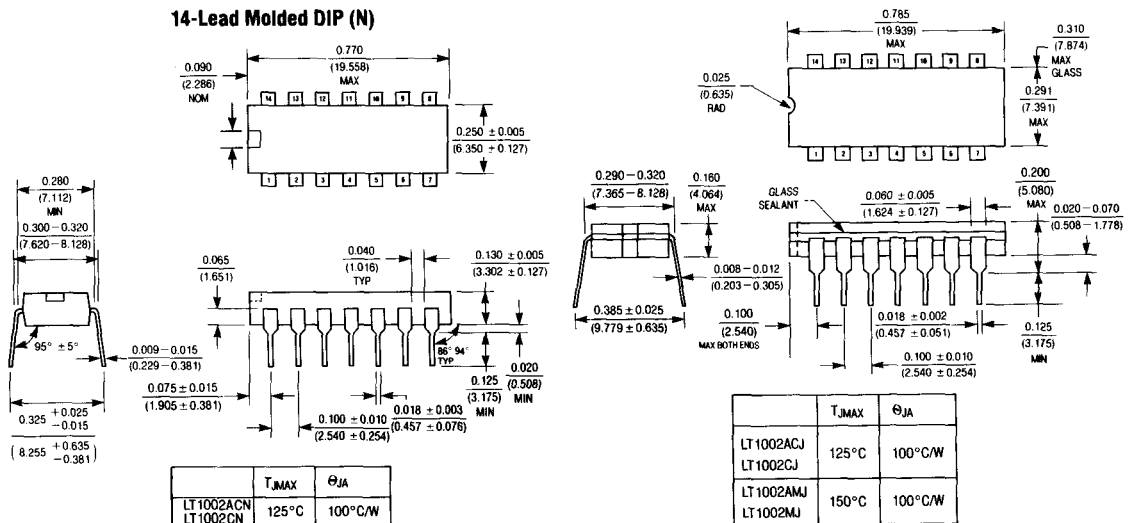


2

PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

14-Lead Cavity DIP (J)

14-Lead Molded DIP (N)



NOTES

FEATURES

- Single Supply Operation
 - Input Voltage Range Extends to Ground
 - Output Swings to Ground while Sinking Current
- *Guaranteed* Offset Voltage 50 μ V Max.
- *Guaranteed* Low Drift 1.3 μ V/ $^{\circ}$ C Max.
- *Guaranteed* Offset Current 0.5nA Max.
- *Guaranteed* High Gain
 - 5mA Load Current 1.5 Million Min.
 - 17mA Load Current 0.8 Million Min.
- *Guaranteed* Low Supply Current 520 μ A Max.
- Supply Current can be Reduced by a Factor of 4
- Low Voltage Noise, 0.1Hz to 10Hz 0.55 μ Vp-p
 - Low Current Noise—
 - Better than OP-07 0.07pA/ $\sqrt{\text{Hz}}$ at 10Hz
- High Input Impedance 250M Ω Min.
- *Guaranteed* Minimum Supply Voltage 2.7V Min.

APPLICATIONS

- Low Power Sample and Hold Circuits
- Battery Powered Precision Instrumentation
 - Strain Gauge Signal Conditioners
 - Thermocouple Amplifiers
- 4mA–20mA Current Loop Transmitters
- Active Filters

DESCRIPTION

The LT1006 is the first precision single supply operational amplifier. Its design has been optimized for single supply operation with a full set of specifications at 5V. Specifications at ± 15 V are also provided.

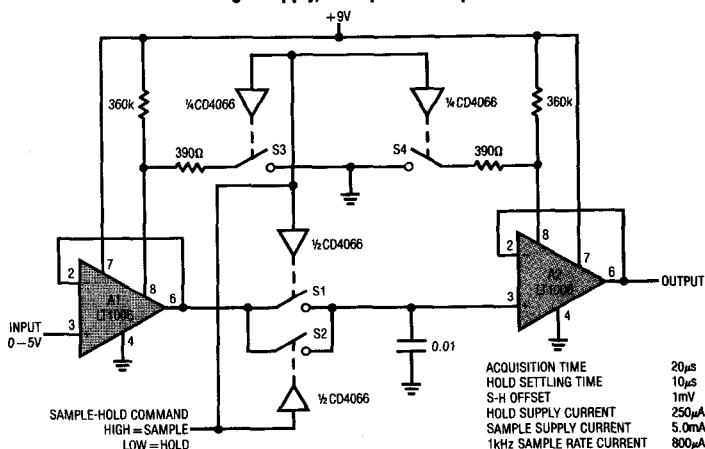
The LT1006 has low offset voltage of 20 μ V, drift of 0.2 μ V/ $^{\circ}$ C, offset current of 120pA, gain of 2.5 million, common-mode rejection of 114dB, and power supply rejection of 126dB.

Although supply current is only 340 μ A, a novel output stage can source or sink in excess of 20mA while retaining high voltage gain. Common-mode input range includes ground to accommodate low ground-referenced inputs from strain gauges or thermocouples, and output can swing to within a few millivolts of ground. If higher slew rate (in excess of 1V/ μ s) or micropower operation (supply current down to 90 μ A) is required, the operating currents can be modified by connecting an external optional resistor to Pin 8.

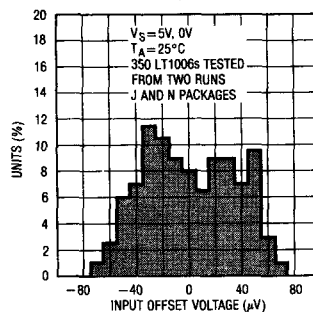
For similar single supply precision dual and quad op amps, please see the LT1013/LT1014 data sheet. For micropower dual and quad op amps, please see the LT1078/LT1079 data sheet.

2

LT1006 Single Supply, Micropower Sample and Hold



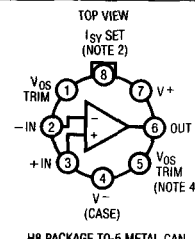
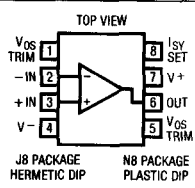
Distribution of Input Offset Voltage



ABSOLUTE MAXIMUM RATINGS

Supply Voltage $\pm 2V$
 Input Voltage Equal to Positive Supply Voltage
 5V Below Negative Supply Voltage
 Differential Input Voltage 30V
 Output Short Circuit Duration Indefinite
 Operating Temperature Range
 LT1006AM, M $-55^{\circ}C$ to $125^{\circ}C$
 LT1006AC, C $0^{\circ}C$ to $70^{\circ}C$
 Storage Temperature Range
 All Devices $-65^{\circ}C$ to $150^{\circ}C$
 Lead Temperature (Soldering, 10 sec) $300^{\circ}C$

PACKAGE/ORDER INFORMATION

 <p>TOP VIEW I_{SY-SET} (NOTE 2) V_{OS} TRIM $-IN$ $+IN$ $V-$ (CASE) V_{OS} TRIM (NOTE 4) $V+$ OUT H8 PACKAGE TO-5 METAL CAN</p>	ORDER PART NUMBER
	LT1006AMH LT1006MH LT1006ACH LT1006CH
 <p>TOP VIEW V_{OS} TRIM $-IN$ $+IN$ $V-$ V_{OS} TRIM (NOTE 4) OUT $V+$ $ISY-SET$ J8 PACKAGE HERMETIC DIP N8 PACKAGE PLASTIC DIP</p>	LT1006AMJ8 LT1006MJ8 LT1006ACJ8 LT1006CJ8 LT1006CN8

ELECTRICAL CHARACTERISTICS $V_S = 5V, V_{CM} = 0V, V_{OUT} = 1.4V, T_A = 25^{\circ}C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1006AM/AC			LT1006M/C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage			20	50		30	80	μV
$\frac{\Delta V_{OS}}{\Delta Time}$	Long Term Input Offset Voltage Stability			0.4			0.5		$\mu V/Mo$
I_{OS}	Input Offset Current			0.12	0.5		0.15	0.9	nA
I_B	Input Bias Current			9	15		10	25	nA
e_n	Input Noise Voltage	0.1Hz to 10Hz		0.55			0.55		$\mu Vp-p$
	Input Noise Voltage Density	$f_o = 10Hz$ (Note 3) $f_o = 1000Hz$ (Note 3)		23	32		23	32	nV/ \sqrt{Hz}
				22	25		22	25	nV/ \sqrt{Hz}
I_n	Input Noise Current Density	$f_o = 10Hz$		0.07			0.08		pA/ \sqrt{Hz}
	Input Resistance Differential Mode Common-Mode	(Note 1)	180	400		100	300		M Ω G Ω
	Input Voltage Range		3.5	3.8		3.5	3.8		V
			0	-0.3		0	-0.3		V
CMRR	Common-Mode Rejection Ratio	$V_{CM} = 0V$ to 3.5V	100	114		97	112		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 2V$ to $\pm 18V, V_O = 0V$	106	126		103	124		dB
A_{VOL}	Large Signal Voltage Gain	$V_O = 0.03V$ to 4V, $R_L = 10k$ $V_O = 0.03V$ to 3.5V, $R_L = 2k$	1.0	2.5		0.7	2.0		$V/\mu V$
			0.5	2.0		0.3	1.8		$V/\mu V$
	Maximum Output Voltage Swing	Output Low, No Load		15	25		15	25	mV
		Output Low, 600 Ω to GND		5	10		5	10	mV
		Output Low, $I_{SINK} = 1mA$		220	350		220	350	mV
		Output High, No Load	4.0	4.4		4.0	4.4		V
		Output High, 600 Ω to GND	3.4	4.0		3.4	4.0		V
SR	Slew Rate		0.25	0.4		0.25	0.4		$V/\mu s$
I_S	Supply Current	$R_{SET} = \infty$ $R_{SET} = 180k$ Pin 8 to Pin 7 (Note 2)		340	520		350	570	μA μA
	Minimum Supply Voltage		2.7			2.7			V

ELECTRICAL CHARACTERISTICS

$V_S = 5V, 0V, V_{CM} = 0.1V, V_O = 1.4V, -55^\circ C \leq T_A \leq 125^\circ C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LT1006AM			LT1006M			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage		●	40	180		60	250	μV	
$\frac{\Delta V_{OS}}{\Delta Temp}$	Input Offset Voltage Drift		●	0.2	1.3		0.3	1.8	$\mu V/^\circ C$	
I_{OS}	Input Offset Current		●	0.4	2.0		0.5	4.0	nA	
I_B	Input Bias Current		●	13	25		16	40	nA	
A_{VOL}	Large Signal Voltage Gain	$V_O = 0.05V$ to $3.5V, R_L = 2k$	●	0.25	0.8		0.15	0.7	$V/\mu V$	
CMRR	Common-Mode Rejection Ratio	$V_{CM} = 0.1V$ to $3.2V$	●	90	103		87	102	dB	
PSRR	Power Supply Rejection Ratio	$V_S = \pm 2V$ to $\pm 18V, V_O = 0V$	●	100	117		97	116	dB	
	Maximum Output Voltage Swing	Output Low, 600 Ω to GND Output High, 600 Ω to GND	● ●	3.2	6 3.8	15	3.1	6 3.8	mV V	
I_S	Supply Current		●	380	630		400	680	μA	

2

ELECTRICAL CHARACTERISTICS

$V_S = 5V, 0V, V_{CM} = 0V, V_O = 1.4V, 0^\circ C \leq T_A \leq 70^\circ C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LT1006AC			LT1006C			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	LT1006N8	● ●	30	110		45	160	μV μV	
$\frac{\Delta V_{OS}}{\Delta Temp}$	Input Offset Voltage Drift	LT1006N8	● ●	0.2	1.3		0.3	1.8	$\mu V/^\circ C$ $\mu V/^\circ C$	
I_{OS}	Input Offset Current		●	0.25	1.2		0.3	2.5	nA	
I_B	Input Bias Current		●	11	20		12	30	nA	
A_{VOL}	Large Signal Voltage Gain	$V_O = 0.04V$ to $3.5V, R_L = 2k$	●	0.35	1.3		0.25	1.2	$V/\mu V$	
CMRR	Common-Mode Rejection Ratio	$V_{CM} = 0V$ to $3.4V$	●	96	109		92	108	dB	
PSRR	Power Supply Rejection Ratio	$V_S = \pm 2V$ to $\pm 18V, V_O = 0V$	●	101	120		97	118	dB	
	Maximum Output Voltage Swing	Output Low, 600 Ω to GND Output High, 600 Ω to GND	● ●	3.3	6 3.9	13	3.2	6 3.9	mV V	
I_S	Supply Current		●	350	570		360	620	μA	

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: This parameter is guaranteed by design and is not tested.

Note 2: Regular operation does not require an external resistor. In order to program the supply current for low power or high speed operation, connect an external resistor from Pin 8 to Pin 7 or from Pin 8 to Pin 4, respectively. Supply current specifications (for $R_{SET} = 180k$) do not include current in R_{SET} .

Note 3: This parameter is tested on a sample basis only. All noise parameters are tested with $V_S = \pm 2.5V, V_O = 0V$.

Note 4: Optional offset nulling is accomplished with a potentiometer connected between the trim terminals and the wiper to V^- . A 10k pot (providing a null range of $\pm 6mV$) is recommended for minimum drift of nullified offset voltage with temperature. For increased trim resolution and accuracy, two fixed resistors can be used in conjunction with a smaller potentiometer. For example: two 4.7k resistors tied to pins 1 and 5, with a 500 Ω pot in the middle, will have a null range of $\pm 150\mu V$.

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V, T_A = 25^\circ C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1006AM/AC			LT1006M/C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage			30	100		50	180	μV
I_{OS}	Input Offset Current			0.1	0.5		0.15	0.9	nA
I_B	Input Bias Current			7.5	12.0		8.0	20.0	nA
	Input Voltage Range		13.5	13.8		13.5	13.8		V
			-15.0	-15.3		-15.0	-15.3		V
CMRR	Common-Mode Rejection Ratio	$V_{CM} = +13.5V, -15V$	100	117		97	116		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 2V$ to $\pm 18V, V_O = 0V$	106	126		103	124		dB
A_{VOL}	Large Signal Voltage Gain	$V_O = \pm 10V, R_L = 2k$ $V_O = \pm 10V, R_L = 600\Omega$	1.5	5.0		1.2	4.0		$V/\mu V$
			0.8	1.5		0.5	1.0		$V/\mu V$
V_{OUT}	Maximum Output Voltage Swing	$R_L = 2k$	± 13	± 14		± 12.5	± 14		V
SR	Slew Rate	$R_{SET} = \infty$ $R_{SET} = 390\Omega$ Pin 8 to Pin 4	0.25	0.4		0.25	0.4		$V/\mu s$
			1.0	1.2		1.0	1.2		$V/\mu s$
I_S	Supply Current			360	540		360	600	μA

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V, -55^\circ C \leq T_A \leq 125^\circ C$, unless otherwise noted.

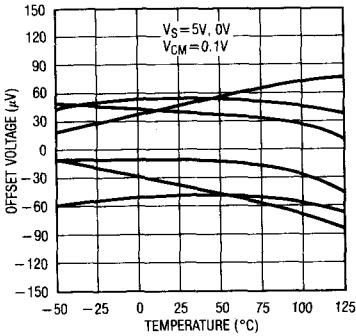
SYMBOL	PARAMETER	CONDITIONS	LT1006AM			LT1006M			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage		●	80	320		110	460	μV
$\frac{\Delta V_{OS}}{\Delta Temp}$	Input Offset Voltage Drift		●	0.5	2.2		0.6	2.8	$\mu V/^\circ C$
I_{OS}	Input Offset Current		●	0.2	2.0		0.3	3.0	nA
I_B	Input Bias Current		●	9	18		11	27	nA
A_{VOL}	Large Signal Voltage Gain	$V_O = \pm 10V, R_L = 2k$	●	0.5	1.5		0.25	1.0	$V/\mu V$
CMRR	Common-Mode Rejection Ratio	$V_{CM} = +13V, -14.9V$	●	97	114		94	113	dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 2V$ to $\pm 18V, V_O = 0V$	●	100	117		97	116	dB
	Maximum Output Voltage Swing	$R_L = 2k$	●	± 12	± 13.8		± 11.5	± 13.8	V
I_S	Supply Current		●	400	650		400	750	μA

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V, 0^\circ C \leq T_A \leq 70^\circ C$, unless otherwise noted.

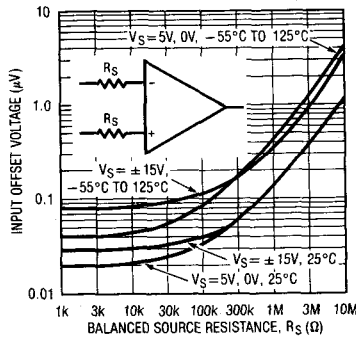
SYMBOL	PARAMETER	CONDITIONS	LT1006AC			LT1006C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	LT1006N8	●	50	200		75	300	μV
			●				80	330	μV
$\frac{\Delta V_{OS}}{\Delta Temp}$	Input Offset Voltage Drift	LT1006N8	●	0.5	2.2		0.6	2.8	$\mu V/^\circ C$
			●				0.7	3.5	$\mu V/^\circ C$
I_{OS}	Input Offset Current		●	0.15	1.0		0.25	2.0	nA
I_B	Input Bias Current		●	8.0	15		10	23	nA
A_{VOL}	Large Signal Voltage Gain	$V_O = \pm 10V, R_L = 2k$	●	1.0	3.0		0.7	2.5	$V/\mu V$
CMRR	Common-Mode Rejection Ratio	$V_{CM} = 13V, -15V$	●	98	116		94	114	dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 2V$ to $\pm 18V, V_O = 0V$	●	101	120		97	118	dB
	Maximum Output Voltage Swing	$R_L = 2k$	●	± 12.5	± 13.9		± 11.5	± 13.8	V
I_S	Supply Current		●	370	600		380	660	μA

TYPICAL PERFORMANCE CHARACTERISTICS

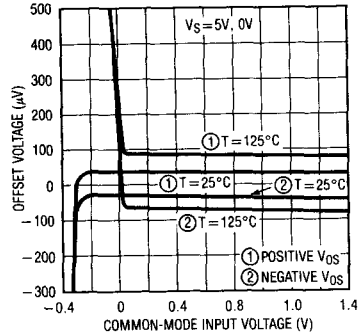
Offset Voltage Drift with Temperature of Representative Units



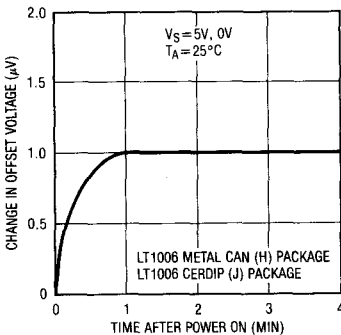
Offset Voltage vs Balanced Source Resistor



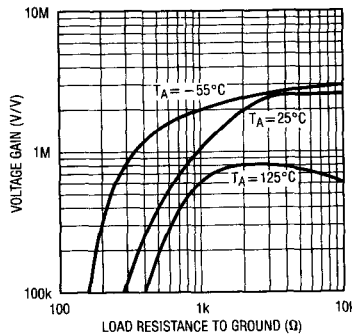
V_{OS} vs Common-Mode Voltage vs Temperature



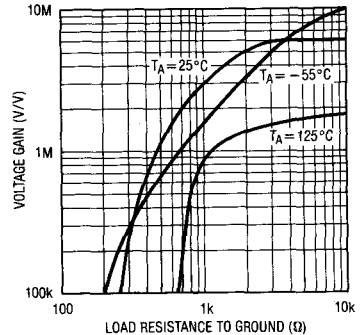
Warm-Up Drift



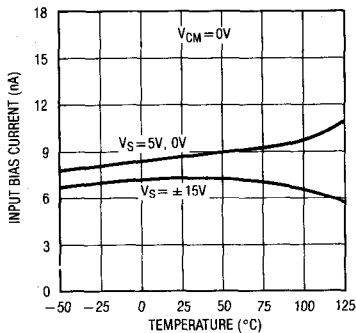
Voltage Gain vs Load Resistance, $V_S = 5V, 0V$



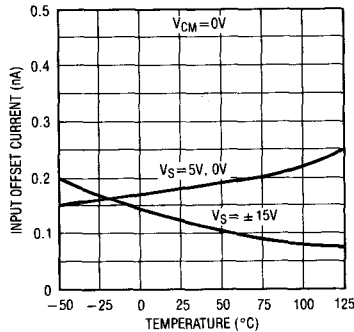
Voltage Gain vs Load Resistance with $V_S = \pm 15V$



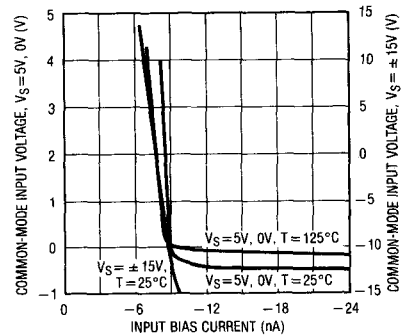
Input Bias Current vs Temperature



Input Offset Current vs Temperature

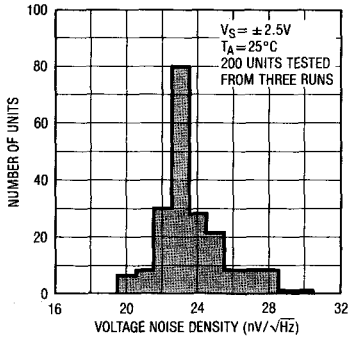


Input Bias Current vs Common-Mode Voltage

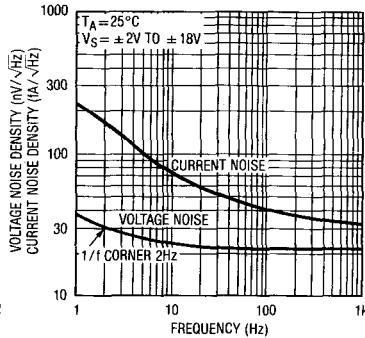


TYPICAL PERFORMANCE CHARACTERISTICS

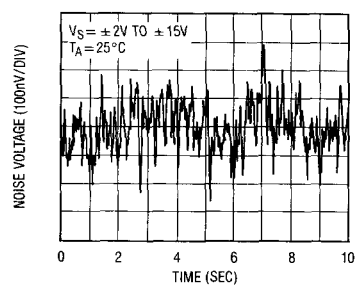
10Hz Voltage Noise Distribution



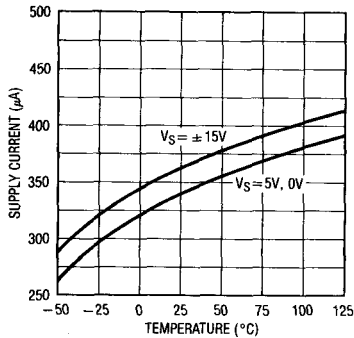
Noise Spectrum



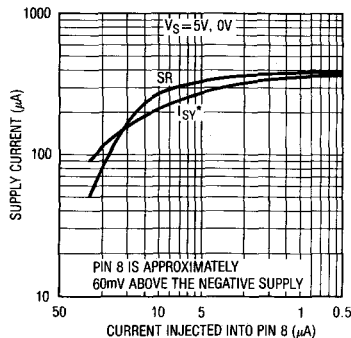
0.1Hz to 10Hz Noise



Supply Current vs Temperature

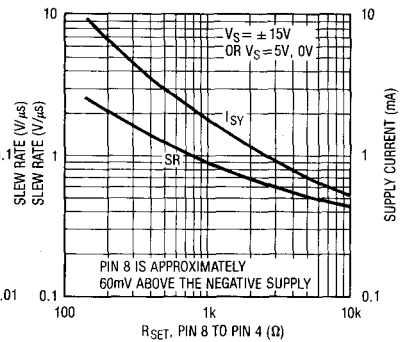


Reducing Power Dissipation

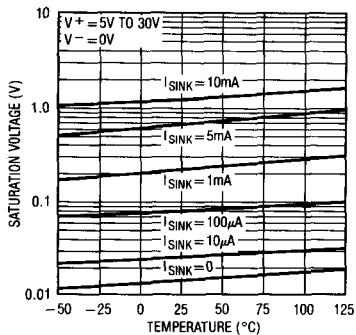


* I_{SV} DOES NOT INCLUDE CURRENT THROUGH R_{SET}

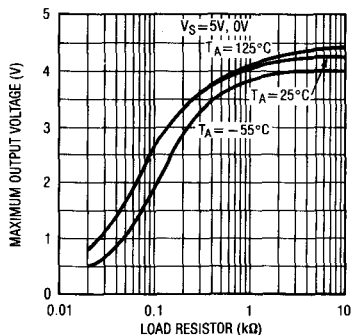
Increasing Slew Rate (R_{SET} to V^-)



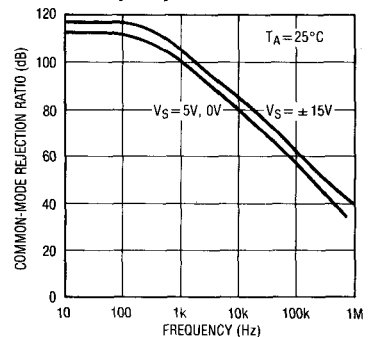
Output Saturation vs Sink Current vs Temperature



Maximum Output Swing vs Load Resistor

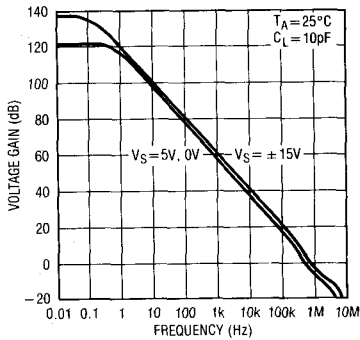


Common-Mode Rejection Ratio vs Frequency

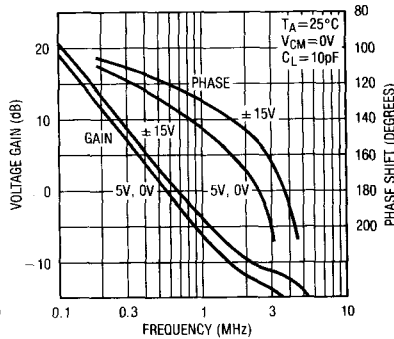


TYPICAL PERFORMANCE CHARACTERISTICS

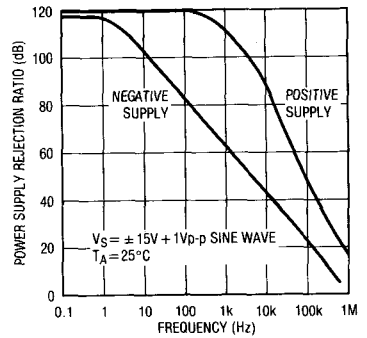
Voltage Gain vs Frequency



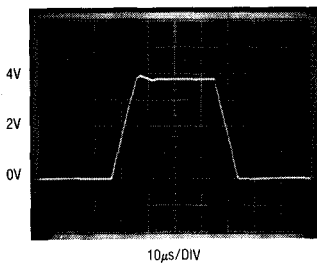
Gain, Phase vs Frequency



Power Supply Rejection Ratio vs Frequency

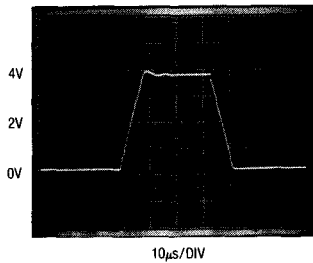


Large Transient Response, VS = 5V, 0V



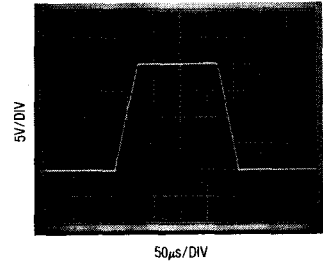
$A_V = 1$
 $R_L = 4.7k \text{ TO } 5V$
 INPUT = 0V TO 3.8V

Large Signal Transient Response, VS = 5V, 0V



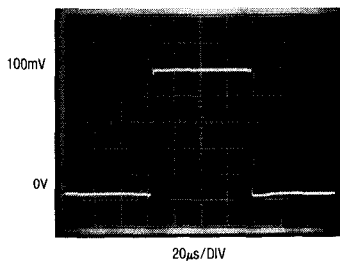
$A_V = 1$
 $R_L = 4.7k \text{ TO GROUND}$
 INPUT = 0V TO 3.8V

Large Signal Transient Response, VS = ±15V



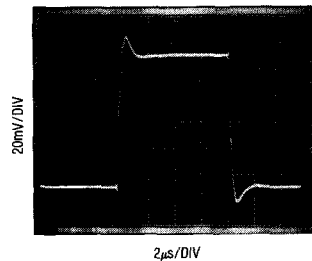
$A_V = 1$

Small Signal Transient Response, VS = 5V, 0V



$A_V = 1$
 $C_L = 10pF$
 $R_L = 600\Omega \text{ TO GND}$
 INPUT = 0V TO 100mV PULSE

Small Signal Transient Response, VCC = ±2.5V TO ±15V



$A_V = 1$
 $C_L = 10pF$

2

APPLICATIONS INFORMATION

The LT1006 is fully specified for single supply operation, i.e., when the negative supply is 0V. Input common-mode range includes ground; the output swings within a few millivolts of ground. Single supply operation, however, can create special difficulties, both at the input and at the output. The LT1006 has specific circuitry which addresses these problems.

At the input, the driving signal can fall below 0V—inadvertently or on a transient basis. If the input is more than a few hundred millivolts below ground, two distinct problems can occur on previous single supply designs, such as the LM124, LM158, OP-20, OP-21, OP-220, OP-221, OP-420:

- a) When the input is more than a diode drop below ground, unlimited current will flow from the substrate (V^- terminal) to the input. This can destroy the unit. On the LT1006, the 400 Ω resistors, in series with the input (see schematic diagram), protect the devices even when the input is 5V below ground.
- b) When the input is more than 400mV below ground (at 25°C), the input stage saturates (transistors Q3 and Q4)

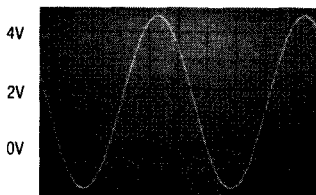
and phase reversal occurs at the output. This can cause lock-up in servo systems. Due to a unique phase reversal protection circuitry (Q21, Q22, Q27, Q28), the LT1006's output does not reverse, as illustrated below, even when the inputs are at $-1.5V$.

At the output, the aforementioned single supply designs either cannot swing to within 600mV of ground (OP-20) or cannot sink more than a few microamperes while swinging to ground (LM124, LM158). The LT1006's all-NPN output stage maintains its low output resistance and high gain characteristics until the output is saturated.

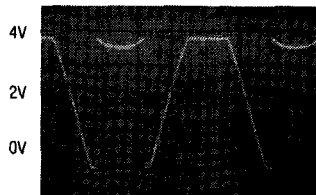
In dual supply operations, the output stage is crossover distortion-free.

Since the output cannot go exactly to ground, but can only approach ground to within a few millivolts, care should be exercised to ensure that the output is not saturated. For example, a 1mV input signal will cause the amplifier to set up in its linear region in the gain 100 configuration shown below, but is not enough to make the amplifier function properly in the voltage follower mode.

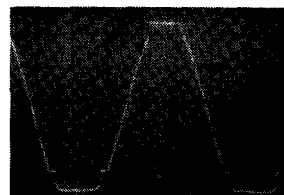
Voltage Follower with Input Exceeding the Negative Common-Mode Range ($V_S = 5V, 0V$)



6Vp-p INPUT, $-1.5V$ TO $4.5V$

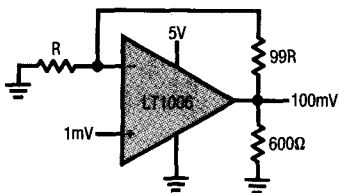


LM324, LM358, OP-20, OP-21
EXHIBIT OUTPUT PHASE
REVERSAL

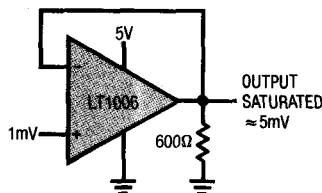


LT1006
NO PHASE REVERSAL

Gain 100 Amplifier



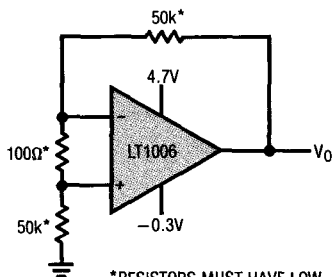
Voltage Follower



APPLICATIONS INFORMATION

In automated production testing the output is forced to 1.4V by the test loop; offset voltage is measured with a common-mode voltage of zero and the negative supply at zero (Pin 4). Without the test loop, these exact conditions cannot be achieved. The test circuit shown ensures that the output will never saturate even with worst-case offset voltages ($-250\mu\text{V}$ over the -55°C to 125°C range). The effective common-mode input is 0.3V with respect to the negative supply. As indicated by the common-mode rejection specifications the difference is only a few microvolts between the two methods of offset voltage measurement.

Test Circuit for Offset Voltage and Offset Drift with Temperature



*RESISTORS MUST HAVE LOW THERMOELECTRIC POTENTIAL.

**THIS CIRCUIT IS ALSO USED AS THE BURN-IN CONFIGURATION, WITH SUPPLY VOLTAGES INCREASED TO $\pm 20\text{V}$.

$V_O = 1000V_{OS}$

Low Supply Operation

The minimum guaranteed supply voltage for proper operation of the LT1006 is 2.7V. Typical supply current at this voltage is $320\mu\text{A}$, therefore power dissipation is only $860\mu\text{W}$.

Noise Testing

For application information on noise testing and calculations, please see the LT1007 or LT1028 data sheet.

Supply Current Programming

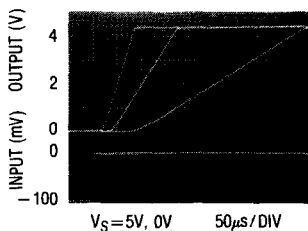
Connecting an optional external resistor to Pin 8 changes the biasing of the LT1006 in order to increase its speed or to decrease its power consumption. If higher slew rate is required, connect the external resistor from Pin 8 to Pin 4 [see performance curves for Increasing Slew Rate (R_{SET} to V^-)]. For lower power consumption, inject a current into Pin 8 (which is approximately 60mV above V^-) as shown on the Reducing Power Dissipation plot. This can be accomplished by connecting R_{SET} to the positive supply, or to save additional power, by obtaining the injected current from a low voltage battery.

2

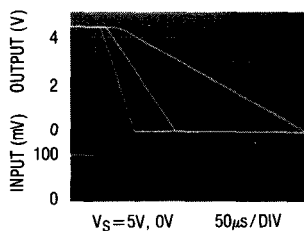
Comparator Applications

The single supply operation of the LT1006 and its ability to swing close to ground while sinking current lends itself to use as a precision comparator with TTL compatible output.

Comparator Rise Response Time to 10mV, 5mV, 2mV Overdrives

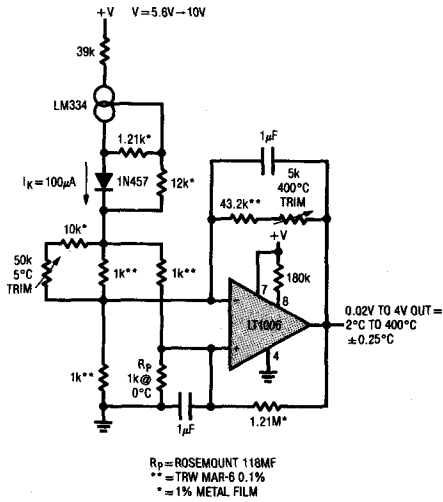


Comparator Fall Response Time to 10mV, 5mV, 2mV Overdrives

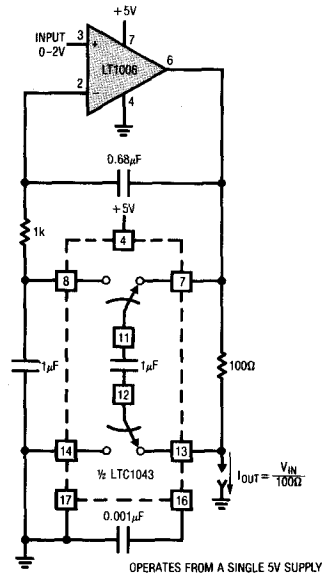


TYPICAL APPLICATIONS

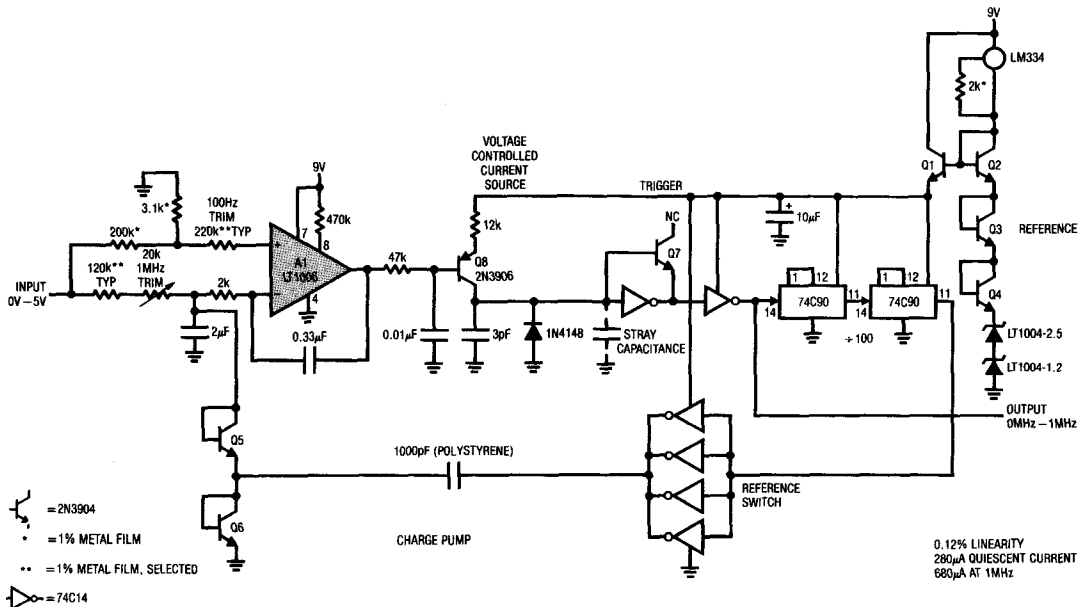
Platinum RTD Signal Conditioner with Curvature Correction



Voltage Controlled Current Source with Ground Referred Input and Output

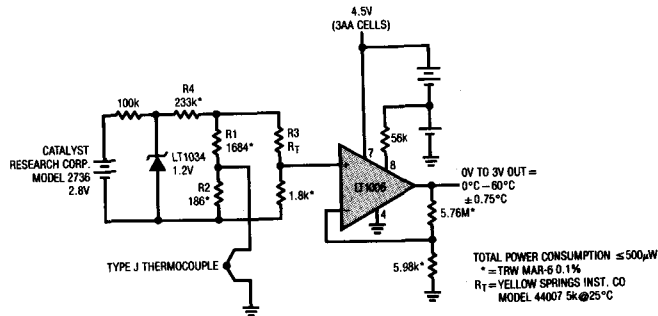


Micropower 1MHz V-F Converter

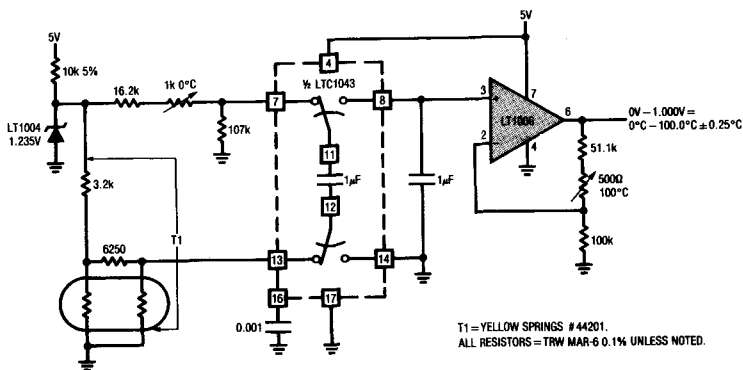


TYPICAL APPLICATIONS

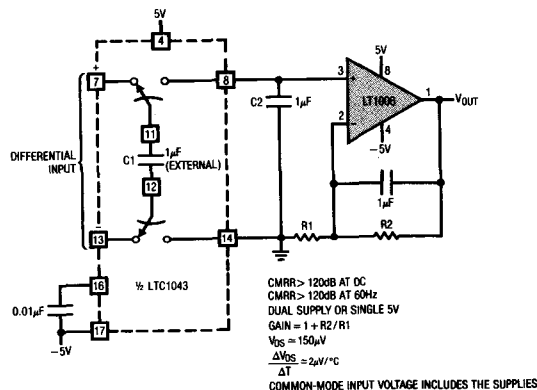
Micropower Thermocouple Signal Conditioner with Cold Junction Compensation



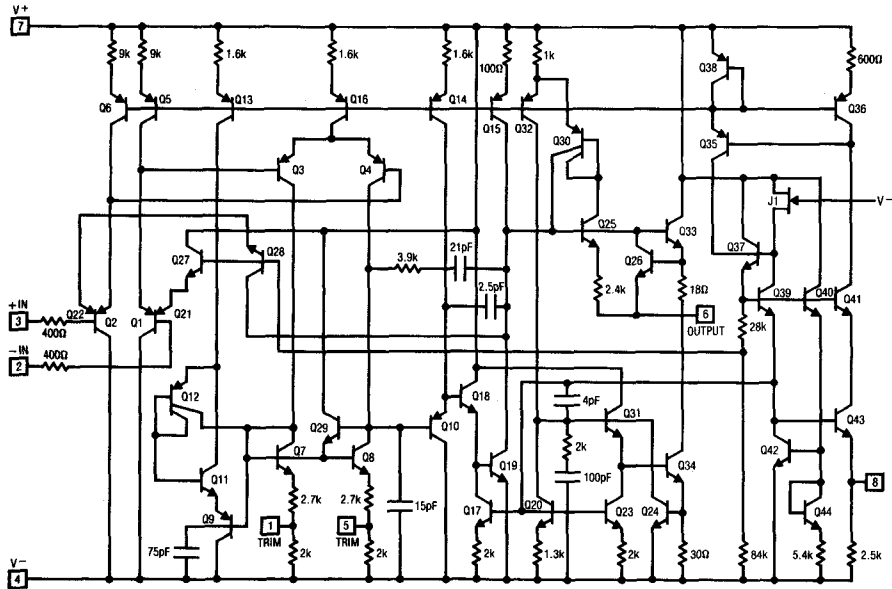
Linear Thermometer



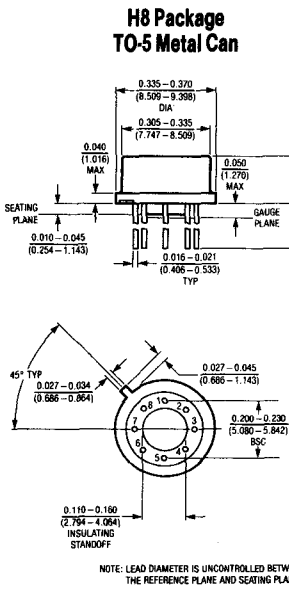
± 5V Precision Instrumentation Amplifier



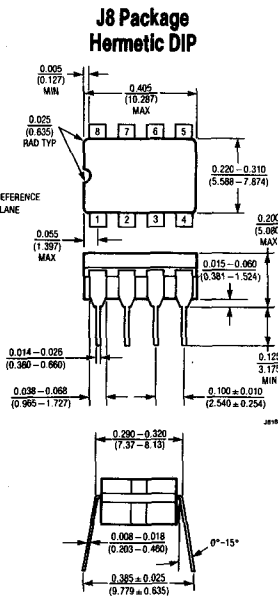
LT1006 SCHEMATIC DIAGRAM



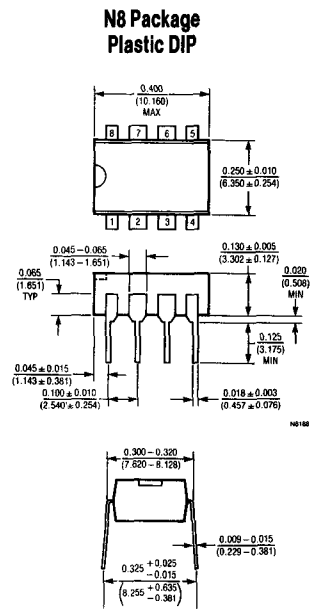
PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.



T_{max}	Θ_{JA}	Θ_{JC}
150°C	150°C/W	45°C/W



T_{max}	Θ_{JA}
150°C	100°C/W



T_{max}	Θ_{JA}
100°C	100°C/W

FEATURES

- Single Supply Operation
 Input Voltage Range Extends to Ground
 Output Swings to Ground while Sinking Current
- *Guaranteed* Offset Voltage 400 μ V Max.
- *Guaranteed* Low Drift 3.5 μ V/ $^{\circ}$ C Max.
- *Guaranteed* Offset Current 0.9nA Max.
- *Guaranteed* High Gain
- 5mA Load Current 1.2 Million Min.
- 17mA Load Current 0.5 Million Min.
- *Guaranteed* Low Supply Current 570 μ A Max.
- Supply Current can be Reduced by a Factor of 4
- Low Voltage Noise, 0.1Hz to 10Hz 0.55 μ Vp-p
- Low Current Noise—
 Better than OP-07 0.08pA/ $\sqrt{\text{Hz}}$ at 10Hz
- High Input Impedance 100M Ω Min.
- *Guaranteed* Minimum Supply Voltage 2.7V Min.

DESCRIPTION

The LT1006S8 is the first precision single supply operational amplifier. Its design has been optimized for single supply operation with a full set of specifications at 5V. Specifications at ± 15 V are also provided.

The LT1006S8 has low offset voltage of 80 μ V, drift of 0.7 μ V/ $^{\circ}$ C, offset current of 150pA, gain of 2 million, common-mode rejection of 112dB, and power supply rejection of 126dB.

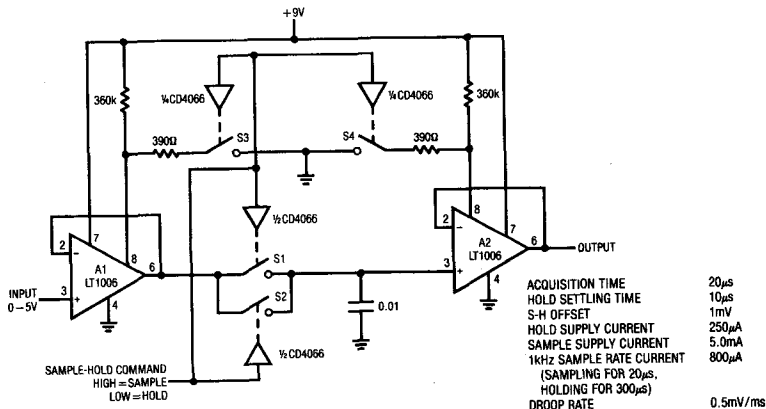
Although supply current is only 350 μ A, a novel output stage can source or sink in excess of 20mA while retaining high voltage gain. Common-mode input range includes ground to accommodate low ground-referenced inputs from strain gauges or thermocouples, and output can swing to within a few millivolts of ground. If higher slew rate (in excess of 1V/ μ s) or micropower operation (supply current down to 90 μ A) is required, the operating currents can be modified by connecting an external optional resistor to Pin 8.

For a similar single supply precision dual op amp in the SO package, please see the LT1013DS8 data sheet.

APPLICATIONS

- Low Power Sample and Hold Circuits
- Battery Powered Precision Instrumentation
 Strain Gauge Signal Conditioners
 Thermocouple Amplifiers
- 4mA–20mA Current Loop Transmitters
- Active Filters

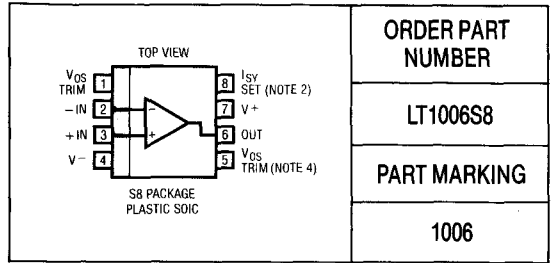
LT1006 Single Supply, Micropower Sample and Hold



ABSOLUTE MAXIMUM RATINGS

Supply Voltage $\pm 22V$
 Input Voltage Equal to Positive Supply Voltage
 5V Below Negative Supply Voltage
 Differential Input Voltage 30V
 Output Short Circuit Duration Indefinite
 Operating Temperature Range $0^{\circ}C$ to $70^{\circ}C$
 Storage Temperature Range $-65^{\circ}C$ to $150^{\circ}C$
 Lead Temperature (Soldering, 10 sec) $300^{\circ}C$

PACKAGE/ORDER INFORMATION



ELECTRICAL CHARACTERISTICS

$V_S = 5V, 0V, V_{CM} = 0V, V_{OUT} = 1.4V, T_A = 25^{\circ}C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1006S8			UNITS
			MIN	TYP	MAX	
V_{OS}	Input Offset Voltage			80	400	μV
$\frac{\Delta V_{OS}}{\Delta Time}$	Long Term Input Offset Voltage Stability			0.7		$\mu V/Mo$
I_{OS}	Input Offset Current			0.15	0.9	nA
I_B	Input Bias Current			10	25	nA
e_n	Input Noise Voltage	0.1Hz to 10Hz		0.55		$\mu Vp-p$
	Input Noise Voltage Density	$f_o = 10Hz$ (Note 3) $f_o = 1000Hz$ (Note 3)		23 22	32 25	nV/\sqrt{Hz} nV/\sqrt{Hz}
i_n	Input Noise Current Density	$f_o = 10Hz$		0.08		pA/\sqrt{Hz}
	Input Resistance	(Note 1)		100	300	M Ω
	Differential Mode				4	G Ω
	Common-Mode					
	Input Voltage Range		3.5 0	3.8 -0.3		V V
CMRR	Common-Mode Rejection Ratio	$V_{CM} = 0V$ to 3.5V	97	112		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 2V$ to $\pm 18V, V_O = 0V$	103	124		dB
A_{VOL}	Large Signal Voltage Gain	$V_O = 0.03V$ to 4V, $R_L = 10k$ $V_O = 0.03V$ to 3.5V, $R_L = 2k$	0.7 0.3	2.0 1.8		$V/\mu V$ $V/\mu V$
V_{OUT}	Maximum Output Voltage Swing	Output Low, No Load Output Low, 600 Ω to GND Output Low, $I_{SINK} = 1mA$ Output High, No Load Output High, 600 Ω to GND		15 5 220 4.0 3.4	25 10 350	mV mV mV V V
SR	Slew Rate		0.25	0.4		$V/\mu s$
I_S	Supply Current	$R_{SET} = \infty$ $R_{SET} = 180k$ Pin 8 to Pin 7 (Note 2)		350 90	570	μA μA
	Minimum Supply Voltage		2.7			V

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V, T_A = 25^\circ C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1006S8			UNITS
			MIN	TYP	MAX	
V_{OS}	Input Offset Voltage			100	525	μV
I_{OS}	Input Offset Current			0.15	0.9	nA
I_B	Input Bias Current			8.0	20.0	nA
	Input Voltage Range		13.5 -15.0	13.8 -15.3		V V
CMRR	Common-Mode Rejection Ratio	$V_{CM} = +13.5V, -15V$	97	116		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 2V$ to $\pm 18V, V_O = 0V$	103	124		dB
A_{VOL}	Large Signal Voltage Gain	$V_O = \pm 10V, R_L = 2k$ $V_O = \pm 10V, R_L = 600\Omega$	1.2 0.5	4.0 1.0		$V/\mu V$ $V/\mu V$
V_{OUT}	Maximum Output Voltage Swing	$R_L = 2k$	± 12.5	± 14		V
SR	Slew Rate	$R_{SET} = \infty$ $R_{SET} = 390\Omega$ Pin 8 to Pin 4	0.25 1.0	0.4 1.2		$V/\mu s$ $V/\mu s$
I_S	Supply Current			360	600	μA

2

ELECTRICAL CHARACTERISTICS
 $V_S = 5V, 0V, V_{CM} = 0V, V_{OUT} = 1.4V, 0^\circ C \leq T_A \leq 70^\circ C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1006S8			UNITS
			MIN	TYP	MAX	
V_{OS}	Input Offset Voltage		●	110	560	μV
ΔV_{OS}	Input Offset Voltage Drift		●	0.7	3.5	$\mu V/^\circ C$
$\Delta Temp$						
I_{OS}	Input Offset Current		●	0.3	2.5	nA
I_B	Input Bias Current		●	12	30	nA
A_{VOL}	Large Signal Voltage Gain	$V_O = 0.04V$ to $3.5V, R_L = 2k$	●	0.25	1.2	$V/\mu V$
CMRR	Common-Mode Rejection Ratio	$V_{CM} = 0V$ to $3.4V$	●	92	108	dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 2V$ to $\pm 18V, V_O = 0V$	●	97	118	dB
V_{OUT}	Maximum Output Voltage Swing	Output Low, 600Ω to GND Output High, 600Ω to GND	● ●	6 3.2	13 3.9	mV V
I_S	Supply Current		●	360	620	μA

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V, 0^\circ C \leq T_A \leq 70^\circ C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1006S8			UNITS
			MIN	TYP	MAX	
V_{OS}	Input Offset Voltage			150	730	μV
$\frac{\Delta V_{OS}}{\Delta Temp}$	Input Offset Voltage Drift			1.0	4.5	$\mu V/^\circ C$
I_{OS}	Input Offset Current			0.25	2.0	nA
I_B	Input Bias Current			10	23	nA
A_{VOL}	Large Signal Voltage Gain	$V_O = \pm 10V, R_L = 2k$		0.7	2.5	$V/\mu V$
CMRR	Common-Mode Rejection Ratio	$V_{CM} = 13V, -15V$		94	114	dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 2V$ to $\pm 18V, V_O = 0V$		97	118	dB
V_{OUT}	Maximum Output Voltage Swing	$R_L = 2k$		± 11.5	± 13.8	V
I_S	Supply Current			380	660	μA

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: This parameter is guaranteed by design and is not tested.

Note 2: Regular operation does not require an external resistor. In order to program the supply current for low power or high speed operation, connect an external resistor from Pin 8 to Pin 7 or from Pin 8 to Pin 4, respectively. Supply current specifications (for $R_{SET} = 180k$) do not include current in R_{SET} .

Note 3: This parameter is tested on a sample basis only. All noise parameters are tested with $V_S = \pm 2.5V, V_O = 0V$.

Note 4: Optional offset nulling is accomplished with a potentiometer connected between the trim terminals and the wiper to V^- . A 10k pot (providing a null range of $\pm 6mV$) is recommended for minimum drift of nulled offset voltage with temperature. For increased trim resolution and accuracy, two fixed resistors can be used in conjunction with a smaller potentiometer. For example: two 4.7k resistors tied to pins 1 and 5, with a 500 Ω pot in the middle, will have a null range of $\pm 150\mu V$.

FEATURES

- *Guaranteed* 4.5 nV/√Hz 10 Hz noise
- *Guaranteed* 3.8 nV/√Hz 1kHz noise
- 0.1 Hz to 10 Hz noise, 60 nV p-p, typical
- *Guaranteed* 7 million min. voltage gain,
 $R_L = 2k\Omega$
- *Guaranteed* 3 million min. voltage gain,
 $R_L = 600\Omega$
- *Guaranteed* 25μV max. offset voltage
- *Guaranteed* 0.6μV/°C max. drift with temperature
- *Guaranteed* 11V/μsec min. slew rate (LT1037)
- *Guaranteed* 117 dB min. CMRR

APPLICATIONS

- Low Noise Signal Processing
- Microvolt Accuracy Threshold Detection
- Strain Gauge Amplifiers
- Direct Coupled Audio Gain Stages
- Sine Wave Generators
- Tape Head Pre-amplifiers
- Microphone Pre-amplifiers

DESCRIPTION

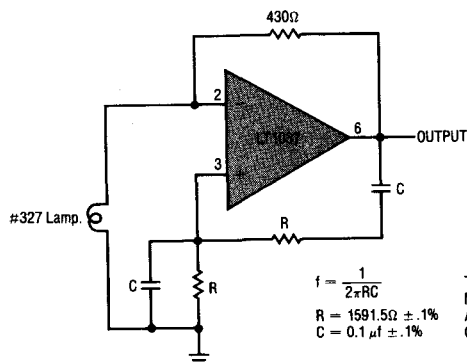
The LT1007/LT1037 series features the lowest noise performance available to date for monolithic operational amplifiers: 2.5nV/√Hz wideband noise (less than the noise of a 400Ω resistor), 1/f corner frequency of 2Hz and 60nV peak to peak 0.1Hz to 10Hz noise. Low noise is combined with outstanding precision and speed specifications: 10μV offset voltage, 0.2μV/°C drift, 130 dB common-mode and power supply rejection, and 60MHz gain-bandwidth-product on the de-compensated LT1037, which is stable for closed loop gains of 5 or greater.

The voltage gain of the LT1007/1037 is an extremely high 20 million driving a 2kΩ load and 12 million driving a 600Ω load to ± 10V.

In the design, processing, and testing of the device, particular attention has been paid to the optimization of the entire distribution of several key parameters. Consequently, the specifications of even the lowest cost grades (the LT1007C and the LT1037C) have been spectacularly improved compared to equivalent grades of competing amplifiers.

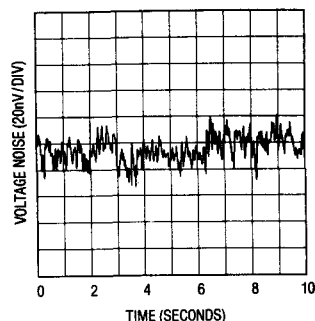
The sine wave generator application shown below utilizes the low noise and low distortion characteristics of the LT1037.

Ultra-Pure 1kHz Sine Wave Generator



Total Harmonic Distortion = < .0025%
 Noise = < .0001%
 Amplitude = ± 8 volts
 Output Frequency = 1.000kHz for values
 given ± .4%

0.1Hz to 10Hz Noise



ABSOLUTE MAXIMUM RATINGS

Supply Voltage..... ±22V
 Input Voltage..... Equal to Supply Voltage
 Output Short Circuit Duration..... Indefinite
 Differential Input Current (Note 8)..... ±25mA
 Lead Temperature (Soldering, 10 sec.)..... 300°C
 Operating Temperature Range
 LT1007/1037AM, M..... -55°C to 125°C
 LT1007/1037AC, C..... 0°C to 70°C
 Storage Temperature Range
 All Devices..... -65°C to 150°C

PACKAGE/ORDER INFORMATION

TOP VIEW		ORDER PART NUMBER	
<p>METAL CAN H PACKAGE</p>		LT1007AMH	LT1037AMH
		LT1007MH	LT1037MH
		LT1007ACH	LT1037ACH
		LT1007CH	LT1037CH
TOP VIEW		ORDER PART NUMBER	
<p>HERMETIC DIP J8 PACKAGE PLASTIC DIP N8 PACKAGE</p>		LT1007AMJ8	LT1037AMJ8
		LT1007MJ8	LT1037MJ8
		LT1007ACJ8	LT1037ACJ8
		LT1007CJ8	LT1037CJ8
		LT1007ACN8	LT1037ACN8
		LT1007CN8	LT1037CN8

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V, T_A = 25^\circ C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1007AM/AC LT1037AM/AC			LT1007M/C LT1037M/C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	(Note 1)		10	25		20	60	μV
$\frac{\Delta V_{OS}}{\Delta Time}$	Long Term Input Offset Voltage Stability	(Notes 2 and 3)		0.2	1.0		0.2	1.0	$\mu V/Mo$
I_{OS}	Input Offset Current			7	30		12	50	nA
I_B	Input Bias Current			±10	±35		±15	±55	nA
e_n	Input Noise Voltage	0.1Hz to 10Hz (Notes 3 and 5)		0.06	0.13		0.06	0.13	$\mu Vp-p$
i_n	Input Noise Voltage Density	$f_o = 10Hz$ (Notes 3 and 4)		2.8	4.5		2.8	4.5	nV/\sqrt{Hz}
		$f_o = 1000Hz$ (Note 3)		2.5	3.8		2.5	3.8	nV/\sqrt{Hz}
i_n	Input Noise Current Density	$f_o = 10Hz$ (Notes 3 and 6)		1.5	4.0		1.5	4.0	pA/\sqrt{Hz}
		$f_o = 1000Hz$ (Notes 3 and 6)		0.4	0.6		0.4	0.6	pA/\sqrt{Hz}
	Input Resistance — Common Mode			7			5		$G\Omega$
	Input Voltage Range			±11.0	±12.5		±11.0	±12.5	V
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 11V$		117	130		110	126	dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 4V$ to $\pm 18V$		110	130		106	126	dB
A_{VOL}	Large Signal Voltage Gain	$R_L \geq 2k\Omega, V_O = \pm 12V$		7.0	20.0		5.0	20.0	$V/\mu V$
		$R_L \geq 1k\Omega, V_O = \pm 10V$		5.0	16.0		3.5	16.0	$V/\mu V$
		$R_L \geq 600\Omega, V_O = \pm 10V$		3.0	12.0		2.0	12.0	$V/\mu V$
V_{OUT}	Maximum Output Voltage Swing	$R_L \geq 2k\Omega$		±13.0	±13.8		±12.5	±13.5	V
		$R_L \geq 600\Omega$		±11.0	±12.5		±10.5	±12.5	V
SR	Slew Rate	LT1007		1.7	2.5		1.7	2.5	$V/\mu S$
		LT1037		11	15		11	15	$V/\mu S$
GBW	Gain-Bandwidth Product:	LT1007		5.0	8.0		5.0	8.0	MHz
		LT1037		45	60		45	60	MHz
Z_o	Open Loop Output Resistance	$V_O = 0, I_O = 0$		70		70		Ω	
P_d	Power Dissipation	LT1007		80	120		80	140	mW
		LT1037		80	130		85	140	mW

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V, -55^\circ C \leq T_A \leq 125^\circ C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1007AM/LT1037AM			LT1007M/LT1037M			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	(Note 1)	●	25	60	50	160	μV	
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Input Offset Drift	(Note 9)	●	0.2	0.6	0.3	1.0	$\mu V/^\circ C$	
I_{OS}	Input Offset Current		●	15	50	20	85	nA	
I_B	Input Bias Current		●	± 20	± 60	± 35	± 95	nA	
	Input Voltage Range		●	± 10.3	± 11.5	± 10.3	± 11.5	V	
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 10.3V$	●	112	126	104	120	dB	
PSRR	Power Supply Rejection Ratio	$V_S = \pm 4.5V$ to $\pm 18V$	●	104	126	100	120	dB	
A_{VOL}	Large Signal Voltage Gain	$R_L \geq 2k\Omega, V_o = \pm 10V$ $R_L \geq 1k\Omega, V_o = \pm 10V$	●	3.0	14.0	2.0	14.0	$V/\mu V$ $V/\mu V$	
V_{OUT}	Maximum Output Voltage Swing	$R_L \geq 2k\Omega$	●	± 12.5	± 13.5	± 12.0	± 13.5	V	
P_d	Power Dissipation		●	100	150	100	170	mW	

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V, 0^\circ C \leq T_A \leq 70^\circ C$, unless otherwise noted.

2

SYMBOL	PARAMETER	CONDITIONS	LT1007AC/LT1037AC			LT1007C/LT1037C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	(Note 1)	●	20	50	35	110	μV	
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Input Offset Drift	(Note 9)	●	0.2	0.6	0.3	1.0	$\mu V/^\circ C$	
I_{OS}	Input Offset Current		●	10	40	15	70	nA	
I_B	Input Bias Current		●	± 14	± 45	± 20	± 75	nA	
	Input Voltage Range		●	± 10.5	± 11.8	± 10.5	± 11.8	V	
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 10.5V$	●	114	126	106	120	dB	
PSRR	Power Supply Rejection Ratio	$V_S = \pm 4.5V$ to $\pm 18V$	●	106	126	102	120	dB	
A_{VOL}	Large Signal Voltage Gain	$R_L \geq 2k\Omega, V_o = \pm 10V$ $R_L \geq 1k\Omega, V_o = \pm 10V$	●	4.0	18.0	2.5	18.0	$V/\mu V$ $V/\mu V$	
V_{OUT}	Maximum Output Voltage Swing	$R_L \geq 2k\Omega$	●	± 12.5	± 13.6	± 12.0	± 13.6	V	
P_d	Power Dissipation		●	90	144	90	160	mW	

NOTES:

The ● denotes the specifications which apply over full operating temperature range.

For MIL-STD components, please refer to LTC 883C data sheet for test listing and parameters.

Note 1: Input Offset Voltage measurements are performed by automatic test equipment approximately 0.5 seconds after application of power. AM and AC grades are guaranteed fully warmed up.

Note 2: Long Term Input Offset Voltage Stability refers to the average trend line of Offset Voltage vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 days are typically $2.5\mu V$ — refer to typical performance curve.

Note 3: This parameter is tested on a sample basis only.

Note 4: 10Hz noise voltage density is sample tested on every lot. Devices 100% tested at 10Hz are available on request.

Note 5: See the test circuit and frequency response curve for 0.1Hz to 10Hz tester in the Applications Information section.

Note 6: See the test circuit for current noise measurement in the Applications Information section.

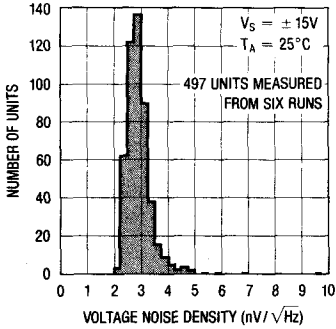
Note 7: This parameter is guaranteed by design and is not tested.

Note 8: The inputs are protected by back-to-back diodes. Current limiting resistors are not used in order to achieve low noise. If differential input voltage exceeds $\pm 0.7V$, the input current should be limited to 25mA.

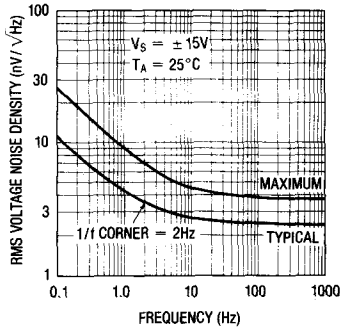
Note 9: The Average Input Offset Drift performance is within the specifications unnullled or when nullled with a pot having a range of $8k\Omega$ to $20k\Omega$.

TYPICAL PERFORMANCE CHARACTERISTICS

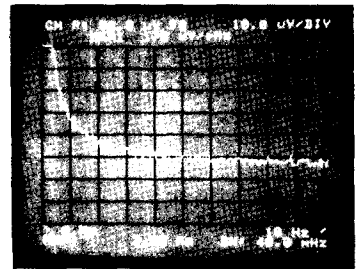
10Hz Voltage Noise Distribution



Voltage Noise vs Frequency

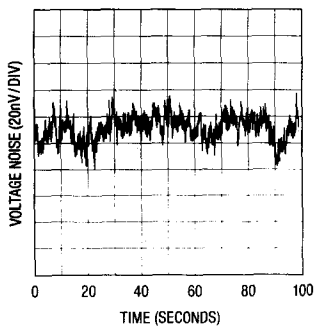


0.02 to 10Hz RMS Noise. Gain = 50,000 (Measured on HP3582 Spectrum Analyzer)

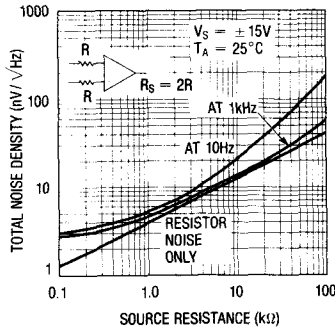


Marker at 2Hz (= 1/f corner) =
 $\frac{179 \mu\text{V}/\sqrt{\text{Hz}}}{50,000} = 3.59 \frac{\text{nV}}{\sqrt{\text{Hz}}}$

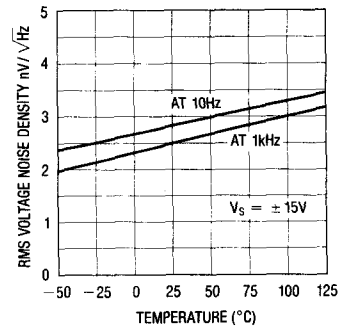
0.01 to 1Hz Peak to Peak Noise



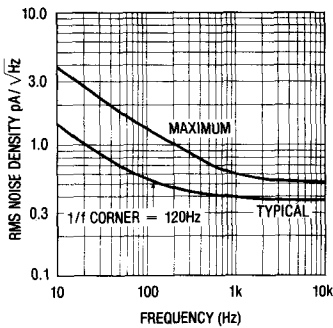
Total Noise vs Source Resistance



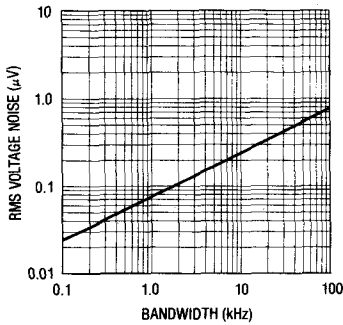
Voltage Noise vs Temperature



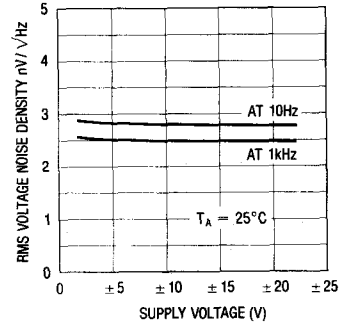
Current Noise vs Frequency



Wideband Voltage Noise (0.1Hz to Frequency Indicated)

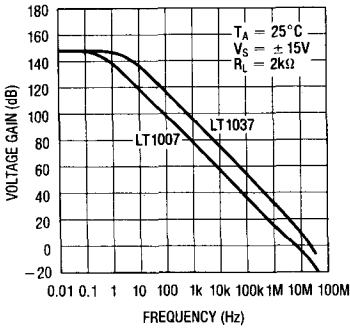


Voltage Noise vs Supply Voltage

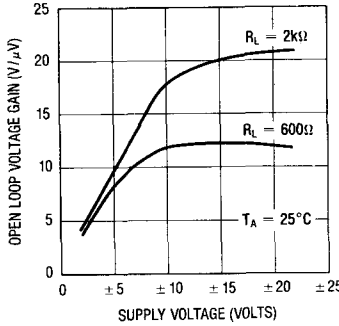


TYPICAL PERFORMANCE CHARACTERISTICS

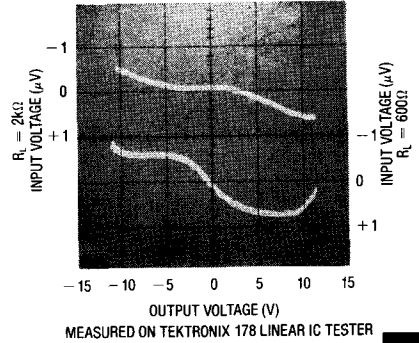
Voltage Gain vs Frequency



Voltage Gain vs Supply Voltage

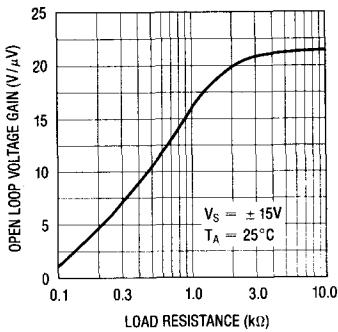


Voltage Gain, $R_L = 2K$ and 600Ω

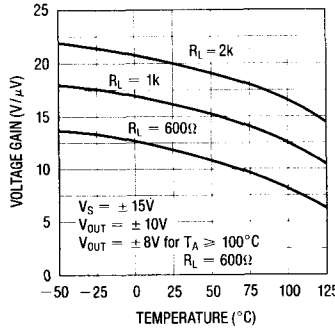


2

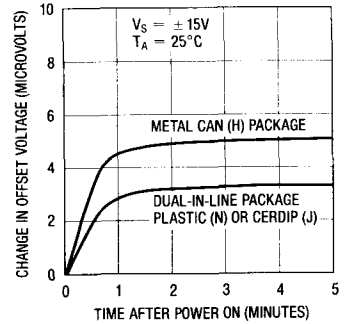
Voltage Gain vs Load Resistance



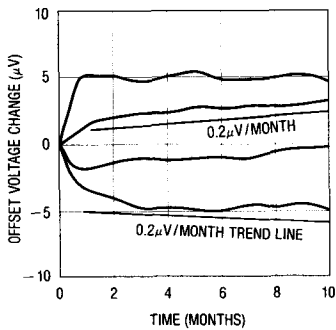
Voltage Gain vs Temperature



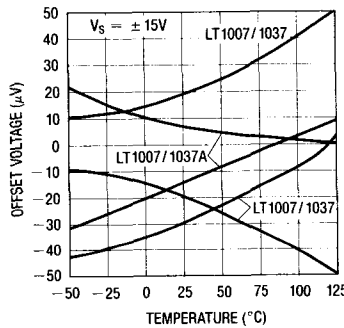
Warm-Up Drift



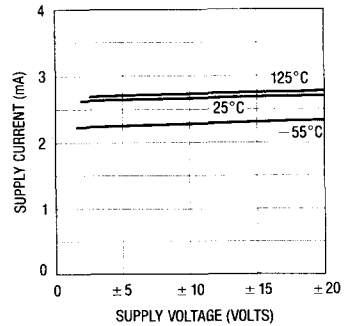
Long Term Stability of Four Representative Units



Offset Voltage Drift with Temperature of Representative Units

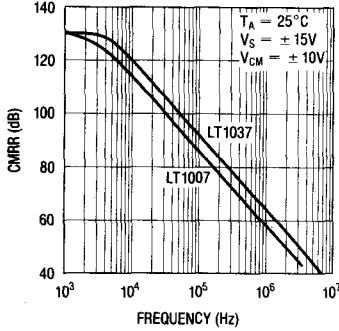


Supply Current vs Supply Voltage

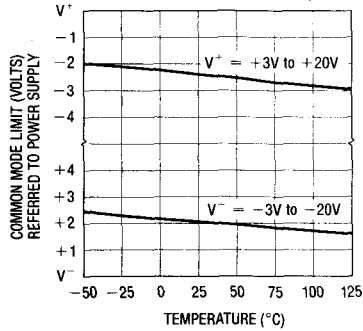


TYPICAL PERFORMANCE CHARACTERISTICS

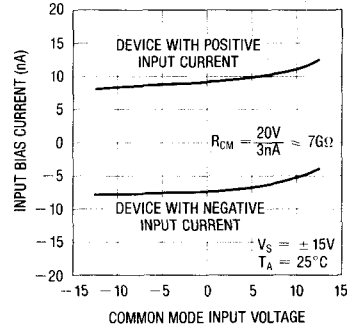
Common Mode Rejection vs Frequency



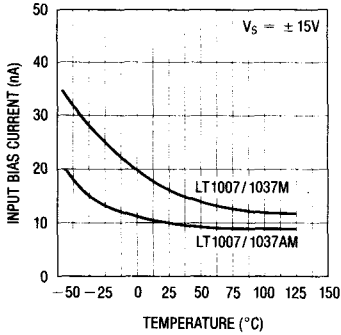
Common Mode Limit vs Temperature



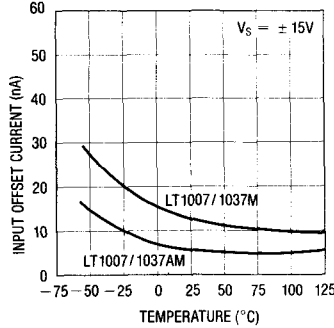
Input Bias Current Over the Common Mode Range



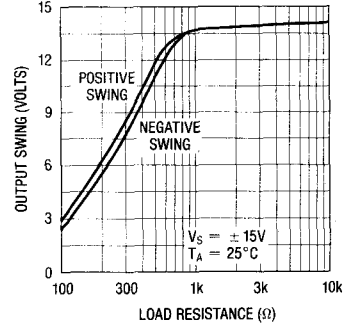
Input Bias Current vs Temperature



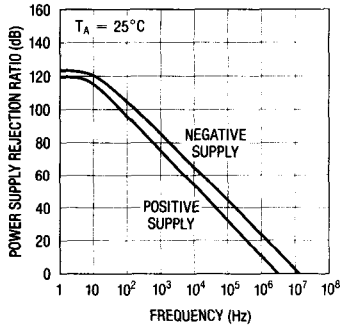
Input Offset Current vs Temperature



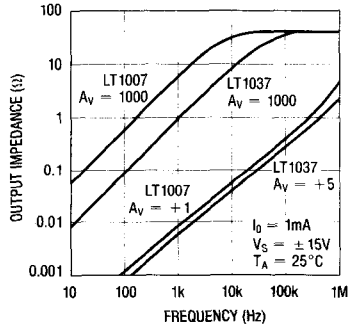
Output Swing vs Load Resistance



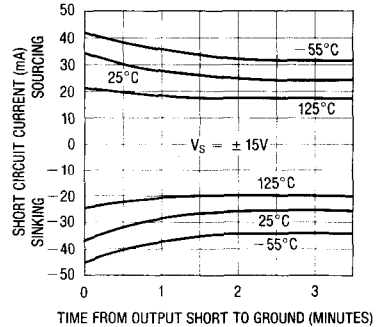
PSRR vs Frequency



Closed Loop Output Impedance

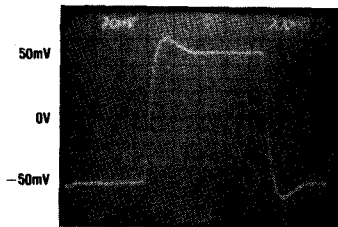


Output Short Circuit Current vs Time



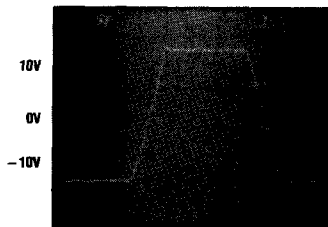
TYPICAL PERFORMANCE CHARACTERISTICS

LT1037 Small Signal Transient Response



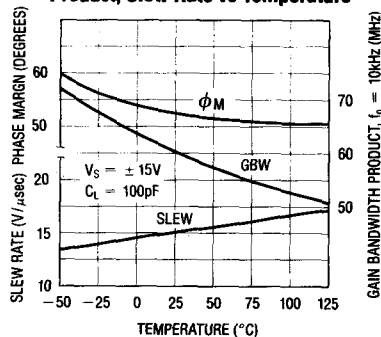
$A_{VCL} = +5$, $V_S = \pm 15V$
 $C_L = 15pF$

LT1037 Large Signal Response

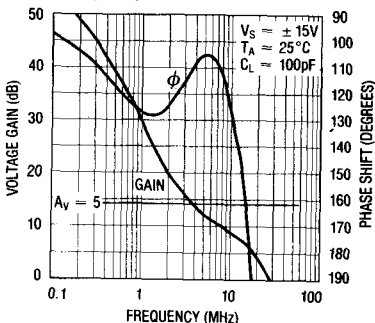


$A_{VCL} = +5$, $V_S = \pm 15V$

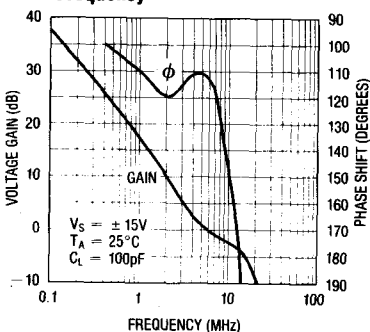
LT1037 Phase Margin, Gain Bandwidth Product, Slew Rate vs Temperature



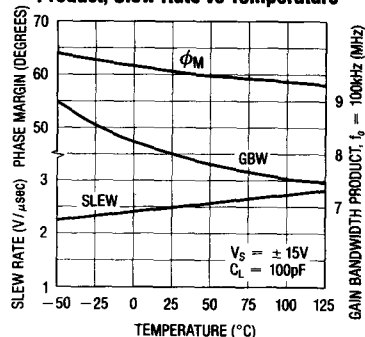
LT1037 Gain, Phase Shift vs Frequency



LT1007 Gain, Phase Shift vs Frequency

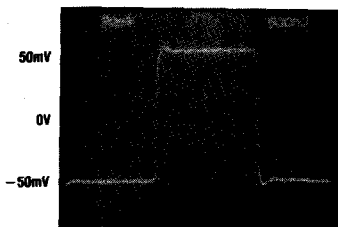


LT1007 Phase Margin, Gain-Bandwidth Product, Slew Rate vs Temperature



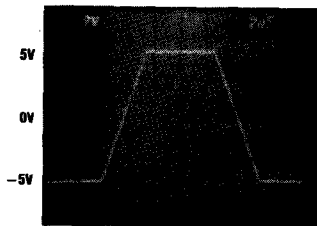
2

LT1007 Small Signal Transient Response



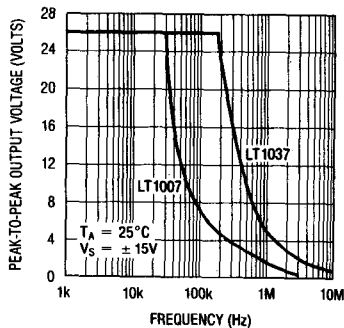
$A_{VCL} = +1$, $V_S = \pm 15V$
 $C_L = 15pF$

LT1007 Large Signal Response



$A_{VCL} = -1$, $V_S = \pm 15V$

Maximum Undistorted Output vs Frequency



APPLICATIONS INFORMATION

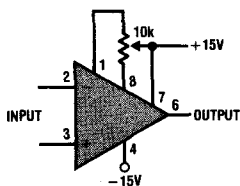
General

The LT1007/1037 series devices may be inserted directly into OP-07, OP-27, OP-37, and 5534 sockets with or without removal of external compensation or nulling components. In addition, the LT1007/1037 may be fitted to 741 sockets with the removal or modification of external nulling components.

Offset Voltage Adjustment

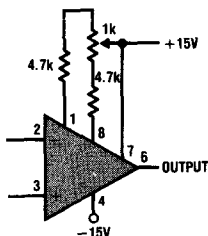
The input offset voltage of the LT1007/1037 and its drift with temperature, are permanently trimmed at wafer testing to a low level. However, if further adjustment of V_{OS} is necessary, the use of a 10k nulling potentiometer will not degrade drift with temperature. Trimming to a value other than zero creates a drift of $(V_{OS}/300) \mu V/^\circ C$, e.g., if V_{OS} is adjusted to $300 \mu V$, the change in drift will be $1 \mu V/^\circ C$.

Standard Adjustment



The adjustment range with a 10k pot is approximately $\pm 2.5mV$. If less adjustment range is needed, the sensitivity and resolution of the nulling can be improved by using a smaller pot in conjunction with fixed resistors. The example has an approximate null range of $\pm 200 \mu V$.

Improved Sensitivity Adjustment

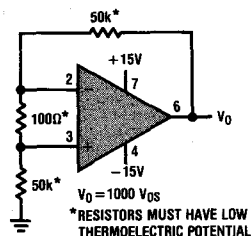


Offset Voltage and Drift

Thermocouple effects, caused by temperature gradients across dissimilar metals at the contacts to the input terminals, can exceed the inherent drift of the

amplifier unless proper care is exercised. Air currents should be minimized, package leads should be short, the two input leads should be close together and maintained at the same temperature.

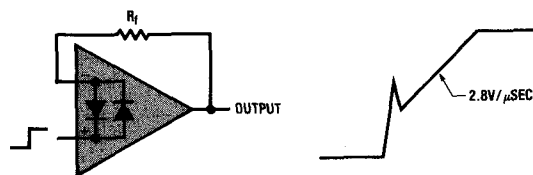
The circuit shown to measure offset voltage is also used as the burn-in configuration for the LT1007/1037, with the supply voltages increased to $\pm 20V$.



Test Circuit for Offset Voltage and Offset Voltage Drift with Temperature

Unity Gain Buffer Applications (LT1007 Only)

When $R_f \leq 100 \Omega$ and the input is driven with a fast, large signal pulse ($> 1V$), the output waveform will look as shown in the pulsed operation diagram.



During the fast feedthrough-like portion of the output, the input protection diodes effectively short the output to the input and a current, limited only by the output short circuit protection, will be drawn by the signal generator. With $R \geq 500 \Omega$, the output is capable of handling the current requirements ($I_L \leq 20mA$ at $10V$) and the amplifier stays in its active mode and a smooth transition will occur.

As with all operational amplifiers when $R_f > 2k \Omega$, a pole will be created with R_f and the amplifier's input capacitance, creating additional phase shift and reducing the phase margin. A small capacitor (20pF to 50pF) in parallel with R_f will eliminate this problem.

APPLICATIONS INFORMATION — NOISE

Noise Testing

The 0.1Hz to 10Hz peak-to-peak noise of the LT1007/1037 is measured in the test circuit shown. The frequency response of this noise tester indicates that the 0.1Hz corner is defined by only one zero. The test time to measure 0.1Hz to 10Hz noise should not exceed 10 seconds, as this time limit acts as an additional zero to eliminate noise contributions from the frequency band below 0.1Hz.

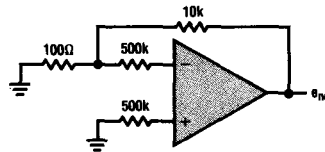
Measuring the typical 60nV peak-to-peak noise performance of the LT1007/1037 requires special test precautions:

- The device should be warmed up for at least five minutes. As the op amp warms up, its offset voltage changes typically $3\mu\text{V}$ due to its chip temperature increasing 10°C to 20°C from the moment the power supplies are turned on. In the 10 second measurement interval these temperature-induced effects can easily exceed tens of nanovolts.
- For similar reasons, the device must be well shielded from air currents to eliminate the possibility of thermoelectric effects in excess of a few nanovolts, which would invalidate the measurements.
- Sudden motion in the vicinity of the device can also "feedthrough" to increase the observed noise.

A noise-voltage density test is recommended when measuring noise on a large number of units. A 10Hz noise-voltage density measurement will correlate well with a 0.1Hz to 10Hz peak-to-peak noise reading since both results are determined by the white noise and the location of the $1/f$ corner frequency.

Current noise is measured in the circuit shown and calculated by the following formula:

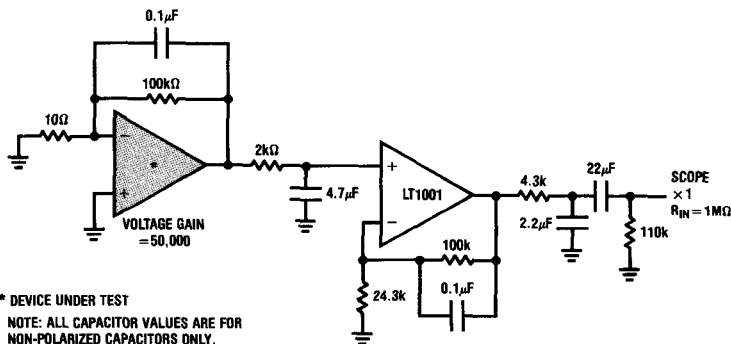
$$i_n = \frac{[e^2_{no} - (130\text{nV})^2]^{1/2}}{1\text{M}\Omega \times 100}$$



The LT1007/1037 achieves its low noise, in part, by operating the input stage at $120\mu\text{A}$ versus the typical $10\mu\text{A}$ of most other op amps. Voltage noise is inversely proportional while current noise is directly proportional to the square root of the stage current. Therefore the LT1007/1037's current noise will be relatively high. At low frequencies, the low $1/f$ current noise corner frequency ($\approx 120\text{Hz}$) minimizes current noise to some extent.

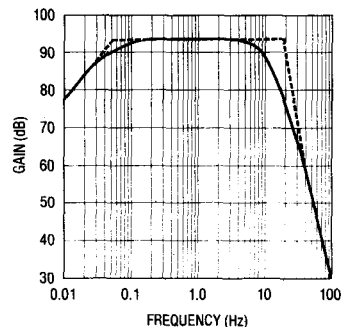
In most practical applications, however, current noise will not limit system performance. This is illustrated in

0.1Hz to 10Hz Noise Test Circuit



* DEVICE UNDER TEST
NOTE: ALL CAPACITOR VALUES ARE FOR NON-POLARIZED CAPACITORS ONLY.

0.1Hz to 10Hz p-p Noise Tester Frequency Response



the total noise versus source resistance plot, where total noise = $[(\text{voltage noise})^2 + (\text{current noise} \times R_s)^2 + (\text{resistor noise})^2]^{1/2}$

Three regions can be identified as a function of source resistance:

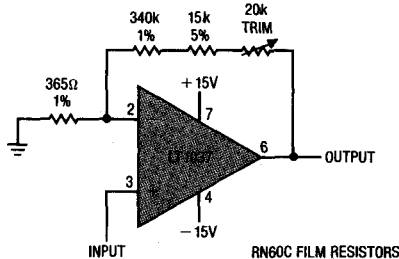
- (i) $R_s \leq 400\Omega$. Voltage noise dominates
- (ii) $400\Omega \leq R_s \leq 50k\Omega$ at 1kHz } Resistor noise dominates
- $400\Omega \leq R_s \leq 8k\Omega$ at 10Hz }

- (iii) $R_s > 50k\Omega$ at 1kHz } Current noise dominates
- $R_s > 8k\Omega$ at 10Hz }

Clearly the LT1007/1037 should not be used in region (iii), where total system noise is at least six times higher than the voltage noise of the op amp, i.e., the low voltage noise specification is completely wasted.

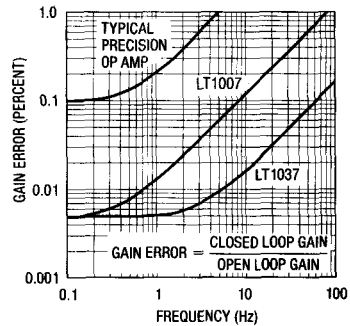
TYPICAL APPLICATIONS

Gain 1000 Amplifier with 0.01% Accuracy, DC to 5Hz

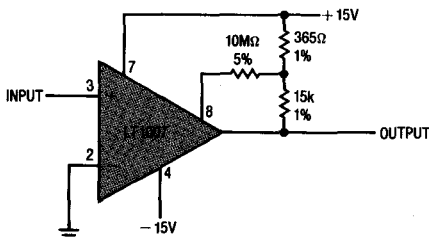


The high gain and wide bandwidth of the LT1037 and (LT1007) is useful in low frequency high closed loop gain amplifier applications. A typical precision Op Amp may have an open loop gain of one million with 500kHz bandwidth. As the gain error plot shows, this device is capable of 0.1% amplifying accuracy up to 0.3Hz only. Even instrumentation range signals can vary at a faster rate. The LT1037's "gain precision — bandwidth product" is 200 times higher, as shown.

Gain Error vs Frequency
Closed Loop Gain = 1000



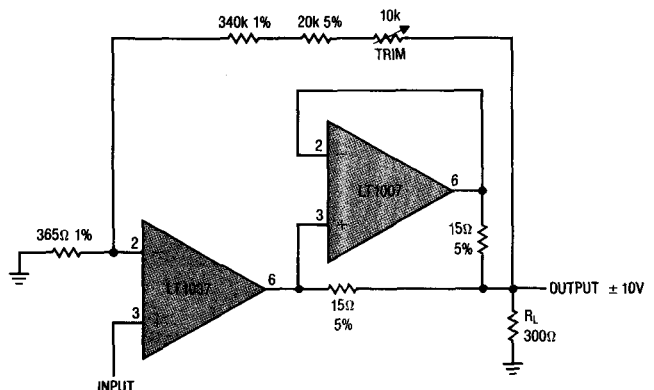
Microvolt Comparator with Hysteresis



Positive feedback to one of the nulling terminals creates approximately 5μV of hysteresis. Output can sink 16mA.

Input offset voltage is typically changed less than 5μV due to the feedback.

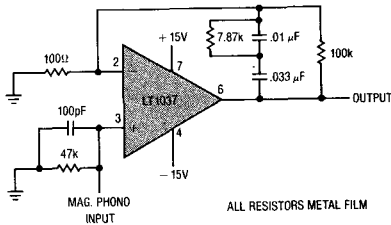
Precision Amplifier Drives 300Ω Load to ±10V



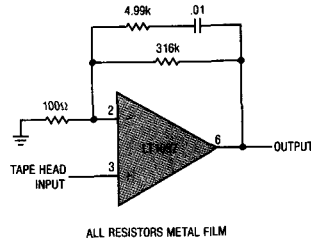
The addition of the LT1007 doubles the amplifier's output drive to ±33mA. Gain accuracy is 0.02%, slightly degraded compared to above because of self heating of the LT1037 under load.

TYPICAL APPLICATIONS

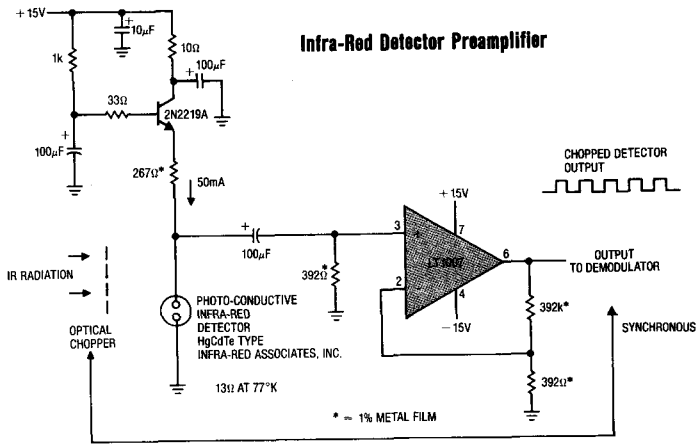
Phono Preamplifier



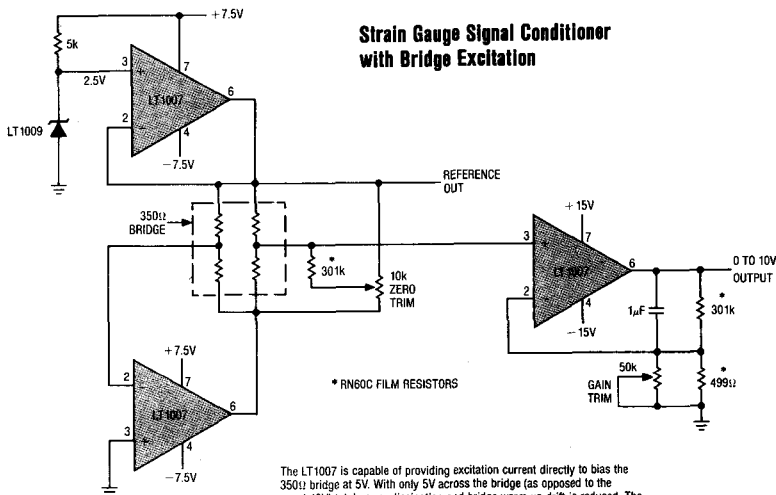
Tape Head Amplifier



Infra-Red Detector Preamplifier

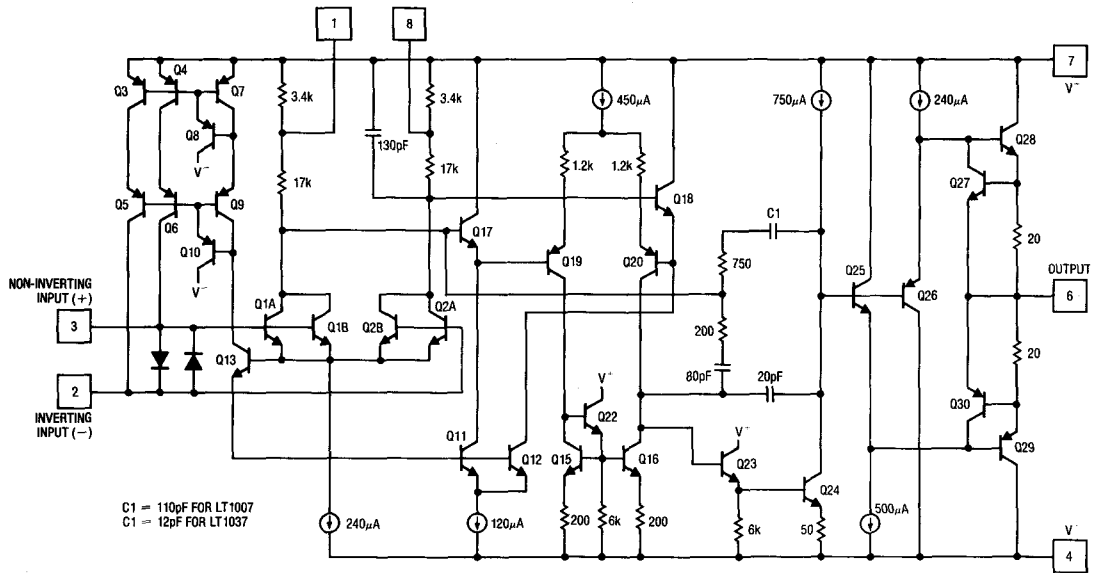


Strain Gauge Signal Conditioner with Bridge Excitation



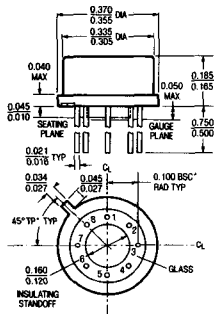
The LT1007 is capable of providing excitation current directly to bias the 350Ω bridge at 5V. With only 5V across the bridge (as opposed to the usual 10V) total power dissipation and bridge warm-up drift is reduced. The bridge output signal is halved, but the LT1007 can amplify the reduced signal accurately.

SCHEMATIC DIAGRAM



PACKAGE DESCRIPTION

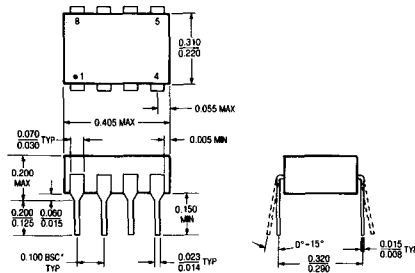
H Package
Metal Can



NOTE: DIMENSIONS IN INCHES

T_j max	θ_{ja}	θ_{jc}
150°C	150°C/W	45°C/W

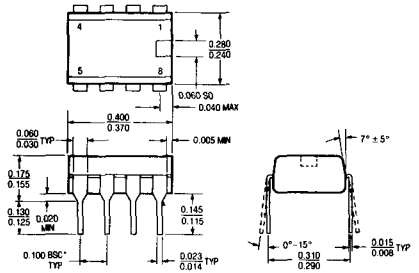
J8 Package
8 Lead Hermetic Dip



NOTE: DIMENSIONS IN INCHES UNLESS OTHERWISE NOTED
*LEADS WITHIN 0.007 OF TRUE POSITION (TP) AT GAUGE PLANE

T_j max	θ_{ja}
150°C	100°C/W

N8 Package
8 Lead Plastic



NOTE: DIMENSIONS IN INCHES UNLESS OTHERWISE NOTED
*LEADS WITHIN 0.007 OF TRUE POSITION (TP) AT GAUGE PLANE.

T_j max	θ_{ja}
100°C	130°C/W

FEATURES

- *Guaranteed* 4.5nV/√Hz 10Hz Noise
- *Guaranteed* 3.8nV/√Hz 1kHz Noise
- 0.1 Hz to 10Hz Noise, 60nVp-p, Typical
- *Guaranteed* 5 Million Min. Voltage Gain, $R_L = 2k\Omega$
- *Guaranteed* 2 Million Min. Voltage Gain, $R_L = 600\Omega$
- *Guaranteed* 60μV Max. Offset Voltage
- *Guaranteed* 1.0μV/°C Max. Drift with Temperature
- *Guaranteed* 11V/μsec Min. Slew Rate (LT1037)
- *Guaranteed* 110dB Min. CMRR

APPLICATIONS

- Low Noise Signal Processing
- Microvolt Accuracy Threshold Detection
- Strain Gauge Amplifiers
- Direct Coupled Audio Gain Stages
- Sine Wave Generators
- Tape Head Preamplifiers
- Microwave Preamplifiers

DESCRIPTION

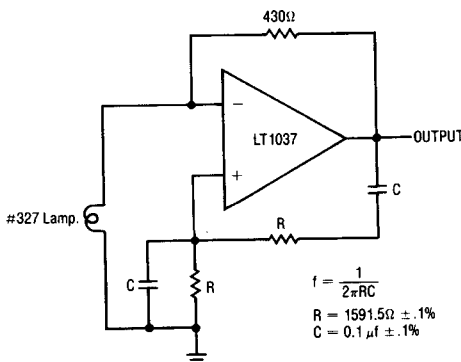
Next to the LT1028, the LT1007/LT1037 series features the lowest noise performance available to date for monolithic operational amplifiers: 2.5nV/√Hz wideband noise (less than the noise of a 400Ω resistor), 1/f corner frequency of 2Hz and 60nV peak to peak 0.1Hz to 10Hz noise. Low noise is combined with outstanding precision and speed specifications: 20μV offset voltage, 0.3μV/°C drift, 126dB common-mode and power supply rejection, and 60MHz gain-bandwidth-product on the decompensated LT1037, which is stable for closed loop gains of 5 or greater.

The voltage gain of the LT1007/LT1037 is an extremely high 20 million driving a 2kΩ load and 12 million driving a 600Ω load to ±10V.

In the design, processing, and testing of the device, particular attention has been paid to the optimization of the entire distribution of several key parameters. Consequently, the specifications have been spectacularly improved compared to competing amplifiers.

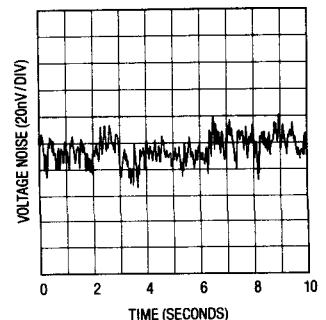
The sine wave generator application shown below utilizes the low noise and low distortion characteristics of the LT1037.

Ultra-Pure 1kHz Sine Wave Generator



Total Harmonic Distortion = < .0025%
 Noise = < .0001%
 Amplitude = ±8 volts
 Output Frequency = 1.000kHz for values
 given ± 4%

0.1Hz to 10Hz Noise

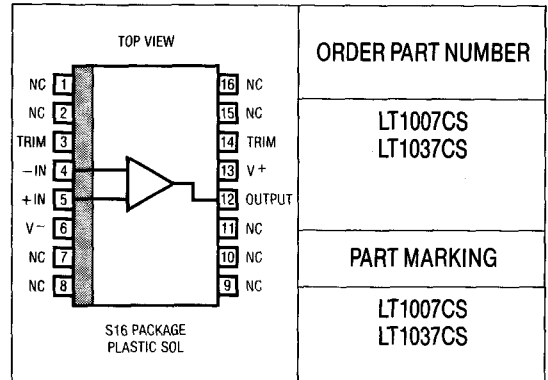


LT1007CS/LT1037CS

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	$\pm 22\text{V}$
Input Voltage	Equal to Supply Voltage
Output Short Circuit Duration	Indefinite
Differential Input Current (Note 5)	$\pm 25\text{mA}$
Lead Temperature (Soldering, 10 sec.)	300°C
Operating Temperature Range	0°C to 70°C
Storage Temperature Range	-65°C to 150°C
All Devices	-65°C to 150°C

PACKAGE/ORDER INFORMATION



ELECTRICAL CHARACTERISTICS $V_S = \pm 15\text{V}$, $T_A = 25^{\circ}\text{C}$, unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS	LT1007C LT1037C			UNITS
			MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	(Note 1)		20	60	μV
$\frac{V_{OS}}{\Delta\text{Time}}$	Long Term Input Offset Voltage Stability	(Notes 2 and 3)		0.2	1.0	$\mu\text{V}/\text{Mo}$
I_{OS}	Input Offset Current			12	50	nA
I_B	Input Bias Current			± 15	± 55	nA
e_n	Input Noise Voltage	0.1Hz to 10Hz (Note 3)		0.06	0.13	$\mu\text{Vp-p}$
	Input Noise Voltage Density	$f_o = 10\text{Hz}$ (Note 3) $f_o = 1000\text{Hz}$ (Note 3)		2.8 2.5	4.5 3.8	$\text{nV}/\sqrt{\text{Hz}}$ $\text{nV}/\sqrt{\text{Hz}}$
i_n	Input Noise Current Density	$f_o = 10\text{Hz}$ (Note 3) $f_o = 1000\text{Hz}$ (Note 3)		1.5 0.4	4.0 0.6	$\text{pA}/\sqrt{\text{Hz}}$ $\text{pA}/\sqrt{\text{Hz}}$
	Input Resistance—Common-Mode			5		G Ω
	Input Voltage Range		± 11.0	± 12.5		V
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm 11\text{V}$	110	126		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 4\text{V}$ to $\pm 18\text{V}$	106	126		dB
A_{VOL}	Large Signal Voltage Gain	$R_L \geq 2\text{k}\Omega$, $V_O = \pm 12\text{V}$ $R_L \geq 1\text{k}\Omega$, $V_O = \pm 10\text{V}$ $R_L \geq 600\Omega$, $V_O = \pm 10\text{V}$	5.0 3.5 2.0	20.0 16.0 12.0		$V/\mu\text{V}$ $V/\mu\text{V}$ $V/\mu\text{V}$
V_{OUT}	Maximum Output Voltage Swing	$R_L \geq 2\text{k}\Omega$ $R_L \geq 600\Omega$	± 12.5 ± 10.5	± 13.5 ± 12.5		V V
SR	Slew Rate	LT1007 $R_L \geq 2\text{k}\Omega$ LT1037 $A_{VOL} \geq 5$	1.7 11	2.5 15		$V/\mu\text{s}$ $V/\mu\text{s}$
GBW	Gain-Bandwidth Product	LT1007 $f_o = 100\text{kHz}$ (Note 4) LT1037 $f_o = 10\text{kHz}$ (Note 4) ($A_{VOL} \geq 5$)	5.0 45	8.0 60		MHz MHz
Z_o	Open Loop Output Resistance	$V_O = 0$, $I_O = 0$		70		Ω
P_d	Power Dissipation	LT1007 LT1037	80 85	140 140		mW mW

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V, 0^\circ C \leq T_A \leq 70^\circ C$, unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS	LT1007C/LT1037C			UNITS
			MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	(Note 1)	●	35	110	μV
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Input Offset Drift	(Note 6)	●	0.3	1.0	$\mu V/^\circ C$
I_{OS}	Input Offset Current		●	15	70	nA
I_B	Input Bias Current		●	± 20	± 75	nA
	Input Voltage Range		●	± 10.5	± 11.8	V
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm 10.5V$	●	106	120	dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 4.5V$ to $\pm 18V$	●	102	120	dB
A_{VOL}	Large Signal Voltage Gain	$R_L \geq 2k\Omega, V_O = \pm 10V$ $R_L \geq 1k\Omega, V_O = \pm 10V$	●	2.5	18.0	$V/\mu V$
			●	2.0	14.0	$V/\mu V$
V_{OUT}	Maximum Output Voltage Swing	$R_L \geq 2k\Omega$	●	± 12.0	± 13.6	V
P_d	Power Dissipation		●	90	160	mW

The ● denotes the specifications which apply over full operating temperature range.

Note 1: Input Offset Voltage measurements are performed by automatic test equipment approximately 0.5 seconds after application of power.

Note 2: Long Term Input Offset Voltage Stability refers to the average trend line of Offset Voltage vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 days are typically $2.5\mu V$.

Note 3: This parameter is tested on a sample basis only.

Note 4: This parameter is guaranteed by design and is not tested.

Note 5: The inputs are protected by back-to-back diodes. Current limiting resistors are not used in order to achieve low noise. If differential input voltage exceeds $\pm 0.7V$, the input current should be limited to 25mA.

Note 6: The Average Input Offset Drift performance is within the specifications unnullled or when nullled with a pot having a range of $8k\Omega$ to $20k\Omega$.

2

NOTES

FEATURES

- **Guaranteed Bias Current**
 25°C 100pA max.
 -55°C to 125°C 600pA max.
- **Guaranteed Offset Voltage** 120μV max.
- **Guaranteed Drift** 1.5μV/°C max.
- **Low Noise, 0.1Hz to 10Hz** 0.5μVp-p
- **Guaranteed Low Supply Current** 600μA max.
- **Guaranteed CMRR** 114 dB min.
- **Guaranteed PSRR** 114 db min.
- **Guaranteed Voltage Gain with 5mA load current**

APPLICATIONS

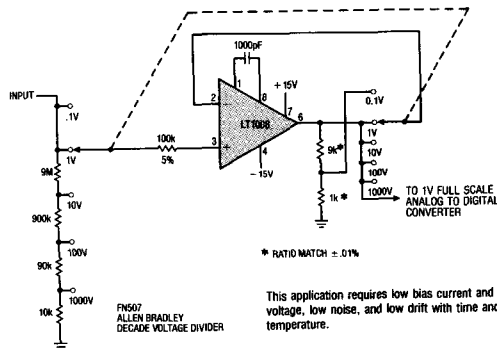
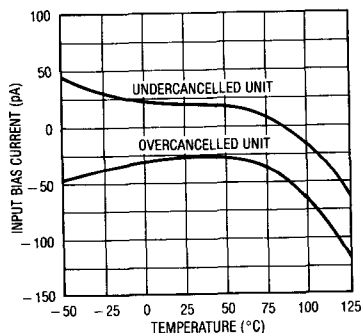
- Precision instrumentation
- Charge integrators
- Wide dynamic range logarithmic amplifiers
- Light meters
- Low frequency active filters
- Standard cell buffers
- Thermocouple amplifiers

DESCRIPTION

The LT1008 is a universal precision operational amplifier which can be used in practically all precision applications. The LT1008 combines for the first time picoampere bias currents (which are maintained over the full -55°C to 125°C temperature range) microvolt offset voltage (and low drift with time and temperature), low voltage and current noise, and low power dissipation. Extremely high common-mode and power supply rejection ratios, and the ability to deliver 5mA load current with high voltage gain round out the LT1008's superb precision specifications.

The all around excellence of the LT1008 eliminates the necessity of the time consuming error analysis procedure of precision system design in many applications; the LT1008 can be stocked as the universal precision op amp.

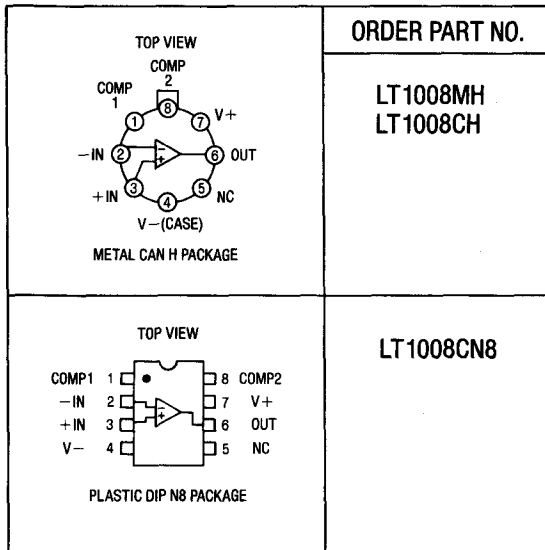
The LT1008 is externally compensated with a single capacitor for additional flexibility in shaping the frequency response of the amplifier. It plugs into and upgrades all standard LM108A/308A applications. For an internally compensated version with even lower offset voltage but otherwise similar performance see the LT1012.

2
Input Amplifier for 4½ Digit Voltmeter

Input Bias Current vs Temperature


ABSOLUTE MAXIMUM RATING

Supply Voltage..... ±20V
 Differential Input Current (Note 1)..... ±10mA
 Input Voltage..... ±20V
 Output Short Circuit Duration..... Indefinite
 Operating Temperature Range
 LT1008M..... -55°C to 125°C
 LT1008C..... 0°C to 70°C
 Storage Temperature Range
 All Devices..... -65°C to 150°C
 Lead Temperature (Soldering, 10 sec.)..... 300°C

PACKAGE/ORDER INFORMATION



ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $V_{CM} = 0V$, $T_A = 25^\circ C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1008M			LT1008C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	Note 2	30	40	120	30	40	120	μV
	Long Term Input Offset Voltage Stability		0.3			0.3			$\mu V/month$
I_{OS}	Input Offset Current	Note 2	30	40	100	30	40	100	pA
I_B	Input Bias Current	Note 2	±30	±40	±100	±30	±40	±100	pA
e_n	Input Noise Voltage	0.1Hz to 10Hz	0.5			0.5			$\mu Vp-p$
e_n	Input Noise Voltage Density	$f_0 = 10Hz$ (Note 3) $f_0 = 1000Hz$ (Note 4)	17	14	30	17	14	30	nV/√Hz
i_n	Input Noise Current Density	$f_0 = 10Hz$	20			20			fA/√Hz
A_{VOL}	Large Signal Voltage Gain	$V_{OUT} = \pm 12V, R_L \geq 10k\Omega$ $V_{OUT} = \pm 10V, R_L \geq 2k\Omega$	200	120	2000	200	120	2000	V/mV
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 13.5V$	114	114	132	114	114	132	dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 2V$ to $\pm 20V$	114	114	132	114	114	132	dB
	Input Voltage Range		±13.5	±13.5	±14.0	±13.5	±13.5	±14.0	V
V_{OUT}	Output Voltage Swing	$R_L = 10k\Omega$	±13	±13	±14	±13	±13	±14	V
	Slew Rate	$C_L = 30pF$	0.1	0.1	0.2	0.1	0.1	0.2	V/ μsec
I_S	Supply Current	Note 2	380			380			μA

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V, V_{CM} = 0V, 0^\circ C \leq T_A \leq 70^\circ C$ for the LT1008C and $-55^\circ C \leq T_A \leq 125^\circ C$ for the LT1008M, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1008M			LT1008C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	Note 2	●	50	250	●	40	180	μV
	Average Temperature Coefficient of Input Offset Voltage		●	0.2	1.5	●	0.2	1.5	$\mu V/^\circ C$
I_{OS}	Input Offset Current	Note 2	●	60	250	●	40	180	pA
	Average Temperature Coefficient of Input Offset Current		●	80	350	●	50	250	pA
I_b	Input Bias Current	Note 2	●	± 80	± 600	●	± 40	± 180	pA
	Average Temperature Coefficient of Input Bias Current		●	± 150	± 800	●	± 50	± 250	pA
A_{VOL}	Large Signal Voltage Gain	$V_{OUT} = \pm 12V, R_L \geq 10k\Omega$	●	100	1000	●	150	1500	V/mV
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 13.5V$	●	108	128	●	110	130	dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 2.5V$ to $\pm 20V$	●	108	126	●	110	128	dB
	Input Voltage Range		●	± 13.5		●	± 13.5		V
V_{OUT}	Output Voltage Swing	$R_L = 10k\Omega$	●	± 13	± 14	●	± 13	± 14	V
I_S	Supply Current		●	400	800	●	400	800	μA

2

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: Differential input voltages greater than 1V will cause excessive current to flow through the input protection diodes unless current limiting resistors are used.

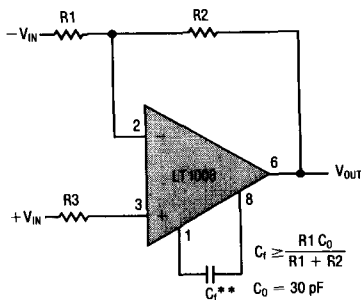
Note 2: These specifications apply for $\pm 2V \leq V_S \leq \pm 20V$ ($\pm 2.5V \leq V_S \leq \pm 20V$ over the temperature range) and $-13.5V \leq V_{CM} \leq 13.5V$ (for $V_S = \pm 15V$).

Note 3: 10Hz noise voltage density is sample tested on every lot. Devices 100% tested at 10Hz are available on request.

Note 4: This parameter is tested on a sample basis only.

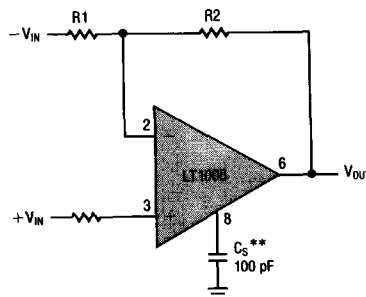
FREQUENCY COMPENSATION CIRCUITS

Standard Compensation Circuit



** BANDWIDTH AND SLEW RATE ARE PROPORTIONAL TO $1/C_T$

Alternate* Frequency Compensation

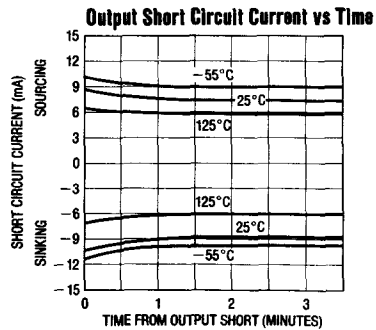
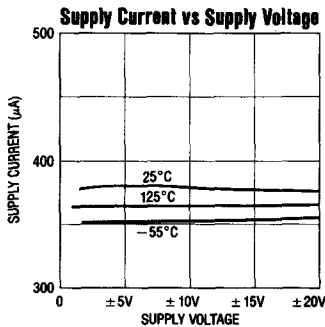
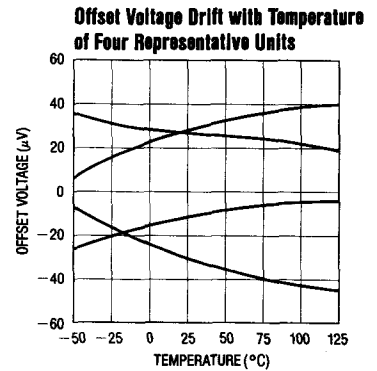
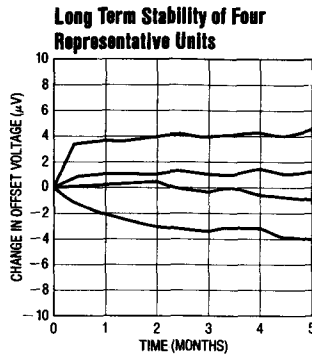
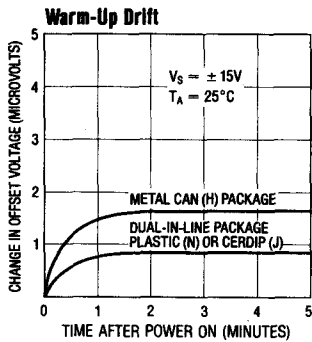
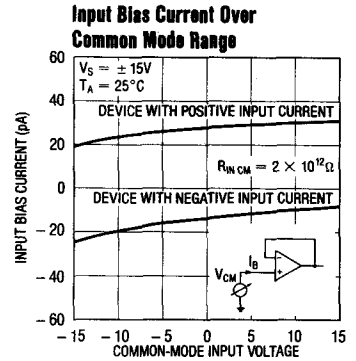
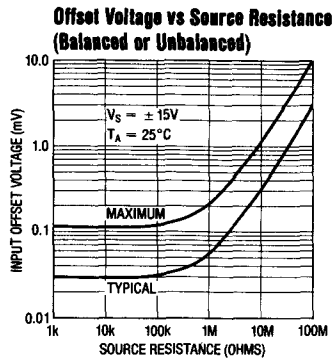
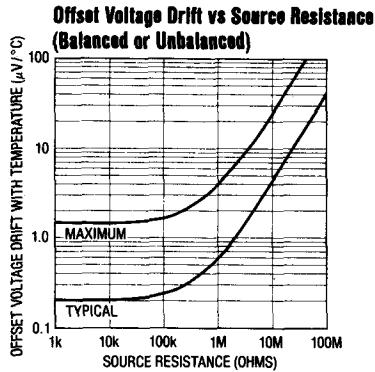


* IMPROVES REJECTION OF POWER SUPPLY NOISE BY A FACTOR OF 5.

** BANDWIDTH AND SLEW RATE ARE PROPORTIONAL TO $1/C_S$

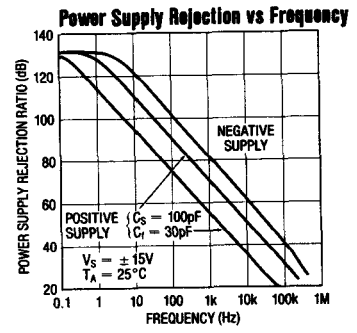
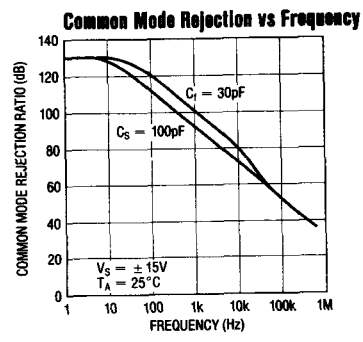
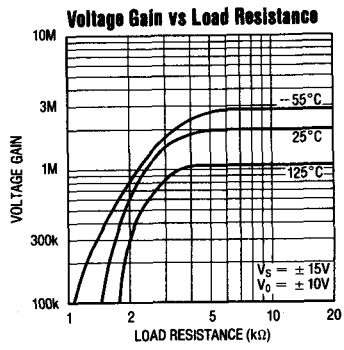
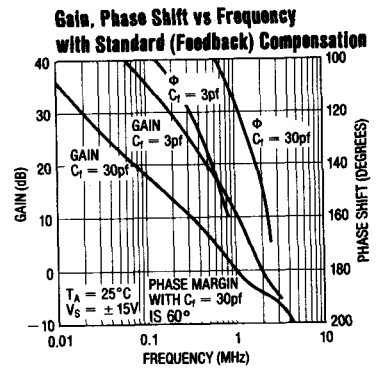
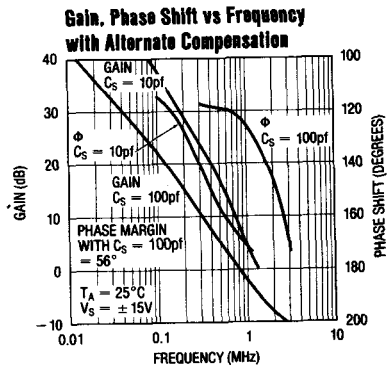
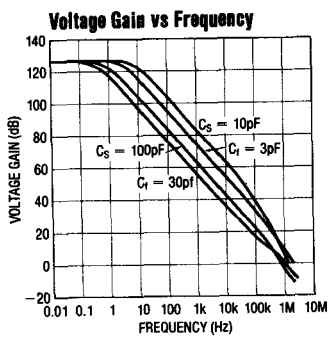
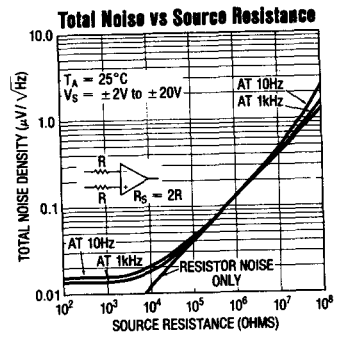
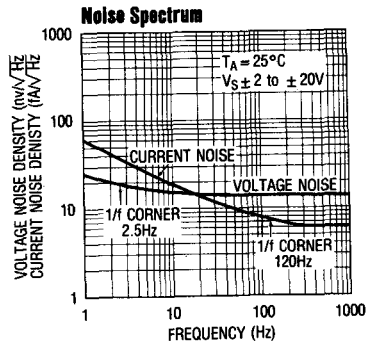
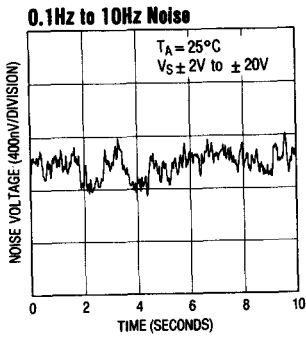
FOR $\frac{R2}{R1} > 200$ NO EXTERNAL FREQUENCY COMPENSATION IS NECESSARY

TYPICAL PERFORMANCE CHARACTERISTICS

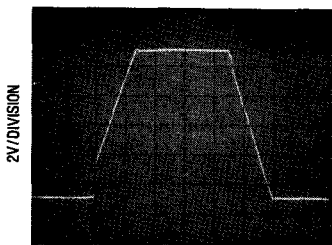


TYPICAL PERFORMANCE CHARACTERISTICS

2

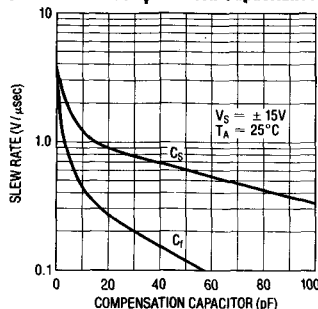


Large Signal Transient Response

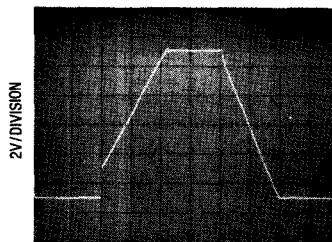


$A_V = +1, C_S = 100\text{pF}, 20\mu\text{sec}/\text{DIV}$

Slow Rate vs Compensation Capacitance

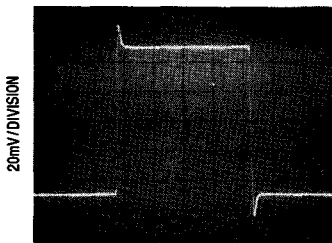


Large Signal Transient Response



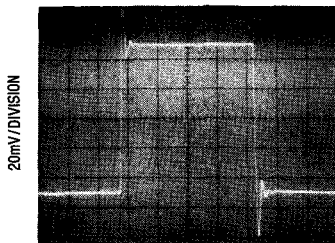
$A_V = +1, C_I = 30\text{pF}, 20\mu\text{sec}/\text{DIV}$

Small Signal Transient Response



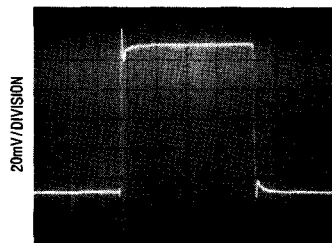
$A_V = +1, C_S = 100\text{pF}, C_{\text{LOAD}} = 100\text{pF}, 5\mu\text{sec}/\text{DIV}$

Small Signal Transient Response



$A_V = +1, C_S = 100\text{pF}, C_{\text{LOAD}} = 600\text{pF}, 5\mu\text{sec}/\text{DIV}$

Small Signal Transient Response



$A_V = +1, C_I = 30\text{pF}, C_{\text{LOAD}} = 100\text{pF}, 5\mu\text{sec}/\text{DIV}$

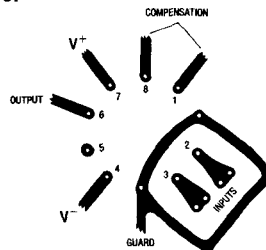
APPLICATIONS INFORMATION

Achieving Picoampere/Microvolt Performance

In order to realize the picoampere — microvolt level accuracy of the LT1008, proper care must be exercised. For example, leakage currents in circuitry external to the op amp can significantly degrade performance. High quality insulation should be used (e.g. Teflon, Kel-F); cleaning of all insulating surfaces to remove fluxes and other residues will probably be required. Surface coating may be necessary to provide a moisture barrier in high humidity environments.

Board leakage can be minimized by encircling the input circuitry with a guard ring operated at a potential close to that of the inputs: in inverting configurations the guard ring should be tied to ground, in non-invert-

ing connections to the inverting input at pin 2. Guarding both sides of the printed circuit board is required. Bulk leakage reduction depends on the guard ring width. Nanoampere level leakage into the compensation terminals can affect offset voltage and drift with temperature.

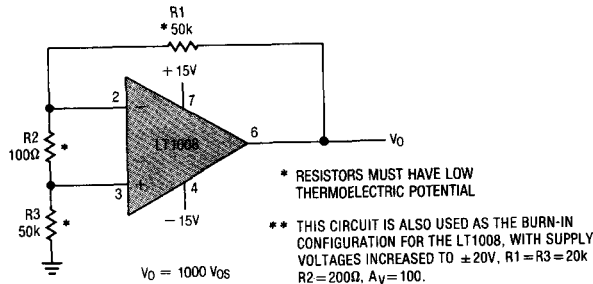


APPLICATIONS INFORMATION

Microvolt level error voltages can also be generated in the external circuitry. Thermocouple effects caused by temperature gradients across dissimilar metals at the contacts to the input terminals can exceed the inherent drift of the amplifier. Air currents over device leads should be minimized, package leads should be short, and the two input leads should be as close together as possible and maintained at the same temperature.

The LT1008 is specified over a wide range of power-supply voltages from $\pm 2V$ to $\pm 18V$. Operation with lower supplies is possible down to $\pm 1.0V$ (two Ni-Cad batteries).

Test Circuit for Offset Voltage and its Drift with Temperature



2

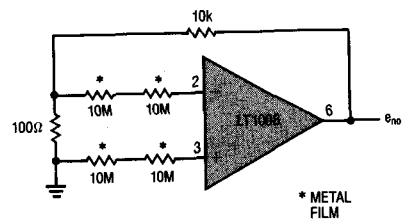
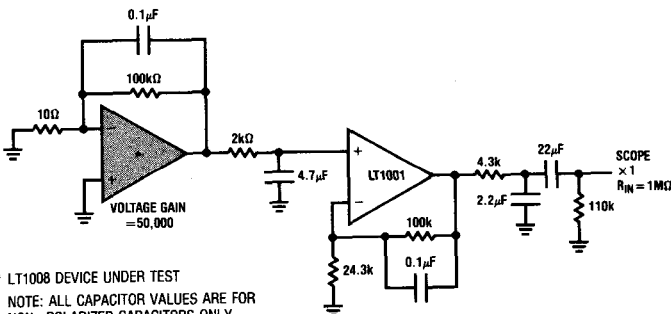
Noise Testing

The 0.1Hz to 10Hz peak-to-peak noise of the LT1008 is measured in the test circuit shown. The frequency response of this noise tester indicates that the 0.1Hz corner is defined by only one zero. The test time to measure 0.1Hz to 10Hz noise should not exceed 10 seconds, as this time limit acts as an additional zero to eliminate noise contributions from the frequency band below 0.1Hz.

A noise-voltage density test is recommended when measuring noise on a large number of units. A 10Hz noise-voltage density measurement will correlate well with a 0.1Hz to 10Hz peak-to-peak noise reading since both results are determined by the white noise and the location of the 1/f corner frequency. Current noise is measured in the circuit shown and calculated by the following formula where the noise of the source resistors is subtracted.

0.1Hz to 10Hz Noise Test Circuit

$$i_n = \frac{[e^2_{no} - (820nV)^2]^{1/2}}{40M\Omega \times 100}$$



APPLICATIONS INFORMATION

Frequency Compensation

The LT1008 is externally frequency compensated with a single capacitor. The two standard compensation circuits shown on page 3 are identical to the LM108A/308A frequency compensation schemes. Therefore, the LT1008 operational amplifiers can be inserted directly into LM108A/308A sockets, with similar AC and upgraded DC performance.

External frequency compensation provides the user with additional flexibility in shaping the frequency response of the amplifier. For example, for a voltage gain of ten, and $C_f = 3\text{pF}$, a gain bandwidth product of 5MHz and slew rate of $1.2\text{V}/\mu\text{sec}$ can be realized. For closed loop gains in excess of 200, no external compensation is necessary, and slew rate increases to $4\text{V}/\mu\text{sec}$. The LT1008 can also be overcompensated (i.e. $C_f > 30\text{pF}$ or $C_S > 100\text{pF}$) to improve capacitive load handling capability or to narrow noise band-

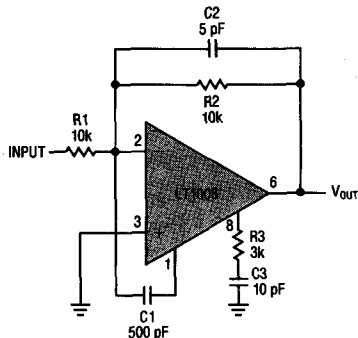
width. In many applications, the feedback loop around the amplifier has gain (e.g. logarithmic amplifiers); overcompensation can stabilize these circuits with a single capacitor.

The availability of the compensation terminals permits the use of feedforward frequency compensation to enhance slew rate in low closed loop gain configurations. The inverter slew rate is increased to $1.4\text{V}/\mu\text{sec}$. The voltage follower feedforward scheme bypasses the amplifier's gain stages and slews at nearly $10\text{V}/\mu\text{sec}$.

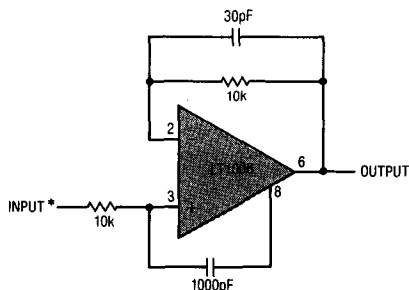
The inputs of the LT1008 are protected with back-to-back diodes. Current limiting resistors are not used, because the leakage of these resistors would prevent the realization of picoampere level bias currents at elevated temperatures. In the voltage follower configuration, when the input is driven by a fast, large signal pulse ($> 1\text{V}$), the input protection diodes effectively short the output to the input during slewing, and a current, limited only by the output short circuit protection will flow through the diodes.

The use of a feedback resistor, as shown in the voltage follower, feedforward diagram, is recommended because this resistor keeps the current below the short circuit limit, resulting in faster recovery and settling of the output.

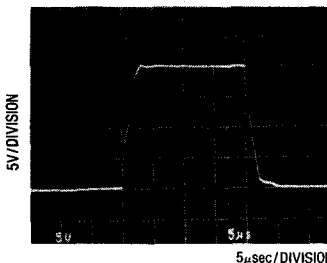
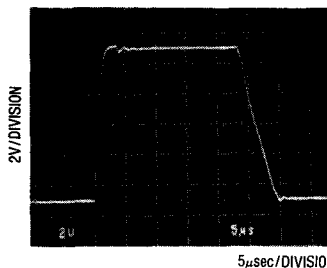
Inverter Feedforward Compensation



Follower Feedforward Compensation

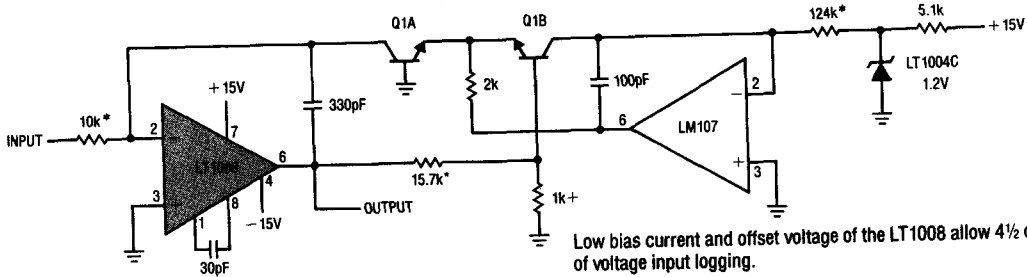


* SOURCE RESISTANCE $\ll 15\text{k}$ FOR STABILITY



APPLICATIONS

Logarithmic Amplifier

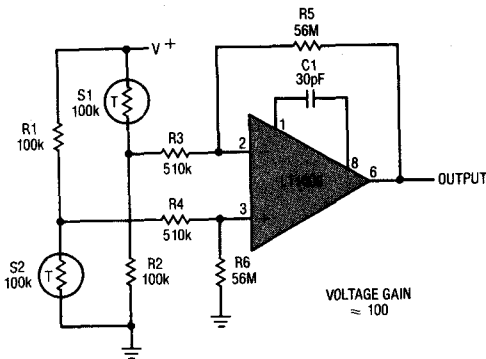


Low bias current and offset voltage of the LT1008 allow 4½ decades of voltage input logging.

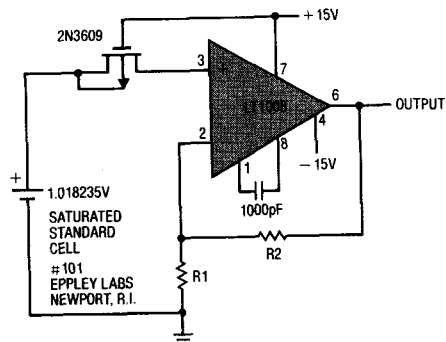
- + = TEL. LABS, TYPE Q81
- * = 1% FILM RESISTOR
- Q1 = 2N2979

2

Amplifier for Bridge Transducers

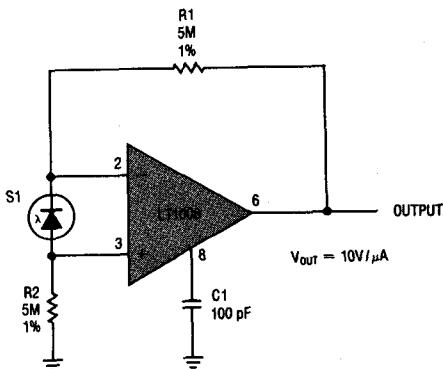


Saturated Standard Cell Amplifier

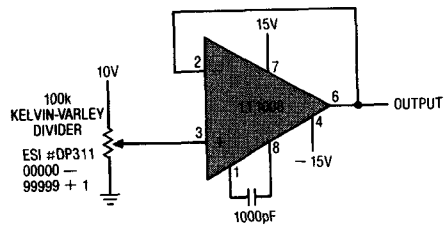


The typical 30pA bias current of the LT1008 will degrade the standard cell by only 1 ppm/year. Noise is a fraction of a ppm. Unprotected gate MOSFET isolates standard cell on power down.

Amplifier For Photodiode Sensor

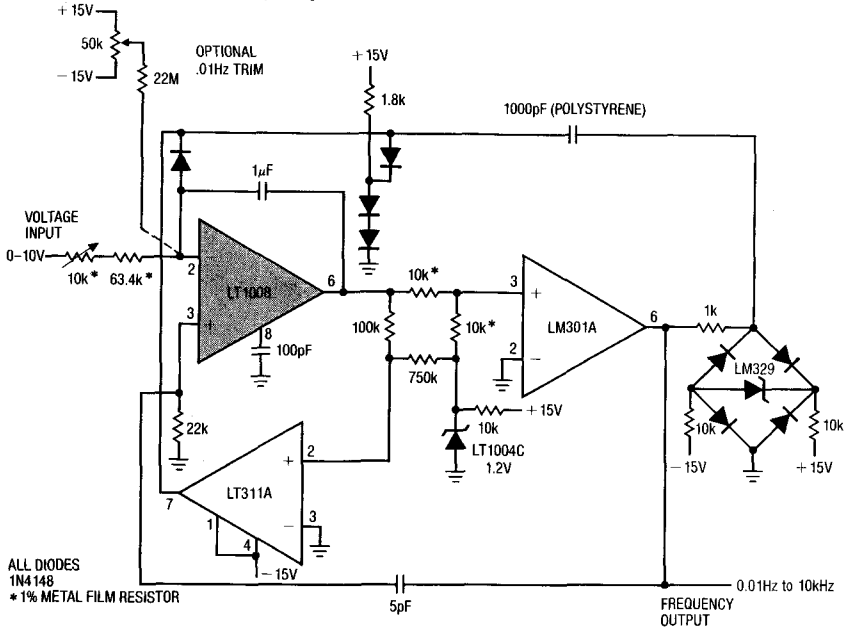


Five Decade Kelvin-Varley Divider Buffered by the LT1008



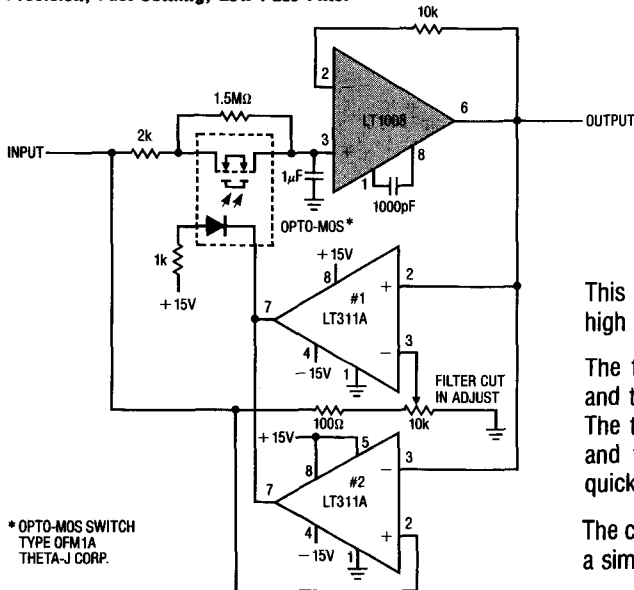
Approximate error due to noise, bias current, common-mode rejection, voltage gain of the amplifier is 1/5 of a least significant bit.

Extended Range Charge Pump Voltage to Frequency Converter



The LT1008 integrator extends low frequency range. Total dynamic range is 0.01Hz to 10kHz (or 120dB) with 0.01% linearity.

Precision, Fast Settling, Low Pass Filter

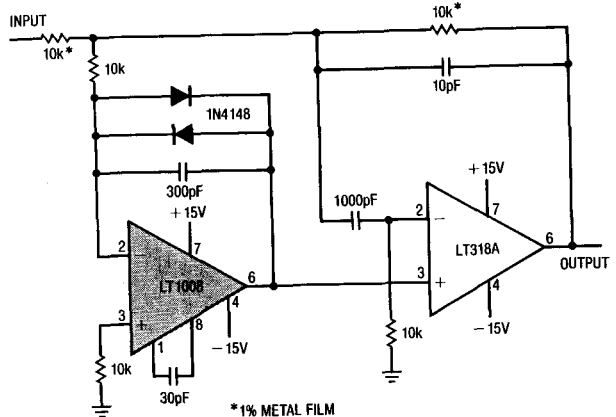
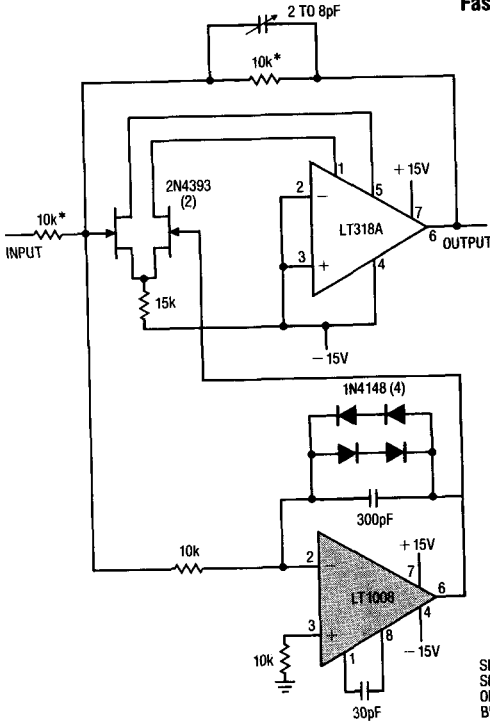


This circuit is useful where fast signal acquisition and high precision are required, as in electronic scales.

The filter's time constant is set by the 2K Ω resistor and the 1 μ F capacitor until comparator #1 switches. The time constant is then set by the 1.5M Ω resistor and the 1 μ F capacitor. Comparator #2 provides a quick reset.

The circuit settles to a final value three times as fast as a simple 1.5M Ω — 1 μ F filter, with almost no DC error.

Fast Precision Inverters

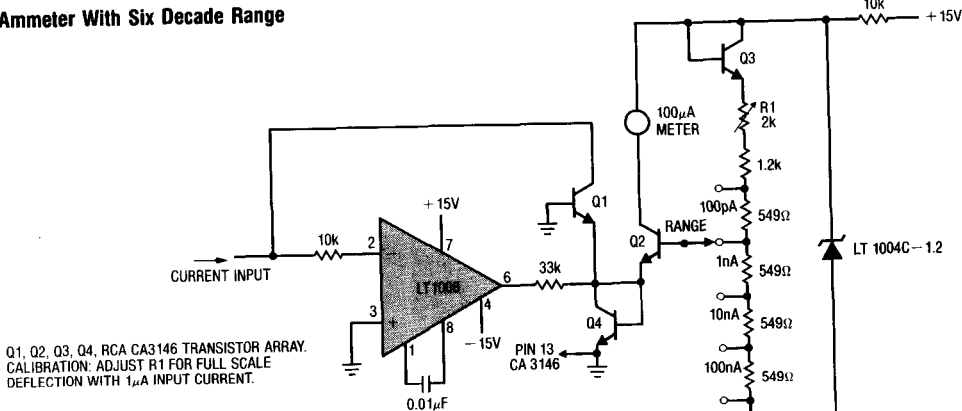


FULL POWER BANDWIDTH = 2MHz
 SLEW RATE = 50V/ μ sec
 SETTLEING (10V STEP) = 12 μ S TO 0.01%
 BIAS CURRENT DC = 30pA
 OFFSET DRIFT = 0.3 μ V/ $^{\circ}$ C
 OFFSET VOLTAGE = 30 μ V

SLEW RATE @ 100V/ μ S
 SETTLEING = 5 μ S TO 0.01% / 10 VOLT STEP
 OFFSET VOLTAGE = 30 μ V
 BIAS CURRENT = 30pA
 * 1% METAL FILM

2

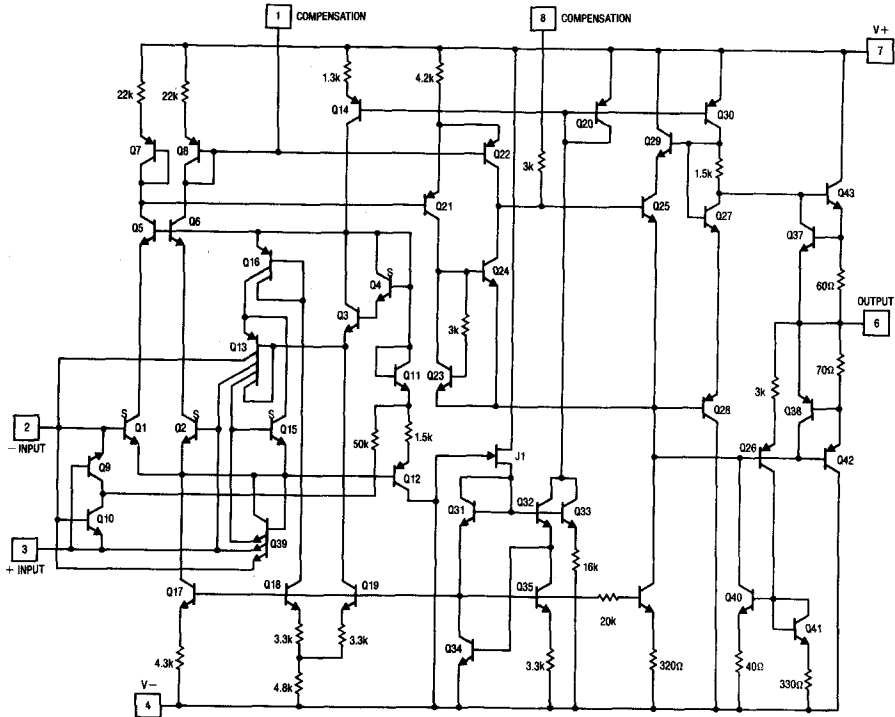
Ammeter With Six Decade Range



Q1, Q2, Q3, Q4, RCA CA3146 TRANSISTOR ARRAY.
 CALIBRATION: ADJUST R1 FOR FULL SCALE
 DEFLECTION WITH 1 μ A INPUT CURRENT.

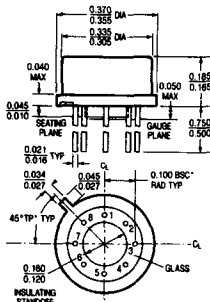
Ammeter measures currents from 100pA to 100 μ A without the use of expensive high value resistors. Accuracy at 100 μ A is limited by the offset voltage between Q1 and Q2 and, at 100pA, by the inverting bias current of the LT1008.

SCHEMATIC DIAGRAM



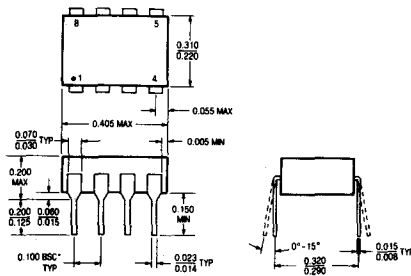
PACKAGE DESCRIPTION

H Package
Metal Can



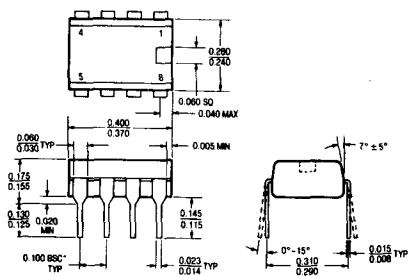
T_{jmax}	$\theta_{j\alpha}$	θ_{jc}
150°C	150°C/W	45°C/W

J8 Package
8 Lead Hermetic Dip



T_{jmax}	$\theta_{j\alpha}$
150°C	100°C/W

N8 Package
8 Lead Plastic



T_{jmax}	$\theta_{j\alpha}$
100°C	130°C/W

FEATURES

- 20MHz Bandwidth
- $75\text{V}/\mu\text{s}$ Slew Rate
- Drives $\pm 10\text{V}$ into 75Ω
- 5mA Quiescent Current
- Drives Capacitive Loads $> 1\mu\text{F}$
- Current and Thermal Limit
- Operates from Single Supply $\geq 4.5\text{V}$
- Very Low Distortion Operation

APPLICATIONS

- Boost Op Amp Output
- Isolate Capacitive Loads
- Drive Long Cables
- Audio Amplifiers
- Video Amplifiers
- Power Small Motors
- Operational Power Supply
- FET Driver

DESCRIPTION

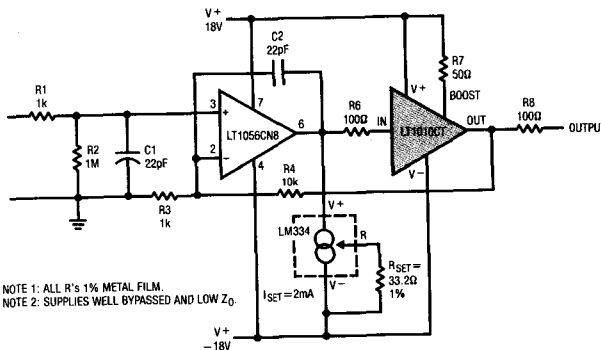
The LT1010 is a fast, unity-gain buffer that can increase the output capability of existing IC op amps by more than an order of magnitude. This easy-to-use part makes fast amplifiers less sensitive to capacitive loading, reduces thermal feedback in precision dc amplifiers and is recommended for a wide range of fast and slow applications.

Designed to be incorporated within the feedback loop, the buffer can isolate almost any reactive load. Internal operating currents are essentially unaffected by supply or output voltage, accounting for the 4.5V to 40V supply voltage range with unchanged specifications. Single-supply operation is also practical.

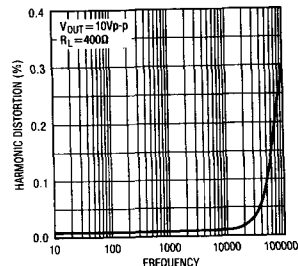
This monolithic IC is supplied in an 8-pin miniDIP and three standard power packages: the solid kovar base TO-5 (TO-39), the steel TO-3 and the plastic TO-220. The low thermal resistance power packages are an aid in reducing operating junction temperatures. With the TO-3, TO-220, and miniDIP packages, an option is available to raise quiescent current and improve speed. The miniDIP version is supplied for those applications not requiring high power dissipation or where board space is a premium.

In the TO-39 package, the LT1010 can sometimes replace the hybrid LH0002. With the exception of speed it exceeds key specifications and fault protection is vastly superior. Further, the lower thermal resistance package and higher maximum operating temperature of the new monolithic circuit allow more usable output.

Very Low Distortion Buffered Pre-Amplifier



NOTE 1: ALL R'S 1% METAL FILM.
 NOTE 2: SUPPLIES WELL BYPASSED AND LOW Z_0 .



LT1010

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage	± 22V	Input Current (Note 2)	± 40mA
Continuous Output Current	± 150mA	Operating Junction Temperature	
Continuous Power Dissipation (Note 1)		LT1010M	- 55°C to 150°C
LT1010MK	5.0W	LT1010C	0°C to 125°C
LT1010CK	4.0W	Storage Temperature	- 65°C to 150°C
LT1010CT	4.0W	Lead Temperature (Soldering, 10 sec.)	300°C
LT1010MH	3.1W		
LT1010CH	2.5W		
LT1010CN8	0.75W		

PRECONDITIONING

100% Thermal Limit Burn in

PACKAGE/ORDER INFORMATION

<p>BOTTOM VIEW</p> <p>K PACKAGE 4-LEAD TO-3 METAL CAN (STEEL)</p>	<p>ORDER PART NUMBER</p> <p>LT1010MK LT1010CK</p>	<p>FRONT VIEW</p> <p>T PACKAGE 5-LEAD TO-220 PLASTIC</p>	<p>ORDER PART NUMBER</p> <p>LT1010CT</p>
<p>BOTTOM VIEW</p> <p>H PACKAGE 4-LEAD TO-39 METAL CAN (KOVAR BASE)</p>	<p>LT1010MH LT1010CH</p>	<p>TOP VIEW</p> <p>N PACKAGE 8-LEAD PLASTIC DIP</p>	<p>LT1010CN8</p>

ELECTRICAL CHARACTERISTICS (See Note 3. Typical values in curves)

SYMBOL	PARAMETER	CONDITIONS (NOTE 3)	LT1010M		LT1010C		UNITS	
			MIN	MAX	MIN	MAX		
V _{OS}	Output Offset Voltage	Note 3	20	110	0	150	mV	
		●	-10	220	-20	220	mV	
		V _S = ±15V, V _{IN} = 0	40	90	20	100	mV	
I _B	Input Bias Current	I _{OUT} = 0	0	150	0	250	μA	
		I _{OUT} ≤ 150mA	0	250	0	500	μA	
		●	0	300	0	800	μA	
A _V	Large Signal Voltage Gain	●	0.995	1.00	0.995	1.00	V/V	
R _{OUT}	Output Resistance	I _{OUT} = ±1mA	6	9	5	10	Ω	
		I _{OUT} = ±150mA	6	9	5	10	Ω	
	Slew Rate	V _S = ±15V, V _{IN} = ±10V V _{OUT} = ±8V, R _L = 100Ω	75		75		V/μs	
V _{SOS} ⁺	Positive Saturation Offset	Note 4, I _{OUT} = 0	●	1.0 1.1	1.0 1.1		V	
V _{SOS} ⁻	Negative Saturation Offset	Note 4, I _{OUT} = 0	●	0.2 0.3	0.2 0.3		V	
R _{SAT}	Saturation Resistance	Note 4, I _{OUT} = ±150mA	●	18 24	22 28		Ω	
V _{BIAS}	Bias Terminal Voltage	Note 5, R _{BIAS} = 20Ω	●	750 560	810 925	700 560	840 880	mV
							9	mA
I _S	Supply Current	I _{OUT} = 0, I _{BIAS} = 0	●	8 9		10	mA	

2

Note 1: For case temperatures above 25°C, dissipation must be derated based on a thermal resistance of 25°C/W with the K and T packages, 40°C/W with the H package, and 130°C/W for N8 package for ambient temperatures above 25°C. See applications information.

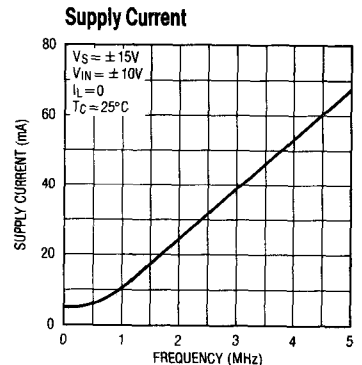
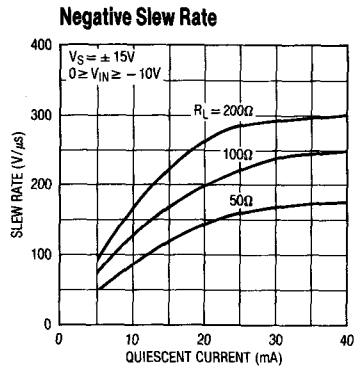
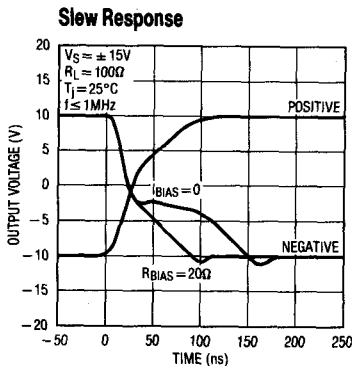
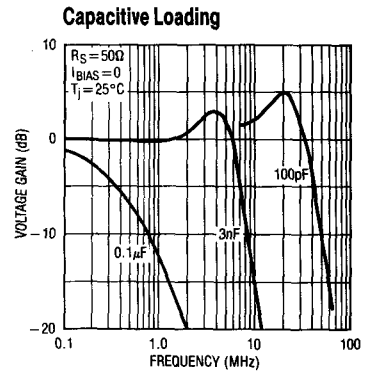
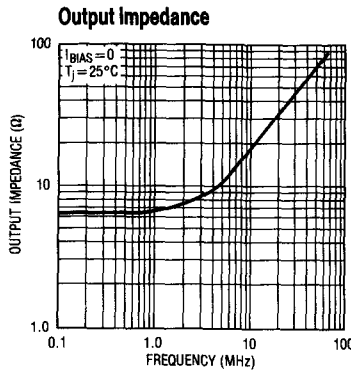
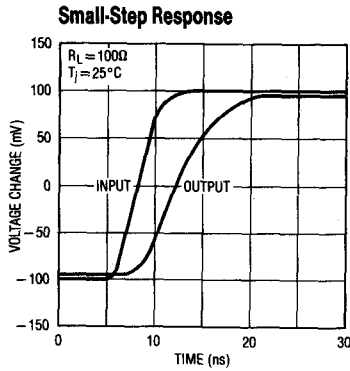
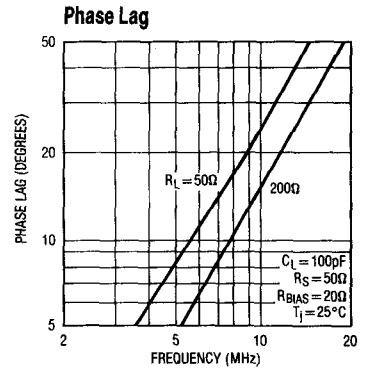
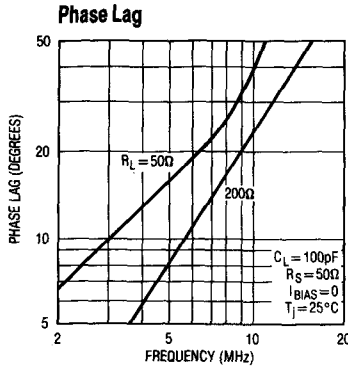
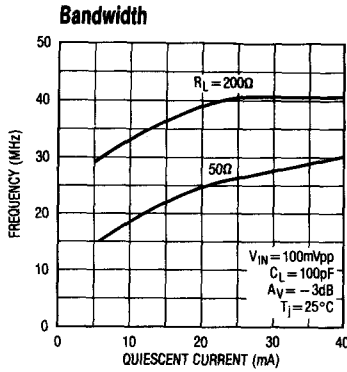
Note 2: In current limit or thermal limit, input current increases sharply with input-output differentials greater than 8V; so input current must be limited. Input current also rises rapidly for input voltages 8V above V⁺ or 0.5V below V⁻.

Note 3: Specifications apply for 4.5V ≤ V_S ≤ 40V, V⁻ + 0.5V ≤ V_{IN} ≤ V⁺ - 1.5V and I_{OUT} = 0, unless otherwise stated. Temperature range is -55°C ≤ T_J ≤ 150°C, T_C ≤ 125°C, for the LT1010M and 0°C ≤ T_J ≤ 125°C, T_C ≤ 100°C, for the LT1010C. The ● denotes the specifications that apply over the full temperature range.

Note 4: The output saturation characteristics are measured with 100mV output clipping. See applications information for determining available output swing and input drive requirements for a given load.

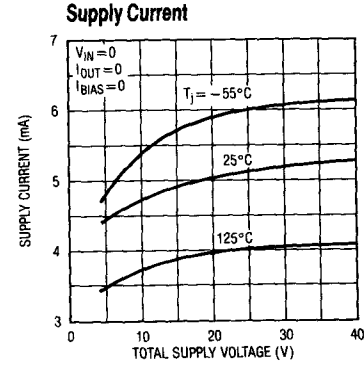
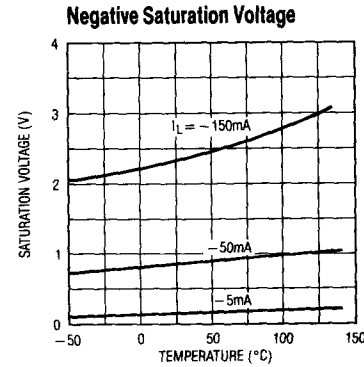
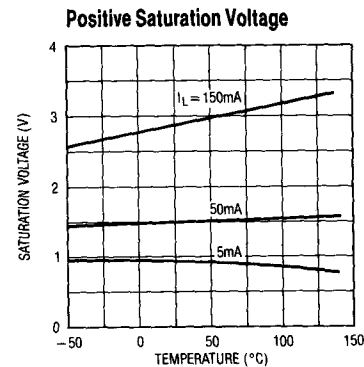
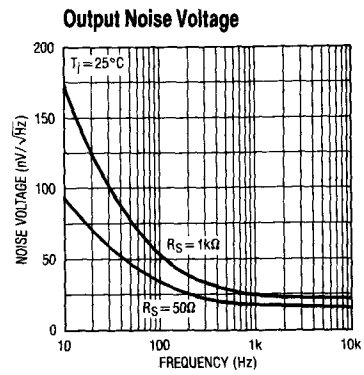
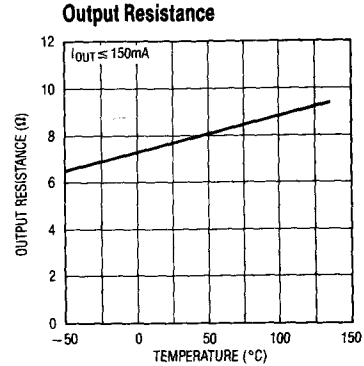
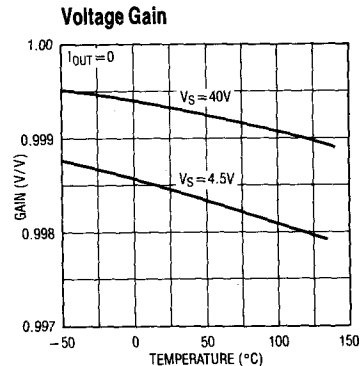
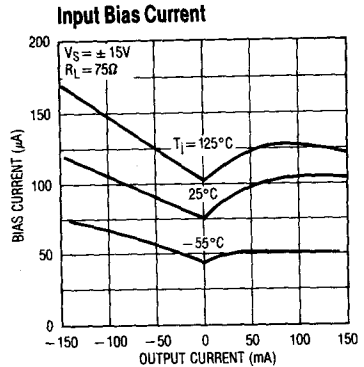
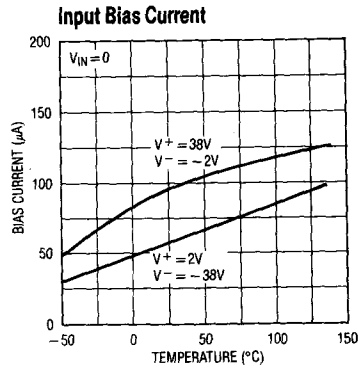
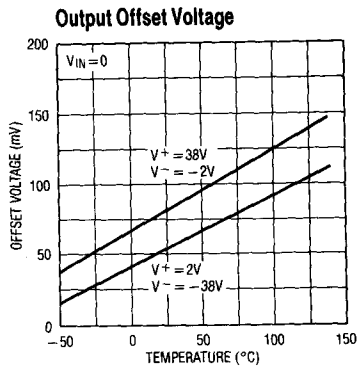
Note 5: With the TO-3 and TO-220 packages, output stage quiescent current can be increased by connecting a resistor between the bias pin and V⁺. The increase is equal to the bias terminal voltage divided by this resistance.

TYPICAL PERFORMANCE CHARACTERISTICS



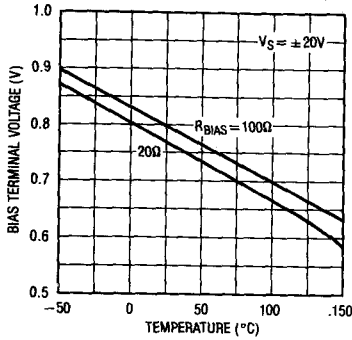
TYPICAL PERFORMANCE CHARACTERISTICS

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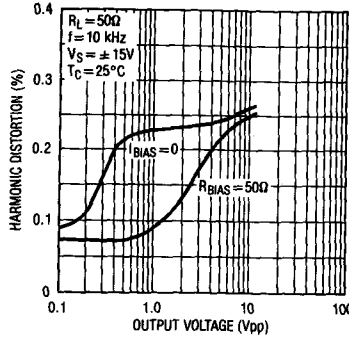


TYPICAL PERFORMANCE CHARACTERISTICS

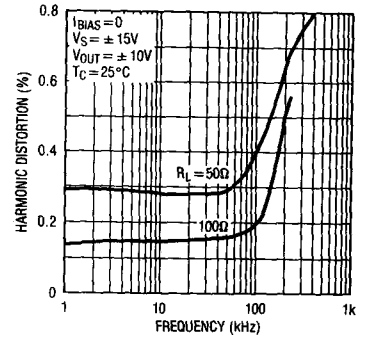
Bias Terminal Voltage



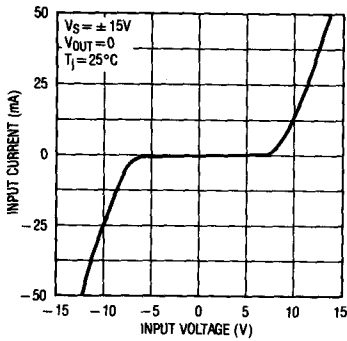
Total Harmonic Distortion



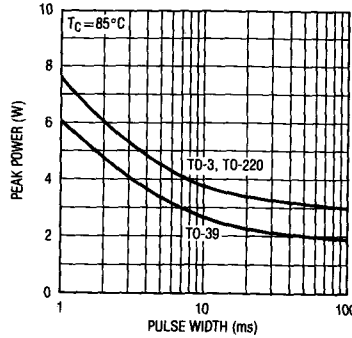
Total Harmonic Distortion



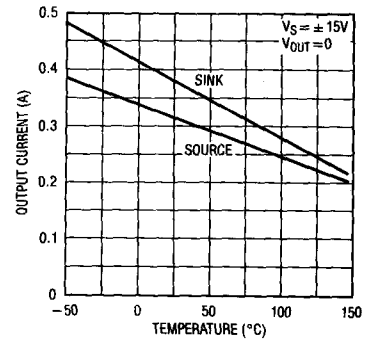
Shorted Input Characteristics



Peak Power Capability



Peak Output Current



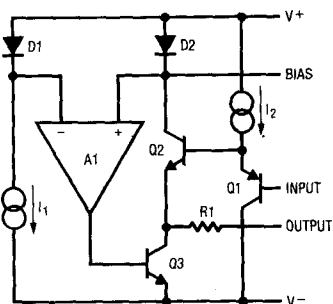
APPLICATIONS INFORMATION

General

These notes briefly describe the LT1010 and how it is used; a detailed explanation is given elsewhere*. Emphasis here will be on practical suggestions that have resulted from working extensively with the part over a wide range of conditions. A number of applications are also outlined that demonstrate the usefulness of the buffer beyond that of driving a heavy load.

Design Concept

The schematic below describes the basic elements of the buffer design. The op amp drives the output sink transistor, Q3, such that the collector current of the output follower, Q2, never drops below the quiescent value (determined by I_1 and the area ratio of D1 and D2). As a result, the high frequency response is essentially that of a simple follower even when Q3 is supplying the load current. The internal feedback loop is isolated from the effects of capacitive loading by a small resistor in the output lead.

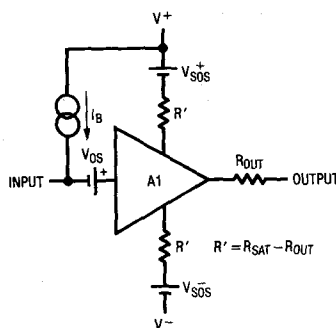


The scheme is not perfect in that the rate of rise of sink current is noticeably less than for source current. This can be mitigated by connecting a resistor between the bias terminal and V^+ , raising quiescent current. A feature of the final design is that the output resistance is largely independent of the follower quiescent current or the output load current. The output will also swing to the negative rail, which is particularly useful with single-supply operation.

*R. J. Widlar, "Unique IC Buffer Enhances Op Amp Designs; Times Fast Amplifiers," *Linear Technology Corp. TP-1*, April, 1984.

Equivalent Circuit

Below 1MHz, the LT1010 is quite accurately represented by the equivalent circuit shown here for both small and large signal operation. The internal element, A1, is an idealized buffer with the unloaded gain specified for the LT1010. Otherwise, it has zero offset voltage, bias current and output resistance. Its output also saturates to the internal supply terminals†.



Loaded voltage gain can be determined from the unloaded gain, A_V , the output resistance, R_{OUT} , and the load resistance, R_L , using:

$$A_{VL} = \frac{A_V R_L}{R_{OUT} + R_L}$$

Maximum positive output swing is given by:

$$V_{OUT}^+ = \frac{(V^+ - V_{SOS}^+) R_L}{R_{SAT} + R_L}$$

The input swing required for this output is:

$$V_{IN}^+ = V_{OUT}^+ \left(1 + \frac{R_{OUT}}{R_L} \right) - V_{OS} + \Delta V_{OS}$$

where ΔV_{OS} is the 100mV clipping specified for the saturation measurements. Negative output swing and input drive requirements are similarly determined.

† See electrical characteristics section for guaranteed limits.

APPLICATIONS INFORMATION

Supply Bypass

The buffer is no more sensitive to supply bypassing than slower op amps, as far as stability is concerned. The $0.1\mu\text{F}$ disc ceramic capacitors usually recommended for op amps are certainly adequate for low frequency work. As always, keeping the capacitor leads short and using a ground plane is prudent, especially when operating at high frequencies.

The buffer slew rate can be reduced by inadequate supply bypass. With output current changes much above $100\text{mA}/\mu\text{s}$, using $10\mu\text{F}$ solid tantalum capacitors on both supplies is good practice, although bypassing from the positive to the negative supply may suffice.

When used in conjunction with an op amp and heavily loaded (resistive or capacitive), the buffer can couple into supply leads common to the op amp causing stability problems with the overall loop and extended settling time. Adequate bypassing can usually be provided by $10\mu\text{F}$ solid tantalum capacitors. Alternately, smaller capacitors could be used with decoupling resistors. Sometimes the op amp has much better high frequency rejection on one supply, so bypass requirements are less on this supply.

Power Dissipation

In many applications, the LT1010 will require heat sinking. Thermal resistance, junction to still air is $150^\circ\text{C}/\text{W}$ for the TO-39 package, $100^\circ\text{C}/\text{W}$ for the TO-220 package, $60^\circ\text{C}/\text{W}$ for the TO-3 package, and $130^\circ\text{C}/\text{W}$ for the miniDIP package. Circulating air, a heat sink, or mounting the package to a printed circuit board will reduce thermal resistance.

In dc circuits, buffer dissipation is easily computed. In ac circuits, signal waveshape and the nature of the load determine dissipation. Peak dissipation can be several

times average with reactive loads. It is particularly important to determine dissipation when driving large load capacitance.

With ac loading, power is divided between the two output transistors. This reduces the effective thermal resistance, junction to case, to $30^\circ\text{C}/\text{W}$ for the TO-39 package and $15^\circ\text{C}/\text{W}$ for the TO-3 and TO-220 packages, as long as the peak rating of neither output transistor is exceeded. The typical curves indicate the peak dissipation capabilities of one output transistor.

Overload Protection

The LT1010 has both instantaneous current limit and thermal overload protection. Foldback current limiting has not been used, enabling the buffer to drive complex loads without limiting. Because of this, it is capable of power dissipation in excess of its continuous ratings.

Normally, thermal overload protection will limit dissipation and prevent damage. However, with more than 30V across the conducting output transistor, thermal limiting is not quick enough to insure protection in current limit. The thermal protection is effective with 40V across the conducting output transistor as long as the load current is otherwise limited to 150mA.

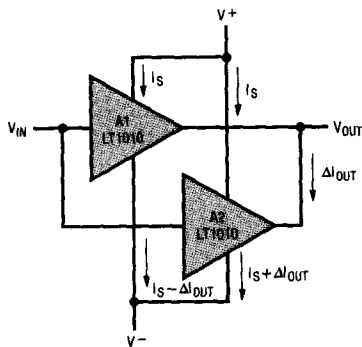
Drive Impedance

When driving capacitive loads, the LT1010 likes to be driven from a low source impedance at high frequencies. Certain low power op amps (e.g., the LM10) are marginal in this respect. Some care may be required to avoid oscillations, especially at low temperatures.

Bypassing the buffer input with more than 200pF will solve the problem. Raising the operating current also works, but this cannot be done with the TO-39 package.

APPLICATIONS INFORMATION

Parallel Operation



Parallel operation provides reduced output impedance, more drive capability and increased frequency response under load. Any number of buffers can be directly paralleled as long as the increased dissipation in individual units caused by mismatches of output resistance and offset voltage is taken into account.

When the inputs and outputs of two buffers are connected together, a current, ΔI_{OUT} , flows between the outputs:

$$\Delta I_{OUT} = \frac{V_{OS1} - V_{OS2}}{R_{OUT1} + R_{OUT2}}$$

where V_{OS} and R_{OUT} are the offset voltage and output resistance of the respective buffers.

Normally, the negative supply current of one unit will increase and the other decrease, with the positive supply current staying the same. The worst case ($V_{IN} - V^+$) increase in standby dissipation can be assumed to be $\Delta I_{OUT} V_T$, where V_T is the total supply voltage.

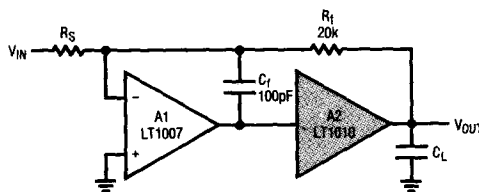
Offset voltage is specified worst case over a range of supply voltages, input voltage and temperature. It would be unrealistic to use these worst case numbers above because paralleled units are operating under identical conditions. The offset voltage specified for $V_S = \pm 15V$, $V_{IN} = 0$ and $T_A = 25^\circ C$ will suffice for a worst case condition.

Output load current will be divided based on the output resistance of the individual buffers. Therefore, the available output current will not quite be doubled unless output resistances are matched. As for offset voltage, the $25^\circ C$ limits should be used for worst case calculations.

Parallel operation is not thermally unstable. Should one unit get hotter than its mates, its share of the output and its standby dissipation will decrease.

As a practical matter, parallel connection needs only some increased attention to heat sinking. In some applications, a few ohms equalization resistance in each output may be wise. Only the most demanding applications should require matching, and then just of output resistance at $25^\circ C$.

Isolating Capacitive Loads



The inverting amplifier above shows the recommended method of isolating capacitive loads. Non-inverting amplifiers are handled similarly.

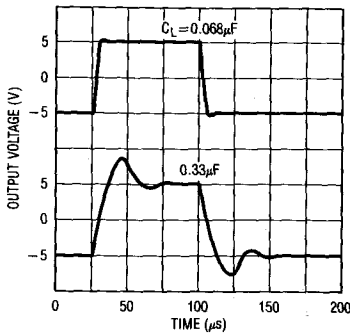
At lower frequencies, the buffer is within the feedback loop so that its offset voltage and gain errors are negligible. At higher frequencies, feedback is through C_f , so that phase shift from the load capacitance acting against the buffer output resistance does not cause loop instability.

Stability depends upon the $R_f C_f$ time constant, or the closed loop bandwidth. With an 80kHz bandwidth, ringing is negligible for $C_L = 0.068\mu F$ and damps rapidly for $C_L = 0.33\mu F$. The pulse response is shown in the graph.

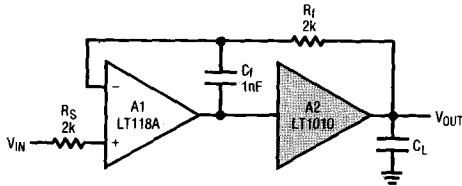
2

APPLICATIONS INFORMATION

Pulse Response



Small signal bandwidth is reduced by C_f , but considerable isolation can be obtained without reducing it below the power bandwidth. Often, a bandwidth reduction is desirable to filter high frequency noise or unwanted signals.

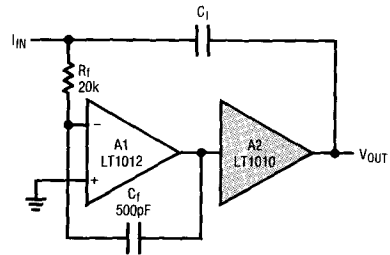


The follower configuration is unique in that capacitive load isolation is obtained without a reduction in small signal bandwidth, although the output impedance of the buffer comes into play at high frequencies. The precision unity-gain buffer above has a 10MHz bandwidth without capacitive loading, yet it is stable for all load capacitance to over $0.3\mu\text{F}$, again determined by $R_f C_f$.

This is a good example of how fast op amps can be made quite easy to use by employing an output buffer.

Integrator

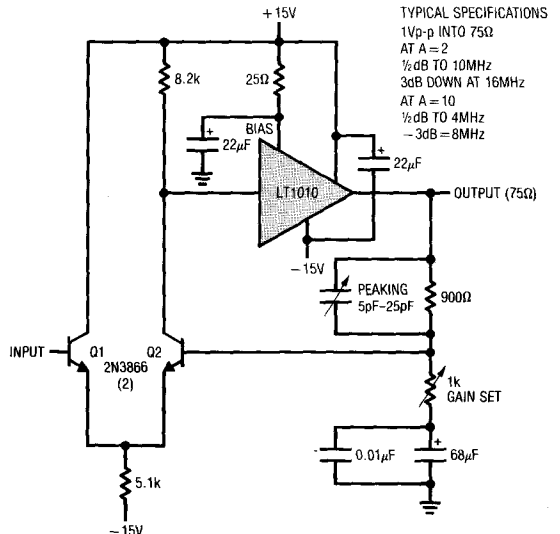
A low pass amplifier can be formed just by using large C_f in the inverter described earlier, as long as the increasing closed loop output impedance above the cutoff frequency is not a problem and the op amp is capable of supplying the required current at the summing junction.



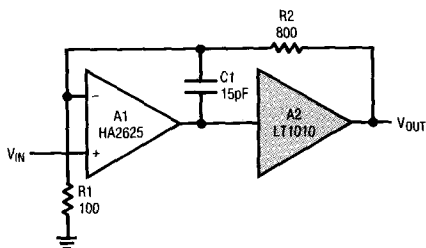
If the integrating capacitor must be driven from the buffer output, the circuit above can be used to provide capacitive load isolation. As before, the stability with large capacitive loads is determined by $R_f C_f$.

Wideband Amplifiers

This simple circuit provides an adjustable gain video amplifier which will drive 1Vp-p into 75Ω. The differential pair provides gain, with the LT1010 serving as an output stage. Feedback is arranged in the conventional manner, although the $68\mu\text{F} - 0.01$ combination limits dc gain to unity for all gain settings. For applications sensitive to NTSC requirements, dropping the 25Ω output stage bias value will aid performance.



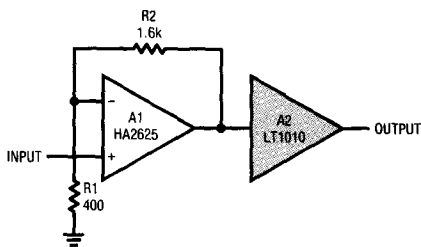
APPLICATIONS INFORMATION



This shows the buffer being used with a wideband amplifier that is not unity-gain stable. In this case, C1 cannot be used to isolate large capacitive loads. Instead, it has an optimum value for a limited range of load capacitances.

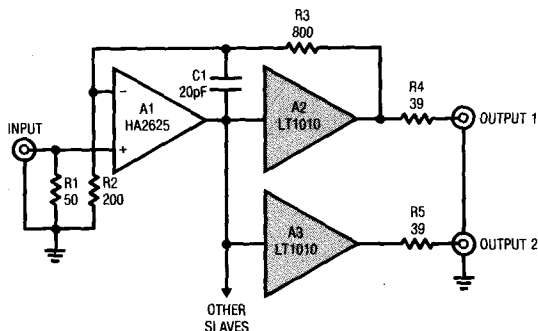
The buffer can cause stability problems in circuits like this. With the TO-3 and TO-220 packages, behavior can be improved by raising the quiescent current with a 20Ω resistor from the bias terminal to V⁺. Alternately, devices in the TO-39 package or miniDIP can be operated in parallel.

It is possible to improve capacitive load stability by operating the buffer class-A at high frequencies. This is done by using quiescent current boost and bypassing the bias terminal to V⁻ with more than 0.02μF.



Putting the buffer outside the feedback loop as shown here will give capacitive load isolation, with large output

capacitors only reducing bandwidth. Buffer offset, referred to the op amp input, is divided by the gain. If the load resistance is known, gain error is determined by the output resistance tolerance. Distortion is low.



The 50Ω video line splitter here puts feedback on one buffer, with the others slaved. Offset and gain accuracy of slaves depend on their matching with master.

When driving long cables, including a resistor in series with the output should be considered. Although it reduces gain, it does isolate the feedback amplifier from the effects of unterminated lines which present a resonant load.

When working with wideband amplifiers, special attention should *always* be paid to supply bypassing, stray capacitance and keeping leads short. Direct grounding of test probes, rather than the usual ground lead, is absolutely necessary for reasonable results.

The LT1010 has slew limitations that are not obvious from standard specifications. Negative slew is subject to glitching, but this can be minimized with quiescent current boost. The appearance is always worse with fast rise signal generators than in practical applications.

2

APPLICATIONS INFORMATION

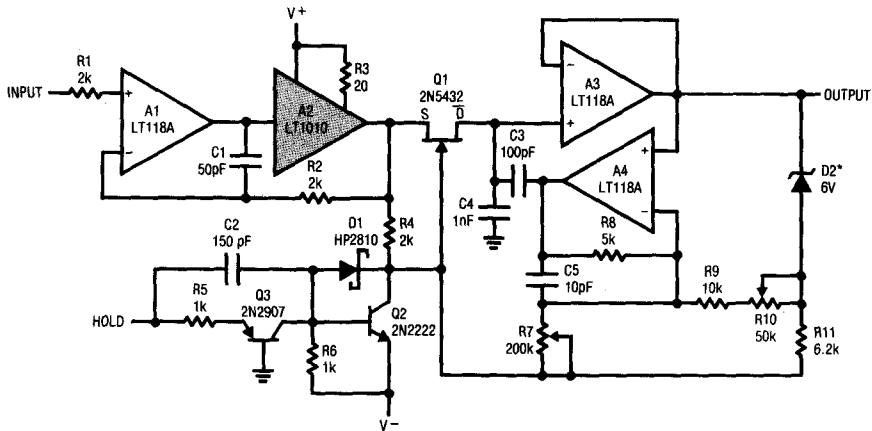
Track and Hold

The 5MHz track and hold shown here has a 400kHz power bandwidth driving $\pm 10V$. A buffered input follower drives the hold capacitor, C4, through Q1, a low resistance FET switch. The positive hold command is supplied by TTL logic, with Q3 level shifting to the switch driver, Q2. The output is buffered by A3.

When the gate is driven to V^- for HOLD, it pulls charge out of the hold capacitor. A compensating charge is put into the hold capacitor through C3. The step into hold is made independent of the input level with R7 and adjusted to zero with R10.

Since internal dissipation can be quite high when driving fast signals into a capacitive load, using a buffer in a power package is recommended. Raising buffer quiescent current to 40mA with R3 improves frequency response.

This circuit is equally useful as a fast acquisition sample and hold. An LF156 might be used for A3 to reduce drift in hold because its lower slew rate is not usually a problem in this application.

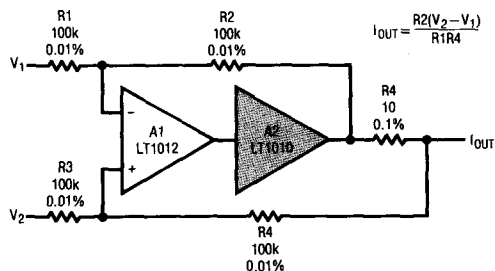


*2N2369 EMITTER BASE JUNCTION

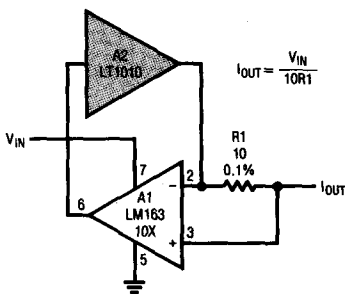
APPLICATIONS INFORMATION

Current Sources

A standard op amp voltage to current converter with a buffer to increase output current is shown here. As usual, excellent matching of the feedback resistors is required to get high output resistance. Output is bi-directional.



This circuit uses an instrumentation amplifier to eliminate the matched resistors. The input is not high impedance and must be driven from a low impedance source like an op amp. Reversal of output sense can be obtained by grounding pin 7 of the LM163 and driving pin 5.

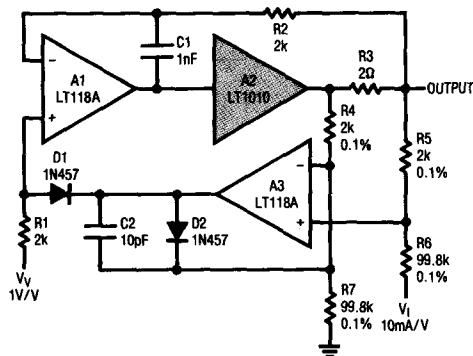


Output resistances of several megohms can be obtained with both circuits. This is impressive considering the

$\pm 150\text{mA}$ output capability. High frequency output characteristics will depend on the bandwidth and slew rate of the amplifiers. Both these circuits have an equivalent output capacitance of about 30nF.

Voltage/Current Regulator

This circuit regulates the output voltage at V_V until the load current reaches a value programmed by V_I . For heavier loads, it is a precision current regulator.



2

With output currents below the current limit, the current regulator is disconnected from the loop by D1, with D2 keeping its output out of saturation. This output clamp enables the current regulator to get control of the output current from the buffer current limit within a microsecond for an instantaneous short.

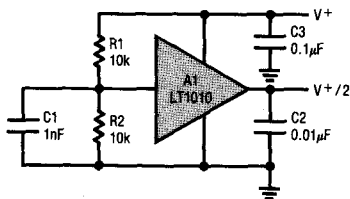
In the voltage regulation mode, A1 and A2 act as a fast voltage follower using the capacitive load isolation technique described earlier. Load transient recovery as well as capacitive load stability are determined by C1. Recovery from short circuit is clean.

Bi-directional current limit can be obtained by adding another op amp connected as a complement to A3.

APPLICATIONS INFORMATION

Supply Splitter

Dual supply op amps and comparators can be operated from a single supply by creating an artificial ground at half the supply voltage. The supply splitter shown here can source or sink 150mA.



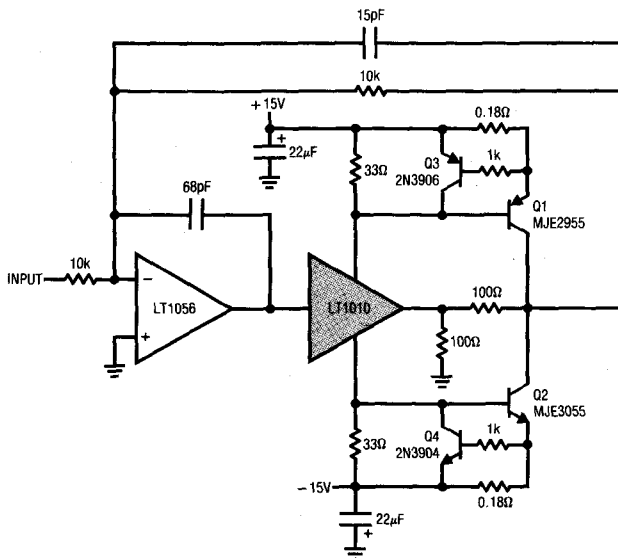
The output capacitor, C2, can be made as large as necessary to absorb current transients. An input capacitor is

also used on the buffer to avoid high frequency instability that can be caused by high source impedance.

High Current Booster

The circuit below uses a discrete stage to get 3A output capacity. The configuration shown provides a clean, quick way to increase LT1010 output power. It is useful for high current loads, such as linear actuator coils in disk drives.

The 33Ω resistors sense the LT1010's supply current, with the grounded 100Ω resistor supplying a load for the LT1010. The voltage drop across the 33Ω resistors biases Q1 and Q2. Another 100Ω value closes a local feedback loop, stabilizing the output stage. Feedback to the LT1056 control amplifier is via the 10k value. Q3 and Q4, sensing across the 0.18Ω units, furnish current limiting at about 3.3A.



HEAT SINK OUTPUT TRANSISTORS

Wideband FET Input Stabilized Buffer

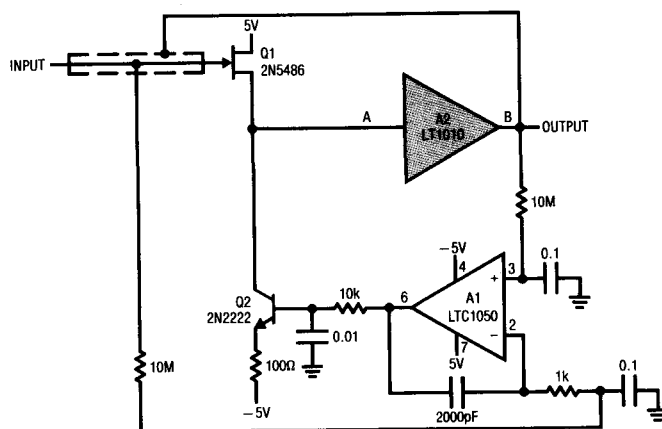
The figure below shows a highly stable unity gain buffer with good speed and high input impedance. Q1 and Q2 constitute a simple, high speed FET input buffer. Q1 functions as a source follower, with the Q2 current source load setting the drain-source channel current. The LT1010 buffer provides output drive capability for cables or whatever load is required. Normally, this open loop configuration would be quite drifty because there is no dc feedback. The LTC1050 contributes this function to stabilize the circuit. It does this by comparing the filtered circuit output to a similarly filtered version of the input signal. The amplified difference between these signals is used to set Q2's bias, and hence Q1's channel current. This forces Q1's V_{GS} to whatever voltage is required to match the circuit's input and output potentials. The 2000pF capacitor at A1 provides stable loop compensation. The RC network in A1's output prevents it from seeing high speed edges coupled through Q2's collector-base junction. A2's output is also fed back to the shield around Q1's gate lead, bootstrapping the circuit's effective input capacitance down to less than 1pF.

Gain Trimmable Wideband FET Amplifier

A potential difficulty with the previous circuit is that the gain is not quite unity. The figure labelled (A) on the next page maintains high speed and low bias while achieving a true unity gain transfer function.

This circuit is somewhat similar, except that the Q2-Q3 stage takes gain. A2 dc stabilizes the input-output path, and A1 provides drive capability. Feedback is to Q2's emitter from A1's output. The 1k adjustment allows the gain to be precisely set to unity. With the LT1010 output stage slew and full power bandwidth (1Vp-p) are 100V/ μ s and 10MHz, respectively. -3dB bandwidth exceeds 35MHz. At A = 10 (e.g., 1k adjustment set at 50 Ω) full power bandwidth stays at 10MHz while the -3dB point falls to 22MHz.

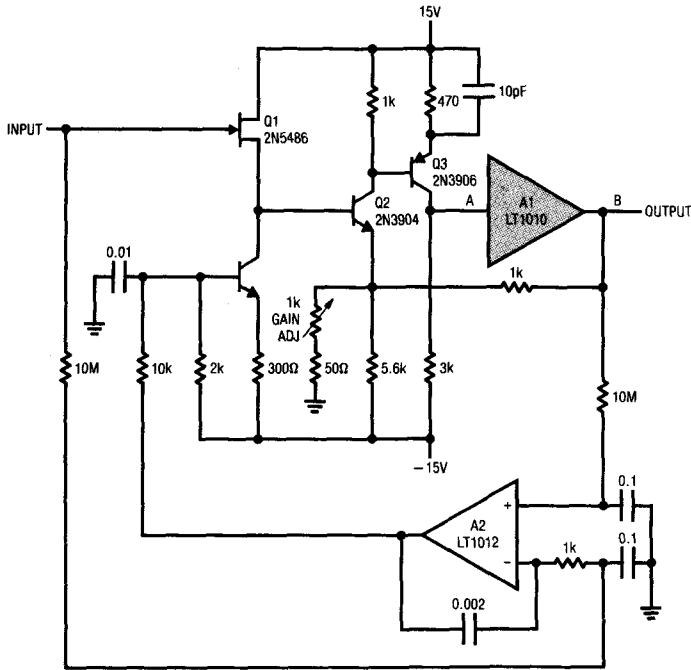
With the optional discrete stage, slew exceeds 1000V/ μ s and full power bandwidth (1Vp-p) is 18MHz. -3dB bandwidth is 58MHz. At A = 10, full power is available to 10MHz, with the -3dB point at 36MHz.



LT1010

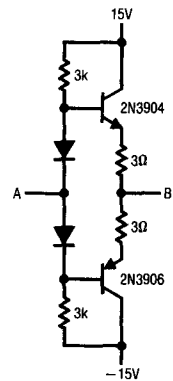
Figures A and B show response with both output stages. The LT1010 is used in Figure A (Trace A= input, Trace B= output). Figure B uses the discrete stage and is slightly

faster. Either stage provides more than adequate performance for driving video cable or data converters, and the LT1012 maintains dc stability under all conditions.



(A)

Gain Trimmable Wideband FET Amplifier



(B)

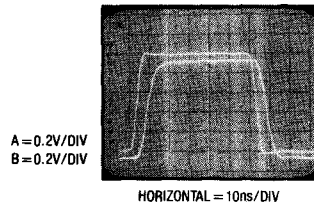
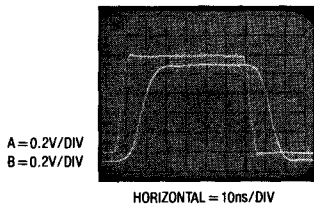


Figure A. Waveforms Using LT1010

Figure B. Waveforms Using Discrete Stage

DEFINITION OF TERMS

Output Offset Voltage: The output voltage measured with reference to the input.

Input Bias Current: The current out of the input terminal.

Large Signal Voltage Gain: The ratio of the output voltage change to the input voltage change over the specified input voltage range.*

Output Resistance: The ratio of the change in output voltage to the change in load current producing it.*

Output Saturation Voltage: The voltage between the output and the supply rail at the limit of the output swing toward that rail.

Saturation Offset Voltage: The output saturation voltage with no load.

Saturation Resistance: The ratio of the change in output saturation voltage to the change in current producing it, going from no load to full load.*

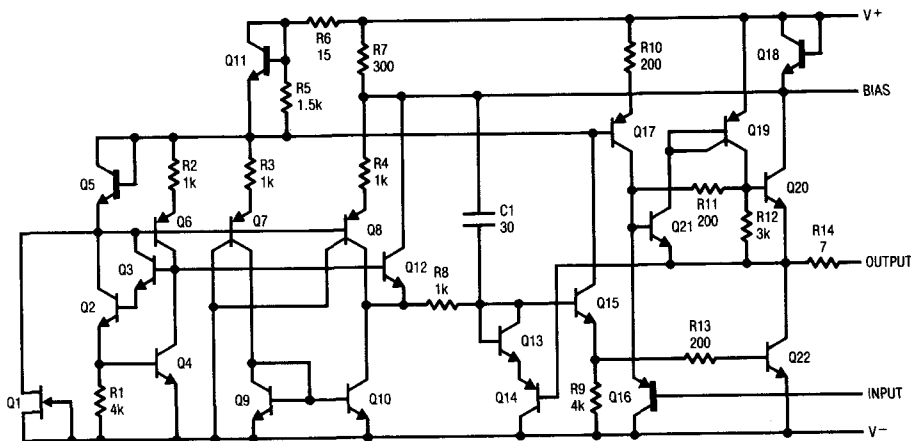
Slew Rate: The average time rate of change of output voltage over the specified output range with an input step between the specified limits.

Bias Terminal Voltage: The voltage between the bias terminal and V+.

Supply Current: The current at either supply terminal with no output loading.

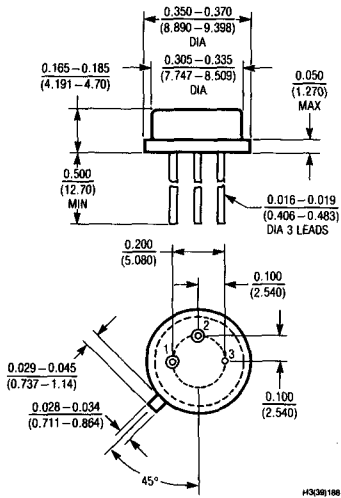
*Pulse measurements (~ 1ms) as required to minimize thermal effects.

SCHEMATIC DIAGRAM (excluding protection circuits)



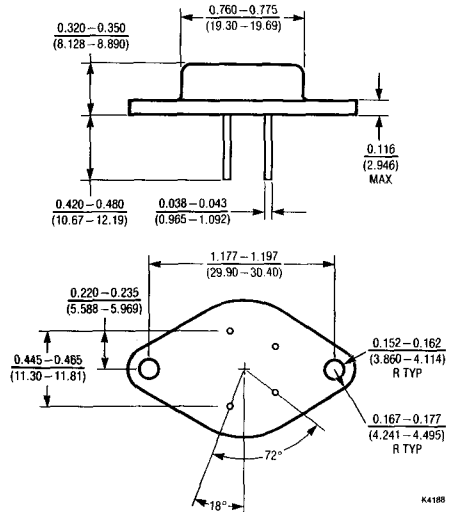
PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

H Package
4-Lead TO-39 Metal Can
(Kovar Base)



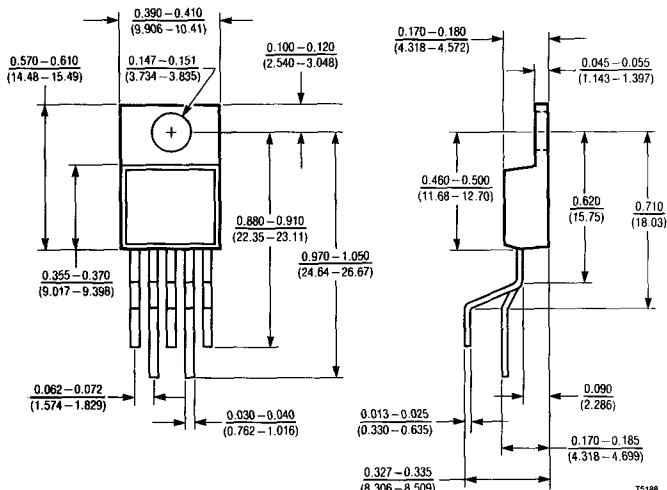
	T_{jmax}	θ_{jc}
LT1010M	150°C	40°C/W
LT1010C	125°C	40°C/W

K Package
4-Lead TO-3 Metal Can
(Steel)



	T_{jmax}	θ_{jc}
LT1010M	150°C	25°C/W
LT1010C	125°C	25°C/W

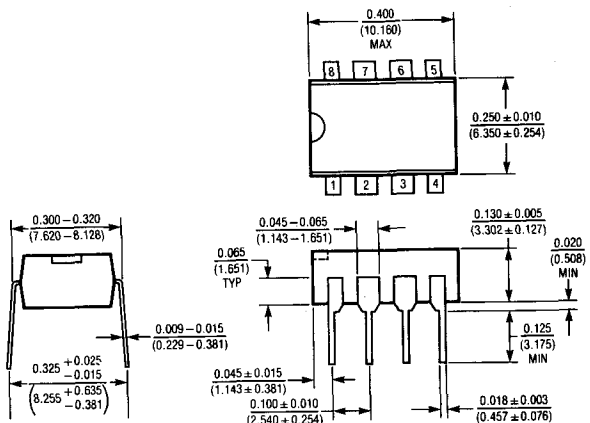
T Package
5-Lead TO-220 Plastic



	T_{jmax}	θ_{jc}
LT1010C	125°C	25°C/W

PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

**N Package
8-Lead Plastic DIP**



MS100

T _{max}	θ _{jc}
150°C	130°C/W

2

NOTES

FEATURES

- OP-07 Type Performance
 - at 1/8th of OP-07's Supply Current
 - at 1/20th of OP-07's Bias and Offset Currents
- *Guaranteed* Offset Voltage 25 μ V Max
- *Guaranteed* Bias Current 100pA Max
- *Guaranteed* Drift 0.6 μ V/ $^{\circ}$ C Max
- Low Noise, 0.1Hz to 10Hz 0.5 μ Vp-p
- *Guaranteed* Low Supply Current 500 μ A Max
- *Guaranteed* CMRR 114dB Min
- *Guaranteed* PSRR 114dB Min
- *Guaranteed* Operation @ ± 1.2 V Supplies

APPLICATIONS

- Replaces OP-07 While Saving Power
- Precision Instrumentation
- Charge Integrators
- Wide Dynamic Range Logarithmic Amplifiers
- Light Meters
- Low Frequency Active Filters
- Thermocouple Amplifiers

DESCRIPTION

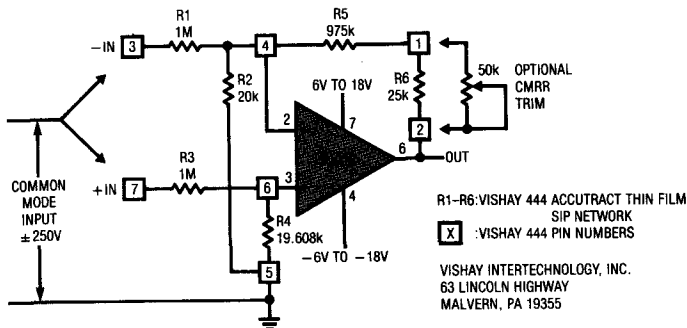
The LT1012 is an internally compensated universal precision operational amplifier which can be used in practically all precision applications. The LT1012 combines picoampere bias currents (which are maintained over the full -55° C to 125° C temperature range), microvolt offset voltage (and low drift with time and temperature), low voltage and current noise, and low power dissipation. The LT1012 achieves precision operation on two Ni-Cad batteries with 1mW of power dissipation. Extremely high common mode and power supply rejection ratios, practically unmeasurable warm-up drift, and the ability to deliver 5mA load current with a voltage gain of one million round out the LT1012's superb precision specifications.

The all around excellence of the LT1012 eliminates the necessity of the time consuming error analysis procedure of precision system design in many applications; the LT1012 can be stocked as the universal internally compensated precision op amp.

Protected by U.S. patents 4,575,685 and 4,775,884

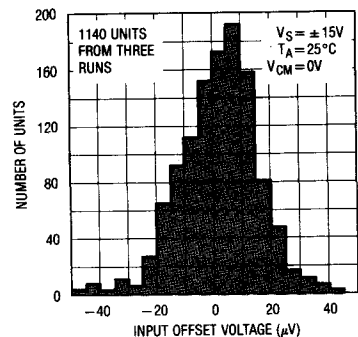
2

± 250 V Common Mode Range Instrumentation Amplifier ($A_V = 1$)



COMMON MODE REJECTION RATIO = 74dB (RESISTOR LIMITED)
 WITH OPTIONAL TRIM = 130dB
 OUTPUT OFFSET (TRIMMABLE TO ZERO) = 500 μ V
 OUTPUT OFFSET DRIFT = 10 μ V/ $^{\circ}$ C
 INPUT RESISTANCE = 1M

Typical Distribution of Input Offset Voltage



LT1012A/LT1012

ABSOLUTE MAXIMUM RATINGS

Supply Voltage..... $\pm 20V$
 Differential Input Current (Note 1)..... $\pm 10mA$
 Input Voltage..... $\pm 20V$
 Output Short Circuit Duration..... Indefinite
 Operating Temperature Range
 LT1012AM, LT1012M..... $-55^{\circ}C$ to $125^{\circ}C$
 LT1012AC, LT1012C,
 LT1012D, LT1012S8..... $0^{\circ}C$ to $70^{\circ}C$
 Storage Temperature Range
 All Devices..... $-65^{\circ}C$ to $150^{\circ}C$
 Lead Temperature (Soldering, 10 sec.)..... $300^{\circ}C$

PACKAGE/ORDER INFORMATION

<p>TOP VIEW H PACKAGE 8-LEAD TO-5 METAL CAN</p>	ORDER PART NUMBER
	LT1012AMH LT1012MH LT1012ACH LT1012CH LT1012DH
<p>TOP VIEW N PACKAGE 8-LEAD PLASTIC DIP</p>	ORDER PART NUMBER
	LT1012ACN8 LT1012CN8 LT1012DN8

<p>TOP VIEW SO PACKAGE 8-LEAD PLASTIC SOIC</p>	ORDER PART NUMBER
	LT1012S8
PART MARKING	1012

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V, V_{CM} = 0V, T_A = 25^{\circ}C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1012AM/AC		LT1012M		LT1012C		UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	(Note 2)	8	25	8	35	10	50	μV
			20	90	20	90	25	120	μV
	Long Term Input Offset Voltage Stability		0.3		0.3	0.3		$\mu V/month$	
I_{OS}	Input Offset Current	(Note 2)	15	100	15	100	20	150	pA
			25	150	25	150	30	200	pA
I_B	Input Bias Current	(Note 2)	± 25	± 100	± 25	± 100	± 30	± 150	pA
			± 35	± 150	± 35	± 150	± 40	± 200	pA
e_n	Input Noise Voltage	$0.1Hz$ to $10Hz$	0.5		0.5		0.5		$\mu Vp-p$
e_n	Input Noise Voltage Density	$f_o = 10Hz$ (Note 3)	17	30	17	30	17	30	nV/\sqrt{Hz}
		$f_o = 1000Hz$ (Note 4)	14	22	14	22	14	22	nV/\sqrt{Hz}
i_n	Input Noise Current Density	$f_o = 10Hz$	20		20		20		fA/\sqrt{Hz}
A_{VOL}	Large Signal Voltage Gain	$V_{OUT} = \pm 12V, R_L \geq 10k\Omega$	300	2000	300	2000	200	2000	V/mV
		$V_{OUT} = \pm 10V, R_L \geq 2k\Omega$	300	1000	200	1000	200	1000	V/mV
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 13.5V$	114	132	114	132	110	132	dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 1.2V$ to $\pm 20V$	114	132	114	132	110	132	dB
	Input Voltage Range		± 13.5	± 14.0	± 13.5	± 14.0	± 13.5	± 14.0	V
V_{OUT}	Output Voltage Swing	$R_L = 10k\Omega$	± 13	± 14	± 13	± 14	± 13	± 14	V
			0.1	0.2	0.1	0.2	0.1	0.2	$V/\mu sec$
I_S	Supply Current	(Note 2)	370	500	380	—	380	—	μA
			380	600	380	600	380	600	μA

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V, V_{CM} = 0V, T_A = 25^\circ C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1012D			LT1012S8			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	(Note 2)		12 25	60 —		15 25	120 180	μV μV
	Long Term Input Offset Voltage Stability			0.3			0.4		$\mu V/month$
I_{OS}	Input Offset Current	(Note 2)		20 30	150 —		50 60	280 380	pA pA
	Input Bias Current	(Note 2)		± 30 ± 40	± 150 —		± 80 ± 120	± 300 ± 400	pA pA
e_n	Input Noise Voltage	0.1Hz to 10Hz		0.5		0.5			μV_{p-p}
e_n	Input Noise Voltage Density	$f_o = 10Hz$ (Note 4)		17	30		17	30	nV/\sqrt{Hz}
		$f_o = 1000Hz$ (Note 4)		14	22		14	22	nV/\sqrt{Hz}
i_n	Input Noise Current Density	$f_o = 10Hz$		20		20			fA/\sqrt{Hz}
A_{VOL}	Large Signal Voltage Gain	$V_{OUT} = \pm 12V, R_L \geq 10k\Omega$	200	2000		200	2000		V/mV
		$V_{OUT} = \pm 10V, R_L \geq 2k\Omega$	200	1000		120	1000		V/mV
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 13.5V$	110	132		110	132		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 1.2V$ to $\pm 20V$	110	132		110	132		dB
	Input Voltage Range		± 13.5	± 14.0		± 13.5	± 14.0		V
V_{OUT}	Output Voltage Swing	$R_L = 10k\Omega$	± 13	± 14		± 13	± 14		V
	Slew Rate		0.1	0.2		0.1	0.2		V/ μsec
I_S	Supply Current	(Note 2)		380	600		380	600	μA

2

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V, V_{CM} = 0V, -55^\circ C \leq T_A \leq 125^\circ C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1012AM			LT1012M			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	(Note 2)	●	30	60		30	180	μV
	Average Temperature Coefficient of Input Offset Voltage		●	40	180		40	250	$\mu V/^\circ C$
I_{OS}	Input Offset Current	(Note 2)	●	30	250		30	250	pA
	Average Temperature Coefficient of Input Offset Current		●	70	350		70	350	pA
I_B	Input Bias Current	(Note 2)	●	± 80	± 600		± 80	± 600	pA
	Average Temperature Coefficient of Input Bias Current		●	± 150	± 800		± 150	± 800	pA
A_{VOL}	Large Signal Voltage Gain	$V_{OUT} = \pm 12V, R_L \geq 10k\Omega$	●	200	1000		150	1000	V/mV
		$V_{OUT} = \pm 10V, R_L \geq 2k\Omega$	●	200	600		100	600	V/mV
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 13.5V$	●	110	128		108	128	dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 1.5V$ to $\pm 20V$	●	110	126		108	126	dB
	Input Voltage Range		●	± 13.5			± 13.5		V
V_{OUT}	Output Voltage Swing	$R_L = 10k\Omega$	●	± 13	± 14		± 13	± 14	V
	Supply Current		●	400	650		400	800	μA

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: Differential input voltages greater than 1V will cause excessive current to flow through the input protection diodes unless limiting resistance is used.

Note 2: These specifications apply for $V_{MIN} \leq V_S \leq \pm 20V$ and $-13.5V \leq V_{CM} \leq 13.5V$ (for $V_S = \pm 15V$). $V_{MIN} = \pm 1.2V$ at $25^\circ C$, $\pm 1.3V$ from $0^\circ C$ to $70^\circ C$, $\pm 1.5V$ from $-55^\circ C$ to $125^\circ C$.

Note 3: 10Hz noise voltage density is sample tested on every lot. Devices 100% tested at 10Hz are available on request.

Note 4: This parameter is tested on a sample basis only.

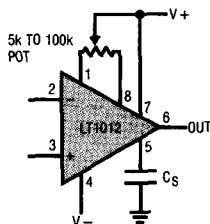
LT1012A/LT1012

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V, V_{CM} = 0V, 0^\circ C \leq T_A \leq 70^\circ C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1012AC			LT1012C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	(Note 2)	•	20	60	20	100	μV	
			•	30	160	30	200	μV	
	Average Temperature Coefficient of Input Offset Voltage	•	0.2	0.6	0.2	1.0	$\mu V/^\circ C$		
I_{OS}	Input Offset Current	(Note 2)	•	25	230	35	230	pA	
			•	40	300	45	300	pA	
	Average Temperature Coefficient of Input Offset Current	•	0.3	2.5	0.3	2.5	$pA/^\circ C$		
I_B	Input Bias Current	(Note 2)	•	± 35	± 230	± 35	± 230	pA	
			•	± 50	± 300	± 50	± 300	pA	
	Average Temperature Coefficient of Input Bias Current	•	0.3	2.5	0.3	2.5	$pA/^\circ C$		
A_{VOL}	Large Signal Voltage Gain	$V_{OUT} = \pm 12V, R_L \geq 10k\Omega$	•	200	1500	150	1500	V/mV	
		$V_{OUT} = \pm 10V, R_L \geq 2k\Omega$	•	200	1000	150	800	V/mV	
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 13.5V$	•	110	130	108	130	dB	
PSRR	Power Supply Rejection Ratio	$V_S = \pm 1.3V$ to $\pm 20V$	•	110	128	108	128	dB	
			•	± 13.5		± 13.5		V	
V_{OUT}	Output Voltage Swing	$R_L = 10k\Omega$	•	± 13	± 14	± 13	± 14	V	
I_S	Supply Current		•	400	600	400	800	μA	

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V, V_{CM} = 0V, 0^\circ C \leq T_A \leq 70^\circ C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1012D			LT1012S8			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	(Note 2)	•	25	140	30	200	μV	
			•	40	—	45	270	μV	
	Average Temperature Coefficient of Input Offset Voltage	•	0.3	1.7	0.3	1.8	$\mu V/^\circ C$		
I_{OS}	Input Offset Current	(Note 2)	•	35	380	60	380	pA	
			•	45	—	80	500	pA	
	Average Temperature Coefficient of Input Offset Current	•	0.35	4.0	0.4	4.0	$pA/^\circ C$		
I_B	Input Bias Current	(Note 2)	•	± 50	± 420	± 100	± 420	pA	
			•	± 65	—	± 150	± 550	pA	
	Average Temperature Coefficient of Input Bias Current	•	0.4	5.0	0.5	5.0	$pA/^\circ C$		
A_{VOL}	Large Signal Voltage Gain	$V_{OUT} = \pm 12V, R_L \geq 10k\Omega$	•	150	1500	150	1500	V/mV	
		$V_{OUT} = \pm 10V, R_L \geq 2k\Omega$	•	150	800	100	800	V/mV	
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 13.5V$	•	108	130	108	130	dB	
PSRR	Power Supply Rejection Ratio	$V_S = \pm 1.3V$ to $\pm 20V$	•	108	128	108	128	dB	
			•	± 13.5		± 13.5		V	
V_{OUT}	Output Voltage Swing	$R_L = 10k\Omega$	•	± 13	± 14	± 13	± 14	V	
I_S	Supply Current		•	400	800	400	800	μA	



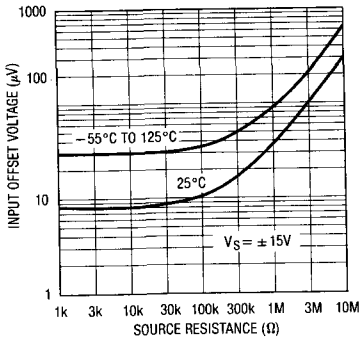
Optional Offset Nulling and Over-Compensation Circuits

Input offset voltage can be adjusted over a $\pm 800\mu V$ range with a 5k to 100k potentiometer.

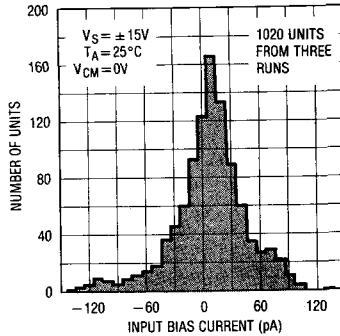
The LT1012 is internally compensated for unity gain stability. The over-compensation capacitor, C_S , can be used to improve capacitive load handling capability, to narrow noise bandwidth, or to stabilize circuits with gain in the feedback loop.

TYPICAL PERFORMANCE CHARACTERISTICS

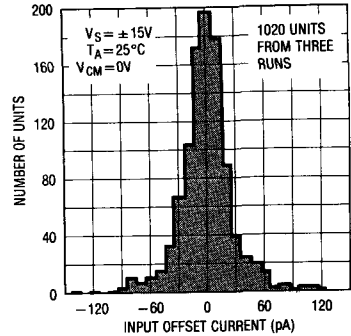
Offset Voltage vs Source Resistance (Balanced or Unbalanced)



Typical Distribution of Input Bias Current

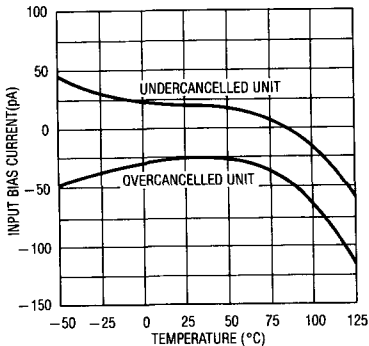


Typical Distribution of Input Offset Current

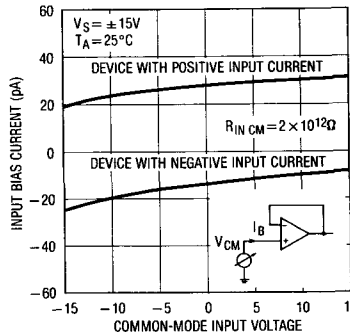


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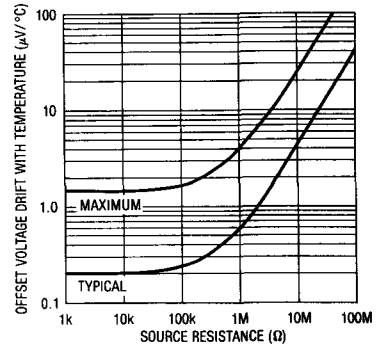
Input Bias Current vs Temperature



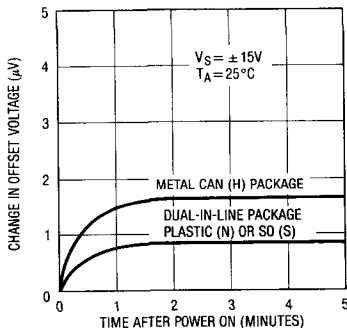
Input Bias Current Over Common Mode Range



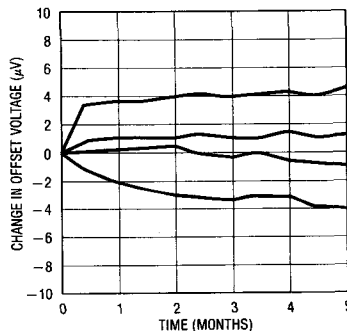
Offset Voltage Drift vs Source Resistance (Balanced or Unbalanced)



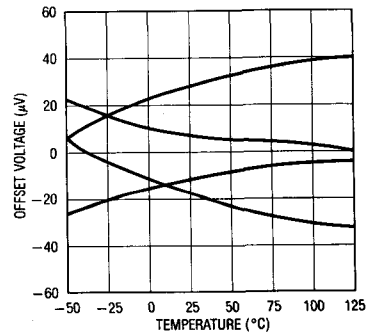
Warm-Up Drift



Long Term Stability of Four Representative Units

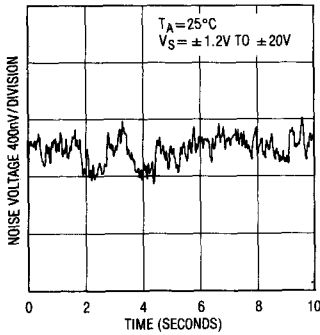


Offset Voltage Drift with Temperature of Four Representative Units

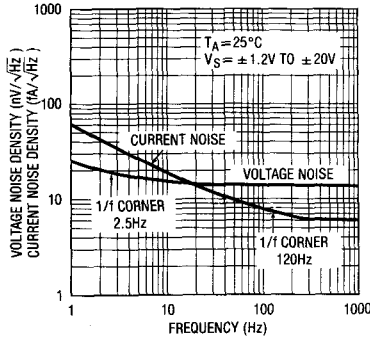


TYPICAL PERFORMANCE CHARACTERISTICS

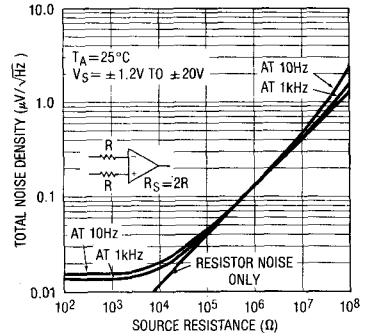
0.1Hz to 10Hz Noise



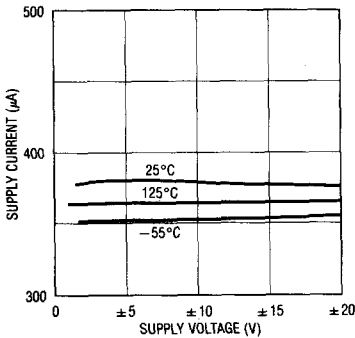
Noise Spectrum



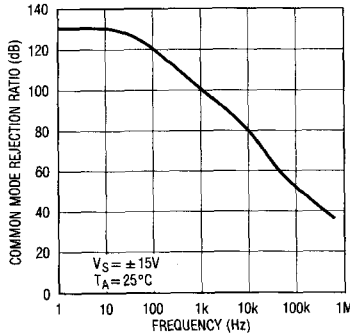
Total Noise vs Source Resistance



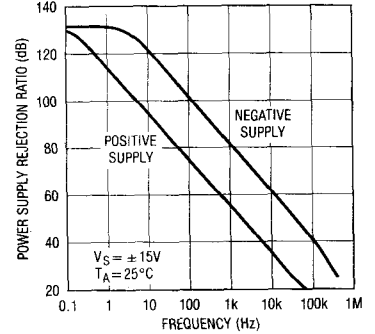
Supply Current vs Supply Voltage



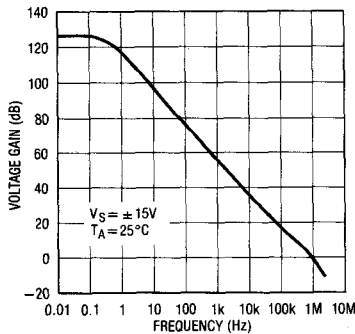
Common Mode Rejection vs Frequency



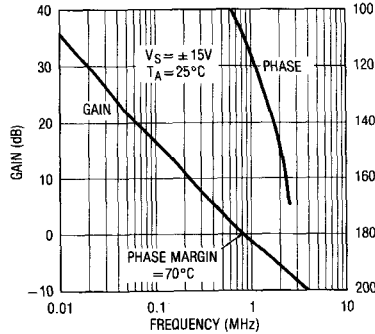
Power Supply Rejection vs Frequency



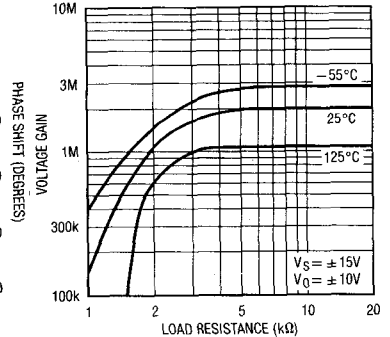
Voltage Gain vs Frequency



Gain, Phase Shift vs Frequency

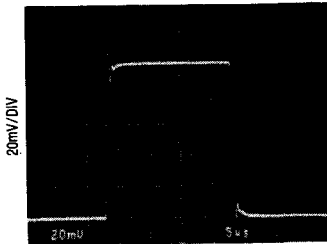


Voltage Gain vs Load Resistance



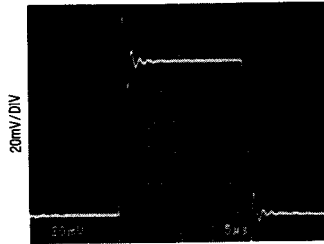
TYPICAL PERFORMANCE CHARACTERISTICS

Small Signal Transient Response



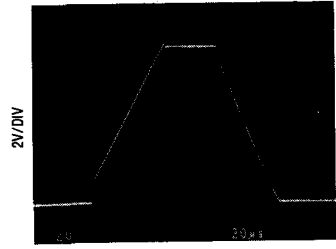
$A_V = +1$, $C_{LOAD} = 100pF$, $5\mu s/DIV$

Small Signal Transient Response



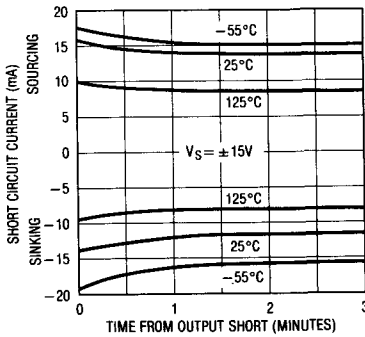
$A_V = +1$, $C_{LOAD} = 1000pF$, $5\mu s/DIV$

Large Signal Transient Response

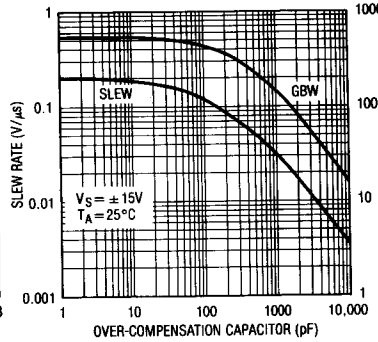


$A_V = +1$, $20\mu s/DIV$

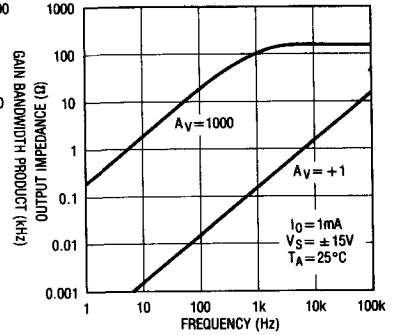
Output Short Circuit Current vs Time



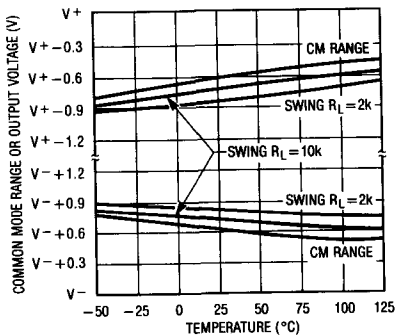
Slew Rate, Gain Bandwidth Product vs Over-Compensation Capacitor



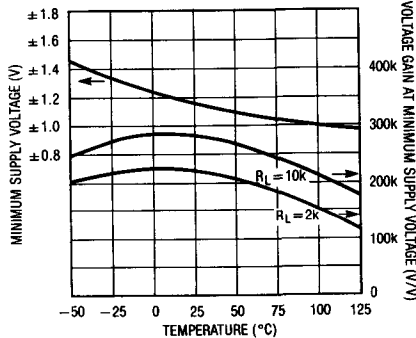
Closed Loop Output Impedance



Common Mode Range and Voltage Swing at Minimum Supply Voltage



Minimum Supply Voltage, Voltage Gain at V_{MIN}



APPLICATIONS INFORMATION

The LT1012 may be inserted directly into OP-07, LM11, 108A or 101A sockets with or without removal of external frequency compensation or nulling components. The LT1012 can also be used in 741, LF411, LF156 or OP-15 applications provided that the nulling circuitry is removed.

Although the OP-97 is a copy of the LT1012, the LT1012 directly replaces and upgrades OP-97 applications. The LT1012C and D have lower offset voltage and drift than the OP-97F. The LT1012A has lower supply current than the OP-97A/E. In addition, all LT1012 grades guarantee operation at $\pm 1.2V$ supplies.

Achieving Picoampere/Microvolt Performance

In order to realize the picoampere/microvolt level accuracy of the LT1012, proper care must be exercised. For example, leakage currents in circuitry external to the op amp can significantly degrade performance. High quality insulation should be used (e.g. Teflon, Kel-F); cleaning of all insulating surfaces to remove fluxes and other residues will probably be required. Surface coating may be necessary to provide a moisture barrier in high humidity environments.

Board leakage can be minimized by encircling the input circuitry with a guard ring operated at a potential close to that of the inputs: in inverting configurations the guard ring should be tied to ground, in non-inverting connections to the inverting input at pin 2. Guarding both sides of the printed circuit

board is required. Bulk leakage reduction depends on the guard ring width. Nanoampere level leakage into the offset trim terminals can affect offset voltage and drift with temperature.

Microvolt level error voltages can also be generated in the external circuitry. Thermocouple effects caused by temperature gradients across dissimilar metals at the contacts to the input terminals can exceed the inherent drift of the amplifier. Air currents over device leads should be minimized, package leads should be short, and the two input leads should be as close together as possible and maintained at the same temperature.

Noise Testing

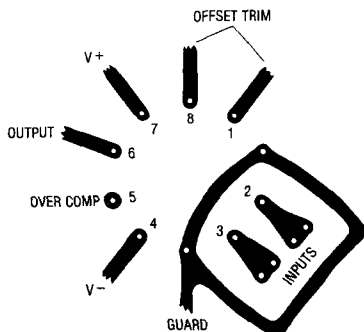
For application information on noise testing and calculations, please see the LT1008 data sheet.

Frequency Compensation

The LT1012 can be overcompensated to improve capacitive load handling capability or to narrow noise bandwidth. In many applications, the feedback loop around the amplifier has gain (e.g. logarithmic amplifiers); overcompensation can stabilize these circuits with a single capacitor.

The availability of the compensation terminal permits the use of feedforward frequency compensation to enhance slew rate. The voltage follower feedforward scheme bypasses the amplifier's gain stages and slews at nearly $10V/\mu s$.

The inputs of the LT1012 are protected with back-to-back diodes. Current limiting resistors are not used, because the leakage of these resistors would prevent the realization of picoampere level bias currents at elevated temperatures. In the voltage follower configuration, when the input is driven by a fast, large signal pulse ($> 1V$), the input protection diodes effectively short the output to the input during slewing, and a current, limited only by the output short circuit protection will flow through the diodes.

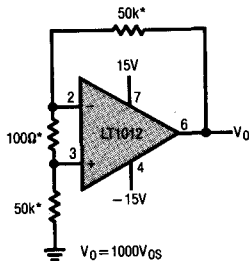


APPLICATIONS INFORMATION

The use of a feedback resistor, as shown in the voltage follower feedforward diagram, is recommended because this resistor keeps the current below the

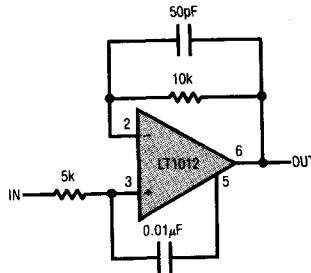
short circuit limit, resulting in faster recovery and settling of the output.

Test Circuit for Offset Voltage and its Drift with Temperature

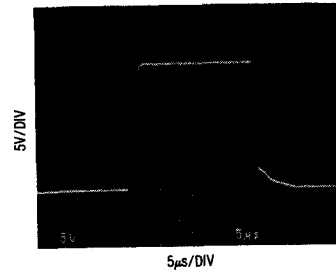


*RESISTORS MUST HAVE LOW THERMOELECTRIC POTENTIAL

Follower Feedforward Compensation



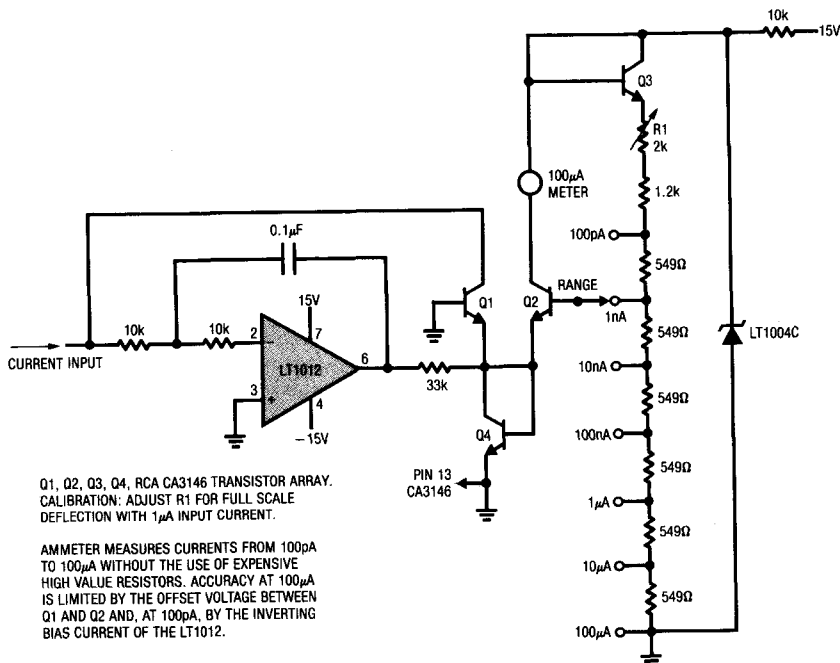
Pulse Response of Feedforward Compensation



2

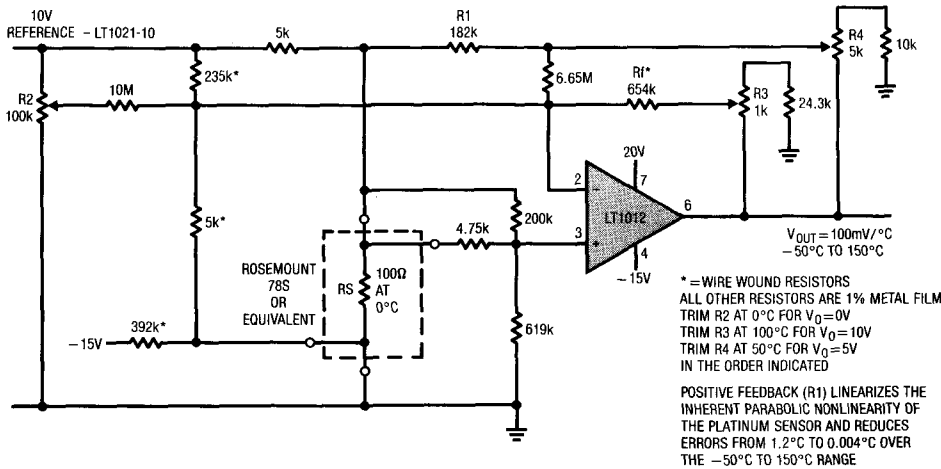
TYPICAL APPLICATIONS

Ammeter with Six Decade Range

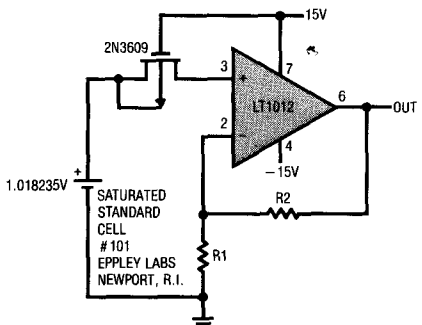


TYPICAL APPLICATIONS

Kelvin-Sensed Platinum Temperature Sensor Amplifier

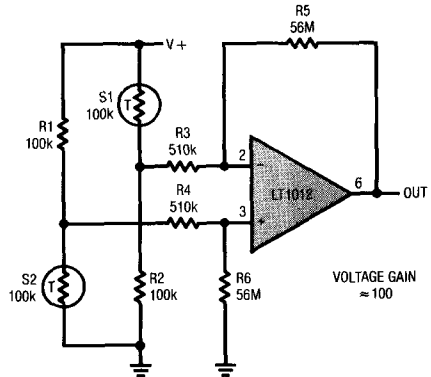


Saturated Standard Cell Amplifier

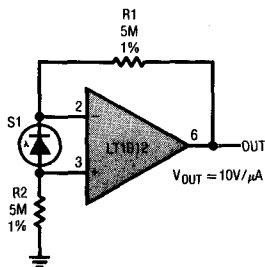


THE TYPICAL 30pA BIAS CURRENT OF THE LT1012 WILL DEGRADE THE STANDARD CELL BY ONLY 1ppm/YEAR. NOISE IS A FRACTION OF A ppm. UNPROTECTED GATE MOSFET ISOLATES STANDARD CELL ON POWER DOWN.

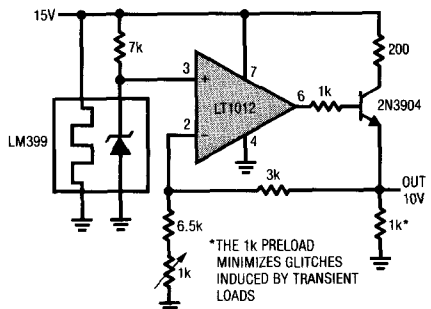
Amplifier for Bridge Transducers



Amplifier for Photodiode Sensor

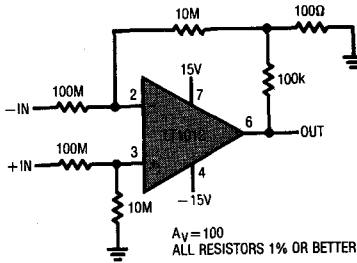


Buffered Reference for A to D Converters

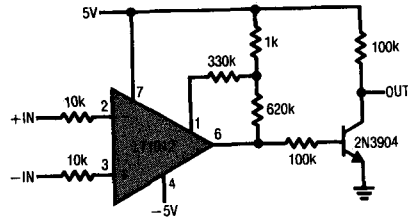


TYPICAL APPLICATIONS

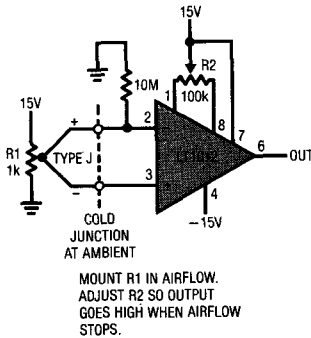
Instrumentation Amplifier with $\pm 100V$ Common Mode Range



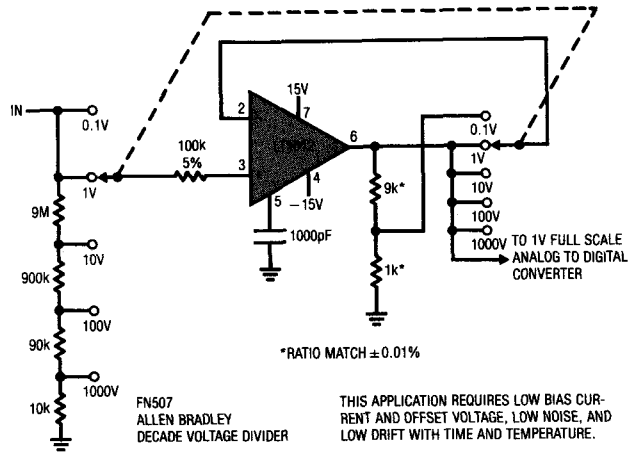
Low Power Comparator with $< 10\mu V$ Hysteresis



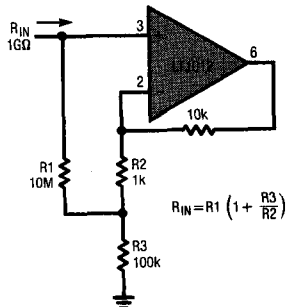
Air Flow Detector



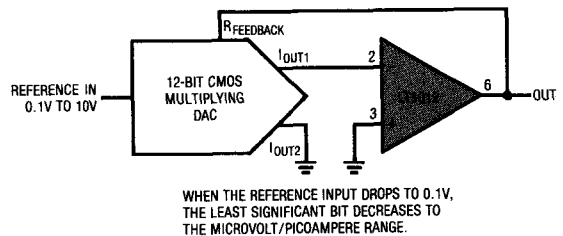
Input Amplifier for 4 1/2 Digit Voltmeter



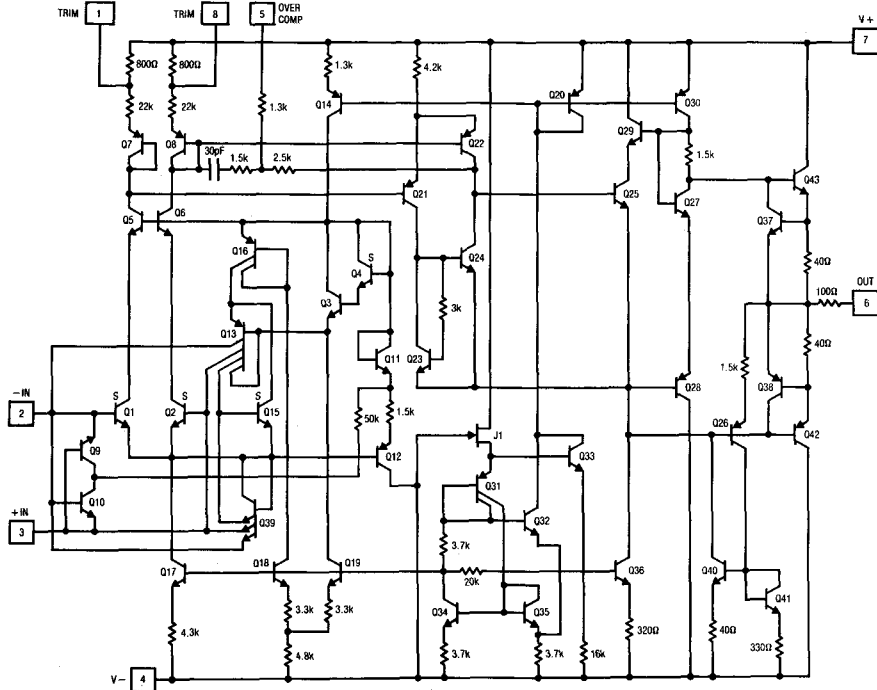
Resistor Multiplier



"No Trims" 12-Bit Multiplying DAC Output Amplifier

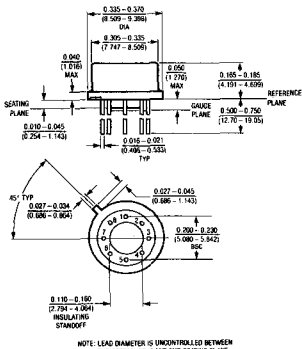


SCHEMATIC DIAGRAM



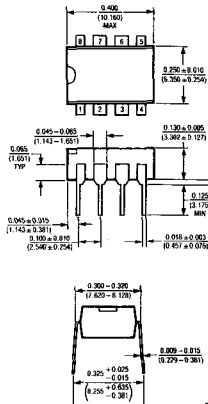
PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

H Package
8-Lead TO-5 Metal Can



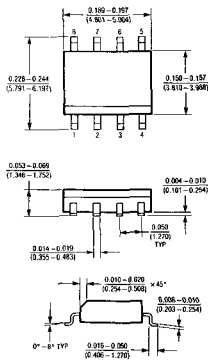
T _{JMAX} 150°C	θ _{JA} 150°C/W	θ _{JC} 45°C/W
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N Package
8-Lead Plastic DIP



T _{JMAX} 100°C	θ _{JA} 130°C/W
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SO Package
8-Lead Plastic SOIC



T _{JMAX} 100°C	θ _{JA} 170°C/W
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NOTES:
1. PBC MATERIAL: PLASTIC
2. LEAD MATERIAL: A-42, TIN PLATED

FEATURES

- Internally Compensated
- *Guaranteed* Offset Voltage 120 μ V Max.
- *Guaranteed* Bias Current 300pA Max.
380pA Max.
- *Guaranteed* Drift 1.8 μ V/ $^{\circ}$ C Max.
0.5 μ Vp-p
- Low Noise, 0.1Hz to 10Hz 600 μ A Max.
- *Guaranteed* Low Supply Current 110dB Min.
- *Guaranteed* CMRR 110dB Min.
- *Guaranteed* PSRR
- *Guaranteed* Voltage Gain with 5mA Load Current

DESCRIPTION

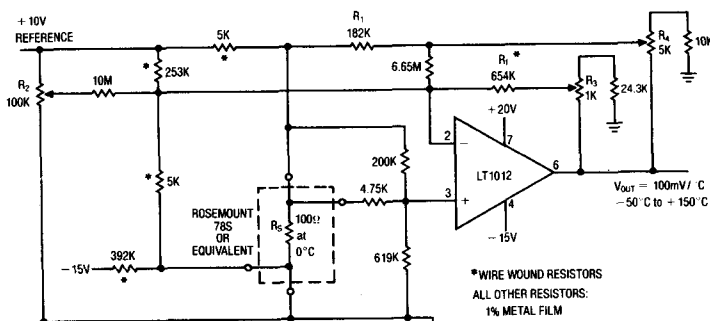
The LT1012 is an internally compensated universal precision operational amplifier which can be used in practically all precision applications. The LT1012 combines picoampere bias currents (which are maintained over the full 0 $^{\circ}$ C to 70 $^{\circ}$ C temperature range), microvolt offset voltage (and low drift with time and temperature), low voltage and current noise, and low power dissipation. Extremely high common-mode and power supply rejection ratios, practically unmeasurable warm-up drift, and the ability to deliver 5mA load current with a voltage gain of a million round out the LT1012's superb precision specifications.

The all around excellence of the LT1012 eliminates the necessity of the time consuming error analysis procedure of precision system design in many applications; the LT1012 can be stocked as the universal internally compensated precision op amp.

APPLICATIONS

- Precision Instrumentation
- Charge Integrators
- Wide Dynamic Range Logarithmic Amplifiers
- Light Meters
- Low Frequency Active Filters
- Standard Cell Buffers
- Thermocouple Amplifiers

Kelvin-Sensed Platinum Temperature Sensor Amplifier

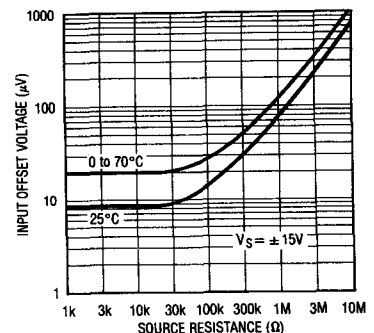


Positive feedback (R_1) linearizes the inherent parabolic nonlinearity of the platinum sensor and reduces errors from 1.2 $^{\circ}$ C to 0.004 $^{\circ}$ C over the -50 $^{\circ}$ C to 150 $^{\circ}$ C range.

* WIRE WOUND RESISTORS
 ALL OTHER RESISTORS:
 1% METAL FILM

Trim R_2 at 0 $^{\circ}$ C for $V_O = 0$ V
 R_3 at 100 $^{\circ}$ C for $V_O = 10$ V
 R_4 at 50 $^{\circ}$ C for $V_O = -5$ V
 in the order indicated

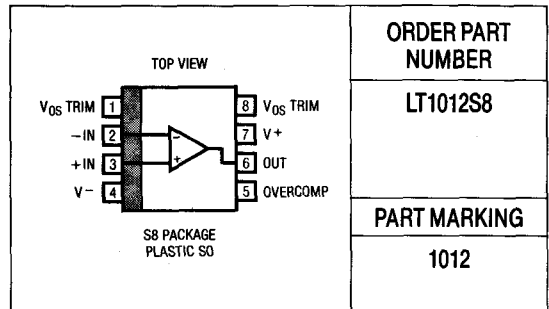
Offset Voltage vs Source Resistance (Balanced or Unbalanced)



ABSOLUTE MAXIMUM RATINGS

Supply Voltage $\pm 20V$
 Differential Input Current (Note 1) $\pm 10mA$
 Input Voltage $\pm 20V$
 Output Short Circuit Duration Indefinite
 Operating Temperature Range $0^{\circ}C$ to $70^{\circ}C$
 Storage Temperature Range $-65^{\circ}C$ to $150^{\circ}C$
 Lead Temperature (Soldering, 10 sec.) $300^{\circ}C$

PACKAGE/ORDER INFORMATION



ELECTRICAL CHARACTERISTICS $V_S = \pm 15V, V_{CM} = 0V, T_A = 25^{\circ}C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1012S8			UNITS
			MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	Note 2		10	120	μV
				25	180	μV
	Long Term Input Offset Voltage Stability			0.3		$\mu V/month$
I_{OS}	Input Offset Current	Note 2		50	280	pA
				60	380	pA
I_B	Input Bias Current	Note 2		± 80	± 300	pA
				± 120	± 400	pA
e_n	Input Noise Voltage	0.1Hz to 10Hz		0.5		$\mu Vp-p$
e_n	Input Noise Voltage Density	$f_o = 10Hz$ (Note 3)		17	30	nV/\sqrt{Hz}
		$f_o = 1000Hz$ (Note 3)		14	22	nV/\sqrt{Hz}
i_n	Input Noise Current Density	$f_o = 10Hz$		20		fA/\sqrt{Hz}
A_{VOL}	Large Signal Voltage Gain	$V_{OUT} = \pm 12V, R_L \geq 10k\Omega$	200	2000		V/mV
		$V_{OUT} = \pm 10V, R_L \geq 2k\Omega$	120	1000		V/mV
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm 13.5V$	110	132		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 2V$ to $\pm 20V$	110	132		dB
				± 13.5	± 14.0	
V_{OUT}	Output Voltage Swing	$R_L = 10k\Omega$	± 13	± 14		V
				0.1	0.2	
I_S	Supply Current	Note 2		380	600	μA

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V, V_{CM} = 0V, 0^\circ C \leq T_A \leq 70^\circ C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1012S8			UNITS
			MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	Note 2	●	20	200	μV
			●	30	270	μV
	Average Temperature Coefficient of Input Offset Voltage		●	0.2	1.8	$\mu V/^\circ C$
I_{OS}	Input Offset Current	Note 2	●	60	380	pA
			●	80	500	pA
	Average Temperature Coefficient of Input Offset Current		●	0.4	4	$pA/^\circ C$
I_B	Input Bias Current	Note 2	●	± 100	± 420	pA
			●	± 150	± 550	pA
	Average Temperature Coefficient of Input Bias Current		●	0.5	5	$pA/^\circ C$
A_{VOL}	Large Signal Voltage Gain	$V_{OUT} = \pm 12V, R_L \geq 10k\Omega$ $V_{OUT} = \pm 10V, R_L \geq 2k\Omega$	●	150	1500	V/mV
			●	100	800	V/mV
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm 13.5V$	●	108	130	dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 2.5V$ to $\pm 20V$	●	108	128	dB
			●	± 13.5		V
V_{OUT}	Output Voltage Swing	$R_L = 10k\Omega$	●	± 13	± 14	V
I_S	Supply Current		●		400 800	μA

2

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: Differential input voltages greater than 1V will cause excessive current to flow through the input protection diodes unless limiting resistance is used.

Note 2: These specifications apply for $\pm 2V \leq V_S \leq \pm 20V$ ($\pm 2.5V \leq V_S \leq \pm 20V$ over the temperature range) and $-13.5V \leq V_{CM} \leq 13.5V$ (for $V_S = \pm 15V$).

Note 3: This parameter is tested on a sample basis only.

NOTES

Quad Precision Op Amp (LT1014) Dual Precision Op Amp (LT1013)

FEATURES

- Single Supply Operation
 - Input Voltage Range Extends to Ground
 - Output Swings to Ground while Sinking Current
- Pin Compatible to 1458 and 324 with Precision Specs
- *Guaranteed* Offset Voltage 150 μ V Max.
- *Guaranteed* Low Drift 2 μ V/ $^{\circ}$ C Max.
- *Guaranteed* Offset Current 0.8nA Max.
- *Guaranteed* High Gain
 - 5mA Load Current 1.5 Million Min.
 - 17mA Load Current 0.8 Million Min.
- *Guaranteed* Low Supply Current 500 μ A Max.
- Low Voltage Noise, 0.1Hz to 10Hz 0.55 μ Vp-p
- Low Current Noise—Better than OP-07, 0.07 pA/ \sqrt Hz

APPLICATIONS

- Battery-Powered Precision Instrumentation
 - Strain Gauge Signal Conditioners
 - Thermocouple Amplifiers
 - Instrumentation Amplifiers
- 4mA–20mA Current Loop Transmitters
- Multiple Limit Threshold Detection
- Active Filters
- Multiple Gain Blocks

DESCRIPTION

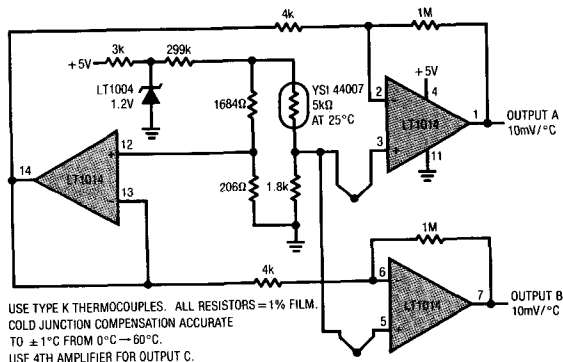
The LT1014 is the first precision quad operational amplifier which directly upgrades designs in the industry standard 14-pin DIP LM324/LM348/OP-11/4156 pin configuration. It is no longer necessary to compromise specifications, while saving board space and cost, as compared to single operational amplifiers.

The LT1014's low offset voltage of 50 μ V, drift of 0.3 μ V/ $^{\circ}$ C, offset current of 0.15nA, gain of 8 million, common-mode rejection of 117dB, and power supply rejection of 120dB qualify it as four truly precision operational amplifiers. Particularly important is the low offset voltage, since no offset null terminals are provided in the quad configuration. Although supply current is only 350 μ A per amplifier, a new output stage design sources and sinks in excess of 20mA of load current, while retaining high voltage gain.

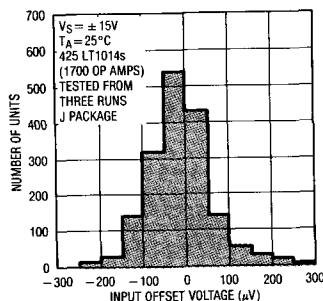
Similarly, the LT1013 is the first precision dual op amp in the 8-pin industry standard configuration, upgrading the performance of such popular devices as the MC1458/1558, LM158 and OP-221. The LT1013's specifications are similar to (even somewhat better than) the LT1014's.

Both the LT1013 and LT1014 can be operated off a single 5V power supply: input common-mode range includes ground; the output can also swing to within a few millivolts of ground. Crossover distortion, so apparent on previous single-supply designs, is eliminated. A full set of specifications is provided with \pm 15V and single 5V supplies.

3 Channel Thermocouple Thermometer



LT1014 Distribution of Offset Voltage



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±22V
Differential Input Voltage	±30V
Input Voltage	Equal to Positive Supply Voltage 5V Below Negative Supply Voltage
Output Short Circuit Duration	Indefinite
Operating Temperature Range	
LT1013AM/LT1013M/ LT1014AM/LT1014M	−55°C to 125°C
LT1013AC/1013C/1013D LT1014AC/1014C/1014D	0°C to 70°C
Storage Temperature Range	
All Grades	−65°C to 150°C
Lead Temperature (Soldering, 10 sec.)	300°C

PACKAGE/ORDER INFORMATION

<p>METAL CAN H PACKAGE</p>	ORDER PART NUMBER
	LT1013AMH LT1013MH LT1013ACH LT1013CH
<p>TOP VIEW HERMETIC DIP J8 PACKAGE PLASTIC DIP N8 PACKAGE</p>	LT1013AMJ8 LT1013MJ8 LT1013ACJ8 LT1013CJ8 LT1013CN8 LT1013DN8
	LT1014AMJ LT1014MJ LT1014ACJ LT1014CJ LT1014CN LT1014DN
<p>TOP VIEW HERMETIC DIP J14 PACKAGE PLASTIC DIP N14 PACKAGE</p>	

ELECTRICAL CHARACTERISTICS

$V_S = \pm 15V$, $V_{CM} = 0V$, $T_A = 25^\circ C$ unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS	LT1013AM LT1013AC LT1014AM LT1014AC			LT1013M/LT1013C LT1013DN8 LT1014M/LT1014C LT1014DN			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	LT1013	—	40	150	—	60	300	μV
		LT1014	—	50	180	—	60	300	μV
		LT1013DN8/LT1014DN	—	—	—	—	200	800	μV
	Long Term Input Offset Voltage Stability		—	0.4	—	—	0.5	—	$\mu V/Mo.$
I_{OS}	Input Offset Current		—	0.15	0.8	—	0.2	1.5	nA
I_B	Input Bias Current		—	12	20	—	15	30	nA
e_n	Input Noise Voltage	0.1Hz to 10Hz	—	0.55	—	—	0.55	—	$\mu Vp-p$
e_n	Input Noise Voltage Density	$f_0 = 10Hz$	—	24	—	—	24	—	nV/\sqrt{Hz}
		$f_0 = 1000Hz$	—	22	—	—	22	—	nV/\sqrt{Hz}
i_n	Input Noise Current Density	$f_0 = 10Hz$	—	0.07	—	—	0.07	—	pA/\sqrt{Hz}
	Input Resistance—Differential Common-Mode	(Note 1)	100	400	—	70	300	—	M Ω
			—	5	—	—	4	—	G Ω

ELECTRICAL CHARACTERISTICS

$V_S = \pm 15V$, $V_{CM} = 0V$, $T_A = 25^\circ C$ unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS	LT1013AM LT1013AC LT1014AM LT1014AC			LT1013M/LT1013C LT1013DN8 LT1014M/LT1014C LT1014DN			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
A_{VOL}	Large Signal Voltage Gain	$V_O = \pm 10V$, $R_L = 2k$ $V_O = \pm 10V$, $R_L = 600\Omega$	1.5 0.8	8.0 2.5	—	1.2 0.5	7.0 2.0	—	$V/\mu V$ $V/\mu V$
	Input Voltage Range		+13.5 -15.0	+13.8 -15.3	—	+13.5 -15.0	+13.8 -15.3	—	V V
CMRR	Common-Mode Rejection Ratio	$V_{CM} = +13.5V$, $-15.0V$	100	117	—	97	114	—	dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 2V$ to $\pm 18V$	103	120	—	100	117	—	dB
	Channel Separation	$V_O = \pm 10V$, $R_L = 2k$	123	140	—	120	137	—	dB
V_{OUT}	Output Voltage Swing	$R_L = 2k$	± 13	± 14	—	± 12.5	± 14	—	V
	Slew Rate		0.2	0.4	—	0.2	0.4	—	$V/\mu s$
I_S	Supply Current	Per Amplifier	—	0.35	0.50	—	0.35	0.55	mA

2

Note 1: This parameter is guaranteed by design and is not tested. Typical parameters are defined as the 60% yield of parameter distributions of individual amplifiers; i.e., out of 100 LT1014s (or 100 LT1013s) typically 240 op amps (or 120) will be better than the indicated specification.

ELECTRICAL CHARACTERISTICS

$V_S^+ = +5V$, $V_S^- = 0V$, $V_{OUT} = 1.4V$, $V_{CM} = 0V$, $T_A = 25^\circ C$ unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS	LT1013AM LT1013AC LT1014AM LT1014AC			LT1013M/LT1013C LT1013DN8 LT1014M/LT1014C LT1014DN			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	LT1013	—	60	250	—	90	450	μV
		LT1014	—	70	280	—	90	450	μV
		LT1013DN8/LT1014DN	—	—	—	—	250	950	μV
I_{OS}	Input Offset Current		—	0.2	1.3	—	0.3	2.0	nA
I_B	Input Bias Current		—	15	35	—	18	50	nA
A_{VOL}	Large Signal Voltage Gain	$V_O = 5mV$ to $4V$, $R_L = 500\Omega$	—	1.0	—	—	1.0	—	$V/\mu V$
	Input Voltage Range		+3.5 0	+3.8 -0.3	—	+3.5 0	+3.8 -0.3	—	V V
V_{OUT}	Output Voltage Swing	Output Low, No Load	—	15	25	—	15	25	mV
		Output Low, 600Ω to Ground	—	5	10	—	5	10	mV
		Output Low, $I_{SINK} = 1mA$	—	220	350	—	220	350	mV
		Output High, No Load	4.0	4.4	—	4.0	4.4	—	V
		Output High, 600Ω to Ground	3.4	4.0	—	3.4	4.0	—	V
I_S	Supply Current	Per Amplifier	—	0.31	0.45	—	0.32	0.50	mA

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $V_{CM} = 0V$, $-55^\circ C \leq T_A \leq 125^\circ C$ unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS	LT1013AM			LT1014AM			LT1013M/LT1014M			UNITS	
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
V_{OS}	Input Offset Voltage	$V_S = +5V$, $0V$; $V_0 = +1.4V$ $-55^\circ C \leq T_A \leq 100^\circ C$ $V_{CM} = 0.1V$, $T_A = 125^\circ C$ $V_{CM} = 0V$, $T_A = 125^\circ C$	●	—	80	300	—	90	350	—	110	550	μV
			●	—	80	450	—	90	480	—	100	750	μV
			●	—	120	450	—	150	480	—	200	750	μV
			●	—	250	900	—	300	960	—	400	1500	μV
	Input Offset Voltage Drift	(Note 2)	●	—	0.4	2.0	—	0.4	2.0	—	0.5	2.5	$\mu V/^\circ C$
I_{OS}	Input Offset Current	$V_S = +5V$, $0V$; $V_0 = +1.4V$	●	—	0.3	2.5	—	0.3	2.8	—	0.4	5.0	nA
			●	—	0.6	6.0	—	0.7	7.0	—	0.9	10.0	nA
I_B	Input Bias Current	$V_S = +5V$, $0V$; $V_0 = +1.4V$	●	—	15	30	—	15	30	—	18	45	nA
			●	—	20	80	—	25	90	—	28	120	nA
A_{VOL}	Large Signal Voltage Gain	$V_0 = \pm 10V$, $R_L = 2k$	●	0.5	2.0	—	0.4	2.0	—	0.25	2.0	—	$V/\mu V$
CMRR	Common-Mode Rejection	$V_{CM} = +13.0V$, $-14.9V$	●	97	114	—	96	114	—	94	113	—	dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 2V$ to $\pm 18V$	●	100	117	—	100	117	—	97	116	—	dB
V_{OUT}	Output Voltage Swing	$R_L = 2k$ $V_S = +5V$, $0V$; $R_L = 600\Omega$ to Ground Output Low Output High	●	± 12	± 13.8	—	± 12	± 13.8	—	± 11.5	± 13.8	—	V
			●	—	6	15	—	6	15	—	6	18	mV
			●	3.2	3.8	—	3.2	3.8	—	3.1	3.8	—	V
			●	—	0.38	0.60	—	0.38	0.60	—	0.38	0.7	mA
I_S	Supply Current Per Amplifier	$V_S = +5V$, $0V$; $V_0 = +1.4V$	●	—	0.34	0.55	—	0.34	0.55	—	0.34	0.65	mA
			●	—	0.38	0.60	—	0.38	0.60	—	0.38	0.7	mA

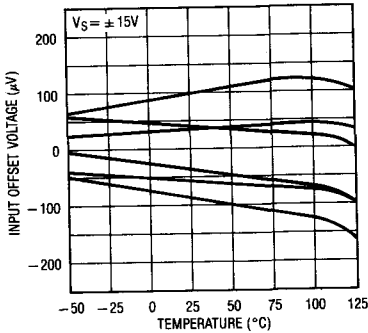
ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $V_{CM} = 0V$, $0^\circ C \leq T_A \leq 70^\circ C$ unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS	LT1013AC			LT1014AC			LT1013C/LT1013DN8 LT1014C/LT1014DN			UNITS	
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
V_{OS}	Input Offset Voltage	LT1013DN8, LT1014DN $V_S = +5V$, $0V$; $V_0 = 1.4V$ LT1013DN8, LT1014DN	●	—	55	240	—	65	270	—	80	400	μV
			●	—	—	—	—	—	—	—	230	1000	μV
			●	—	75	350	—	85	380	—	110	570	μV
			●	—	—	—	—	—	—	—	280	1200	μV
	Average Input Offset Voltage Drift	(Note 2) LT1013DN, LT1014DN	●	—	0.3	2.0	—	0.3	2.0	—	0.4	2.5	$\mu V/^\circ C$
			●	—	—	—	—	—	—	0.7	5.0	$\mu V/^\circ C$	
I_{OS}	Input Offset Current	$V_S = +5V$, $0V$; $V_0 = 1.4V$	●	—	0.2	1.5	—	0.2	1.7	—	0.3	2.8	nA
			●	—	0.4	3.5	—	0.4	4.0	—	0.5	6.0	nA
I_B	Input Bias Current	$V_S = +5V$, $0V$; $V_0 = 1.4V$	●	—	13	25	—	13	25	—	16	38	nA
			●	—	18	55	—	20	60	—	24	90	nA
A_{VOL}	Large Signal Voltage Gain	$V_0 = \pm 10V$, $R_L = 2k$	●	1.0	5.0	—	1.0	5.0	—	0.7	4.0	—	$V/\mu V$
CMRR	Common-Mode Rejection Ratio	$V_{CM} = +13.0V$, $-15.0V$	●	98	116	—	98	116	—	94	113	—	dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 2V$ to $\pm 18V$	●	101	119	—	101	119	—	97	116	—	dB
V_{OUT}	Output Voltage Swing	$R_L = 2k$ $V_S = +5V$, $0V$; $R_L = 600\Omega$ Output Low Output High	●	± 12.5	± 13.9	—	± 12.5	± 13.9	—	± 12.0	± 13.9	—	V
			●	—	6	13	—	6	13	—	6	13	mV
			●	3.3	3.9	—	3.3	3.9	—	3.2	3.9	—	V
			●	—	0.36	0.55	—	0.36	0.55	—	0.37	0.60	mA
I_S	Supply Current per Amplifier	$V_S = +5V$, $0V$; $V_0 = 1.4V$	●	—	0.32	0.50	—	0.32	0.50	—	0.34	0.55	mA
			●	—	0.36	0.55	—	0.36	0.55	—	0.37	0.60	mA

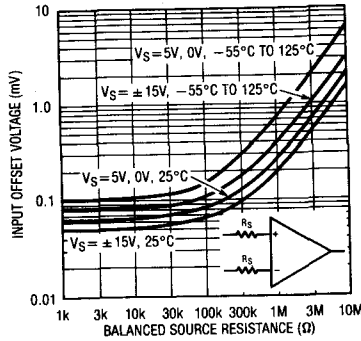
Note 2: This parameter is not 100% tested.
The ● denotes the specifications which apply over the full operating temperature range.

TYPICAL PERFORMANCE CHARACTERISTICS

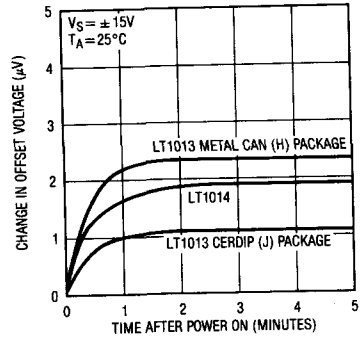
Offset Voltage Drift with Temperature of Representative Units



Offset Voltage vs Balanced Source Resistance

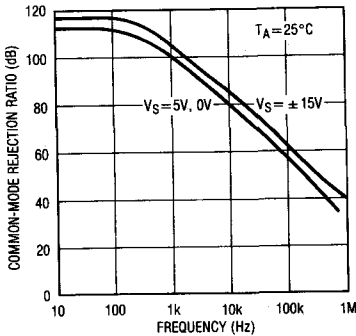


Warm-Up Drift

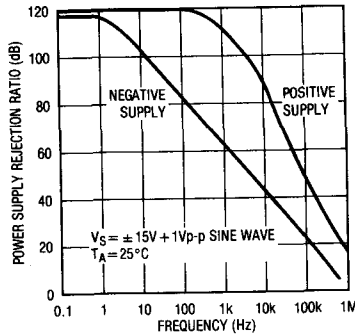


2

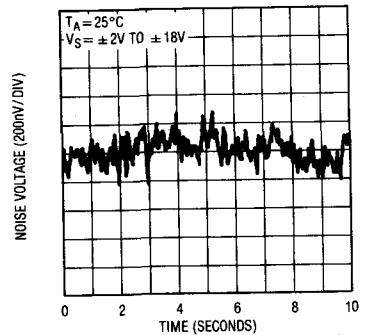
Common-Mode Rejection Ratio vs Frequency



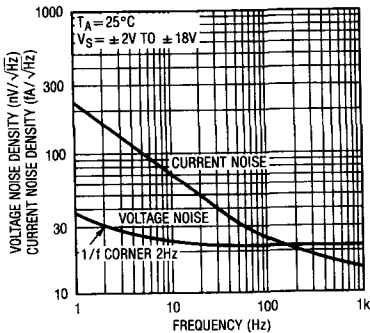
Power Supply Rejection Ratio vs Frequency



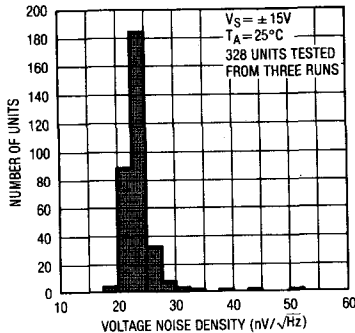
0.1Hz to 10Hz Noise



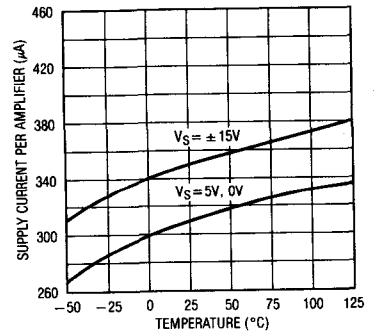
Noise Spectrum



10Hz Voltage Noise Distribution

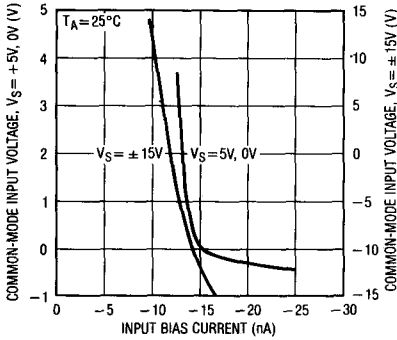


Supply Current vs Temperature

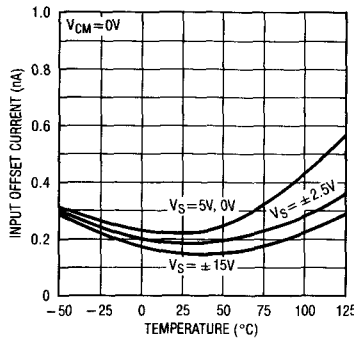


TYPICAL PERFORMANCE CHARACTERISTICS

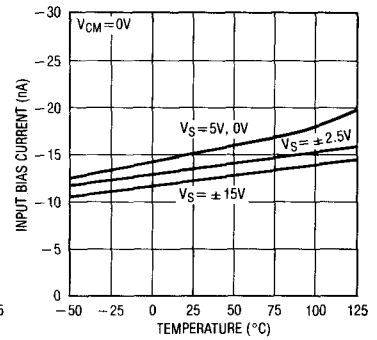
Input Bias Current vs Common-Mode Voltage



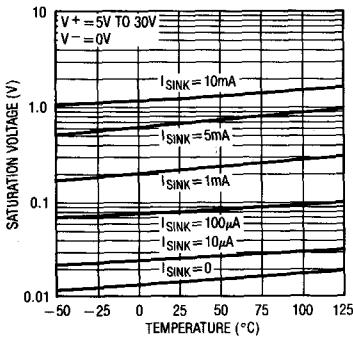
Input Offset Current vs Temperature



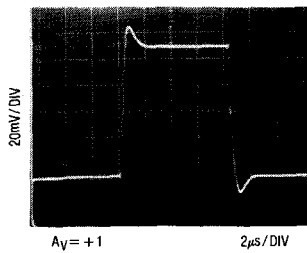
Input Bias Current vs Temperature



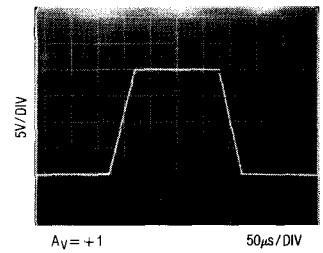
Output Saturation vs Sink Current vs Temperature



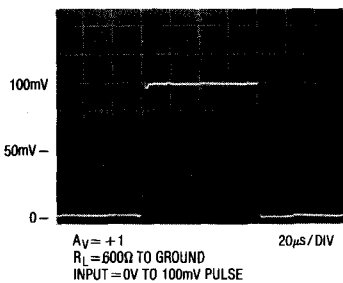
Small Signal Transient Response, VS = ±15V



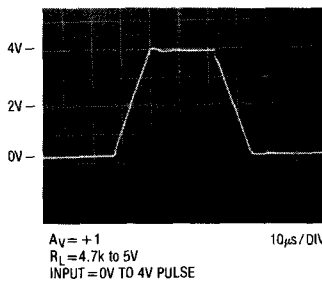
Large Signal Transient Response, VS = ±15V



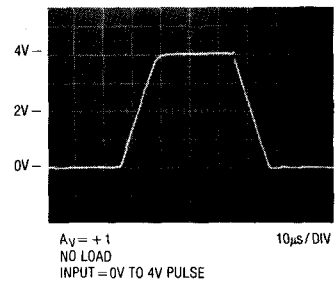
Small Signal Transient Response, VS = 5V, 0V



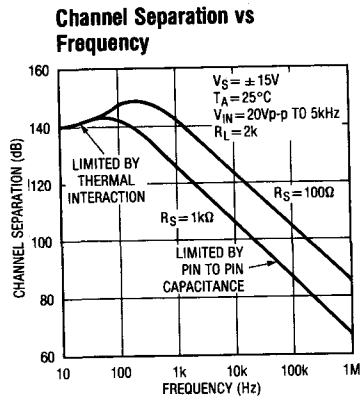
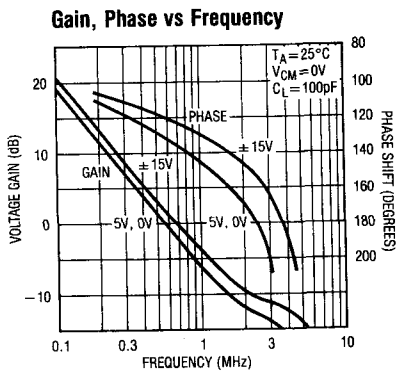
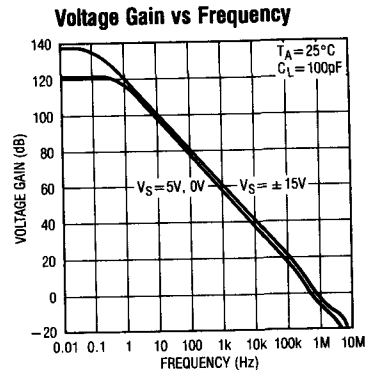
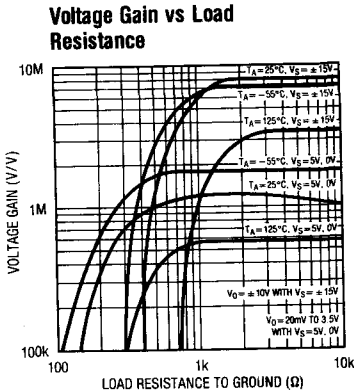
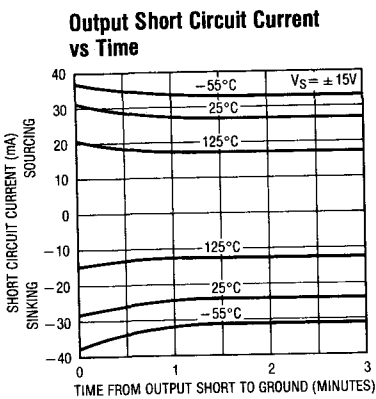
Large Signal Transient Response, VS = 5V, 0V



Large Signal Transient Response, VS = 5V, 0V



TYPICAL PERFORMANCE CHARACTERISTICS



2

APPLICATIONS INFORMATION

Single Supply Operation

The LT1013/1014 are fully specified for single supply operation, i.e., when the negative supply is 0V. Input common-mode range includes ground; the output swings within a few millivolts of ground. Single supply operation, however, can create special difficulties, both at the input and at the output. The LT1013/LT1014 have specific circuitry which addresses these problems.

At the input, the driving signal can fall below 0V—inadvertently or on a transient basis. If the input is more than

a few hundred millivolts below ground, two distinct problems can occur on previous single supply designs, such as the LM124, LM158, OP-20, OP-21, OP-220, OP-221, OP-420:

a) When the input is more than a diode drop below ground, unlimited current will flow from the substrate (V^- terminal) to the input. This can destroy the unit. On the LT1013/1014, the 400 Ω resistors, in series with the input (see schematic diagram), protect the devices even when the input is 5V below ground.

APPLICATIONS INFORMATION

(b) When the input is more than 400mV below ground (at 25°C), the input stage saturates (transistors Q3 and Q4) and phase reversal occurs at the output. This can cause lock-up in servo systems. Due to a unique phase reversal protection circuitry (Q21, Q22, Q27, Q28), the LT1013/1014's outputs do not reverse, as illustrated below, even when the inputs are at -1.5V.

There is one circumstance, however, under which the phase reversal protection circuitry does not function: when the other op amp on the LT1013, or one specific amplifier of the other three on the LT1014, is driven hard into negative saturation at the output.

- A when D's output is in negative saturation. B's and C's outputs have no effect.
- B when C's output is in negative saturation. A's and D's outputs have no effect.
- C when B's output is in negative saturation. A's and D's outputs have no effect.
- D when A's output is in negative saturation. B's and C's outputs have no effect.

At the output, the aforementioned single supply designs either cannot swing to within 600mV of ground (OP-20) or cannot sink more than a few microamperes while swinging to ground (LM124, LM158). The LT1013/1014's all-NPN output stage maintains its low output resistance and high gain characteristics until the output is saturated.

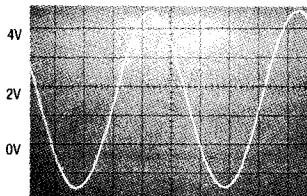
In dual supply operations, the output stage is crossover distortion-free.

Comparator Applications

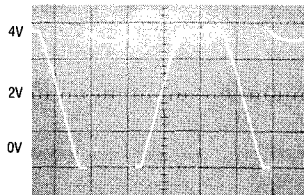
The single supply operation of the LT1013/1014 lends itself to its use as a precision comparator with TTL compatible output:

In systems using both op amps and comparators, the LT1013/1014 can perform multiple duties; for example, on the LT1014, two of devices can be used as op amps and the other two as comparators.

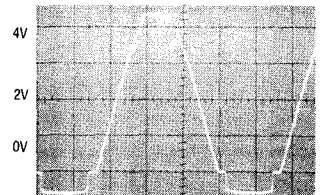
Voltage Follower with Input Exceeding the Negative Common-Mode Range



6Vp-p INPUT, -1.5V TO 4.5V

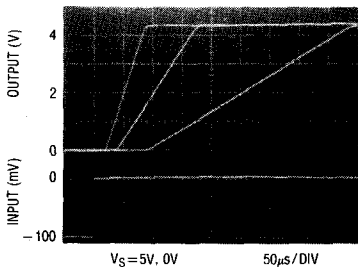


LM324, LM358, OP-20
EXHIBIT OUTPUT PHASE
REVERSAL

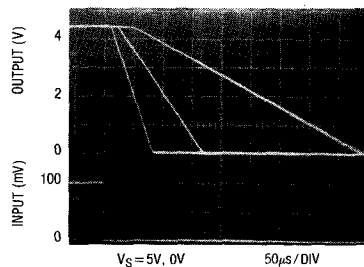


LT1013/LT1014
NO PHASE REVERSAL

Comparator Rise Response Time 10mV, 5mV, 2mV Overdrives



Comparator Fall Response Time to 10mV, 5mV, 2mV Overdrives



APPLICATIONS INFORMATION

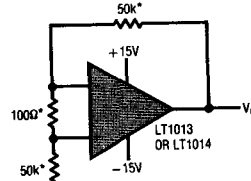
Low Supply Operation

The minimum supply voltage for proper operation of the LT1013/1014 is 3.4V (three Ni-Cad batteries). Typical supply current at this voltage is 290 μ A, therefore power dissipation is only one milliwatt per amplifier.

Noise Testing

For application information on noise testing and calculations, please see the LT1007 or LT1008 data sheet.

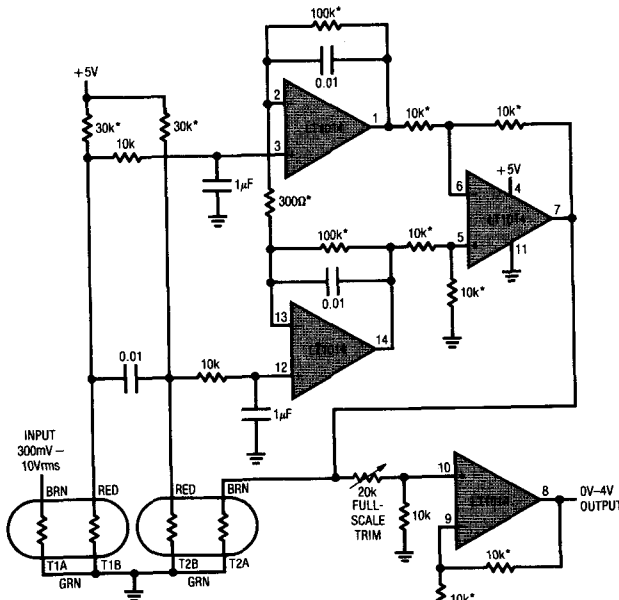
Test Circuit for Offset Voltage and Offset Drift with Temperature



*RESISTORS MUST HAVE LOW THERMOELECTRIC POTENTIAL.
 **THIS CIRCUIT IS ALSO USED AS THE BURN-IN CONFIGURATION, WITH SUPPLY VOLTAGES INCREASED TO ± 20 V.
 $V_0 = 1000V_{OS}$

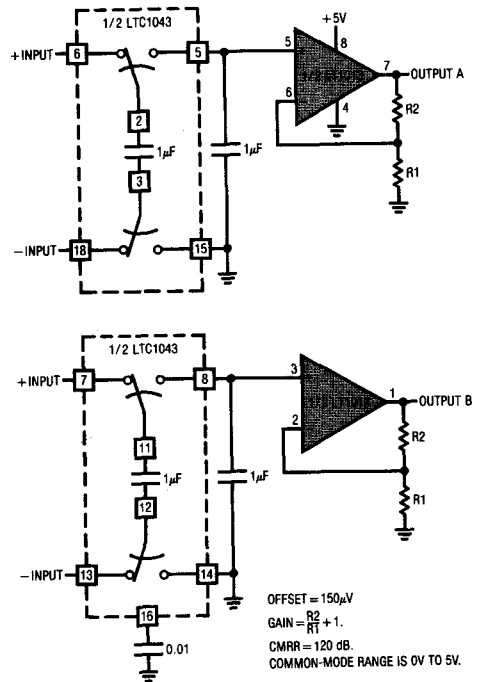
TYPICAL APPLICATIONS

50MHz Thermal rms to DC Converter



2% ACCURACY, DC-50MHz.
 100:1 CREST FACTOR CAPABILITY.
 *0.1% RESISTOR.
 T1-T2 = YELLOW SPRINGS INST. CO. THERMISTOR COMPOSITE # 44018.
 ENCLOSE T1 AND T2 IN STYROFOAM.
 7.5mW DISSIPATION.

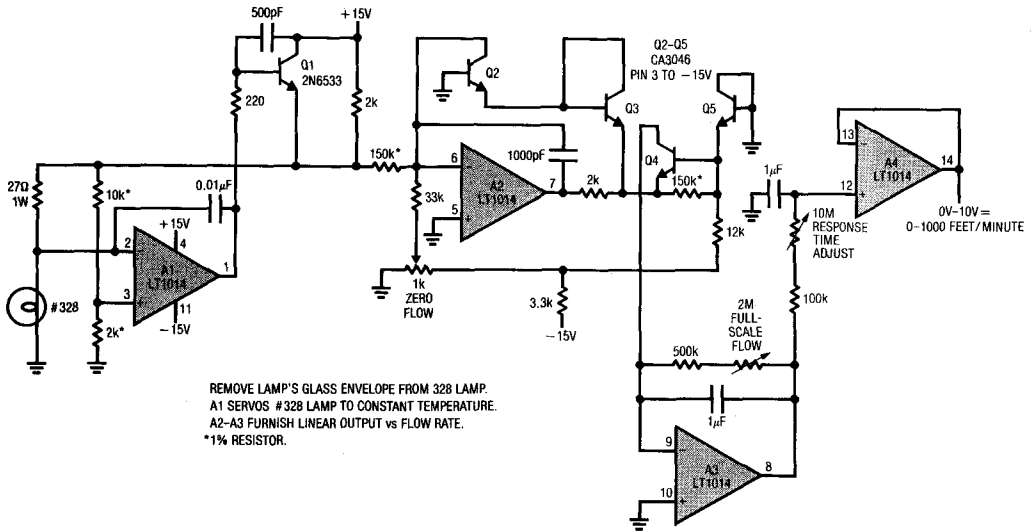
5V Single Supply Dual Instrumentation Amplifier



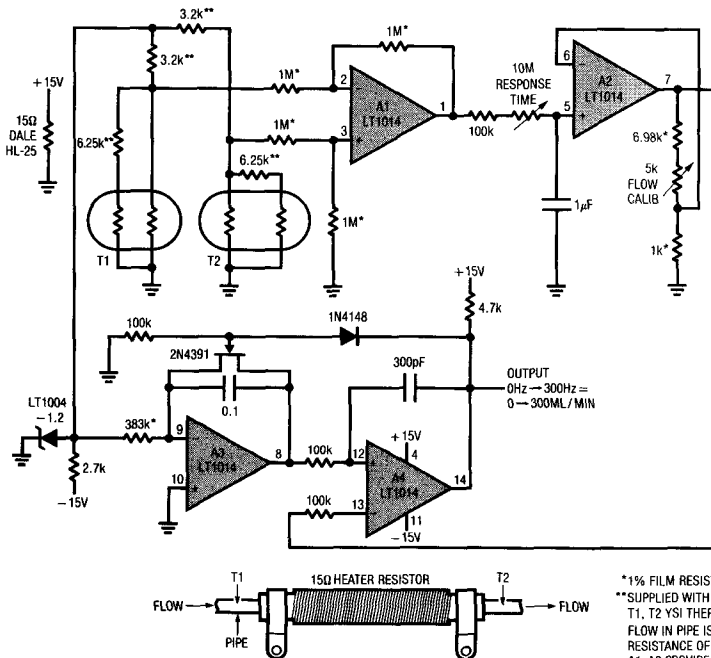
OFFSET = 150 μ V
 GAIN = $\frac{R_2}{R_1} + 1$.
 CMRR = 120 dB.
 COMMON-MODE RANGE IS 0V TO 5V.

TYPICAL APPLICATIONS

Hot Wire Anemometer

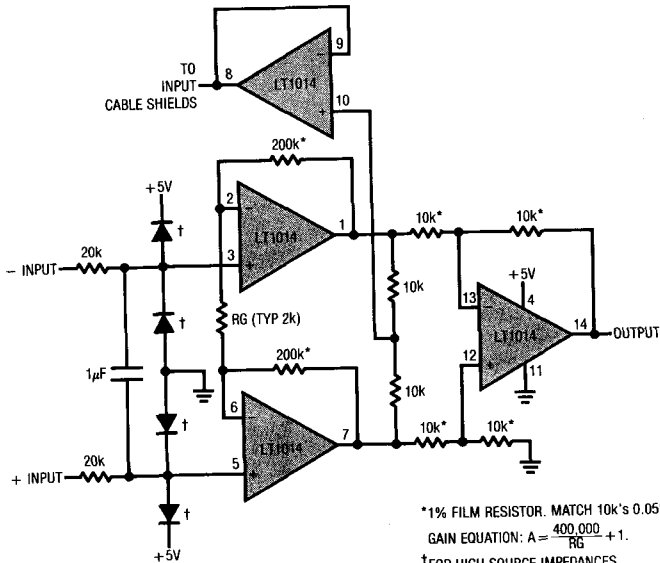


Liquid Flowmeter



TYPICAL APPLICATIONS

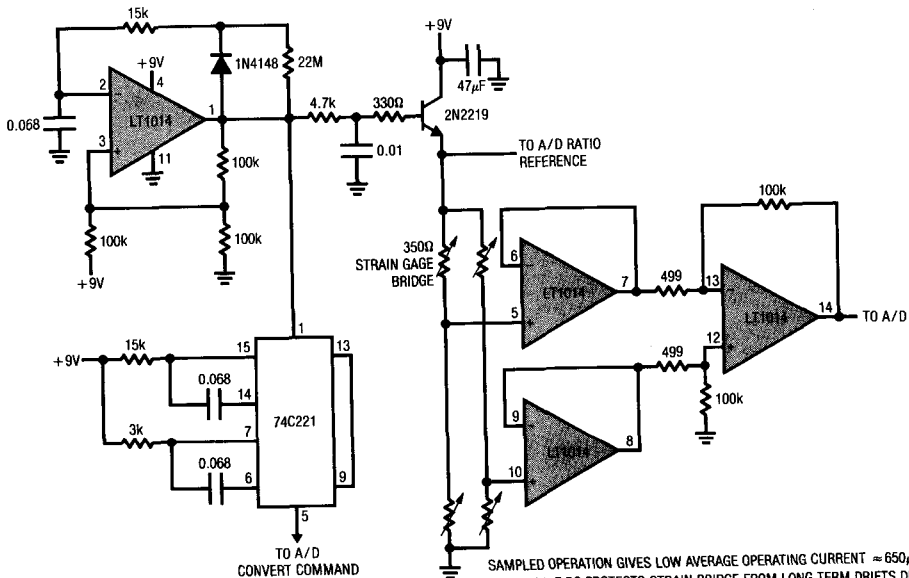
5V Powered Precision Instrumentation Amplifier



*1% FILM RESISTOR. MATCH 10k's 0.05%
 GAIN EQUATION: $A = \frac{400,000}{R_G} + 1$.
 †FOR HIGH SOURCE IMPEDANCES, USE 2N2222 AS DIODES.

2

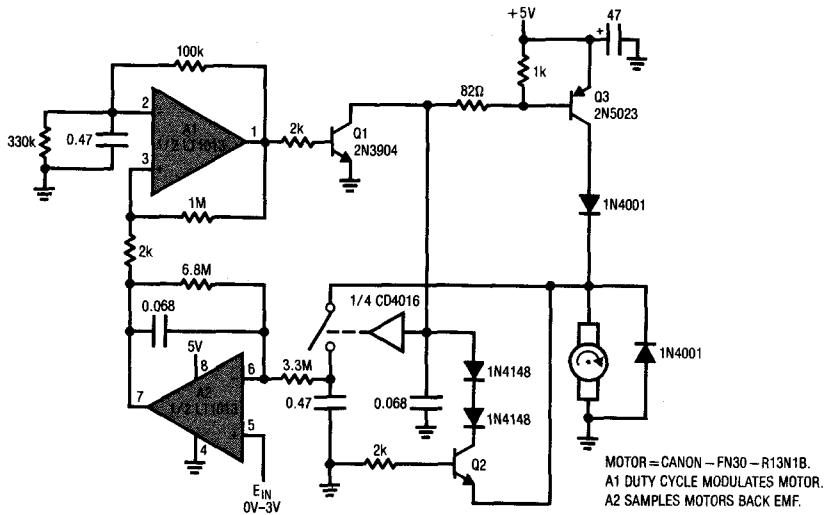
9V Battery Powered Strain Gage Signal Conditioner



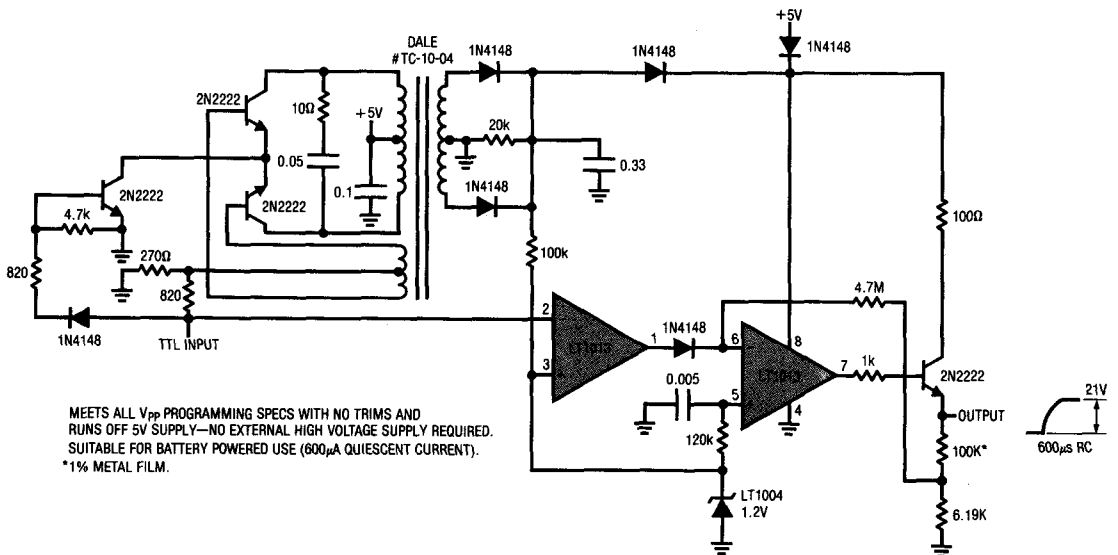
SAMPLED OPERATION GIVES LOW AVERAGE OPERATING CURRENT $\approx 650\mu A$.
 4.7k-0.01µF RC PROTECTS STRAIN BRIDGE FROM LONG TERM DRIFTS DUE TO HIGH $\Delta V/\Delta T$ STEPS.

TYPICAL APPLICATIONS

**5V Powered Motor Speed Controller
No Tachometer Required**

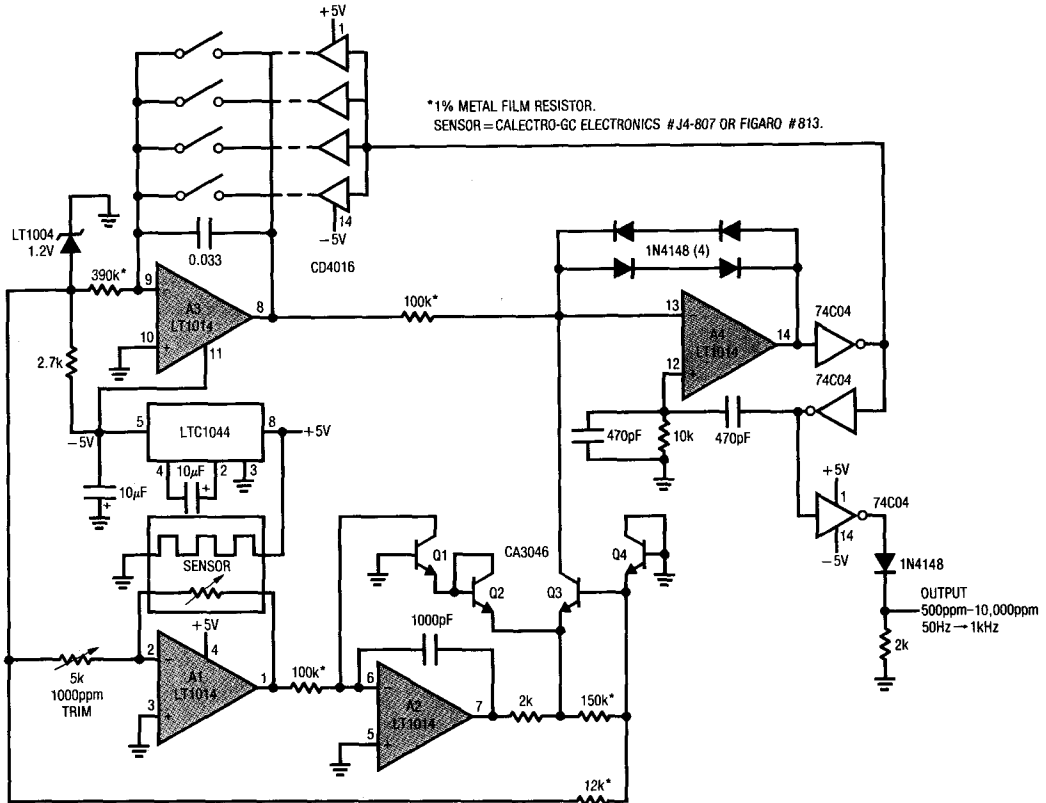


5V Powered EEPROM Pulse Generator



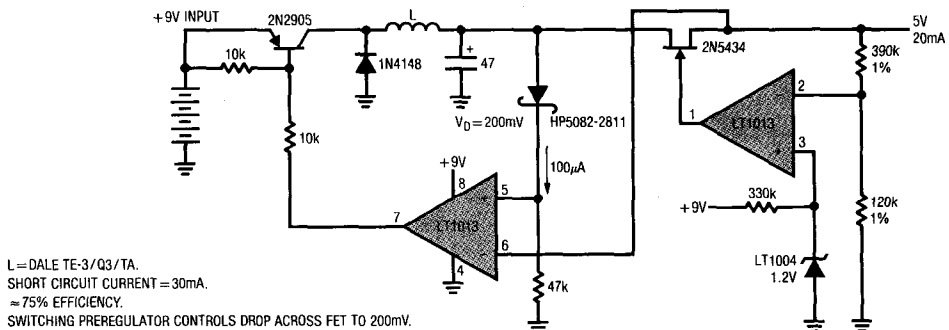
TYPICAL APPLICATIONS

Methane Concentration Detector with Linearized Output



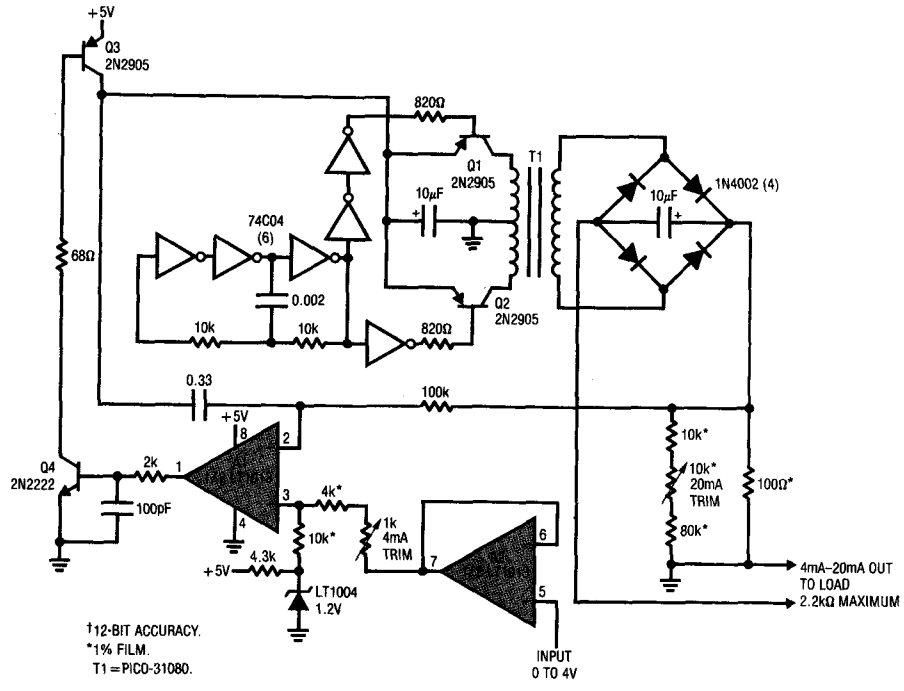
2

Low Power 9V to 5V Converter

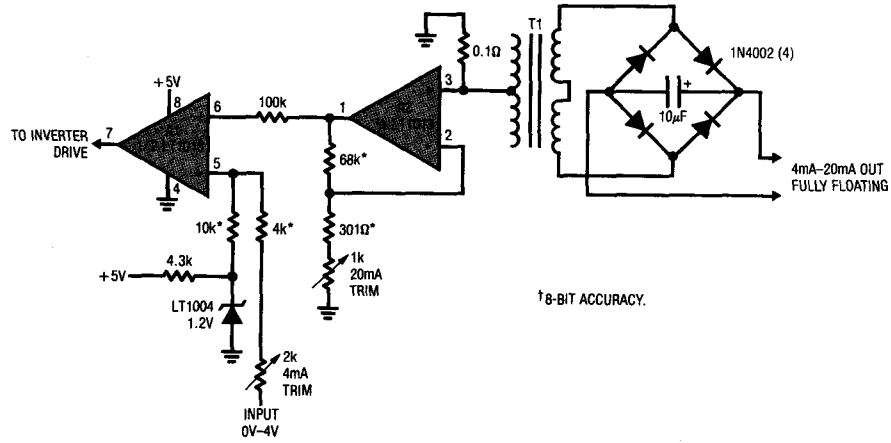


TYPICAL APPLICATIONS

5V Powered 4mA-20mA Current Loop Transmitter †

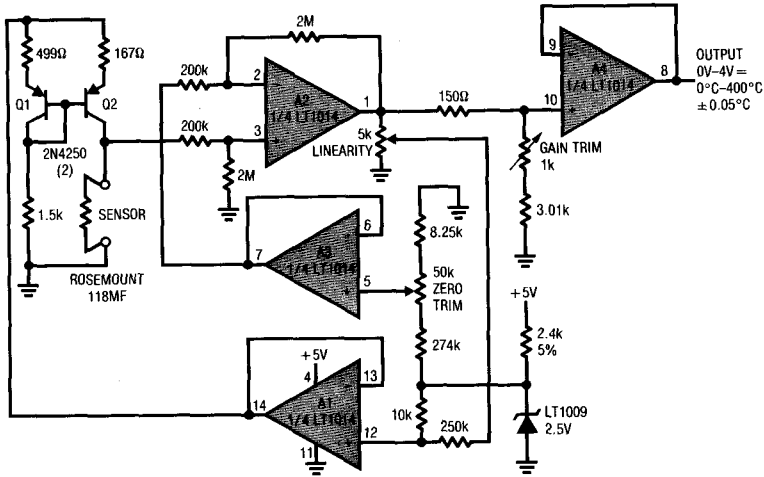


Fully Floating Modification to 4mA-20mA Current Loop †



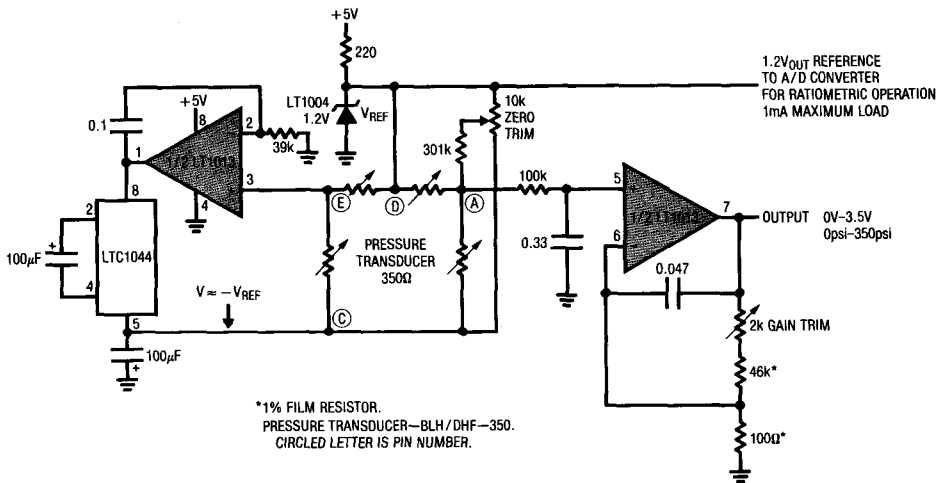
TYPICAL APPLICATIONS

5V Powered, Linearized Platinum RTD Signal Conditioner



ALL RESISTORS ARE TRW-MAR-6 METAL FILM.
 RATIO MATCH 2M-200K ±0.01%.
 TRIM SEQUENCE:
 SET SENSOR TO 0° VALUE.
 ADJUST ZERO FOR 0V OUT.
 SET SENSOR TO 100°C VALUE.
 ADJUST GAIN FOR 1.000V OUT.
 SET SENSOR TO 400°C.
 ADJUST LINEARITY FOR 4.000V OUT, REPEAT AS REQUIRED.

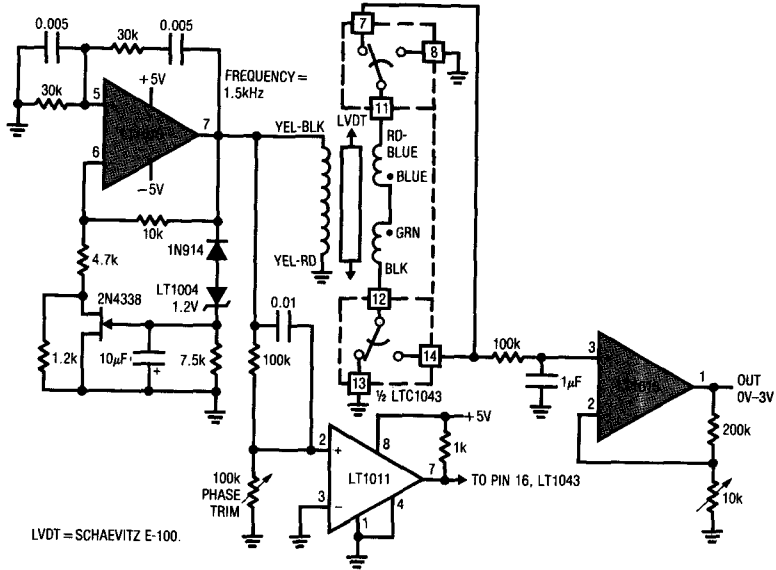
Strain Gage Bridge Signal Conditioner



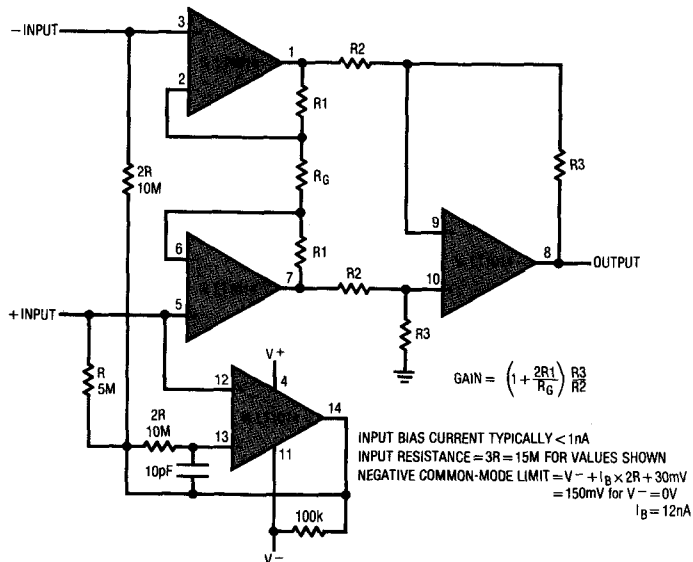
*1% FILM RESISTOR.
 PRESSURE TRANSDUCER—BLH/DHF—350.
 CIRCLED LETTER IS PIN NUMBER.

TYPICAL APPLICATIONS

LVDT Signal Conditioner

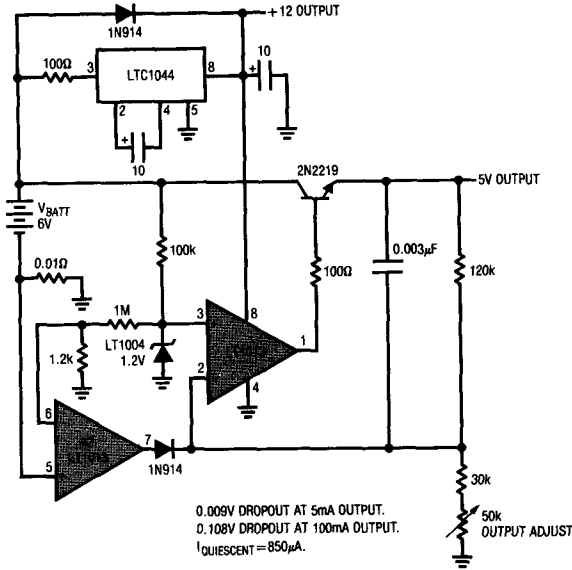


Triple Op Amp Instrumentation Amplifier with Bias Current Cancellation

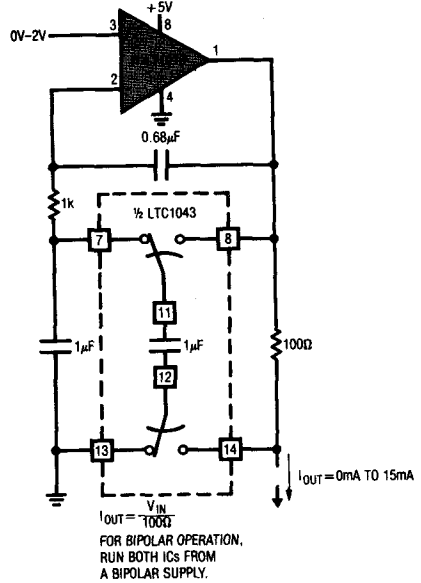


TYPICAL APPLICATIONS

Low Dropout Regulator for 6V Battery

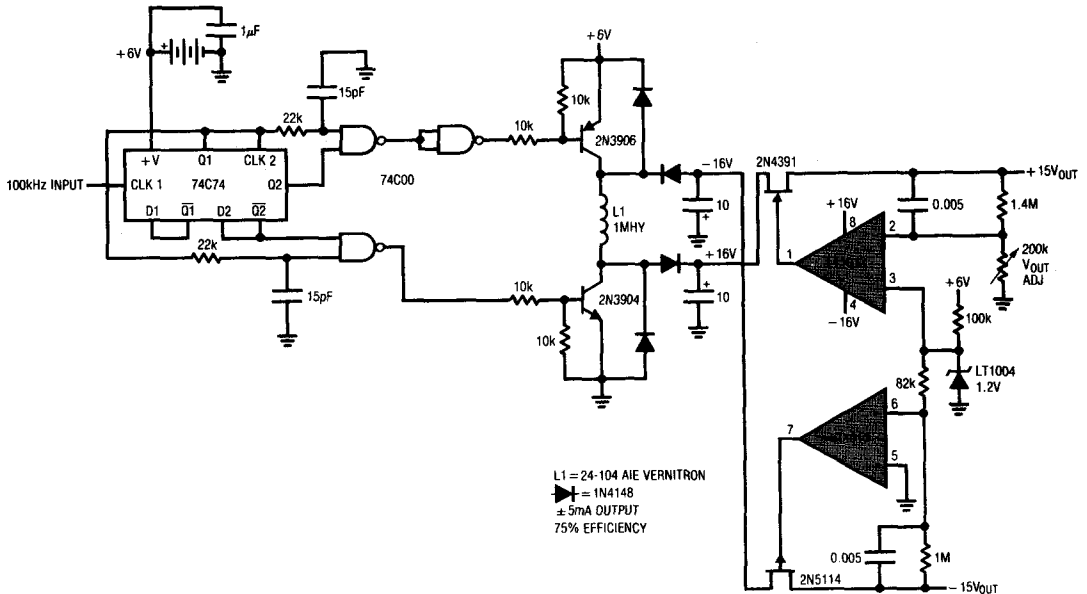


Voltage Controlled Current Source with Ground Referred Input and Output



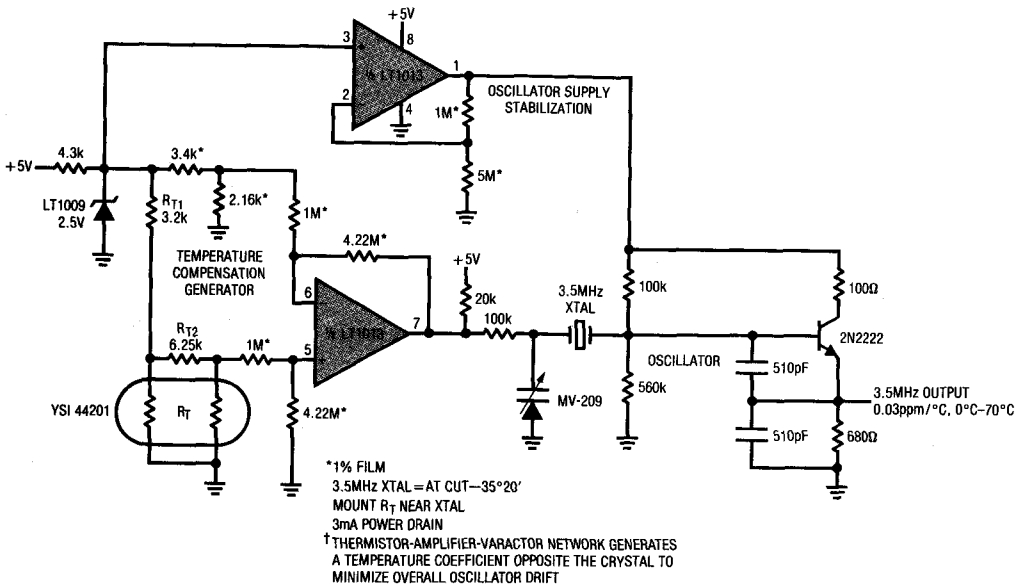
2

6V to ±15V Regulating Converter

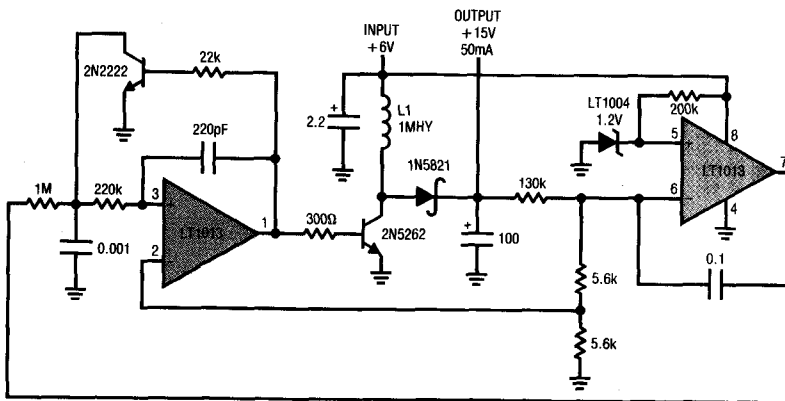


TYPICAL APPLICATIONS

Low Power, 5V Driven, Temperature Compensated Crystal Oscillator (TXCO)†



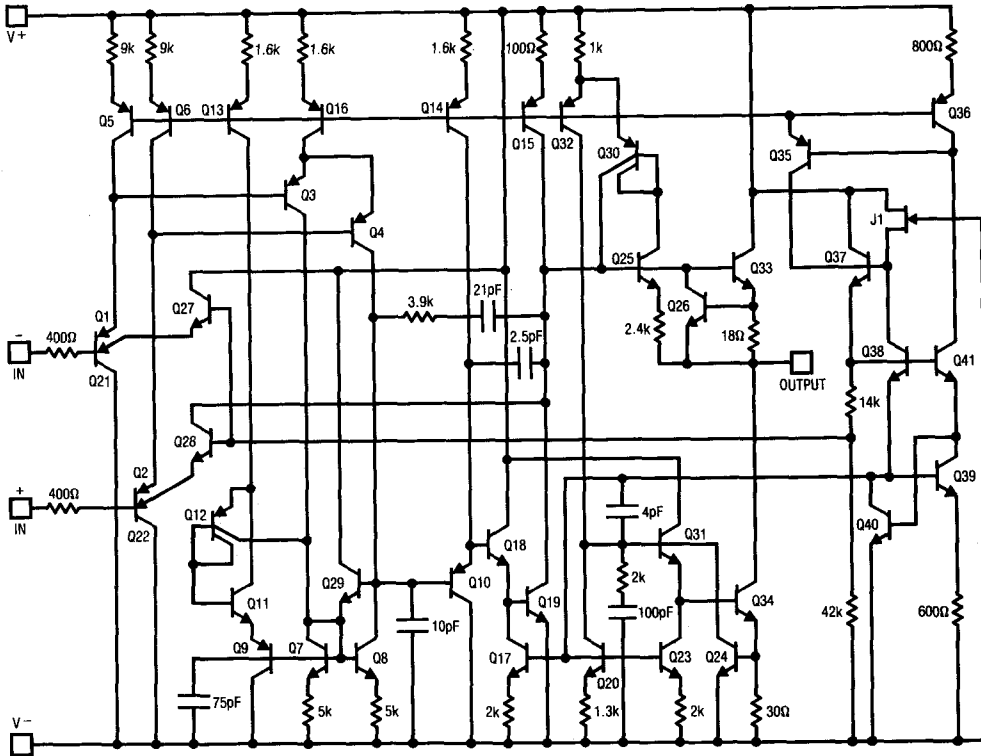
Step-Up Switching Regulator for 6V Battery



L1 = AIE-VERNITRON 24-104
 78% EFFICIENCY

SCHEMATIC DIAGRAM

1/2 LT1013, 1/4 LT1014

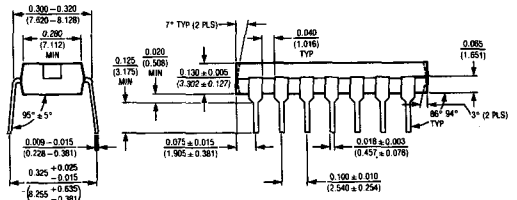
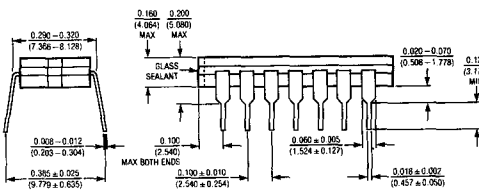
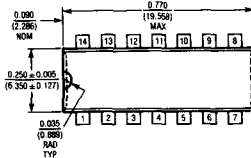
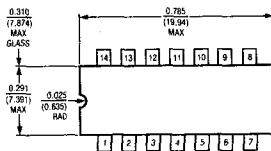


2

PACKAGE DESCRIPTION

J Package 14 Lead Cavity DIP

N Package 14 Lead Molded DIP

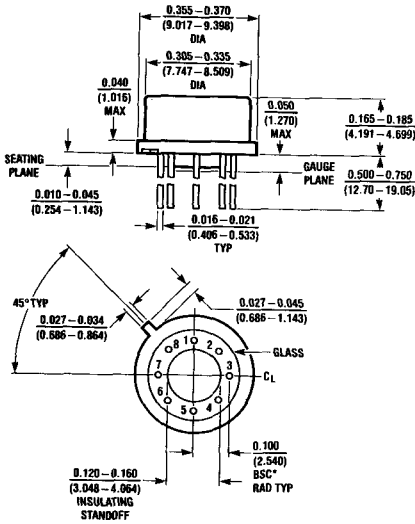


T_{jmax}	Θ_{JA}
150°C	100°C/W

T_{jmax}	Θ_{JA}
100°C	100°C/W

PACKAGE DESCRIPTION

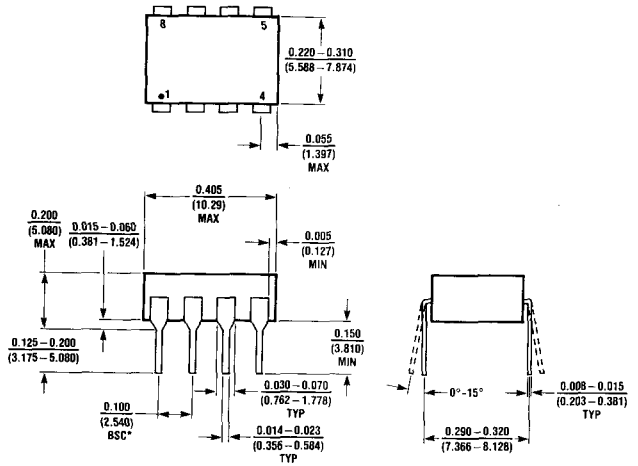
**H Package
Metal Can**



NOTE: DIMENSIONS IN INCHES (MILLIMETERS)

T_{jmax}	θ_{ja}	θ_{jc}
150°C	150°C/W	45°C/W

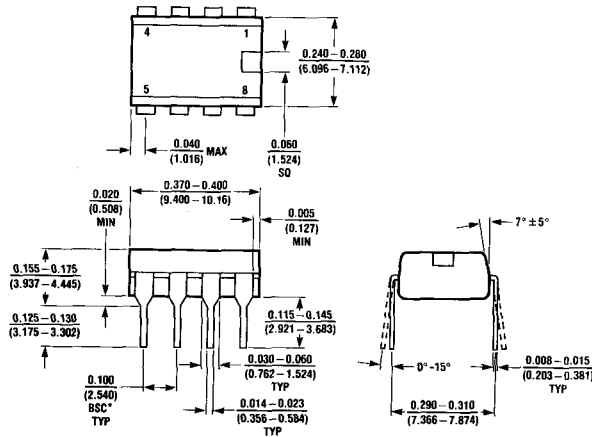
**J8 Package
8 Lead Hermetic DIP**



NOTE: DIMENSIONS IN INCHES (MILLIMETERS) UNLESS OTHERWISE NOTED
*LEADS WITHIN 0.007 OF TRUE POSITION (TP) AT GAUGE PLANE

T_{jmax}	θ_{ja}
150°C	100°C/W

**N8 Package
8 Lead Plastic**



NOTE: DIMENSIONS IN INCHES UNLESS OTHERWISE NOTED
*LEADS WITHIN 0.007 OF TRUE POSITION (TP) AT GAUGE PLANE

T_{jmax}	θ_{ja}
100°C	130°C/W

FEATURES

- Single Supply Operation
 - Input Voltage Range Extends to Ground
 - Output Swings to Ground while Sinking Current
- Pin Compatible to 1458 and 324 with Precision Specs
- *Guaranteed* Offset Voltage 800 μ V Max.
- *Guaranteed* Low Drift 5 μ V/ $^{\circ}$ C Max.
- *Guaranteed* Offset Current 1.5nA Max.
- *Guaranteed* High Gain
 - 5mA Load Current 1.2 Million Min.
 - 17mA Load Current 0.5 Million Min.
- *Guaranteed* Low Supply Current 550 μ A Max.
- Low Voltage Noise, 0.1Hz to 10Hz 0.55 μ Vp-p
- Low Current Noise—Better than OP-07, 0.07pA/ \sqrt Hz

APPLICATIONS

- Battery-Powered Precision Instrumentation
 - Strain Gauge Signal Conditioners
 - Thermocouple Amplifiers
 - Instrumentation Amplifiers
- 4mA–20mA Current Loop Transmitters
- Multiple Limit Threshold Detectors
- Active Filters
- Multiple Gain Blocks

DESCRIPTION

The LT1013 is the first precision dual op amp in the 8-pin small outline (SO) package, upgrading the performance of such popular devices as the MC1458, LM358 and OP-221.

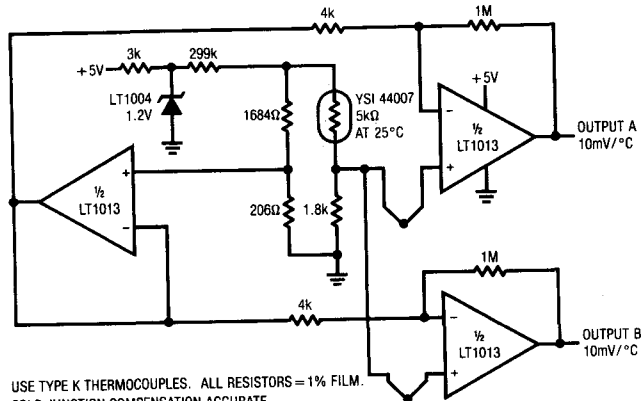
The LT1013's low offset voltage of 200 μ V, drift of 0.7 μ V/ $^{\circ}$ C, offset current of 0.2nA, gain of 7 million, common-mode rejection of 114dB, and power supply rejection of 117dB qualify it as two truly precision operational amplifiers. Particularly important is the low offset voltage, since no offset null terminals are provided in the dual configuration. Although supply current is only 350 μ A per amplifier, a new output stage design sources and sinks in excess of 20mA of load current, while retaining gain voltage gain.

The LT1013 can be operated off a single 5V power supply: input common-mode range includes ground; the output can also swing to within a few millivolts of ground. Crossover distortion, so apparent on previous single-supply designs, is eliminated. A full set of specifications is provided with \pm 15V and single 5V supplies.

REFER TO TABLE OF CONTENTS FOR REVISED DATA LOCATION

2

3 Channel Thermocouple Thermometer



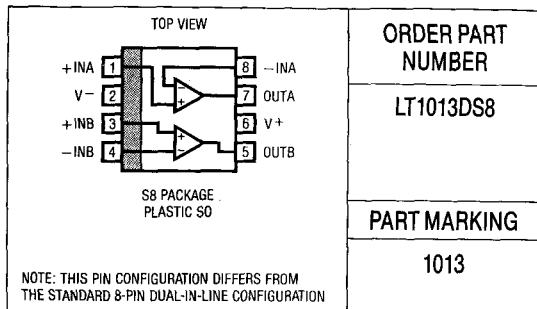
USE TYPE K THERMOCOUPLES. ALL RESISTORS = 1% FILM.
 COLD JUNCTION COMPENSATION ACCURATE
 TO \pm 1 $^{\circ}$ C FROM 0 $^{\circ}$ C \rightarrow 60 $^{\circ}$ C.
 USE 4TH AMPLIFIER FOR OUTPUT C.

LT1013DS8

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	$\pm 22V$
Differential Input Voltage	$\pm 30V$
Input Voltage	Equal to Positive Supply Voltage 5V Below Negative Supply Voltage
Output Short Circuit Duration	Indefinite
Operating Temperature Range	$0^{\circ}C$ to $70^{\circ}C$
Storage Temperature Range	
All Grades	$-65^{\circ}C$ to $150^{\circ}C$
Lead Temperature (Soldering, 10 sec.)	$300^{\circ}C$

PACKAGE/ORDER INFORMATION



ELECTRICAL CHARACTERISTICS $V_S = \pm 15V, V_{CM} = 0V, T_A = 25^{\circ}C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1013D			UNITS
			MIN	TYP	MAX	
V_{OS}	Input Offset Voltage			200	800	μV
	Long Term Input Offset Voltage Stability			0.5		$\mu V/Mo.$
I_{OS}	Input Offset Current			0.2	1.5	nA
I_B	Input Bias Current			15	30	nA
e_n	Input Noise Voltage	0.1Hz to 10Hz		0.55		$\mu Vp-p$
e_n	Input Noise Voltage Density	$f_0 = 10Hz$		24		nV/\sqrt{Hz}
		$f_0 = 1000Hz$		22		nV/\sqrt{Hz}
i_n	Input Noise Current Density	$f_0 = 10Hz$		0.07		pA/\sqrt{Hz}
	Input Resistance—Differential Common-Mode	(Note 1)	70	300 4		M Ω G Ω
A_{VOL}	Large Signal Voltage Gain	$V_O = \pm 10V, R_L \geq 2k$ $V_O = \pm 10V, R_L = 600\Omega$	1.2 0.5	7.0 2.0		$V/\mu V$ $V/\mu V$
	Input Voltage Range		+13.5 -15.0	+13.8 -15.3		V V
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm 13.5V, -15.0V$	97	114		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 2V$ to $\pm 18V$	100	117		dB
	Channel Separation	$V_O = \pm 10V, R_L = 2k$	120	137		dB
V_{OUT}	Output Voltage Swing	$R_L = 2k$	± 12.5	± 14		V
	Slew Rate		0.2	0.4		$V/\mu s$
I_S	Supply Current	Per Amplifier		0.35	0.55	mA

ELECTRICAL CHARACTERISTICS

$V_S^+ = +5V$, $V_S^- = 0V$, $V_{OUT} = 1.4V$, $V_{CM} = 0V$, $T_A = 25^\circ C$, unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS	LT1013D			UNITS
			MIN	TYP	MAX	
V_{OS}	Input Offset Voltage			250	950	μV
I_{OS}	Input Offset Current			0.3	2.0	nA
I_B	Input Bias Current			18	50	nA
A_{VOL}	Large Signal Voltage Gain	$V_O = 5mV$ to $4V$, $R_L = 500\Omega$		1.0		$V/\mu V$
	Input Voltage Range		+3.5 0	+3.8 -0.3		V
V_{OUT}	Output Voltage Swing	Output Low, No Load		15	25	mV
		Output Low, 600Ω to Ground		5	10	mV
		Output Low, $I_{SINK} = 1mA$		220	350	mV
		Output High, No Load		4.0	4.4	V
		Output High, 600Ω to Ground		3.4	4.0	V
I_S	Supply Current	Per Amplifier		0.32	0.50	mA

2

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $V_{CM} = 0V$, $0^\circ C \leq T_A \leq 70^\circ C$ unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS	LT1013D			UNITS	
			MIN	TYP	MAX		
V_{OS}	Input Offset Voltage	$V_S = +5V$, $0V$; $V_O = 1.4V$	●	230	1000	μV	
	Average Input Offset Voltage Drift	(Note 2)	●	280	1200	μV	
I_{OS}	Input Offset Current	$V_S = +5V$, $0V$; $V_O = 1.4V$	●	0.7	5.0	$\mu V/^\circ C$	
			●	0.3	2.8	nA	
I_B	Input Bias Current	$V_S = +5V$, $0V$; $V_O = 1.4V$	●	0.5	6.0	nA	
			●	16	38	nA	
			●	24	90	nA	
A_{VOL}	Large Signal Voltage Gain	$V_O = \pm 10V$, $R_L = 2k$	●	0.7	4.0	$V/\mu V$	
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm 13.0V$, $-15.0V$	●	94	113	dB	
PSRR	Power Supply Rejection Ratio	$V_S = \pm 2V$ to $\pm 18V$	●	97	116	dB	
V_{OUT}	Output Voltage Swing	$R_L = 2k$	●	± 12.0	± 13.9	V	
		$V_S = +5V$, $0V$; $R_L = 600\Omega$	●		6	13	mV
		Output Low Output High	●	3.2	3.9	V	
I_S	Supply Current per Amplifier	$V_S = +5V$, $0V$; $V_O = 1.4V$	●	0.37	0.60	mA	
			●	0.34	0.55	mA	

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: This parameter is guaranteed by design and is not tested. Typical parameters are defined as the 60% yield of parameter distributions of individual amplifiers; i.e., out of 100 LT1013s typically 120 op amps will be better than the indicated specification.

Note 2: This parameter is not 100% tested.

NOTES

High Speed, Precision JFET Input Operational Amplifier

FEATURES

- *Guaranteed* Slew Rate
23V / μ s Min.
- *Guaranteed* Offset Voltage
250 μ V Max.
–55°C to 125°C
750 μ V Max.
- *Guaranteed* Drift
5 μ V / °C Max.
- *Guaranteed* Bias Current
70°C
180pA Max.
125°C
4nA Max.
- Gain-Bandwidth Product
8.5MHz Typ.
- Settling Time to 0.05% (10V Step)
0.9 μ s Typ.

APPLICATIONS

- Fast D/A Output Amplifiers (12, 14, 16 Bits)
- High Speed Instrumentation
- Fast, Precision Sample and Hold
- Voltage-to-Frequency Converters
- Logarithmic Amplifiers

DESCRIPTION

The LT1022 JFET input operational amplifier combines high speed and precision performance.

A 26V / μ s slew rate and 8.5MHz gain-bandwidth product are simultaneously achieved with offset voltage of typically 80 μ V, 1.5 μ V / °C drift, bias currents of 50pA at 70°C, 500pA at 125°C. The output delivers 20mA of load current without gain degradation.

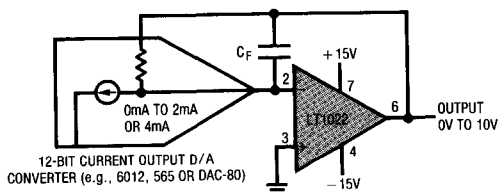
The 250 μ V maximum offset voltage specification represents less than 1/2 least significant bit error in a 14-bit, 10V system.

The LT1022A meets or exceeds all OP-16A and OP-16E specifications. It is faster and more accurate without stability problems at cold temperatures.

The LT1022 can be used as the output amplifier for 12-bit current output D/A converters, as shown below.

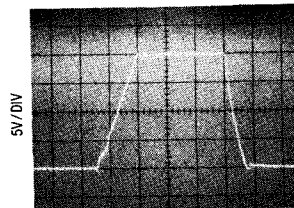
For a more accurate, lower power dissipation, but slower JFET input op amp, please refer to the LT1055 data sheet.

12-Bit Voltage Output D/A Converter



$C_F = 15\text{pF TO } 33\text{pF}$
 SETTTLING TIME TO 2mV (0.8 LSB) = 1.5 μ s TO 2 μ s

Large Signal Response



$A_V = 1$, $C_L = 100\text{pF}$, 0.5 μ s / DIV
 $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{V}$

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	± 20V
Differential Input Voltage	± 40V
Input Voltage	± 20V
Output Short Circuit Duration	Indefinite
Operating Temperature Range	
LT1022AM / 1022M	-55°C to 125°C
LT1022AC / 1022C	0°C to 70°C
Storage Temperature Range	
All Devices	-65°C to 150°C
Lead Temperature (Soldering, 10 sec.)	300°C

PACKAGE/ORDER INFORMATION

<p>TOP VIEW N/C BALANCE 1 8 7 V+ -IN 2 6 OUT +IN 3 5 BALANCE V- 4</p> <p>METAL CAN H PACKAGE</p>	ORDER PART NUMBER
	LT1022AMH LT1022MH LT1022ACH LT1022CH
<p>TOP VIEW BAL 1 8 N/C -IN 2 7 V+ +IN 3 6 OUT V- 4 5 BAL</p> <p>PLASTIC DIP N8 PACKAGE</p>	LT1022CN8

ELECTRICAL CHARACTERISTICS

$V_S = \pm 15V$, $T_A = 25^\circ C$, $V_{CM} = 0V$ unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS	LT1022AM LT1022AC			LT1022M LT1022CH LT1022CN8			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage (Note 1)	H Package N8 Package	—	80	250	—	100	600	μV μV
I_{OS}	Input Offset Current	Fully Warmmed Up	—	2	10	—	2	20	pA
I_B	Input Bias Current	Fully Warmmed Up $V_{CM} = +10V$	—	± 10 + 30	± 50 + 100	—	± 10 + 30	± 50 + 150	pA pA
	Input Resistance—Differential —Common-Mode	$V_{CM} = -11V$ to $+8V$ $V_{CM} = +8V$ to $+11V$	—	10^{12} 10^{12} 10^{11}	— — —	—	10^{12} 10^{12} 10^{11}	— — —	Ω Ω Ω
	Input Capacitance		—	4	—	—	4	—	pF
e_n	Input Noise Voltage	0.1Hz to 10Hz	—	2.5	—	—	2.8	—	μV_{p-p}
e_n	Input Noise Voltage Density	$f_0 = 10Hz$ (Note 2) $f_0 = 1kHz$ (Note 3)	—	28 14	50 20	—	30 15	60 22	nV/ \sqrt{Hz} nV/ \sqrt{Hz}
i_n	Input Noise Current Density	$f_0 = 10Hz$, 1kHz (Note 4)	—	1.8	4	—	1.8	4	fA/ \sqrt{Hz}
A_{VOL}	Large Signal Voltage Gain	$V_0 = \pm 10V$ $R_L = 2k$ $R_L = 1k$	150 130	400 300	—	120 100	400 300	—	V/mV V/mV
	Input Voltage Range		± 10.5	± 12	—	± 10.5	± 12	—	V
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm 10.5V$	86	94	—	82	92	—	dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 10V$ to $\pm 18V$	88	104	—	86	102	—	dB
V_{OUT}	Output Voltage Swing	$R_L = 2k$	± 12	± 13.2	—	± 12	± 13.2	—	V
SR	Slew Rate		23	26	—	18	24	—	V/ μs
GBW	Gain-Bandwidth Product	$f = 1MHz$	—	8.5	—	—	8.0	—	MHz
I_S	Supply Current		—	5.2	7.0	—	5.2	7.0	mA
	Settling Time	A = +1 or A = -1 10V Step to 0.05% 10V Step to 0.02%	—	0.9 1.3	—	—	0.9 1.3	—	μs μs
	Offset Voltage Adjustment Range	$R_{POT} = 100k$	—	± 7	—	—	± 7	—	mV

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V, V_{CM} = 0V, 0^\circ C \leq T_A \leq 70^\circ C$ unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS	LT1022AC			LT1022CH LT1022CN8			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage (Note 1)	H Package	● —	140	480	—	180	1000	μV
		N8 Package	● —	—	—	—	300	1700	μV
	Average Temperature Coefficient of Input Offset Voltage	H Package	● —	1.3	5.0	—	1.8	9.0	$\mu V / ^\circ C$
		N8 Package (Note 5)	● —	—	—	—	3.0	15.0	$\mu V / ^\circ C$
I_{OS}	Input Offset Current	Warmed Up, $T_A = 70^\circ C$	● —	15	80	—	18	100	pA
I_B	Input Bias Current	Warmed Up, $T_A = 70^\circ C$	● —	± 50	± 200	—	± 60	± 250	pA
A_{VOL}	Large Signal Voltage Gain	$V_O = \pm 10V, R_L = 2k$	● 80	250	—	60	250	—	V/mV
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm 10.4V$	● 85	93	—	80	91	—	dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 10V$ to $\pm 18V$	● 86	103	—	84	101	—	dB
V_{OUT}	Output Voltage Swing	$R_L = 2k$	● ± 12	± 13.1	—	± 12	± 13.1	—	V

2

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V, V_{CM} = 0V, -55^\circ C \leq T_A \leq 125^\circ C$ unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS	LT1022AM			LT1022M			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	(Note 1)	● —	230	750	—	300	1500	μV
		(Note 5)	● —	1.5	5.0	—	2.0	9.0	$\mu V / ^\circ C$
I_{OS}	Input Offset Current	Warmed Up, $T_A = 125^\circ C$	● —	0.3	2.0	—	0.30	3.0	nA
		Warmed Up, $T_A = 125^\circ C$	● —	± 0.5	± 4.0	—	± 0.7	± 6.0	nA
I_B	Input Bias Current	Warmed Up, $T_A = 125^\circ C$	● 40	120	—	35	120	—	V/mV
A_{VOL}	Large Signal Voltage Gain	$V_O = \pm 10V, R_L = 2k$	● 85	92	—	80	90	—	dB
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm 10.4V$	● 86	102	—	84	100	—	dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 10V$ to $\pm 17V$	● ± 12	± 12.9	—	± 12	± 12.9	—	V
V_{OUT}	Output Voltage Swing	$R_L = 2k$	● ± 12	± 12.9	—	± 12	± 12.9	—	V

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: Offset voltage is measured under two different conditions:

- (a) approximately 0.5 seconds after application of power;
- (b) at $T_A = 25^\circ C$, with the chip self-heated to approximately $45^\circ C$ to account for chip temperature rise when the device is fully warmed up.

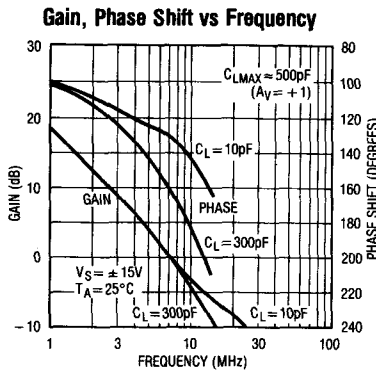
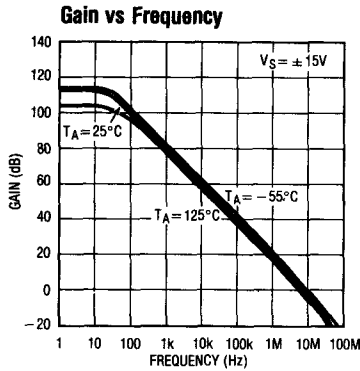
Note 2: 10Hz noise voltage density is sample tested on every lot of A grades. Devices 100% tested at 10Hz are available on request.

Note 3: This parameter is tested on a sample basis only.

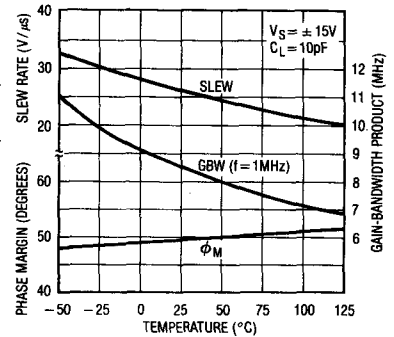
Note 4: Current noise is calculated from the formula: $i_n = (2qI_B)^{1/2}$, where $q = 1.6 \times 10^{-19}$ coulomb. The noise of source resistors up to 1G Ω swamps the contribution of current noise.

Note 5: Offset voltage drift with temperature is practically unchanged when the offset voltage is trimmed to zero with a 100k potentiometer between the balance terminals and the wiper tied to V^+ . Devices tested to tighter drift specifications are available on request.

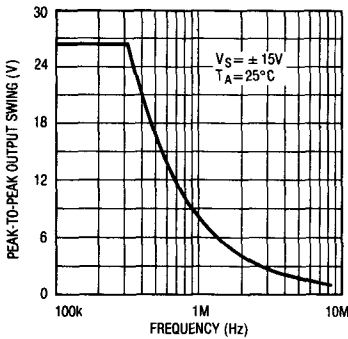
TYPICAL PERFORMANCE CHARACTERISTICS



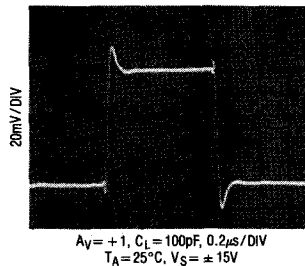
Phase Margin, Gain Bandwidth Product, Slew Rate vs Temperature



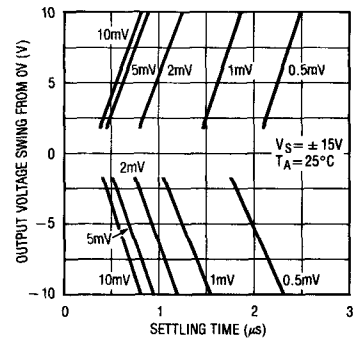
Undistorted Output Swing vs Frequency



Small Signal Response



Settling Time



The typical behavior of many LT1022 parameters is identical to the LT1056. Please refer to the LT1055/1056 data sheet for the following typical performance characteristics:

- Input Bias and Offset Currents vs Temperature
- Input Bias Current Over the Common-Mode Range
- Distribution of Input Offset Voltage (H and N8 Package)
- Distribution of Offset Voltage Drift with Temperature
- Warm-Up Drift
- Long Term Drift of Representative Units
- 0.1Hz to 10Hz Noise
- Voltage Noise vs Frequency
- Noise vs Chip Temperature

- Output Impedance vs Frequency
- Common-Mode Range vs Temperature
- Common-Mode and Power Supply Rejections vs Temperature
- Common-Mode Rejection Ratio vs Frequency
- Power Supply Rejection Ratio vs Frequency
- Voltage Gain vs Temperature
- Supply Current vs Supply Voltage
- Output Swing vs Load Resistance
- Short Circuit Current vs Time

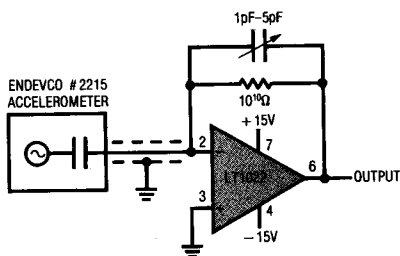
APPLICATIONS INFORMATION

The LT1056 applications information is directly applicable to the LT1022. Please consult the LT1055/1056 data sheet for details on:

- (1) plug-in compatibility to industry standard devices
- (2) offset nulling
- (3) achieving picoampere/microvolt performance
- (4) phase-reversal protection
- (5) high speed operation (including settling time test circuit)
- (6) noise performance
- (7) simplified circuit schematic.

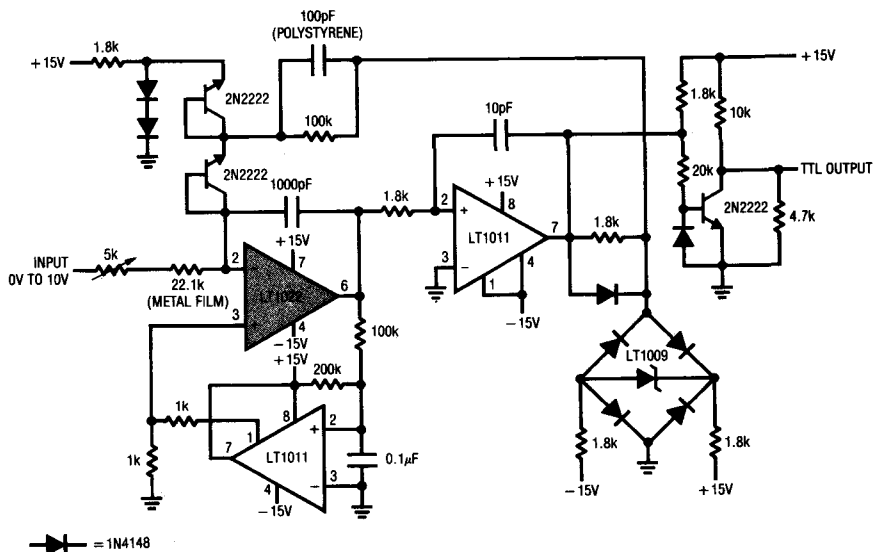
TYPICAL APPLICATIONS

Fast Piezoelectric Accelerometer



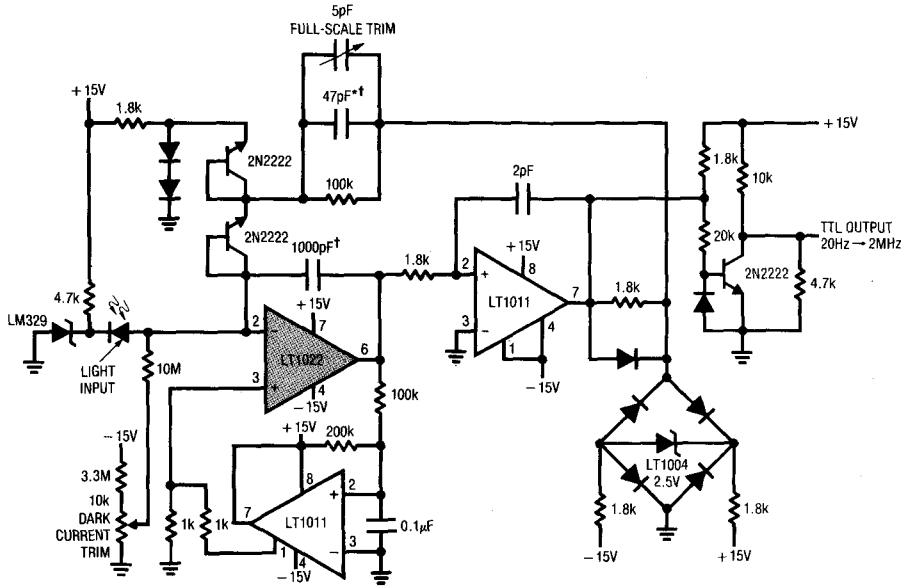
2

10Hz to 1MHz Voltage-to-Frequency Converter



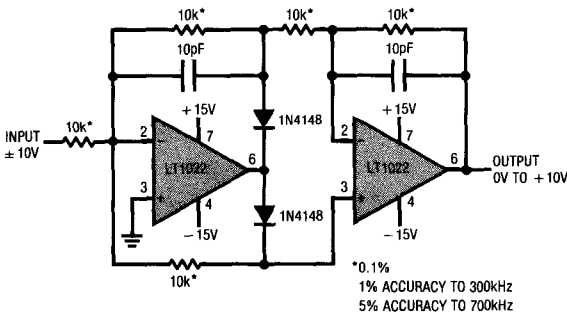
TYPICAL APPLICATIONS

PIN Photodiode-to-Frequency Converter

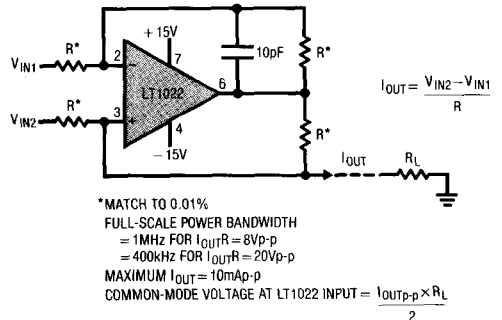


SCALE FACTOR =
 1mV/Hz AT 900 NANOMETERS FROM 20nW TO 2mW
 ∇ = HEWLETT PACKARD PHOTODIODE HP5082-4204
 \rightarrow = 1N4148
 \dagger POLYSTYRENE
 * SELECT VALUE FOR 2mW IN = 2MHz OUT.

Wide Bandwidth Absolute Value Circuit

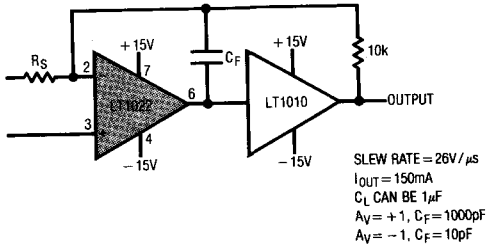


Fast, Differential Input Current Source

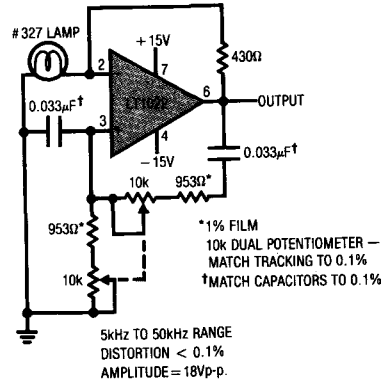


TYPICAL APPLICATIONS

High Output Current Op Amp

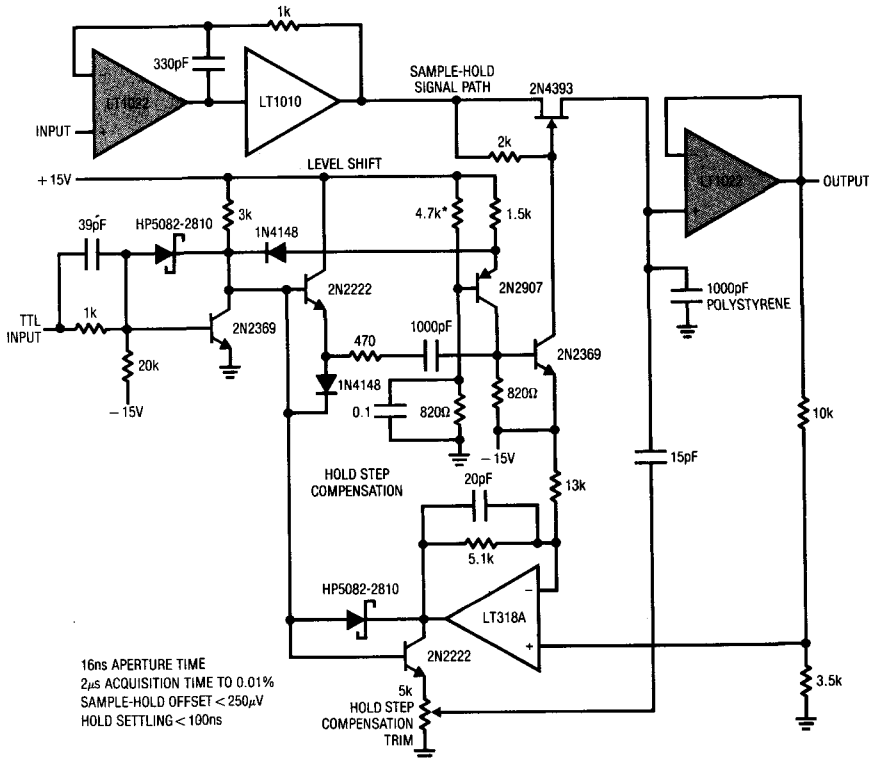


Low Distortion Sine Wave Oscillator



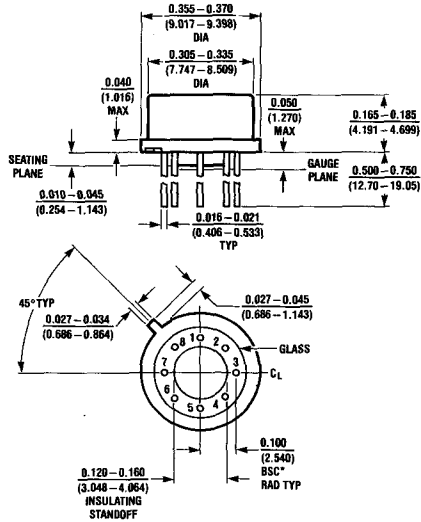
2

Fast, Precision Sample-Hold



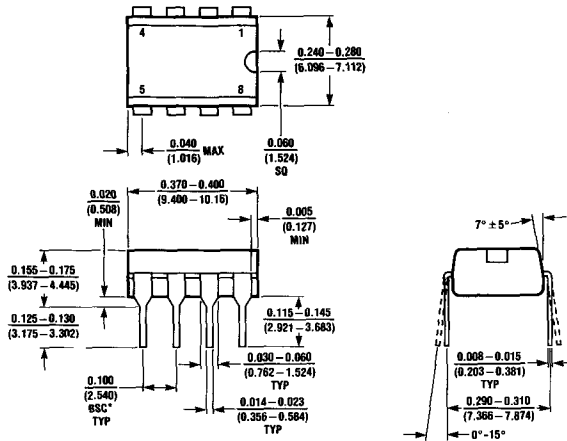
PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

**H Package
Metal Can**



T_{jmax}	$\theta_{j\theta}$	θ_{jC}
150°C	150°C/W	45°C/W

**N8 Package
8 Lead Plastic**



*LEADS WITHIN 0.007 OF TRUE POSITION (TP) AT GAUGE PLANE

T_{jmax}	$\theta_{j\theta}$
100°C	130°C/W

Dual, Matched Picoampere, Microvolt Input, Low Noise Op Amp

FEATURES

- *Guaranteed* Offset Voltage 50 μ V Max.
- *Guaranteed* Bias Current 120pA Max.
 25°C 700pA Max.
 -55°C to 125°C 1.5 μ V/°C Max.
- *Guaranteed* Drift 0.5 μ Vp-p
- Low Noise, 0.1Hz to 10Hz 600 μ A Max.
- *Guaranteed* Supply Current 112dB Min.
- *Guaranteed* CMRR 112dB Min.
- *Guaranteed* PSRR
- *Guaranteed* Voltage Gain with 5mA Load Current
- *Guaranteed* Matching Characteristics

APPLICATIONS

- Strain Gauge Signal Conditioner
- Dual Limit Precision Threshold Detection
- Charge Integrators
- Wide Dynamic Range Logarithmic Amplifiers
- Light Meters
- Low Frequency Active Filters
- Standard Cell Buffers
- Thermocouple Amplifiers

DESCRIPTION

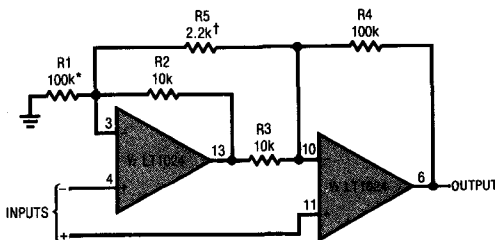
The LT1024 dual, matched internally compensated universal precision operational amplifier can be used in practically all precision applications requiring multiple op amps. The LT1024 combines picoampere bias currents (which are maintained over the full -55°C to 125°C temperature range), microvolt offset voltage (and low drift with time and temperature), low voltage and current noise, and low power dissipation. Extremely high common-mode and power supply rejection ratios, practically immeasurable warm-up drift, and the ability to deliver 5mA load current with a voltage gain of a million round out the LT1024's superb precision specifications.

Tight matching is guaranteed on offset voltage, non-inverting bias currents and common-mode and power supply rejections.

The all-around excellence of the LT1024 eliminates the necessity of the time-consuming error analysis procedure of precision system design in many dual applications; the LT1024 can be stocked as the universal dual op amp in the 14-pin DIP configuration.

For a single op amp with similar specifications, see the LT1012 data sheet; for a single supply dual precision op amp in the 8-pin configuration, see the LT1013 data sheet.

Two Op Amp Instrumentation Amplifier

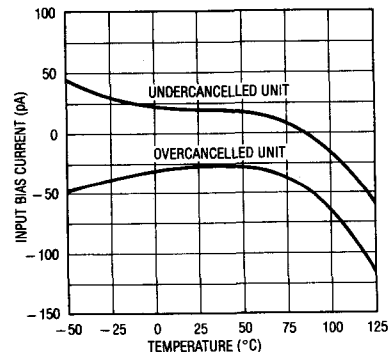


$$\text{GAIN} = \frac{R_4}{R_3} \left[1 + \frac{1}{2} \left(\frac{R_2}{R_1 + R_4} \right) + \frac{R_2 + R_3}{R_5} \right] \approx 100$$

*TRIM FOR COMMON-MODE REJECTION
 †TRIM FOR GAIN

TYPICAL PERFORMANCE:
 OFFSET VOLTAGE = 20 μ V
 BIAS CURRENT = \pm 30pA
 OFFSET CURRENT = 30pA

Input Bias Current vs Temperature



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	± 20V
Differential Input Current (Note 1)	± 10mA
Input Voltage	± 20V
Output Short Circuit Duration	Indefinite
Operating Temperature Range	
LT1024AM/LT1024M	−55°C to 125°C
LT1024AC/LT1024C	0°C to 70°C
Storage Temperature Range	
All Devices	−65°C to 150°C
Lead Temperature (Soldering, 10 sec.)	300°C

PACKAGE/ORDER INFORMATION

TOP VIEW

NULL (A) 1 14 V+ (A)
 NULL (A) 2 13 OUT (A)
 − IN (A) 3 12 V− (A)
 + IN (A) 4 11 + IN (B)
 V− (B) 5 10 − IN (B)
 OUT (B) 6 9 NULL (B)
 V+ (B) 7 8 NULL (B)

D PACKAGE N PACKAGE
 14 PIN HERMETIC 14 PIN PLASTIC
 (SIDE BRAZED)

NOTE: DEVICE MAY BE OPERATED EVEN IF INSERTION IS REVERSED, THIS IS DUE TO INHERENT SYMMETRY OF PIN LOCATIONS OF AMPLIFIERS A AND B (NOTE 2).

ORDER PART NUMBER

LT1024AMD
LT1024MD
LT1024ACN
LT1024CN

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V, V_{CM} = 0V, T_A = 25^\circ C$ unless otherwise noted

Individual Amplifiers

SYMBOL	PARAMETER	CONDITIONS	LT1024AM/LT1024AC			LT1024M/LT1024C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage			15	50		20	100	μV
	Long Term Input Offset Voltage Stability			0.3		0.3			$\mu V/month$
I_{OS}	Input Offset Current			20	100		25	180	pA
I_B	Input Bias Current			± 25	± 120		± 30	± 200	pA
e_n	Input Noise Voltage	0.1Hz to 10Hz		0.5		0.5			$\mu Vp-p$
e_n	Input Noise Voltage Density	$f_0 = 10Hz$ (Note 3)		17	33		17	33	nV/\sqrt{Hz}
		$f_0 = 1000Hz$ (Note 3)		14	24		14	24	nV/\sqrt{Hz}
i_n	Input Noise Current Density	$f_0 = 10Hz$		20		20			fA/\sqrt{Hz}
A_{VOL}	Large Signal Voltage Gain	$V_{OUT} = \pm 12V, R_L \geq 10k\Omega$	250	2000		180	2000		V/mV
		$V_{OUT} = \pm 10V, R_L \geq 2k\Omega$	150	1000		100	1000		V/mV
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm 13.5V$	112	132		108	132		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 2V$ to $\pm 20V$	112	132		108	132		dB
	Input Voltage Range		± 13.5	± 14.0		± 13.5	± 14.0		V
V_{OUT}	Output Voltage Swing	$R_L = 10k\Omega$	± 13	± 14		± 13	± 14		V
	Slew Rate		0.1	0.2		0.1	0.2		V/ μs
I_S	Supply Current per Amplifier			380	600		380	700	μA

Matching Specifications

SYMBOL	PARAMETER	CONDITIONS	LT1024AM/LT1024AC			LT1024M/LT1024C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
	Input Offset Voltage Match		—	20	75	—	25	150	μV
I_B^+	Average Non-Inverting Bias Current		—	± 30	± 150	—	± 40	± 250	pA
I_{OS}^+	Non-Inverting Offset Current		—	30	150	—	30	300	pA
$\Delta CMRR$	Common Mode Rejection Ratio Match	$V_{CM} = \pm 13.5V$	110	132	—	106	132	—	dB
$\Delta PSRR$	Power Supply Rejection Ratio Match	$V_S = \pm 2V$ to $20V$	110	132	—	106	132	—	dB
	Channel Separation	$f \leq 10Hz$ (Note 3)	134	150	—	134	150	—	dB

ELECTRICAL CHARACTERISTICS

$V_S = \pm 15V$, $V_{CM} = 0V$, $0^\circ C \leq T_A \leq 70^\circ C$ for the LT1024AC and LT1024C;
 $-55^\circ C \leq T_A \leq 125^\circ C$ for the LT1024AM and LT1024M unless otherwise noted

Individual Amplifiers

SYMBOL	PARAMETER	CONDITIONS	LT1024AM/LT1024AC			LT1024M/LT1024C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	$0^\circ C$ to $70^\circ C$ $-55^\circ C$ to $125^\circ C$	●	30	120		35	200	μV
			●	40	200		50	300	μV
	Average Temperature Coefficient of Input Offset Voltage		●	0.25	1.5		0.3	2.0	$\mu V/^\circ C$
I_{OS}	Input Offset Current	$0^\circ C$ to $70^\circ C$ $-55^\circ C$ to $125^\circ C$	●	40	250		50	300	pA
			●	80	350		100	500	pA
	Average Temperature Coefficient of Input Offset Current		●	0.5	2.5		0.7	3	$pA/^\circ C$
I_B	Input Bias Current	$0^\circ C$ to $70^\circ C$ $-55^\circ C$ to $125^\circ C$	●	± 40	± 250		± 50	± 400	pA
			●	± 100	± 700		± 200	± 1300	pA
	Average Temperature Coefficient of Input Bias Current	$0^\circ C$ to $70^\circ C$ $-55^\circ C$ to $125^\circ C$	●	0.4	3		0.5	4	$pA/^\circ C$
			●	1	6		2	12	$pA/^\circ C$
A_{VOL}	Large Signal Voltage Gain	$V_{OUT} = \pm 12V$, $R_L \geq 10k\Omega$	●	150	1000		150	1000	V/mV
		$V_{OUT} = \pm 10V$, $R_L \geq 2k\Omega$	●	100	600		100	600	V/mV
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm 13.5V$	●	108	128		106	128	dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 2.5V$ to $\pm 18V$	●	108	128		106	128	dB
	Input Voltage Range		●	± 13.5		± 13.5		V	
V_{OUT}	Output Voltage Swing	$R_L = 10k\Omega$	●	± 13	± 14		± 13	± 14	V
I_S	Supply Current		●	400	800		400	900	μA

2

Matching Specifications

SYMBOL	PARAMETER	CONDITIONS	LT1024AM/LT1024AC			LT1024M/LT1024C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
	Input Offset Voltage Match	$0^\circ C$ to $70^\circ C$ $-55^\circ C$ to $125^\circ C$	●	35	170		45	300	μV
			●	—	50	280	—	70	500
	Input Offset Voltage Tracking		●	—	0.3	2.0	—	0.4	3.5
I_B^+	Average Non-Inverting Bias Current	$0^\circ C$ to $70^\circ C$	●	± 40	± 300		± 50	± 500	pA
		$-55^\circ C$ to $125^\circ C$	●	± 100	± 800		± 200	± 1400	pA
I_{OS}^+	Non-Inverting Offset Current	$0^\circ C$ to $70^\circ C$	●	—	40	300	—	50	500
		$-55^\circ C$ to $125^\circ C$	●	—	80	800	—	150	1500
$\Delta CMRR$	Common-Mode Rejection Ratio Match	$V_{CM} = \pm 13.5V$	●	106	128	—	104	128	—
$\Delta PSRR$	Power Supply Rejection Ratio Match	$V_S = \pm 2.5V$ to $\pm 18V$	●	106	128	—	104	128	—

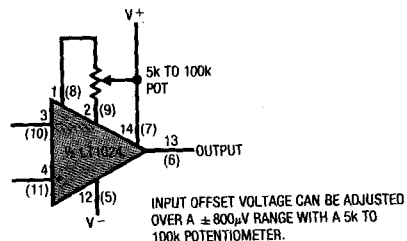
The ● denotes the specifications which apply over the full operating temperature range.

Note 1: Differential input voltages greater than 1V will cause excessive current to flow through the input protection diodes unless limiting resistance is used.

Note 2: The V^+ supply terminals are completely independent and may be powered by separate supplies if desired (this approach, however, would sacrifice the advantages of the power supply rejection ratio matching). The V^- supply terminals are both connected to the common substrate and must be tied to the same voltage. Both V^- pins should be used.

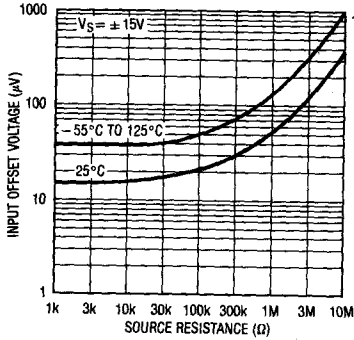
Note 3: This parameter is tested on a sample basis only.

Optional Offset Nulling Circuit

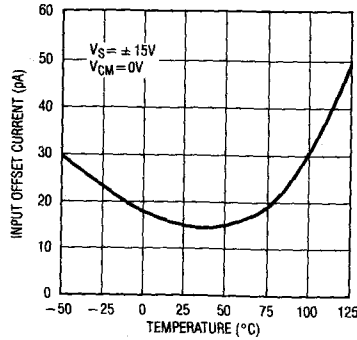


TYPICAL PERFORMANCE CHARACTERISTICS

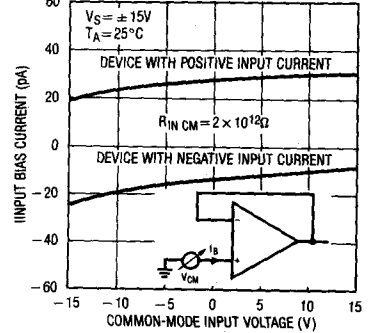
Offset Voltage vs Source Resistance (Balanced or Unbalanced)



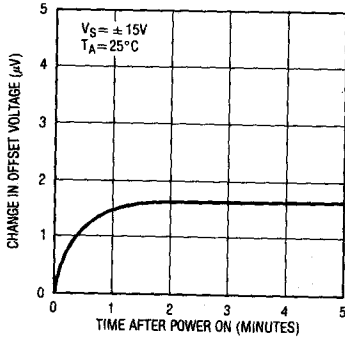
Input Offset Current vs Temperature



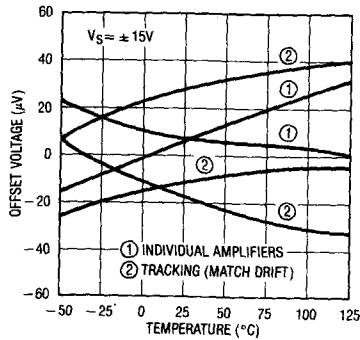
Input Bias Current Over Common-Mode Range



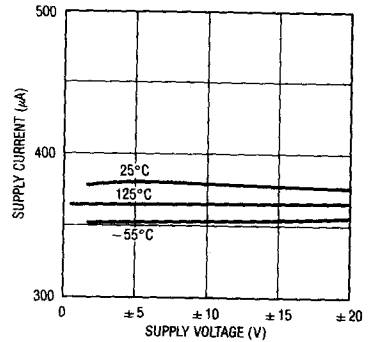
Warm-Up Drift



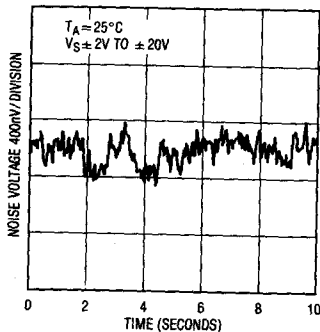
Offset Voltage Drift and Tracking with Temperature of Representative Units



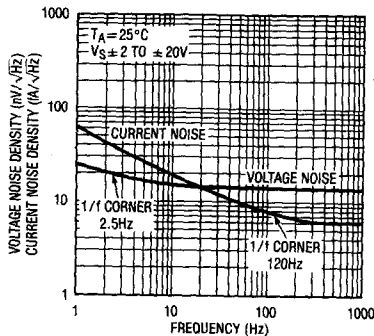
Supply Current vs Supply Voltage per Amplifier



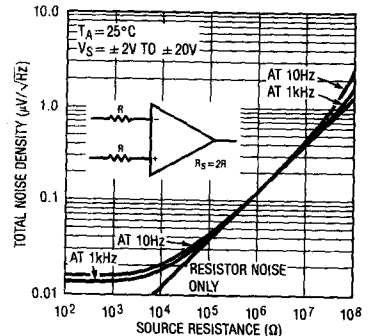
0.1Hz to 10Hz Noise



Noise Spectrum

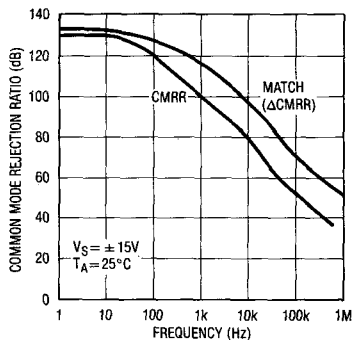


Total Noise vs Source Resistance

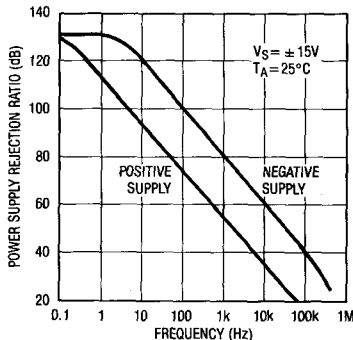


TYPICAL PERFORMANCE CHARACTERISTICS

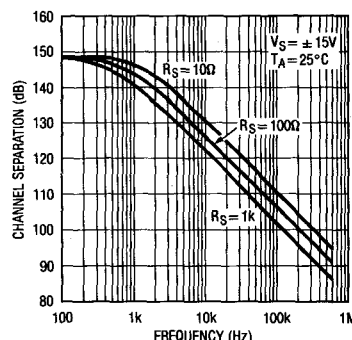
Common-Mode Rejection and CMRR Match vs Frequency



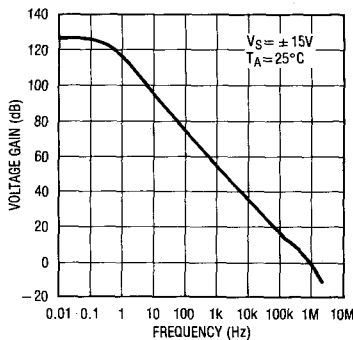
Power Supply Rejection vs Frequency



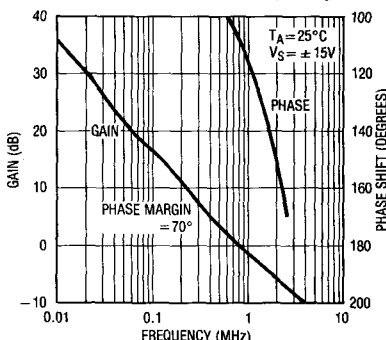
Channel Separation vs Frequency



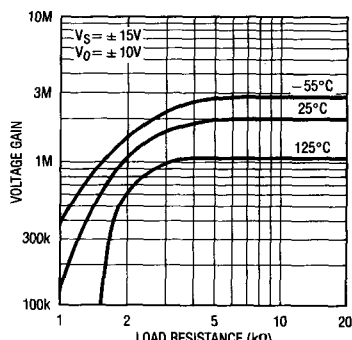
Voltage Gain vs Frequency



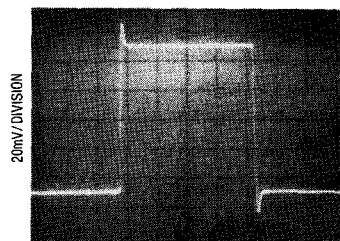
Gain, Phase Shift vs Frequency



Voltage Gain vs Load Resistance

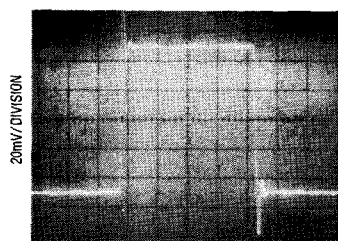


Small Signal Transient Response



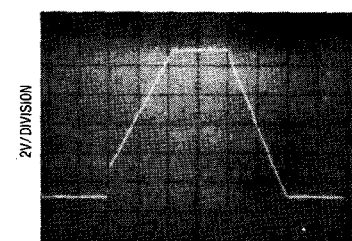
$A_V = +1$, $C_{LOAD} = 100pF$, $5\mu sec/DIV$

Small Signal Transient Response



$A_V = +1$, $C_{LOAD} = 1000pF$, $5\mu sec/DIV$

Large Signal Transient Response



$A_V = +1$, $20\mu sec/DIV$

APPLICATIONS INFORMATION

The LT1024 may be inserted directly into OP-10, OP-207 or OP227 sockets with or without removal of external nulling components.

The LT1024 is specified over a wide range of power supply voltages from $\pm 2V$ to $\pm 18V$. Operation with lower supplies is possible down to $\pm 1.2V$ (two NiCad batteries).

Advantages of Matched Dual Op Amps

In many applications, the performance of a system depends on the matching between two operational amplifiers rather than the individual characteristics of the two op amps. Two or three op amp instrumentation amplifiers, tracking voltage references, and low drift active filters are some of the circuits requiring matching between two op amps.

The well-known triple op amp configuration illustrates these concepts. Output offset is a function of the difference between the offsets of the two halves of the LT1024. This error cancellation principle holds for a considerable number of input-referred parameters in addition to offset voltage and its drift with temperature. Input bias current will be the average of the two non-inverting input currents (I_{B^+}). The difference between these two cur-

rents (I_{OS^+}) is the offset current of the instrumentation amplifier. Common-mode and power supply rejections will be dependent only on the match between the two amplifiers (assuming perfect resistor matching).

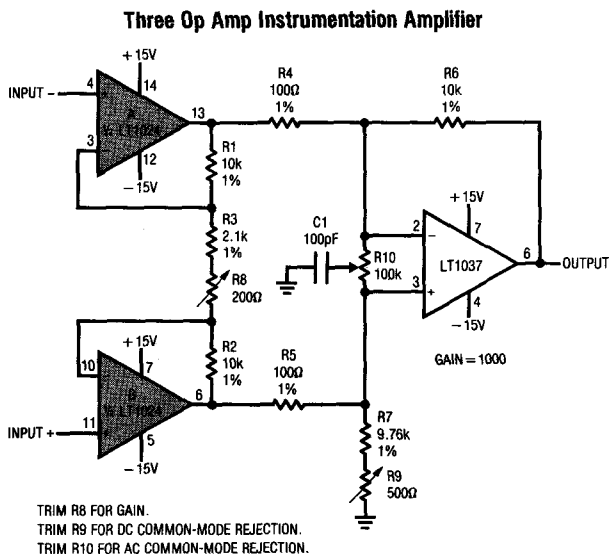
The concepts of common-mode and power supply rejection ratio match ($\Delta CMRR$ and $\Delta PSRR$) are best demonstrated with a numerical example:

Assume $CMRR_A = +1.0\mu V/V$ or 120dB and $CMRR_B = +0.5\mu V/V$ or 126dB, then $\Delta CMRR = 0.5\mu V/V$ or 126dB if $CMRR_B = -0.5\mu V/V$, which is still 126dB, then $\Delta CMRR = 1.5\mu V/V$ or 116.5dB.

Typical performance of the instrumentation amplifier:

- Input offset voltage = $25\mu V$.
- Input bias current = $30pA$.
- Input resistance = $10^{12}\Omega$.
- Input offset current = $30pA$.
- Input noise = $0.7\mu Vp-p$.
- Power bandwidth ($V_0 = \pm 10V$) = 80kHz.

Clearly, the LT1024, by specifying and guaranteeing all of these matching parameters, can significantly improve the performance of matching dependent circuits.



APPLICATIONS INFORMATION

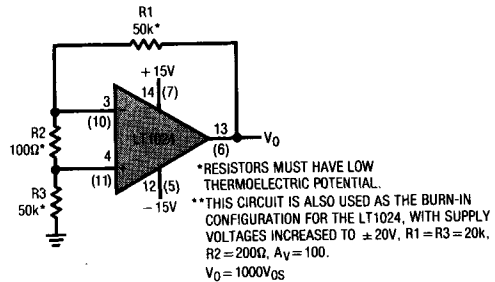
Achieving Picoampere/Microvolt Performance

In order to realize the picoampere/microvolt level accuracy of the LT1024, proper care must be exercised. For example, leakage currents in circuitry external to the op amp can significantly degrade performance. High quality insulation should be used (e.g., Teflon, Kel-F); cleaning of all insulating surfaces to remove fluxes and other residues will probably be required. Surface coating may be necessary to provide a moisture barrier in high humidity environments.

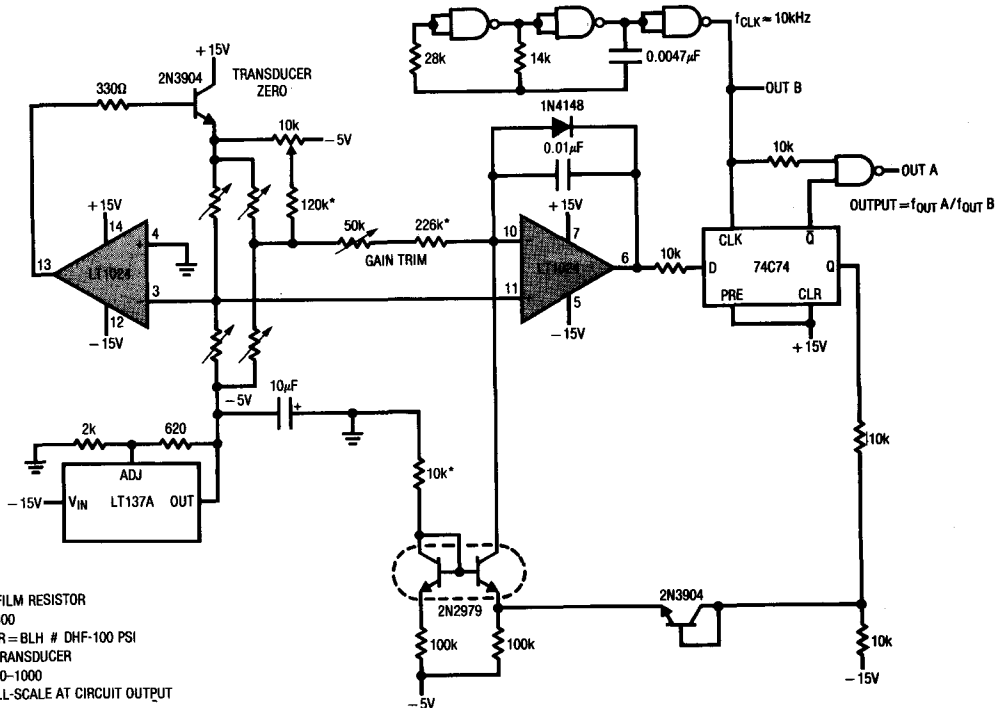
Board leakage can be minimized by encircling the input circuitry with a guard ring operated at a potential close to that of the inputs: in inverting configurations, the guard ring should be tied to ground, in non-inverting connections, to the inverting input. Guarding both sides of the printed circuit board is required. Bulk leakage reduction depends on the guard ring width. Nanoampere level leakage into the offset trim terminals can affect offset voltage and drift with temperature.

Microvolt level error voltages can also be generated in the external circuitry. Thermocouple effects caused by temperature gradients across dissimilar metals at the contacts to the input terminals can exceed the inherent drift of the amplifier. Air currents over device leads should be minimized, package leads should be short, and the two input leads should be as close together as possible and maintained at the same temperature.

Test Circuit for Offset Voltage and its Drift with Temperature

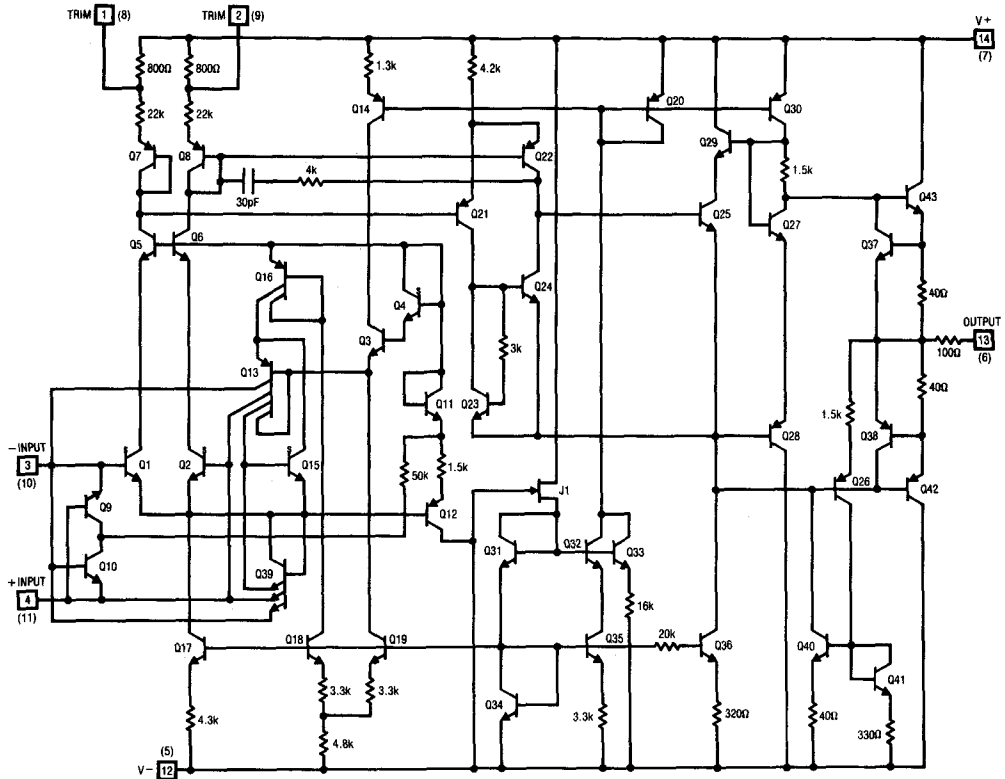


Direct Pressure Transducer to Digital Output Signal Conditioner



SCHEMATIC DIAGRAM

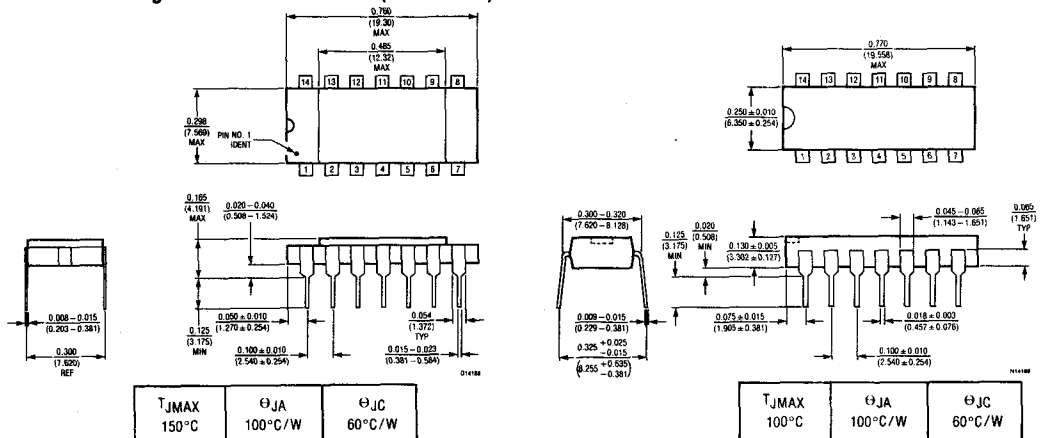
1/2 LT1024



PACKAGE DESCRIPTION

D14 Package 14-Lead Hermetic DIP (Sidebrazed)

N14 Package 14-Lead Plastic



FEATURES

- Voltage Noise 1.1nV/√Hz Max. at 1kHz
0.85nV/√Hz Typ. at 1kHz
1.0nV/√Hz Typ. at 10Hz
35nVp-p Typ., 0.1Hz to 10Hz
- Voltage and Current Noise 100% Tested
- Gain-Bandwidth Product 50MHz Min.
- Slew Rate 11V/μs Min.
- Offset Voltage 40μV Max.
- Voltage Gain 7 Million Min.
- Drift with Temperature 0.8μV/°C Max.

DESCRIPTION

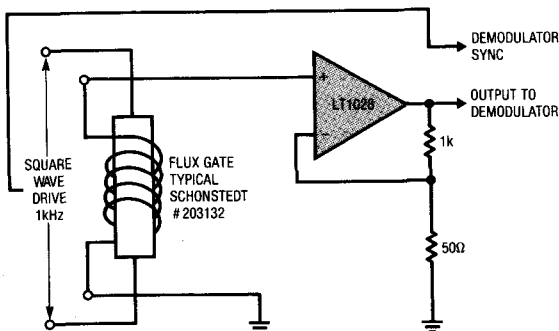
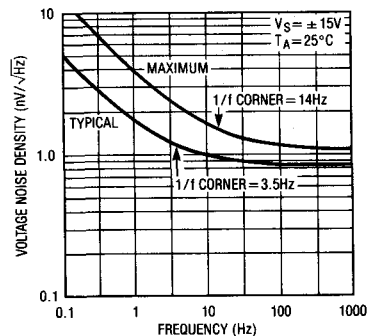
The LT1028 achieves a new standard of excellence in noise performance with 0.85nV/√Hz 1kHz noise, 1.0nV/√Hz 10Hz noise. This ultra low noise is combined with excellent high speed specifications (gain-bandwidth product is 75MHz), distortion free output, and true precision parameters (0.1μV/°C drift, 10μV offset voltage, 30 million voltage gain). Although the LT1028 input stage operates at nearly 1mA of collector currents to achieve low voltage noise, input bias current is only 25nA.

The LT1028's voltage noise is less than the noise of a 50Ω resistor. Therefore, even in very low source impedance transducer or audio amplifier applications, the LT1028's contribution to total system noise will be negligible.

2
APPLICATIONS

- Low Noise Frequency Synthesizers
- High Quality Audio
- Infrared Detectors
- Accelerometer and Gyro Amplifiers
- 350Ω Bridge Signal Conditioning
- Magnetic Resonance Coil Amplifiers
- Hydrophone Amplifier

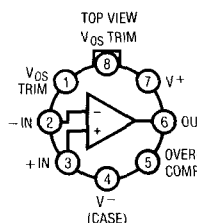
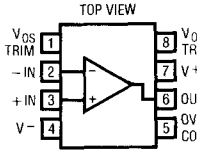
 REFER TO TABLE OF CONTENTS
 FOR REVISED DATA LOCATION

Flux Gate Amplifier

Voltage Noise vs Frequency


ABSOLUTE MAXIMUM RATINGS

Supply Voltage
 -55°C to 105°C ±22V
 105°C to 125°C ±16V
 Differential Input Current (Note 8) ±25mA
 Input Voltage Equal to Supply Voltage
 Output Short Circuit Duration Indefinite
 Operating Temperature Range
 LT1028AM, M -55°C to 125°C
 LT1028AC, C 0°C to 70°C
 Storage Temperature Range
 All Devices -65°C to 150°C
 Lead Temperature (Soldering, 10 sec.) 300°C

PACKAGE/ORDER INFORMATION

	ORDER PART NUMBER
 <p>TOP VIEW V_{OS} TRIM</p> <p>H8 PACKAGE TO-5 METAL CAN</p>	<p>LT1028AMH LT1028MH LT1028ACH LT1028CH</p>
 <p>TOP VIEW V_{OS} TRIM</p> <p>J8 PACKAGE HERMETIC DIP N8 PACKAGE PLASTIC DIP</p>	<p>LT1028AMJ8 LT1028MJ8 LT1028ACJ8 LT1028CJ8 LT1028ACN8 LT1028CN8</p>

ELECTRICAL CHARACTERISTICS V_S = ±15V, T_A = 25°C, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1028AM/AC			LT1028M/C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V _{OS}	Input Offset Voltage	(Note 1)		10	40		20	80	μV
$\frac{\Delta V_{OS}}{\Delta Time}$	Long Term Input Offset Voltage Stability	(Note 2)		0.3			0.3		μV/Mo
I _{OS}	Input Offset Current	V _{CM} = 0V		12	50		18	100	nA
I _B	Input Bias Current	V _{CM} = 0V		±25	±90		±30	±180	nA
e _n	Input Noise Voltage	0.1Hz to 10Hz (Note 3)		35	75		35	90	nVp-p
	Input Noise Voltage Density	f _o = 10Hz (Note 4) f _o = 1000Hz, 100% tested		1.0	1.7		1.0	1.9	nV/√Hz
				0.85	1.1		0.9	1.2	nV/√Hz
i _n	Input Noise Current Density	f _o = 10Hz (Notes 3 and 5) f _o = 1000Hz, 100% tested		4.7	10.0		4.7	12.0	pA/√Hz
				1.0	1.6		1.0	1.8	pA/√Hz
	Input Resistance Common-Mode Differential Mode			300			300		MΩ kΩ
	Input Capacitance			5			5		pF
	Input Voltage Range		±11.0	±12.2		±11.0	±12.2		V
CMRR	Common-Mode Rejection Ratio	V _{CM} = ±11V	114	126		110	126		dB
PSRR	Power Supply Rejection Ratio	V _S = ±4V to ±18V	117	133		110	132		dB
A _{VOL}	Large Signal Voltage Gain	R _L ≥ 2kΩ, V _O = ±12V R _L ≥ 1kΩ, V _O = ±10V R _L ≥ 600Ω, V _O = ±10V	7.0	30.0		5.0	30.0		V/μV
			5.0	20.0		3.5	20.0		V/μV
			3.0	15.0		2.0	15.0		V/μV
V _{OUT}	Maximum Output Voltage Swing	R _L ≥ 2kΩ R _L ≥ 600Ω	±12.3	±13.0		±12.0	±13.0		V
			±11.0	±12.2		±10.5	±12.2		V
SR	Slew Rate	A _{VCL} = -1	11	15		11	15		V/μs
GBW	Gain-Bandwidth Product	f _o = 20kHz (Note 6)	50	75		50	75		MHz
Z _o	Open Loop Output Impedance	V _O = 0, I _O = 0		80			80		Ω
I _S	Supply Current			7.4	9.5		7.6	10.5	mA

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V, -55^\circ C \leq T_A \leq 125^\circ C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1028AM			LT1028M			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	(Note 1)	●	30	120	45	180	μV	
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Input Offset Drift	(Note 7)	●	0.2	0.8	0.25	1.0	$\mu V/^\circ C$	
I_{OS}	Input Offset Current	$V_{CM} = 0V$	●	25	90	30	180	nA	
I_B	Input Bias Current	$V_{CM} = 0V$	●	± 40	± 150	± 50	± 300	nA	
	Input Voltage Range		●	± 10.3	± 11.7	± 10.3	± 11.7	V	
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm 10.3V$	●	106	122	100	120	dB	
PSRR	Power Supply Rejection Ratio	$V_S = \pm 4.5V$ to $\pm 16V$	●	110	130	104	130	dB	
A_{VOL}	Large Signal Voltage Gain	$R_L \geq 2k\Omega, V_O = \pm 10V$ $R_L \geq 1k\Omega, V_O = \pm 10V$	●	3.0 2.0	14.0 10.0	2.0 1.5	14.0 10.0	$V/\mu V$ $V/\mu V$	
V_{OUT}	Maximum Output Voltage Swing	$R_L \geq 2k\Omega$	●	± 10.3	± 11.6	± 10.3	± 11.6	V	
I_S	Supply Current		●	8.7	11.5	9.0	13.0	mA	

2

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V, 0^\circ C \leq T_A \leq 70^\circ C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1028AC			LT1028C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	(Note 1)	●	15	80	30	125	μV	
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Input Offset Drift	(Note 7)	●	0.1	0.8	0.2	1.0	$\mu V/^\circ C$	
I_{OS}	Input Offset Current	$V_{CM} = 0V$	●	15	65	22	130	nA	
I_B	Input Bias Current	$V_{CM} = 0V$	●	± 30	± 120	± 40	± 240	nA	
	Input Voltage Range		●	± 10.5	± 12.0	± 10.5	± 12.0	V	
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm 10.5V$	●	110	124	106	124	dB	
PSRR	Power Supply Rejection Ratio	$V_S = \pm 4.5V$ to $\pm 18V$	●	114	132	107	132	dB	
A_{VOL}	Large Signal Voltage Gain	$R_L \geq 2k\Omega, V_O = \pm 10V$ $R_L \geq 1k\Omega, V_O = \pm 10V$	●	5.0 4.0	25.0 18.0	3.0 2.5	25.0 18.0	$V/\mu V$ $V/\mu V$	
V_{OUT}	Maximum Output Voltage Swing	$R_L \geq 2k\Omega$ $R_L \geq 600\Omega$ (Note 9)	●	± 11.5 ± 9.5	± 12.7 ± 11.0	± 11.5 ± 9.0	± 12.7 ± 10.5	V V	
I_S	Supply Current		●	8.0	10.5	8.2	11.5	mA	

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: Input Offset Voltage measurements are performed by automatic test equipment approximately 0.5 sec. after application of power. In addition, at $T_A = 25^\circ C$, offset voltage is measured with the chip heated to approximately $55^\circ C$ to account for the chip temperature rise when the device is fully warmed up.

Note 2: Long Term Input Offset Voltage Stability refers to the average trend line of Offset Voltage vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 days are typically $2.5\mu V$.

Note 3: This parameter is tested on a sample basis only.

Note 4: 10Hz noise voltage density is sample tested on every lot. Devices 100% tested at 10Hz are available on request.

Note 5: Current noise is defined and measured with balanced source resistors. The resultant voltage noise (after subtracting the resistor noise on an RMS basis) is divided by the sum of the two source resistors to obtain current noise. Maximum 10Hz current noise can be inferred from 100% testing at 1kHz.

Note 6: Gain-bandwidth product is not tested. It is guaranteed by design and by inference from the slew rate measurement.

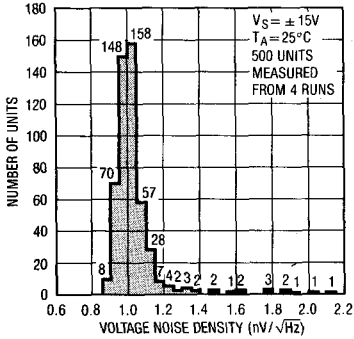
Note 7: This parameter is not 100% tested.

Note 8: The inputs are protected by back-to-back diodes. Current limiting resistors are not used in order to achieve low noise. If differential input voltage exceeds $\pm 1.8V$, the input current should be limited to 25mA.

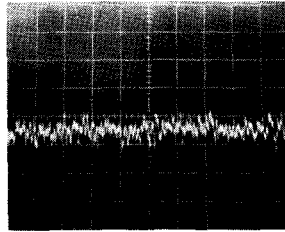
Note 9: This parameter guaranteed by design, fully warmed up at $T_A = 70^\circ C$. It includes chip temperature increase due to supply and load currents.

TYPICAL PERFORMANCE CHARACTERISTICS

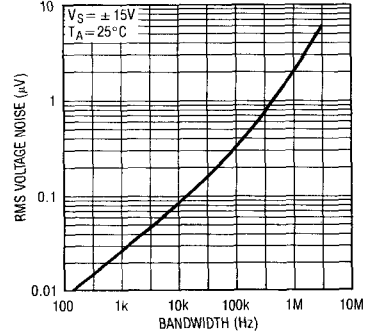
10Hz Voltage Noise Distribution



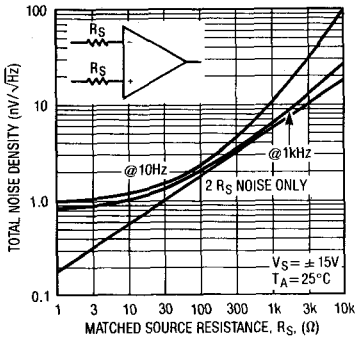
Wideband Noise, DC to 20kHz



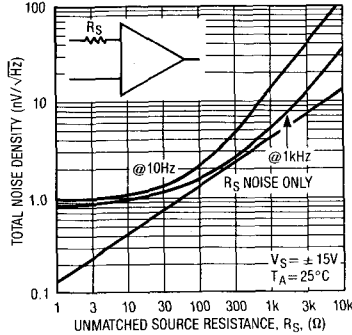
Wideband Voltage Noise (0.1Hz to Frequency Indicated)



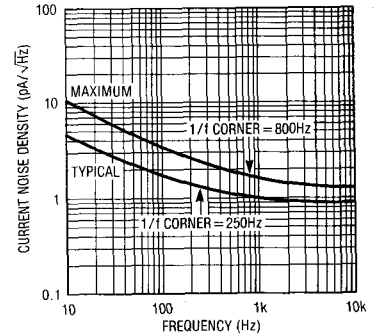
Total Noise vs Matched Source Resistance



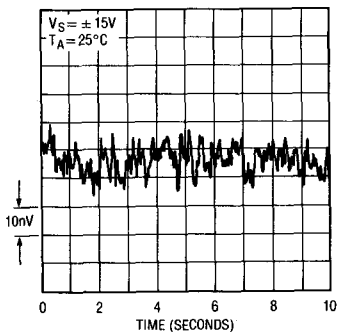
Total Noise vs Unmatched Source Resistance



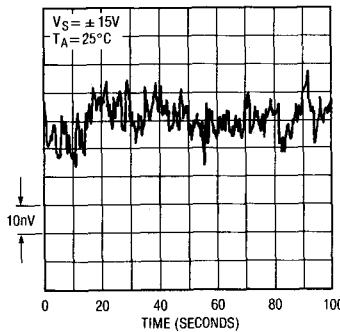
Current Noise Spectrum



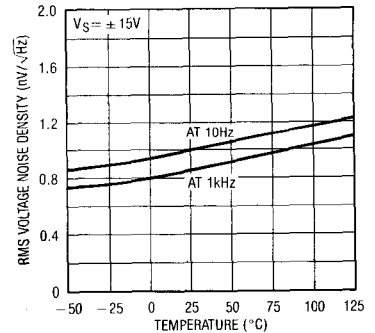
0.1Hz to 10Hz Voltage Noise



0.01Hz to 1Hz Voltage Noise

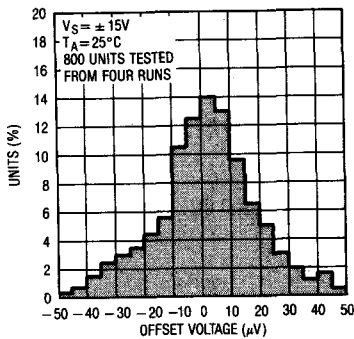


Voltage Noise vs Temperature

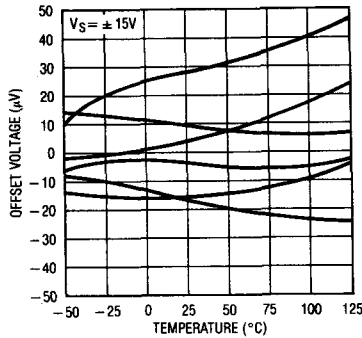


TYPICAL PERFORMANCE CHARACTERISTICS

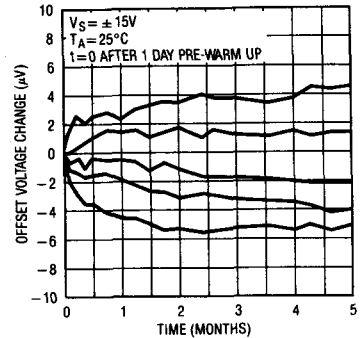
Distribution of Input Offset Voltage



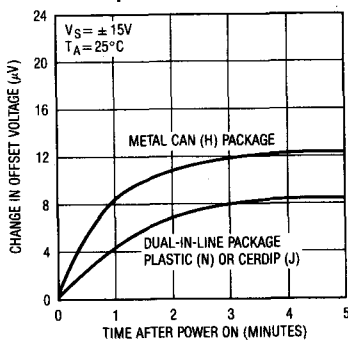
Offset Voltage Drift with Temperature of Representative Units



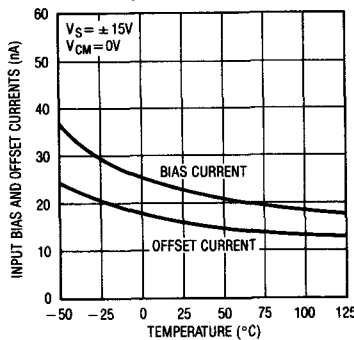
Long Term Stability of Five Representative Units



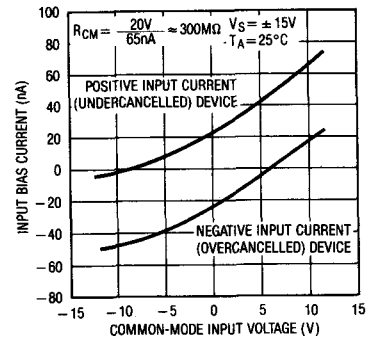
Warm-Up Drift



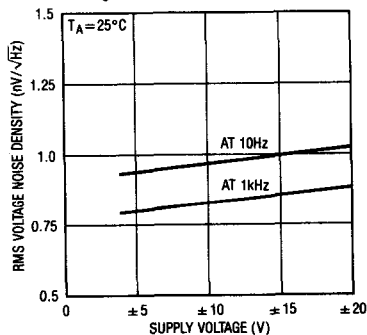
Input Bias and Offset Currents Over Temperature



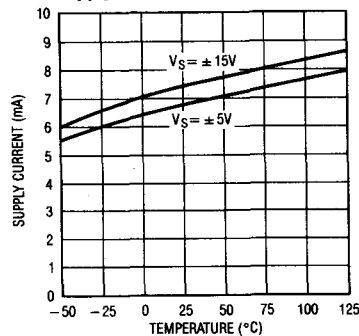
Bias Current Over the Common-Mode Range



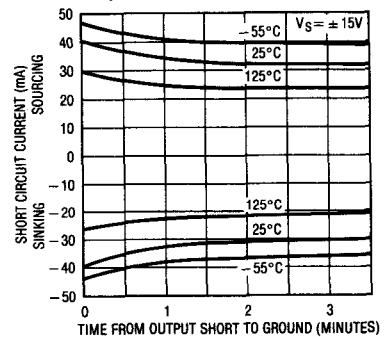
Voltage Noise vs Supply Voltage



Supply Current vs Temperature

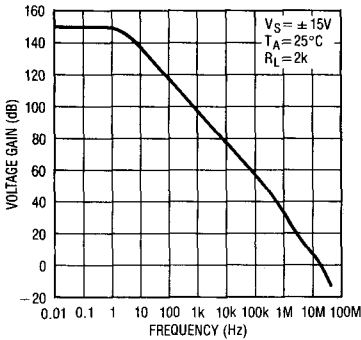


Output Short Circuit Current vs Time

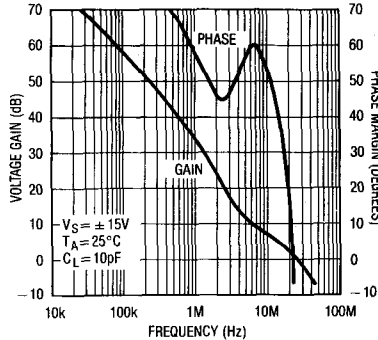


TYPICAL PERFORMANCE CHARACTERISTICS

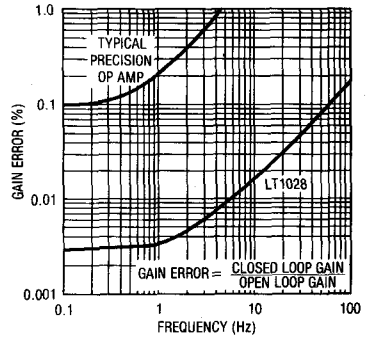
Voltage Gain vs Frequency



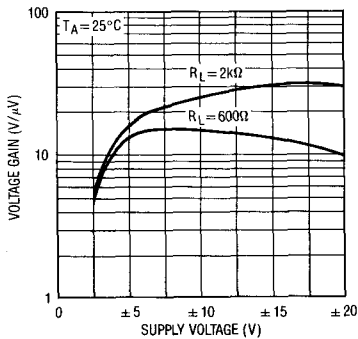
Gain, Phase vs Frequency



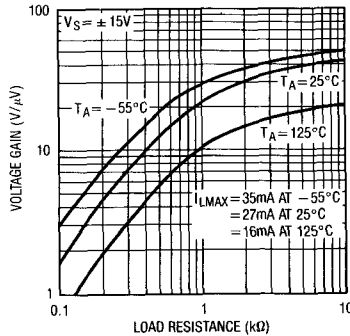
Gain Error vs Frequency
Closed Loop Gain = 1000



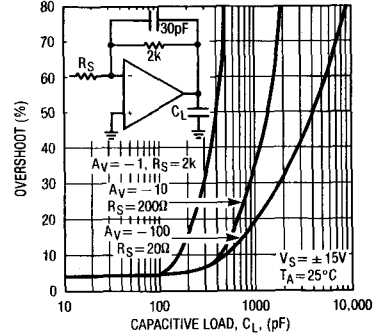
Voltage Gain vs Supply Voltage



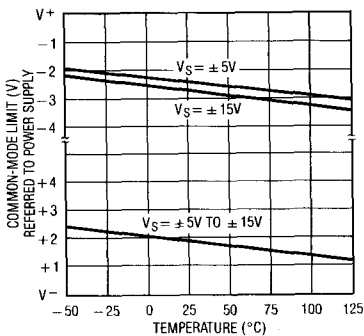
Voltage Gain vs Load Resistance



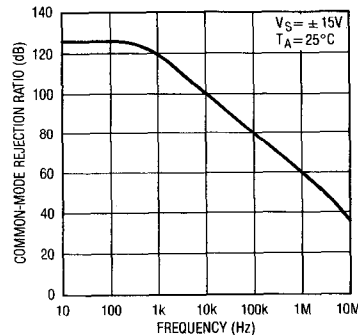
Capacitance Load Handling



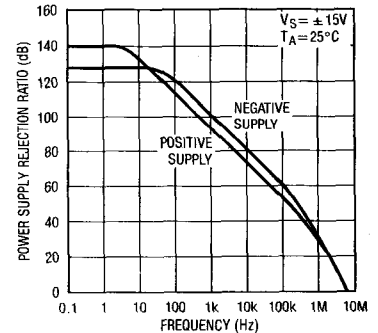
Common-Mode Limit Over Temperature



Common-Mode Rejection Ratio vs Frequency

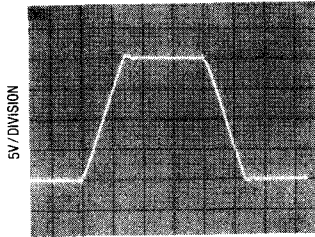


Power Supply Rejection Ratio vs Frequency



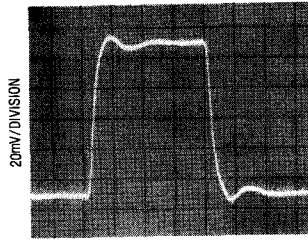
TYPICAL PERFORMANCE CHARACTERISTICS

Large Signal Transient Response



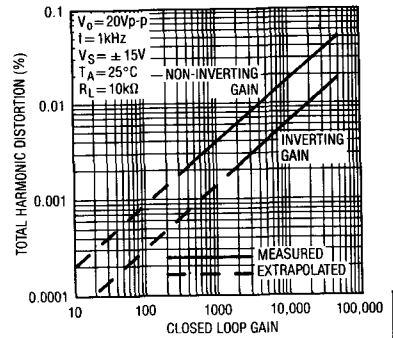
$A_V = -1, R_S = R_L = 2k, C_1 = 30pF$

Small Signal Transient Response



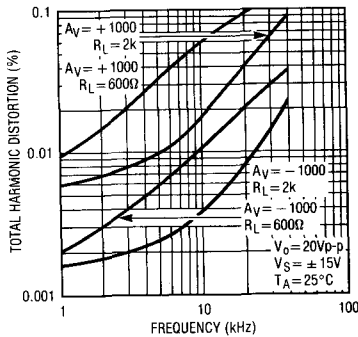
$A_V = -1, R_S = R_L = 2k\Omega$
 $C_1 = 30pF, C_L = 80pF$

Total Harmonic Distortion vs Closed Loop Gain

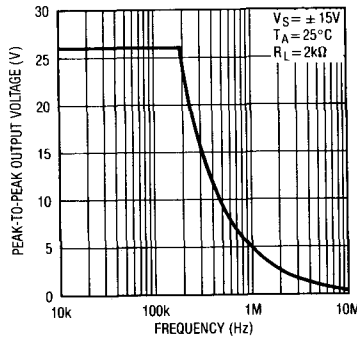


2

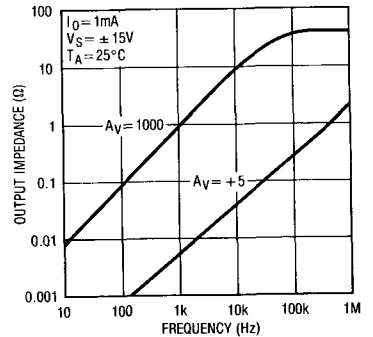
Total Harmonic Distortion vs Frequency and Load Resistance



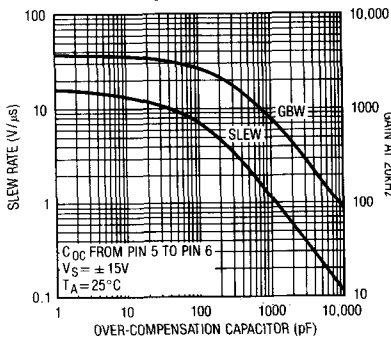
Maximum Undistorted Output vs Frequency



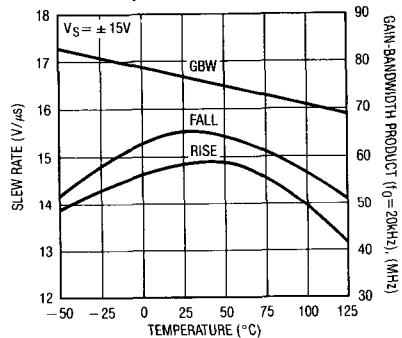
Closed Loop Output Impedance



Slew Rate, Gain-Bandwidth-Product vs Over-Compensation Capacitor



Slew Rate, Gain-Bandwidth Product Over Temperature



APPLICATIONS INFORMATION —NOISE

Voltage Noise vs Current Noise

The LT1028's less than $1\text{nV}/\sqrt{\text{Hz}}$ voltage noise is three times better than the lowest voltage noise heretofore available (on the LT1007/1037). A necessary condition for such low voltage noise is operating the input transistors at nearly 1mA of collector currents, because voltage noise is inversely proportional to the square root of the collector current. Current noise, however, is directly proportional to the square root of the collector current. Consequently, the LT1028's current noise is significantly higher than on most monolithic op amps.

Therefore, to realize truly low noise performance it is important to understand the interaction between voltage noise (e_n), current noise (i_n) and resistor noise (r_n).

Total Noise vs Source Resistance

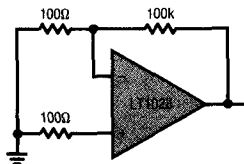
The total input referred noise of an op amp is given by

$$e_t = [e_n^2 + r_n^2 + (i_n R_{eq})^2]^{1/2}$$

where R_{eq} is the total equivalent source resistance at the two inputs

$$\text{and } r_n = \sqrt{4kTR_{eq}} = 0.13\sqrt{R_{eq}} \text{ in nV}/\sqrt{\text{Hz}} \text{ at } 25^\circ\text{C}$$

As a numerical example, consider the total noise at 1kHz of the gain 1000 amplifier shown below.



$$R_{eq} = 100\Omega + 100\Omega \parallel 100k \approx 200\Omega$$

$$r_n = 0.13\sqrt{200} = 1.84\text{nV}/\sqrt{\text{Hz}}$$

$$e_n = 0.85\text{nV}/\sqrt{\text{Hz}}$$

$$i_n = 1.0\text{pA}/\sqrt{\text{Hz}}$$

$$e_t = [0.85^2 + 1.84^2 + (1.0 \times 0.2)^2]^{1/2} = 2.04\text{nV}/\sqrt{\text{Hz}}$$

$$\text{output noise} = 1000 e_t = 2.04\mu\text{V}/\sqrt{\text{Hz}}$$

At very low source resistance ($R_{eq} < 400\Omega$) voltage noise dominates. As R_{eq} is increased resistor noise becomes the largest term—as in the example above—and the LT1028's voltage noise becomes negligible. As R_{eq} is further increased, current noise becomes important. At 1kHz, when R_{eq} is in excess of 20k Ω , the current noise component is larger than the resistor noise. The total noise versus matched source resistance plot illustrates the above calculations.

The plot also shows that current noise is more dominant at low frequencies, such as 10Hz. This is because resistor noise is flat with frequency, while the $1/f$ corner of current noise is typically at 250Hz. At 10Hz when $R_{eq} > 1k\Omega$, the current noise term will exceed the resistor noise.

When the source resistance is unmatched, the total noise versus unmatched source resistance plot should be consulted. Note that total noise is lower at source resistances below 1k Ω because the resistor noise contribution is less. When $R_S > 1k\Omega$ total noise is not improved, however. This is because bias current cancellation is used to reduce input bias current. The cancellation circuitry injects two correlated current noise components into the two inputs. With matched source resistors the injected current noise creates a common-mode voltage noise and gets rejected by the amplifier. With source resistance in one input only, the cancellation noise is added to the amplifier's inherent noise.

In summary, the LT1028 is the optimum amplifier for noise performance—provided that the source resistance is kept low. The following table depicts which op amp manufactured by Linear Technology should be used to minimize noise—as the source resistance is increased beyond the LT1028's level of usefulness.

**Best Op Amp for Lowest Total Noise
vs Source Resistance**

SOURCE RESISTANCE (Note 1)	BEST OP AMP	
	AT LOW FREQ (10Hz)	WIDEBAND (1kHz)
0 to 400 Ω	LT1028	LT1028
400 Ω to 4k Ω	LT1007/1037	LT1028
4k Ω to 40k Ω	LT1001	LT1007/1037
40k Ω to 500k Ω	LT1012	LT1001
500k Ω to 5M Ω	LT1012 or LT1055	LT1012
> 5M	LT1055	LT1055

Note 1: Source resistance is defined as matched or unmatched, e.g., $R_S = 1k\Omega$ means: 1k Ω at each input, or 1k Ω at one input and zero at the other.

APPLICATIONS INFORMATION — NOISE

Noise Testing—Voltage Noise

The LT1028's RMS voltage noise density can be accurately measured using the Quan Tech Noise Analyzer, Model 5173 or an equivalent noise tester. Care should be taken, however, to subtract the noise of the source resistor used. Prefabricated test cards for the Model 5173 set the device under test in a closed loop gain of 31 with a 60Ω source resistor and a 1.8kΩ feedback resistor. The noise of this resistor combination is $0.13\sqrt{58} = 1.0\text{nV}/\sqrt{\text{Hz}}$. An LT1028 with $0.85\text{nV}/\sqrt{\text{Hz}}$ noise will read $(0.85^2 + 1.0^2)^{1/2} = 1.31\text{nV}/\sqrt{\text{Hz}}$. For better resolution, the resistors should be replaced with a 10Ω source and 300Ω feedback resistor. Even a 10Ω resistor will show an apparent noise which is 8–10% too high.

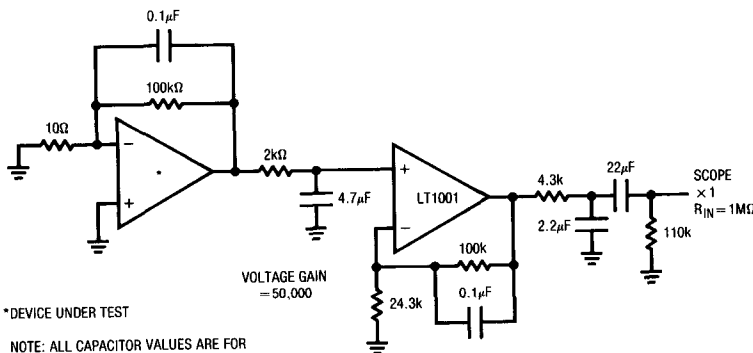
The 0.1Hz to 10Hz peak-to-peak noise of the LT1028 is measured in the test circuit shown. The frequency response of this noise tester indicates that the 0.1Hz corner is defined by only one zero. The test time to measure 0.1Hz to 10Hz noise should not exceed 10 seconds, as this time limit acts as an additional zero to eliminate noise contributions from the frequency band below 0.1Hz.

Measuring the typical 35nV peak-to-peak noise performance of the LT1028 requires special test precautions:

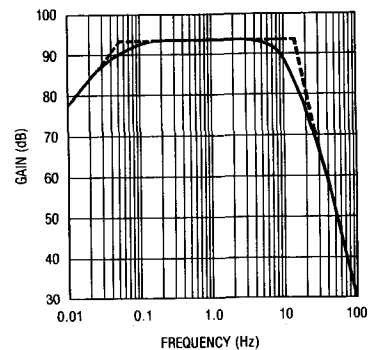
- (a) The device should be warmed up for at least five minutes. As the op amp warms up, its offset voltage changes typically $10\mu\text{V}$ due to its chip temperature increasing 30°C to 40°C from the moment the power supplies are turned on. In the 10 second measurement interval these temperature-induced effects can easily exceed tens of nanovolts.
- (b) For similar reasons, the device must be well shielded from air currents to eliminate the possibility of thermoelectric effects in excess of a few nanovolts, which would invalidate the measurements.
- (c) Sudden motion in the vicinity of the device can also "feedthrough" to increase the observed noise.

A noise-voltage density test is recommended when measuring noise on a large number of units. A 10Hz noise-voltage density measurement will correlate well with a 0.1Hz to 10Hz peak-to-peak noise reading since both results are determined by the white noise and the location of the 1/f corner frequency.

0.1Hz to 10Hz Noise Test Circuit



0.1Hz to 10Hz p-p Noise Tester Frequency Response



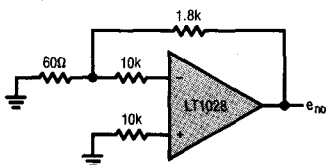
APPLICATIONS INFORMATION

—NOISE

Noise Testing—Current Noise

Current noise density (i_n) is defined by the following formula, and can be measured in the circuit shown:

$$i_n = \frac{[e_{no}^2 - (31 \times 18.4nV/\sqrt{Hz})^2]^{1/2}}{20k \times 31}$$



If the Quan Tech Model 5173 is used, the noise reading is input-referred, therefore the result should not be divided by 31; the resistor noise should not be multiplied by 31.

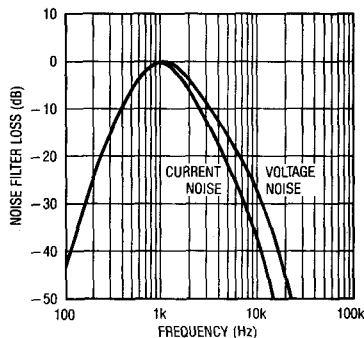
100% Noise Testing

The 1kHz voltage and current noise is 100% tested on the LT1028 as part of automated testing; the approximate frequency response of the filters is shown. The limits on the automated testing are established by extensive correlation tests on units measured with the Quan Tech Model 5173.

10Hz voltage noise density is sample tested on every lot. Devices 100% tested at 10Hz are available on request for an additional charge.

10Hz current noise is not tested on every lot but it can be inferred from 100% testing at 1kHz. A look at the current noise spectrum plot will substantiate this statement. The only way 10Hz current noise can exceed the guaranteed limits is if its 1/f corner is higher than 800Hz and/or its white noise is high. If that is the case then the 1kHz test will fail.

Automated Tester Noise Filter



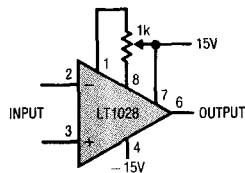
APPLICATIONS INFORMATION

General

The LT1028 series devices may be inserted directly into OP-07, OP-27, OP-37, LT1007 and LT1037 sockets with or without removal of external nulling components. In addition, the LT1028 may be fitted to 5534 sockets with the removal of external compensation components.

Offset Voltage Adjustment

The input offset voltage of the LT1028 and its drift with temperature, are permanently trimmed at wafer testing to a low level. However, if further adjustment of V_{OS} is necessary, the use of a 1k nulling potentiometer will not degrade drift with temperature. Trimming to a value other than zero creates a drift of $(V_{OS}/300) \mu V/^\circ C$, e.g., if V_{OS} is adjusted to $300 \mu V$, the change in drift will be $1 \mu V/^\circ C$.



The adjustment range with a 1k pot is approximately $\pm 1.1mV$.

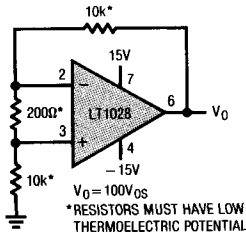
Offset Voltage and Drift

Thermocouple effects, caused by temperature gradients across dissimilar metals at the contacts to the input terminals, can exceed the inherent drift of the amplifier unless proper care is exercised. Air currents should be minimized, package leads should be short, the two input leads should be close together and maintained at the same temperature.

APPLICATIONS INFORMATION

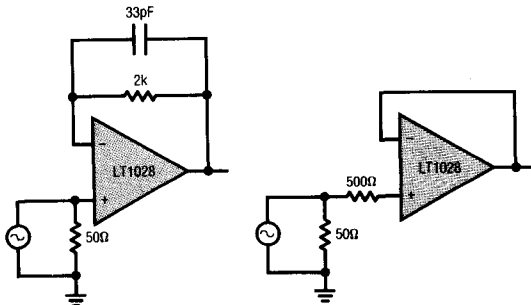
The circuit shown to measure offset voltage is also used as the burn-in configuration for the LT1028.

Test Circuit for Offset Voltage and Offset Voltage Drift with Temperature

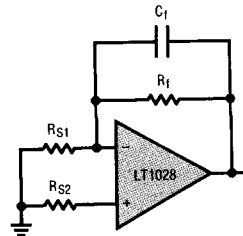


Frequency Response

The LT1028's Gain, Phase vs Frequency plot indicates that the device is stable in closed loop gains greater than +2 or -1 because phase margin is about 50° at an open loop gain of 6dB. In the voltage follower configuration phase margin seems inadequate. This is indeed true when the output is shorted to the inverting input and the non-inverting input is driven from a 50Ω source impedance. However, when feedback is through a parallel R-C network (provided $C_f < 68\text{pF}$), the LT1028 will be stable because of interaction between the input resistance and capacitance and the feedback network. Larger source resistance at the non-inverting input has a similar effect. The following voltage follower configurations are stable:



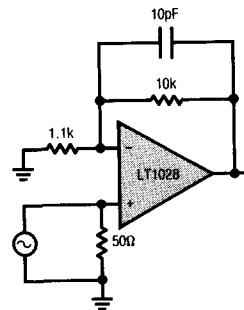
Another configuration which requires unity gain stability is shown below. When C_f is large enough to effectively short the output to the input at 15MHz, oscillations can occur. The insertion of $R_{S2} \geq 500\Omega$ will prevent the LT1028 from oscillating. When $R_{S1} \geq 500\Omega$, the additional noise contribution due to the presence of R_{S2} will be minimal. When $R_{S1} \leq 100\Omega$, R_{S2} is not necessary, because R_{S1} represents a heavy load on the output through the C_f short. When $100\Omega < R_{S1} < 500\Omega$, R_{S2} should match R_{S1} . For example, $R_{S1} = R_{S2} = 300\Omega$ will be stable. The noise increase due to R_{S2} is 40%.



2

If C_f is only used to cut noise bandwidth, a similar effect can be achieved using the over-compensation terminal.

The Gain, Phase plot also shows that phase margin is about 45° at a gain of 10 (20dB). The following configuration has a high (~70%) overshoot without the 10pF capacitor because of additional phaseshift caused by the feedback resistor—input capacitance pole. The presence of the 10pF capacitor cancels this pole and reduces overshoot to 5%.

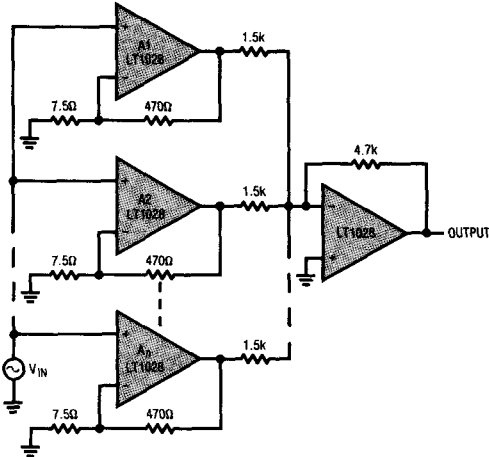


Over-Compensation

The LT1028 is equipped with a frequency over-compensation terminal (pin 5). A capacitor connected between pin 5 and the output will reduce noise bandwidth. Details are shown on the Slew Rate, Gain-Bandwidth Product vs Over-Compensation Capacitor plot. An additional benefit is increased capacitive load handling capability.

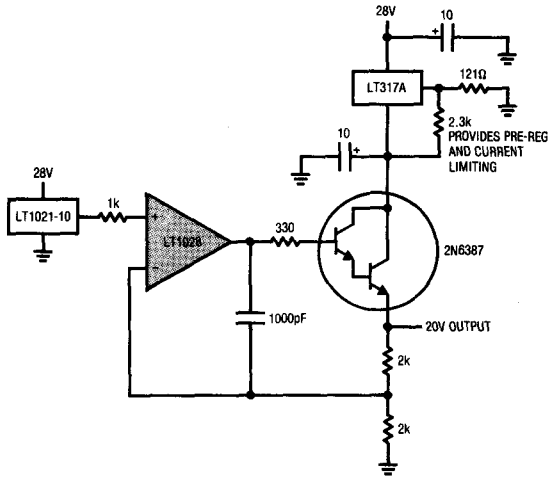
TYPICAL APPLICATIONS

Paralleling Amplifiers to Reduce Voltage Noise

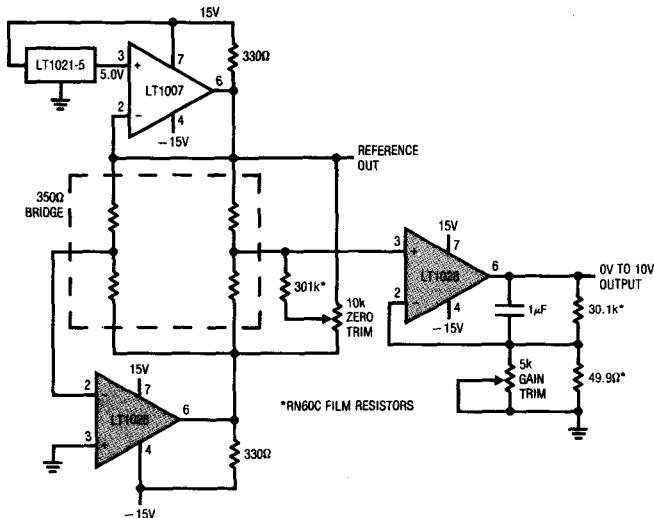


1. ASSUME VOLTAGE NOISE OF LT1028 AND 7.5Ω SOURCE RESISTOR = $0.9\text{nV}/\sqrt{\text{Hz}}$.
2. GAIN WITH n LT1028'S IN PARALLEL = $n \times 200$.
3. OUTPUT NOISE = $\sqrt{n} \times 200 \times 0.9\text{nV}/\sqrt{\text{Hz}}$.
4. INPUT REFERRED NOISE = $\frac{\text{OUTPUT NOISE}}{n \times 200} = 0.9 \text{ nV}/\sqrt{\text{Hz}}$.
5. NOISE CURRENT AT INPUT INCREASES \sqrt{n} TIMES.
6. IF $n=5$, GAIN = 1000, BANDWIDTH = 1MHz, RMS NOISE, DC TO 1MHz, = $\frac{2\mu\text{V}}{\sqrt{5}} = 0.9\mu\text{V}$.

Low Noise Voltage Regulator



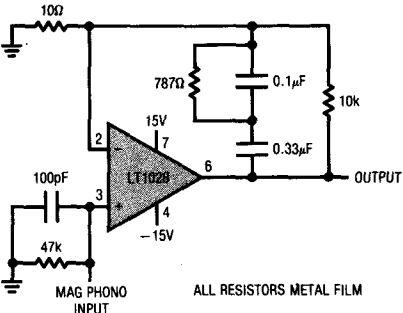
Strain Gauge Signal Conditioner with Bridge Excitation



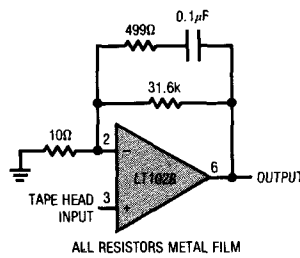
THE LT1028'S NOISE CONTRIBUTION IS NEGLIGIBLE COMPARED TO THE BRIDGE NOISE.

TYPICAL APPLICATIONS

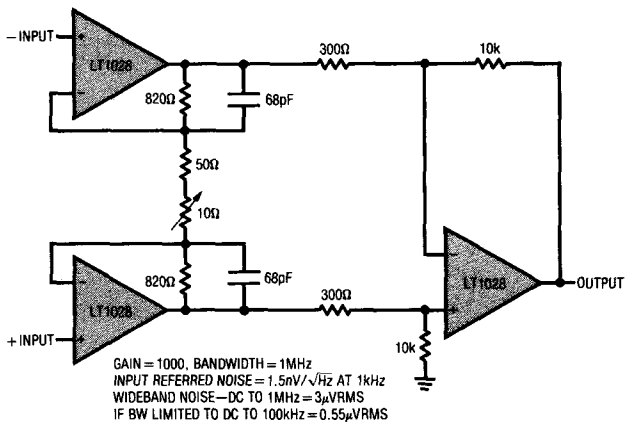
Phono Preamplifier



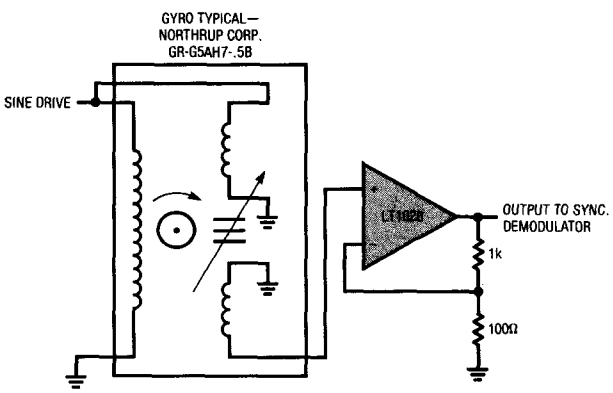
Tape Head Amplifier



Low Noise, Wide Bandwidth Instrumentation Amplifier



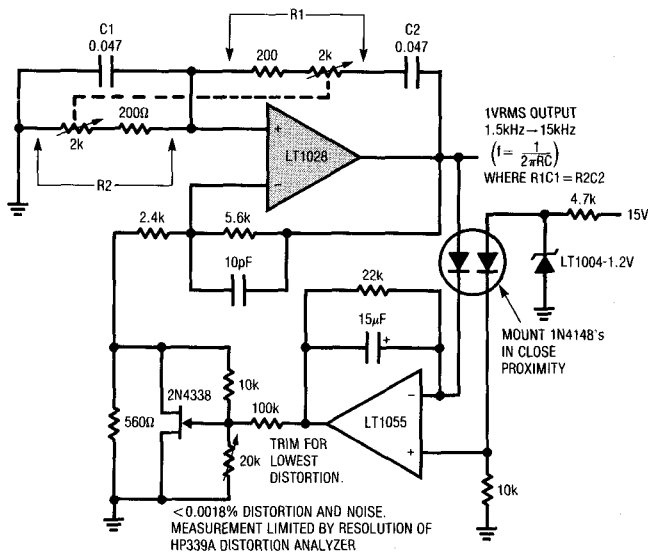
Gyro Pick-Off Amplifier



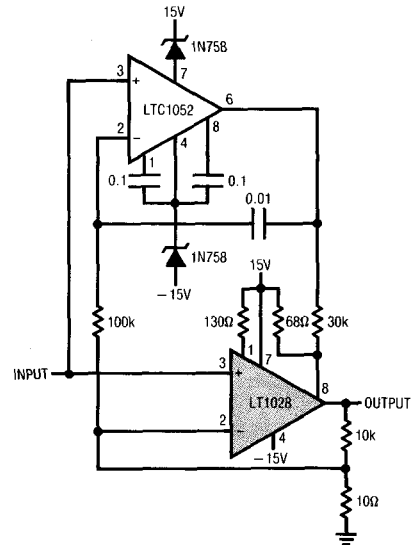
2

TYPICAL APPLICATIONS

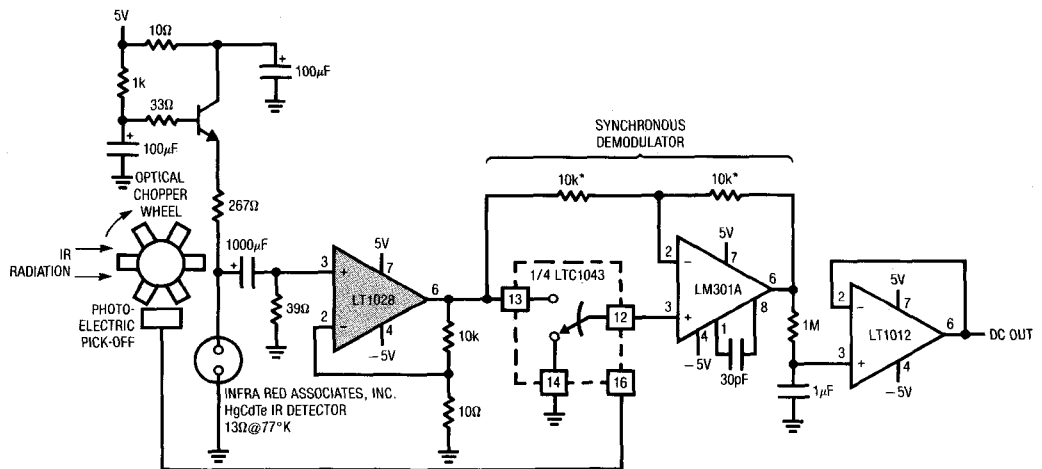
Super Low Distortion Variable Sine Wave Oscillator



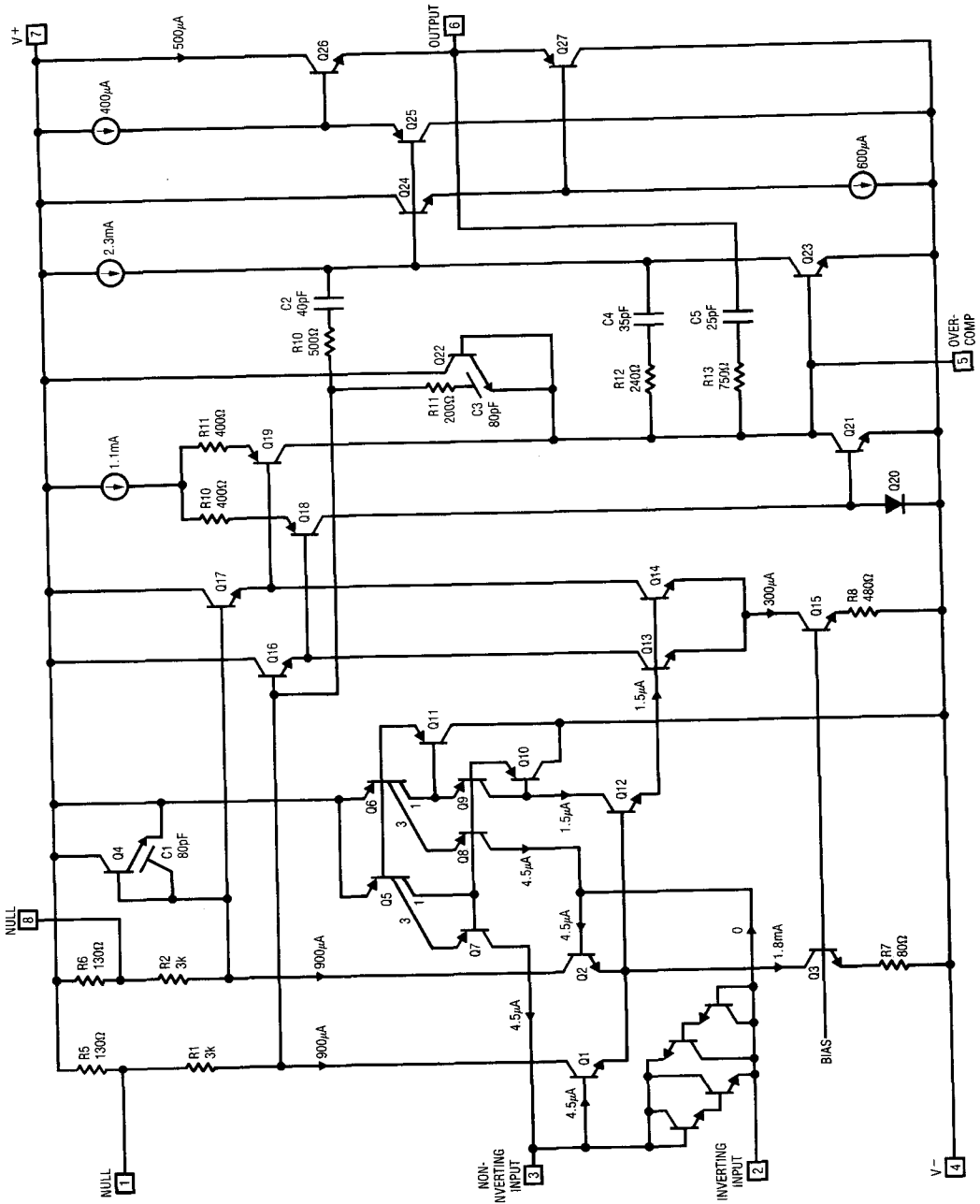
Chopper Stabilized Amplifier



Low Noise Infrared Detector

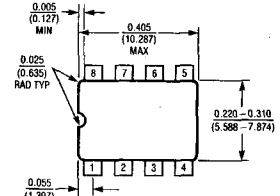
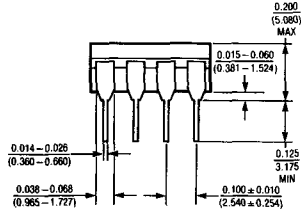
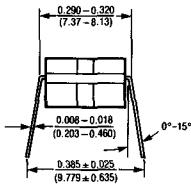


SCHEMATIC DIAGRAM



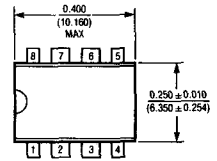
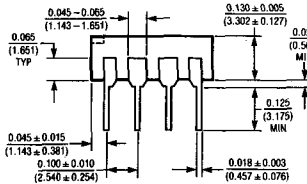
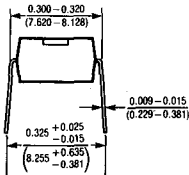
PACKAGE DESCRIPTIONS Dimensions in inches (millimeters) unless otherwise noted.

J Package
8-Lead Ceramic DIP



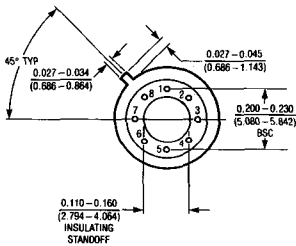
T_{max}	θ_{JA}
165°C	100°C/W

N Package
8-Lead Plastic DIP

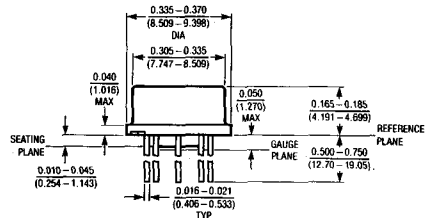


T_{max}	θ_{JA}
115°C	130°C/W

H Package
8-Lead TO-5 Metal Can



NOTE: LEAD DIAMETER IS UNCONTROLLED BETWEEN THE REFERENCE PLANE AND SEATING PLANE.



T_{max}	θ_{JA}	θ_{JC}
175°C	140°C/W	40°C/W

FEATURES

- Voltage Noise
 - 1.2nV/√Hz Max. at 1kHz
 - 0.9nV/√Hz Typ. at 1kHz
 - 1.0nV/√Hz Typ. at 10Hz
 - 35nVp-p Typ., 0.1Hz to 10Hz
- Voltage and Current Noise 100% Tested
- Gain-Bandwidth Product 50MHz Min.
- Slew Rate 11V/μs Min.
- Offset Voltage 80μV Max.
- Voltage Gain 5 Million Min.
- Drift with Temperature 1μV/°C Max.

DESCRIPTION

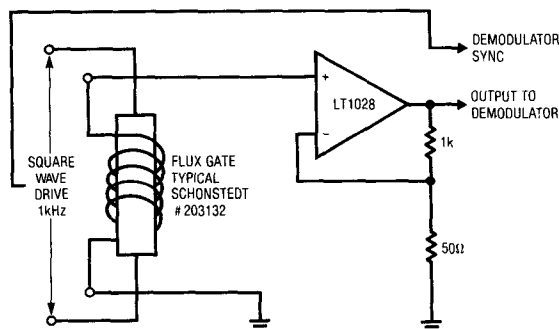
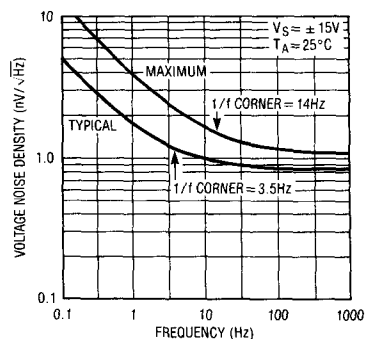
The LT1028 achieves a new standard of excellence in noise performance with 0.9nV/√Hz 1kHz noise, 1.0nV/√Hz 10Hz noise. This ultra low noise is combined with excellent high speed specifications (gain-bandwidth product is 75MHz), distortion free output, and true precision parameters (0.2μV/°C drift, 20μV offset voltage, 30 million voltage gain). Although the LT1028 input stage operates at nearly 1mA of collector currents to achieve low voltage noise, input bias currents are only 30nA.

The LT1028's voltage noise is less than the noise of a 50Ω resistor. Therefore, even in very low source impedance transfer function audio amplifier applications, the LT1028's contribution to total system noise will be negligible.

APPLICATIONS

- Low Noise Frequency Synthesizers
- High Quality Audio
- Infrared Detectors
- Accelerometer Output Amplifiers
- 350Ω Bridge Signal Conditioning
- Magnetic Search Coil Amplifiers
- Hydrophone Amplifiers

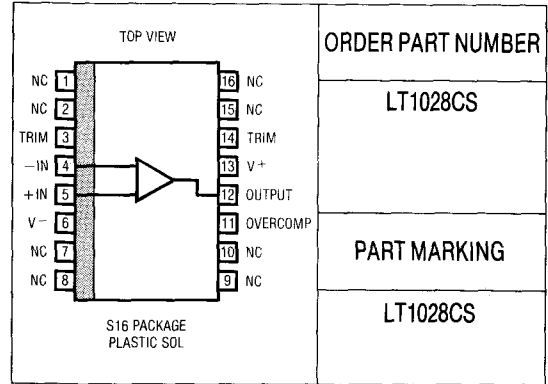
 REFER TO TABLE OF CONTENTS
 FOR REVISED DATA LOCATION

Flux Gate Amplifier

Voltage Noise vs Frequency


ABSOLUTE MAXIMUM RATINGS

Supply Voltage $\pm 22\text{V}$
 Differential Input Current (Note 4) $\pm 25\text{mA}$
 Input Voltage Equal to Supply Voltage
 Output Short Circuit Duration Indefinite
 Operating Temperature Range 0°C to 70°C
 Storage Temperature Range
 All Devices -65°C to 150°C
 Lead Temperature (Soldering, 10 sec.) 300°C

PACKAGE/ORDER INFORMATION



ELECTRICAL CHARACTERISTICS $V_S = \pm 15\text{V}$, $T_A = 25^\circ\text{C}$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1028CS			UNITS
			MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	(Note 1)		20	80	μV
$\frac{\Delta V_{OS}}{\Delta \text{Time}}$	Long Term Input Offset Voltage Stability	(Note 2)		0.3		$\mu\text{V/Mo}$
I_{OS}	Input Offset Current	$V_{CM} = 0\text{V}$		18	100	nA
I_B	Input Bias Current	$V_{CM} = 0\text{V}$		± 30	± 180	nA
e_n	Input Noise Voltage	0.1Hz to 10Hz (Note 3)		35	90	nVp-p
	Input Noise Voltage Density	$f_o = 10\text{Hz}$ (Note 3) $f_o = 1000\text{Hz}$, 100% tested		1.0	1.9	$\text{nV}/\sqrt{\text{Hz}}$
				0.9	1.2	$\text{nV}/\sqrt{\text{Hz}}$
i_n	Input Noise Current Density	$f_o = 10\text{Hz}$ (Notes 3 and 5) $f_o = 1000\text{Hz}$, 100% tested		4.7	12.0	$\text{pA}/\sqrt{\text{Hz}}$
				1.0	1.8	$\text{pA}/\sqrt{\text{Hz}}$
	Input Resistance Common-Mode Differential Mode			300		$\text{M}\Omega$
				20		$\text{k}\Omega$
	Input Capacitance			5		pF
	Input Voltage Range		± 11.0	± 12.2		V
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm 11\text{V}$	110	126		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 4\text{V}$ to $\pm 18\text{V}$	110	132		dB
A_{VOL}	Large Signal Voltage Gain	$R_L \geq 2\text{k}\Omega$, $V_o = \pm 12\text{V}$	5.0	30.0		$\text{V}/\mu\text{V}$
		$R_L \geq 1\text{k}\Omega$, $V_o = \pm 10\text{V}$	3.5	20.0		$\text{V}/\mu\text{V}$
		$R_L \geq 600\Omega$, $V_o = \pm 10\text{V}$	2.0	15.0		$\text{V}/\mu\text{V}$
V_{OUT}	Maximum Output Voltage Swing	$R_L \geq 2\text{k}\Omega$	± 12.0	± 13.0		V
		$R_L \geq 600\Omega$	± 10.5	± 12.2		V
SR	Slew Rate	$A_{VOL} = -1$	11	15		$\text{V}/\mu\text{s}$
GBW	Gain-Bandwidth Product	$f_o = 20\text{kHz}$ (Note 6)	50	75		MHz
Z_o	Open Loop Output Impedance	$V_o = 0$, $I_o = 0$		80		Ω
I_S	Supply Current		7.6	10.5		mA

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V, 0^\circ C \leq T_A \leq 70^\circ C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1028CS			UNITS
			MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	(Note 1)	●	30	125	μV
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Input Offset Drift	(Note 7)	●	0.2	1.0	$\mu V/^\circ C$
I_{OS}	Input Offset Current	$V_{CM} = 0V$	●	22	130	nA
I_B	Input Bias Current	$V_{CM} = 0V$	●	± 40	± 240	nA
	Input Voltage Range		●	± 10.5	± 12.0	V
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm 10.5V$	●	106	124	dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 4.5V$ to $\pm 18V$	●	107	132	dB
A_{VOL}	Large Signal Voltage Gain	$R_L \geq 2k\Omega, V_O = \pm 10V$ $R_L \geq 1k\Omega, V_O = \pm 10V$	●	3.0 2.5	25.0 18.0	$V/\mu V$ $V/\mu V$
V_{OUT}	Maximum Output Voltage Swing	$R_L \geq 2k\Omega$	●	± 11.5	± 12.7	V
I_S	Supply Current		●	8.2	11.5	mA

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: Input Offset Voltage measurements are performed by automatic test equipment approximately 0.5 sec. after application of power. In addition, at $T_A = 25^\circ C$, offset voltage is measured with the chip heated to approximately $55^\circ C$ to account for the chip temperature rise when the device is fully warmed up.

Note 2: Long Term Input Offset Voltage Stability refers to the average trend line of Offset Voltage vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 days are typically $2.5\mu V$.

Note 3: This parameter is tested on a sample basis only.

Note 4: The inputs are protected by back-to-back diodes. Current limiting resistors are not used in order to achieve low noise. If differential input voltage exceeds $\pm 1.8V$, the input current should be limited to 25mA.

Note 5: Current noise is defined and measured with balanced source resistors. The resultant voltage noise (after subtracting the resistor noise on an RMS basis) is divided by the sum of the two source resistors to obtain current noise. Maximum 10Hz current noise can be inferred from 100% testing at 1kHz.

Note 6: Gain-bandwidth product is not tested. It is guaranteed by design and by inference from the slew rate measurement.

Note 7: This parameter is not 100% tested.

NOTES

Precision Chopper Stabilized Operational Amplifier With Internal Capacitors

FEATURES

- No External Components Required
- Noise Tested and Guaranteed
- Low Aliasing Errors
- Maximum Offset Voltage $5\mu\text{V}$
- Maximum Offset Voltage Drift $0.5\mu\text{V}/^\circ\text{C}$
- Low Noise $1.6\mu\text{V}_{\text{p-p}}$ (0.1Hz to 10Hz)
- Minimum Voltage Gain, 130dB
- Minimum PSRR, 125dB
- Minimum CMRR, 120dB
- Low Supply Current 1mA
- Single Supply Operation 4.75V to 16V
- Input Common Mode Range Includes Ground
- Output Swings to Ground
- Typical Overload Recovery Time 3ms

APPLICATIONS

- Thermocouple Amplifiers
- Electronic Scales
- Medical Instrumentation
- Strain Gauge Amplifiers
- High Resolution Data Acquisition
- DC Accurate R, C Active Filters

DESCRIPTION

The LTC1050 is a high performance, low cost chopper stabilized operational amplifier. The unique achievement of the LTC1050 is that it integrates on chip the two sample-and-hold capacitors usually required externally by other chopper amplifiers. Further, the LTC1050 offers better combined overall DC and AC performance than is available from other chopper stabilized amplifiers with or without internal sample/hold capacitors.

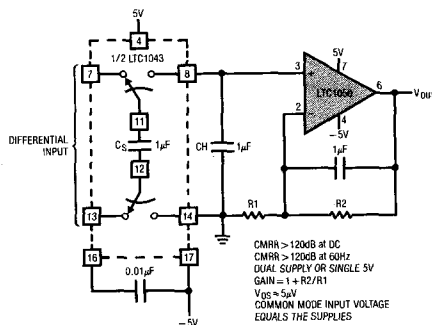
The LTC1050 has an offset voltage of $0.5\mu\text{V}$, drift of $0.01\mu\text{V}/^\circ\text{C}$, DC to 10Hz, input noise voltage of $1.6\mu\text{V}_{\text{p-p}}$ and a typical voltage gain of 160dB. The slew rate of $4\text{V}/\mu\text{s}$ and a gain bandwidth product of 2.5MHz are achieved with only 1mA of supply current.

Overload recovery times from positive and negative saturation conditions are 1.5ms and 3ms respectively, which represents an improvement of about 100 times over chopper amplifiers using external capacitors. Pin 5 is an optional external clock input, useful for synchronization purposes.

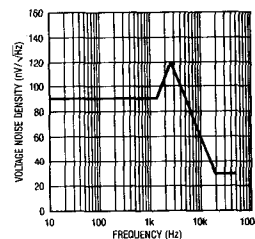
The LTC1050 is available in standard 8-pin metal can, plastic and ceramic dual in line packages as well as an 8-pin SO8 package. The LTC1050 can be an improved plug in replacement for most standard op amps.

TYPICAL APPLICATION

High Performance Low Cost Instrumentation Amplifier



Noise Spectrum



LTC1050

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Total Supply Voltage ($V+$ to $V-$)	18V
Input Voltage	($V+ + 0.3V$) to ($V- - 0.3V$)
Output Short Circuit Duration	Indefinite

Operating Temperature Range

LTC1050 AM/M	-55°C to 125°C
LTC1050 AC/C	-40°C to 85°C
Storage Temperature Range	-65°C to 150°C
Lead Temperature (Soldering, 10 sec.)	300°C

PACKAGE/ORDER INFORMATION

TOP VIEW	ORDER PART NUMBER	TOP VIEW	ORDER PART NUMBER
<p>8 LEAD METAL CAN</p>	LTC1050AMH LTC1050MH LTC1050ACH LTC1050CH	<p>8 LEAD PLASTIC SOIC</p>	LTC1050CS8
<p>14 LEAD PLASTIC DIP</p>	LTC1050AMJ8 LTC1050MJ8 LTC1050ACJ8 LTC1050CJ8 LTC1050ACN8 LTC1050CN8		LTC1050ACN LTC1050CN

ELECTRICAL CHARACTERISTICS

$V_S = \pm 5V$, $T_A =$ operating temperature range unless otherwise specified.

PARAMETER	CONDITIONS	LTC1050AM			LTC1050AC			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$T_A = 25^\circ\text{C}$ (Note 3)		± 0.5	± 5	± 0.5	± 5		μV
Average Input Offset Drift	(Note 3)	●	± 0.01	± 0.05	± 0.01	± 0.05		$\mu\text{V}/^\circ\text{C}$
Long Term Offset Voltage Drift			50		50			$\text{nV}/\sqrt{\text{Mo}}$
Input Offset Current	$T_A = 25^\circ\text{C}$ (Note 5)	●	± 20	± 60 ± 150	± 20	± 60 ± 150		pA
Input Bias Current	$T_A = 25^\circ\text{C}$ (Note 5)	●	± 10	± 30 ± 800	± 10	± 30 ± 100		pA
Input Noise Voltage	0.1Hz to 10Hz (Note 6) DC to 1Hz		1.6 0.6	2.1	1.6 0.6	2.1		μV_{pp} μV_{pp}
Input Noise Current	$f = 10\text{Hz}$ (Note 4)		2.2		2.2			$\text{fA}/\sqrt{\text{Hz}}$
Common Mode Rejection Ratio	$V_{\text{CM}} = V- \text{ to } +2.7V$, $T_A = 25^\circ\text{C}$	●	120 120	140	120 120	140		dB dB
Power Supply Rejection Ratio	$V_S = \pm 2.375V$ to $\pm 8V$	●	125	140	125	140		dB
Large Signal Voltage Gain	$R_L = 10\text{k}\Omega$, $V_{\text{OUT}} = \pm 4V$	●	130	160	130	160		dB
Maximum Output Voltage Swing	$R_L = 10\text{k}\Omega$ $R_L = 100\text{k}\Omega$	●	± 4.7	± 4.85 ± 4.95	± 4.7	± 4.85 ± 4.95		V V
Slew Rate	$R_L = 10\text{k}\Omega$, $C_L = 50\text{pF}$		4		4			$\text{V}/\mu\text{s}$
Gain Bandwidth Product			2.5		2.5			MHz
Supply Current	No Load, $T_A = 25^\circ\text{C}$	●	1	1.5 2.3	1	1.5 2.3		mA mA
Internal Sampling Frequency			2.5		2.5			kHz

ELECTRICAL CHARACTERISTICS

$V_S = \pm 5V$, $T_A =$ operating temperature range unless otherwise specified.

PARAMETER	CONDITIONS	LTC1050M			LTC1050C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$T_A = 25^\circ\text{C}$ (Note 3)		± 0.5	± 5	± 0.5	± 5	μV	
Average Input Offset Drift	(Note 3)	●	± 0.01	± 0.05	± 0.01	± 0.05	$\mu\text{V}/^\circ\text{C}$	
Long Term Offset Voltage Drift			50		50		$\text{nV}/\sqrt{\text{Mo}}$	
Input Offset Current	$T_A = 25^\circ\text{C}$ (Note 5)	●	± 20	± 100 ± 200	± 20	± 125 ± 200	pA pA	
Input Bias Current	$T_A = 25^\circ\text{C}$ (Note 5)	●	± 10	± 50 ± 1000	± 10	± 75 ± 150	pA pA	
Input Noise Voltage	$R_S = 100\Omega$, 0.1Hz to 10Hz (Note 6) $R_S = 100\Omega$, DC to 1Hz		1.6		1.6		$\mu\text{V}_{\text{p-p}}$ $\mu\text{V}_{\text{p-p}}$	
Input Noise Current	$f = 10\text{Hz}$ (Note 4)		2.2		2.2		$\text{fA}/\sqrt{\text{Hz}}$	
Common Mode Rejection Ratio	$V_{\text{CM}} = V - I_O + 2.7V$, $T_A = 25^\circ\text{C}$	●	114 110	130	114 110	130	dB dB	
Power Supply Rejection Ratio	$V_S = \pm 2.375V$ to $\pm 8V$	●	120	140	120	140	dB	
Large Signal Voltage Gain	$R_L = 10\text{k}\Omega$, $V_{\text{OUT}} = \pm 4V$	●	120	160	120	160	dB	
Maximum Output Voltage Swing	$R_L = 10\text{k}\Omega$ $R_L = 100\text{k}\Omega$	●	± 4.7	± 4.85 ± 4.95	± 4.7	± 4.85 ± 4.95	V V	
Slew Rate	$R_L = 10\text{k}\Omega$, $C_L = 50\text{pF}$		4		4		$\text{V}/\mu\text{s}$	
Gain Bandwidth Product			2.5		2.5		MHz	
Supply Current	No Load, $T_A = 25^\circ\text{C}$	●	1	1.5 2.3	1	1.5 2.3	mA mA	
Internal Sampling Frequency			2.5		2.5		kHz	

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: Absolute Maximum ratings are those values beyond which life of the device may be impaired.

Note 2: Connecting any terminal to voltages greater than V_+ or less than V_- may cause destructive latch-up. It is recommended that no sources operating from external supplies be applied prior to power-up of the LTC1050.

Note 3: These parameters are guaranteed by design. Thermocouple effects preclude measurement of these voltage levels in high speed automatic test systems. V_{OS} is measured to a limit determined by test equipment capability.

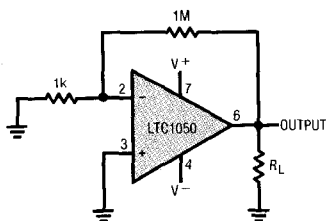
Note 4: Current Noise is calculated from the formula: $I_n = \sqrt{2q \cdot I_b}$ where $q = 1.6 \times 10^{-19}$ Coulomb.

Note 5: At $T_A \leq 0^\circ\text{C}$ these parameters are guaranteed by design and not tested.

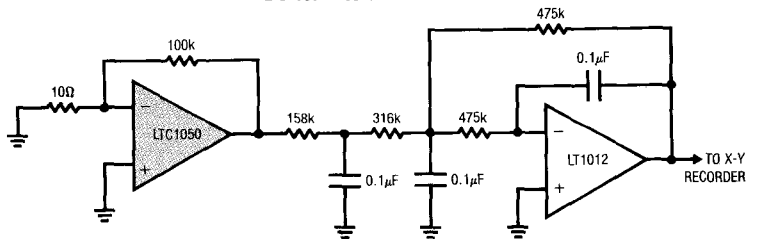
Note 6: Every lot of LTC1050AM and LTC1050AC is 100% tested for Broad-band Noise @ 1kHz and sample tested for Input Noise Voltage @ 0.1Hz to 10Hz.

TEST CIRCUITS

Electrical Characteristics Test Circuit



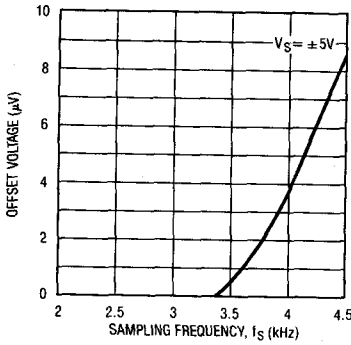
DC-10Hz Noise Test Circuit



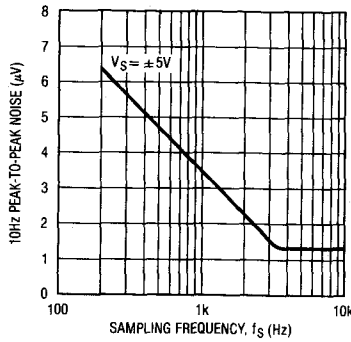
FOR 1Hz NOISE BW INCREASE ALL THE CAPACITORS BY A FACTOR OF 10.

TYPICAL PERFORMANCE CHARACTERISTICS

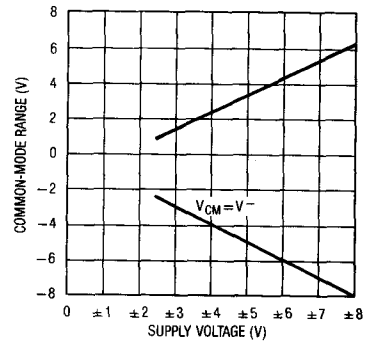
Offset Voltage vs Sampling Frequency



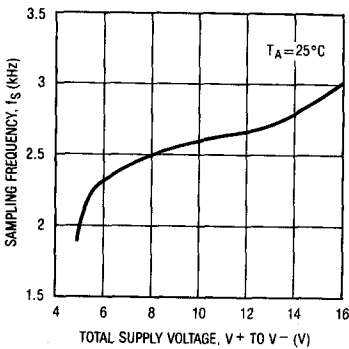
10Hz_{p-p} Noise vs Sampling Frequency



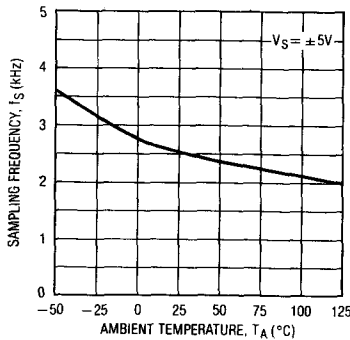
Common-Mode Input Range vs Supply Voltage



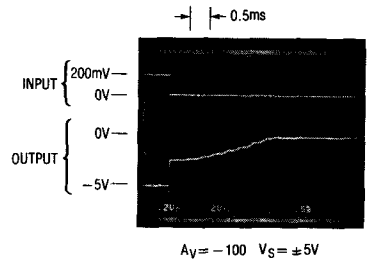
Sampling Frequency vs Supply Voltage



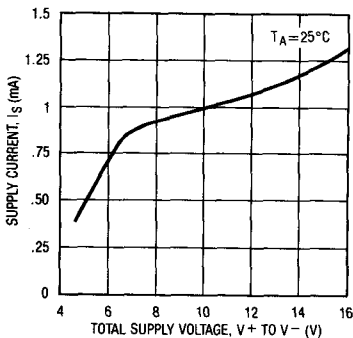
Sampling Frequency vs Temperature



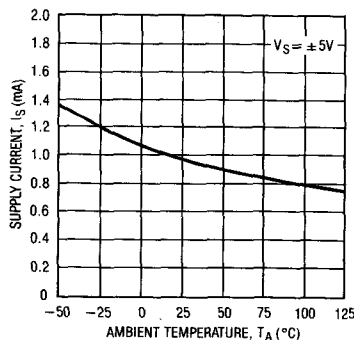
Overload Recovery



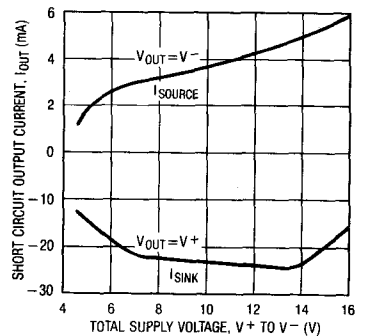
Supply Current vs Supply Voltage



Supply Current vs Temperature

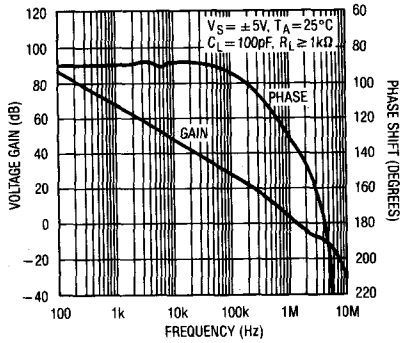


Output Short Circuit Current vs Supply Voltage

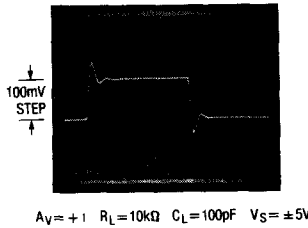


TYPICAL PERFORMANCE CHARACTERISTICS

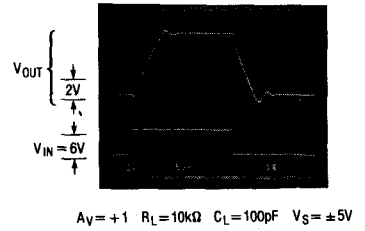
Gain/Phase vs Frequency



Small Signal Transient Response

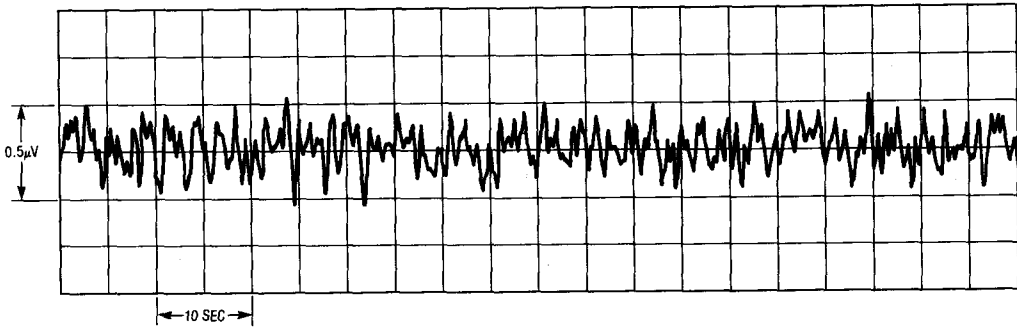


Large Signal Transient Response

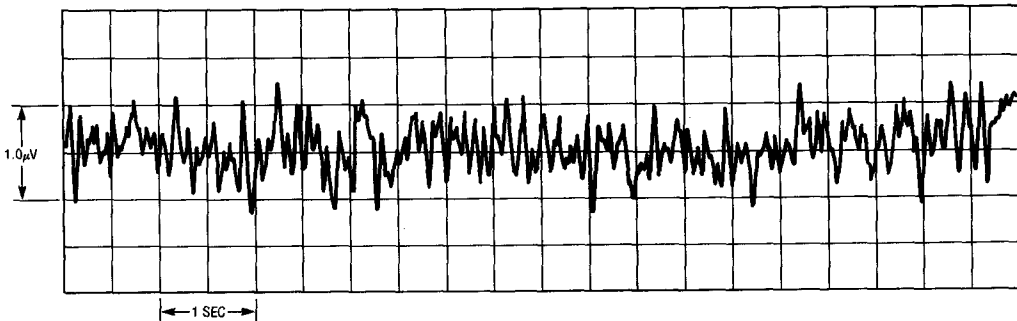


2

LTC1050 DC to 1Hz Noise



LTC1050 DC to 10Hz Noise



APPLICATIONS INFORMATION

ACHIEVING PICOAMPERE/MICROVOLT PERFORMANCE

Picoamperes

In order to realize the picoampere level of accuracy of the LTC1050, proper care must be exercised. Leakage currents in circuitry external to the amplifier can significantly degrade performance. High quality insulation should be used (e.g., Teflon, Kel-F); cleaning of all insulating surfaces to remove fluxes and other residues will probably be necessary — particularly for high temperature performance. Surface coating may be necessary to provide a moisture barrier in high humidity environments.

Board leakage can be minimized by encircling the input connections with a guard ring operated at a potential close to that of the inputs: in inverting configurations the guard ring should be tied to ground; in non-inverting connections to the inverting input (see Figure 1). Guarding both sides of the printed circuit board is required. Bulk leakage reduction depends on the guard ring width.

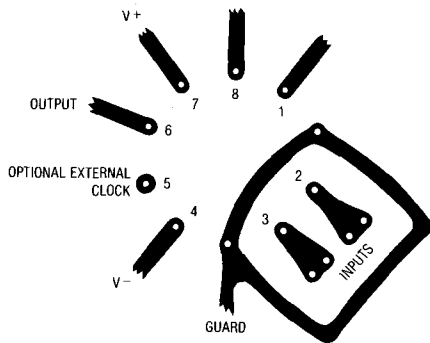


Figure 1.

Microvolts

Thermocouple effects must be considered if the LTC1050's ultra low drift is to be fully utilized. Any connection of dissimilar metals forms a thermoelectric junction producing an electric potential which varies with temperature (Seebeck effect). As temperature sensors, thermocouples exploit this phenomenon to produce useful information. In low drift amplifier circuits the effect is a primary source of error.

Connectors, switches, relay contacts, sockets, resistors, solder, and even copper wire are all candidates for thermal EMF generation. Junctions of copper wire from different manufacturers can generate thermal EMFs of $200\text{nV}/^\circ\text{C}$ — 4 times the maximum drift specification of the LTC1050. The copper/kovar junction, formed when wire or printed circuit traces contact a package lead, has a thermal EMF of approximately $35\mu\text{V}/^\circ\text{C}$ — 700 times the maximum drift specification of the LTC1050.

Minimizing thermal EMF-induced errors is possible if judicious attention is given to circuit board layout and component selection. It is good practice to minimize the number of junctions in the amplifier's input signal path. Avoid connectors, sockets, switches and relays where possible. In instances where this is not possible, attempt to balance the number and type of junctions so that differential cancellation occurs. Doing this may involve deliberately introducing junctions to offset unavoidable junctions.

Figure 2 is an example of the introduction of an unnecessary resistor to promote differential thermal balance. Maintaining compensating junctions in close physical proximity will keep them at the same temperature and reduce thermal EMF errors.

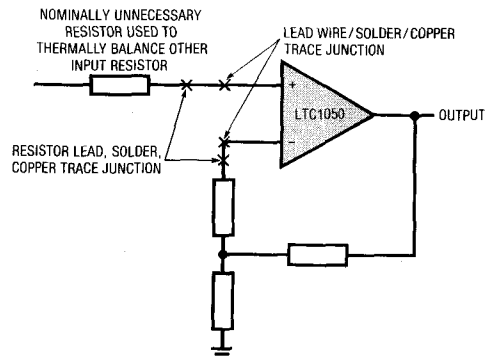


Figure 2.

APPLICATIONS INFORMATION

When connectors, switches, relays and/or sockets are necessary they should be selected for low thermal EMF activity. The same techniques of thermally balancing and coupling the matching junctions are effective in reducing the thermal EMF errors of these components.

Resistors are another source of thermal EMF errors. Table 1 shows the thermal EMF generated for different resistors. The temperature gradient across the resistor is important, not the ambient temperature. There are two junctions formed at each end of the resistor and if these junctions are at the same temperature, their thermal EMFs will cancel each other. The thermal EMF numbers are approximate and vary with resistor value. High values give higher thermal EMF.

Table 1. Resistor Thermal EMF

Resistor Type	Thermal EMF/°C Gradient
Tin Oxide	~ mV/°C
Carbon Composition	~ 450 μ V/°C
Metal Film	~ 20 μ V/°C
Wire Wound	
Evenohm	~ 2 μ V/°C
Manganin	~ 2 μ V/°C

PACKAGE-INDUCED OFFSET VOLTAGE

Package-induced thermal EMF effects are another important source of errors. It arises at the copper/kovar junctions formed when wire or printed circuit traces contact a package lead. Like all the previously mentioned thermal EMF effects, it is outside the LTC1050's offset nulling loop and cannot be cancelled. Metal can H packages exhibit the worst warm-up drift. The input offset voltage specification of the LTC1050 is actually set by the package-induced warm-up drift rather than by the circuit itself. The thermal time constant ranges from 0.5 to 3 minutes, depending on package type.

OPTIONAL EXTERNAL CLOCK

An external clock is not required for the LTC1050 to operate. The internal clock circuit of the LTC1050 sets the nominal sampling frequency at around 2.5kHz. This frequency is chosen such that it is high enough to remove the am-

plifier $1/f$ noise, yet still low enough to allow internal circuits to settle. The oscillator of the internal clock circuit has a frequency 4 times the sampling frequency and its output is brought out to pin 5 through a 2k Ω resistor. When the LTC1050 operates without using an external clock, pin 5 should be left floating and capacitive loading on this pin should be avoided. If the oscillator signal on pin 5 is used to drive other external circuits, a buffer with low input capacitance is required to minimize loading on this pin. Figure 3 illustrates the internal sampling frequency versus capacitive loading at pin 5.

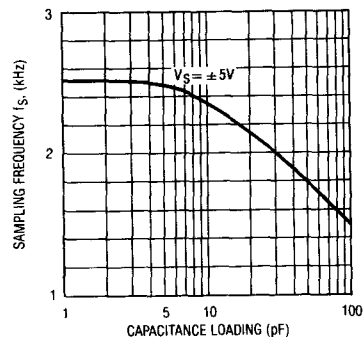


Figure 3. Sampling Frequency vs Capacitance Loading at Pin 5

When an external clock is used, it is directly applied to pin 5. The internal oscillator signal on pin 5 has very low drive capability and can be over-driven by any external signal. When the LTC1050 operates on $\pm 5V$ power supplies, the external clock level is TTL compatible.

Using an external clock can affect performance of the LTC1050. Effects of external clock frequency on input offset voltage and input noise voltage are shown in the section of typical performance characteristics. The sampling frequency is the external clock frequency divided by 4. Input bias currents at temperatures below 100°C are dominated by the charge injection of input switches and they are basically proportional to the sampling frequency. At higher temperatures, input bias currents are mainly due to leakage currents of the input protection devices and are insensitive to the sampling frequency.

APPLICATIONS INFORMATION

LOW SUPPLY OPERATION

The minimum supply for proper operation of the LTC1050 is typically below 4.0V ($\pm 2.0V$). In single supply applications, PSRR is guaranteed down to 4.7V ($\pm 2.35V$) to ensure proper operation down to the minimum TTL specified voltage of 4.75V.

PIN COMPATIBILITY

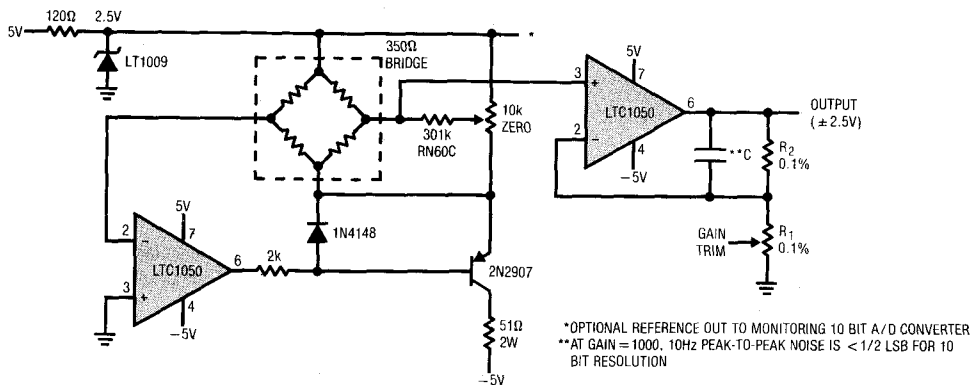
The LTC1050 is pin compatible with the 8-pin versions of 7650, 7652 and other chopper-stabilized amplifiers. The 7650 and 7652 require the use of two external capacitors

connected to pin 1 and 8 which are not needed for the LTC1050. Pin 1 and pin 8 of the LTC1050 are not connected internally while pin 5 is an optional external clock input pin. The LTC1050 can be a direct plug in for the 7650 and 7652 even if the two capacitors are left on the circuit board.

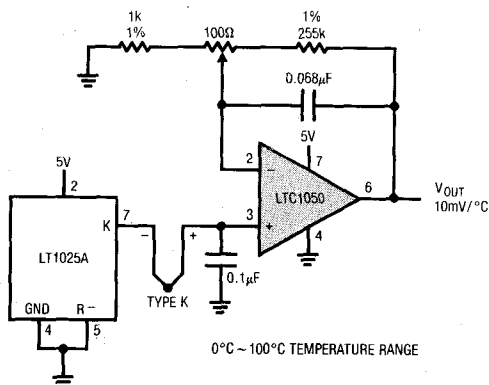
In applications operating from below +16V total power supply, ($\pm 8V$), the LTC1050 can replace many industry-standard operational amplifiers such as the 741, LM101, LM108, OP07, etc. For devices like the 741 and LM101, the removal of any connection to pin 5 is all that is needed.

TYPICAL APPLICATIONS

Strain Gauge Signal Conditioner with Bridge Excitation

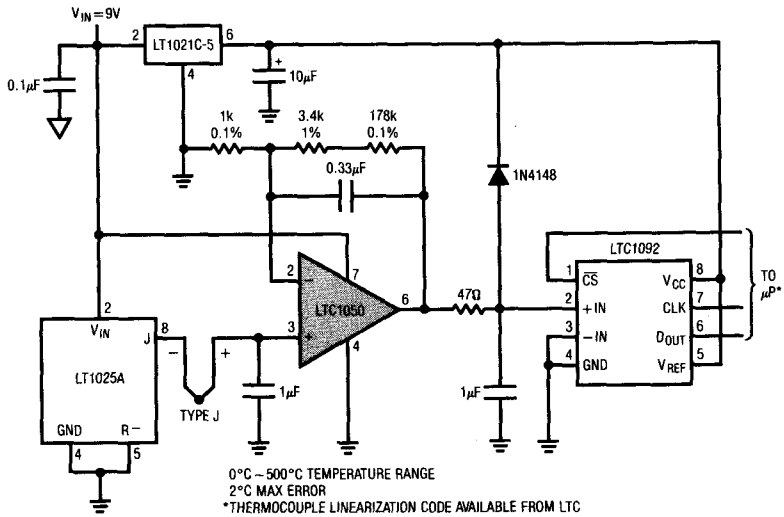


Single Supply Thermocouple Amplifier



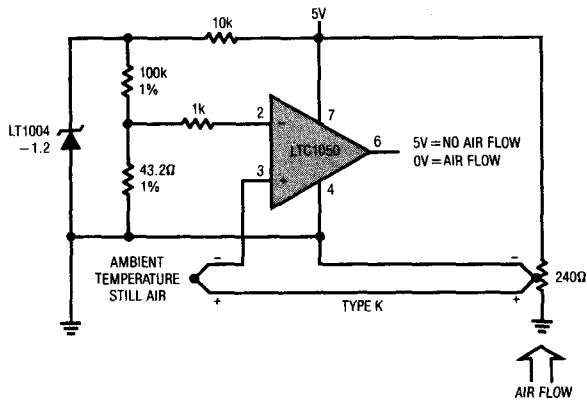
TYPICAL APPLICATIONS

Battery Operated Temperature Monitor with 10-Bit Serial Output A/D



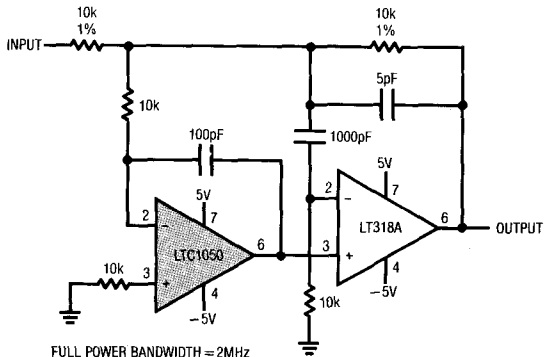
2

Air Flow Detector



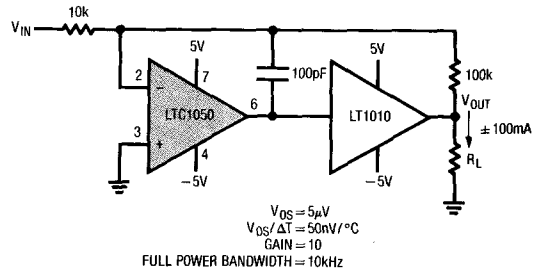
TYPICAL APPLICATIONS

Fast Precision Inverter



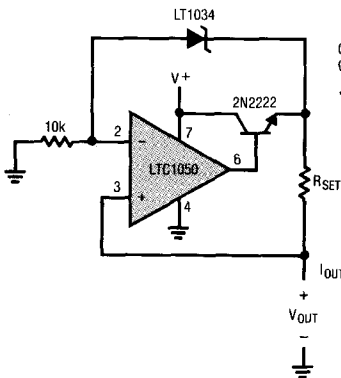
FULL POWER BANDWIDTH = 2MHz
 SLEW RATE $\geq 40V/\mu S$
 SETTLING TIME = 5 μS TO 0.01% (10V STEP)
 OFFSET VOLTAGE = 5 μV
 OFFSET DRIFT = 50mV/°C

$\pm 100mA$ Output Drive



$V_{OS} = 5\mu V$
 $V_{OS}/\Delta T = 50mV/^\circ C$
 GAIN = 10
 FULL POWER BANDWIDTH = 10kHz

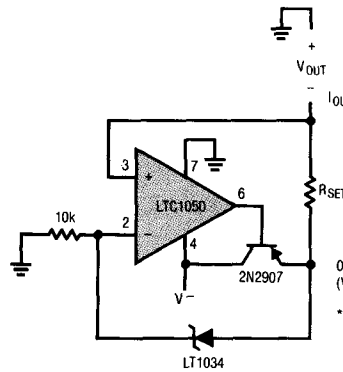
Ground Referred Precision Current Sources



$0 \leq I_{OUT} \leq 25mA^*$
 $0.2V \leq V_{OUT} \leq (V^+) - 2V$

*MAXIMUM CURRENT LIMITED BY
 POWER DISSIPATION OF 2N2222

$$I_{OUT} = \frac{1.235V}{R_{SET}}$$



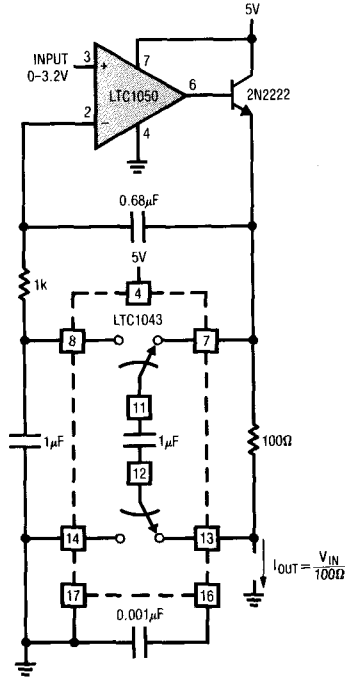
$$I_{OUT} = \frac{1.235V}{R_{SET}}$$

$0 \leq I_{OUT} \leq 25mA^*$
 $(V^-) + 2V \leq V_{OUT} \leq -1.8V$

*MAXIMUM CURRENT LIMITED BY
 POWER DISSIPATION OF 2N2907

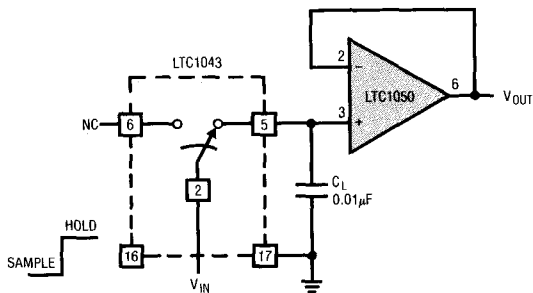
TYPICAL APPLICATIONS

**Precision Voltage Controlled Current Source
with Ground Referred Input and Output**



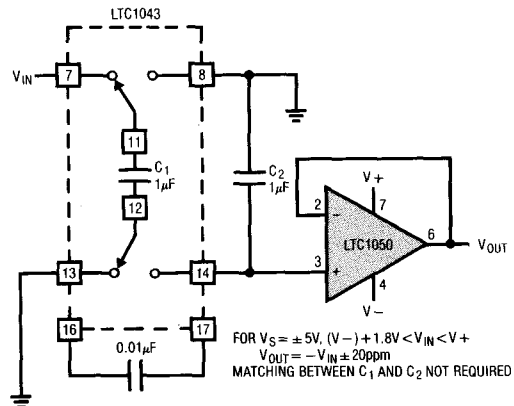
2

Sample-and-Hold Amplifier



FOR $1V \leq V_{IN} \leq 4V$, THE HOLD STEP IS $\leq 300\mu V$.
ACQUISITION TIME IS DETERMINED BY THE SWITCH R_{ON} ,
 C_L TIME CONSTANT

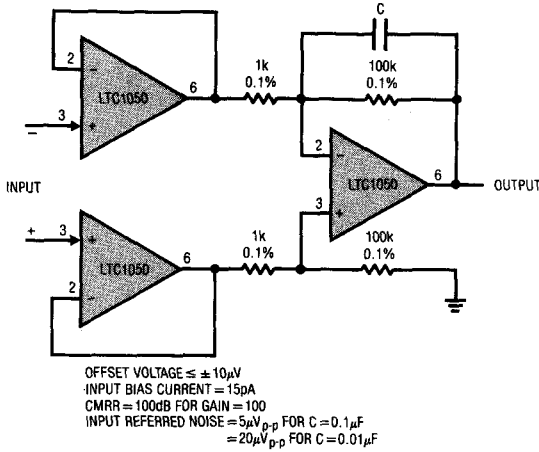
Ultra Precision Voltage Inverter



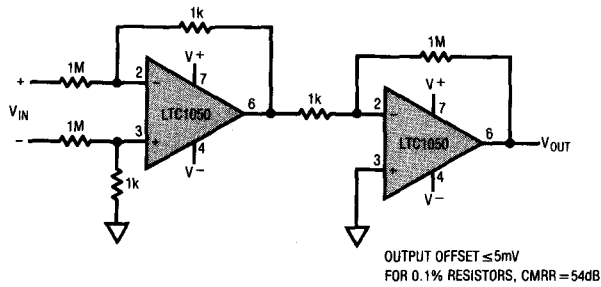
FOR $V_S = \pm 5V$, $(V_-) + 1.8V < V_{IN} < V_+$
 $V_{OUT} = -V_{IN} \pm 20ppm$
MATCHING BETWEEN C_1 AND C_2 NOT REQUIRED

TYPICAL APPLICATIONS

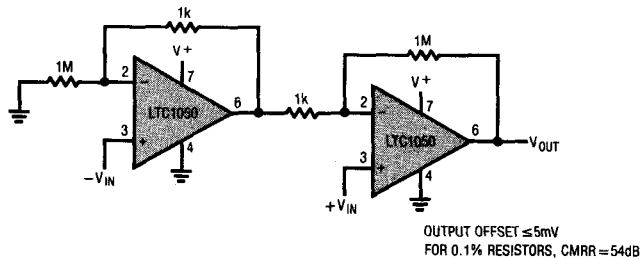
Instrumentation Amplifier with Low Offset and Input Bias Current



Instrumentation Amplifier with 100V Common Mode Input Voltage

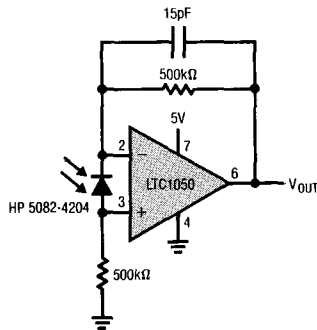


Single Supply Instrumentation Amplifier



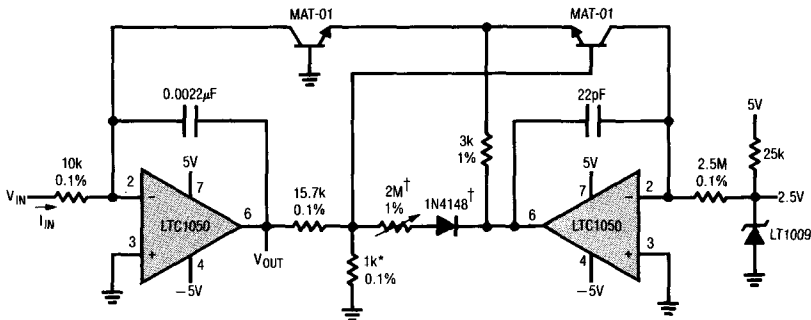
TYPICAL APPLICATIONS

Photodiode Amplifier



2

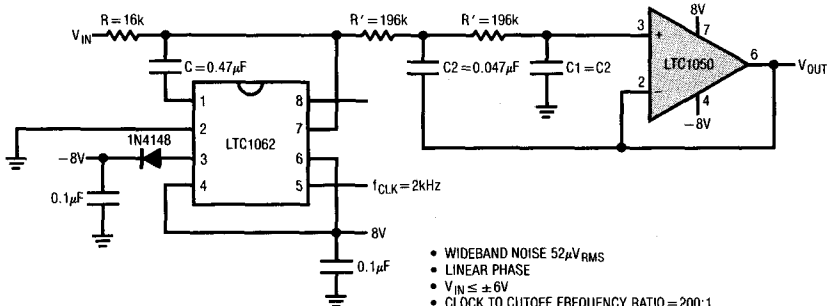
6 Decade Log Amplifier



ERROR REFERRED TO INPUT < 1%
 FOR INPUT CURRENT RANGE 1nA ~ 1mA
 †TEL LAB TYPE Q81
 ‡CORRECTS FOR NONLINEARITIES

$$V_{OUT} = -\text{LOG} \left(\frac{I_{IN}}{1\mu A} \right) = -\text{LOG} \left(\frac{V_{IN}}{10\text{mV}} \right) = -\text{LOG} (V_{IN}) - 2\text{V}$$

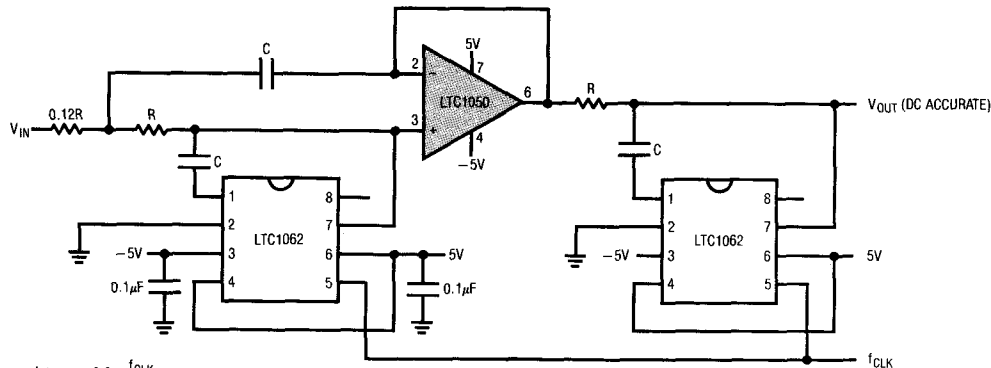
DC Accurate, 10Hz, 7th Order Lowpass Bessel Filter



- WIDEBAND NOISE 52μV RMS
- LINEAR PHASE
- $V_{IN} \leq \pm 6\text{V}$
- CLOCK TO CUTOFF FREQUENCY RATIO = 200:1

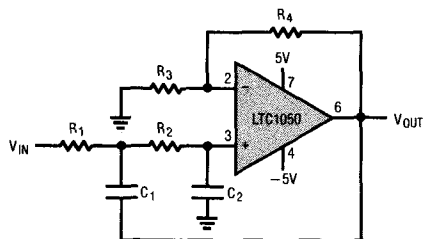
TYPICAL APPLICATIONS

DC Accurate 10th Order Max Flat Lowpass Filter



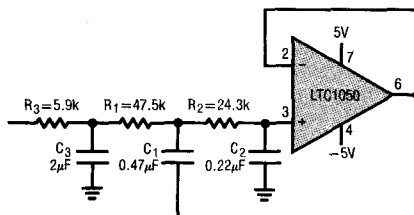
- $f_{CUTOFF} = 0.9 \times \frac{f_{CLK}}{100}$
- $RC = 0.2244 \times \frac{1}{f_{CUTOFF}}$
- 60dB/OCT. SLOPE
- PASSBAND ERROR $< 0.1\text{dB}$ FOR $0 \leq f \leq 0.67 f_{CUTOFF}$
- THD = 0.04%, WIDEBAND NOISE = $120\mu\text{V}_{RMS}$
- $f_{CLK} = 100\text{kHz}$

DC Accurate, Noninverting 2nd Order Lowpass Filter



$Q = 0.707$, $f_C = 20\text{Hz}$. FOR $f_C = 10\text{Hz}$, THE RESISTOR (R_1 , R_2) VALUES SHOULD BE DOUBLED.

Gain of One, 10Hz 3rd Order Bessel DC Accurate Lowpass Filter

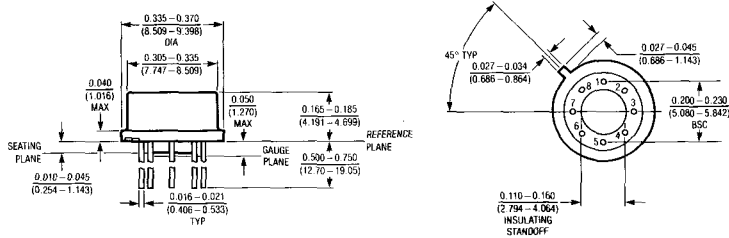


Component Values

DC GAIN	R_3	R_4	R_1	R_2	C_1	C_2
1	∞	0	32.4k	18.7k	0.47 μF	0.22 μF
2	10k	10k	11.8k	24.3k	0.47 μF	0.47 μF
4	10.5k	31.6k	18.7k	34.8k	0.22 μF	0.47 μF
6	10.2k	51.1k	14k	46.4k	0.22 μF	0.47 μF
8	10.2k	71.5k	11.8k	54.9k	0.22 μF	0.47 μF
10	10.1k	90.9k	10.5k	61.9k	0.22 μF	0.47 μF

PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

H Package
8 Lead TO-5 Metal Can



NOTE: LEAD DIAMETER IS UNCONTROLLED BETWEEN THE REFERENCE PLANE AND SEATING PLANE.

FIG 100

2

J Package
8 Lead Ceramic DIP

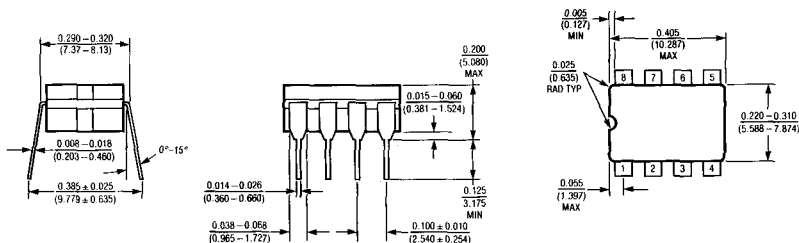


FIG 101

N Package
8 Lead Plastic DIP

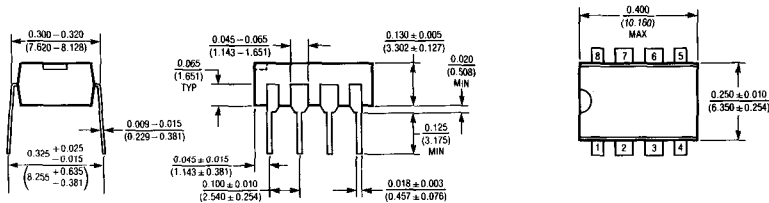
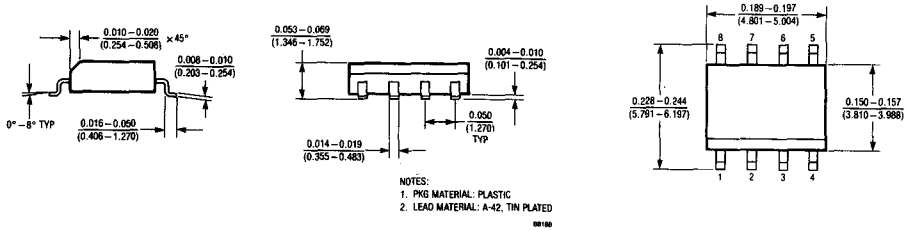


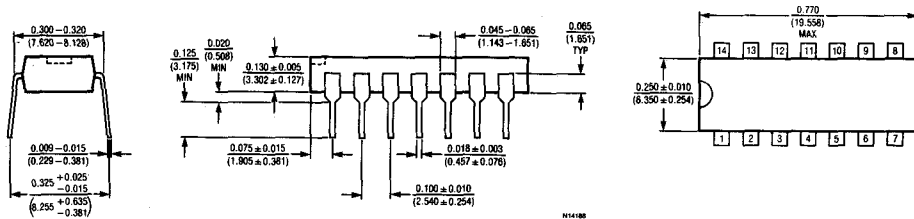
FIG 102

PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

S8 Package
8 Lead Plastic SOIC



N Package
14 Lead Plastic DIP



FEATURES

- Guaranteed Max. Offset 5μV
- Guaranteed Max. Offset Drift 0.05μV/°C
- Typ. Offset Drift 0.01μV/°C
- Excellent Long Term Stability 100nV/√Month
- Guaranteed Max. Input Bias Current 30pA
- Over Operating Temperature Range
 - Guaranteed Min. Gain 120dB
 - Guaranteed Min. CMRR 120dB
 - Guaranteed Min. PSRR 120dB
- Single Supply Operation 4.75V to 16V
(Input Voltage Range Extends to Ground)
- External Capacitors can be Returned to V⁻ with No Noise Degradation

APPLICATIONS

- Thermocouple Amplifiers
- Strain Gauge Amplifiers
- Low Level Signal Processing
- Medical Instrumentation

DESCRIPTION

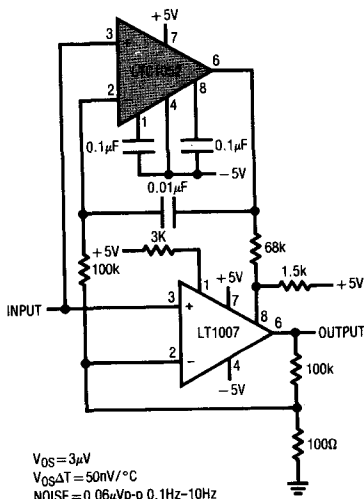
The LTC1052 and LTC7652 are low noise Chopper-stabilized op amps (CSOA™) manufactured using Linear Technology's enhanced LTCMOS™ silicon gate process. Chopper-stabilization constantly corrects offset voltage errors. Both initial offset and changes in the offset due to time, temperature and common-mode voltage are corrected. This, coupled with picoampere input currents, gives these amplifiers unmatched performance.

Low frequency (1/f) noise is also improved by the chopping technique. Instead of increasing continuously at a 3dB/octave rate, the internal chopping causes noise to decrease at low frequencies.

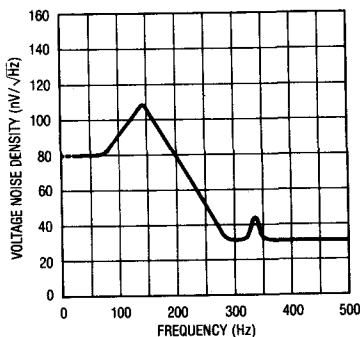
The chopper circuitry is entirely internal and completely transparent to the user. Only two external capacitors are required to alternately sample and hold the offset correction voltage and the amplified input signal. Control circuitry is brought out on the 14-pin version to allow the sampling of the LTC1052 to be synchronized with an external frequency source.

2

Ultra Low Noise, Low Drift Amplifier



LTC1052 Noise Spectrum



CSOA™ and LTCMOS™ are trademarks of Linear Technology Corporation.
Teflon™ is a trademark of DuPont.

LTC1052/LTC7652

ABSOLUTE MAXIMUM RATINGS

(Notes 1 and 2)

Total Supply Voltage (V^+ to V^-)	18V
Input Voltage	($V^+ + 0.3V$) to ($V^- - 0.3V$)
Output Short Circuit Duration	Indefinite
Operating Temperature Range	
LTC1052C/LTC7652C	-40°C to 85°C
LTC1052M	-55°C to 125°C
Storage Temperature Range	-55°C to 150°C
Lead Temperature (Soldering, 10 sec.)	300°C

PACKAGE/ORDER INFORMATION

TOP VIEW	ORDER PART NUMBER	REPLACES
<p>METAL CAN H PACKAGE</p>	LTC7652CH	ICL7652CTV ICL7652ITV ICL7650CTV-1 ICL7650ITV-1
	LTC1052CH	ICL7650CTV ICL7650ITV
	LTC1052MH	ICL7650MTV
<p>HERMETIC DIP J8 PACKAGE PLASTIC DIP N8 PACKAGE</p>	LTC1052CN8 LTC1052CJ8 LTC1052MJ8	ICL7650CPA ICL7650JA
<p>HERMETIC DIP J14 PACKAGE PLASTIC DIP N14 PACKAGE</p>	LTC1052CJ LTC1052CN LTC1052MJ	ICL7652IJD ICL7650IJD ICL7652CPD ICL7650CPD ICL7650MJD

ELECTRICAL CHARACTERISTICS

$V_S = \pm 5V$, $T_A =$ operating temperature range, test circuit TC1, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	LTC1052M			LTC1052C/LTC7652C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	$T_A = 25^\circ C$ (Note 3)	± 0.5	± 5		± 0.5	± 5		μV
$\Delta V_{OS}/\Delta Temp$	Average Input Offset Drift	(Note 3)	± 0.01	± 0.05		± 0.01	± 0.05		$\mu V/^\circ C$
$\Delta V_{OS}/\Delta Time$	Long Term Offset Voltage Stability			100			100		nV/ \sqrt{Month}
I_{OS}	Input Offset Current	$T_A = 25^\circ C$	± 5	± 30		± 5	± 30		pA
				± 2000			± 350		pA
I_B	Input Bias Current	$T_A = 25^\circ C$	± 1	± 30		± 1	± 30		pA
				± 1000			± 175		pA
e_{np-p}	Input Noise Voltage	$R_S = 100\Omega$, DC to 10Hz, TC3 $R_S = 100\Omega$, DC to 1Hz, TC3		1.5 0.5			1.5 0.5		μV_{p-p} μV_{p-p}
i_n	Input Noise Current	$f = 10Hz$ (Note 5)		0.6			0.6		fA/ \sqrt{Hz}
CMRR	Common-Mode Rejection Ratio	$V_{CM} = V^-$ to $+2.7V$	\bullet	120	140		120	140	dB
PSRR	Power Supply Rejection Ratio	$V_{SUPPLY} = \pm 2.375V$ to $\pm 8V$	\bullet	120	150		120	150	dB
A_{VOL}	Large Signal Voltage Gain	$R_L = 10k$, $V_{OUT} = \pm 4V$	\bullet	120	150		120	150	dB
V_{OUT}	Maximum Output Voltage Swing	(Note 4) $R_L = 10k$ $R_L = 100k$	\bullet	± 4.7	± 4.85 ± 4.95		± 4.7	± 4.85 ± 4.95	V V
SR	Slew Rate	$R_L = 10k$, $C_L = 50pF$		4			4		V/ μs
GBW	Gain Bandwidth Product			1.2			1.2		MHz
I_S	Supply Current	No Load, $T_A = 25^\circ C$	\bullet	1.7	2.0 3.0		1.7	2.0 3.0	mA mA
f_S	Internal Sampling Frequency			330			330		Hz
	Clamp On Current	$R_L = 100k$	\bullet	25	100		25	100	μA
	Clamp Off Current	$-4V < V_{OUT} < +4V$	\bullet	10	100 2		10	100 1	pA nA

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: Absolute Maximum Ratings are those values beyond which the life of the device may be impaired.

Note 2: Connecting any terminal to voltages greater than V^+ or less than V^- may cause destructive latch-up. It is recommended that no sources operating from external supplies be applied prior to power-up of the LTC1052/LTC7652.

Note 3: These parameters are guaranteed by design. Thermocouple effects preclude measurement of these voltage levels in high speed automatic testing. V_{OS} is measured to a limit determined by test equipment capability. Voltages on C_{EXTA} and C_{EXTB} , A_{VOL} , CMRR and PSRR are measured to insure proper operation of the nulling loop to insure meeting the V_{OS} and V_{OS} drift specifications. See Package-Induced V_{OS} in applications section.

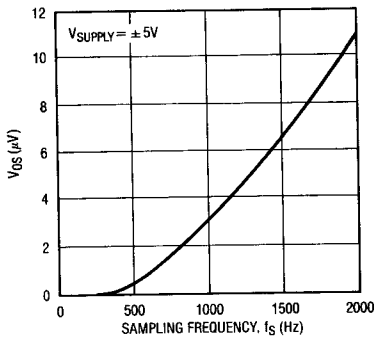
Note 4: Output clamp not connected.

Note 5: Current noise is calculated from the formula: $i_n = (2q I_B)^{1/2}$, where $q = 1.6 \times 10^{-19}$ coulomb.

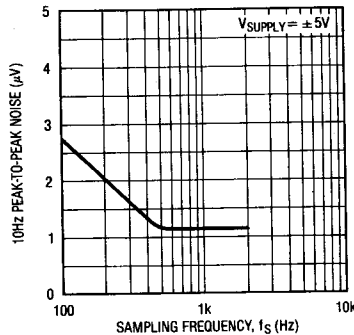
TYPICAL PERFORMANCE CHARACTERISTICS

2

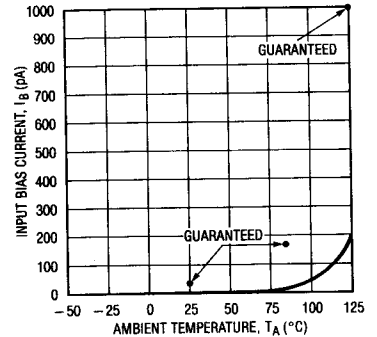
Offset Voltage vs Sampling Frequency



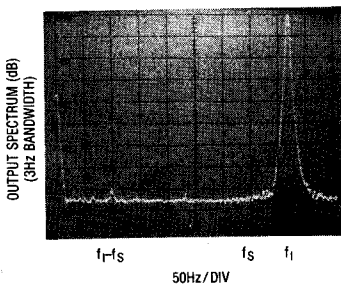
10Hzp-p Noise vs Sampling Frequency



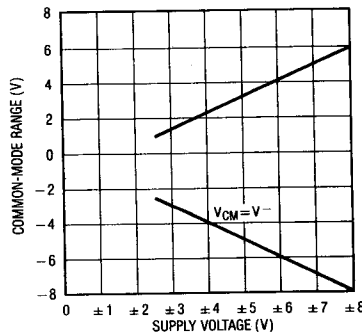
Input Bias Current vs Temperature



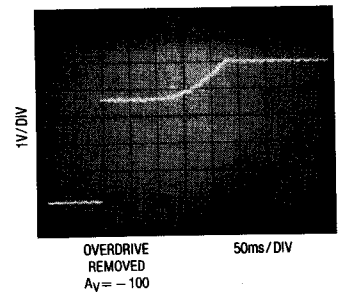
Aliasing Error



Common-Mode Input Range vs Supply Voltage

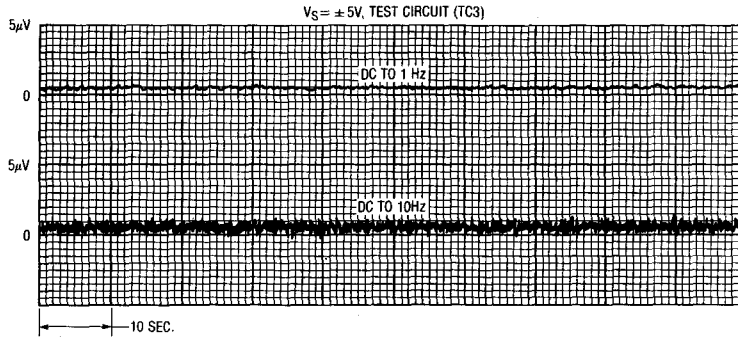


Overload Recovery (Output Clamp Not Used)



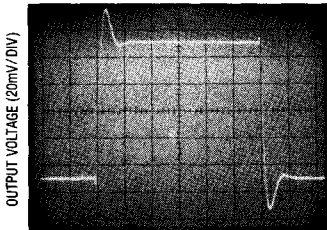
TYPICAL PERFORMANCE CHARACTERISTICS

Input Noise Voltage



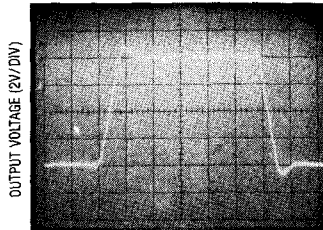
2-43

Small Signal Transient Response*



$A_V = +1$
 $R_L = 10k$
 $C_L = 100pF$
 $V_S = \pm 5V$

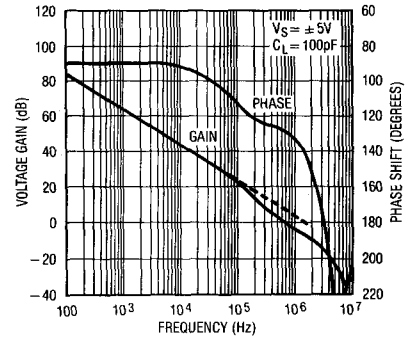
Large Signal Transient Response*



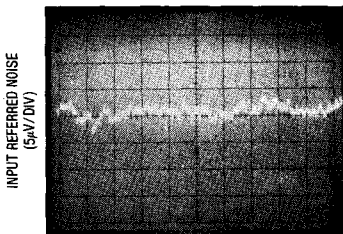
$A_V = +1$
 $R_L = 10k$
 $C_L = 100pF$
 $V_S = \pm 5V$

*RESPONSE IS NOT DEPENDENT ON PHASE OF CLOCK

Gain Phase vs Frequency

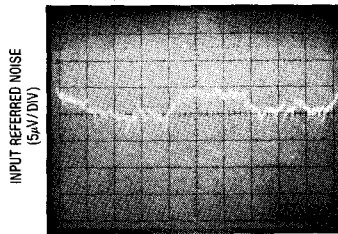


Broadband Noise, $C_{EXT} = 0.1\mu F$



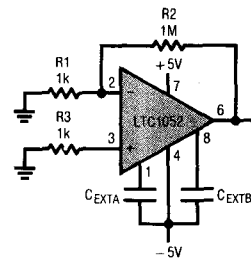
$A_V = -1000$

Broadband Noise, $C_{EXT} = 1.0\mu F$



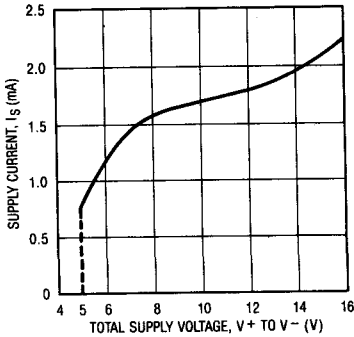
$A_V = -1000$

Broadband Noise Test Circuit (TC2)

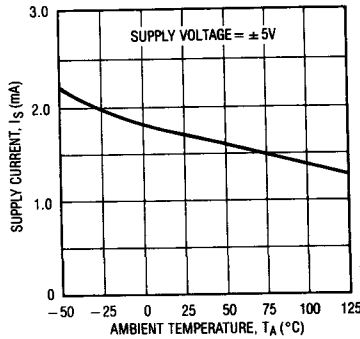


TYPICAL PERFORMANCE CHARACTERISTICS

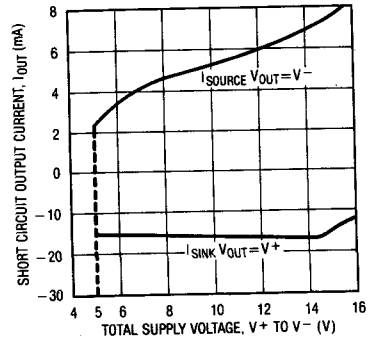
Supply Current vs Supply Voltage



Supply Current vs Temperature

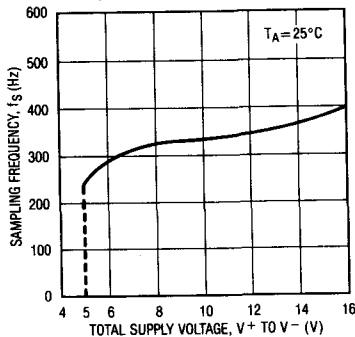


Output Short Circuit Current vs Supply Voltage

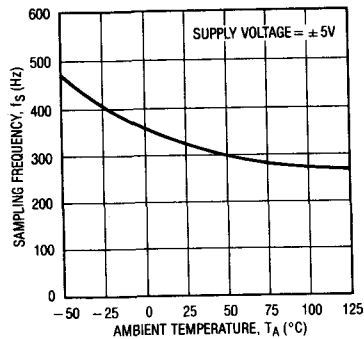


2

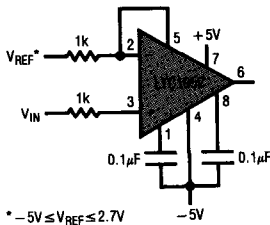
Sampling Frequency vs Supply Voltage



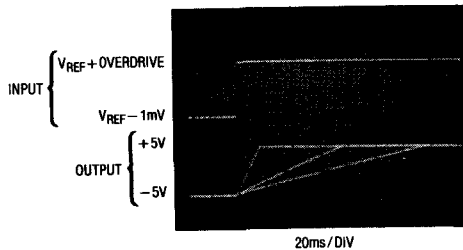
Sampling Frequency vs Temperature



Comparator Operation

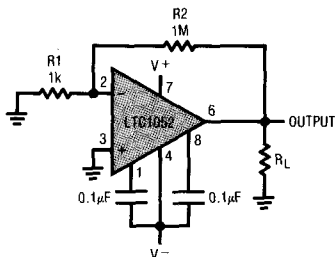


Response Time vs Overdrive

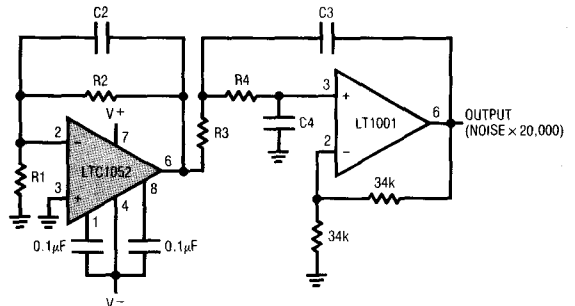


TEST CIRCUITS

Electrical Characteristics Test Circuit (TC1)



DC to 10Hz and DC to 1Hz Noise Test Circuit (TC3)



BANDWIDTH	R1	R2	R3	R4	C2	C3	C4
10Hz	16.2k	162k	16.2k	16.2k	0.1µF	1.0µF	1.0µF
1Hz	16.2k	162k	162k	162k	1.0µF	1.0µF	1.0µF

THEORY OF OPERATION

DC OPERATION

The shaded portion of the LTC1052 block diagram (Figure 1) entirely determines the amplifier's DC characteristics. During the auto-zero portion of the cycle, the inputs are shorted together and a feedback path is closed around the input stage to null its offset. Switch S2 and capacitor C_{EXTA} act as a sample and hold to store the nulling voltage during the next step—the sampling cycle.

In the sampling cycle, the zeroed amplifier is used to amplify the differential input voltage. Switch S2 connects the amplified input voltage to C_{EXTB} and the output gain stage. C_{EXTB} and S2 act as a sample and hold to store the amplified input signal during the auto-zero cycle. By switching between these two states at a frequency much higher than the signal frequency, a continuous output results.

Notice that during the auto-zero cycle the inputs are not only shorted together, but are also shorted to the negative input. This forces nulling with the common-mode voltage present and accounts for the extremely high CMRR of the LTC1052. In the same fashion, variations in power supply are also nulled. For nulling to take place, the offset voltage, common-mode voltage and power supply must not change at a frequency which is high compared to the frequency response of the nulling loop.

AC OPERATION AND ALIASING ERRORS

So far, the DC performance of the LTC1052 has been explained. As the input signal frequency increases, the problem of aliasing must be addressed. Aliasing is the spurious formation of low and high frequency signals caused by the mixing of the input signal with the sampling frequency, f_s . The frequency of the error signals, f_E , is:

$$f_E = f_s \pm f_i$$

where f_i = input signal frequency.

Normally it is the difference frequency ($f_s - f_i$) which is of concern because the high frequency ($f_s + f_i$) can be easily filtered. As the input frequency approaches the sampling frequency, the difference frequency approaches zero and will cause DC errors—the exact problem that the chopping amplifier is meant to eliminate.

The solution is simple. Filter the input so the sampling loop never sees any frequency near the sampling frequency.

At a frequency well below the sampling frequency, the LTC1052 forces I_1 to equal I_2 (see Figure 1B). This makes δI zero, thus the gain of the sampling loop zero at this and higher frequencies—i.e., a low pass filter. The corner frequency of this low pass filter is set by the output stage pole ($1/R_{L4} g_{m5} R_{L5} C_2$).

THEORY OF OPERATION

For frequencies above this pole, I_2 is:

$$I_2 = V_{IN} g_{m6} \times \frac{1}{SC2} \times SC1$$

and

$$I_1 - I_2 = V_{IN} g_{m1} - V_{IN} g_{m6} \times \frac{C1}{C2}$$

The LTC1052 is very carefully designed so that $g_{m1} = g_{m6}$ and $C1 = C2$. Substituting these values in the above equation shows $I_1 - I_2 = 0$.

The g_{m6} input stage, with $C1$ and $C2$, not only filters the input to the sampling loop, but also acts as a high frequency path to give the LTC1052 good high frequency response. The unity-gain cross frequencies for both the DC path and high frequency path are identical

$$[f_{3dB} = \frac{1}{2\pi} (g_{m1}/C1) = \frac{1}{2\pi} (g_{m6}/C2)].$$

This makes the frequency response smooth and continuous and eliminates sampling noise in the output as the loop transitions from the high gain DC loop to the high frequency loop.

The typical curves show just how well the amplifier works. The output spectrum shows the difference frequency ($f_1 - f_s = 100\text{Hz}$) is down by 80dB and the frequency response curve shows no abnormalities or perturbations. Also note the well-behaved small and large signal step responses and the absence of the sampling frequency in the output spectrum. If the dynamics of the amplifier, i.e., slew rate and overshoot, depend on the sampling clock, the sampling frequency will appear in the output spectrum.

2

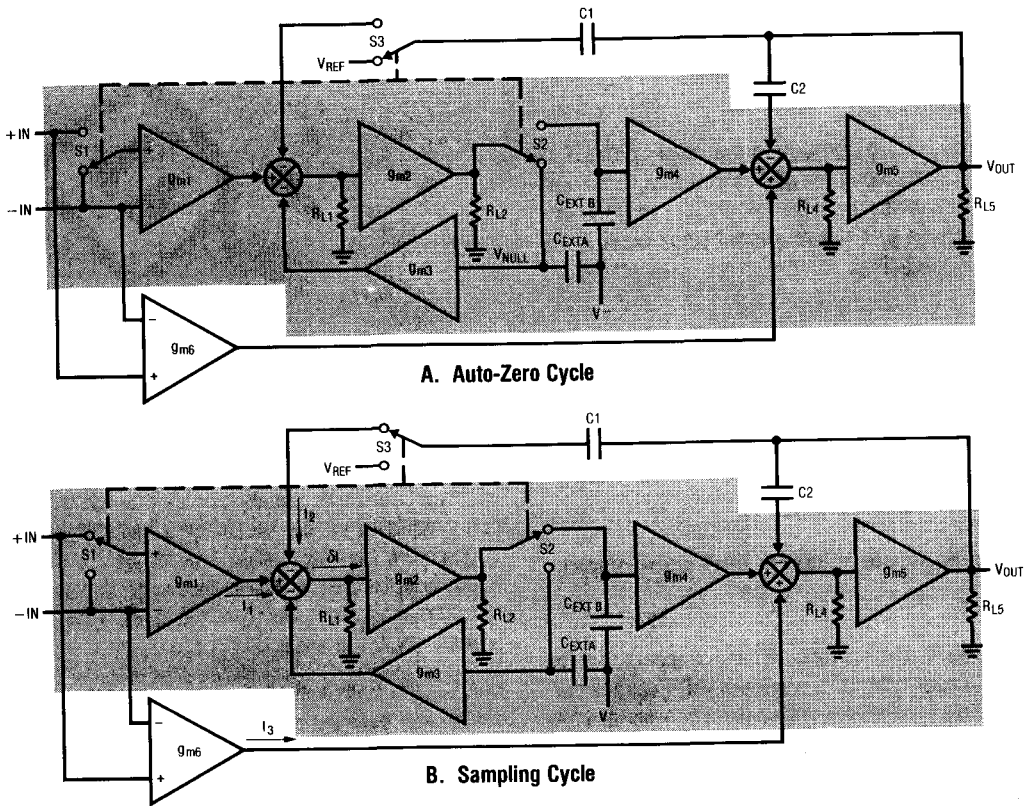


Figure 1. LTC1052 Block Diagram

APPLICATIONS INFORMATION

EXTERNAL CAPACITORS

C_{EXTA} and C_{EXTB} are the holding elements of a sample and hold circuit. The important capacitor characteristics are leakage current and dielectric absorption. A high quality film-type capacitor such as mylar or polypropylene provides excellent performance. However, low grade capacitors such as ceramic are suitable in many applications.

Capacitors with very high dielectric absorption (ceramic) can take several seconds to settle after power is first turned on. This settling appears as clock ripple on the output and, as the capacitor settles, the ripple gradually disappears. If fast settling after power turn-on is important, mylar or polypropylene is recommended.

Above 85°C, leakage, both from the holding capacitors and the printed circuit board, becomes important. To maintain the capabilities of the LTC1052 it may be necessary to use Teflon™ capacitors and Teflon standoffs when operating at 125°C (see Achieving Picoampere/Microvolt Performance).

C_{EXTA} and C_{EXTB} are normally in the range of 0.1μF to 1.0μF. All specifications are guaranteed with 0.1μF and the broadband noise (see typical photos) is only very slightly degraded with 0.1μF. Output clock ripple is not present for capacitors of 0.1μF or greater at any temperature.

On competitive devices, connecting C_{EXTA} and C_{EXTB} to V⁻ causes an increase in amplifier noise. Design changes have eliminated this problem on the LTC1052. On the 14-pin LTC1052 and 8-pin LTC7652, the capacitors can be returned to V⁻ or C_{RETURN} with no change in noise performance.

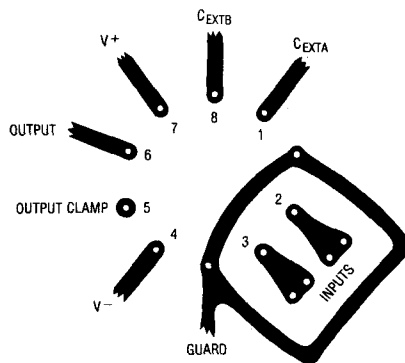
ACHIEVING PICOAMPERE/MICROVOLT PERFORMANCE

Picoamperes

In order to realize the picoampere level of accuracy of the LTC1052, proper care must be exercised. Leakage currents in circuitry external to the amplifier can significantly degrade performance. High quality insulation should be used (e.g., Teflon, Kel-F); cleaning of all insulating surfaces to remove fluxes and other residues will probably be

necessary—particularly for high temperature performance. Surface coating may be necessary to provide a moisture barrier in high humidity environments.

Board leakage can be minimized by encircling the input connections with a guard ring operated at a potential close to that of the inputs: in inverting configurations the guard ring should be tied to ground; in non-inverting connections to the inverting input. Guarding both sides of the printed circuit board is required. Bulk leakage reduction depends on the guard ring width.



Microvolts

Thermocouple effects must be considered if the LTC1052's ultra low drift is to be fully utilized. Any connection of dissimilar metals forms a thermoelectric junction producing an electric potential which varies with temperature (Seebeck effect). As temperature sensors, thermocouples exploit this phenomenon to produce useful information. In low drift amplifier circuits the effect is a primary source of error.

Connectors, switches, relay contacts, sockets, resistors, solder, and even copper wire are all candidates for thermal EMF generation. Junctions of copper wire from different manufacturers can generate thermal EMFs of 200nV/°C—4 times the maximum drift specification of

APPLICATIONS INFORMATION

the LTC1052. The copper/kovar junction, formed when wire or printed circuit traces contact a package lead, has a thermal EMF of approximately $35\mu\text{V}/^\circ\text{C}$ —700 times the maximum drift specification of the LTC1052.

Minimizing thermal EMF-induced errors is possible if judicious attention is given to circuit board layout and component selection. It is good practice to minimize the number of junctions in the amplifier's input signal path. Avoid connectors, sockets, switches and relays where possible. In instances where this is not possible, attempt to balance the number and type of junctions so that differential cancellation occurs. Doing this may involve deliberately introducing junctions to offset unavoidable junctions.

Figure 2 is an example of the introduction of an unnecessary resistor to promote differential thermal balance. Maintaining compensating junctions in close physical proximity will keep them at the same temperature and reduce thermal EMF errors.

When connectors, switches, relays and/or sockets are necessary they should be selected for low thermal EMF activity. The same techniques of thermally balancing and coupling the matching junctions are effective in reducing the thermal EMF errors of these components.

Resistors are another source of thermal EMF errors. Table I shows the thermal EMF generated for different resistors. The temperature gradient across the resistor is important,

Table I. Resistor Thermal EMF

Resistor Type	Thermal EMF/ $^\circ\text{C}$ Gradient
Tin Oxide	$\sim \text{mV}/^\circ\text{C}$
Carbon Composition	$\sim 450\mu\text{V}/^\circ\text{C}$
Metal Film	$\sim 20\mu\text{V}/^\circ\text{C}$
Wire Wound	
Evenohm	$\sim 2\mu\text{V}/^\circ\text{C}$
Manganin	$\sim 2\mu\text{V}/^\circ\text{C}$

not the ambient temperature. There are two junctions formed at each end of the resistor and if these junctions are at the same temperature, their thermal EMFs will cancel each other. The thermal EMF numbers are approximate and vary with resistor value. High values give higher thermal EMF.

When all of these errors are considered, it may seem impossible to take advantage of the extremely low drift specifications of the LTC1052. To show that this is not the case, examine the temperature test circuit of Figure 3. The lead lengths of the resistors connected to the amplifier's inputs are identical. The thermal capacity and thermal resistance each input sees is balanced because of the symmetrical connection of resistors and their identical size. Thermal EMF-induced shifts are equal in phase and amplitude, thus cancellation occurs.

Figure 4 shows the response of this circuit under temperature transient conditions. Metal film resistors and an 8-pin DIP socket were used. Care was taken in the construction to thermally balance the inputs to the amplifier. The units were placed in an oven and allowed to stabilize at 25°C . The recording was started, and after 100 seconds the oven, preset to 125°C , was switched on. The test was first performed on an 8-pin plastic package and then was repeated for a TO-5 package plugged into the same test board. It is significant that the change in V_{OS} , even under these severe thermal transient conditions, is quite good. As temperature stabilizes, note that the steady-state change of V_{OS} is well within the maximum $\pm 0.05\mu\text{V}/^\circ\text{C}$ drift specification.

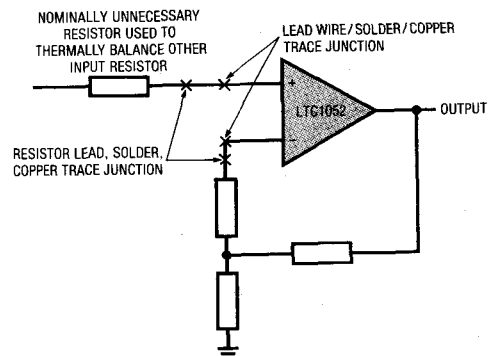


Figure 2

APPLICATIONS INFORMATION

Very slight air currents can still affect even this arrangement. Figure 5 shows strip charts of output noise with the circuit covered and with no cover in "still" air. This data illustrates why it is often prudent to enclose the LTC1052 and its attendant components inside some form of thermal baffle.

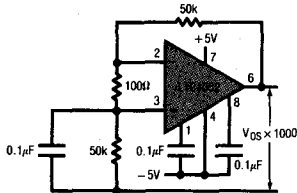


Figure 3. Offset Drift Test Circuit

PACKAGE-INDUCED OFFSET VOLTAGE

Since the LTC1052 is constantly fixing its own offset, it may be asked why there is any error at all, even under transient temperature conditions. The answer is simple. The LTC1052 can only fix offsets inside its own nulling loop. There are many thermal junctions outside this loop that cannot be distinguished from legitimate signals.

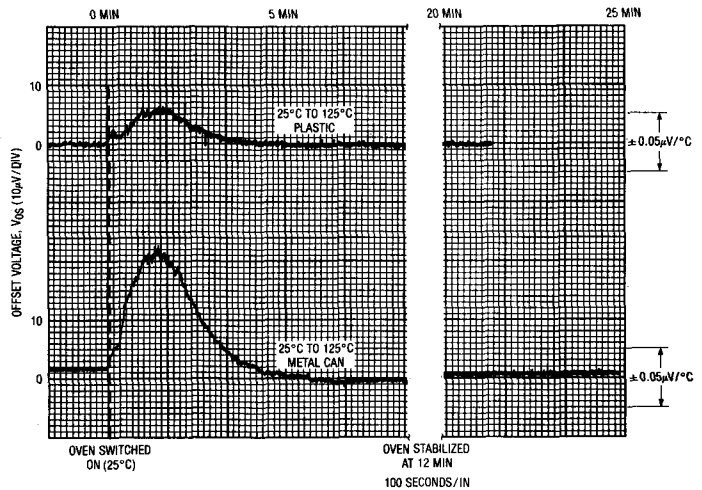


Figure 4. Transient Response of Offset Drift Test Circuit with 100°C Temperature Step

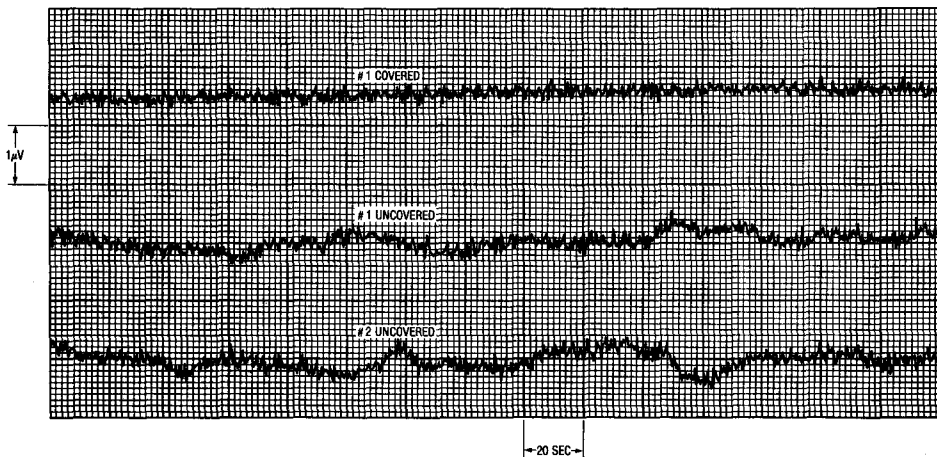


Figure 5. DC to 1Hz (Test Circuit TC3)

APPLICATIONS INFORMATION

Some have been discussed previously, but the package thermal EMF effects are an important source of errors.

Notice the difference in the thermal response curves of Figure 4. This can only be attributed to the package since everything else is identical. In fact, the V_{OS} specification is set by the package-induced warm-up drift, not by the LTC1052. TO-99 metal cans exhibit the worst warm-up drift and Linear Technology sample tests TO-99 lots to minimize this problem.

Two things make 100% screening costly: (1) the extreme precision required on the LTC1052 and (2) the thermal time constant of the package is 0.5 to 3 minutes, depending on package type. The first precludes the use of automatic handling equipment and the second takes a long time. Bench test equipment is available to 100% test for warmed-up drift if offsets of less than $\pm 5\mu V$ are required.

CLOCK

The LTC1052 has an internal clock, setting the nominal sampling frequency at 330Hz. On 8-pin devices there is no way to control the clock externally. In some applications it may be desirable to control the sampling clock and this is the function of the 14-pin device.

CLK IN, CLK OUT and $\overline{INT/\overline{EXT}}$ are provided to accomplish this. With no external connection, an internal pull-up holds $\overline{INT/\overline{EXT}}$ at the V^+ supply and the 14-pin device self-oscillates at 330Hz. In this mode there is a signal on the CLK IN pin of 660Hz (2 times sampling frequency) with a 30% duty cycle. A divide-by-two drives the CLK OUT pin and sets the sampling frequency.

To use an external clock, connect $\overline{INT/\overline{EXT}}$ to V^- and the external clock to CLK IN. The logic threshold of CLK IN is 2.5V below the positive supply. This allows CMOS logic to drive it directly with logic supplies of V^+ and ground. CLK IN can be driven from V^+ to V^- if desired. The duty cycle of the external clock is not particularly critical but should be kept between 30% and 60%.

Capacitance between CLK IN and CLK OUT (pins 13 and 12) can cause the divide-by-two circuit to malfunction. To avoid this, keep this capacitance below 5pF.

OUTPUT CLAMP

If the LTC1052 is driven into saturation, the nulling loop, attempting to force the differential input voltage to zero, will drive C_{EXTA} and C_{EXTB} to a supply rail. After the saturating drive is removed, the capacitors take a finite time to recover—this is the overload recovery time. The overload recovery is longest when the capacitors are driven to the negative rail (see Overload Recovery in typical performance section). The overload recovery time in this case is typically 225ms. In the opposite direction, i.e., C_{EXTA} and C_{EXTB} at positive rail, it is about ten times faster (25ms). The overload recovery time for the LTC1052 is much faster than competitive devices, but if a faster overload recovery time is necessary, the output clamp function can be used.

When the output clamp is connected to the negative input it prevents the amplifier from saturating and thus keeps C_{EXTA} and C_{EXTB} at their nominal voltages. The output clamp is a switch that turns on when the output gets to within approximately 1V of either supply rail. This switch is in parallel with the amplifier's feedback resistor and as the output moves closer to the rail, the switch on-resistance decreases, reducing the closed loop gain. The output swing is reduced when the clamp function is used.

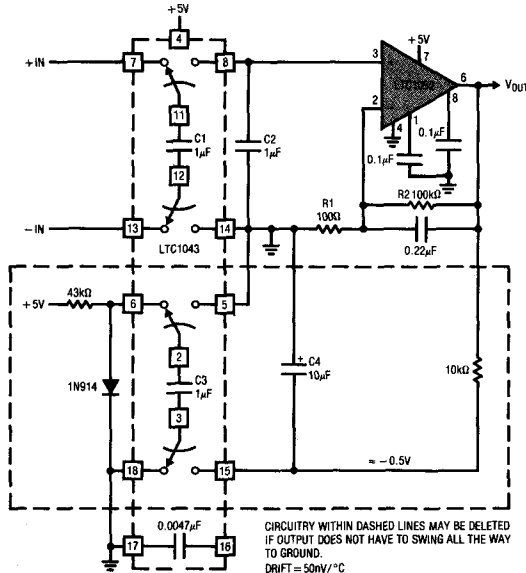
How much current the output clamp leaks when off is important because, when used, it is connected to the amplifier's negative input. Any current acts like input bias current and will degrade accuracy. At the other extreme, the maximum current the clamp conducts when on determines how much overdrive the clamp will take and still keep the amplifier from saturating. Both of these numbers are guaranteed in the table of electrical characteristics.

LOW SUPPLY OPERATION

The minimum supply voltage for proper operation of the LTC1052 is typically 4.0V ($\pm 2.0V$). In single supply applications, PSRR is guaranteed down to 4.7V ($\pm 2.35V$). This assures proper operation down to the minimum TTL specified voltage of 4.75V.

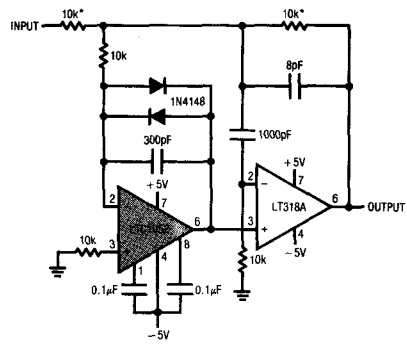
TYPICAL APPLICATIONS

5V Powered Ultra Precision Instrumentation Amplifier



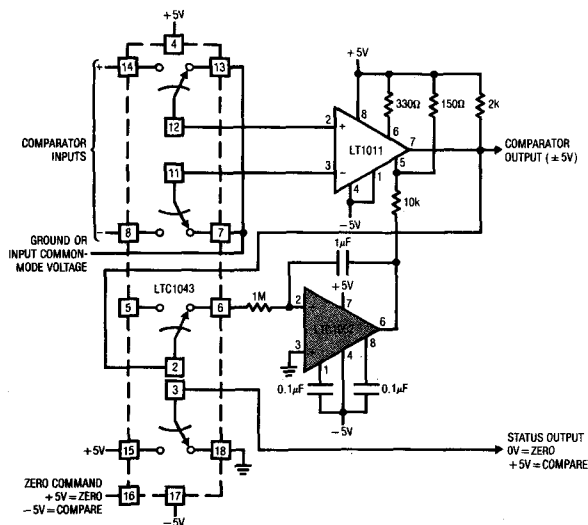
CIRCUITRY WITHIN DASHED LINES MAY BE DELETED IF OUTPUT DOES NOT HAVE TO SWING ALL THE WAY TO GROUND.
 DRIFT = 50nV/°C
 $V_{OS} = 3\mu V$
 $GAIN = \frac{R_2}{R_1} + 1$
 $CMRR = > 120dB$ DC - 20kHz
 BANDWIDTH = 10Hz

Fast Precision Inverter



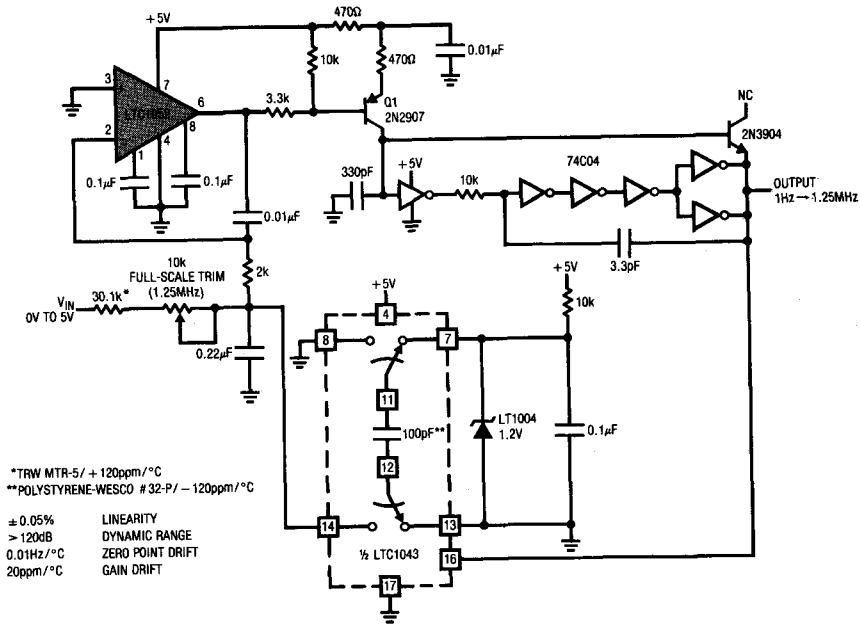
*1% METAL FILM
 FULL POWER BANDWIDTH = 2MHz
 SLEW RATE = 40V/ μs
 SETTLING (10V STEP) = 12 μs TO 0.01%
 BIAS CURRENT DC = 30pA
 OFFSET DRIFT = 50nV/°C
 OFFSET VOLTAGE = 5 μV

Offset Stabilized Comparator



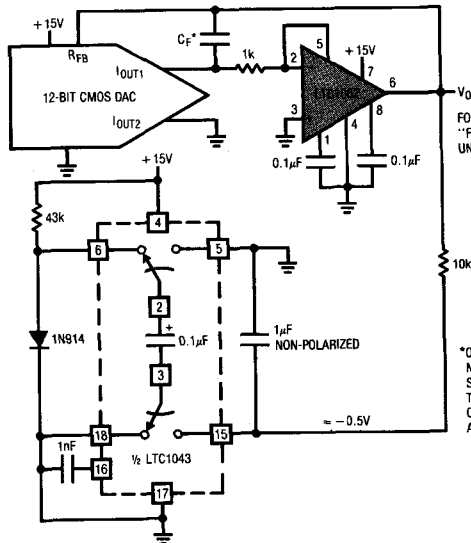
TYPICAL APPLICATIONS

1Hz → 1.25MHz Voltage-to-Frequency Converter (+5V Supply)

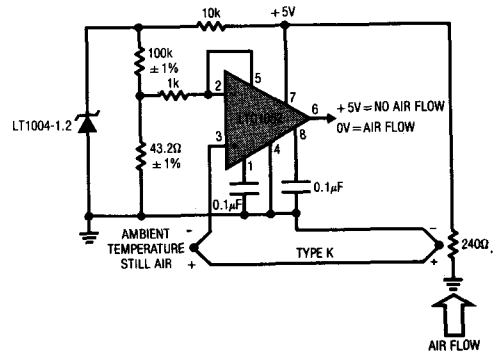


2

No V_{OS} Adjust* CMOS DAC Buffer—Single Supply

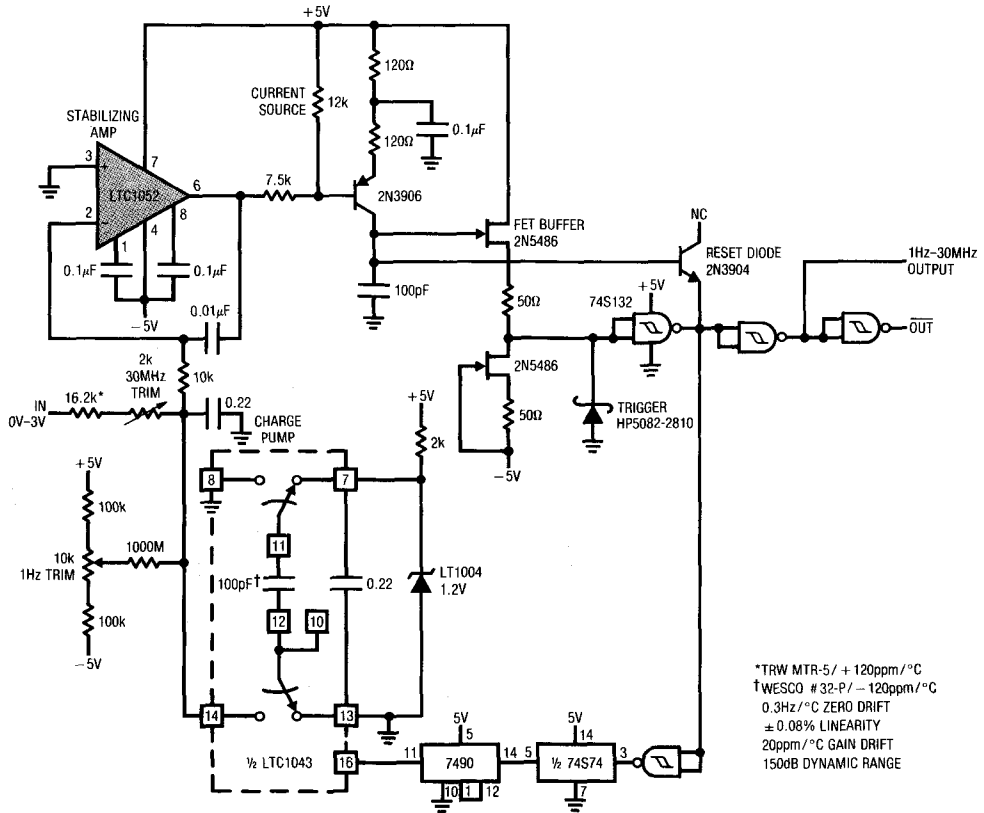


Air Flow Detector



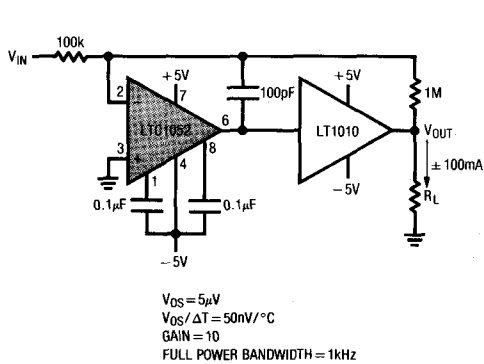
TYPICAL APPLICATIONS

1Hz → 30MHz Voltage-to-Frequency Converter



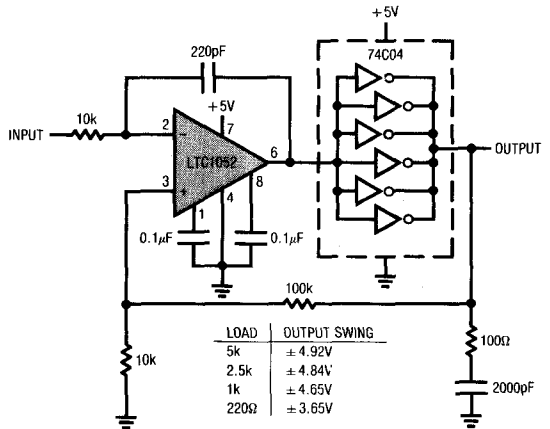
*TRW MTR-5/ +120ppm/°C
 †WESCO #32-P/ -120ppm/°C
 0.3Hz/°C ZERO DRIFT
 ±0.08% LINEARITY
 20ppm/°C GAIN DRIFT
 150dB DYNAMIC RANGE

±100mA Output Drive



$V_{OS} = 5\mu V$
 $V_{OS}/\Delta T = 50nV/^\circ C$
 GAIN = 10
 FULL POWER BANDWIDTH = 1kHz

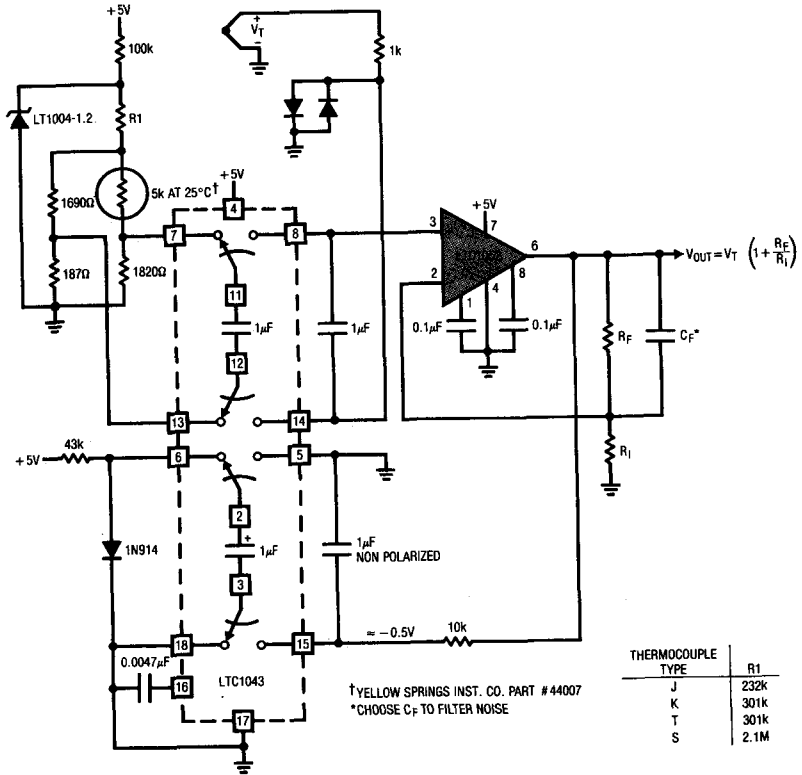
Increasing Output Current



LOAD	OUTPUT SWING
5k	± 4.92V
2.5k	± 4.84V
1k	± 4.65V
220Ω	± 3.65V

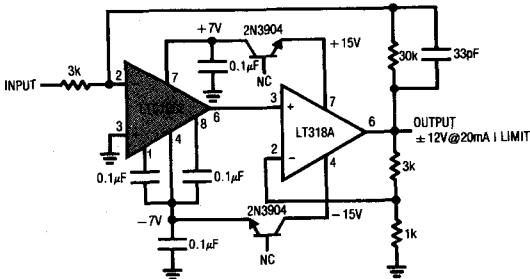
TYPICAL APPLICATIONS

Single +5V Thermocouple Amplifier with Cold Junction Compensation



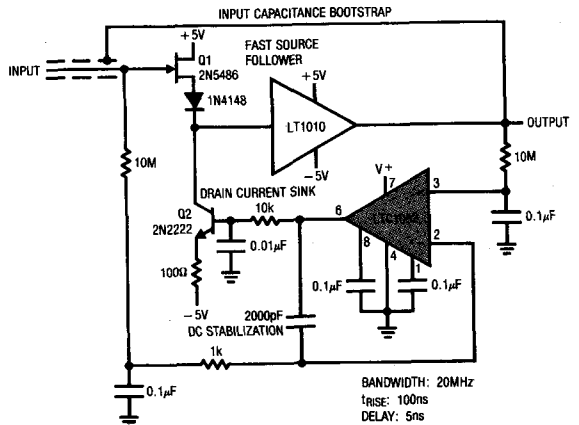
2

Increasing Output Current and Voltage (V_{SUPPLY} = ±15V)



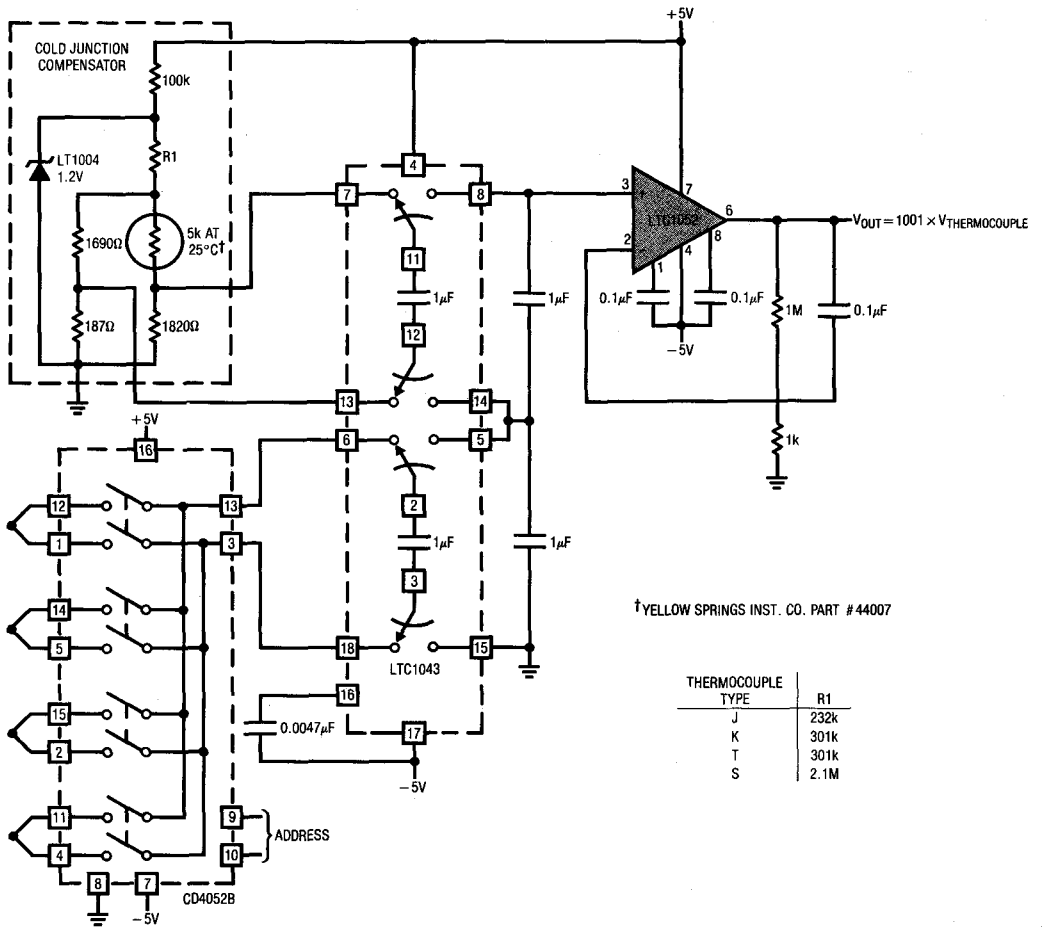
STABLE FOR ALL GAINS, INVERTING AND NON-INVERTING. OBSERVE LTC1052 COMMON-MODE INPUT LIMITS

DC Stabilized FET Probe



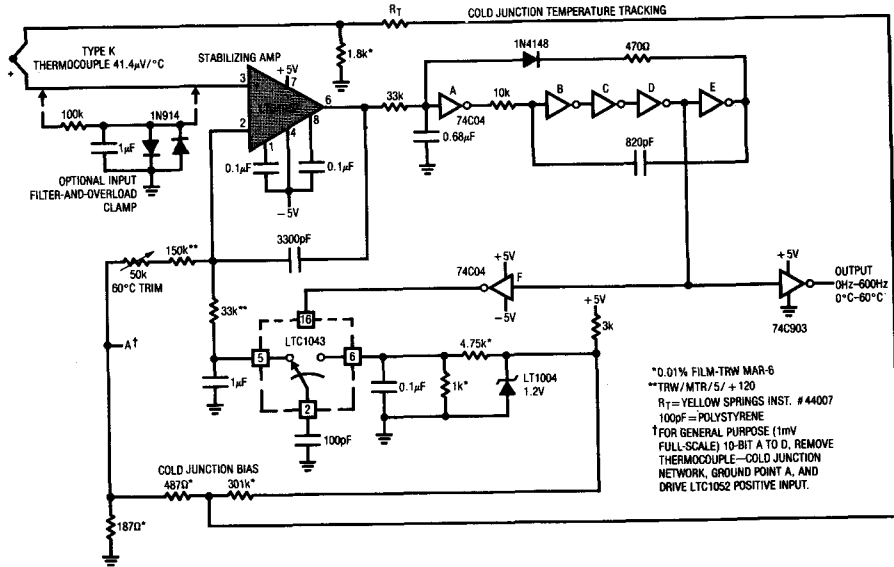
TYPICAL APPLICATIONS

Precision Multiplexed Differential Thermocouple Amplifier



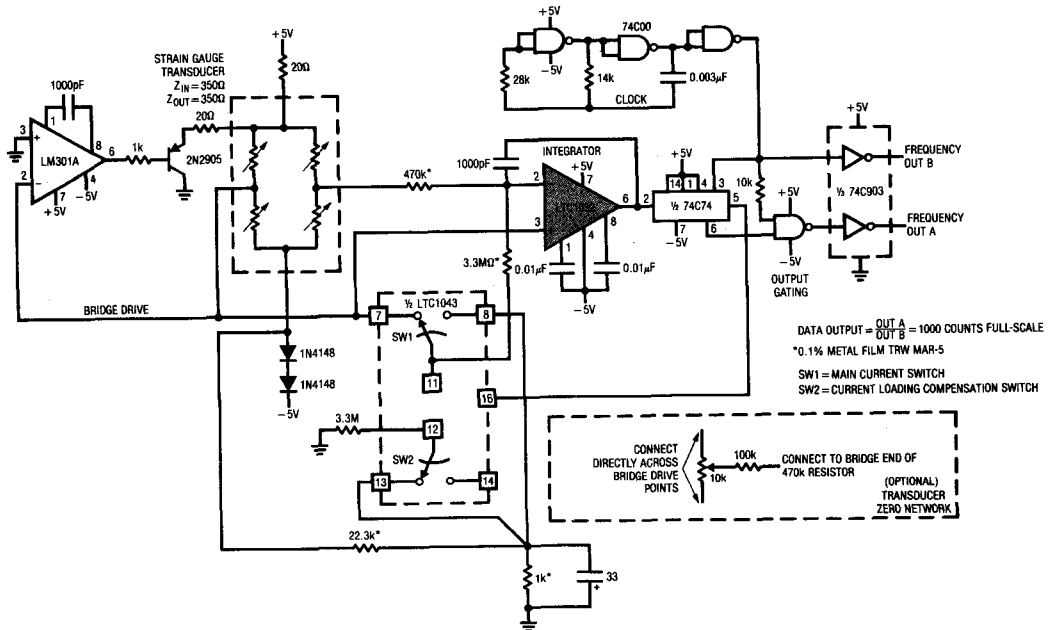
TYPICAL APPLICATIONS

Direct Thermocouple-to-Frequency Converter



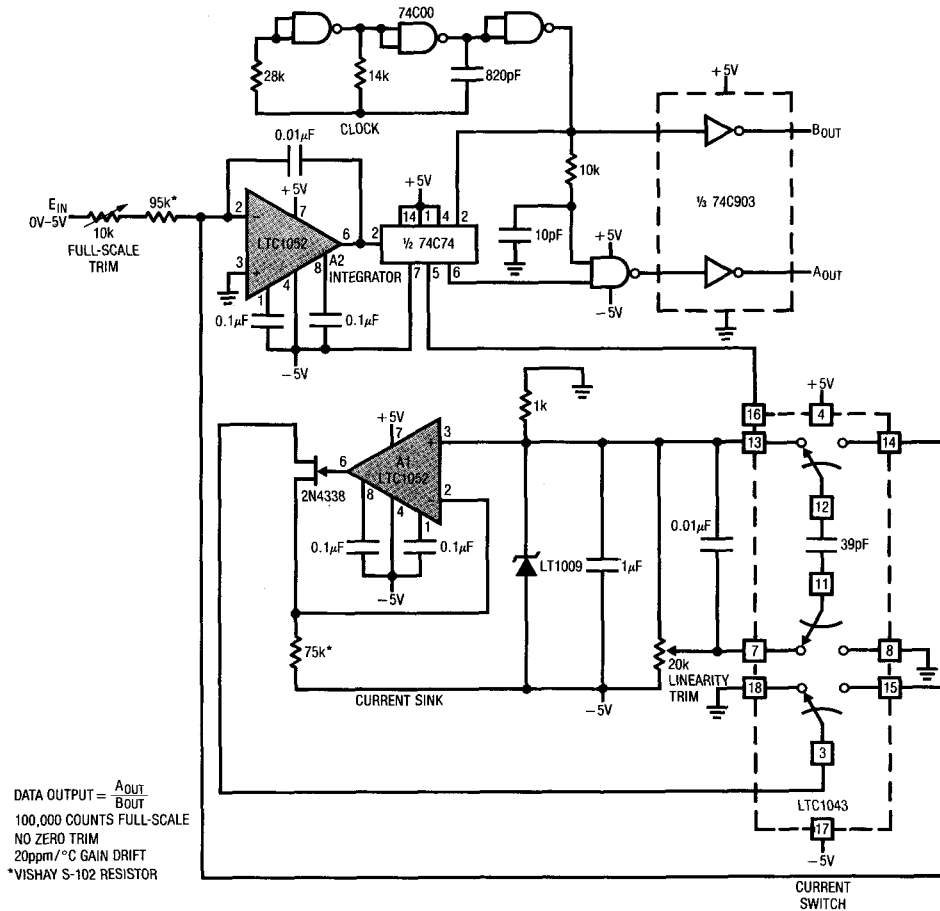
2

Direct 10-Bit Strain Gauge Digitizer



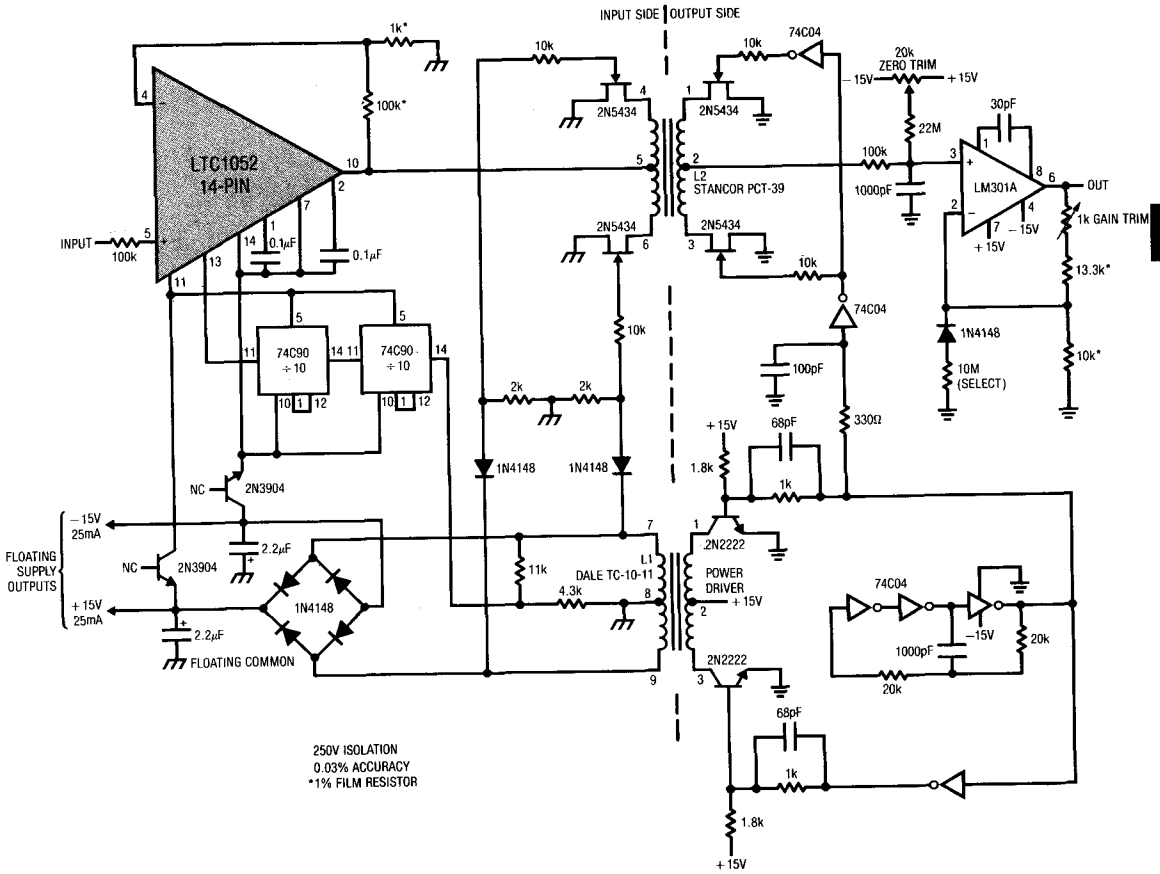
TYPICAL APPLICATIONS

16-Bit A → D Converter



TYPICAL APPLICATIONS

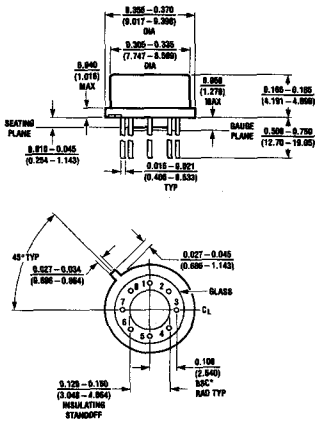
Precision Isolation Amplifier



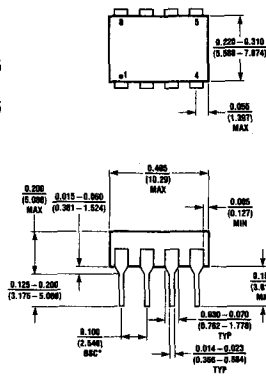
2

PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

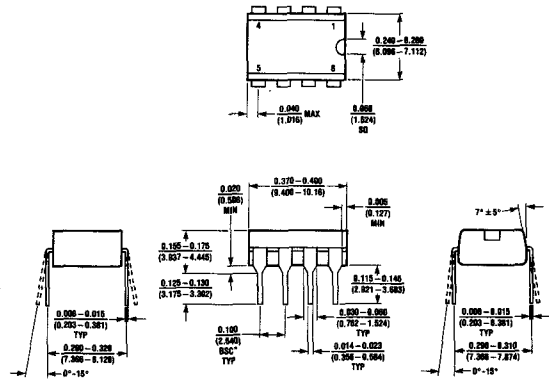
**H Package
Metal Can**



**J8 Package
8 Lead Hermetic Dip**



**N8 Package
8 Lead Plastic**



*LEADS WITHIN 0.007 OF TRUE POSITION (TP) AT GAUGE PLANE

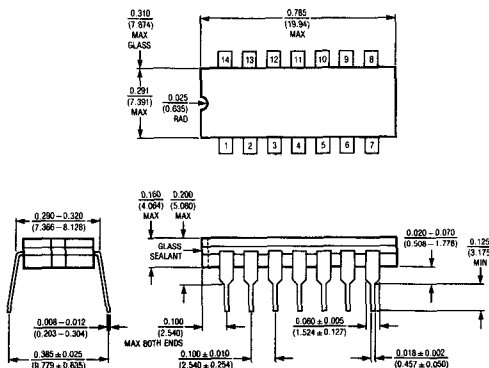
*LEADS WITHIN 0.007 OF TRUE POSITION (TP) AT GAUGE PLANE

T _{jmax} 150°C	Θ _{JA} 150°C/W	Θ _{Jc} 45°C/W
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T _{jmax} 150°C	Θ _{JA} 100°C/W
----------------------------	----------------------------

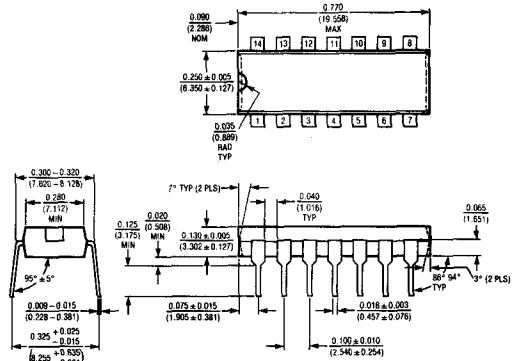
T _{jmax} 110°C	Θ _{JA} 150°C/W
----------------------------	----------------------------

**J Package
14-Lead Hermetic DIP**



T _{jmax} 150°C	Θ _{JA} 80°C/W
----------------------------	---------------------------

**N Package
14-Lead Plastic**



T _{jmax} 110°C	Θ _{JA} 130°C/W
----------------------------	----------------------------

FEATURES

- *Guaranteed* Max. Offset 5 μ V
- *Guaranteed* Max. Offset Drift 0.05 μ V/°C
- Typ. Offset Drift 0.01 μ V/°C
- Excellent Long Term Stability 100nV/ $\sqrt{\text{Month}}$
- *Guaranteed* Max. Input Bias Current 30pA
- Over Operating Temperature Range
 - Guaranteed* Min. Gain 120dB
 - Guaranteed* Min. CMRR 120dB
 - Guaranteed* Min. PSRR 120dB
- Single Supply Operation 4.75V to 16V
 (Input Voltage Range Extends to Ground)
- External Capacitors can be Returned to V⁻ with No Noise Degradation

APPLICATIONS

- Thermocouple Amplifiers
- Strain Gauge Amplifiers
- Low Level Signal Processing
- Medical Instrumentation

DESCRIPTION

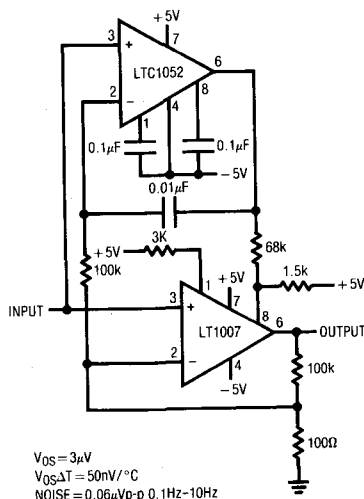
The LTC1052 is a low noise chopper-stabilized op amp (CSOA) manufactured using Linear Technology's enhanced LTCMOS™ silicon gate process. Chopper-stabilization constantly corrects offset voltage errors. Both initial offset and changes in the offset due to time, temperature and common-mode voltage are corrected. This, coupled with picoampere input currents, gives this amplifier unmatched performance.

Low frequency (1/f) noise is also improved by the chopping technique. Instead of increasing continuously at a 3dB/octave rate, the internal chopping causes noise to decrease at low frequencies.

The chopper circuitry is entirely internal and completely transparent to the user. Only two external capacitors are required to alternately sample and hold the offset correction voltage and the amplified input signal. Control circuitry is brought out on the 14-pin version to allow the sampling of the LTC1052 to be synchronized with an external frequency source.

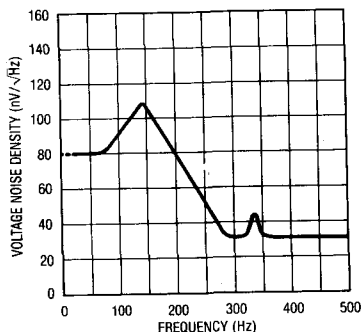
The LTC1052CS is a direct replacement for the ICL7652 in surface mounted packages.

Ultra Low Noise, Low Drift Amplifier



$V_{OS} = 3\mu\text{V}$
 $V_{OSAT} = 50\text{nV}/^\circ\text{C}$
 NOISE = 0.06 $\mu\text{Vp-p}$ 0.1Hz-10Hz

LTC1052 Noise Spectrum



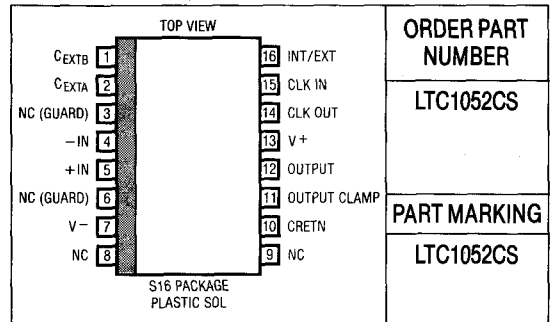
CSOA™ and LTCMOS™ are trademarks of Linear Technology Corporation.
 Teflon™ is a trademark of DuPont.

ABSOLUTE MAXIMUM RATINGS

(Notes 1 and 2)

Total Supply Voltage (V^+ to V^-).....	18V
Input Voltage..... ($V^+ + 0.3V$) to ($V^- - 0.3V$)	
Output Short Circuit Duration.....	Indefinite
Operating Temperature Range.....	-40°C to 85°C
Storage Temperature Range.....	-65°C to 150°C
Lead Temperature (Soldering, 10 sec.).....	300°C

PACKAGE/ORDER INFORMATION



ELECTRICAL CHARACTERISTICS

$V_S = \pm 15V$, $T_A =$ operating temperature range, test circuit TC1 (Note 6), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	LTC1052C		UNITS
			MIN	TYP MAX	
V_{OS}	Input Offset Voltage	$T_A = 25^\circ\text{C}$ (Note 3)		± 0.5 ± 5	μV
$\frac{\Delta V_{OS}}{\Delta \text{Temp}}$	Average Input Offset Drift	(Note 3)	●	± 0.01 ± 0.05	$\mu\text{V}/^\circ\text{C}$
$\frac{\Delta V_{OS}}{\Delta \text{Time}}$	Long Term Offset Voltage Stability			100	nV/ $\sqrt{\text{Month}}$
I_{OS}	Input Offset Current	$T_A = 25^\circ\text{C}$	●	± 5 ± 30 ± 350	pA pA
I_B	Input Bias Current	$T_A = 25^\circ\text{C}$	●	± 1 ± 30 ± 175	pA pA
e_{npp}	Input Noise Voltage	$R_S = 100\Omega$, DC to 10Hz, TC3 (Note 6) $R_S = 100\Omega$, DC to 1Hz, TC3 (Note 6)		1.5 0.5	$\mu\text{Vp-p}$ $\mu\text{Vp-p}$
i_n	Input Noise Current	$f = 10\text{Hz}$ (Note 5)		0.6	fA/ $\sqrt{\text{Hz}}$
CMRR	Common-Mode Rejection Ratio	$V_{CM} = V^-$ to $+2.7V$	●	120 140	dB
PSRR	Power Supply Rejection Ratio	$V_{SUPPLY} = \pm 2.375V$ to $\pm 8V$	●	120 150	dB
A_{VOL}	Large Signal Voltage Gain	$R_L = 10k$, $V_{OUT} = \pm 4V$	●	120 150	dB
V_{OUT}	Maximum Output Voltage Swing (Note 4)	$R_L = 10k$ $R_L = 100k$	●	± 4.7 ± 4.85 ± 4.95	V V
SR	Slew Rate	$R_L = 10k$, $C_L = 50pF$		4	V/ μs
GBW	Gain Bandwidth Product			1.2	MHz
I_S	Supply Current	No Load, $T_A = 25^\circ\text{C}$	●	1.7 2.0 3.0	mA mA
f_S	Internal Sampling Frequency			330	Hz
	Clamp On Current	$R_L = 100k$	●	25 100	μA
	Clamp Off Current	$-4V < V_{OUT} < +4V$	●	10 100 1	pA nA

The ● denotes specifications which apply over the full operating temperature range.

Note 1: Absolute Maximum Ratings are those values beyond which the life of the device may be impaired.

Note 2: Connecting any terminal to voltages greater than V^+ or less than V^- may cause destructive latch-up. It is recommended that no sources operating from external supplies be applied prior to power-up of the LTC1052.

Note 3: These parameters are guaranteed by design. Thermocouple effects preclude measurement of these voltage levels in high speed automatic

testing. V_{OS} is measured to a limit determined by test equipment capability. Voltages on C_{EXTA} and C_{EXTB} , A_{VOL} , CMRR and PSRR are measured to insure proper operation of the nulling loop to insure meeting the V_{OS} and V_{OS} drift specifications.

Note 4: Output clamp not connected.

Note 5: Current noise is calculated from the formula: $i_n = (2q I_B)^{1/2}$, where $q = 1.6 \times 10^{-19}$ coulomb.

Note 6: For description of test circuits see LTC1052 standard package data sheet.

FEATURES

- *Guaranteed* Offset Voltage
 -55°C to +125°C
- *Guaranteed* Drift
- *Guaranteed* Bias Current
 70°C
 125°C
- *Guaranteed* Slew Rate

150 μ V Max.
 500 μ V Max.
 4 μ V/°C Max.

150pA Max.
 2.5nA Max.
 12V/ μ s Min.

DESCRIPTION

The LT1055/1056 JFET input operational amplifiers combine precision specifications with high speed performance.

For the first time, 16V/ μ s slew rate and 6.5MHz gain-bandwidth product are simultaneously achieved with offset voltage of typically 50 μ V, 1.2 μ V/°C drift, bias currents of 40pA at 70°C and 500pA at 125°C.

The 150 μ V maximum offset voltage specification is the best available on any JFET input operational amplifier.

The LT1055 and LT1056 are differentiated by their operating currents. The lower power dissipation LT1055 achieves lower bias and offset currents and offset voltage. The additional power dissipation of the LT1056 permits higher slew rate, bandwidth and faster settling time with a slight sacrifice in DC performance.

The voltage to frequency converter shown below is one of the many applications which utilize both the precision and high speed of the LT1055/1056.

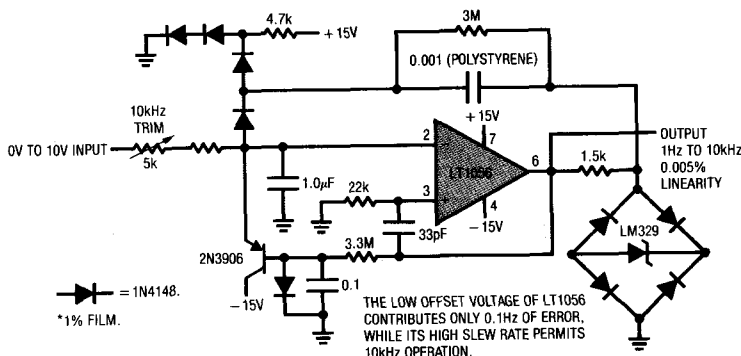
For a JFET input op amp with 23V/ μ s guaranteed slew rate, refer to the LT1022 data sheet.

2

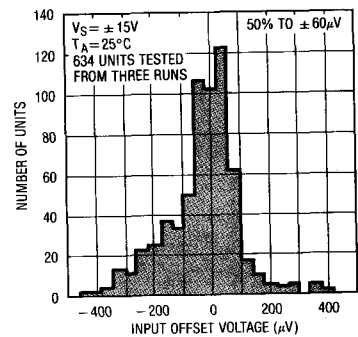
APPLICATIONS

- Precision, High Speed Instrumentation
- Logarithmic Amplifiers
- D/A Output Amplifiers
- Photodiode Amplifiers
- Voltage to Frequency Converters
- Frequency to Voltage Converters
- Fast, Precision Sample and Hold

0 to 10kHz Voltage-to-Frequency Converter



Distribution of Input Offset Voltage (H Package)



LT1055/LT1056

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	± 20V
Differential Input Voltage	± 40V
Input Voltage	± 20V
Output Short Circuit Duration	Indefinite
Operating Temperature Range	
LT1055AM / 1055M / 1056AM / 1056M	− 55°C to 125°C
LT1055AC / 1055C / 1056AC / 1056C	0°C to 70°C
Storage Temperature Range	
All Devices	− 65°C to 150°C
Lead Temperature (Soldering, 10 sec.)	300°C

PACKAGE/ORDER INFORMATION

TOP VIEW		ORDER PART NUMBER	
<p>METAL CAN H PACKAGE</p>		LT1055AMH	LT1056AMH
		LT1055MH	LT1056MH
		LT1055ACH	LT1056ACH
		LT1055CH	LT1056CH
<p>PLASTIC DIP N8 PACKAGE</p>		LT1055CN8 LT1056CN8	

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $T_A = 25^\circ C$, $V_{CM} = 0V$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1055AM / 1056AM LT1055AC / 1056AC			LT1055M / 1056M LT1055CH / 1056CH LT1055CN8 / 1056CN8			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage (Note 1)	LT1055 H Package LT1056 H Package LT1055 N8 Package LT1056 N8 Package	—	50	150	—	70	400	μV
I_{OS}	Input Offset Current	Fully Warmed Up	—	2	10	—	2	20	pA
I_B	Input Bias Current	Fully Warmed Up $V_{CM} = +10V$	—	± 10	± 50	—	± 10	± 50	pA
	Input Resistance—Differential —Common-Mode	$V_{CM} = -11V$ to +8V $V_{CM} = +8V$ to +11V	—	10^{12}	—	—	10^{12}	—	Ω
	Input Capacitance		—	10^{11}	—	—	10^{11}	—	Ω
e_n	Input Noise Voltage	0.1 Hz to 10 Hz LT1055 LT1056	—	1.8	—	—	2.0	—	μV_{p-p}
e_n	Input Noise Voltage Density	$f_0 = 10Hz$ (Note 2) $f_0 = 1kHz$ (Note 3)	—	28	50	—	30	60	nV/\sqrt{Hz}
I_n	Input Noise Current Density	$f_0 = 10Hz, 1kHz$ (Note 4)	—	1.8	4	—	1.8	4	fA/\sqrt{Hz}
A_{VOL}	Large Signal Voltage Gain	$V_0 = \pm 10V$ $R_L = 2k$ $R_L = 1k$	150	400	—	120	400	—	V/mV
	Input Voltage Range		± 11	± 12	—	± 11	± 12	—	V
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm 11V$	86	100	—	83	98	—	dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 10V$ to ± 18V	90	106	—	88	104	—	dB
V_{OUT}	Output Voltage Swing	$R_L = 2k$	± 12	± 13.2	—	± 12	± 13.2	—	V
SR	Slew Rate	LT1055 LT1056	10	13	—	7.5	12	—	V/ μs
GBW	Gain Bandwidth Product	$f = 1MHz$ LT1055 LT1056	—	5.0	—	—	4.5	—	MHz
I_S	Supply Current	LT1055 LT1056	—	2.8	4.0	—	2.8	4.0	mA
	Offset Voltage Adjustment Range	$R_{POT} = 100k$	—	± 5	—	—	± 5	—	mV

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $V_{CM} = 0V$, $0^\circ C \leq T_A \leq 70^\circ C$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1055AC LT1056AC			LT1055CH/1056CH LT1055CN8/1056CN8			UNITS	
			MIN	TYP	MAX	MIN	TYP	MAX		
V_{OS}	Input Offset Voltage (Note 1)	LT1055 H Package	●	—	100	330	—	140	750	μV
		LT1056 H Package	●	—	100	360	—	140	800	μV
		LT1055 N8 Package	●	—	—	—	—	250	1250	μV
		LT1056 N8 Package	●	—	—	—	—	280	1350	μV
	Average Temperature Coefficient of Input Offset Voltage	H Package (Note 5)	●	—	1.2	4.0	—	1.6	8.0	$\mu V/^\circ C$
		N8 Package (Note 5)	●	—	—	—	—	3.0	12.0	$\mu V/^\circ C$
I_{OS}	Input Offset Current	Warmed Up $T_A = 70^\circ C$	●	—	10	50	—	16	80	pA
		LT1055 LT1056	●	—	14	70	—	18	100	pA
I_B	Input Bias Current	Warmed Up $T_A = 70^\circ C$	●	—	± 30	± 150	—	± 40	± 200	pA
		LT1055 LT1056	●	—	± 40	± 180	—	± 50	± 240	pA
A_{VOL}	Large Signal Voltage Gain	$V_O = \pm 10V$, $R_L = 2k$	●	80	250	—	60	250	—	V/mV
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm 10.5V$	●	85	100	—	82	98	—	dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 10V$ to $\pm 18V$	●	89	105	—	87	103	—	dB
V_{OUT}	Output Voltage Swing	$R_L = 2k$	●	± 12	± 13.1	—	± 12	± 13.1	—	V

2

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $V_{CM} = 0V$, $-55^\circ C \leq T_A \leq 125^\circ C$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1055AM LT1056AM			LT1055M LT1056M			UNITS	
			MIN	TYP	MAX	MIN	TYP	MAX		
V_{OS}	Input Offset Voltage (Note 1)	LT1055	●	—	180	500	—	250	1200	μV
		LT1056	●	—	180	550	—	250	1250	μV
	Average Temperature Coefficient of Input Offset Voltage	(Note 5)	●	—	1.3	4.0	—	1.8	8.0	$\mu V/^\circ C$
I_{OS}	Input Offset Current	Warmed Up $T_A = 125^\circ C$	●	—	0.20	1.2	—	0.25	1.8	nA
		LT1055 LT1056	●	—	0.25	1.5	—	0.30	2.4	nA
I_B	Input Bias Current	Warmed Up $T_A = 125^\circ C$	●	—	± 0.4	± 2.5	—	± 0.5	± 4.0	nA
		LT1055 LT1056	●	—	± 0.5	± 3.0	—	± 0.6	± 5.0	nA
A_{VOL}	Large Signal Voltage Gain	$V_O = \pm 10V$, $R_L = 2k$	●	40	120	—	35	120	—	V/mV
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm 10.5V$	●	85	100	—	82	98	—	dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 10V$ to $\pm 17V$	●	88	104	—	86	102	—	dB
V_{OUT}	Output Voltage Swing	$R_L = 2k$	●	± 12	± 12.9	—	± 12	± 12.9	—	V

The ● denotes the specifications which apply over the full operating temperature range.

For MIL-STD components, please refer to LTC883 data sheet for test listing and parameters.

Note 1: Offset voltage is measured under two different conditions: (a) approximately 0.5 seconds after application of power; (b) at $T_A = 25^\circ C$ only, with the chip heated to approximately $38^\circ C$ for the LT1055 and to $45^\circ C$ for the LT1056, to account for chip temperature rise when the device is fully warmed up.

Note 2: 10Hz noise voltage density is sample tested on every lot of A grades. Devices 100% tested at 10Hz are available on request.

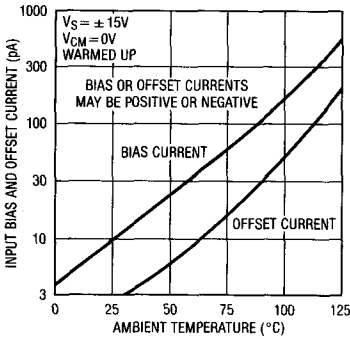
Note 3: This parameter is tested on a sample basis only.

Note 4: Current noise is calculated from the formula: $i_n = (2q|I_B|)^{1/2}$, where $q = 1.6 \times 10^{-19}$ coulomb. The noise of source resistors up to 1GΩ swamps the contribution of current noise.

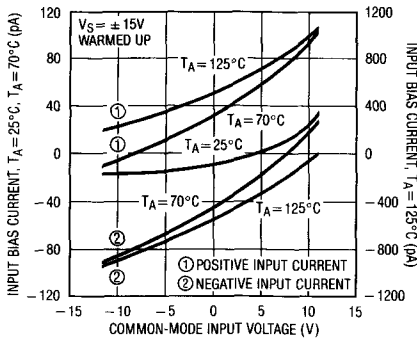
Note 5: Offset voltage drift with temperature is practically unchanged when the offset voltage is trimmed to zero with a 100k potentiometer between the balance terminals and the wiper tied to V^+ . Devices tested to tighter drift specifications are available on request.

TYPICAL PERFORMANCE CHARACTERISTICS

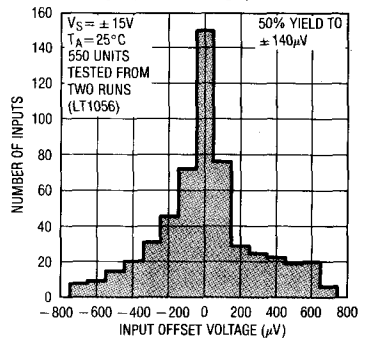
Input Bias and Offset Currents vs Temperature



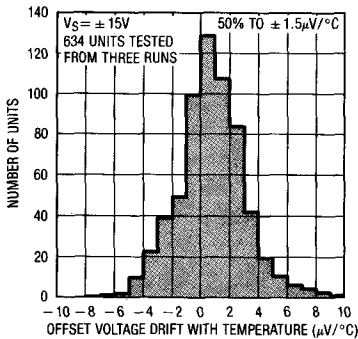
Input Bias Current Over the Common-Mode Range



Distribution of Input Offset Voltage (N8 Package)

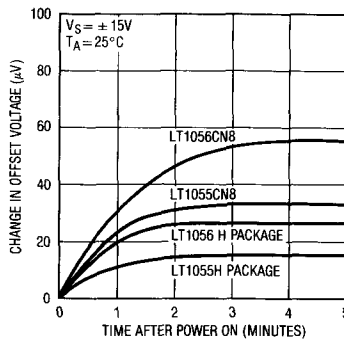


Distribution of Offset Voltage Drift with Temperature (H Package)*

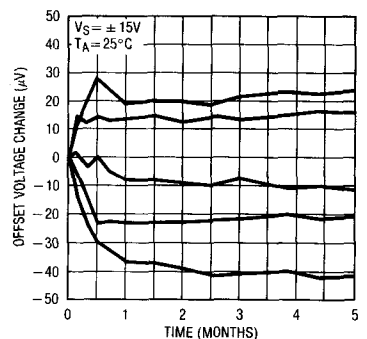


*DISTRIBUTION IN THE PLASTIC (N8) PACKAGE IS SIGNIFICANTLY WIDER.

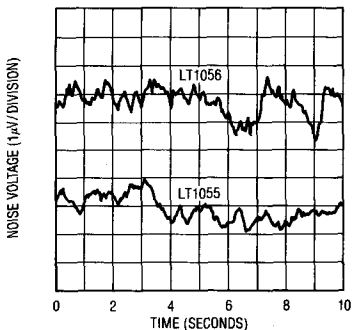
Warm-Up Drift



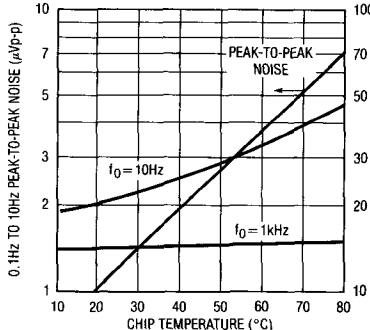
Long Term Drift of Representative Units



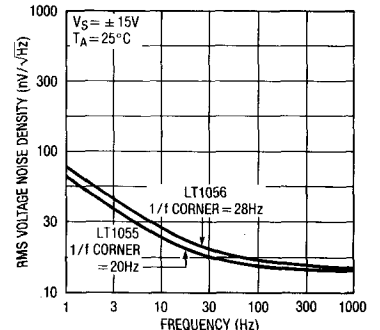
0.1Hz to 10Hz Noise



Noise vs Chip Temperature

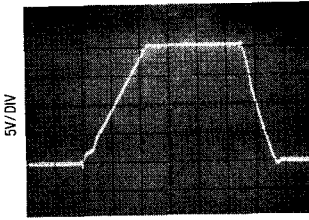


Voltage Noise vs Frequency



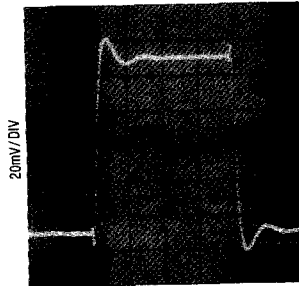
TYPICAL PERFORMANCE CHARACTERISTICS

LT1056 Large Signal Response



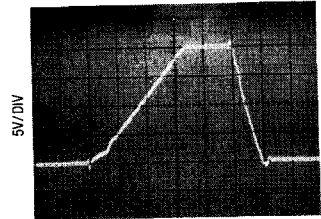
$A_V = +1$, $C_L = 100\text{pF}$, $0.5\mu\text{s}/\text{DIV}$

Small Signal Response



$A_V = +1$, $C_L = 100\text{pF}$, $0.2\mu\text{s}/\text{DIV}$

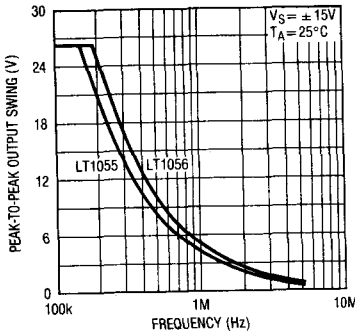
LT1055 Large Signal Response



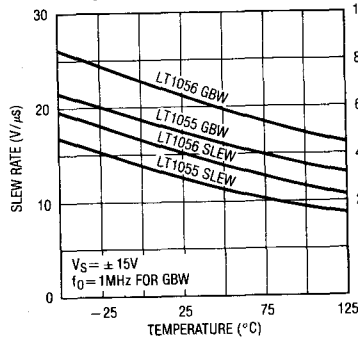
$A_V = 1$, $C_L = 100\text{pF}$, $0.5\mu\text{s}/\text{DIV}$

2

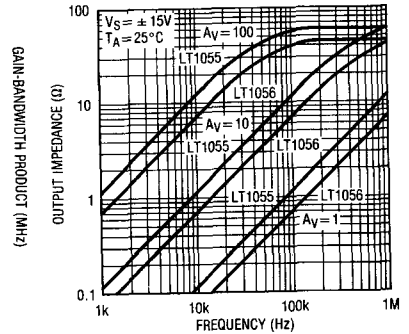
Undistorted Output Swing vs Frequency



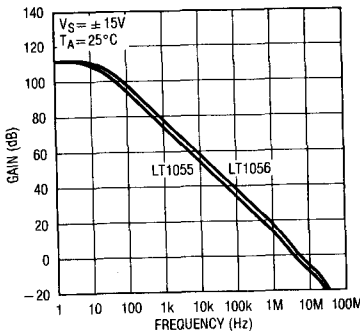
Slew Rate, Gain-Bandwidth vs Temperature



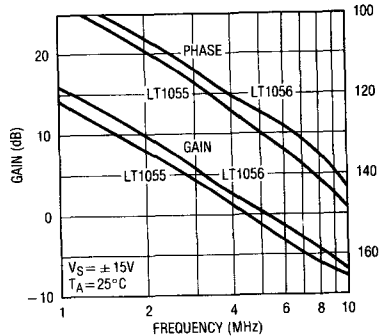
Output Impedance vs Frequency



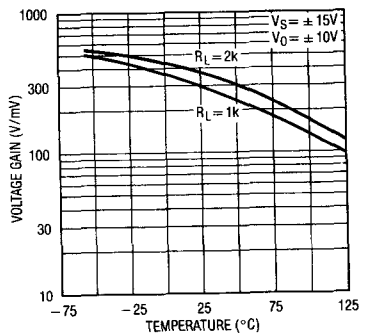
Gain vs Frequency



Gain, Phase Shift vs Frequency

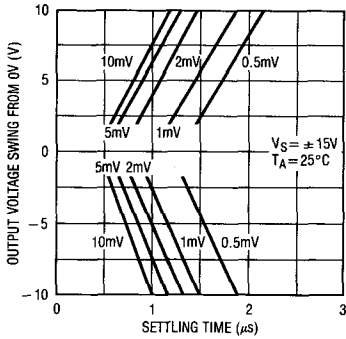


Voltage Gain vs Temperature

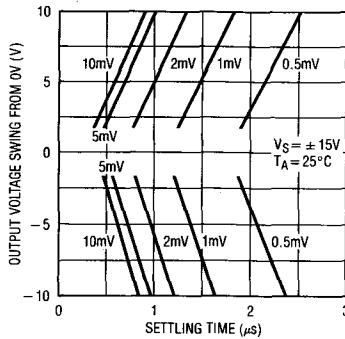


TYPICAL PERFORMANCE CHARACTERISTICS

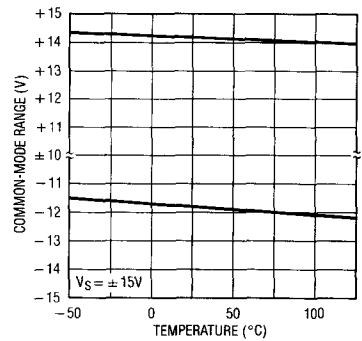
LT1055 Settling Time



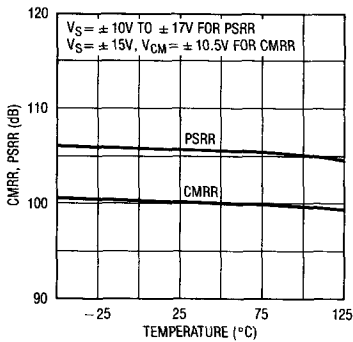
LT1056 Settling Time



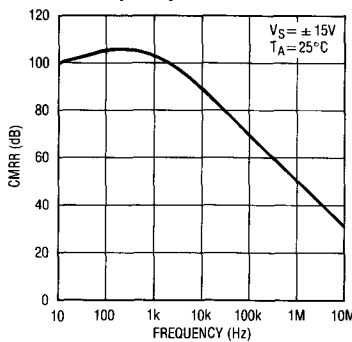
Common-Mode Range vs Temperature



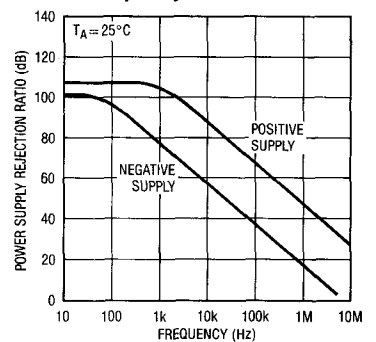
Common-Mode and Power Supply Rejections vs Temperature



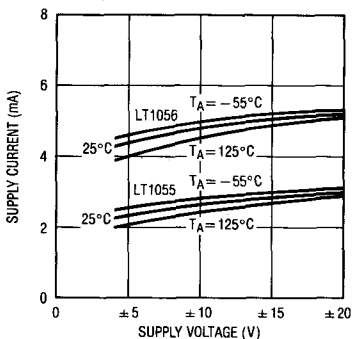
Common-Mode Rejection Ratio vs Frequency



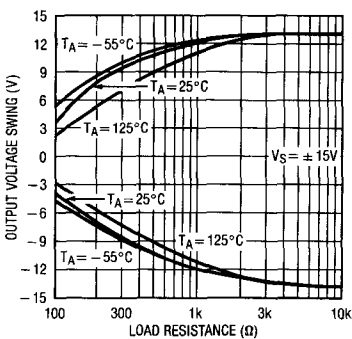
Power Supply Rejection Ratio vs Frequency



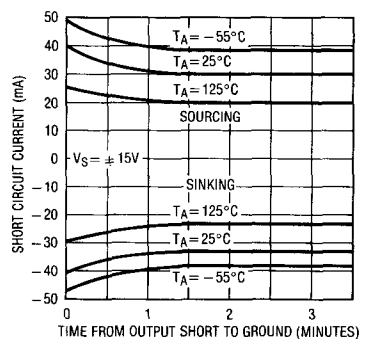
Supply Current vs Supply Voltage



Output Swing vs Load Resistance



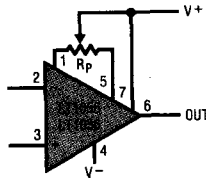
Short Circuit Current vs Time



APPLICATIONS INFORMATION

The LT1055/1056 may be inserted directly into LF155A/355A, LF156A/356A, OP-15 and OP-16 sockets. Offset nulling will be compatible with these devices with the wiper of the potentiometer tied to the positive supply.

Offset Nulling



No appreciable change in offset voltage drift with temperature will occur when the device is nulled with a potentiometer, R_p , ranging from 10k to 200k.

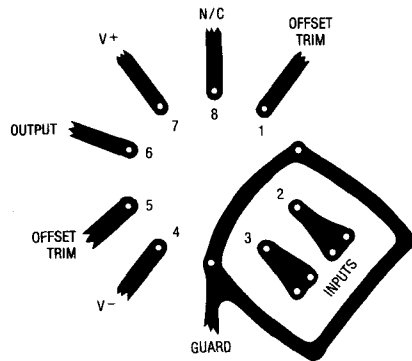
The LT1055/1056 can also be used in LF351, LF411, AD547, AD611, OPA-111, and TL081 sockets, provided that the nulling circuitry is removed. Because of the LT1055/1056's low offset voltage, nulling will not be necessary in most applications.

Achieving Picoampere/Microvolt Performance

In order to realize the picoampere-microvolt level accuracy of the LT1055/1056 proper care must be exercised. For example, leakage currents in circuitry external to the op amp can significantly degrade performance. High quality insulation should be used (e.g. Teflon™, Kel-F); cleaning of all insulating surfaces to remove fluxes and other residues will probably be required. Surface coating may be necessary to provide a moisture barrier in high humidity environments.

Board leakage can be minimized by encircling the input circuitry with a guard ring operated at a potential close to that of the inputs: in inverting configurations the guard ring should be tied to ground, in non-inverting connections to the inverting input at pin 2. Guarding both sides of the printed circuit board is required. Bulk leakage reduction depends on the guard ring width.

Teflon™ is a trademark of DuPont.



The LT1055/1056 has the lowest offset voltage of any JFET input op amp available today. However, the offset voltage and its drift with time and temperature are still not as good as on the best bipolar amplifiers because the transconductance of FETs is considerably lower than that of bipolar transistors. Conversely, this lower transconductance is the main cause of the significantly faster speed performance of FET input op amps.

Offset voltage also changes somewhat with temperature cycling. The AM grades show a typical $20\mu\text{V}$ hysteresis ($30\mu\text{V}$ on the M grades) when cycled over the -55°C to 125°C temperature range. Temperature cycling from 0°C to 70°C has a negligible (less than $10\mu\text{V}$) hysteresis effect.

The offset voltage and drift performance are also affected by packaging. In the plastic N8 package the molding compound is in direct contact with the chip, exerting pressure on the surface. While NPN input transistors are largely unaffected by this pressure, JFET device matching and drift are degraded. Consequently, for best DC performance, as shown in the typical performance distribution plots, the TO-5 H package is recommended.

Noise Performance

The current noise of the LT1055/1056 is practically immeasurable at $1.8\text{fA}/\sqrt{\text{Hz}}$. At 25°C it is negligible up to $1\text{G}\Omega$ of source resistance, R_s (compared to the noise of R_s). Even at 125°C it is negligible to $100\text{M}\Omega$ of R_s .

APPLICATIONS INFORMATION

The voltage noise spectrum is characterized by a low 1/f corner in the 20Hz to 30Hz range, significantly lower than on other competitive JFET input op amps. Of particular interest is the fact that, with any JFET IC amplifier, the frequency location of the 1/f corner is proportional to the square root of internal gate leakage currents and, therefore, noise doubles every 20°C. Furthermore, as illustrated in the noise versus chip temperature curves, the 0.1Hz to 10Hz peak-to-peak noise is a strong function of temperature, while wideband noise ($f_0 = 1\text{kHz}$) is practically unaffected by temperature.

Consequently, for optimum low frequency noise, chip temperature should be minimized. For example, operating an LT1056 at $\pm 5\text{V}$ supplies or with a 20°C/W case-to-ambient heat sink reduces 0.1Hz to 10Hz noise from typically 2.5 $\mu\text{Vp-p}$ ($\pm 15\text{V}$, free-air) to 1.5 $\mu\text{Vp-p}$. Similarly, the noise of an LT1055 will be 1.8 $\mu\text{Vp-p}$ typically because of its lower power dissipation and chip temperature.

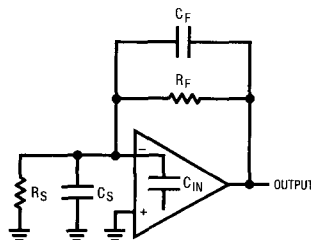
High Speed Operation

Settling time is measured in the test circuit shown. This test configuration has two features which eliminate problems common to settling time measurements: (1) probe capacitance is isolated from the "false summing" node, and (2) it does not require a "flat top" input pulse since

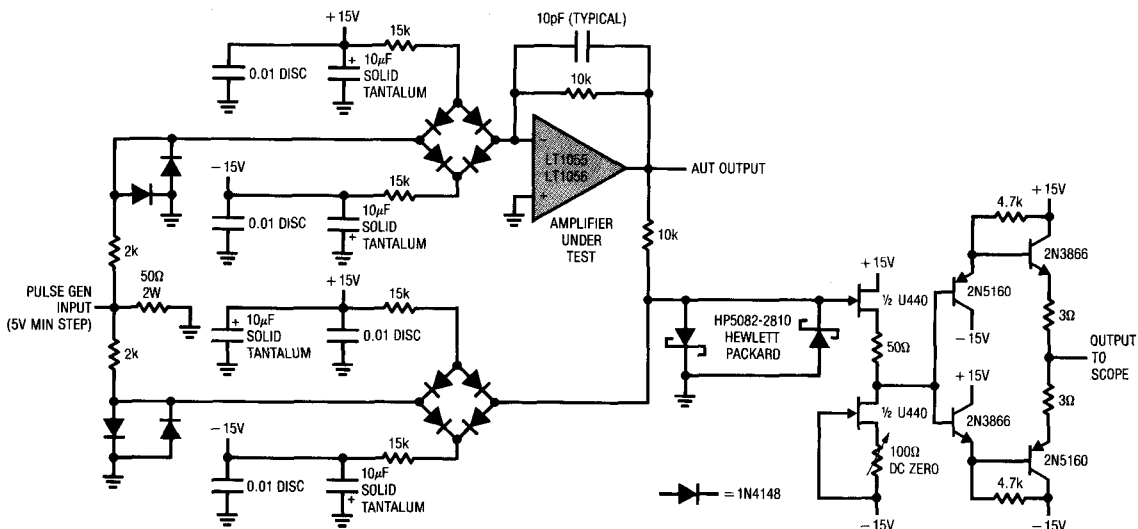
the input pulse is merely used to steer current through the diode bridges. For more details, please see Application Note 10.

As with most high speed amplifiers, care should be taken with supply decoupling, lead dress and component placement.

When the feedback around the op amp is resistive (R_F), a pole will be created with R_F , the source resistance and capacitance (R_S , C_S), and the amplifier input capacitance ($C_{IN} \approx 4\text{pF}$). In low closed loop gain configurations and with R_S and R_F in the kilohm range, this pole can create excess phase shift and even oscillation. A small capacitor (C_F) in parallel with R_F eliminates this problem. With $R_S(C_S + C_{IN}) = R_F C_F$, the effect of the feedback pole is completely removed.



Settling Time Test Circuit

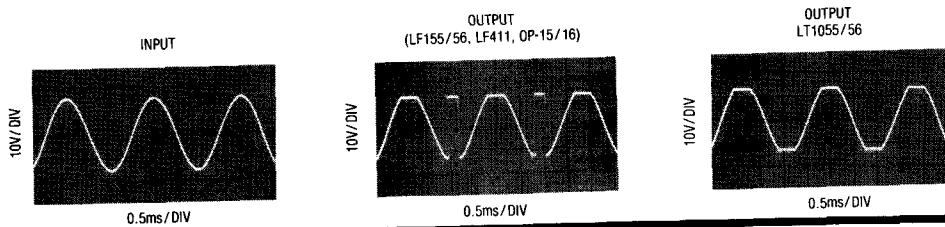
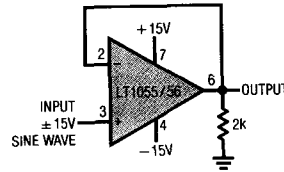


APPLICATIONS INFORMATION

Phase Reversal Protection

Most industry standard JFET input op amps (e.g., LF155/156, LF351, LF411, OP15/16) exhibit phase reversal at the output when the negative common-mode limit at the input is exceeded (i.e., from -12V to -15V with $\pm 15\text{V}$ supplies). This can cause lock-up in servo systems. As shown below, the LT1055/1056 does not have this problem due to unique phase reversal protection circuitry (Q1 on simplified schematic).

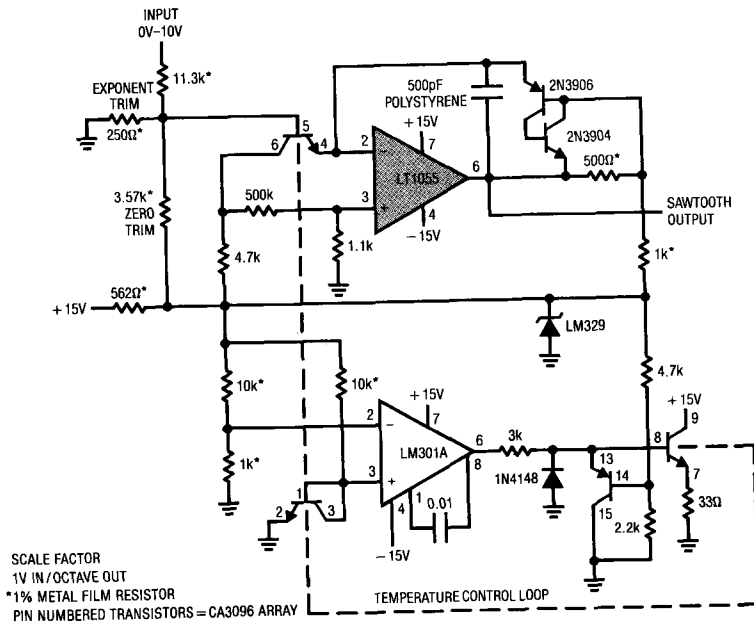
Voltage Follower with Input Exceeding the Negative Common-Mode Range



2

TYPICAL APPLICATIONS †

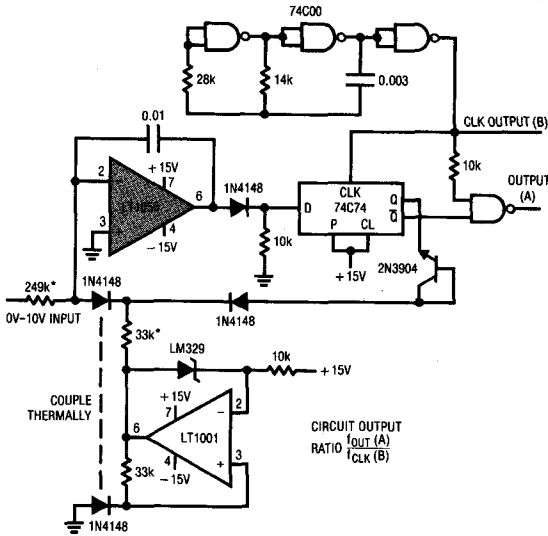
Exponential Voltage-to-Frequency Converter for Music Synthesizers



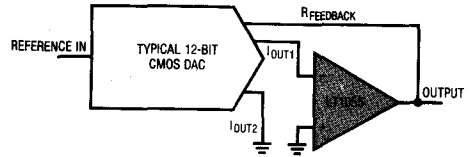
† For ten additional applications utilizing the LT1055 and LT1056, please see the LTC1043 data sheet and Application Note 3.

TYPICAL APPLICATIONS

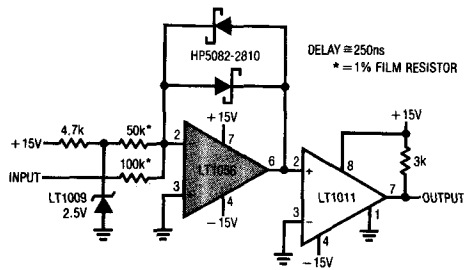
12-Bit Charge Balance Analog-to-Digital Converter



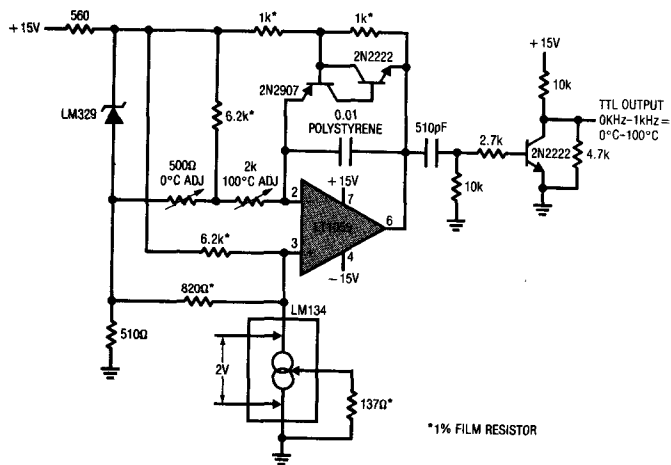
Fast "No Trims" 12-Bit Multiplying CMOS DAC Amplifier



Fast, 16-Bit Current Comparator



Temperature-to-Frequency Converter



TYPICAL APPLICATIONS

100kHz Voltage Controlled Oscillator

*1% FILM RESISTOR

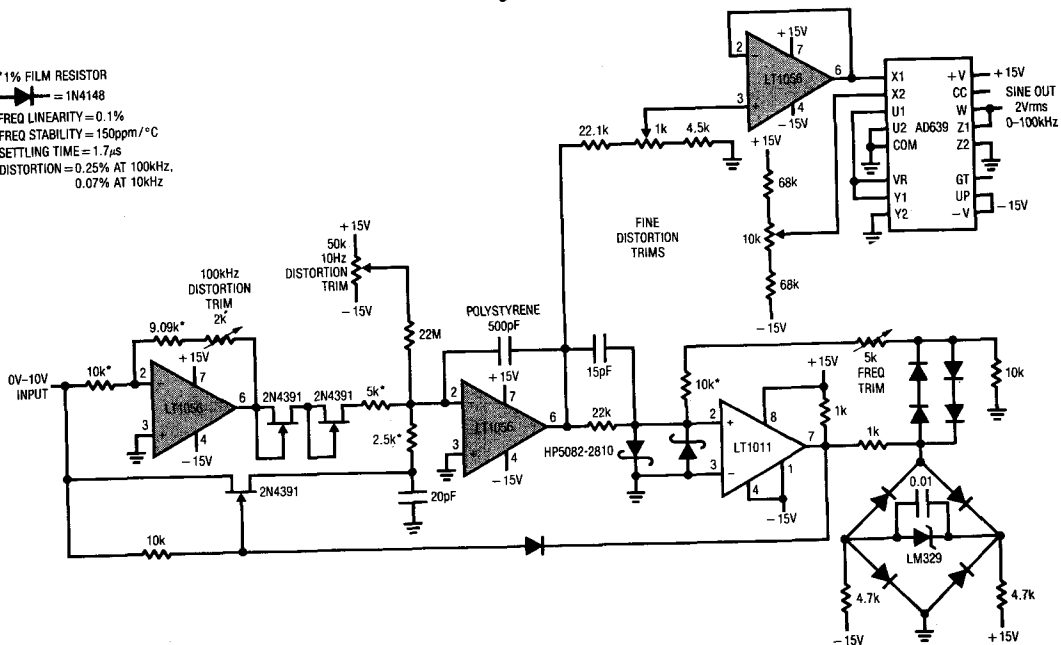
▶ = 1N4148

FREQ LINEARITY = 0.1%

FREQ STABILITY = 150ppm/°C

SETTLING TIME = 1.7μs

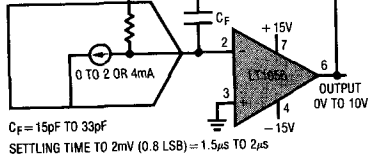
DISTORTION = 0.25% AT 100kHz,
0.07% AT 10kHz



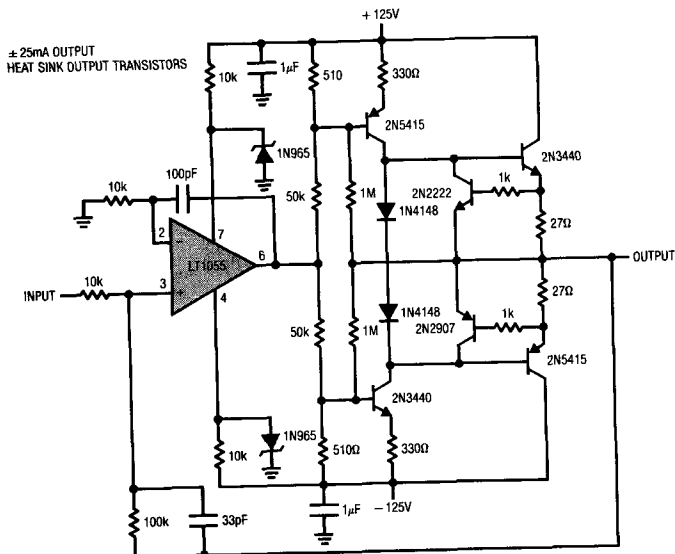
2

12-Bit Voltage Output D/A Converter

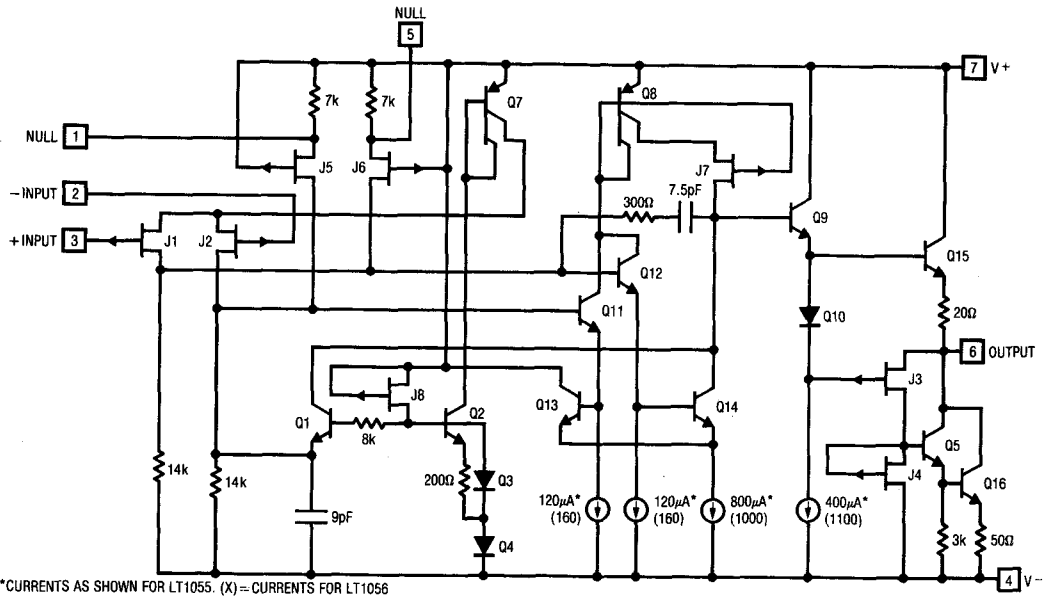
12-BIT CURRENT OUTPUT D/A CONVERTER (e.g., 6012, 565 OR DAC-80)



±120V Output Precision Op Amp

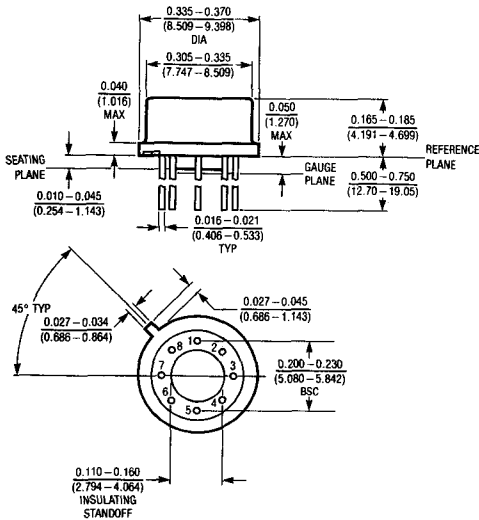


SIMPLIFIED SCHEMATIC



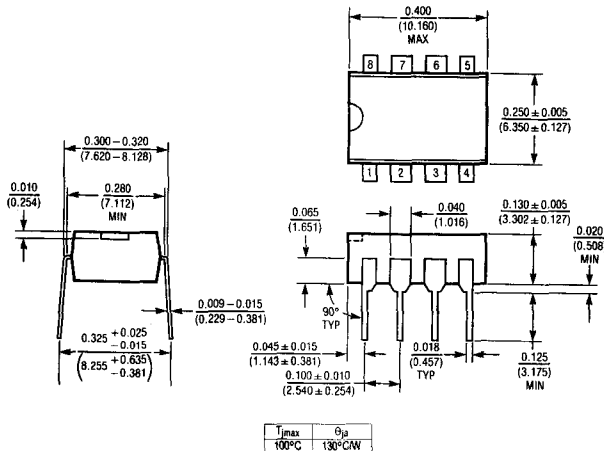
PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

H Package Metal Can



T_{jmax}	$\theta_{j\theta}$	θ_{jc}
150°C	150°C/W	45°C/W

**N8 Package
8 Lead Plastic**



FEATURES

- *Guaranteed* Offset Voltage
0°C to 70°C
- Low Drift
- *Guaranteed* Bias Current
70°C Warmed Up
- *Guaranteed* Slew Rate

DESCRIPTION

1.5mV Max.
 2.2mV Max.
 4 μ V/°C Typ.

400pA Max.
 9V/ μ s Min.

The LT1055/LT1056 JFET input operational amplifiers combine precision specifications with high speed performance.

For the first time in an SO package, 14V/ μ s slew rate and 5.5MHz gain-bandwidth product are simultaneously achieved with offset voltage of typically 0.5mV, 4 μ V/°C drift, and bias currents of 60pA at 70°C.

The 1.5mV maximum offset voltage specification is the best available on any JFET input operational amplifier in the plastic SO package.

The LT1055 and LT1056 are differentiated by their operating currents. The lower power dissipation LT1055 achieves lower bias and offset currents and offset voltage. The additional power dissipation of the LT1056 permits higher slew rate, bandwidth and faster settling time with a slight sacrifice in DC performance.

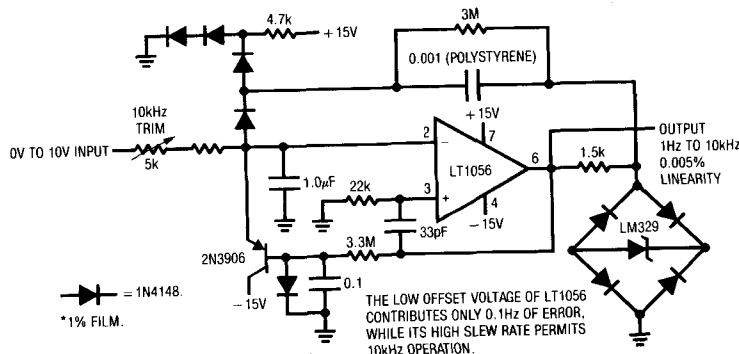
The voltage to frequency converter shown below is one of the many applications which utilize both the precision and high speed of the LT1055/LT1056.

APPLICATIONS

- Precision, High Speed Instrumentation
- Logarithmic Amplifiers
- D/A Output Amplifiers
- Photodiode Amplifiers
- Voltage to Frequency Converters
- Frequency to Voltage Converters
- Fast, Precision Sample and Hold

2

0 to 10kHz Voltage-to-Frequency Converter



LT1055S8/LT1056S8

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	$\pm 20V$
Differential Input Voltage	$\pm 40V$
Input Voltage	$\pm 20V$
Output Short Circuit Duration	Indefinite
Operating Temperature Range	$0^{\circ}C$ to $70^{\circ}C$
Storage Temperature Range	
All Devices	$-65^{\circ}C$ to $150^{\circ}C$
Lead Temperature (Soldering, 10 sec.)	$300^{\circ}C$

PACKAGE/ORDER INFORMATION

<p>TOP VIEW</p> <p>S8 PACKAGE PLASTIC SO</p>	ORDER PART NUMBER
	LT1055S8 LT1056S8
	PART MARKING
	1055 1056

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $T_A = 25^{\circ}C$, $V_{CM} = 0V$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1055S8 LT1056S8			UNITS
			MIN	TYP	MAX	
V_{OS}	Input Offset Voltage (Note 1)			500	1500	μV
I_{OS}	Input Offset Current	Fully Warm Up		5	30	pA
I_B	Input Bias Current	Fully Warm Up		± 30	± 100	pA
		$V_{CM} = +10V$		30	150	pA
	Input Resistance			0.4		Ω
	—Differential	$V_{CM} = -11V$ to $+8V$		0.4		Ω
	—Common-Mode	$V_{CM} = +8V$ to $+11V$		0.05		Ω
	Input Capacitance			4		pF
e_n	Input Noise Voltage	0.1Hz to 10Hz	LT1055	2.5		μV_p-p
			LT1056	3.5		μV_p-p
e_n	Input Noise Voltage Density	$f_o = 10Hz$ (Note 2)		35	70	nV/\sqrt{Hz}
		$f_o = 1kHz$ (Note 2)		15	22	nV/\sqrt{Hz}
i_n	Input Noise Current Density	$f_o = 10Hz, 1kHz$ (Note 3)		2.5	10	fA/\sqrt{Hz}
A_{VOL}	Large Signal Voltage Gain	$V_O = \pm 10V$		120	400	V/mV
		$R_L = 2k$		100	300	V/mV
		$R_L = 1k$		± 11	± 12	V
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm 11V$		83	98	dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 10V$ to $\pm 18V$		88	104	dB
V_{OUT}	Output Voltage Swing	$R_L = 2k$		± 12	± 13.2	V
SR	Slew Rate		LT1055	7.5	12	$V/\mu s$
			LT1056	9.0	14	$V/\mu s$
GBW	Gain-Bandwidth Product	$f = 1MHz$	LT1055	4.5		MHz
			LT1056	5.5		MHz
I_S	Supply Current		LT1055	2.8	4.0	mA
			LT1056	5.0	7.0	mA
	Offset Voltage Adjustment Range	$R_{POT} = 100k$		± 5		mV

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V, V_{CM} = 0V, 0^\circ C \leq T_A \leq 70^\circ C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1055S8/1056S8			UNITS
			MIN	TYP	MAX	
V_{OS}	Input Offset Voltage (Note 1)			800	2200	μV
	Average Temperature Coefficient of Input Offset Voltage			4	15	$\mu V/^\circ C$
I_{OS}	Input Offset Current	Warmed Up $T_A = 70^\circ C$		18	150	pA
I_B	Input Bias Current	Warmed Up $T_A = 70^\circ C$		± 60	± 400	pA
A_{VOL}	Large Signal Voltage Gain	$V_O = \pm 10V, R_L = 2k$		60	250	V/mV
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm 10.5V$		82	98	dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 10V$ to $\pm 18V$		87	103	dB
V_{OUT}	Output Voltage Swing	$R_L = 2k$		± 12	± 13.1	V

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: Offset voltage is measured under two different conditions:

(a) approximately 0.5 seconds after application of power; (b) at $T_A = 25^\circ C$ only, with the chip heated to approximately $38^\circ C$ for the LT1055 and to $45^\circ C$ for the LT1056, to account for chip temperature rise when the device is fully warmed up.

Note 2: This parameter is tested on a sample basis only.

Note 3: Current noise is calculated from the formula: $i_n = (2qI_B)^{1/2}$, where $q = 1.6 \times 10^{-19}$ coulomb. The noise of source resistors up to $1G\Omega$ swamps the contribution of current noise.

Note 4: Offset voltage drift with temperature is practically unchanged when the offset voltage is trimmed to zero with a $100k$ potentiometer between the balance terminals and the wiper tied to V^+ .

2

NOTES

Dual and Quad, JFET Input Precision High Speed Op Amps

FEATURES

- 14V/μs Slew Rate
- 5MHz Gain-Bandwidth Product
- Fast Settling Time
- 150μV Offset Voltage (LT1057)
- 180μV Offset Voltage (LT1058)
- 2μV/°C V_{OS} Drift
- 50pA Bias Current at 70°C
- Low Voltage Noise

10V/μs Min.

1.3μs to 0.02%

450μV Max.

600μV Max.

7μV/°C Max.

13nV/√Hz @ 1kHz

26nV/√Hz @ 10Hz

APPLICATIONS

- Precision, High Speed Instrumentation
- Fast, Precision Sample and Hold
- Logarithmic Amplifiers
- D/A Output Amplifiers
- Photodiode Amplifiers
- Voltage to Frequency Converters
- Frequency to Voltage Converters

DESCRIPTION

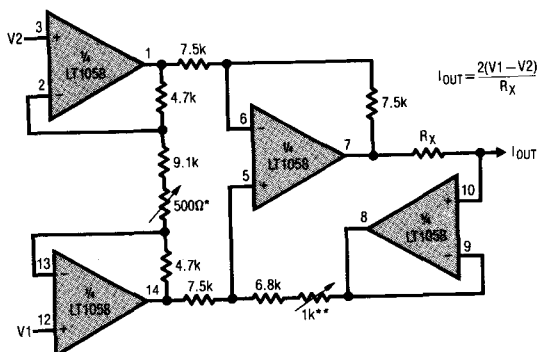
The LT1057 is a matched JFET input dual op amp in the industry standard 8 pin configuration, featuring a combination of outstanding high speed and precision specifications. It replaces all the popular bipolar and JFET input dual op amps. In particular, the LT1057 upgrades the performance of systems using the LF412A and OP-215 JFET input duals.

The LT1058 is the lowest offset quad JFET input operational amplifier in the standard 14 pin configuration. It offers significant accuracy improvement over presently available JFET input quad operational amplifiers. It can replace four single precision JFET input op amps, while saving board space, power dissipation and cost.

Both the LT1057 and LT1058 are available in all standard packages: plastic and hermetic DIP and (LT1057 only) metal can.

2

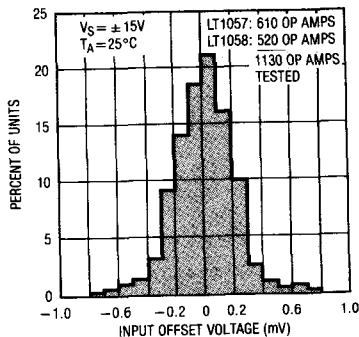
Current Output, High Speed, High Input Impedance Instrumentation Amplifier



*GAIN ADJUST

 **COMMON-MODE REJECTION ADJUST
 BANDWIDTH ≈ 2MHz

Distribution of Offset Voltage (All Packages, LT1057 and LT1058)



ABSOLUTE MAXIMUM RATINGS

Supply Voltage $\pm 20V$
 Differential Input Voltage $\pm 40V$
 Input Voltage $\pm 20V$
 Output Short Circuit Duration Indefinite
 Operating Temperature Range
 LT1057AM/LT1057M/
 LT1058AM/LT1058M $-55^{\circ}C$ to $125^{\circ}C$
 LT1057AC/LT1057C/
 LT1058AC/LT1058C $0^{\circ}C$ to $70^{\circ}C$
 Storage Temperature Range
 All Devices $-65^{\circ}C$ to $150^{\circ}C$
 Lead Temperature (Soldering, 10 sec.) $300^{\circ}C$

PACKAGE/ORDER INFORMATION

	ORDER PART NO.
<p>METAL CAN H PACKAGE</p>	LT1057AMH LT1057MH LT1057ACH LT1057CH
<p>HERMETIC DIP J8 PACKAGE PLASTIC DIP N8 PACKAGE</p>	LT1057AMJ8 LT1057MJ8 LT1057ACJ8 LT1057CJ8 LT1057ACN8 LT1057CN8
<p>HERMETIC DIP J14 PACKAGE PLASTIC DIP N14 PACKAGE</p>	LT1058AMJ LT1058MJ LT1058ACJ LT1058CJ LT1058ACN LT1058CN

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V, T_A = 25^{\circ}C, V_{CM} = 0V$ unless otherwise noted. (Note 1)

SYMBOL	PARAMETER	CONDITIONS	LT1057AM/LT1058AM LT1057AC/LT1058AC			LT1057M/LT1058M LT1057C/LT1058C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	LT1057 LT1058	150	450	200	800		μV	
			180	600	250	1000		μV	
I_{OS}	Input Offset Current	Fully Warmd Up	3	40	4	50		pA	
I_b	Input Bias Current	Fully Warmd Up	± 5	± 50	± 7	± 75		pA	
	Input Resistance-Differential			10^{12}		10^{12}		Ω	
	-Common-Mode	$V_{CM} = -11V$ to $8V$ $V_{CM} = 8V$ to $11V$		10^{12}		10^{12}		Ω	
				10^{11}		10^{11}		Ω	
	Input Capacitance		4		4			pF	
e_n	Input Noise Voltage	0.1Hz to 10Hz LT1057 LT1058	2.0		2.1			μV_p-p	
			2.4		2.5			μV_p-p	
e_n	Input Noise Voltage Density	$f_0 = 10Hz$ $f_0 = 1kHz$ (Note 2)	26		28			nV/ \sqrt{Hz}	
			13	22	14	24		nV/ \sqrt{Hz}	
i_n	Input Noise Current Density	$f_0 = 10Hz, 1kHz$ (Note 3)	1.5	4	1.8	6		fA/ \sqrt{Hz}	
A_{VOL}	Large Signal Voltage Gain	$V_O = \pm 10V, R_L = 2k$ $V_O = \pm 10V, R_L = 1k$	150	350	100	300		V/mV	
			120	250	80	220		V/mV	
	Input Voltage Range		± 10.5	14.3	± 10.5	14.3		V	
				-11.5		-11.5			
CMRR	Common-Mode Rejection Ratio	LT1057 LT1058	86	100	82	98		dB	
			84	98	80	96		dB	
PSRR	Power Supply Rejection Ratio	$V_S = \pm 10V$ to $\pm 18V$	88	103	86	102		dB	
V_{OUT}	Output Voltage Swing	$R_L = 2k$	± 12	± 13	± 12	± 13		V	

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V, T_A = 25^\circ C, V_{CM} = 0V$ unless otherwise noted. (Note 1)

SYMBOL	PARAMETER	CONDITIONS	LT1057AM/LT1058AM LT1057AC/LT1058AC			LT1057M/LT1058M LT1057C/LT1058C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew Rate		10	14		8	13		V/ μ s
GBW	Gain-Bandwidth Product	$f = 1MHz$ (Note 5)	3.5	5		3	5		MHz
I_S	Supply Current Per Amplifier			1.6	2.5		1.7	2.8	mA
	Channel Separation	DC to 5kHz, $V_{IN} = \pm 10V$		132			130		dB

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V, V_{CM} = 0V, 0^\circ C \leq T_A \leq 70^\circ C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1057AC LT1058AC			LT1057C LT1058C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	LT1057	•	250	800	330	1400		μ V
		LT1058	•	300	1200	400	1800		μ V
	Average Temperature Coefficient of Input Offset Voltage	LT1057 H/J8 Package	•	1.8	7	2.3	12		μ V/ $^\circ$ C
		N8 Package	•	3	10	4	16		μ V/ $^\circ$ C
		LT1058 J Package (Note 4)	•	2.5	10	3	15		μ V/ $^\circ$ C
		N Package (Note 4)	•	4	15	5	22		μ V/ $^\circ$ C
I_{OS}	Input Offset Current	Warmed Up, $T_A = 70^\circ C$		18	150	20	250		pA
I_B	Input Bias Current	Warmed Up, $T_A = 70^\circ C$		± 50	± 250	± 60	± 350		pA
A_{VOL}	Large Signal Voltage Gain	$V_O = \pm 10V, R_L = 2k$	•	70	220	50	200		V/mV
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm 10.4V$	•	85	98	80	96		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 10V$ to $\pm 18V$	•	87	102	84	100		dB
V_{OUT}	Output Voltage Swing	$R_L = 2k$	•	± 12	± 12.8	± 12	± 12.8		V
I_S	Supply Current Per Amplifier	$T_A = 70^\circ C$			2.8		3.2		mA
					1.4		1.5		mA

2

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V, V_{CM} = 0V, -55^\circ C \leq T_A \leq 125^\circ C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1057AM LT1058AM			LT1057M LT1058M			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	LT1057	•	300	1100	400	2000		μ V
		LT1058	•	380	1600	550	2500		μ V
	Average Temperature Coefficient of Input Offset Voltage	LT1057	•	2.0	7	2.5	12		μ V/ $^\circ$ C
		LT1058 (Note 4)	•	2.5	10	3	15		μ V/ $^\circ$ C
I_{OS}	Input Offset Current	Warmed Up, $T_A = 125^\circ C$		0.15	2	0.2	3		nA
I_B	Input Bias Current	Warmed Up, $T_A = 125^\circ C$		± 0.6	± 4.5	± 0.7	± 6		nA
A_{VOL}	Large Signal Voltage Gain	$V_O = \pm 10V, R_L = 2k$	•	40	120	30	110		V/mV
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm 10.4V$	•	84	97	80	95		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 10V$ to $\pm 17V$	•	86	100	83	98		dB
V_{OUT}	Output Voltage Swing	$R_L = 2k$	•	± 12	± 12.7	± 12	± 12.6		V
I_S	Supply Current Per Amplifier	$T_A = 125^\circ C$		1.25	1.9	1.3	2.2		mA

The • denotes the specifications which apply over the full operating temperature range.

Note 1: Typical parameters are defined as the 60% yield of distributions of individual amplifiers; i.e., out of 100 LT1058s or (100 LT1057s), typically 240 op amps (or 120 for the LT1057) will be better than the indicated specification.

Note 2: This parameter is tested on a sample basis only.

Note 3: Current noise is calculated from the formula:

$$i_n = (2qI_b)^{1/2}$$

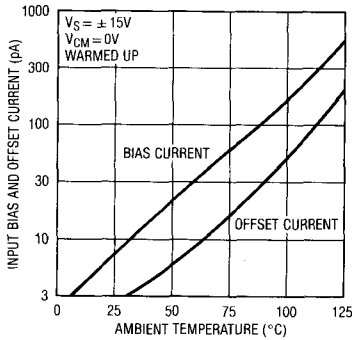
where $q = 1.6 \times 10^{-19}$ coulomb. The noise of source resistors up to 1G Ω swamps the contribution of current noise.

Note 4: This parameter is not 100% tested.

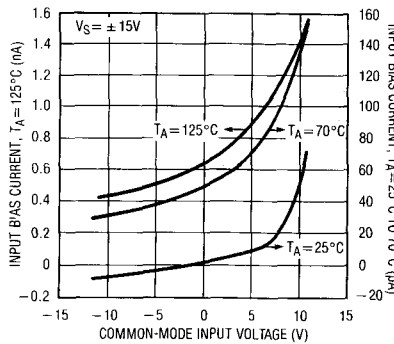
Note 5: Gain-bandwidth product is not tested. It is guaranteed by design and by inference from the slew rate measurement.

TYPICAL PERFORMANCE CHARACTERISTICS

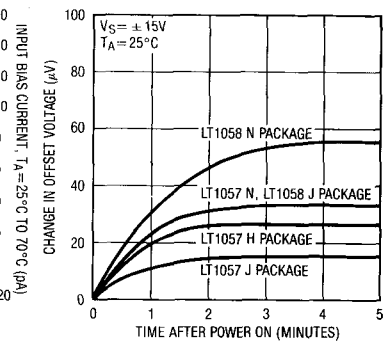
Input Bias and Offset Currents vs Temperature



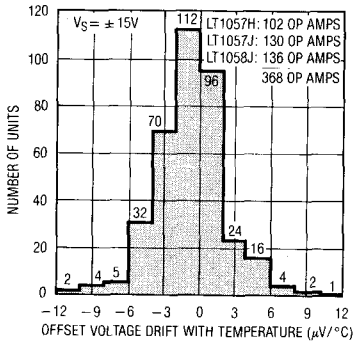
Input Bias Current Over the Common-Mode Range



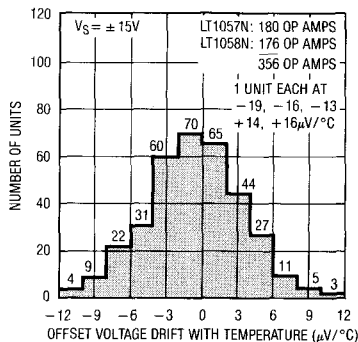
Warm-Up Drift



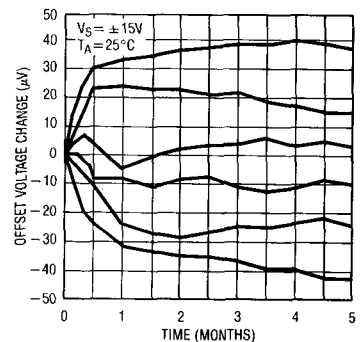
Distribution of Offset Voltage Drift with Temperature (H and J Package)



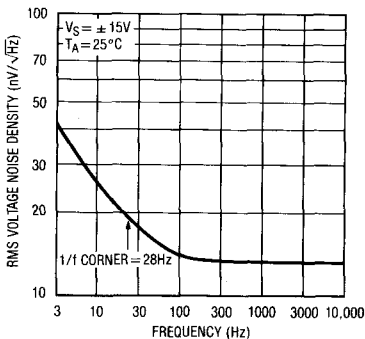
Distribution of Offset Voltage Drift with Temperature (Plastic N Package)



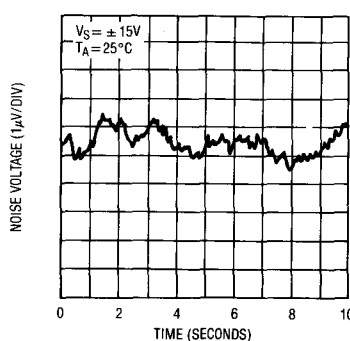
Long Term Drift of Representative Units



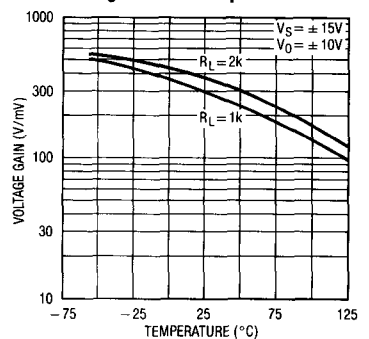
Voltage Noise vs Frequency



0.1Hz to 10Hz Noise

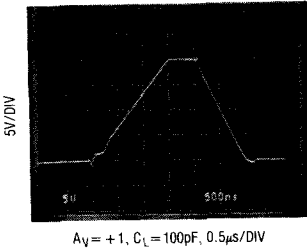


Voltage Gain vs Temperature

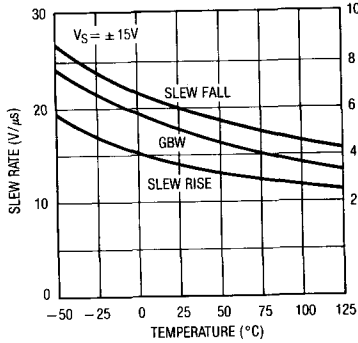


TYPICAL PERFORMANCE CHARACTERISTICS

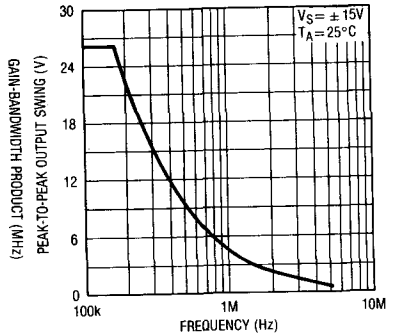
Large Signal Response



Slew Rate, Gain-Bandwidth Product vs Temperature

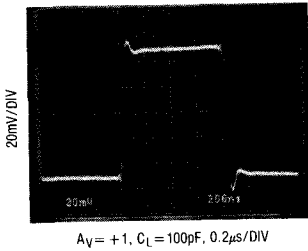


Undistorted Output Swing vs Frequency

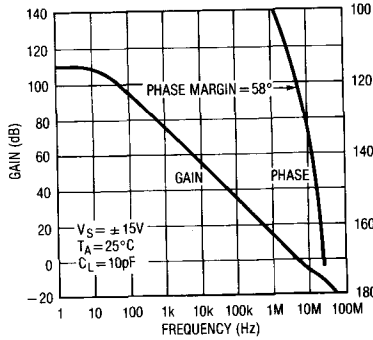


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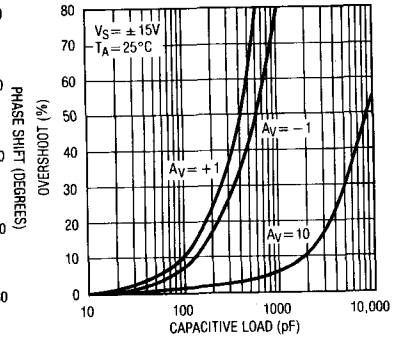
Small Signal Response



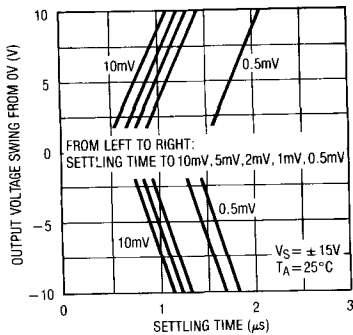
Gain, Phase Shift vs Frequency



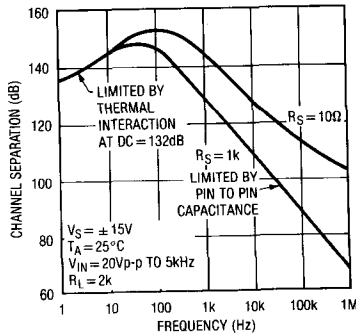
Capacitive Load Handling



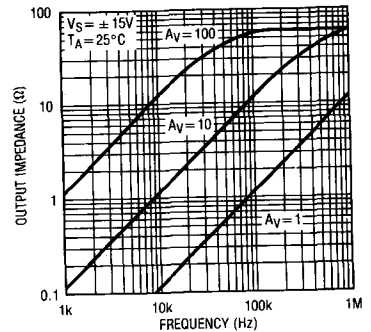
Settling Time



Channel Separation vs Frequency

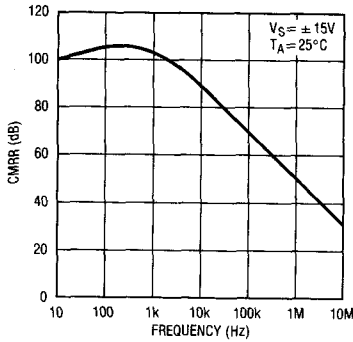


Output Impedance vs Frequency

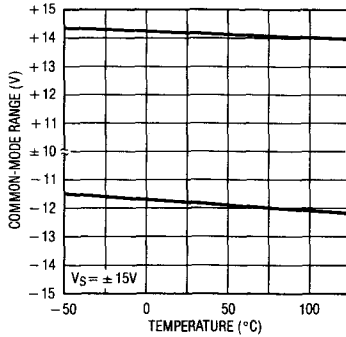


TYPICAL PERFORMANCE CHARACTERISTICS

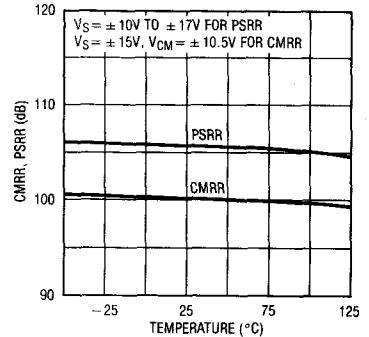
Common-Mode Rejection Ratio vs Frequency



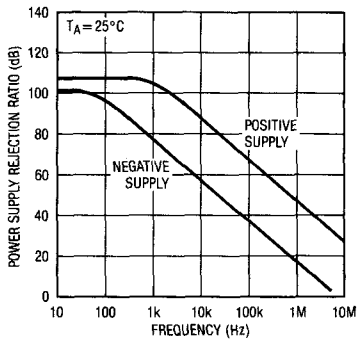
Common-Mode Range vs Temperature



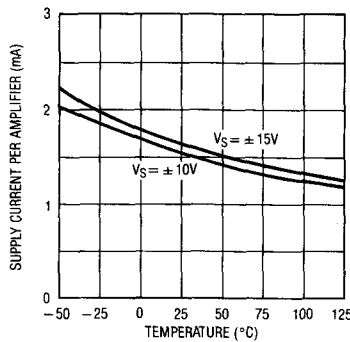
Common-Mode and Power Supply Rejections vs Temperature



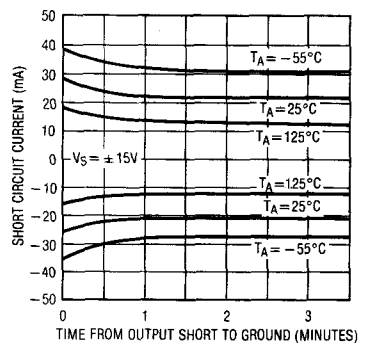
Power Supply Rejection Ratio vs Frequency



Supply Current vs Temperature



Short Circuit Current vs Time (One Output Shorted to Ground)



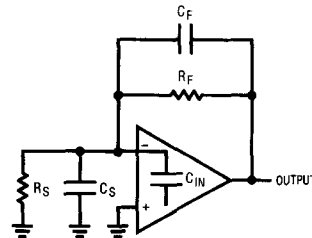
APPLICATIONS INFORMATION

The LT1057 may be inserted directly into LF353, LF412, LF442, TL072, TL082 and OP-215 sockets. The LT1058 plugs into LF347, LF444, TL074, TL084 sockets. Of course, all standard dual and quad bipolar op amps can also be replaced by these devices.

High Speed Operation

When the feedback around the op amp is resistive (R_F), a pole will be created with R_F , the source resistance and capacitance (R_S, C_S), and the amplifier input capacitance ($C_{IN} \approx 4\text{pF}$). In low closed loop gain configurations and with R_S and R_F in the kilohm range, this pole can create excess phase shift and even oscillation. A small capacitor

(C_F) in parallel with R_F eliminates this problem. With $R_S(C_S + C_{IN}) = R_F C_F$, the effect of the feedback pole is completely removed.



APPLICATIONS INFORMATION

Settling time is measured in a test circuit which can be found in the LT1055/LT1056 data sheet and in Application Note 10.

Achieving Picoampere/Microvolt Performance

In order to realize the picoampere/microvolt level accuracy of the LT1057/LT1058, proper care must be exercised. For example, leakage currents in circuitry external to the op amp can significantly degrade performance. High quality insulation should be used (e.g., Teflon™, Kel-F); cleaning of all insulating surfaces to remove fluxes and other residues will probably be required. Surface coating may be necessary to provide a moisture barrier in high humidity environments.

Board leakage can be minimized by encircling the input circuitry with a guard ring operated at a potential close to that of the inputs; in inverting configurations the guard ring should be tied to ground, in non-inverting connections to the inverting input. Guarding both sides of the printed circuit board is required. Bulk leakage reduction depends on the guard ring width.

The LT1057/LT1058 have the lowest offset voltage of any dual and quad JFET input op amps available today. However, the offset voltage and its drift with time and temperature are still not as good as on the best bipolar amplifiers because the transconductance of FETs is considerably lower than that of bipolar transistors. Conversely, this lower transconductance is the main cause of the significantly faster speed performance of FET input op amps.

Teflon™ is a trademark of DuPont.

Offset voltage also changes somewhat with temperature cycling. The AM grades show a typical 40μV hysteresis (50μV on the M grades) when cycled over the -55°C to 125°C temperature range. Temperature cycling from 0°C to 70°C has a negligible (less than 20μV) hysteresis effect.

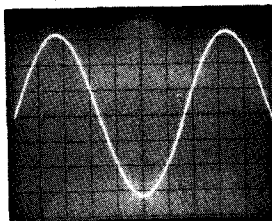
The offset voltage and drift performance are also affected by packaging. In the plastic N package the molding compound is in direct contact with the chip, exerting pressure on the surface. While NPN input transistors are largely unaffected by this pressure, JFET device drift is degraded. Consequently, for best drift performance, as shown in the typical performance distribution plots, the J or H packages are recommended.

In applications where speed and picoampere bias currents are not necessary, Linear Technology offers the bipolar input, pin compatible LT1013 and LT1014 dual and quad op amps. These devices have significantly better DC specifications than any JFET input device.

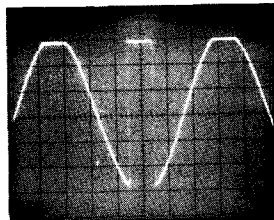
Phase Reversal Protection

Most industry standard JFET input single, dual and quad op amps (e.g., LF156, LF351, LF353, LF411, LF412, OP-15, OP-16, OP-215, TL084) exhibit phase reversal at the output when the negative common-mode limit at the input is exceeded (i.e., below -12V with ±15V supplies). The photos show a ±16V sine wave input (A), the response of an LF412A in the unity gain follower mode (B), and the response of the LT1057/LT1058 (C).

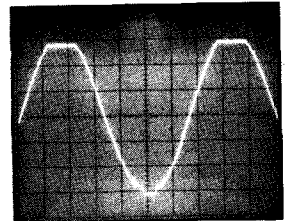
The phase reversal of photo (B) can cause lock-up in servo systems. The LT1057/LT1058 does not phase-reverse due to a unique phase reversal protection circuit.



(A) ±16V Sine Wave Input



(B) LF412A Output

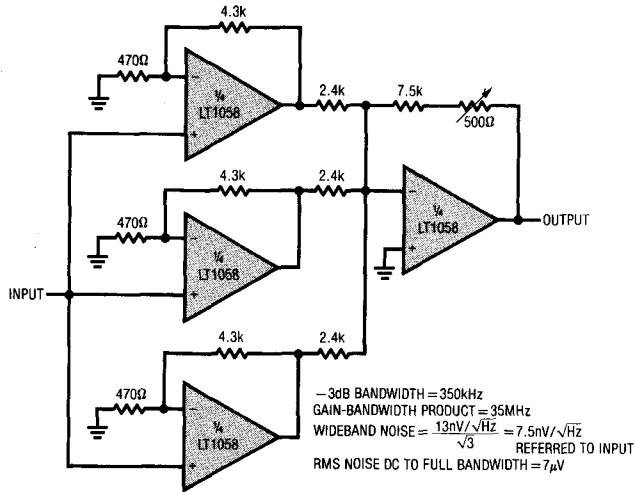


(C) LT1057/LT1058 Output

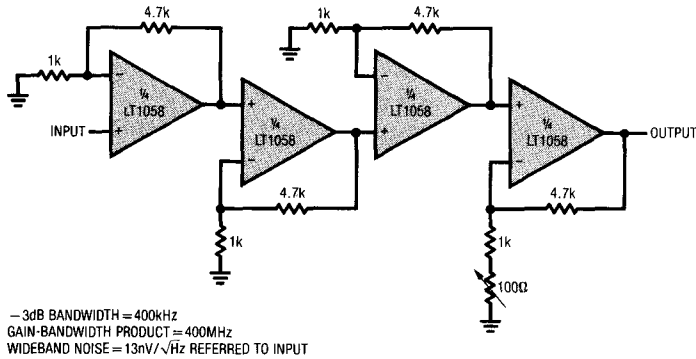
All Photos 5V/Div Vertical Scale, 50μs/Div Horizontal Scale

APPLICATIONS

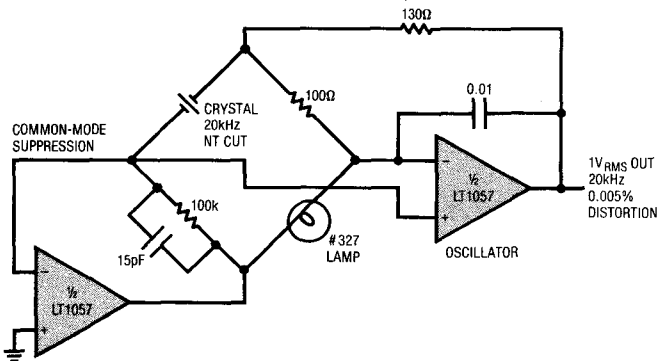
Low Noise, Wideband, Gain = 100 Amplifier with High Input Impedance



Wideband, High Input Impedance, Gain = 1000 Amplifier

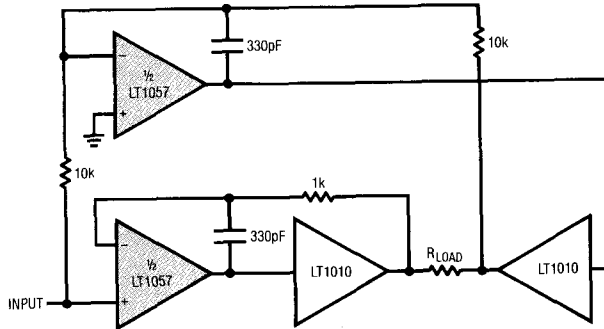


Low Distortion, Crystal Stabilized Oscillator



APPLICATIONS

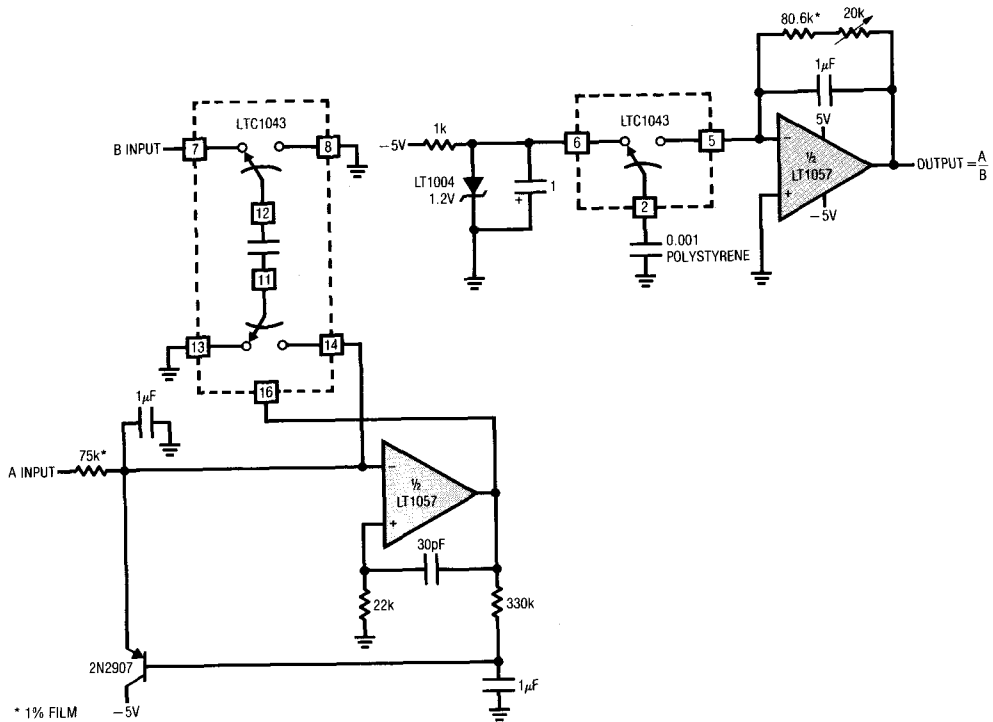
Fast, Precision Bridge Amplifier



SLEW RATE = 14V/μs
 OUTPUT CURRENT TO LOAD = 150mA
 LOAD CAPACITANCE: UP TO 1μF

2

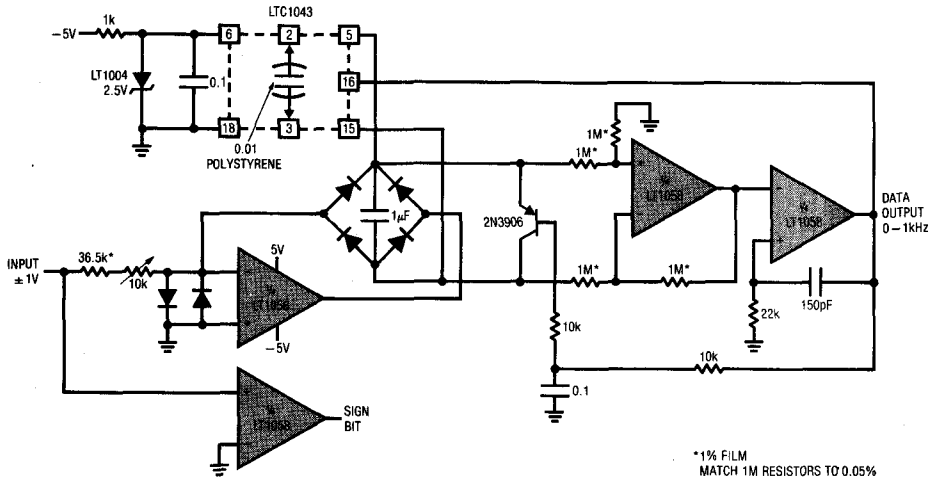
Analog Divider



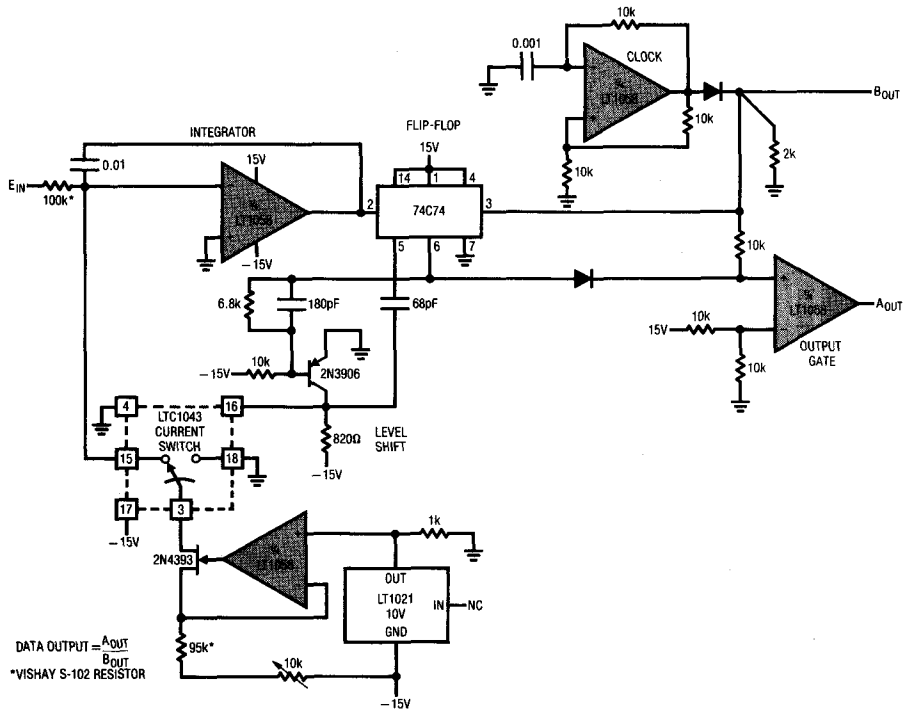
* 1% FILM

APPLICATIONS

Bipolar Input (AC) V-F Converter

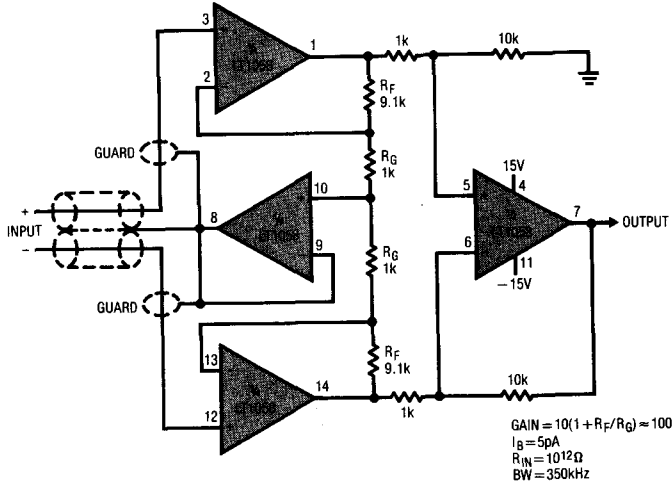


12 Bit A-D Converter



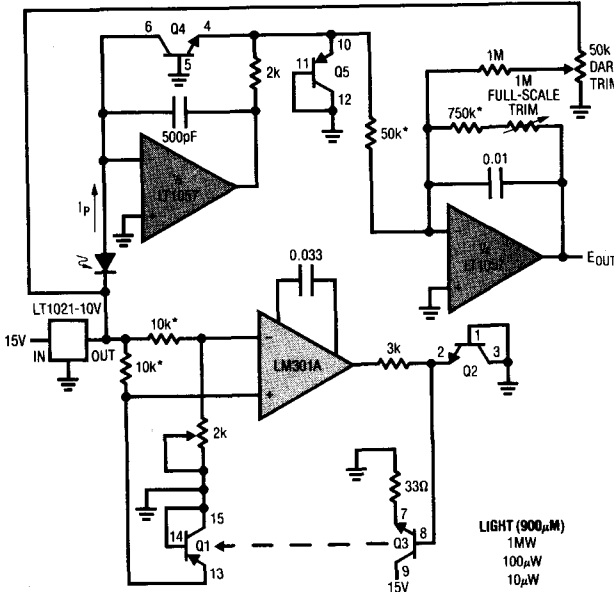
APPLICATIONS

Instrumentation Amplifier with Shield Driver



2

100dB Range Logarithmic Photodiode Amplifier

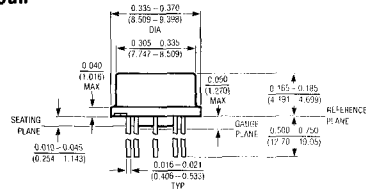
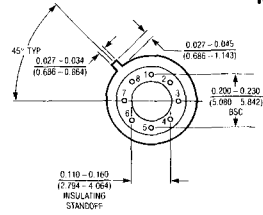


LIGHT (900nm)	DIODE CURRENT	CIRCUIT OUTPUT
1mW	350μA	10.0V
100μW	35μA	7.85V
10μW	3.5μA	5.70V
1μW	350nA	3.55V
100nW	35nA	1.40V
10nW	3.5nA	-0.75V

= HP-5082-4204 PIN PHOTODIODE.
 Q1-Q5 = CA3096.
 CONNECT SUBSTRATE OF CA3096
 ARRAY TO Q4'S EMITTER.
 *1% RESISTOR
100dB RANGE LOGARITHMIC PHOTODIODE AMPLIFIER

PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

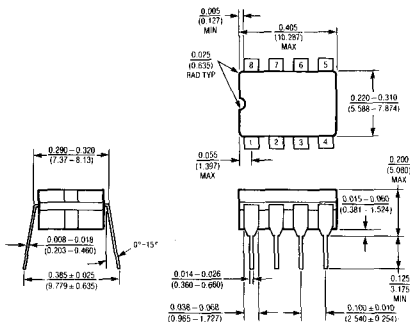
**H Package
Metal Can**



NOTE: LEAD DIAMETER IS UNCONTROLLED BETWEEN THE REFERENCE PLANE AND SEATING PLANE.

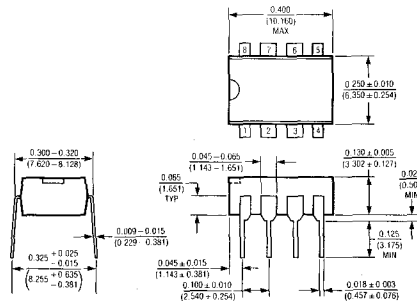
T_{jmax}	θ_{ja}	θ_{jc}
150°C	150°C/W	45°C/W

**J8 Package
8 Lead Hermetic Dip**



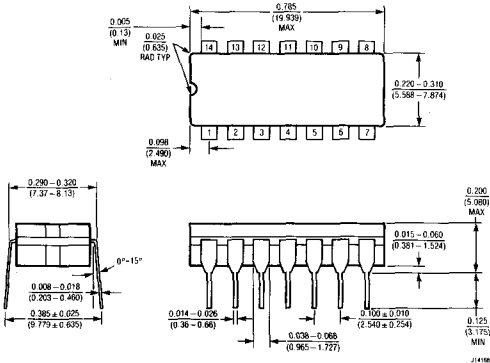
T_{jmax}	θ_{ja}
150°C	100°C/W

**N8 Package
8 Lead Plastic**



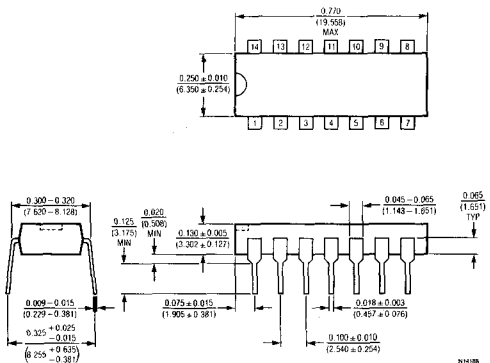
T_{jmax}	θ_{ja}
100°C	130°C/W

**J Package
14-Lead Hermetic DIP**



T_{jmax}	θ_{ja}
150°C	100°C/W

**N Package
14-Lead Plastic**



T_{jmax}	θ_{ja}
110°C	130°C/W

FEATURES

- 13V/μs Slew Rate
- 5MHz Gain-Bandwidth Product
- Fast Settling Time
- 300μV Offset Voltage (LT1057)
- 5μV/°C V_{OS} Drift
- 60pA Bias Current at 70°C
- Low Voltage Noise

8V/μs Min.

1.3μs to 0.02%

 13nV/√Hz @ 1kHz
 26nV/√Hz @ 10Hz

DESCRIPTION

The LT1057 is a matched JFET input dual op amp in the industry standard 8 pin configuration, featuring a combination of outstanding high speed and precision specifications. It replaces all the popular bipolar and JFET input dual op amps. In particular, the LT1057 upgrades the performance of systems using the LF412A and OP-215 JFET input duals.

For the first time, precision dual JFET op amps are available in a surface mounted package for extended operating temperatures (-40°C to +85°C), the LT1057IS is offered.

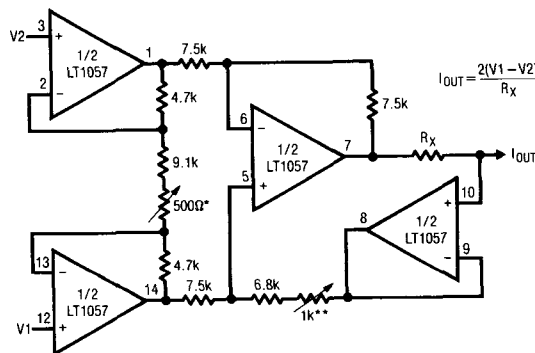
APPLICATIONS

- Precision, High Speed Instrumentation
- Fast, Precision Sample and Hold
- Logarithmic Amplifiers
- D/A Output Amplifiers
- Photodiode Amplifiers
- Voltage to Frequency Converters
- Frequency to Voltage Converters

REFER TO TABLE OF CONTENTS
FOR REVISED DATA LOCATION

2

Current Output, High Speed, High Input Impedance Instrumentation Amplifier



*GAIN ADJUST
 **COMMON-MODE REJECTION ADJUST
 BANDWIDTH ≈ 2MHz

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	± 20V
Differential Input Voltage	± 40V
Input Voltage	± 20V
Output Short Circuit Duration	Indefinite
Operating Temperature Range	
LT1057S	0°C to 70°C
LT1057IS	- 40°C to 85°C
Storage Temperature Range	
All Devices	- 65°C to 150°C
Lead Temperature (Soldering, 10 sec.)	300°C

PACKAGE/ORDER INFORMATION

	ORDER PART NUMBER
	LT1057S LT1057IS
	PART MARKING
	LT1057S LT1057IS

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V, T_A = 25^\circ C, V_{CM} = 0V$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage			0.3	2	mV
I_{OS}	Input Offset Current	Fully Warmd Up		5	50	pA
I_B	Input Bias Current	Fully Warmd Up		± 10	± 100	pA
	Input Resistance —Differential			0.4		TΩ
	—Common-Mode	$V_{CM} = -11V$ to $+8V$ $V_{CM} = +8V$ to $+11V$		0.4		TΩ
	Input Capacitance			4		pF
e_n	Input Noise Voltage	0.1Hz to 10Hz		2.1		μVp-p
e_n	Input Noise Voltage Density	$f_0 = 10Hz$ $f_0 = 1kHz$		26		nV/√Hz
				13		nV/√Hz
i_n	Input Noise Current Density	$f_0 = 10Hz, 1kHz$		1.8		fA/√Hz
A_{VOL}	Large Signal Voltage Gain	$V_O = \pm 10V$		100	300	V/mV
		$R_L = 2k$ $R_L = 1k$		50	220	V/mV
	Input Voltage Range		± 10.5	14.3	- 11.5	V
						V
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm 10.5V$	82	98		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 10V$ to $\pm 18V$	86	102		dB
V_{OUT}	Output Voltage Swing	$R_L = 2k$	± 12	± 13		V
SR	Slew Rate		8	13		V/μs
GBW	Gain-Bandwidth Product	$f = 1MHz$ (Note 1)	3	5		MHz
I_S	Supply Current Per Amplifier			1.7	2.8	mA
	Channel Separation	DC to 5kHz, $V_{IN} = \pm 10V$		130		dB

ELECTRICAL CHARACTERISTICS

$V_S = \pm 15V$, $V_{CM} = 0V$, $0^\circ C \leq T_A \leq 70^\circ C$ (LT1057S) or $-40^\circ C \leq T_A \leq 85^\circ C$ (LT1057IS), unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage		•		0.5	2.5	mV
	Average Temperature Coefficient of Input Offset Voltage		•		5		$\mu V/^\circ C$
I_{OS}	Input Offset Current	Warmed Up, $T_A = 70^\circ C$ (LT1057S)			20	250	pA
		Warmed Up, $T_A = 85^\circ C$ (LT1057IS)			35	400	pA
I_B	Input Bias Current	Warmed Up, $T_A = 70^\circ C$ (LT1057S)			± 60	± 400	pA
		Warmed Up, $T_A = 85^\circ C$ (LT1057IS)			± 100	± 700	pA
A_{VOL}	Large Signal Voltage Gain	$V_O = \pm 10V$, $R_L = 2k$	•	50	200		V/mV
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm 10.5V$	•	80	96		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 10V$ to $\pm 18V$	•	84	100		dB
V_{OUT}	Output Voltage Swing	$R_L = 2k$	•	± 12	± 12.8		V

The • denotes the specifications which apply over the full operating temperature range.

Note 1: Gain bandwidth product is not tested. It is guaranteed by design and by inference from the slew rate measurement.

2

NOTES

Micropower, Dual and Quad, Single Supply, Precision Op Amps

FEATURES

- 50 μ A Max Supply Current per Amplifier
- 70 μ V Max Offset Voltage
- 250pA Max Offset Current
- 0.6 μ Vp-p 0.1Hz to 10Hz Voltage Noise
- 3pAp-p 0.1Hz to 10Hz Current Noise
- 0.4 μ V/ $^{\circ}$ C Offset Voltage Drift
- 200kHz Gain-Bandwidth-Product
- 0.07V/ μ s Slew Rate
- Single Supply Operation
 - Input Voltage Range Includes Ground
 - Output Swings to Ground while Sinking Current
 - No Pull Down Resistors are Needed
- Output Sources and Sinks 5mA Load Current

APPLICATIONS

- Battery or Solar Powered Systems
 - Portable Instrumentation
 - Remote Sensor Amplifier
 - Satellite Power Supply
- Micropower Sample and Hold
- Thermocouple Amplifier
- Micropower Filters

DESCRIPTION

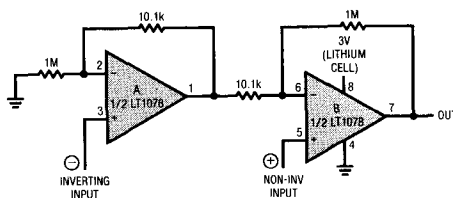
The LT1078 is a micropower dual op amp in the standard 8-pin configuration; the LT1079 is a micropower quad op amp offered in the standard 14-pin packages. Both devices are optimized for single supply operation at 5V. \pm 15V specifications are also provided.

Micropower performance of competing devices is achieved at the expense of seriously degrading precision, noise, speed, and output drive specifications. The design effort of the LT1078/1079 was concentrated on reducing supply current without sacrificing other parameters. The offset voltage achieved is the lowest on any dual or quad non-chopper stabilized op amp—micropower or otherwise. Offset current, voltage and current noise, slew rate and gain-bandwidth-product are all two to ten times better than on previous micropower op amps.

The 3dB corner of the voltage noise spectrum is at 0.7Hz, at least three times lower than on any monolithic op amp. This results in low frequency (0.1Hz to 10Hz) noise performance which can only be found on devices with an order of magnitude higher supply current.

Both the LT1078 and LT1079 can be operated from a single supply (as low as one lithium cell or two Ni-cad batteries). The input range goes below ground. The all-NPN output stage swings to within a few millivolts of ground while sinking current—no power consuming pull down resistors are needed.

**Single Battery, Micropower, Gain = 100,
Instrumentation Amplifier**

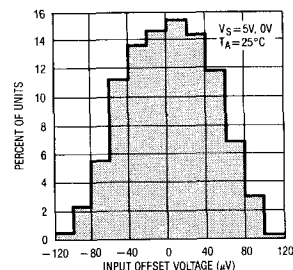


TYPICAL PERFORMANCE

INPUT OFFSET VOLTAGE = 40 μ V
 INPUT OFFSET CURRENT = 0.2nA
 TOTAL POWER DISSIPATION = 240 μ W
 COMMON-MODE REJECTION = 110dB (AMPLIFIER LIMITED)
 GAIN BANDWIDTH PRODUCT = 200KHZ

OUTPUT NOISE = 85 μ Vp-p 0.1Hz TO 10Hz
 = 300 μ A RMS OVER FULL BANDWIDTH
 INPUT RANGE = 0.03V TO 3.8V
 OUTPUT RANGE = 0.03V TO 2.3V (0.3mA \leq V_{IN+} - V_{IN-} \leq 23mV)
 OUTPUTS SINK CURRENT—NO PULL DOWN RESISTORS ARE NEEDED

**Distribution of Input Offset Voltage
(LT1078 and LT1079 in All Packages)**



ABSOLUTE MAXIMUM RATINGS

Supply Voltage ± 22V
 Differential Input Voltage ± 30V
 Input Voltage Equal to Positive Supply Voltage
 5V Below Negative Supply Voltage
 Output Short Circuit Duration Indefinite
 Operating Temperature Range
 LT1078AM/LT1078M/
 LT1079AM/LT1079M - 55°C to 125°C
 LT1078AC/LT1078C/
 LT1079AC/LT1079C 0°C to 70°C
 Storage Temperature Range
 All Grades - 65°C to 150°C
 Lead Temperature (Soldering, 10 sec.) 300°C

PACKAGE/ORDER INFORMATION

<p>V - (CASE) H PACKAGE 8 LEAD TO-5 METAL CAN</p>	ORDER PART NUMBER
	LT1078AMH LT1078MH LT1078ACH LT1078CH
<p>TOP VIEW J PACKAGE 8 LEAD CERAMIC DIP N PACKAGE 8 LEAD PLASTIC DIP</p>	LT1078AMJ8 LT1078MJ8 LT1078ACJ8 LT1078CJ8 LT1078ACN8 LT1078CN8
	LT1079AMJ LT1079MJ LT1079ACJ LT1079CJ LT1079ACN LT1079CN
<p>TOP VIEW J PACKAGE 14 LEAD CERAMIC DIP N PACKAGE 14 LEAD PLASTIC DIP</p>	

ELECTRICAL CHARACTERISTICS $V_S = 5V, 0V, V_{CM} = 0.1V, V_O = 1.4V, T_A = 25^\circ C$, unless noted.

SYMBOL	PARAMETER	CONDITIONS (NOTE 1)	LT1078AM/AC LT1079AM/AC			LT1078M/C LT1079M/C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	LT1078 LT1079	30	70		40	120		μV
$\frac{\Delta V_{OS}}{\Delta Time}$	Long Term Input Offset Voltage Stability		0.4			0.5			$\mu V/Mo$
I_{OS}	Input Offset Current		0.05	0.25		0.05	0.35		nA
I_B	Input Bias Current		6	8		6	10		nA
e_n	Input Noise Voltage	0.1Hz to 10Hz (Note 2)	0.6	1.2		0.6			μV_{p-p}
	Input Noise Voltage Density	$f_o = 10Hz$ (Note 2) $f_o = 1000Hz$ (Note 2)	29 28	45 37		29 28			nV/ \sqrt{Hz} nV/ \sqrt{Hz}
i_n	Input Noise Current	0.1Hz to 10Hz (Note 2)	2.3	4.0		2.3			pA $_{p-p}$
	Input Noise Current Density	$f_o = 10Hz$ (Note 2) $f_o = 1000Hz$	0.06 0.02	0.10		0.06 0.02			pA/ \sqrt{Hz} pA/ \sqrt{Hz}
	Input Resistance Differential Mode Common-Mode	(Note 3)	400	800 6		300	800 6		M Ω G Ω
	Input Voltage Range		3.5 0	3.8 -0.3		3.5 0	3.8 -0.3		V V
CMRR	Common-Mode Rejection Ratio	$V_{CM} = 0V$ to 3.5V	97	110		94	108		dB
PSRR	Power Supply Rejection Ratio	$V_S = 2.3V$ to 12V	102	114		100	114		dB
A_{VOL}	Large Signal Voltage Gain	$V_O = 0.03V$ to 4V, No Load $V_O = 0.03V$ to 3.5V, $R_L = 50k$	200	1000		150	1000		V/mV
			150	600		120	600		V/mV

ELECTRICAL CHARACTERISTICS $V_S = 5V, 0V, V_{CM} = 0.1V, V_O = 1.4V, T_A = 25^\circ C$, unless noted.

SYMBOL	PARAMETER	CONDITIONS (NOTE 1)	LT1078AM/AC LT1079AM/AC			LT1078M/C LT1079M/C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
	Maximum Output Voltage Swing	Output Low, No Load		3.5	6		3.5	6	mV
		Output Low, 2k to GND		0.55	1.0		0.55	1.0	mV
		Output Low, $I_{SINK} = 100\mu A$		95	130		95	130	mV
		Output High, No Load	4.2	4.4		4.2	4.4		V
		Output High, 2k to GND	3.5	3.9		3.5	3.9		V
SR	Slew Rate	$A_v = +1, V_S = \pm 2.5V$	0.04	0.07		0.04	0.07	$V/\mu s$	
GBW	Gain Bandwidth Product	$f_o \leq 20kHz$		200		200		kHz	
I_S	Supply Current per Amplifier			38	50		39	55	μA
	Channel Separation	$\Delta V_{IN} = 3V, R_L = 10k$		130		130			dB
	Minimum Supply Voltage	(Note 4)		2.2	2.3		2.2	2.3	V

ELECTRICAL CHARACTERISTICS $V_S = 5V, 0V, V_{CM} = 0.1V, V_O = 1.4V, -55^\circ C \leq T_A \leq 125^\circ C$, unless noted.

SYMBOL	PARAMETER	CONDITIONS	LT1078AM/1079AM			LT1078M/1079M			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	LT1078	●	65	250		85	370	μV
		LT1079	●	80	260		100	400	μV
$\Delta V_{OS}/\Delta T$	Input Offset Voltage Drift	(Note 5)	●	0.4	1.8		0.5	2.5	$\mu V/^\circ C$
I_{OS}	Input Offset Current		●	0.07	0.50		0.07	0.70	nA
I_B	Input Bias Current		●	7	10		7	12	nA
CMRR	Common-Mode Rejection Ratio	$V_{CM} = 0.05V$ to 3.2V	●	92	106		88	104	dB
PSRR	Power Supply Rejection Ratio	$V_S = 3.1V$ to 12V	●	98	110		94	110	dB
A_{VOL}	Large Signal Voltage Gain	$V_O = 0.05V$ to 4V, No Load	●	110	600		80	600	V/mV
		$V_O = 0.05V$ to 3.5V, $R_L = 50k$	●	80	400		60	400	V/mV
	Maximum Output Voltage Swing	Output Low, No Load	●	4.5	8		4.5	8	mV
		Output Low, $I_{SINK} = 100\mu A$	●	125	170		125	170	mV
		Output High, No Load	●	3.9	4.2		3.9	4.2	V
		Output High, 2k to GND	●	3.0	3.7		3.0	3.7	V
				●	43	60		45	70
I_S	Supply Current per Amplifier		●	43	60		45	70	μA

2

ELECTRICAL CHARACTERISTICS $V_S = 5V, 0V, V_{CM} = 0.1V, V_O = 1.4V, 0^\circ C \leq T_A \leq 70^\circ C$, unless noted.

SYMBOL	PARAMETER	CONDITIONS	LT1078AC/1079AC			LT1078C/1079C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	LT1078	●	50	150		60	240	μV
		LT1079	●	60	180		70	270	μV
$\Delta V_{OS}/\Delta T$	Input Offset Voltage Drift	(Note 5)	●	0.4	1.8		0.5	2.5	$\mu V/^\circ C$
I_{OS}	Input Offset Current		●	0.06	0.35		0.06	0.50	nA
I_B	Input Bias Current		●	6	9		6	11	nA
CMRR	Common-Mode Rejection Ratio	$V_{CM} = 0V$ to 3.4V	●	94	108		90	106	dB
PSRR	Power Supply Rejection Ratio	$V_S = 2.6V$ to 12V	●	100	112		97	112	dB
A_{VOL}	Large Signal Voltage Gain	$V_O = 0.05V$ to 4V, No Load	●	150	750		110	750	V/mV
		$V_O = 0.05V$ to 3.5V, $R_L = 50K$	●	110	500		80	500	V/mV
	Maximum Output Voltage Swing	Output Low, No Load	●	4.0	7		4.0	7	mV
		Output Low, $I_{SINK} = 100\mu A$	●	105	150		105	150	mV
		Output High, No Load	●	4.1	4.3		4.1	4.3	V
		Output High, 2k to GND	●	3.3	3.8		3.3	3.8	V
			●	40	55		42	63	μA
I_S	Supply Current per Amplifier		●	40	55		42	63	μA

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V, T_A = 25^\circ C$, unless noted.

SYMBOL	PARAMETER	CONDITIONS	LT1078AM/AC LT1079AM/AC			LT1078M/C LT1079M/C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage		45	250		50	350	μV	
I_{OS}	Input Offset Current		0.05	0.25		0.05	0.35	nA	
I_B	Input Bias Current		6	8		6	10	nA	
	Input Voltage Range		13.5	13.8		13.5	13.8	V	
			-15.0	-15.3		-15.0	-15.3	V	
CMRR	Common-Mode Rejection Ratio	$V_{CM} + 13.5V, -15V$	100	114		97	114	dB	
PSRR	Power Supply Rejection Ratio	$V_S = 5V, 0V$ to $\pm 18V$	102	114		100	114	dB	
A_{VOL}	Large Signal Voltage Gain	$V_O = \pm 10V, R_L = 50k$ $V_O = \pm 10V, R_L = 2k$	1000 400	5000 1100		1000 300	5000 1100	V/mV V/mV	
V_{OUT}	Maximum Output Voltage Swing	$R_L = 50k$ $R_L = 2k$	± 13.0 ± 11.0	± 14.0 ± 13.2		± 13.0 ± 11.0	± 14.0 ± 13.2	V V	
SR	Slew Rate		0.06	0.10		0.06	0.10	V/ μs	
I_S	Supply Current per Amplifier		46	65		47	75	μA	

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V, -55^\circ C \leq T_A \leq 125^\circ C$, unless noted.

SYMBOL	PARAMETER	CONDITIONS	LT1078AM/1079AM			LT1078M/1079M			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage		●	85	430		100	600	μV
$\Delta V_{OS}/\Delta T$	Input Offset Voltage Drift	(Note 5)	●	0.4	1.8		0.5	2.5	$\mu V/^\circ C$
I_{OS}	Input Offset Current		●	0.07	0.50		0.07	0.70	nA
I_B	Input Bias Current		●	7	10		7	12	nA
A_{VOL}	Large Signal Voltage Gain	$V_O = \pm 10V, R_L = 5k$	●	200	700		150	700	V/mV
CMRR	Common-Mode Rejection Ratio	$V_{CM} = +13V, -14.9V$	●	94	110		90	110	dB
PSRR	Power Supply Rejection Ratio	$V_S = 5V, 0V$ to $\pm 18V$	●	98	110		94	110	dB
	Maximum Output Voltage Swing	$R_L = 5k$	●	± 11.0	± 13.5		± 11.0	± 13.5	V
I_S	Supply Current per Amplifier		●	52	80		54	95	μA

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V, 0^\circ C \leq T_A \leq 70^\circ C$, unless noted.

SYMBOL	PARAMETER	CONDITIONS	LT1078AC/1079AC			LT1078C/1079C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage		●	60	330		75	460	μV
$\Delta V_{OS}/\Delta T$	Input Offset Voltage Drift	(Note 5)	●	0.4	1.8		0.5	2.5	$\mu V/^\circ C$
I_{OS}	Input Offset Current		●	0.06	0.35		0.06	0.50	nA
I_B	Input Bias Current		●	6	9		6	11	nA
A_{VOL}	Large Signal Voltage Gain	$V_O = \pm 10V, R_L = 5k$	●	300	1200		250	1200	V/mV
CMRR	Common-Mode Rejection Ratio	$V_{CM} = 13V, -15V$	●	97	112		94	112	dB
PSRR	Power Supply Rejection Ratio	$V_S = 5V, 0V$ to $\pm 18V$	●	100	112		97	112	dB
	Maximum Output Voltage Swing	$R_L = 5k$	●	± 11.0	± 13.6		± 11.0	± 13.6	V
I_S	Supply Current per Amplifier		●	49	73		50	85	μA

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: Typical parameters are defined as the 60% yield of parameter distributions of individual amplifiers; i.e., out of 100 LT1079s (or 100 LT1078s) typically 240 op amps (or 120) will be better than the indicated specification.

Note 2: This parameter is tested on a sample basis only. All noise

parameters are tested with $V_S = \pm 2.5V, V_O = 0V$.

Note 3: This parameter is guaranteed by design and is not tested.

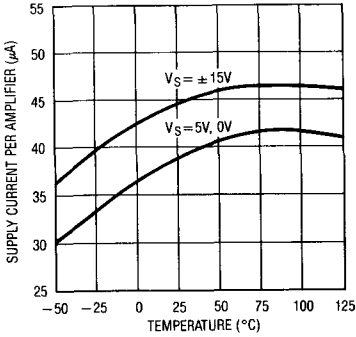
Note 4: Power supply rejection ratio is measured at the minimum supply voltage. The op amps actually work at 1.8V supply but with a typical offset skew of $-300\mu V$.

Note 5: This parameter is not 100% tested.

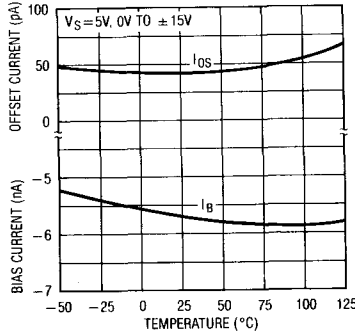
TYPICAL PERFORMANCE CHARACTERISTICS

2

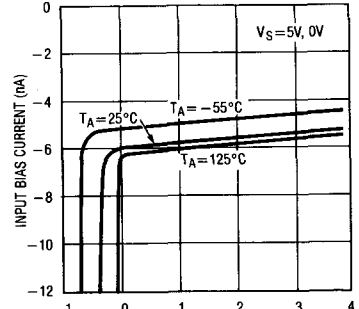
Supply Current vs Temperature



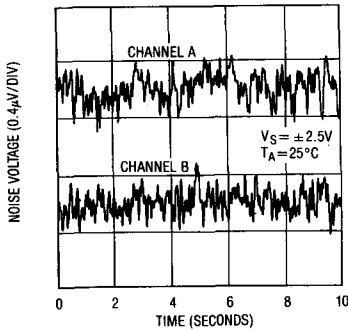
Input Bias and Offset Currents vs Temperature



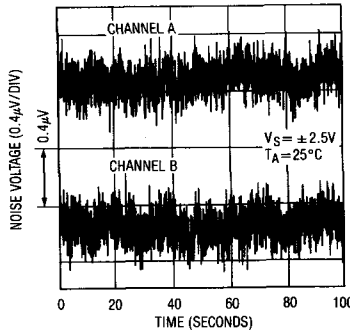
Input Bias Current vs Common-Mode Voltage



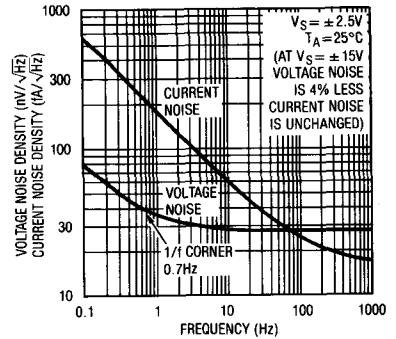
0.1Hz to 10Hz Noise



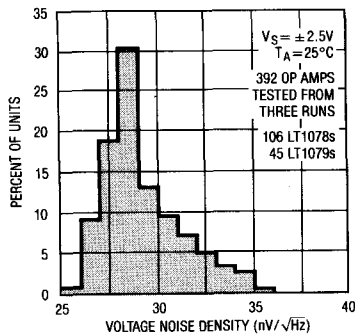
0.01Hz to 10Hz Noise



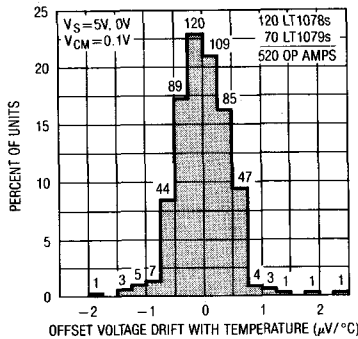
Noise Spectrum



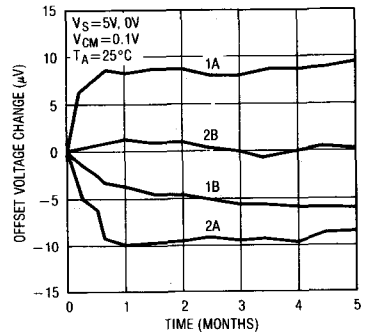
10Hz Voltage Noise Distribution



Distribution of Offset Voltage Drift with Temperature (In All Packages)

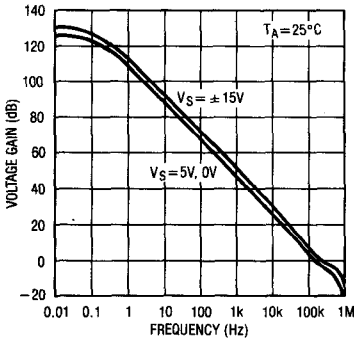


Long Term Stability of Two Representative Units (LT1078)

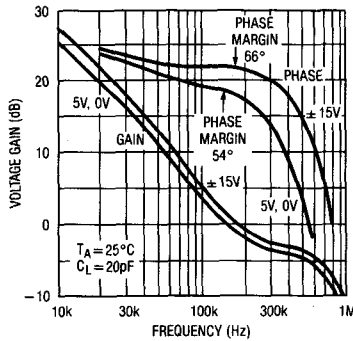


TYPICAL PERFORMANCE CHARACTERISTICS

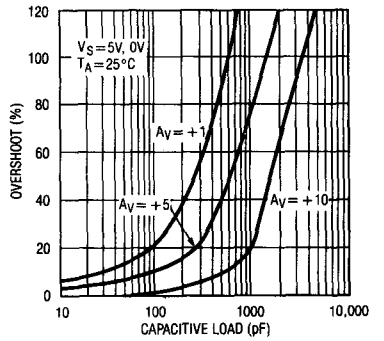
Voltage Gain vs Frequency



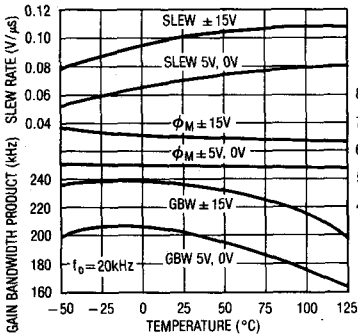
Gain, Phase vs Frequency



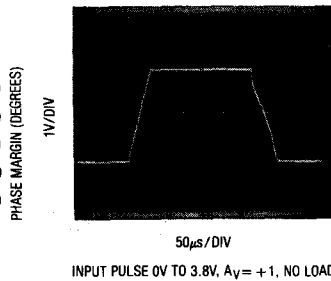
Capacitive Load Handling



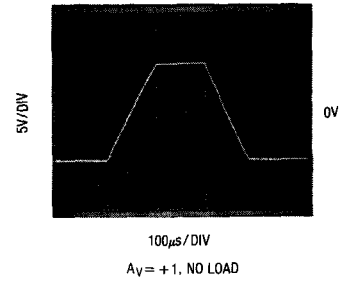
Slow Rate, Gain Bandwidth Product and Phase Margin vs Temperature



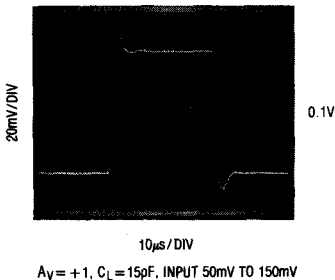
Large Signal Transient Response VS = 5V, 0V



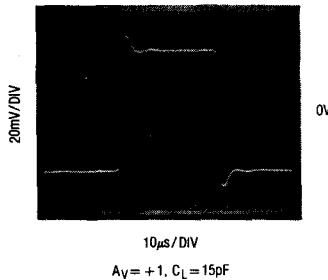
Large Signal Transient Response VS = ±15V



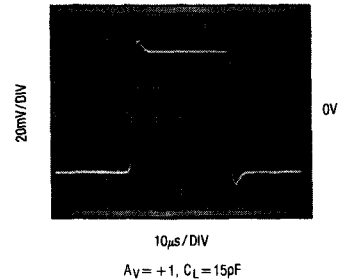
Small Signal Transient Response VS = 5V, 0V



Small Signal Transient Response VS = ±2.5V

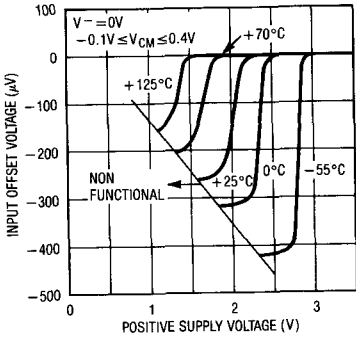


Small Signal Transient Response VS = ±15V

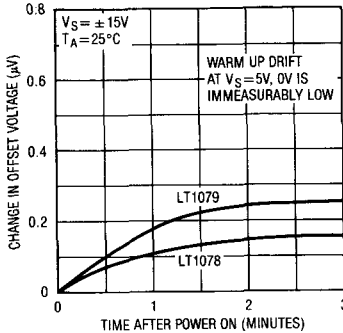


TYPICAL PERFORMANCE CHARACTERISTICS

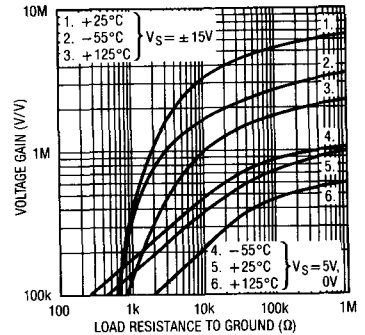
Minimum Supply Voltage



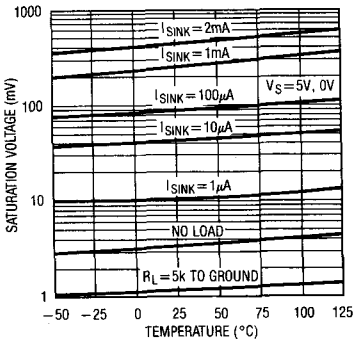
Warm-Up Drift



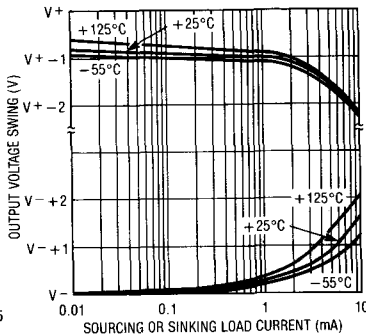
Voltage Gain vs Load Resistance



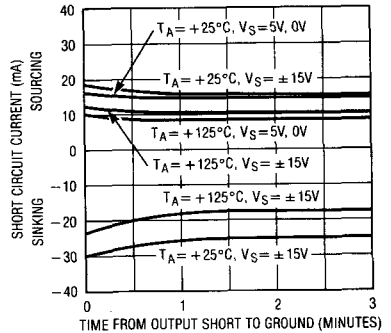
Output Saturation vs Temperature vs Sink Current



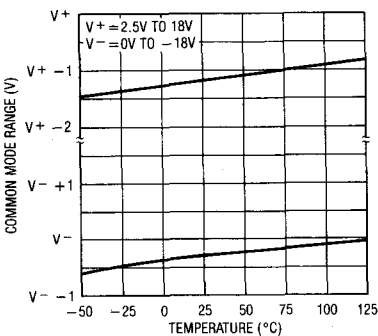
Output Voltage Swing vs Load Current



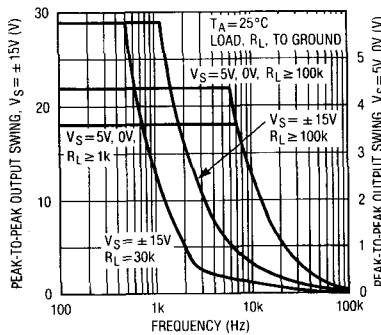
Short Circuit Current vs Time



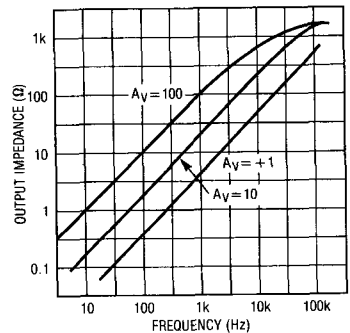
Common Mode Range vs Temperature



Undistorted Output Swing vs Frequency

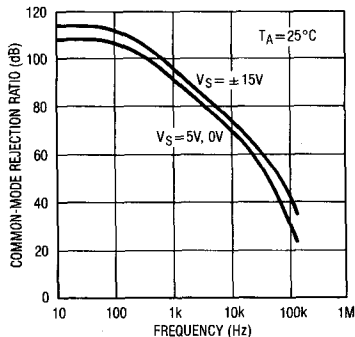


Closed Loop Output Impedance

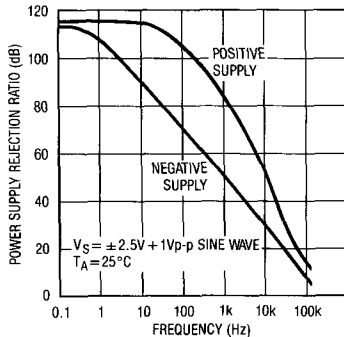


TYPICAL PERFORMANCE CHARACTERISTICS

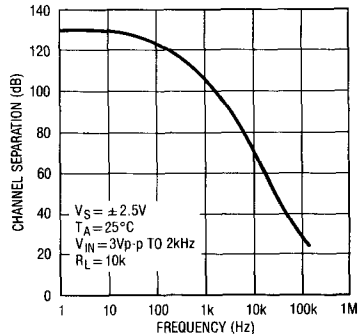
Common-Mode Rejection Ratio vs Frequency



Power Supply Rejection Ratio vs Frequency



Channel Separation vs Frequency



APPLICATIONS INFORMATION

The LT1078/LT1079 devices are fully specified with $V^+ = 5V$, $V^- = 0$, $V_{CM} = 0.1V$. This set of operating conditions appears to be the most representative for battery powered micropower circuits. Offset voltage is internally trimmed to a minimum value at these supply voltages. When 9V or 3V batteries or $\pm 2.5V$ dual supplies are used, bias and offset current changes will be minimal. Offset voltage changes will be just a few microvolts as given by the PSRR and CMRR specifications. For example, if $PSRR = 114dB (= 2\mu V/V)$, at 9V the offset voltage change will be $8\mu V$. Similarly, $V_S = \pm 2.5V$, $V_{CM} = 0$ is equivalent to a common-mode voltage change of 2.4V or a V_{OS} change of $7\mu V$ if $CMRR = 110dB (= 3\mu V/V)$.

A full set of specifications is also provided at $\pm 15V$ supply voltages for comparison with other devices and for completeness.

Single Supply Operation

The LT1078/LT1079 are fully specified for single supply operation, i.e., when the negative supply is 0V. Input common-mode range goes below ground and the output swings within a few millivolts of ground while sinking current. All competing micropower op amps either cannot swing to within 600mV of ground (OP-20, OP-220, OP-420)

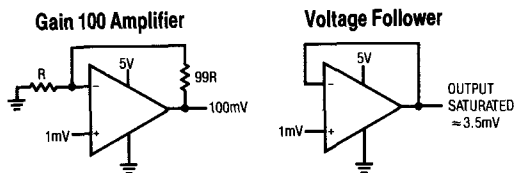
or need a pull down resistor connected to the output to swing to ground (OP-90, OP-290, OP-490, HA5141/42/44). This difference is critical because in many applications these competing devices cannot be operated as micropower op amps and swing to ground simultaneously.

As an example, consider the instrumentation amplifier shown on the front page. When the common-mode signal is low and the output is high, amplifier A has to sink current. When the common-mode signal is high and the output low, amplifier B has to sink current. The competing devices require a 12k pull down resistor at the output of amplifier A and a 15k at the output of B to handle the specified signals. (The LT1078 does not need pull down resistors.) When the common-mode input is high and the output is high these pull down resistors draw $300\mu A$ ($150\mu A$ each), which is excessive for micropower applications.

The instrumentation amplifier is by no means the only application requiring current sinking capability. In 7 of the 9 single supply applications shown in this data sheet the op amps have to be able to sink current. In two of the applications the first amplifier has to sink only the 6nA input bias current of the second op amp. The competing devices, however, cannot even sink 6nA without a pull down resistor.

APPLICATIONS INFORMATION

Since the output of the LT1078/LT1079 cannot go exactly to ground, but can only approach ground to within a few millivolts, care should be exercised to ensure that the output is not saturated. For example, a 1 mV input signal will cause the amplifier to set up in its linear region in the gain 100 configuration shown below, but is not enough to make the amplifier function properly in the voltage follower mode.



Single supply operation can also create difficulties at the input. The driving signal can fall below 0V—inadvertently

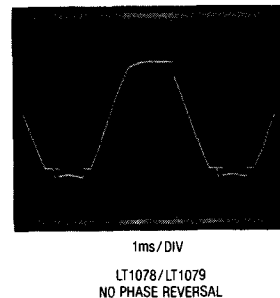
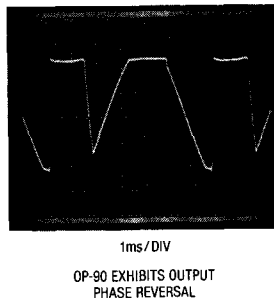
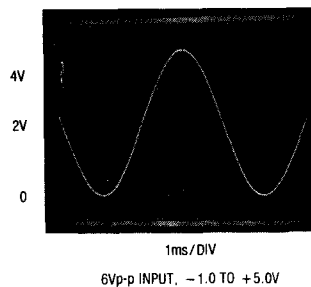
or on a transient basis. If the input is more than a few hundred millivolts below ground, two distinct problems can occur on previous single supply designs, such as the LM124, LM158, OP-20, OP-21, OP-220, OP-221, OP-420 (a and b), OP-90/290/490 (b only):

a) When the input is more than a diode drop below ground, unlimited current will flow from the substrate (V^- terminal) to the input. This can destroy the unit. On the LT1078/LT1079, resistors in series with the input protect the devices even when the input is 5V below ground.

b) When the input is more than 400mV below ground (at 25°C), the input stage saturates and phase reversal occurs at the output. This can cause lock-up in servo systems. Due to a unique phase reversal protection circuitry, the LT1078/LT1079's output does not reverse, as illustrated below, even when the inputs are at $-1.0V$.

2

Voltage Follower with Input Exceeding the Negative Common-Mode Range ($V_S = 5V, 0V$)

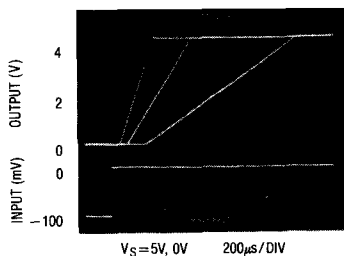


Comparator Applications

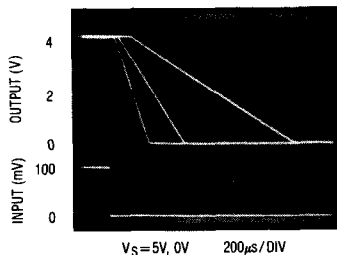
The single supply operation of the LT1078/1079 and its ability to swing close to ground while sinking current

lends itself to use as a precision comparator with TTL compatible output.

Comparator Rise Response Time to 10mV, 5mV, 2mV Overdrives



Comparator Fall Response Time to 10mV, 5mV, 2mV Overdrives



APPLICATIONS INFORMATION

Matching Specifications

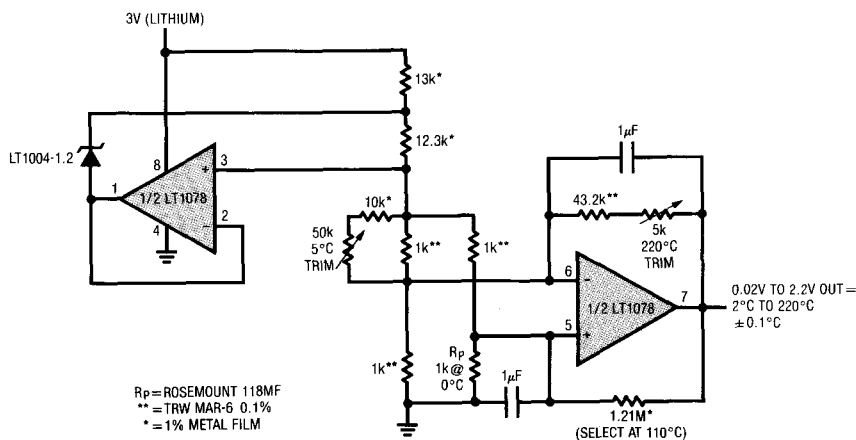
In many applications the performance of a system depends on the matching between two op amps, rather than the individual characteristics of the two devices. The two and three op amp instrumentation amplifier configurations shown in this data sheet are examples. Matching characteristics are not 100% tested on the LT1078/79.

Some specifications are guaranteed by definition. For example, $70\mu\text{V}$ maximum offset voltage implies that mismatch cannot be more than $140\mu\text{V}$. 97dB ($= 14\mu\text{V/V}$) CMRR means that worst case CMRR match is 91dB ($= 28\mu\text{V/V}$). However, the following table can be used to estimate the expected matching performance at $V_S = 5\text{V}$, 0V between the two sides of the LT1078, and between amplifiers A and D, and between amplifiers B and C of the LT1079.

PARAMETER	LT1078A/M/AC LT1079A/M/AC		LT1078M/C LT1079M/C		UNITS	
	50% YIELD	98% YIELD	50% YIELD	98% YIELD		
V_{OS} Match, ΔV_{OS}	LT1078	30	110	50	190	μV
	LT1079	40	150	50	250	
Temperature Coefficient ΔV_{OS}	0.5	1.2	0.6	1.8	$\mu\text{V}/^\circ\text{C}$	
Average Non-Inverting I_B	6	8	6	10	nA	
Match of Non-Inverting I_B	0.12	0.4	0.15	0.5	nA	
CMRR Match	120	100	117	97	dB	
PSRR Match	117	105	117	102	dB	

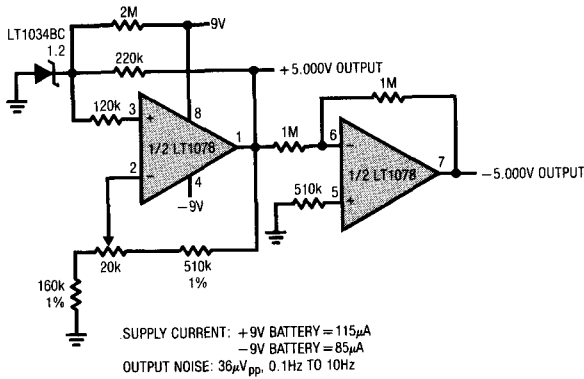
TYPICAL APPLICATIONS

Platinum RTD Signal Conditioner with Curvature Correction



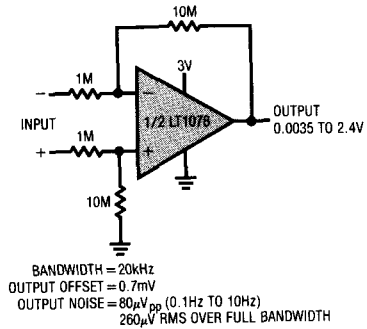
TYPICAL APPLICATIONS

Micropower, 10ppm/°C, ±5V Reference



THE LT1078 CONTRIBUTES LESS THAN 3% OF THE TOTAL OUTPUT NOISE AND DRIFT WITH TIME AND TEMPERATURE. THE ACCURACY OF THE -5V OUTPUT DEPENDS ON THE MATCHING OF THE TWO 1M RESISTORS.

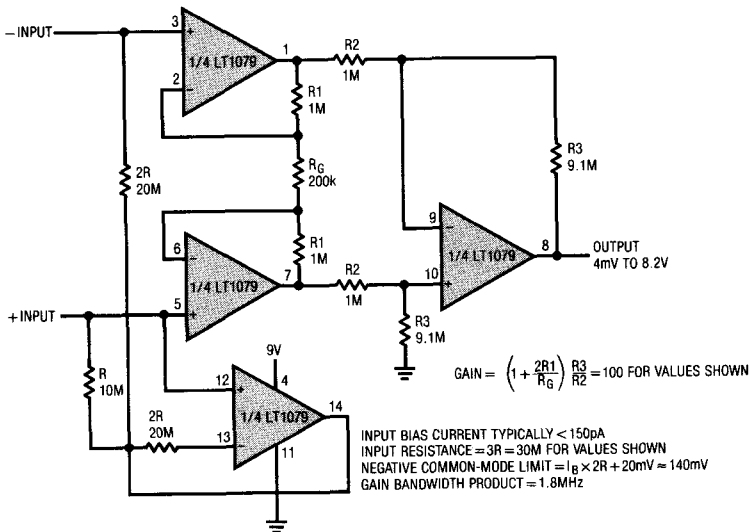
Gain of 10 Difference Amplifier



THE USEFULNESS OF DIFFERENCE AMPLIFIERS IS LIMITED BY THE FACT THAT THE INPUT RESISTANCE IS EQUAL TO THE SOURCE RESISTANCE. THE PICO-AMPERE OFFSET CURRENT AND LOW CURRENT NOISE OF THE LT1078 ALLOWS THE USE OF 1MΩ SOURCE RESISTORS WITHOUT DEGRADATION IN PERFORMANCE. IN ADDITION, WITH MEGAΩHM RESISTORS MICROPOWER OPERATION CAN BE MAINTAINED.

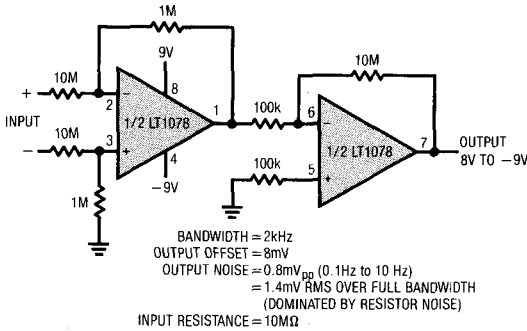
2

Picoampere Input Current, Triple Op Amp Instrumentation Amplifier with Bias Current Cancellation

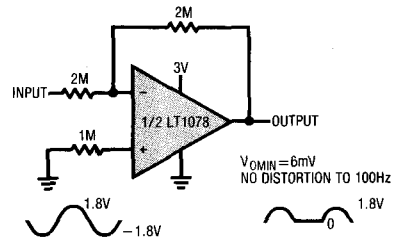


TYPICAL APPLICATIONS

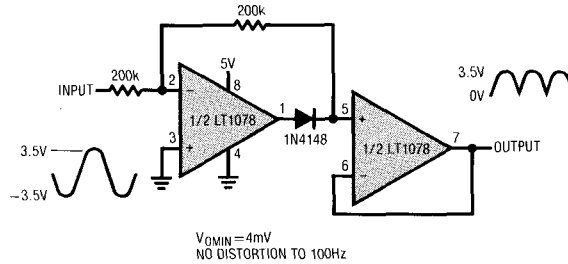
+85V, -100V Common Mode Range Instrumentation Amplifier (A_v = 10)



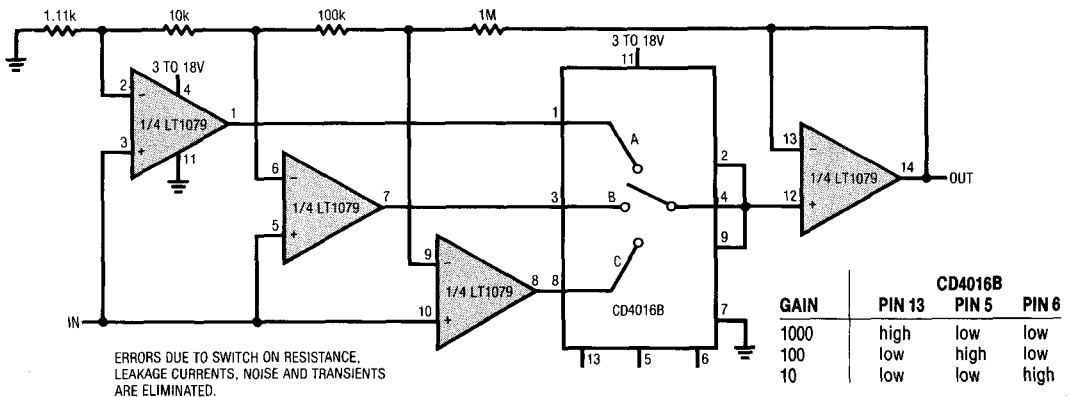
Half-Wave Rectifier



Absolute Value Circuit (Full-Wave Rectifier)

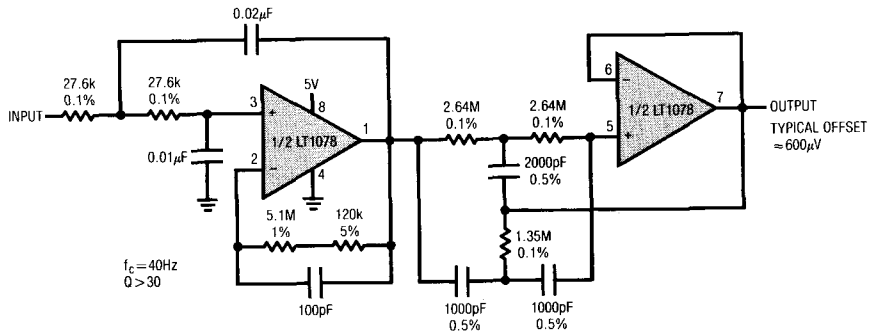


Programmable Gain Amplifier (Single Supply)



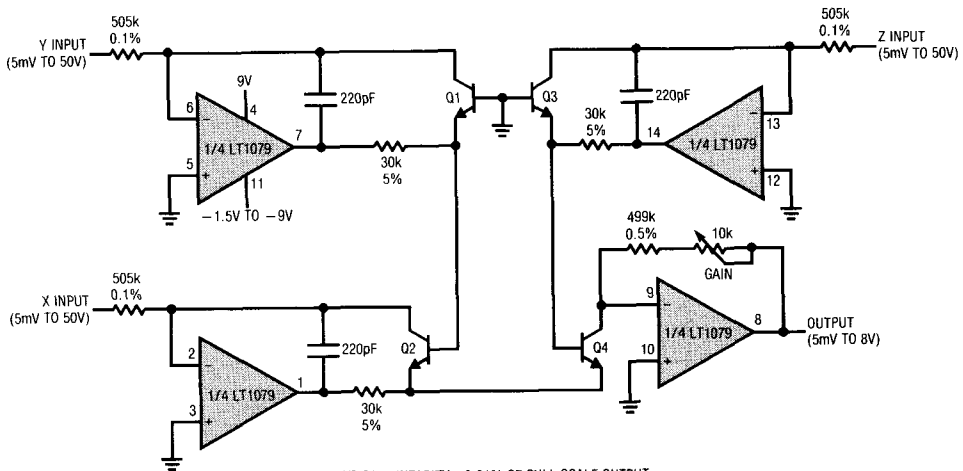
TYPICAL APPLICATIONS

Single Supply, Micropower, Second Order Low Pass Filter with 60Hz Notch



2

Micropower Multiplier/Divider



TYPICAL LINEARITY = 0.01% OF FULL SCALE OUTPUT

Q1-Q4 = MAT-04

NEGATIVE SUPPLY CURRENT = $165\mu\text{A} + \frac{X+Y+Z+OUT}{500k}$

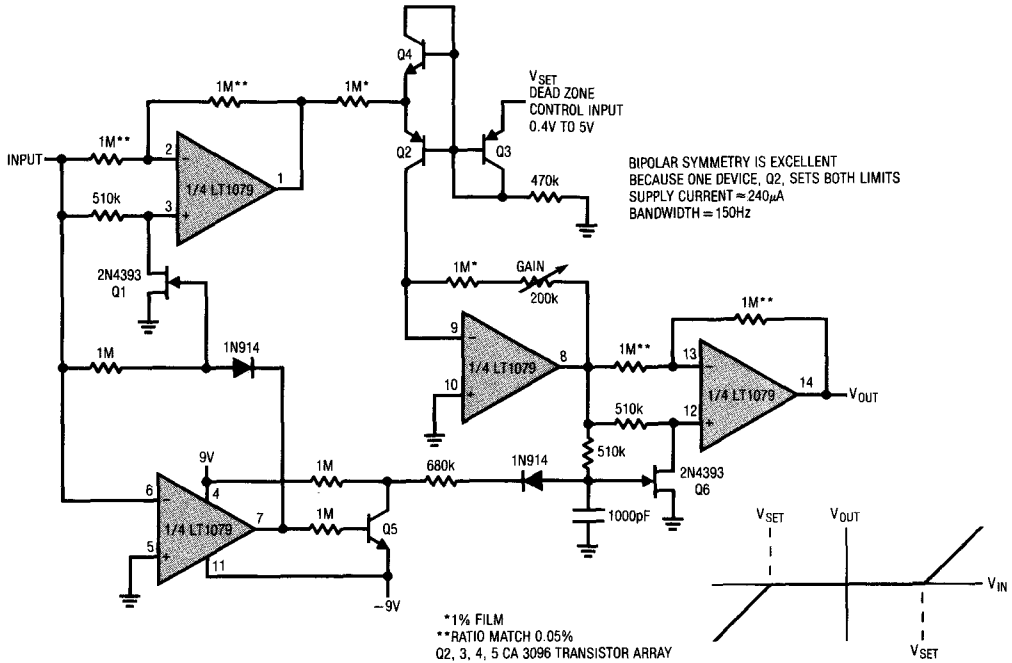
OUTPUT = $\frac{(X)(Y)}{(Z)}$ POSITIVE INPUTS ONLY

POSITIVE SUPPLY CURRENT = $165\mu\text{A} + \frac{OUT}{500k}$

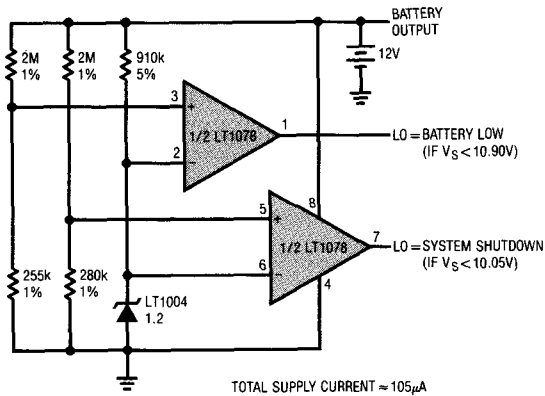
BANDWIDTH (< 3V_{pp} SIGNAL): X AND Y INPUTS = 10kHz
Z INPUT = 4kHz

TYPICAL APPLICATIONS

Micropower Dead Zone Generator

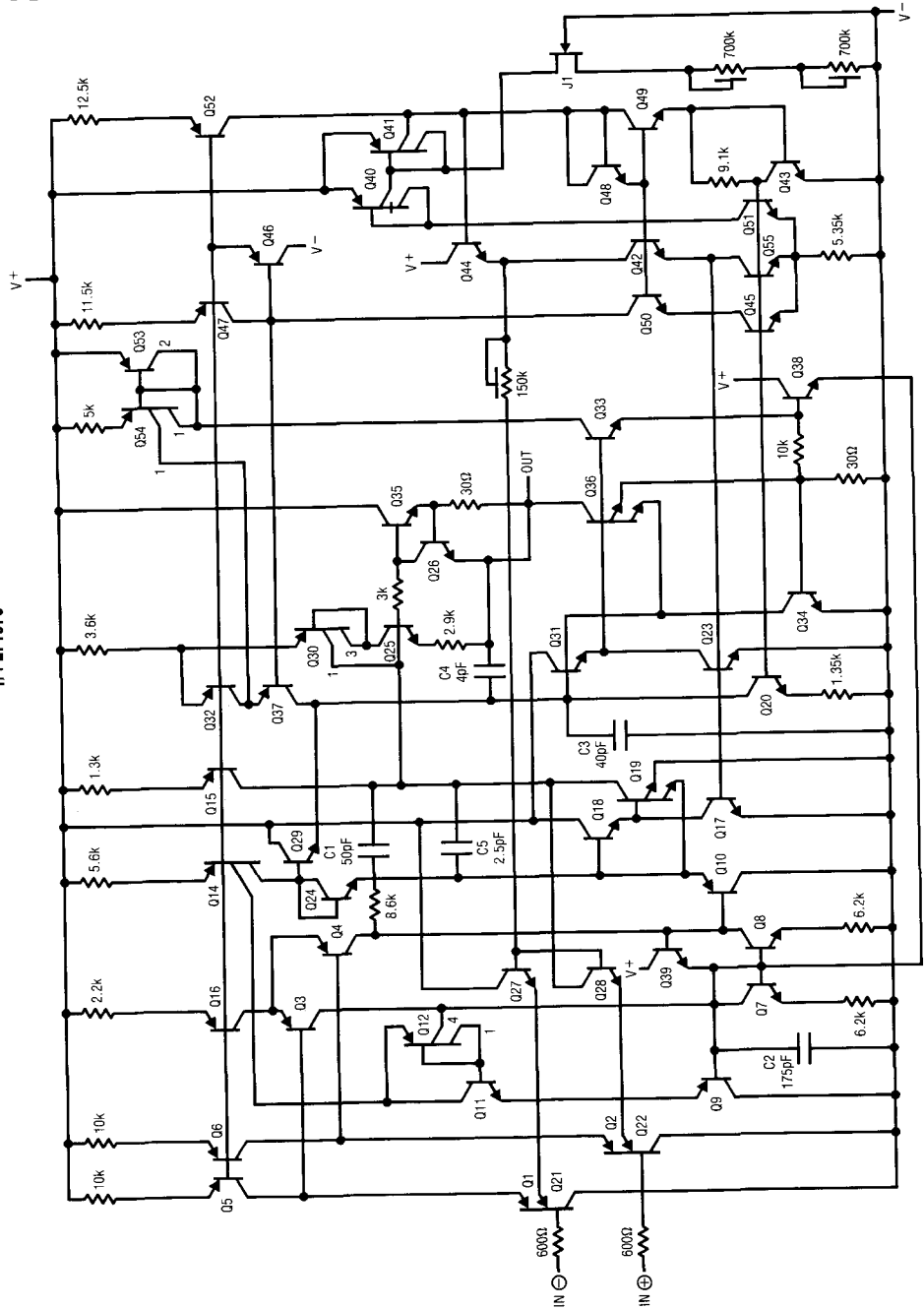


Lead Acid Low Battery Detector with System Shutdown



SIMPLIFIED SCHEMATIC

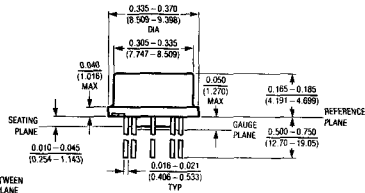
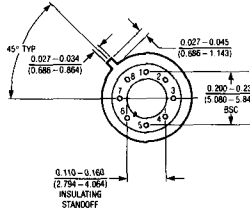
1/2 LT1078
1/4 LT1079



2

PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

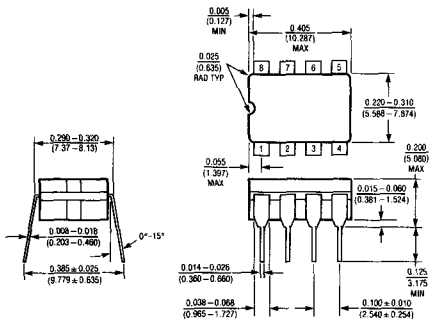
H Package
8 Lead TO-5 Metal Can



NOTE: LEAD DIAMETER IS UNCONTROLLED BETWEEN THE REFERENCE PLANE AND SEATING PLANE.

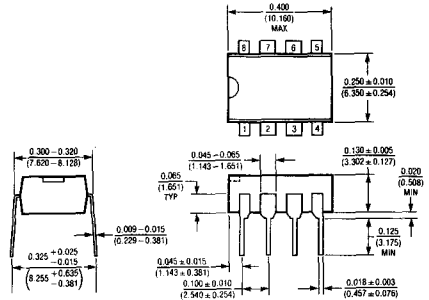
T_{JMAX}	θ_{JA}	θ_{JC}
150°C	150°C/W	45°C/W

J Package
8 Lead Ceramic DIP



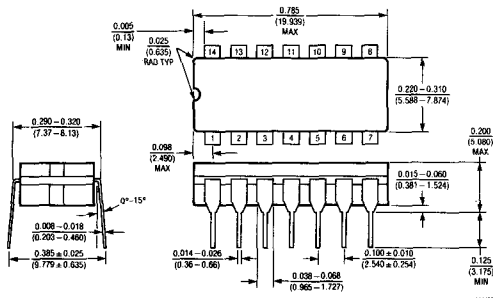
T_{JMAX}	θ_{JA}
150°C	100°C/W

N Package
8 Lead Plastic DIP



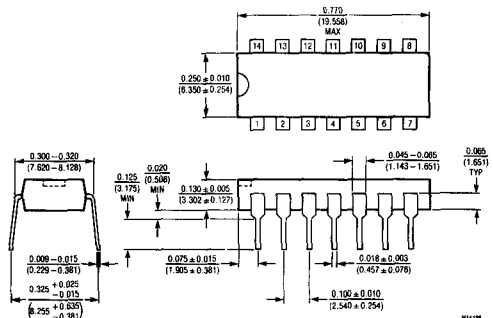
T_{JMAX}	θ_{JA}
100°C	130°C/W

J Package
14 Lead Ceramic DIP



T_{JMAX}	θ_{JA}
150°C	100°C/W

N Package
14 Lead Plastic DIP



T_{JMAX}	θ_{JA}
110°C	130°C/W

FEATURES

- 17 μ A Max Supply Current per Amplifier
- 70 μ V Max Offset Voltage
- 250pA Max Offset Current
- 5nA Max Input Bias Current
- 0.9 μ Vp-p 0.1Hz to 10Hz Voltage Noise
- 1.5pAp-p 0.1Hz to 10Hz Current Noise
- 0.5 μ V/ $^{\circ}$ C Offset Voltage Drift
- 85kHz Gain-Bandwidth-Product
- 0.04V/ μ s Slew Rate
- Single Supply Operation
 - Input Voltage Range Includes Ground
 - Output Swings to Ground while Sinking Current
 - No Pull Down Resistors are Needed
- Output Sources and Sinks 5mA Load Current

APPLICATIONS

- Battery or Solar Powered Systems
 - Portable Instrumentation
 - Remote Sensor Amplifier
 - Satellite Circuits
- Micropower Sample and Hold
- Thermocouple Amplifier
- Micropower Filters

DESCRIPTION

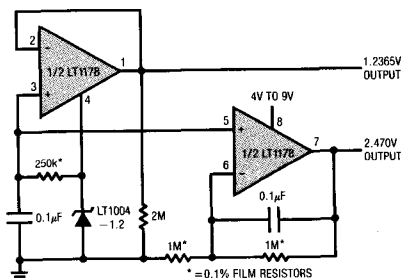
The LT1178 is a micropower dual op amp in the standard 8-pin configuration; the LT1179 is a micropower quad op amp offered in the standard 14-pin packages. Both devices are optimized for single supply operation at 5V. Specifications are also provided at ± 15 V supplies.

The extremely low supply current is combined with true precision specifications: offset voltage is 30 μ V, offset current is 50pA. Both offset parameters have low drift with temperature. The 1.5pAp-p output noise and picoampere offset current permit the use of megaohm level source resistors without introducing serious errors. Voltage noise, at 0.9 μ Vp-p, is remarkably low considering the low supply current.

Both the LT1178 and LT1179 can be operated from a single supply (as low as one lithium cell or two Ni-cad batteries). The input range goes below ground. The all-NPN output stage swings to within a few millivolts of ground while sinking current—no power consuming pull down resistors are needed.

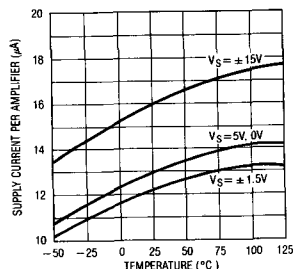
For applications where three times higher supply current is acceptable, the micropower LT1078 dual and LT1079 quad are recommended. The LT1078/79 have significantly higher bandwidth, slew rate; lower voltage noise and better output drive capability.

Self-Buffered, Dual Output, Micropower Reference



* = 0.1% FILM RESISTORS
 TOTAL BATTERY CURRENT = 26 μ A
 OUTPUT ACCURACY = $\pm 0.4\%$ MAX
 TEMPERATURE COEFFICIENT = 20ppm/ $^{\circ}$ C
 LOAD REGULATION = 25ppm/mA, $I_L \leq 5$ mA, $V^+ \geq 5$ V
 LINE REGULATION = 10ppm/V

Supply Current vs Temperature



ABSOLUTE MAXIMUM RATINGS

- Supply Voltage $\pm 22V$
- Differential Input Voltage $\pm 30V$
- Input Voltage Equal to Positive Supply Voltage
..... 5V Below Negative Supply Voltage
- Output Short Circuit Duration Indefinite
- Operating Temperature Range
LT1178AM/LT1178M/
LT1179AM/LT1179M $-55^{\circ}C$ to $125^{\circ}C$
LT1178AC/LT1178C/
LT1179AC/LT1179C $0^{\circ}C$ to $70^{\circ}C$
- Storage Temperature Range
All Grades $-65^{\circ}C$ to $150^{\circ}C$
- Lead Temperature (Soldering, 10 sec.) $300^{\circ}C$

PACKAGE/ORDER INFORMATION

	ORDER PART NUMBER
	LT1178AMH LT1178MH LT1178ACH LT1178CH
	LT1178AMJ8 LT1178MJ8 LT1178ACJ8 LT1178CJ8 LT1178ACN8 LT1178CN8
	LT1179AMJ LT1179MJ LT1179ACJ LT1179CJ LT1179ACN LT1179CN

ELECTRICAL CHARACTERISTICS $V_S = 5V, 0V, V_{CM} = 0.1V, V_O = 1.4V, T_A = 25^{\circ}C$, unless noted.

SYMBOL	PARAMETER	CONDITIONS (NOTE 1)	LT1178AM/IC LT1179AM/IC			LT1178M/IC LT1179M/IC			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	LT1178 LT1179	30 35	70 100		40 40	120 150	μV μV	
$\frac{\Delta V_{OS}}{\Delta Time}$	Long Term Input Offset Voltage Stability		0.5			0.6			$\mu V/Mo$
I_{OS}	Input Offset Current		0.05	0.25		0.05	0.35	nA	
I_B	Input Bias Current		3	5		3	6	nA	
e_n	Input Noise Voltage	0.1Hz to 10Hz (Note 2)	0.9	2.0		0.9		$\mu Vp-p$	
	Input Noise Voltage Density	$f_o = 10Hz$ (Note 2) $f_o = 1000Hz$ (Note 2)	50 49	75 65		50 49		nV/ \sqrt{Hz} nV/ \sqrt{Hz}	
i_n	Input Noise Current	0.1Hz to 10Hz (Note 2)	1.5	2.5		1.5		pAp-p	
	Input Noise Current Density	$f_o = 10Hz$ (Note 2) $f_o = 1000Hz$	0.03 0.01	0.07		0.03 0.01		pA/ \sqrt{Hz} pA/ \sqrt{Hz}	
	Input Resistance Differential Mode Common-Mode	(Note 3)	0.8	2.0 12		0.6	2.0 12	G Ω G Ω	
	Input Voltage Range		3.5 0	3.9 -0.3		3.5 0	3.9 -0.3	V V	
CMRR	Common-Mode Rejection Ratio	$V_{CM} = 0V$ to $3.5V$	93	103		90	102	dB	
PSRR	Power Supply Rejection Ratio	$V_S = 2.2V$ to $12V$	94	104		92	104	dB	
A_{VOL}	Large Signal Voltage Gain	$V_O = 0.03V$ to $4V$, No Load (Note 3) $V_O = 0.03V$ to $3.5V, R_L = 50k$	140 80	700 200		110 70	700 200	V/mV V/mV	

ELECTRICAL CHARACTERISTICS $V_S = 5V, 0V, V_{CM} = 0.1V, V_O = 1.4V, T_A = 25^\circ C$, unless noted.

SYMBOL	PARAMETER	CONDITIONS (NOTE 1)	LT1178AM/AC LT1179AM/AC			LT1178M/C LT1179M/C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
	Maximum Output Voltage Swing	Output Low, No Load		6.5	9		6.5	9	mV
		Output Low, 2k to GND		0.2	0.6		0.2	0.6	mV
		Output Low, $I_{SINK} = 100\mu A$		120	160		120	160	mV
		Output High, No Load	4.2	4.4		4.2	4.4		V
		Output High, 2k to GND	3.5	3.8		3.5	3.8		V
SR	Slew Rate	$A_V = +1, C_L = 10pF$ (Note 3)	0.013	0.025		0.013	0.025	V/ μs	
GBW	Gain Bandwidth Product	$f_o \leq 5kHz$		60		60		kHz	
I_S	Supply Current per Amplifier	$V_S = \pm 1.5V, V_O = 0V$		13	18		14	21	μA
				12	17		13	20	μA
	Channel Separation	$\Delta V_{IN} = 3V, R_L = 10k$		130		130		dB	
	Minimum Supply Voltage	(Note 4)		2.0	2.2		2.0	2.2	V

ELECTRICAL CHARACTERISTICS $V_S = 5V, 0V, V_{CM} = 0.1V, V_O = 1.4V, -55^\circ C \leq T_A \leq 125^\circ C$, unless noted.

SYMBOL	PARAMETER	CONDITIONS	LT1178AM/1179AM			LT1178M/1179M			UNITS	
			MIN	TYP	MAX	MIN	TYP	MAX		
V_{OS}	Input Offset Voltage	LT1178	●	80	290		100	420	μV	
		LT1179	●	90	320		110	450	μV	
$\Delta V_{OS}/\Delta T$	Input Offset Voltage Drift	(Note 5)	●	0.5	2.2		0.6	3.0	$\mu V/^\circ C$	
I_{OS}	Input Offset Current		●	0.07	0.50		0.07	0.70	nA	
I_B	Input Bias Current		●	4	7		4	8	nA	
CMRR	Common-Mode Rejection Ratio	$V_{CM} = 0.05V$ to 3.2V	●	87	100		84	98	dB	
PSRR	Power Supply Rejection Ratio	$V_S = 3.0V$ to 12V	●	88	100		86	100	dB	
A_{VOL}	Large Signal Voltage Gain	$V_O = 0.05V$ to 4V, No Load (Note 3)	●	70	350		55	350	V/mV	
		$V_O = 0.05V$ to 3.5V, $R_L = 50k$	●	40	130		35	130	V/mV	
	Maximum Output Voltage Swing	Output Low, No Load	●		9	13		9	13	mV
		Output Low, $I_{SINK} = 100\mu A$	●		160	220		160	220	mV
		Output High, No Load	●	3.9	4.2		3.9	4.2	V	
		Output High, 2k to GND	●	3.0	3.7		3.0	3.7	V	
				●		14	23		15	27

ELECTRICAL CHARACTERISTICS $V_S = 5V, 0V, V_{CM} = 0.1V, V_O = 1.4V, 0^\circ C \leq T_A \leq 70^\circ C$, unless noted.

SYMBOL	PARAMETER	CONDITIONS	LT1178AC/1179AC			LT1178C/1179C			UNITS	
			MIN	TYP	MAX	MIN	TYP	MAX		
V_{OS}	Input Offset Voltage	LT1178	●	50	170		65	250	μV	
		LT1179	●	60	200		70	290	μV	
$\Delta V_{OS}/\Delta T$	Input Offset Voltage Drift	(Note 5)	●	0.5	2.2		0.6	3.0	$\mu V/^\circ C$	
I_{OS}	Input Offset Current		●	0.06	0.35		0.06	0.50	nA	
I_B	Input Bias Current		●	3	6		3	7	nA	
CMRR	Common-Mode Rejection Ratio	$V_{CM} = 0V$ to 3.4V	●	90	101		86	100	dB	
PSRR	Power Supply Rejection Ratio	$V_S = 2.5V$ to 12V	●	90	102		88	102	dB	
A_{VOL}	Large Signal Voltage Gain	$V_O = 0.05V$ to 4V, No Load (Note 3)	●	105	500		80	500	V/mV	
		$V_O = 0.05V$ to 3.5V, $R_L = 50k$	●	55	160		45	160	V/mV	
	Maximum Output Voltage Swing	Output Low, No Load	●		8	11		8	11	mV
		Output Low, $I_{SINK} = 100\mu A$	●		140	190		140	190	mV
		Output High, No Load	●	4.1	4.3		4.1	4.3	V	
		Output High, 2k to GND	●	3.3	3.8		3.3	3.8	V	
I_S	Supply Current per Amplifier		●	14	21		15	24	μA	

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V, T_A = 25^\circ C$, unless noted.

SYMBOL	PARAMETER	CONDITIONS	LT1178AM/AC LT1179AM/AC			LT1178M/C LT1179M/C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage			80	350		100	480	μV
I_{OS}	Input Offset Current			0.05	0.25		0.05	0.35	nA
I_B	Input Bias Current			3	5		3	6	nA
	Input Voltage Range		13.5 -15.0	13.9 -15.3		13.5 -15.0	13.9 -15.3		V V
CMRR	Common-Mode Rejection Ratio	$V_{CM} = 13.5V, -15V$	97	106		94	106		dB
PSRR	Power Supply Rejection Ratio	$V_S = 5V, 0V$ to $\pm 18V$	96	112		94	112		dB
A_{VOL}	Large Signal Voltage Gain	$V_O = \pm 10V, R_L = 50k$ $V_O = \pm 10V, \text{No Load}$	300 600	1200 2500		250 400	1000 2500		V/mV V/mV
V_{OUT}	Maximum Output Voltage Swing	$R_L = 50k$ $R_L = 2k$	± 13.0 ± 11.0	± 14.2 ± 12.7		± 13.0 ± 11.0	± 14.2 ± 12.7		V V
SR	Slew Rate	$A_V = +1$	0.02	0.04		0.02	0.04		V/ μs
GBW	Gain Bandwidth Product	$f_0 \leq 5kHz$		85			85		kHz
I_S	Supply Current per Amplifier			16	21		17	25	μA

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V, -55^\circ C \leq T_A \leq 125^\circ C$, unless noted.

SYMBOL	PARAMETER	CONDITIONS	LT1178AM/1179AM			LT1178M/1179M			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	●		140	630		170	880	μV
$\Delta V_{OS}/\Delta T$	Input Offset Voltage Drift	(Note 5)	●	0.6	2.8		0.7	4.0	$\mu V/^\circ C$
I_{OS}	Input Offset Current	●		0.07	0.50		0.07	0.70	nA
I_B	Input Bias Current	●		4	7		4	8	nA
A_{VOL}	Large Signal Voltage Gain	$V_O = \pm 10V, R_L = 50k$	●	120	500		100	500	V/mV
CMRR	Common-Mode Rejection Ratio	$V_{CM} = +13V, -14.9V$	●	92	103		88	103	dB
PSRR	Power Supply Rejection Ratio	$V_S = 5V, 0V$ to $\pm 18V$	●	91	109		88	109	dB
	Maximum Output Voltage Swing	$R_L = 5k$	●	± 11.0	± 13.5		± 11.0	± 13.5	V
I_S	Supply Current per Amplifier	●		18	26		19	30	μA

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V, 0^\circ C \leq T_A \leq 70^\circ C$, unless noted.

SYMBOL	PARAMETER	CONDITIONS	LT1178AC/1179AC			LT1178C/1179C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	●		100	480		130	660	μV
$\Delta V_{OS}/\Delta T$	Input Offset Voltage Drift	(Note 5)	●	0.6	2.8		0.7	4.0	$\mu V/^\circ C$
I_{OS}	Input Offset Current	●		0.06	0.35		0.06	0.35	nA
I_B	Input Bias Current	●		3	6		3	7	nA
A_{VOL}	Large Signal Voltage Gain	$V_O = \pm 10V, R_L = 50k$	●	200	800		150	750	V/mV
CMRR	Common-Mode Rejection Ratio	$V_{CM} = 13V, -15V$	●	94	104		91	104	dB
PSRR	Power Supply Rejection Ratio	$V_S = 5V, 0V$ to $\pm 18V$	●	93	110		91	110	dB
	Maximum Output Voltage Swing	$R_L = 5k$	●	± 11.0	± 13.6		± 11.0	± 13.6	V
I_S	Supply Current per Amplifier	●		17	24		18	28	μA

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: Typical parameters are defined as the 60% yield of parameter distributions of individual amplifiers; i.e., out of 100 LT1179s (or 100 LT1178s) typically 240 op amps (or 120) will be better than the indicated specification.

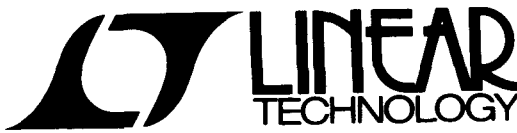
Note 2: This parameter is tested on a sample basis only. All noise

parameters are tested with $V_S = \pm 2.5V, V_O = 0V$.

Note 3: This parameter is guaranteed by design and is not tested.

Note 4: Power supply rejection ratio is measured at the minimum supply voltage. The op amps actually work at 1.7V supply but with a typical offset skew of $-300\mu V$.

Note 5: This parameter is not 100% tested.



LF155A/355A/155/355
LF156A/356A/156/356

JFET-Input Operational Amplifiers
Low Supply Current (LF155)
High Speed (LF156)

FEATURES

- *Guaranteed* Offset Voltage Drift on All Grades
- *Guaranteed* Slew Rate on All Grades
- *Guaranteed* Low Input Offset Current 10pA Max.
- *Guaranteed* Low Input Bias Current 50pA Max.
- *Guaranteed* High Slew Rate (156A/356A) 10V/ μ s Min.
- Fast Settling to 0.01% 1.5 μ s

APPLICATIONS

- Output Amplifiers for D/A Converters
- Fast Sample and Hold Circuits
- High Speed Integrators
- Photocell Amplifiers
- High Input Impedance Buffers

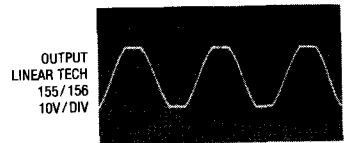
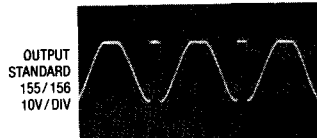
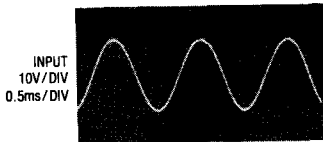
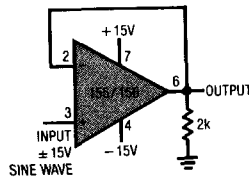
DESCRIPTION

Linear Technology's LF155/156 series features several improvements compared to similar types from other manufacturers: offset voltage drift with temperature and slew rate are guaranteed on all grades, not just on the more expensive "A" grades. Other specifications such as voltage gain and high temperature bias and offset currents are also improved.

The industry standard LF155/156 devices exhibit phase reversal at the output when the negative common-mode limit at the input is exceeded (i.e., from $-12V$ to $-15V$ with $\pm 15V$ supplies). This can cause lock-up in servo systems. As shown below, Linear Technology's LF155/156 does not have this problem due to unique phase reversal protection circuitry. For applications requiring higher performance, see the LT1055 and LT1056 data sheets.

2

Voltage Follower with Input Exceeding the Negative Common-Mode Range



LF155A/355A/155/355 LF156A/356A/156/356

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	
LF155A/155/355A,	
LF156A/156/356A	± 22V
LF355/356	± 18V
Differential Input Voltage	
LF155A/155/156A/156	± 40V
LF355A/355/356A/356	± 30V
Input Voltage (Note 1)	
LF155A/155/156A/156	± 20V
LF355A/355/356A/356	± 16V
Output Short Circuit Duration	Indefinite
Operating Temperature Range	
LF155A/155/156A/156	-55°C to 125°C
LF355A/355/356A/356	0°C to 70°C
Maximum Junction Temperature	
LF155A/155/156A/156	150°C
LF355A/355/356A/356	100°C
Storage Temperature Range	
All Devices	-65°C to 150°C
Lead Temperature (Soldering, 10 sec.)	300°C

PACKAGE/ORDER INFORMATION

TOP VIEW	ORDER PART NUMBER
<p>H PACKAGE METAL CAN</p>	LF155H LF156H LF155AH LF156AH LF355H LF356H LF355AH LF356AH
<p>N8 PACKAGE 8 PIN PLASTIC</p>	LF355N8 LF356N8 LF355AN8 LF356AN8
	V _{OS} is adjusted with a 20k or 50k potentiometer between the balance terminals. The wiper is tied to V ⁺

ELECTRICAL CHARACTERISTICS (Note 2)

SYMBOL	PARAMETER	CONDITIONS	LF155A/156A LF355A/356A			LF155/156			LF355/356			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V _{OS}	Input Offset Voltage	T _A = 25°C Over Temperature 355A/356A	•	1	2	2	3.5	3	8	mV		
$\frac{\Delta V_{OS}}{\Delta T}$	Average TC of Input Offset Voltage	R _S = 50Ω	•	3	5	5	15	5	25	μV/°C		
			•	0.5	0.5	0.5	μV/°C per mV					
I _{OS}	Input Offset Current	T _J = 25°C (Note 3) T _J ≤ 125°C T _J ≤ 70°C	•	3	10	3	20	3	50	pA		
			•	9	9	1.5	nA					
I _B	Input Bias Current	T _J = 25°C (Note 3) T _J ≤ 125°C T _J ≤ 70°C	•	30	50	30	100	30	200	pA		
			•	15	15	3.0	nA					
R _{IN}	Input Resistance	T _J = 25°C		10 ¹²	10 ¹²	10 ¹²	Ω					
A _{VOL}	Large Signal Voltage Gain	V _S = ± 15V, T _A = 25°C, V _O = ± 10V, R _L = 2k Over Temperature	•	75	200	50	200	40	200	V/mV		
			•	30	25	25	V/mV					

ELECTRICAL CHARACTERISTICS (Note 2)

SYMBOL	PARAMETER	CONDITIONS	LF155A/156A LF355A/356A			LF155/156			LF355/356			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V _O	Output Voltage Swing	V _S = ±15V, R _L = 10k V _S = ±15V, R _L = 2k	● ±12	±13		±12	±13		±12	±13		V
			● ±10	±12		±10	±12		±10	±12		V
V _{CM}	Input Common-Mode Voltage Range	V _S = ±15V	● ±11	+15.1 -12		±11	+15.1 -12		±10	+15.1 -12		V
CMRR	Common-Mode Rejection Ratio		● .85	100		85	100		80	100		dB
PSRR	Supply Voltage Rejection Ratio	V _S = ±10V to ±18V V _S = ±10V to ±15V	● 85	100		85	100		80	100		dB dB
I _S	Supply Current	T _A = 25°C, V _S = ±15V LF155/355 Series LF156/356 Series LF356A		2	4		2	4		2	4	mA
				5	7		5	7		5	10	mA
				6	7		—	—		—	—	—
SR	Slew Rate	A _v = +1 T _A = 25°C, V _S = ±15V LF155/355 Series LF156/356 Series		5	7		5	7		2.5	6	V/μs
				10	12		10	12		10	12	V/μs
GBW	Gain Bandwidth Product	T _A = 25°C, V _S = ±15V LF155/355 Series LF156/356 Series		—	2.5		2.5	5		2.5	5	MHz
				4	5		4	5		4	5	MHz
t _S	Settling Time to 0.01%	T _A = 25°C, V _S = ±15V LF155 Series (Note 5) LF156 Series		4			4			4		μs
				1.5			1.5			1.5		μs
e _n	Input Noise Voltage Density	T _A = 25°C, V _S = ±15V f = 100Hz LF155 Series LF156 Series		25			25			25		nV/√Hz
				15			15			15		nV/√Hz
				20			20			20		nV/√Hz
i _n	Input Noise Current Density	T _A = 25°C, V _S = ±15V f = 100Hz f = 1000Hz		0.01			0.01			0.01		pA/√Hz
				0.01			0.01			0.01		pA/√Hz
C _{IN}	Input Capacitance		●	3		3			3		pF	

2

The ● denotes the specifications which apply over the full operating temperature range. The shaded electrical specifications indicate those parameters which have been improved or guaranteed test limits provided for the first time.

For MIL-STD components, please refer to LTC 883C data sheet for test listing and parameters.

Note 1: Unless otherwise specified, the absolute maximum negative input voltage is equal to the negative power supply voltage.

Note 2: Unless otherwise stated, these test conditions apply:

	LF155A/156A LF155/156	LF355A/356A	LF355/356
Supply Voltage, V _S	±15V ≤ V _S ≤ ±20V	±15V ≤ V _S ≤ ±18V	V _S = ±15V
T _A	-55°C ≤ T _A ≤ +125°C	0°C ≤ T _A ≤ +70°C	0°C ≤ T _A ≤ +70°C

and V_{OS}, I_B and I_{OS} are measured at V_{CM} = 0.

Note 3: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_J. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D. T_J = T_A + Θ_{JA} P_D where Θ_{JA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

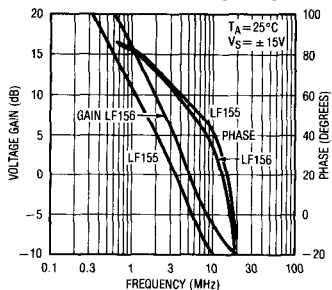
Note 4: The temperature coefficient of the adjusted input offset voltage changes only a small amount (0.5μV/°C typically) for each mV of adjustment from its original unadjusted value. Common-mode rejection and open loop voltage gain are also unaffected by offset adjustment.

Note 5: Settling time is defined here for a unity gain inverter connection using 2kΩ resistors. It is the time required for the error voltage (the voltage at the inverting input pin on the amplifier) to settle to within 0.01% of its final value from the time a 10V step input is applied to the inverter.

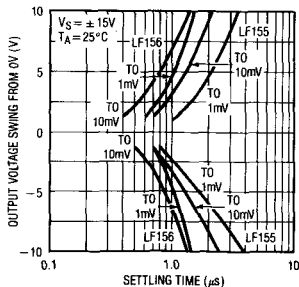
LF155A/355A/155/355 LF156A/356A/156/356

TYPICAL PERFORMANCE CHARACTERISTICS

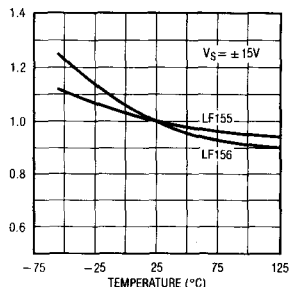
Gain, Phase vs Frequency



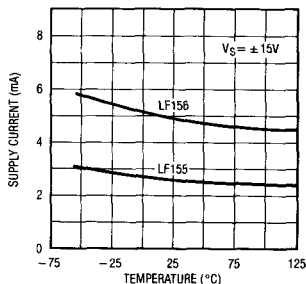
Inverter Settling Time



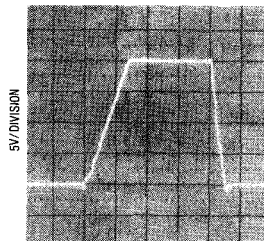
Normalized Slew Rate vs Temperature



Supply Current vs Temperature

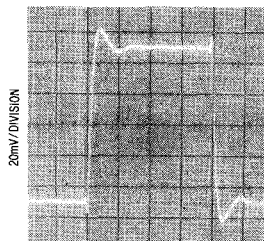


LF156 Large Signal Response



$A_v = +1$, $C_L = 100\text{pF}$, $1\mu\text{s}/\text{DIV}$

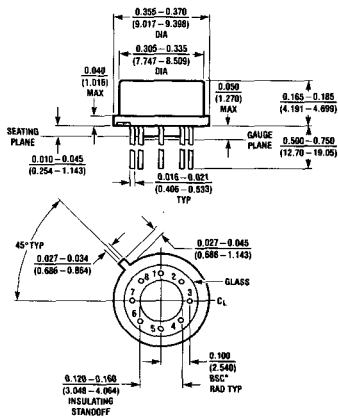
LF156 Small Signal Response



$A_v = +1$, $C_L = 100\text{pF}$, $0.2\mu\text{s}/\text{DIV}$

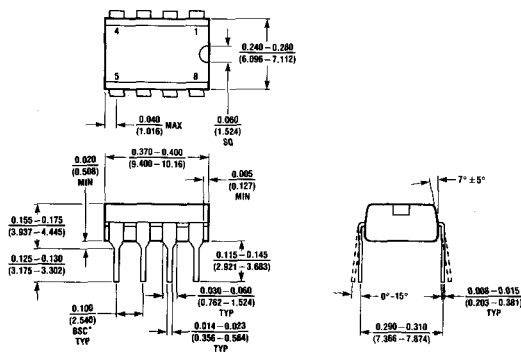
PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

H Package Metal Can



$T_{j\text{max}}$	$\theta_{j\text{a}}$	$\theta_{j\text{c}}$
150°C	150°C/W	45°C/W

N8 Package 8 Lead Plastic



*LEADS WITHIN 0.007 OF TRUE POSITION (TP) AT GAUGE PLANE

$T_{j\text{max}}$	$\theta_{j\text{a}}$
100°C	130°C/W

FEATURES

- Internally Trimmed Offset Voltage 1mV Max.
- Offset Voltage Drift $10\mu\text{V}/^\circ\text{C}$ Max.
- High Slew Rate $10\text{V}/\mu\text{s}$ Min.
- Wide Bandwidth 3.5MHz Min.
- Low Supply Current per Amplifier 1.8mA Typ.
- Low Input Bias Current 10pA Typ.
- Standard 8-Pin Configuration
- All Packages Available: Metal Can
Hermetic DIP
Plastic DIP

APPLICATIONS

- Sample and Hold Amplifiers
- Output Amplifier for Dual Current Output DACs
- High Speed Integrators
- Photocell Amplifiers
- High Input Impedance Instrumentation Amplifiers

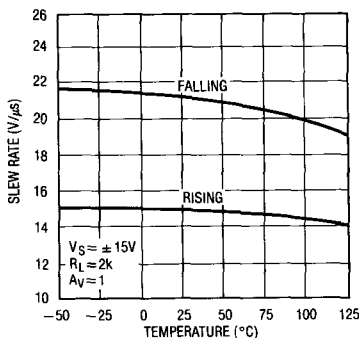
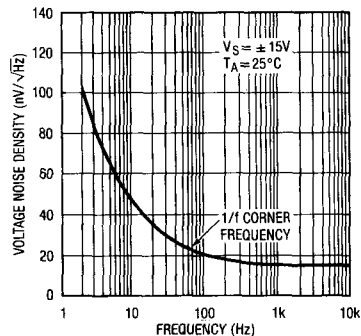
DESCRIPTION

Linear Technology's LF412A and OP-215 series of dual JFET input op amps feature several improvements compared to similar types from other manufacturers.

Both devices have lower input bias and offset currents over the entire temperature range, and are available in all standard 8-pin packages.

In addition, Linear's LF412A has lower voltage noise and higher voltage gain. Linear's OP-215 supply currents are nearly halved.

Please see the LT1057/LT1058 data sheet for applications requiring higher performance. The LT1057 is a pin compatible JFET input dual, the LT1058 is a JFET input quad op amp in the standard 14-pin DIP configuration.

2
Slew Rate

Voltage Noise Density vs Frequency


LF412A/OP-215

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	
LF412AM/AC, OP-215A/E	± 22V
LF412M/C, OP-215C/G	± 18V
Internal Power Dissipation	670mW
Operating Temperature Range	
LF412AM/M, OP-215A/C	-55°C to 125°C
LF412AC/C, OP-215E/G	0°C to 70°C
Differential Input Voltage	
LF412AM/AC, OP-215A/E	± 40V
LF412M/C, OP-215C/G	± 30V
Input Voltage (Note A)	
LF412AM/AC, OP-215A/E	± 20V
LF412M/C, OP-215C/G	± 16V
Output Short Circuit Duration	Indefinite
Storage Temperature Range	-65°C to 150°C
Lead Temperature (Soldering, 10 sec)	300°C

Note A: Maximum negative input voltage is equal to the negative supply voltage.

PACKAGE/ORDER INFORMATION

<p>TOP VIEW V+ OUTPUT A 1 -IN A 2 +IN A 3 V- (CASE) 4 H PACKAGE METAL CAN</p> <p>TOP VIEW OUTPUT A 1 -IN A 2 +IN A 3 V- 4 J8 PACKAGE HERMETIC DIP N8 PACKAGE PLASTIC DIP</p>	ORDER PART NUMBER																			
	<table border="0"> <tr> <td>LF412AMH</td> <td>OP-215AH</td> </tr> <tr> <td>LF412MH</td> <td>OP-215CH</td> </tr> <tr> <td>LF412ACH</td> <td>OP-215EH</td> </tr> <tr> <td>LF412CH</td> <td>OP-215GH</td> </tr> </table> <table border="0"> <tr> <td>LF412AMJ8</td> <td>OP-215AJ8</td> </tr> <tr> <td>LF412MJ8</td> <td>OP-215CJ8</td> </tr> <tr> <td>LF412ACJ8</td> <td>OP-215EJ8</td> </tr> <tr> <td>LF412CJ8</td> <td>OP-215GJ8</td> </tr> <tr> <td>LF412ACN8</td> <td>OP-215EN8</td> </tr> <tr> <td>LF412CN8</td> <td>OP-215GN8</td> </tr> </table>	LF412AMH	OP-215AH	LF412MH	OP-215CH	LF412ACH	OP-215EH	LF412CH	OP-215GH	LF412AMJ8	OP-215AJ8	LF412MJ8	OP-215CJ8	LF412ACJ8	OP-215EJ8	LF412CJ8	OP-215GJ8	LF412ACN8	OP-215EN8	LF412CN8
LF412AMH	OP-215AH																			
LF412MH	OP-215CH																			
LF412ACH	OP-215EH																			
LF412CH	OP-215GH																			
LF412AMJ8	OP-215AJ8																			
LF412MJ8	OP-215CJ8																			
LF412ACJ8	OP-215EJ8																			
LF412CJ8	OP-215GJ8																			
LF412ACN8	OP-215EN8																			
LF412CN8	OP-215GN8																			

ELECTRICAL CHARACTERISTICS

$V_S = \pm 20V$ for LF412A, $V_S = \pm 15V$ for all other grades.
 $V_{CM} = 0V$, $T_A = 25^\circ C$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	OP-215A/E			LF412AM/AC			LF412, OP-215C/G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage		-	0.2	1.0	-	0.3	1.0	-	0.5	3.0	mV
I_{OS}	Input Offset Current	$T_J = 25^\circ C$ (Note 1) Warmed-Up $V_S = \pm 15V$	-	6	50	-	6	50	-	10	100	pA
I_B	Input Bias Current	$T_J = 25^\circ C$ (Note 1) Warmed-Up $V_S = \pm 15V$	-	± 10	± 100	-	± 10	± 100	-	± 15	± 200	pA
			-	± 15	± 300	-	± 15	± 300	-	± 20	± 400	pA
R_{IN}	Input Resistance		-	10^{12}	-	-	10^{12}	-	-	10^{12}	-	Ω
A_{VOL}	Large Signal Voltage Gain	$R_L \geq 2k\Omega$, $V_O = \pm 10V$ $V_S = \pm 15V$	150	400	-	100	300	-	50	250	-	V/mV
V_O	Output Voltage Swing	$R_L = 10k\Omega$, $V_S = \pm 15V$ $R_L = 2k\Omega$, $V_S = \pm 15V$	± 12	± 13	-	± 12	± 13	-	± 12	± 13	-	V
			± 11	± 12.7	-	± 11	± 12.7	-	± 11	± 12.7	-	V
I_S	Supply Current		-	3.6	6.0	-	3.6	5.6	-	3.8	6.0	mA
SR	Slew Rate	$V_S = \pm 15V$	10	15	-	10	15	-	8	13	-	V/ μs
GBW	Gain Bandwidth Product	$V_S = \pm 15V$ (Note 2)	3.5	5.7	-	3.5	5.7	-	3.0	5.5	-	MHz
	Settling Time	to 0.01% to 0.10%	-	2.3	-	-	2.3	-	-	2.4	-	μs
			-	1.1	-	-	1.1	-	-	1.2	-	μs
	Input Voltage Range		± 11	+ 14.5 - 11.5	-	± 16	+ 19.5 - 16.5	-	± 11	+ 14.5 - 11.5	-	V
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm 16V$ $V_{CM} = \pm 11V$ $V_{CM} = \pm 10.5V$	-	73	100	-	80	100	-	-	-	dB
			-	80	100	-	-	-	-	72	100	dB
			-	-	-	-	-	-	-	88	100	dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 10V$ to $\pm 20V$ $V_S = \pm 10V$ to $\pm 18V$	-	-	-	80	100	-	-	-	-	dB
			-	86	100	-	-	-	-	80	100	dB
e_n	Input Noise Voltage Density	$f_o = 100Hz$ $f_o = 1000Hz$	-	20	-	-	20	-	-	20	-	nV/ \sqrt{Hz}
			-	15	-	-	15	-	-	15	-	nV/ \sqrt{Hz}
i_n	Input Noise Current Density	$f_o = 100Hz$ $f_o = 1000Hz$	-	0.01	-	-	0.01	-	-	0.01	-	pA/ \sqrt{Hz}
			-	0.01	-	-	0.01	-	-	0.01	-	pA/ \sqrt{Hz}
	Channel Separation	$f = 1Hz$ to $20kHz$	-	120	-	-	120	-	-	120	-	dB

ELECTRICAL CHARACTERISTICS $V_S = \pm 20V$ for LF412A, $V_S = \pm 15V$ for all other grades.
 $V_{CM} = 0V$, $-55^\circ C \leq T_A \leq 125^\circ C$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	OP-215A			LF412AM			LF412M, OP-215C			UNITS	
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
V_{OS}	Input Offset Voltage		●	—	0.5	2.0	—	0.7	2.0	—	1.0	5.0	mV
	Average Input Offset Voltage Drift		●	—	3	10	—	4	10	—	5	20	$\mu V/^\circ C$
I_{OS}	Input Offset Current	$T_J = 125^\circ C$ (Note 1)	●	—	0.8	8	—	0.8	8	—	1.0	12	nA
		$T_A = 125^\circ C$, Warmed-Up $V_S = \pm 15V$	●	—	1.2	14	—	1.2	14	—	1.5	22	nA
I_B	Input Bias Current	$T_J = 125^\circ C$ (Note 1)	●	—	± 1.5	± 10	—	± 1.5	± 10	—	± 1.8	± 15	nA
		$T_A = 125^\circ C$, Warmed-Up $V_S = \pm 15V$	●	—	± 2.2	± 18	—	± 2.2	± 18	—	± 2.7	± 28	nA
	Input Voltage Range	OP-215	●	± 10.3	$+14.5$ -11.5	—	—	—	—	± 10.3	$+14.5$ -11.5	—	V
		LF412	●	—	—	—	± 16	$+19.5$ -16.5	—	± 11	$+14.5$ -11.5	—	V
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm 16V$	●	—	—	—	80	100	—	—	—	—	dB
		$V_{CM} = \pm 11V$	●	—	—	—	—	—	—	70	100	—	dB
		$V_{CM} = \pm 10.3V$	●	82	100	—	—	—	—	80	100	—	dB
I_S	Supply Current		●	—	4.2	6.8	—	4.0	5.6	—	4.2	6.8	mA
PSRR	Power Supply Rejection Ratio	$V_S = \pm 10V$ to $\pm 20V$	●	—	—	—	80	100	—	—	—	—	dB
		$V_S = \pm 10V$ to $\pm 16V$	●	80	100	—	—	—	—	78	100	—	dB
A_{VOL}	Large Signal Voltage Gain	$R_L \geq 2k\Omega$, $V_O = \pm 10V$ $V_S = \pm 15V$	●	30	150	—	30	150	—	25	150	—	V/mV
V_O	Output Voltage Swing	$R_L \geq 10k\Omega$, $V_S = \pm 15V$	●	± 12	± 13	—	± 12	± 13	—	± 12	± 13	—	V

2

ELECTRICAL CHARACTERISTICS $V_S = \pm 20V$ for LF412A, $V_S = \pm 15V$ for all other grades.
 $V_{CM} = 0V$, $0^\circ C \leq T_A \leq 70^\circ C$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	OP-215E			LF412AC			LF412C, OP-215G			UNITS	
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
V_{OS}	Input Offset Voltage		●	—	0.4	1.65	—	0.5	1.45	—	0.7	3.9	mV
	Average Input Offset Voltage Drift		●	—	3	15	—	4	10	—	5	20	$\mu V/^\circ C$
I_{OS}	Input Offset Current	$T_J = 70^\circ C$ (Note 1)	●	—	0.06	0.45	—	0.06	0.45	—	0.08	0.65	nA
		$T_A = 70^\circ C$, Warmed-Up $V_S = \pm 15V$	●	—	0.08	0.8	—	0.08	0.8	—	0.10	1.2	nA
I_B	Input Bias Current	$T_J = 70^\circ C$ (Note 1)	●	—	± 0.12	± 0.7	—	± 0.12	± 0.7	—	± 0.14	± 0.9	nA
		$T_A = 70^\circ C$, Warmed-Up $V_S = \pm 15V$	●	—	± 0.16	± 1.4	—	± 0.16	± 1.4	—	± 0.19	± 1.8	nA
	Input Voltage Range	OP-215	●	± 10.3	$+14.5$ -11.5	—	—	—	—	± 10.3	$+14.5$ -11.5	—	V
		LF412	●	—	—	—	± 16	$+19.5$ -11.5	—	± 11	$+14.5$ -11.5	—	V
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm 16V$	●	—	—	—	80	100	—	—	—	—	dB
		$V_{CM} = \pm 11V$	●	—	—	—	—	—	—	70	100	—	dB
		$V_{CM} = \pm 10.3V$	●	80	100	—	—	—	—	76	100	—	dB
I_S	Supply Current		●	—	4.0	6.8	—	3.8	5.6	—	4.0	6.8	mA
PSRR	Power Supply Rejection Ratio	$V_S = \pm 10V$ to $\pm 20V$	●	—	—	—	80	100	—	—	—	—	dB
		$V_S = \pm 10V$ to $\pm 16V$	●	80	100	—	—	—	—	76	100	—	dB
A_{VOL}	Large Signal Voltage Gain	$R_L \geq 2k\Omega$, $V_O = \pm 10V$ $V_S = \pm 15V$	●	50	180	—	50	180	—	35	180	—	V/mV
V_O	Output Voltage Swing	$R_L \geq 10k\Omega$, $V_S = \pm 15V$	●	± 12	± 13	—	± 12	± 13	—	± 12	± 13	—	V

The ● denotes the specifications which apply over the full operating temperature range. The shaded electrical specifications indicate those parameters which have been improved or guaranteed test limits provided for the first time.

Note 1: Input bias and offset currents are specified for two different conditions. The T specification is with the junction at ambient temperature; the

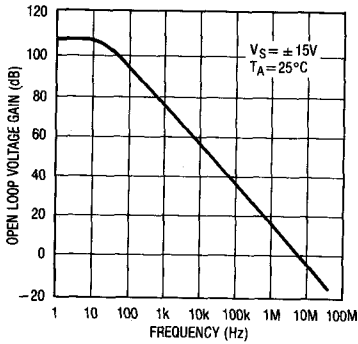
warmed-up specification is with the device operating in a warmed-up condition at the ambient temperature specified.

Note 2: Gain-bandwidth product is not tested. It is guaranteed by design and by inference from the slew rate measurement.

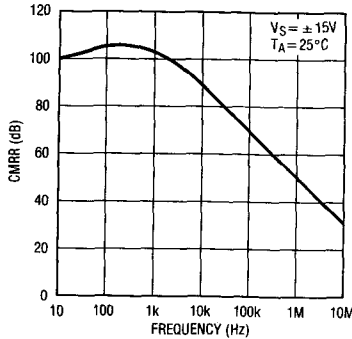
Note 3: The LF412A is 100% tested to this specification. All other grades are sample tested.

TYPICAL PERFORMANCE CHARACTERISTICS

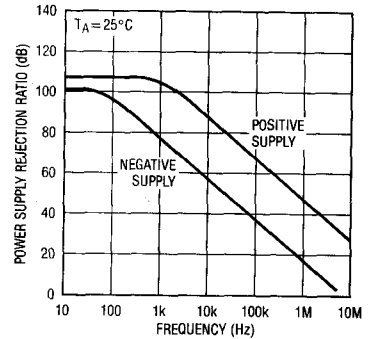
Open-Loop Frequency Response



Common-Mode Rejection Ratio vs Frequency



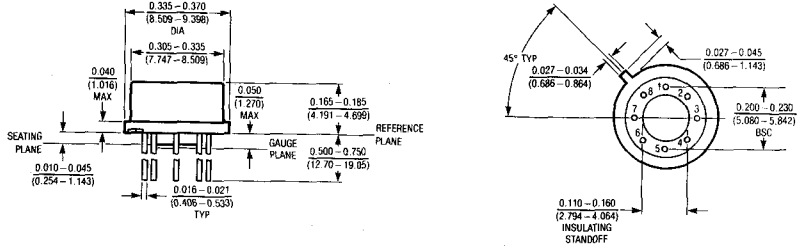
Power Supply Rejection Ratio vs Frequency



PACKAGE DESCRIPTIONS

Dimensions in inches (millimeters) unless otherwise noted.

H Package TO-5 Metal Can

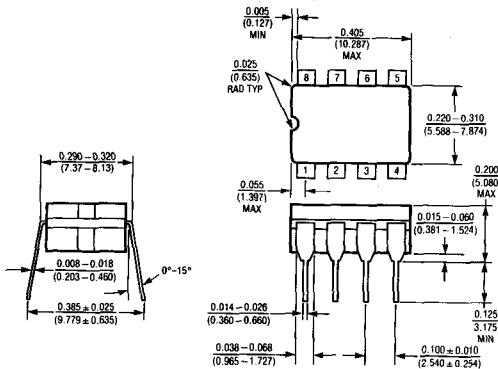


T_{jmax} 165°C	θ_{ja} 140°C/W	θ_{jc} 40°C/W
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NOTE: LEAD DIAMETER IS UNCONTROLLED BETWEEN THE REFERENCE PLANE AND SEATING PLANE.

H018A

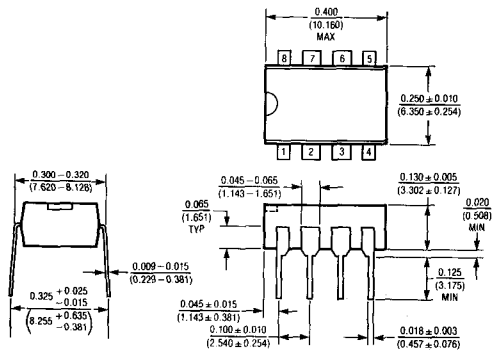
J Package 8 Lead Cerdip



T_{jmax} 155°C	θ_{ja} 100°C/W
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J018B

N Package 8 Lead Molded Dip



T_{jmax} 115°C	θ_{ja} 130°C/W
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N018A

FEATURES

- *Guaranteed* 2nA Max. Input Bias Current
- *Guaranteed* 600 μ A Max. Supply Current
- *Guaranteed* 0.5mV Max. Offset Voltage
- *Guaranteed* 5 μ V/ $^{\circ}$ C Max. Drift
- Wide Supply Voltage Range: ± 2 V to ± 20 V
- Interchangeable with Other Manufacturers' LH2108

APPLICATIONS

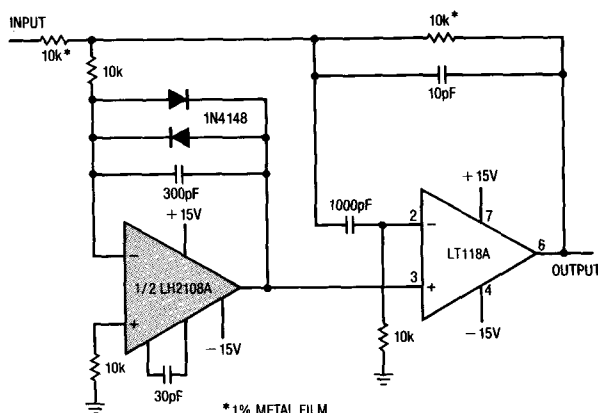
- Integrators
- Transducer Amplifiers
- Analog Memories
- Light Meters

DESCRIPTION

The LH2108A series of precision operational amplifiers is particularly well suited for high source impedance applications requiring low offset and bias currents, as well as low power dissipation. Unlike FET input amplifiers, the offset and bias currents of the LH2108A do not change significantly with temperature variations. Advanced design, processing and testing techniques make Linear's LH2108A a superior choice over previous devices.

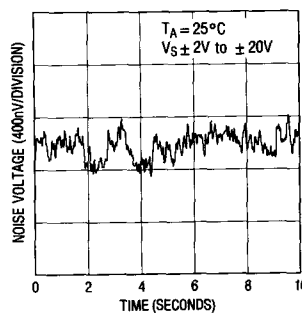
For higher performance dual amplifiers, see the LT1024, LT1002, and LT1013 data sheets.

Fast Precision Inverter



*1% METAL FILM
 FULL POWER BANDWIDTH = 2MHz
 SLEW RATE = 50V/ μ s

0.1Hz to 10Hz Noise

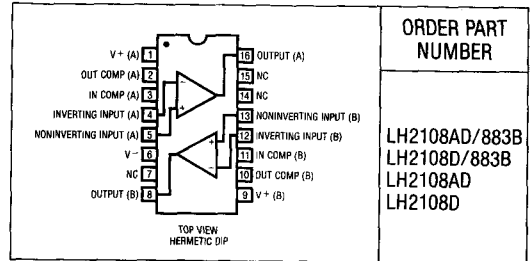


LH2108A

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	± 20V
Differential Input Current (Note 1)	± 10mA
Input Voltage (Note 2)	± 15V
Output Short Circuit Duration	Indefinite
Operating Temperature Range	-55°C to 125°C
Storage Temperature Range	-65°C to 150°C
Lead Temperature (Soldering, 10 sec.)	300°C

PACKAGE/ORDER INFORMATION



ELECTRICAL CHARACTERISTICS

± 5V ≤ V_S ≤ ± 20V and -55°C ≤ T_A ≤ 125°C unless otherwise noted.

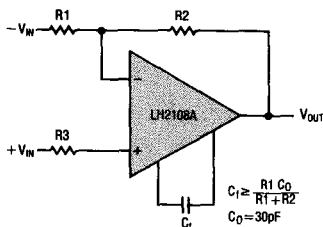
SYMBOL	PARAMETER	CONDITIONS	LH2108A			LH2108			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V _{OS}	Input Offset Voltage	T _A = 25°C	0.3	0.5	1.0	0.7	2.0	3.0	mV mV
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Temperature Coefficient of Input Offset Voltage		1.0	5.0		3.0	15		μV/°C
I _{OS}	Input Offset Current	T _A = 25°C	0.05	0.2	0.4	0.05	0.2	0.4	nA nA
$\frac{\Delta I_{OS}}{\Delta Temp}$	Average Temperature Coefficient of Input Offset Current		0.5	2.5		0.5	2.5		pA/°C
I _B	Input Bias Current	T _A = 25°C	0.5	2.0	3.0	0.5	2.0	3.0	nA nA
A _{VOL}	Large Signal Voltage Gain	T _A = 25°C, V _S = ± 15V, V _{OUT} = ± 10V, R _L ≥ 10kΩ	80	300	40	50	300	25	V/mV V/mV
CMRR	Common Mode Rejection Ratio		96	110		85	100		dB
PSRR	Power Supply Rejection Ratio		96	110		80	96		dB
	Input Voltage Range	V _S = ± 15V	± 13.5			± 13.5			V
V _{OUT}	Output Voltage Swing	V _S = ± 15V, R _L = 10kΩ	± 13	± 14		± 13	± 14		V
R _{IN}	Input Resistance	T _A = 25°C	30	70		30	70		MΩ
I _S	Supply Current	T _A = 25°C	0.3	0.6		0.3	0.6		nA mA
		T _A = 125°C	0.15	0.4		0.15	0.4		

Note 1: Differential input voltages greater than 1V will cause excessive current to flow through the input protection diodes unless current limiting resistance is used.

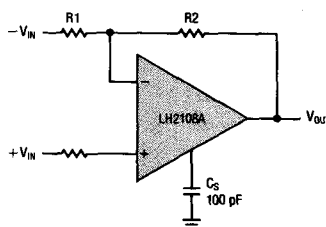
Note 2: For supply voltages less than ± 15V, the maximum input voltage is equal to the supply voltage. For typical performance, see LM108A data sheet.

COMPENSATION CIRCUITS

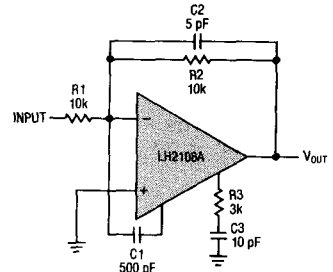
Standard Compensation Circuit



Alternate Frequency Compensation



Feedforward Compensation



FEATURES

- Guaranteed Operation at +1.2V
- Op Amp and Reference on Single Chip
- Low Supply Current 400 μ A
- Capable of Floating Mode Operation
- Low Reference Drift 20ppm/ $^{\circ}$ C
- Low Offset Voltage
- Output Swings to Within 15mV of Rails

DESCRIPTION

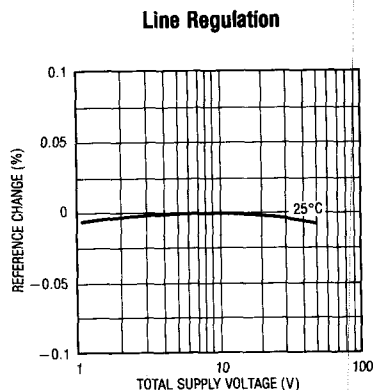
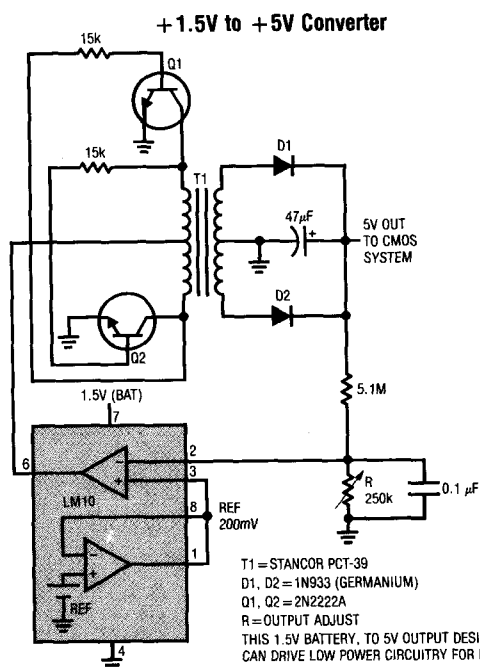
The LM10 combines a precision reference, a reference buffer amplifier and an independent, high quality op amp on a single chip. The device is capable of operation from a single supply as low as 1.1V, from dual supplies up to ± 20 V and typically draws 270 μ A supply current. Input voltage range for the op amp includes ground, while the unloaded output can swing to within 15mV of each rail. Further, the LM10 will deliver 20mA output current and still swing within ± 400 mV of the supply rails.

APPLICATIONS

- Remote Signal Conditioner/Transmitter
- Battery Operated Instruments
- Precision Current Regulators
- Precision Voltage Regulators
- Thermocouple Transmitter

With its low operating current and floating operation capability, the LM10 is ideal for two wire analog transmitter circuits where the processed signal is carried on the same line used for power. The LM10 is suggested for portable battery powered equipment and is fully specified for operation from a single 1.2V battery. Other applications include precision current and voltage regulators, operating from very low voltages to several hundred volts.

2



LM10

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage	
LM10/LM10B/LM10C	45V
LM10BL/LM10CL	7V
Differential Input Voltage (Note 1)	
LM10/LM10B/LM10C	±40V
LM10BL/LM10CL	±7V
Output Short Circuit Duration	
	Indefinite
Operating Temperature Range (Note 2)	
LM10	-55°C ≤ T _A ≤ 125°C
LM10B/LM10BL	-25°C ≤ T _A ≤ 85°C
LM10C/LM10CL	0°C ≤ T _A ≤ 70°C
Storage Temperature Range	
	-65°C ≤ T _A ≤ 150°C
Lead Temperature (Soldering, 10 sec.)	
	300°C

PACKAGE/ORDER INFORMATION

TOP VIEW REFERENCE FEEDBACK	ORDER PART NUMBER	
	<p>METAL CAN H PACKAGE</p>	LM10H
	LM10CH	LM10BLH
	LM10CLH	
TOP VIEW	ORDER PART NUMBER	
	<p>J8 HERMETIC PACKAGE NB PLASTIC DIP PACKAGE</p>	LM10CN8
	LM10CJ8	LM10CLJ8
	LM10J8	LM10BJ8
	LM10BLJ8	

OP AMP ELECTRICAL CHARACTERISTICS (Note 3)

SYMBOL	PARAMETER	CONDITIONS	LM10/LM10B			LM10C		UNITS
			MIN	TYP	MAX	MIN	MAX	
V _{OS}	Input Offset Voltage		●	0.3	2.0	0.5	4.0	mV
			●		3.0			
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Offset Voltage Drift		●	2.0		5.0		μV/°C
I _{OS}	Input Offset Current	(Note 4)	●	0.25	0.7	0.4	2.0	nA
			●		1.5			
$\frac{\Delta I_{OS}}{\Delta Temp}$	Offset Current Drift		●	2.0		5.0		pA/°C
I _B	Input Bias Current		●	10	20	12	30	nA
			●		30			
$\frac{\Delta I_B}{\Delta Temp}$	Bias Current Drift		●	60		90		pA/°C
A _{VOL}	Large Signal Voltage Gain	V _S = ±20V, I _{OUT} = 0, V _{OUT} = ±19.95V	●	120	400	80	400	V/mV
		V _S = ±20V, V _{OUT} = ±19.4V I _{OUT} = ±20mA I _{OUT} = ±15mA	●	80		50		V/mV
		V _S = ±20V, V _{OUT} = ±19.4V I _{OUT} = ±20mA I _{OUT} = ±15mA	●	50	130	25	130	V/mV
		V _S = ±20V, V _{OUT} = ±19.4V I _{OUT} = ±20mA I _{OUT} = ±15mA	●	20		15		V/mV
		V _S = ±0.6V, I _{OUT} = ±2mA V _{OUT} = ±0.4V, V _{CM} = -0.4V		1.5	3.0	1.0	3.0	V/mV
		V _S = ±0.65V, I _{OUT} = ±2mA V _{OUT} = ±0.3V, V _{CM} = -0.4V	●	0.5		0.75		V/mV
	Shunt Gain (Note 5)	0.1mA ≤ I _{OUT} ≤ 5mA, R _L = 1.1kΩ 1.2V ≤ V _{OUT} ≤ 40V 1.3V ≤ V _{OUT} ≤ 40V	●	14	33	10	33	V/mV
			●	6		6		V/mV
		0.1mA ≤ I _{OUT} ≤ 20mA, R _L = 250Ω 1.5V ≤ V _{OUT} ≤ 40V	●	8	25	6	25	V/mV
			●	4		4		V/mV

OP AMP ELECTRICAL CHARACTERISTICS (Note 3)

SYMBOL	PARAMETER	CONDITIONS	LM10/LM10B			LM10C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
CMRR	Common-Mode Rejection Ratio	$V_S = \pm 20V$ $-20V \leq V_{CM} \leq 19.15V$ $-20V \leq V_{CM} \leq 19V$	●	93	102		90	102	dB
			●	87			87		dB
PSRR	Power Supply Rejection Ratio	$-0.2V \geq V^- \geq -39V$ $V^+ = 1.0V$ $V^+ = 1.1V$	●	90	96		87	96	dB
			●	84			84		dB
			●	96	106		93	106	dB
R_{IN}	Input Resistance	(Note 6)	●	250	500		150	400	k Ω
			●	150			115		k Ω
I_S	Supply Current		●	270	400		300	500	μA
ΔI_S	Supply Current Change	$1.2V \leq V_S \leq 40V$ $1.3V \leq V_S \leq 40V$	●		500			570	μA
			●	15	75		15	75	μA
			●		75			75	μA

2

REFERENCE AMPLIFIER ELECTRICAL CHARACTERISTICS (Note 3)

SYMBOL	PARAMETER	CONDITIONS	LM10/LM10B			LM10C			UNITS	
			MIN	TYP	MAX	MIN	TYP	MAX		
V_{REF}	Feedback Sense Voltage	Voltage at Pin 1 with Pin 1 Connected to Pin 8	●	195	200	205	190	200	210	mV
$\frac{\Delta V_{REF}}{\Delta Temp}$	Reference Drift		●	0.002			0.003			% / $^{\circ}C$
	Feedback Current	Current into Pin 8	●	20	50	65	22	75	90	nA
	Line Regulation	$0 \leq I_{REF} \leq 1mA$, $V_{REF} = 200mV$ $1.2V \leq V_S \leq 40V$ $1.3V \leq V_S \leq 40V$	●	0.001 0.003			0.001 0.008			% / V
			●	0.001 0.006			0.001 0.01			% / V
	Load Regulation	$0 \leq I_{REF} \leq 1mA$ $V^+ - V_{REF} \geq 1.0V$ $V^+ - V_{REF} \geq 1.1V$	●	0.01 0.1			0.01 0.15			%
			●	0.01 0.15			0.01 0.20			%
	Reference Amplifier Gain	$0.2V \leq V_{REF} \leq 35V$	●	50	75		25	70		V/mV
			●	23			15			V/mV

OP AMP ELECTRICAL CHARACTERISTICS (Note 3)

SYMBOL	PARAMETER	CONDITIONS	LM108L			LM10CL			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage			0.3	2.0		0.5	4.0	mV
			●		3.0		5.0		mV
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Offset Voltage Drift		●	2.0		5.0			$\mu V/^\circ C$
I_{OS}	Input Offset Current	(Note 4)	●	0.1	0.7	0.2	2.0		nA
			●		1.5		3.0		nA
$\frac{\Delta I_{OS}}{\Delta Temp}$	Offset Current Drift		●	2.0		5.0			$pA/^\circ C$
I_B	Input Bias Current		●	10	20	12	30		nA
			●		30		40		nA
$\frac{\Delta I_B}{\Delta Temp}$	Bias Current Drift		●	60		90			$pA/^\circ C$
A_{VOL}	Large Signal Voltage Gain	$V_S = \pm 3.25V, I_{OUT} = 0, V_{OUT} = \pm 3.2V$	●	60	300	40	300		V/mV
			●	40		25			V/mV
		$V_S = \pm 3.25V, V_{OUT} = \pm 2.75V, I_{OUT} = \pm 10mA$	●	10	25	5	25		V/mV
			●	4		3		V/mV	
		$I_{OUT} = \pm 2mA, V_{CM} = -0.4V, V_S = \pm 0.6V, V_{OUT} = \pm 0.4V, V_S = \pm 0.65V, V_{OUT} = \pm 0.3V$	●	1.5	3.0	1.0	3.0		V/mV
			●	0.5		0.75		V/mV	
	Shunt Gain (Note 5)	$0.1mA \leq I_{OUT} \leq 10mA, R_L = 500\Omega, 1.5V \leq V^+ \leq 6.5V$	●	8	30	6	30		V/mV
			●	4		4		V/mV	
CMRR	Common-Mode Rejection Ratio	$V_S = \pm 3.25V, -3.25V \leq V_{CM} \leq 2.4V, -3.25V \leq V_{CM} \leq 2.25V$	●	89	102	80	102		dB
			●	83		74		dB	
PSRR	Power Supply Rejection Ratio	$-0.2V \geq V^- \geq -5.4V, V^+ = 1.0V, V^+ = 1.2V$	●	86	96	80	96		dB
			●	80		74		dB	
PSRR		$V^- = -0.2V, 1.0V \leq V^+ \leq 6.3V, 1.1V \leq V^+ \leq 6.3V$	●	94	106	80	106		dB
			●	88		74		dB	
R_{IN}	Input Resistance	(Note 6)	●	250	500	150	400		k Ω
			●	150		115		k Ω	
I_S	Supply Current		●	260	400	280	500		μA
			●		500		570		μA

REFERENCE AMPLIFIER ELECTRICAL CHARACTERISTICS (Note 3)

SYMBOL	PARAMETER	CONDITIONS	LM10BL			LM10CL			UNITS	
			MIN	TYP	MAX	MIN	TYP	MAX		
V_{REF}	Feedback Sense Voltage	Voltage at Pin 1 with Pin 1 Connected to Pin 8	●	195 194	200 200	205 206	190 189	200 200	210 211	mV mV
$\frac{\Delta V_{REF}}{\Delta Temp}$	Reference Drift		●	0.002			0.003			%/°C
	Feedback Current	Current into Pin 8	●	20	50 65		22	75 90		nA nA
	Line Regulation	$0 \leq I_{REF} \leq 0.5mA$, $V_{REF} = 200mV$ $1.2V \leq V_S \leq 6.5V$ $1.3V \leq V_S \leq 6.5V$	●	0.001 0.01 0.001 0.02			0.001 0.02 0.001 0.03			%/V %/V
	Load Regulation	$0 \leq I_{REF} \leq 0.5mA$ $V^+ - V_{REF} \geq 1.0V$ $V^+ - V_{REF} \geq 1.1V$	●	0.01 0.1 0.01 0.15			0.01 0.15 0.01 0.20			% %
	Reference Amplifier Gain	$0.2V \leq V_{REF} \leq 5.5V$	●	30 20	70		20 15	70		V/mV V/mV

The ● denotes the specifications which apply over full operating temperature range.

Note 1: The input voltage can exceed the supply voltages as long as the voltage from the input to any other terminal does not exceed the maximum differential voltage, and the maximum junction temperature is not exceeded due to the excess power dissipation that occurs when the input voltage is less than the negative supply voltage.

Note 2: The maximum operating junction temperatures are: 150°C for the LM10; 100°C for the LM10B and LM10BL; and 85°C for the LM10C and LM10CL. Package derating factors will be found on the back page of this data sheet.

Note 3: These specifications apply for the following conditions unless otherwise noted:

	at 25°C	over temperature
(a)	$V^- \leq V_{CM} \leq V^+ - 0.85V$	$V^- \leq V_{CM} \leq V^+ - 1.0V$
(b)	$1.2V \leq V_S \leq V_{MAX}$	$1.3V \leq V_S \leq V_{MAX}$

$V_{REF} = 0.2V$ and $0 \leq I_{REF} \leq 1.0mA$ where $V_{MAX} = 40V$ for the LM10, LM10B and LM10C and $V_{MAX} = 6.5V$ for the LM10BL and LM10CL. The specifications do not include errors due to thermal gradients ($\tau_1 \approx 20ms$), die heating ($\tau_2 \approx 0.2$ sec) or package heating.

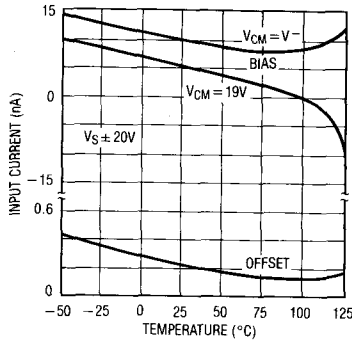
Note 4: For $T_J > 90^\circ C$, I_{OS} may exceed 1.5nA when $V_{CM} = V^-$. When the common-mode input voltage is within 100mV of the negative supply and $T_J = 125^\circ C$, the offset current will be less than 5nA.

Note 5: Shunt gain defines the operation in floating applications when the output is connected to the V^+ terminal and input common-mode is referred to V^- (see typical applications). The effects of larger output voltage swing with higher load resistance can be accounted for by adding the positive supply rejection error.

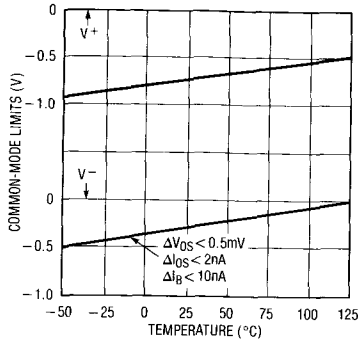
Note 6: Guaranteed by design.

TYPICAL PERFORMANCE CHARACTERISTICS (Op Amp)

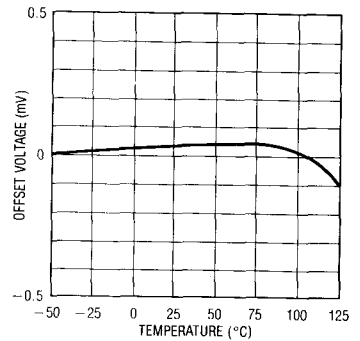
Input Current



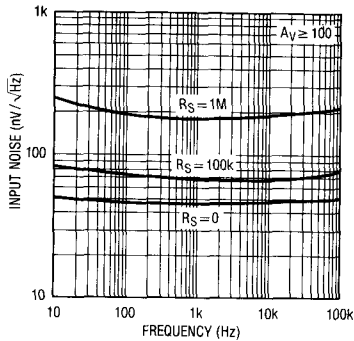
Common-Mode Limits



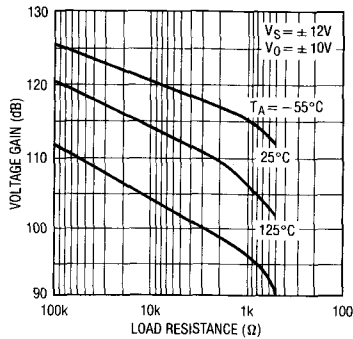
Offset Voltage Drift



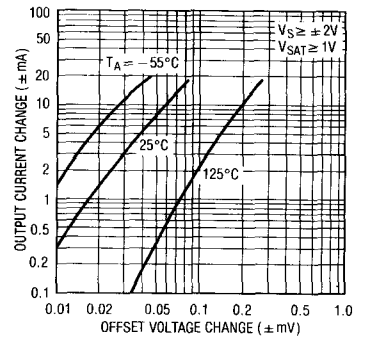
Input Noise Voltage



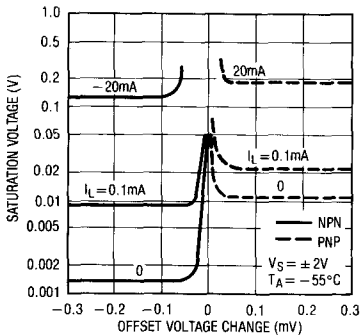
DC Voltage Gain



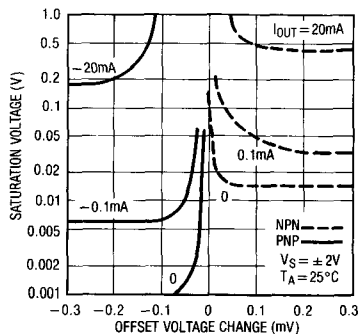
Transconductance



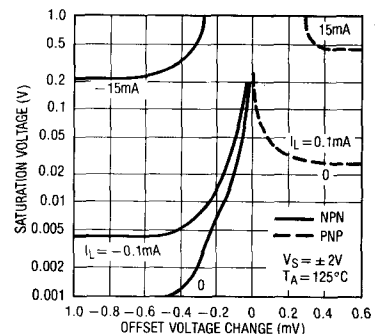
Output Saturation Characteristics



Output Saturation Characteristics



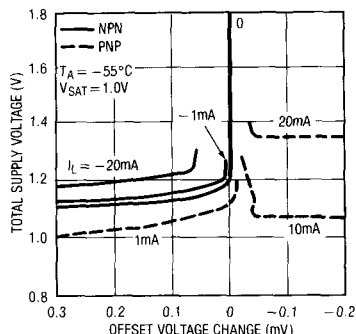
Output Saturation Characteristics



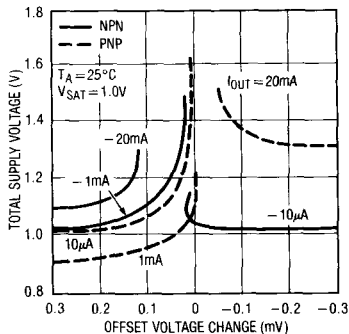
TYPICAL PERFORMANCE CHARACTERISTICS (Op Amp)

2

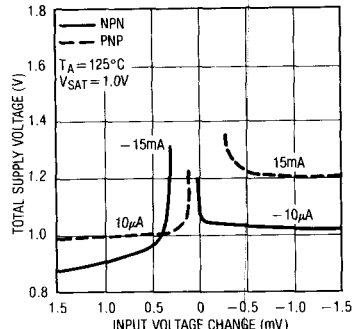
Minimum Supply Voltage



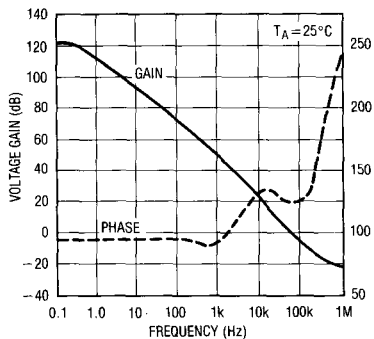
Minimum Supply Voltage



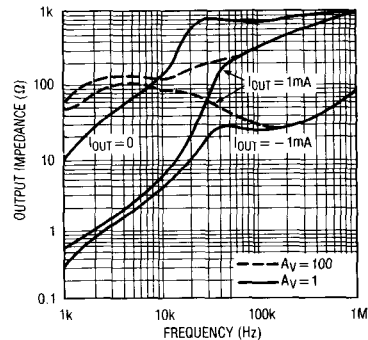
Minimum Supply Voltage



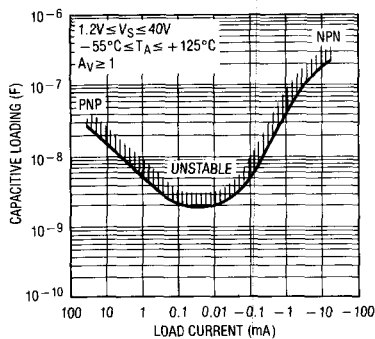
Frequency Response



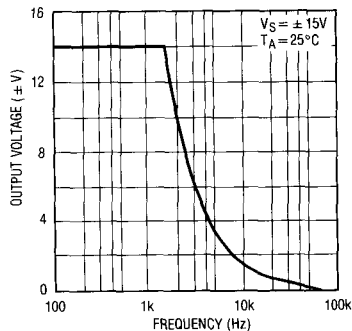
Output Impedance



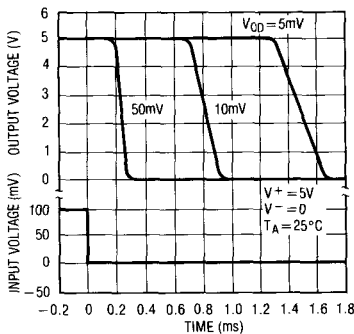
Typical Stability Range



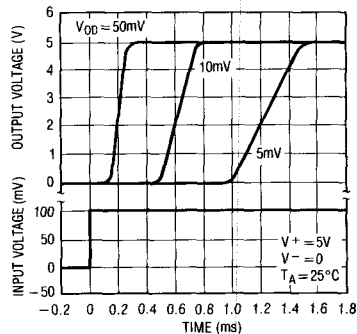
Large Signal Response



Comparator Response Time for Various Input Overdrives

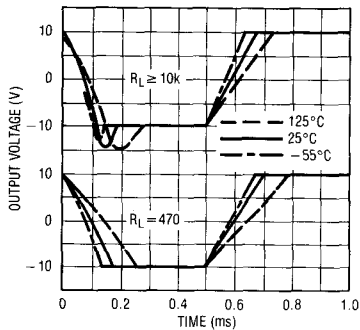


Comparator Response Time for Various Input Overdrives

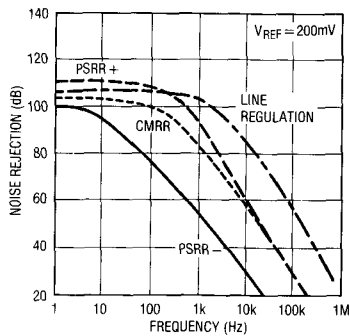


TYPICAL PERFORMANCE CHARACTERISTICS

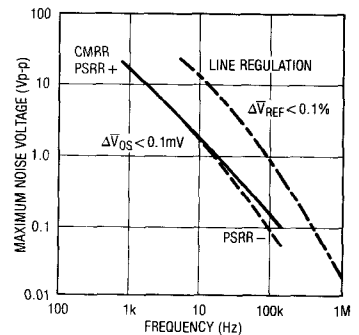
Follower Pulse Response



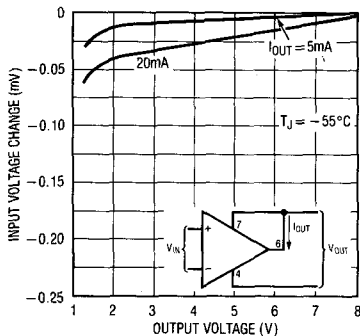
Noise Rejection



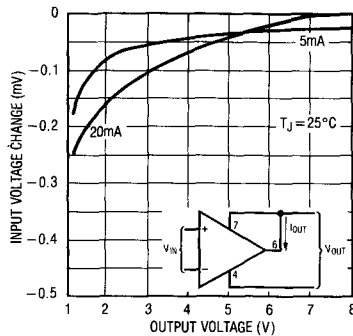
Rejection Slew Limiting



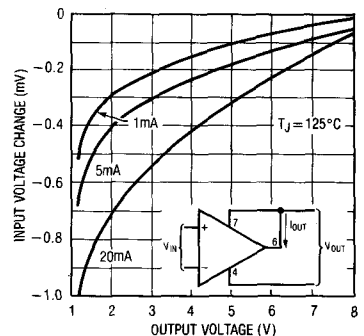
Shunt Gain



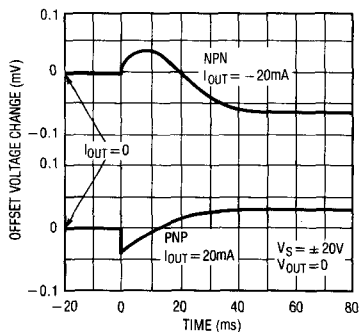
Shunt Gain



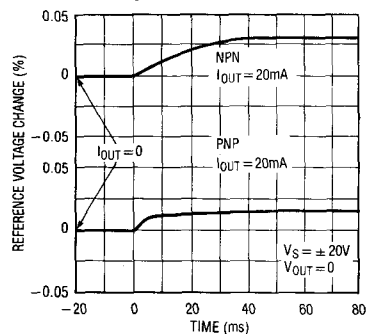
Shunt Gain



Thermal Gradient Feedback

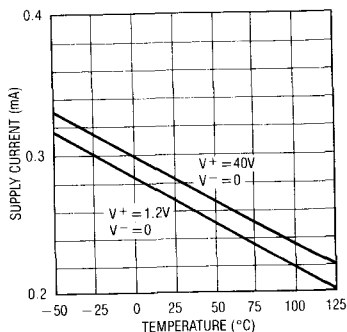


Change in Reference Op Amp Loading

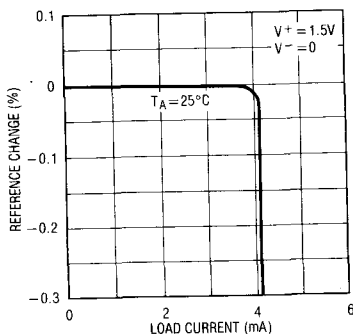


TYPICAL PERFORMANCE CHARACTERISTICS (Reference)

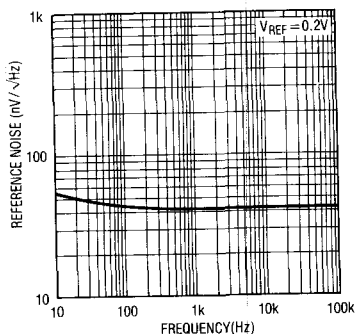
Supply Current



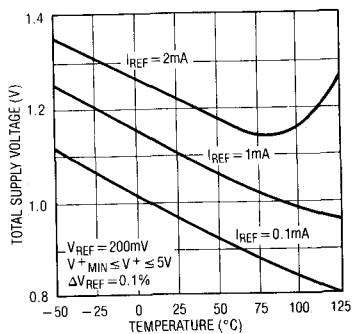
Load Regulation



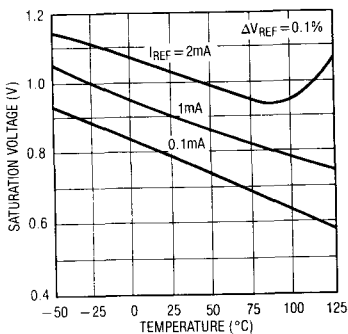
Reference Noise Voltage



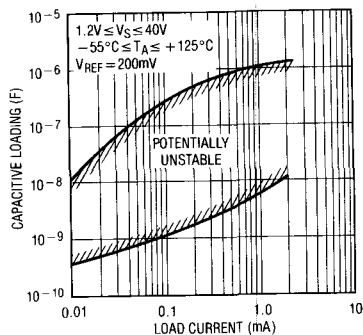
Minimum Supply Voltage



Output Saturation

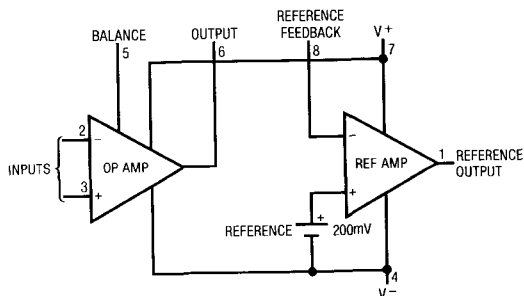


Typical Stability Range



2

BLOCK DIAGRAM



LM10

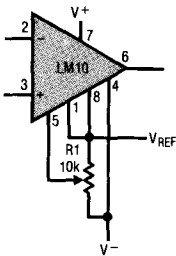
APPLICATION HINTS

With heavy amplifier loading to V^- , resistance drops in the V^- lead can adversely affect reference regulation.

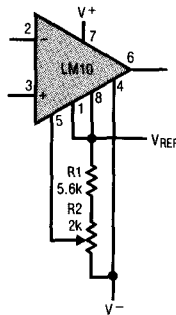
Lead resistance can approach 1Ω . Therefore, the common to the reference circuitry should be connected as close as possible to the package.

TYPICAL APPLICATIONS

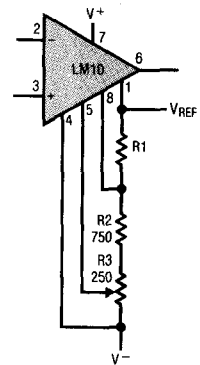
Standard Offset Adjustment



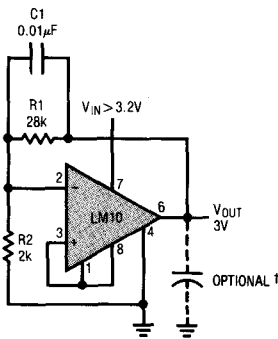
Limited Range Offset Adjustment



Limited Range Offset Adjustment with Boosted Reference

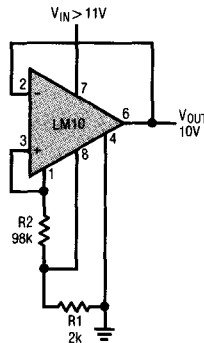


Low Voltage Regulator

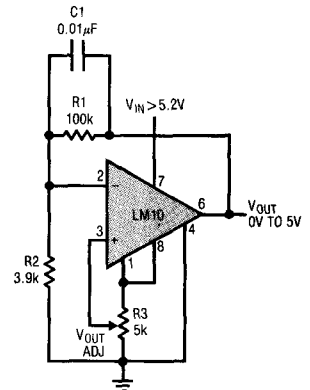


† USE ELECTROLYTIC OUTPUT CAPACITORS

Best Regulation

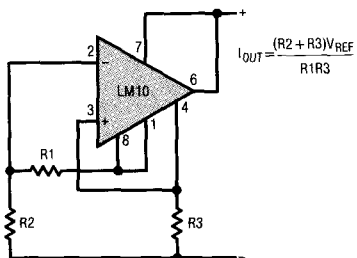


0V to 5V Regulator

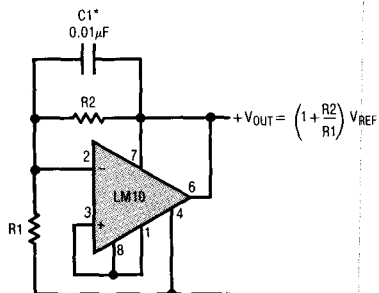


TYPICAL APPLICATIONS

Two-Terminal Current Regulator



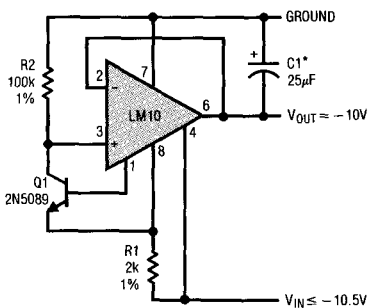
Shunt Regulator



*REQUIRED FOR CAPACITIVE LOADING

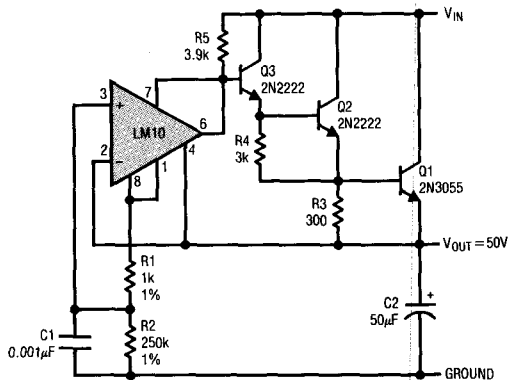
2

Negative Regulator



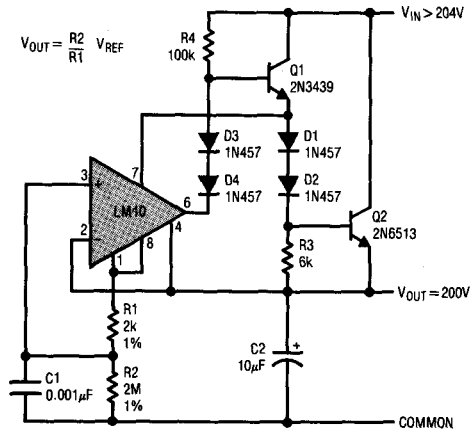
*ELECTROLYTIC

Floating Regulator

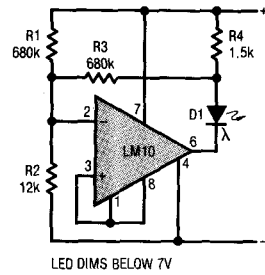


TYPICAL APPLICATIONS

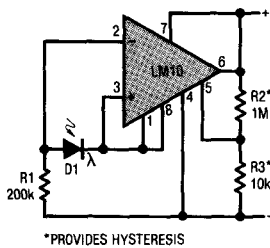
High Voltage Regulator



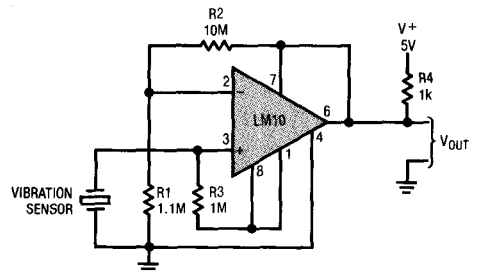
6V Battery-Level Indicator



Light Level Sensor

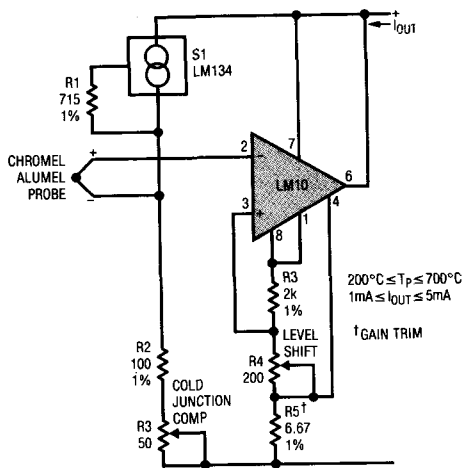


Transducer Amplifier

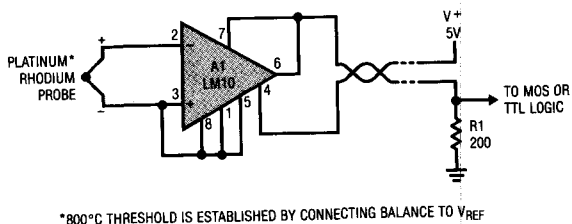


TYPICAL APPLICATIONS

Thermocouple Transmitter

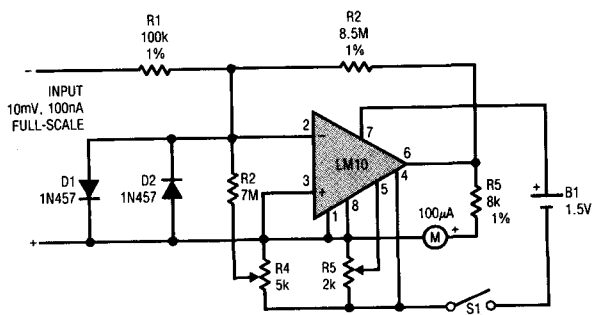


Flame Detector

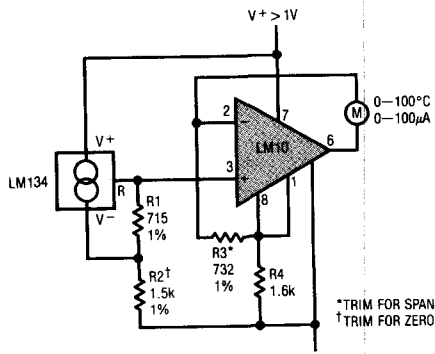


2

Meter Amplifier

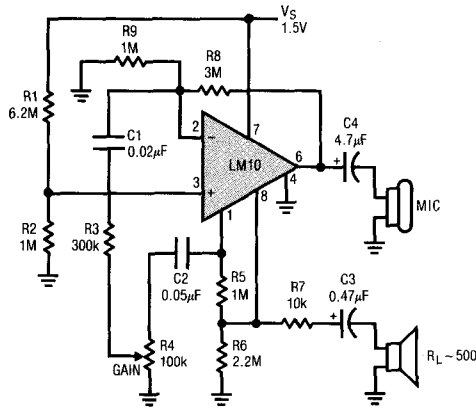


Thermometer

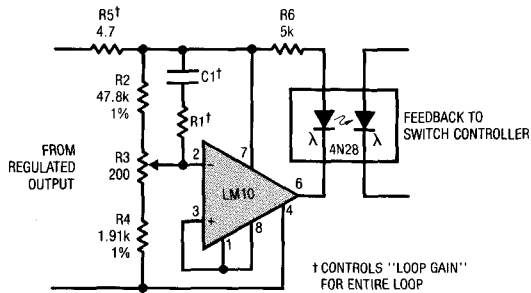


TYPICAL APPLICATIONS

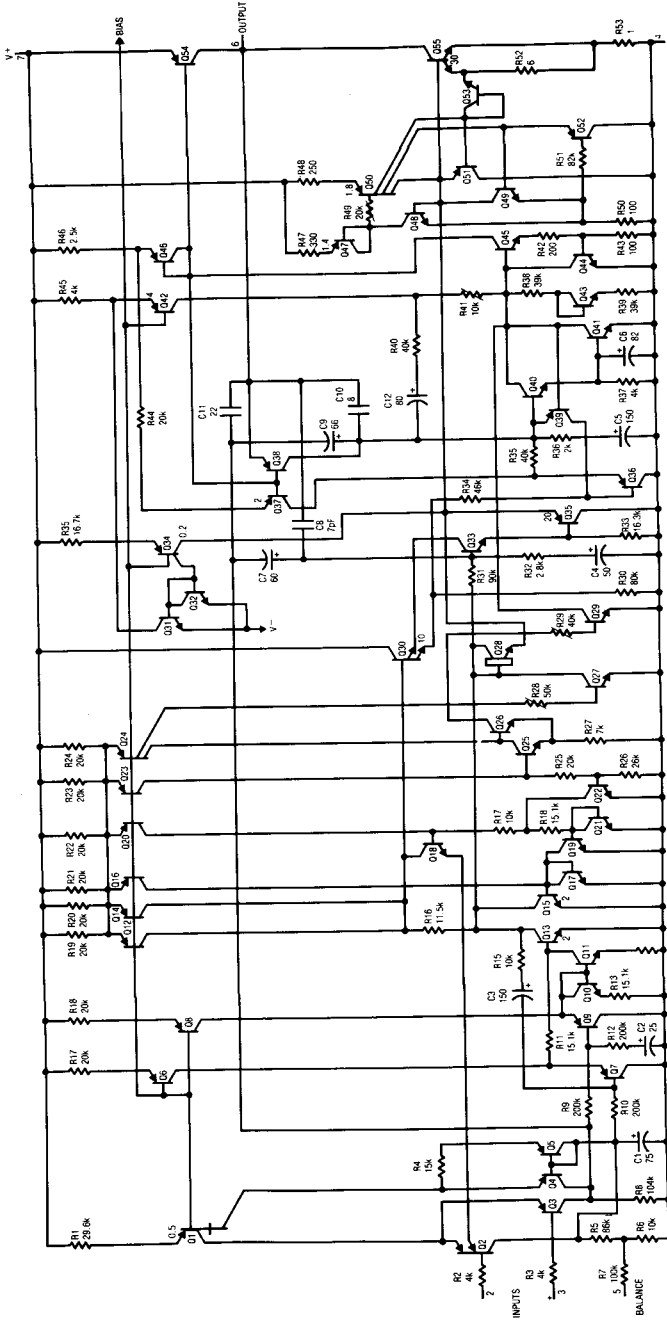
Microphone Amplifier
 $A_V \approx 1k$



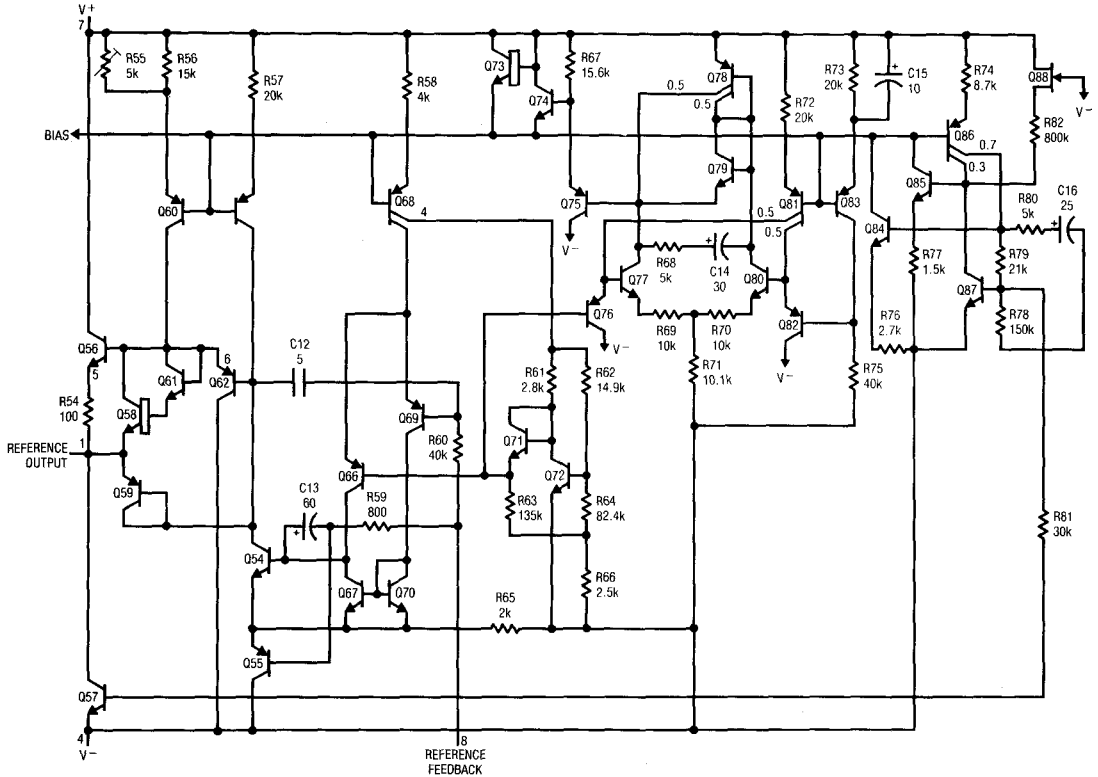
Isolated Voltage Sensor
for Switching Regulators



OP AMP SCHEMATIC DIAGRAM

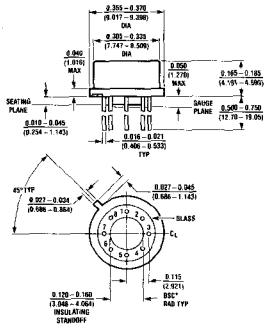


REFERENCE AND INTERNAL REGULATOR SCHEMATIC DIAGRAM



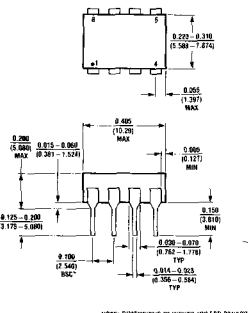
PACKAGE DESCRIPTION

H Package
Metal Can



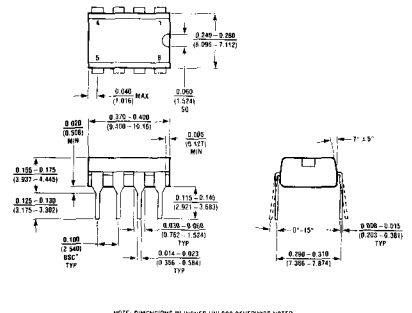
T_{jmax}	θ_{ja}	θ_{jc}
150°C	150°C/W	45°C/W

J8 Package
8 Lead Hermetic Dip



T_{jmax}	θ_{ja}
150°C	100°C/W

N8 Package
8 Lead Plastic



T_{jmax}	θ_{ja}
100°C	130°C/W

FEATURES

- 30 Volt Differential Input Range
- 75 nA Input Bias Current
- Wide Common Mode Voltage Range

APPLICATIONS

- Signal Conditioning Amplifiers
- Voltage Followers
- Comparators

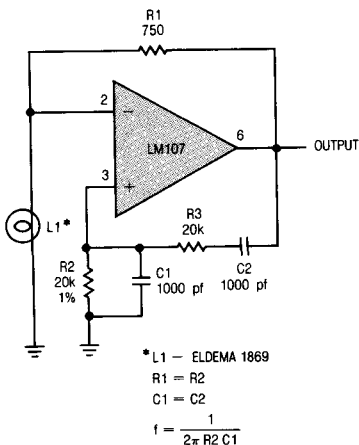
DESCRIPTION

The LM101A and LM107 are general purpose operational amplifiers, featuring low bias current and the ability to operate with high input differential voltages up to 30 Volts. Unlike many FET input amplifiers, the output of the LM101A/107 does not reverse if the common mode range is exceeded, making them particularly useful in comparator and oscillator circuits.

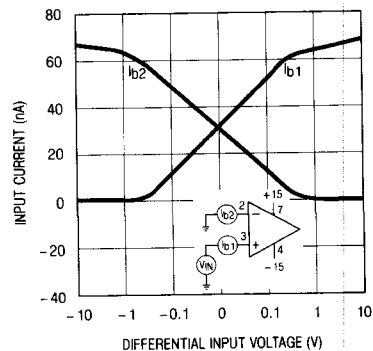
The LM101A uses external compensation, allowing the frequency response and slew rate to be optimized for the application. The LM107 is identical to the LM101A with the exception that the compensation capacitor is internal. Linear's LM101A and LM107 include improved design and processing techniques resulting in superior long term stability and reliability over previous devices. The curve of bias current versus differential input voltage indicates that a minimal change in input current occurs over a wide range of input signal, which is important in many applications.

2

Wein Bridge Sine Wave Oscillator



Bias Current vs Differential Input Voltage



LM101A/LM301A LM107/LM307

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	
LM101A/LM107	± 22 Volts
LM301A/LM307	± 18 Volts
Differential Input Voltage	± 30 Volts
Input Voltage, Note 2	± 15 Volts
Output Short Circuit Duration, Note 3	Indefinite
Operating Temperature Range	
LM101A/LM107	-55°C to 125°C
LM301A/LM307	0°C to 70°C
Maximum Junction Temperature	
LM101A/LM107	150°C
LM301A/LM307	100°C
Storage Temperature Range	
All Devices	-65°C to 150°C
Lead Temperature (Soldering, 10 sec.)	300°C

PACKAGE/ORDER INFORMATION

<p>METAL CAN H PACKAGE * PINS 1, 5, 8 NO CONNECTION ON LM107/307</p>	ORDER PART NUMBER
	LM101AH LM301AH LM107H LM307H
<p>J8 PACKAGE HERMETIC DIP * PINS 1, 5, 8 NO CONNECTION ON LM107/307</p>	LM101AJ8 LM301AJ8 LM107J8 LM307J8

ELECTRICAL CHARACTERISTICS (Note 1)

SYMBOL	PARAMETER	CONDITIONS	LM101A/LM107		LM301A/LM307		UNITS		
			MIN	TYP	MAX	MIN		TYP	MAX
V_{OS}	Input Offset Voltage	$R_S \leq 50K\Omega, T_A = 25^\circ C$ $R_S \leq 50K\Omega$	●	0.7	2.0	2.0	7.5	mV	
					3.0	10			mV
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Temperature Coefficient of Input Offset Voltage	$R_S \leq 50K\Omega$	●	3.0	15	6.0	30	$\mu V/^\circ C$	
I_{OS}	Input Offset Current	$T_A = 25^\circ C$	●	1.5	10	3.0	50	nA	
					20	70			nA
$\frac{\Delta I_{OS}}{\Delta Temp}$	Average Temperature Coefficient of Input Offset Current	$25^\circ C \leq T_A \leq T_{MAX}$ $T_{MIN} \leq T_A \leq 25^\circ C$		0.01	0.1	0.01	0.3	nA/°C	
I_B	Input Bias Current	$T_A = 25^\circ C$	●	30	75	70	250	nA	
					100	300			nA
A_{VOL}	Large Signal Voltage Gain	$T_A = 25^\circ C, V_S = \pm 15V, V_{OUT} = \pm 10V, R_L \geq 2K\Omega$ $V_S = \pm 15V, V_{OUT} = \pm 10V, R_L \geq 2K\Omega$	●	50	160	25	160	V/mV	
				25		15		V/mV	
CMRR	Common Mode Rejection Ratio	$R_S \leq 50K\Omega$	●	80	96	70	90	dB	
PSRR	Power Supply Rejection Ratio	$R_S \leq 50K\Omega$	●	80	96	70	96	dB	
			●	Input Voltage Range	$V_S = \pm 20V$	± 15			V
							●	$V_S = \pm 15V$	+ 15
		- 13	± 12	- 13	V				
V_{OUT}	Output Voltage Swing	$V_S = \pm 15V, R_L = 10K\Omega$ $R_L = 2K\Omega$	●	± 12	± 14	± 12	± 14	V	
			●	± 10	± 13	± 10	± 13	V	
R_{IN}	Input Resistance	$T_A = 25^\circ C$		1.5	4.0	0.5	2.0	MΩ	
I_S	Supply Current	$T_A = 25^\circ C, V_S = \pm 20V$ $T_A = 125^\circ C, V_S = \pm 20V$	●	1.8	3.0	1.8	3.0	mA	
				1.2	2.5			mA	

The ● denotes the specifications which apply over the full operating temperature range.

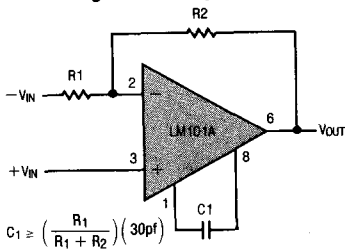
Note 1: Unless otherwise noted; all measurements are made with unity gain compensation ($C_1 = 30$ pf for the LM101A/301A); these specifications apply for $\pm 5V \leq V_S \leq \pm 20V$ for the LM101A/LM107; and $\pm 5V \leq V_S \leq \pm 15V$ for the LM301A/LM307.

Note 2: For supply voltages less than ± 15 Volts, the maximum input voltage is equal to the supply voltage.

Note 3: The output may be shorted to ground or either power supply indefinitely, provided the case temperature is below 125°C for the LM101A/107 and below 70°C for the LM301A/307.

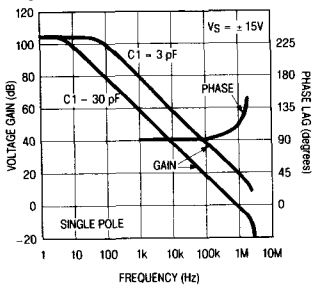
TYPICAL PERFORMANCE CHARACTERISTICS (LM101A)

Single Pole Compensation

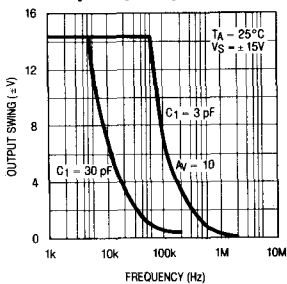


$C_1 = 30\text{pF}$ for unity gain stability. At gains above 1 frequency response can be maximized by decreasing C_1 .

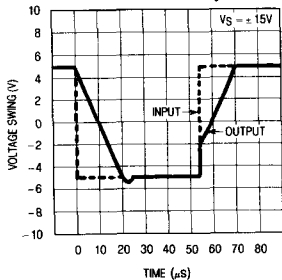
Open Loop Frequency Response



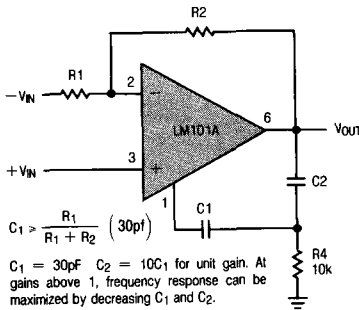
Single Pole Large Signal Frequency Response



Single Pole Voltage Follower Pulse Response

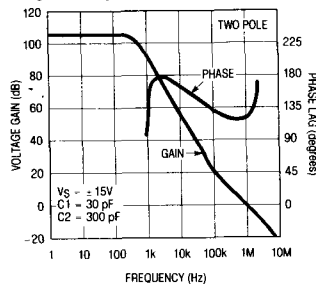


Two Pole Compensation

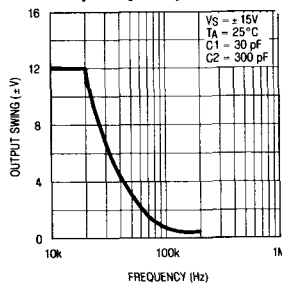


$C_1 = 30\text{pF}$ $C_2 = 10C_1$ for unit gain. At gains above 1, frequency response can be maximized by decreasing C_1 and C_2 .

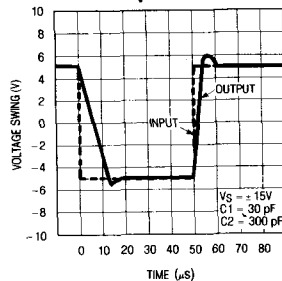
Open Loop Frequency Response



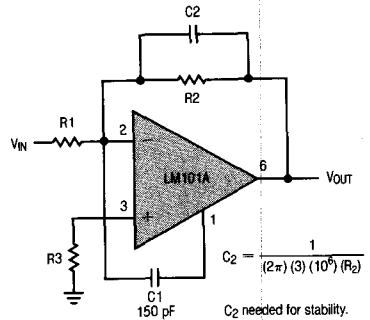
2 Pole Large Signal Frequency Response



2 Pole Voltage Follower Pulse Response

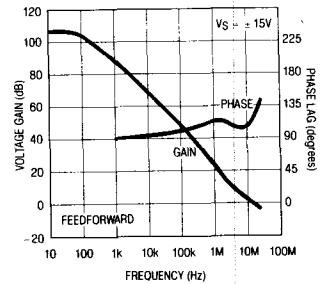


Feedforward Compensation

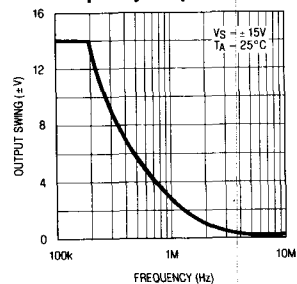


$C_2 = \frac{1}{(2\pi)(3)(10^6)(R_2)}$
 C_2 needed for stability.

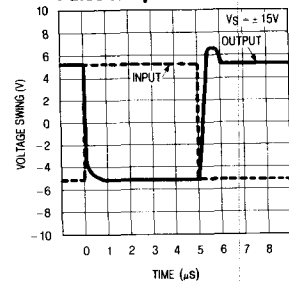
Open Loop Frequency Response



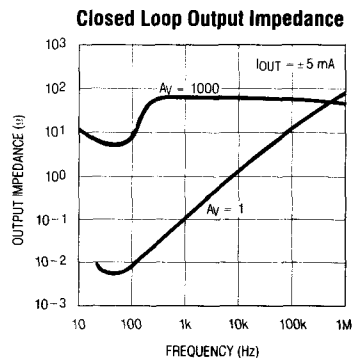
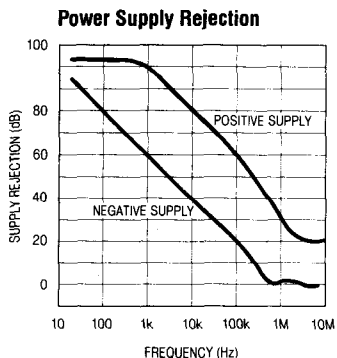
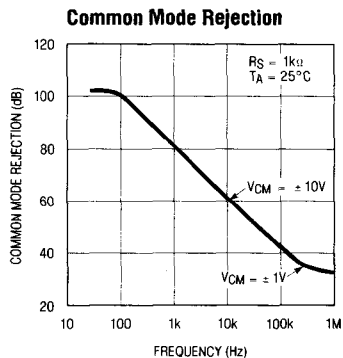
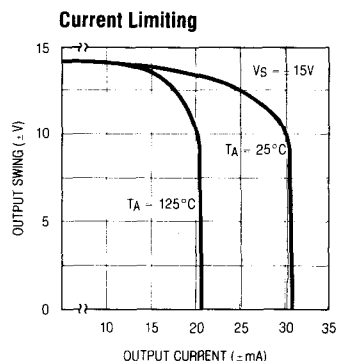
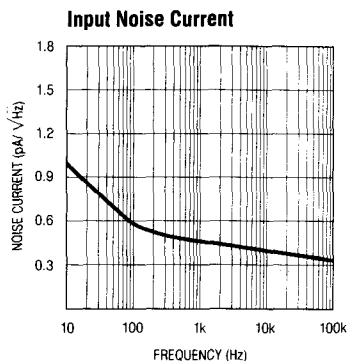
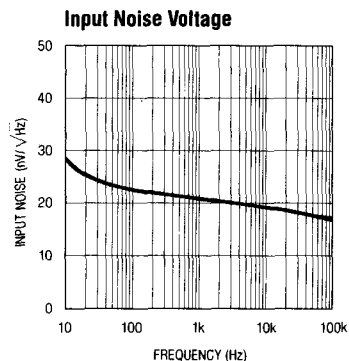
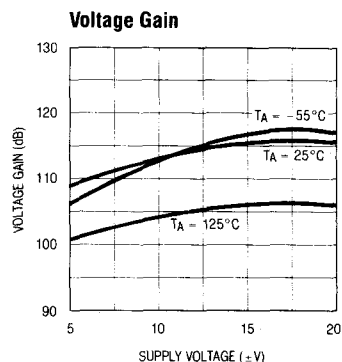
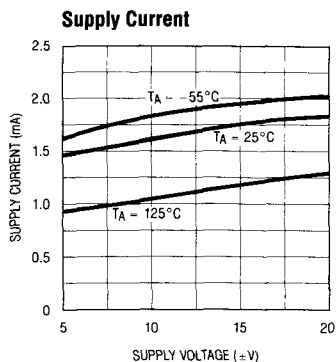
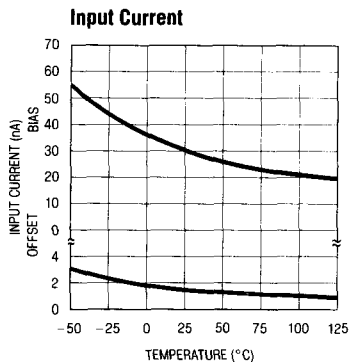
Feedforward Large Signal Frequency Response



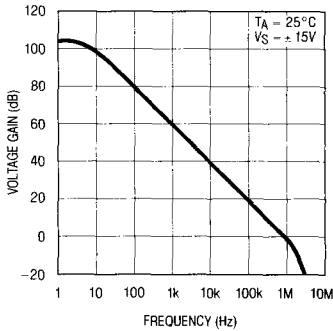
Feedforward Inverter Pulse Response



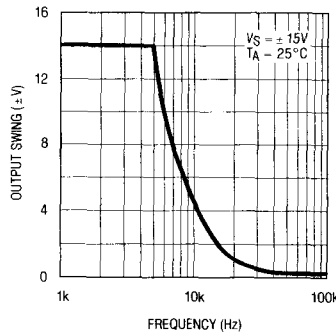
TYPICAL PERFORMANCE CHARACTERISTICS (LM101A/LM107)



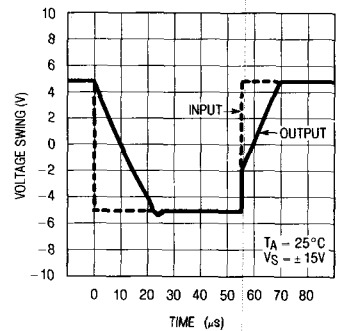
LM107
Open Loop Frequency Response



LM107
Large Signal Frequency Response

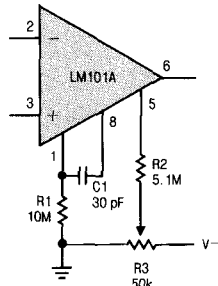


LM107
Voltage Follower Pulse Response

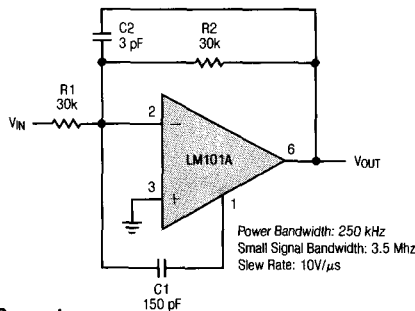


TYPICAL APPLICATIONS

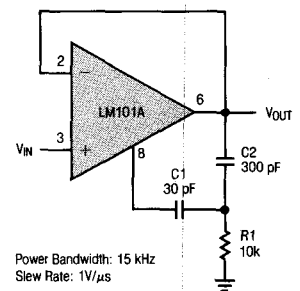
Standard Compensation and Offset Balancing Circuit



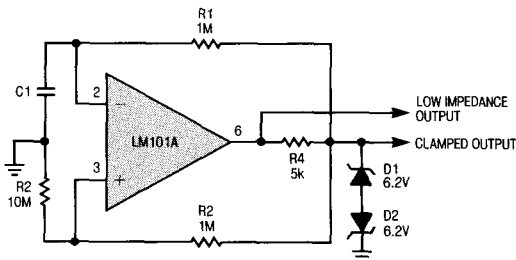
Fast Summing Amplifier



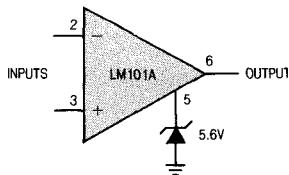
Fast Voltage Follower



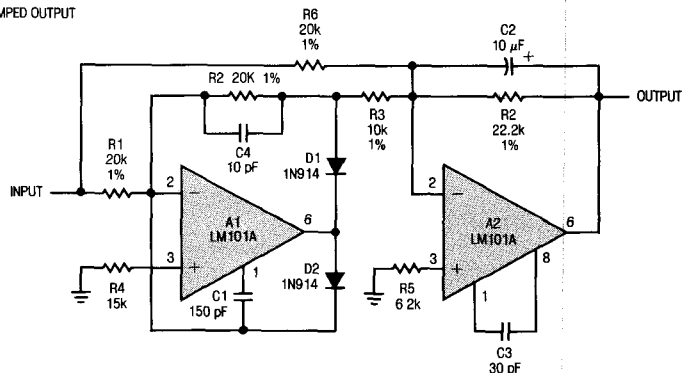
Low Frequency Square Wave Generator



Voltage Comparator with Clamp

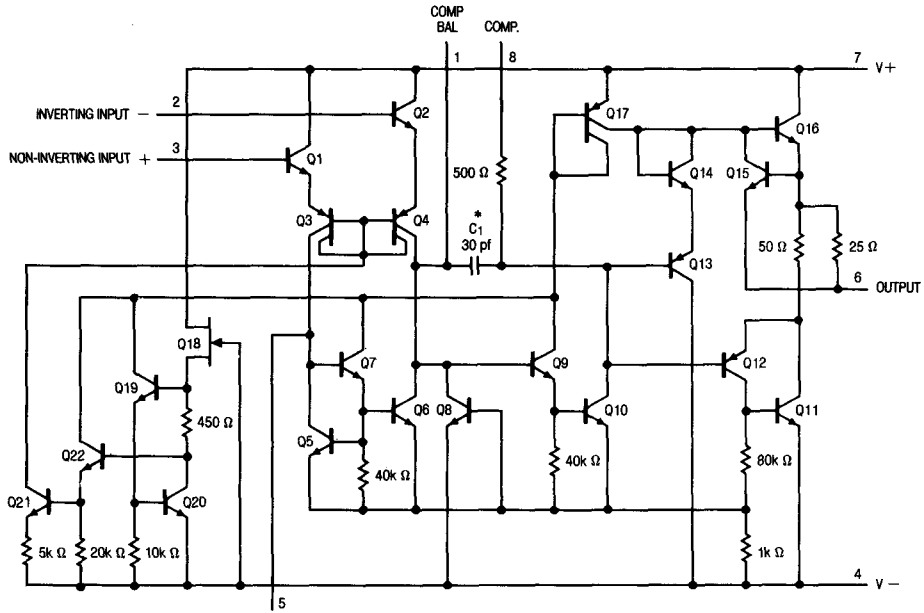


Precision Rectifier



LM101A/LM301A LM107/LM307

SCHEMATIC DIAGRAM

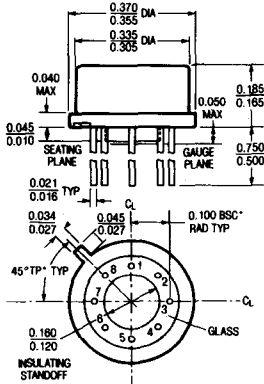


* C1 FOR LM107 ONLY
FOR LM107, THERE ARE NO INTERNAL
CONNECTIONS TO PINS 1, 5 AND 8

OFFSET BALANCE

PACKAGE DESCRIPTION

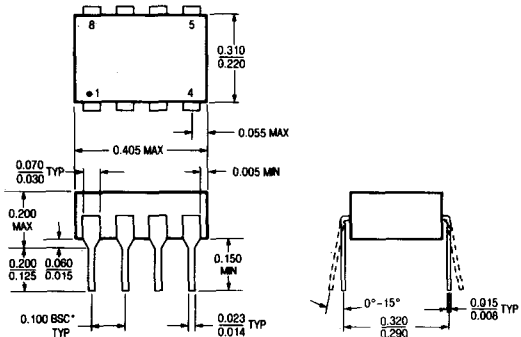
**H Package
Metal Can**



NOTE: DIMENSIONS IN INCHES

T_{jmax}	θ_{ja}	θ_{jc}
150°C	150°C/W	45°C/W

**J8 Package
8 Lead Hermetic Dip**



NOTE: DIMENSIONS IN INCHES UNLESS OTHERWISE NOTED.
*LEADS WITHIN 0.007 OF TRUE POSITION (TP) AT GAUGE PLANE

T_{jmax}	θ_{ja}
150°C	100°C/W

FEATURES

- *Guaranteed* 200pA max. input offset current
- *Guaranteed* 2nA max. input bias current
- *Guaranteed* 600 μ A max. supply current
- *Guaranteed* 0.5mV max. offset voltage
- *Guaranteed* 5 μ V/ $^{\circ}$ C max. drift
- Wide supply voltage range: ± 2 V to ± 18 V

APPLICATIONS

- Integrators
- Transducer amplifiers
- Analog memories
- Light meters

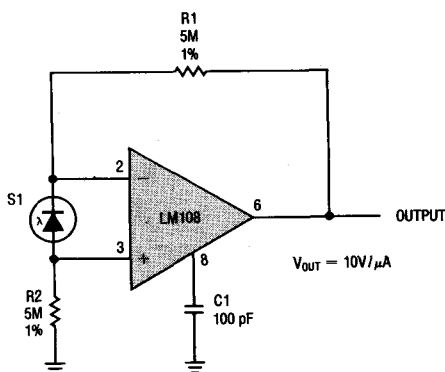
DESCRIPTION

The LM108 series of precision operational amplifiers are particularly well-suited for high source impedance applications requiring low offset and bias currents as well as low power dissipation. Unlike FET input amplifiers, the offset and bias currents of the LM108 do not change significantly with temperature variations. Advanced design, processing and testing techniques make Linear's LM108 a superior choice over previous devices.

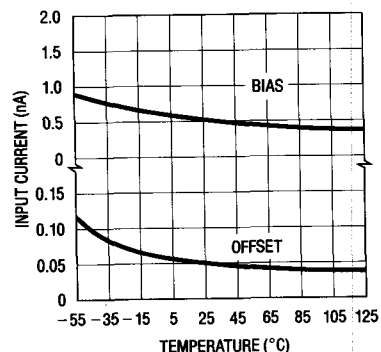
A photodiode sensor application is shown below. For applications requiring higher performance, see the LT1008, and LT1012.

2

Amplifier For Photodiode Sensor



Input Currents



LM108A/LM308A LM108/LM308

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	
LM108A/LM108	± 20V
LM308A/LM308	± 18V
Differential Input Current (Note 1)	± 10mA
Input Voltage (Note 2)	± 15V
Output Short Circuit Duration	Indefinite
Operating Temperature Range	
LM108A/LM108	-55°C to 125°C
LM308A/LM308	0°C to 70°C
Storage Temperature Range	
All Devices	-65°C to 150°C
Lead Temperature (Soldering, 10 sec.)	300°C

PACKAGE/ORDER INFORMATION

<p>TOP VIEW COMP 1 1, COMP 2 2, -IN 2, +IN 3, V- (CASE) 4, V+ 7, OUT 6, NC 5, COMP 2 8</p> <p>METAL CAN H PACKAGE</p>	ORDER PART NO.
	LM108AH LM108H LM308AH LM308H
<p>TOP VIEW COMP 1 1, -IN 2, +IN 3, V- 4, COMP 2 8, COMP 2 8, OUT 6, V+ 7, NC 5</p> <p>PLASTIC DIP N8 PACKAGE</p>	ORDER PART NO.
	LM308AN8 LM308N8

ELECTRICAL CHARACTERISTICS ± 5V ≤ V_S ≤ ± 20V and -55°C ≤ T_A ≤ 125°C, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LM108A			LM108			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V _{OS}	Input Offset Voltage	T _A = 25°C	●	0.3	0.5 1.0	0.7	2.0 3.0	mV mV	
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Temperature Coefficient of Input Offset Voltage		●	1.0	5.0	3.0	15	μV/°C	
I _{OS}	Input Offset Current	T _A = 25°C	●	0.05	0.2 0.4	0.05	0.2 0.4	nA nA	
$\frac{\Delta I_{OS}}{\Delta Temp}$	Average Temperature Coefficient of Input Offset Current		●	0.5	2.5	0.5	2.5	pA/°C	
I _B	Input Bias Current	T _A = 25°C	●	0.5	2.0 3.0	0.5	2.0 3.0	nA nA	
A _{VOL}	Large Signal Voltage Gain	T _A = 25°C, V _S = ± 15V, V _{OUT} = ± 10V, R _L ≥ 10kΩ	●	80 40	300	50 25	300	V/mV V/mV	
CMRR	Common Mode Rejection Ratio		●	96	110	85	100	dB	
PSRR	Power Supply Rejection Ratio		●	96	110	80	96	dB	
	Input Voltage Range	V _S = ± 15V	●	± 13.5		± 13.5		V	
V _{OUT}	Output Voltage Swing	V _S = ± 15V, R _L = 10kΩ	●	± 13	± 14	± 13	± 14	V	
R _{IN}	Input Resistance	T _A = 25°C (Note 3)		30	70	30	70	MΩ	
I _S	Supply Current	T _A = 25°C T _A = 125°C		0.3 0.15	0.6 0.4	0.3 0.15	0.6 0.4	mA mA	

ELECTRICAL CHARACTERISTICS $\pm 5V \leq V_s \leq \pm 15V$ and $0^\circ C \leq T_A \leq 70^\circ C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LM308A			LM308			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	$T_A = 25^\circ C$	●	0.3	0.5 0.73		2.0	7.5 10	mV mV
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Temperature Coefficient of Input Offset Voltage		●	2.0	5.0		6.0	30	$\mu V/^\circ C$
I_{OS}	Input Offset Current	$T_A = 25^\circ C$	●	0.2	1.0 1.5		0.2	1.0 1.5	nA nA
$\frac{\Delta I_{OS}}{\Delta Temp}$	Average Temperature Coefficient of Input Offset Current		●	2.0	10		2.0	10	$\mu A/^\circ C$
I_B	Input Bias Current	$T_A = 25^\circ C$	●	1.5	7.0 10		1.5	7.0 10	nA nA
A_{VOL}	Large Signal Voltage Gain	$T_A = 25^\circ C, V_S \pm 15V, V_{OUT} = \pm 10V, R_L \geq 10k\Omega$	●	80 60	300		25 15	300	V/mV V/mV
CMRR	Common Mode Rejection Ratio		●	96	110		80	100	dB
PSRR	Power Supply Rejection Ratio		●	96	110		80	96	dB
	Input Voltage Range	$V_S = \pm 15V$	●	± 14			± 14		V
V_{OUT}	Output Voltage Swing	$V_S = \pm 15V, R_L = 10k\Omega$	●	± 13	± 14		± 13	± 14	V
R_{IN}	Input Resistance	$T_A = 25^\circ C$ (Note 3)	●	10	40		10	40	M Ω
I_S	Supply Current	$T_A = 25^\circ C$		0.3	0.8		0.3	0.8	mA

2

The ● denotes the specifications which apply over the full operating temperature range.

For MIL-STD components, please refer to LTC 883 data sheet for test listing and parameters.

Note 1: Differential input voltages greater than 1V will cause excessive current to flow through the input protection diodes unless current limiting resistance is used.

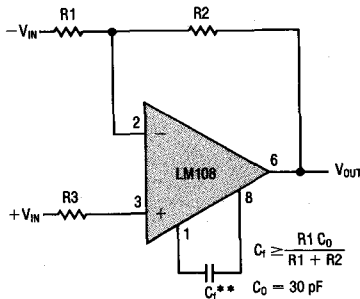
Note 2: For supply voltages less than $\pm 15V$, the maximum input voltage is equal to the supply voltage.

Note 3: Guaranteed by design.

TYPICAL APPLICATIONS

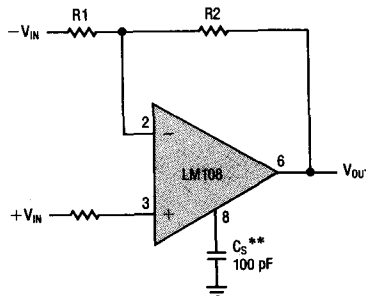
COMPENSATION CIRCUITS

Standard Compensation Circuit



** BANDWIDTH AND SLEW RATE ARE PROPORTIONAL TO $1/C_1$

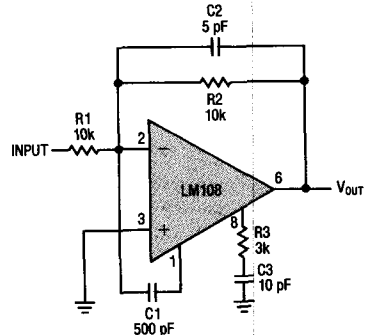
Alternate* Frequency Compensation



* IMPROVES REJECTION OF POWER SUPPLY NOISE BY A FACTOR OF TEN.

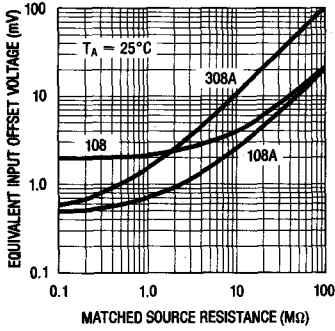
** BANDWIDTH AND SLEW RATE ARE PROPORTIONAL TO $1/C_S$

Feedforward Compensation

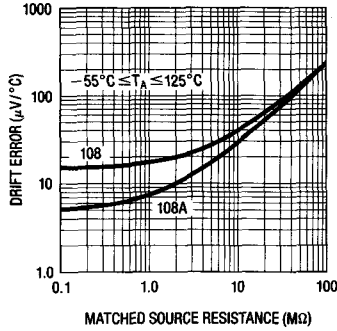


TYPICAL PERFORMANCE CHARACTERISTICS

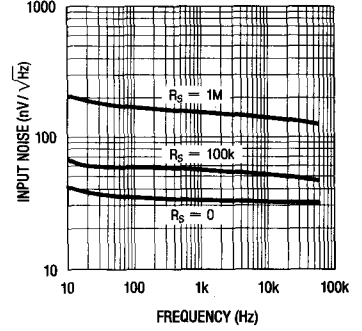
Guaranteed Offset Error



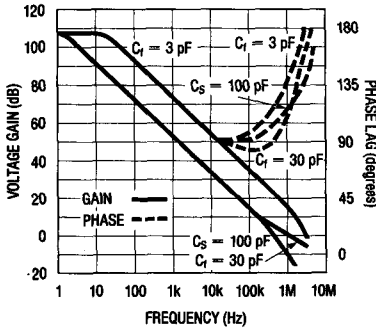
Guaranteed Drift Error



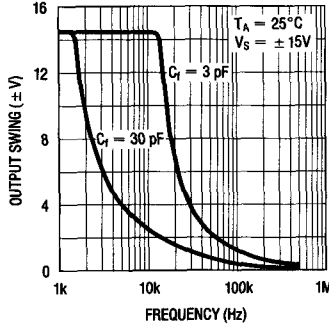
Input Noise Voltage



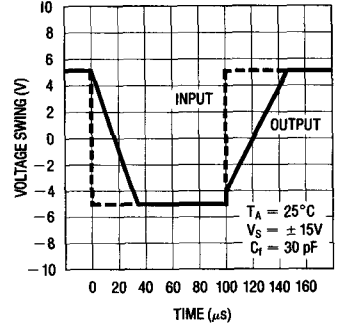
Open Loop Frequency Response



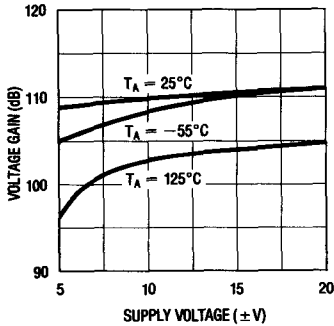
Large Signal Frequency Response



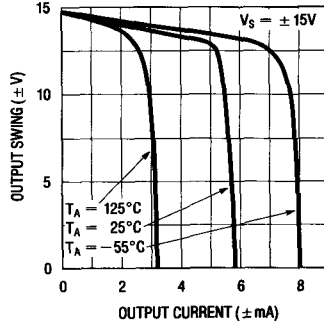
Voltage Follower Pulse Response



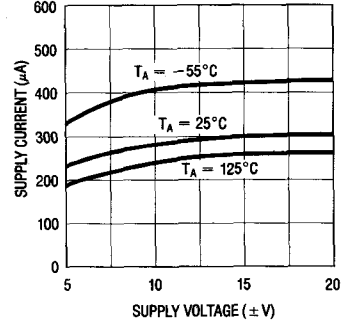
Voltage Gain



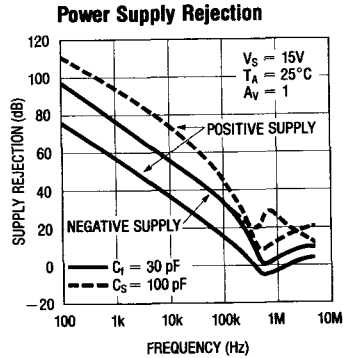
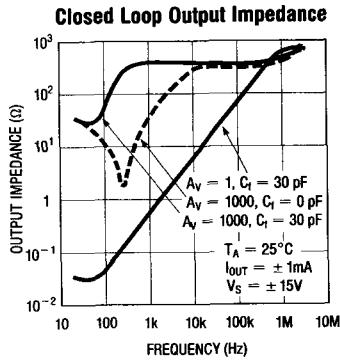
Output Swing



Supply Current

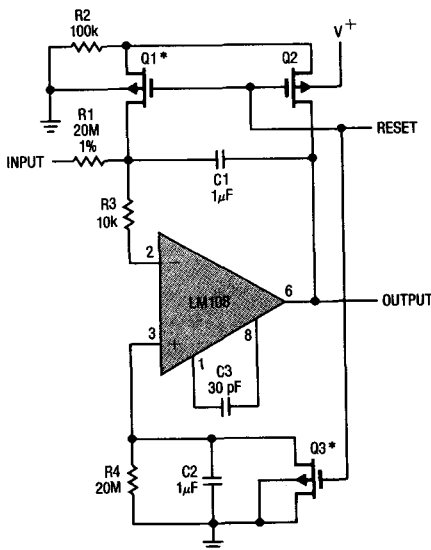


TYPICAL PERFORMANCE CHARACTERISTICS



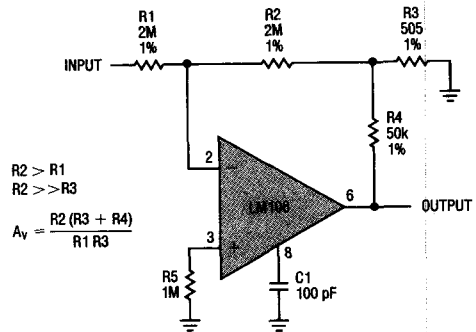
TYPICAL APPLICATIONS

Low Drift Integrator With Reset



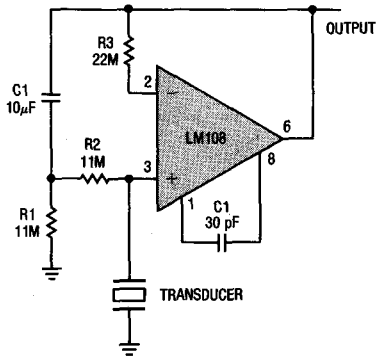
* Q1 AND Q3 SHOULD NOT HAVE INTERNAL GATE-PROTECTION DIODES.

Inverting Amplifier With High Input Resistance

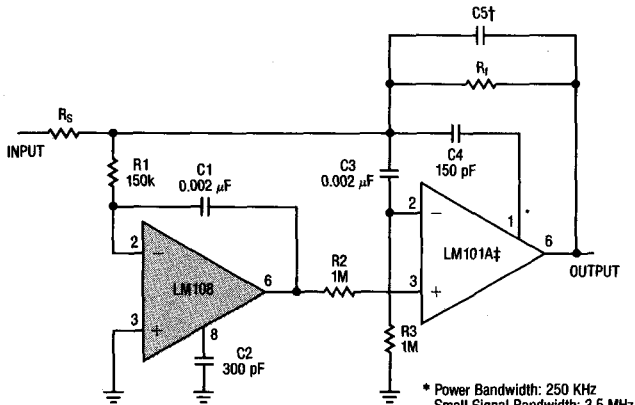


TYPICAL APPLICATIONS

Amplifier For Piezoelectric Transducers



Fast* Summing Amplifier

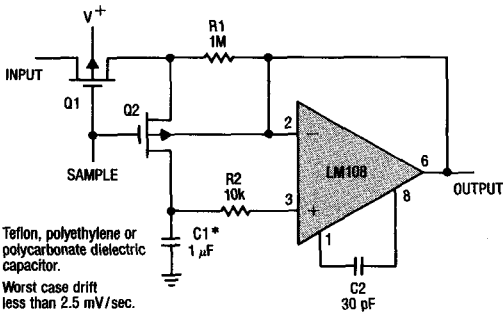


* Power Bandwidth: 250 KHz
Small Signal Bandwidth: 3.5 MHz
Slew Rate: 10V/µS

$$f_{CS} = \frac{6 \times 10^{-8}}{R_f}$$

‡ In addition to increasing speed, the LM101A raises high and low frequency gain, increases output drive capability and eliminates thermal feedback.

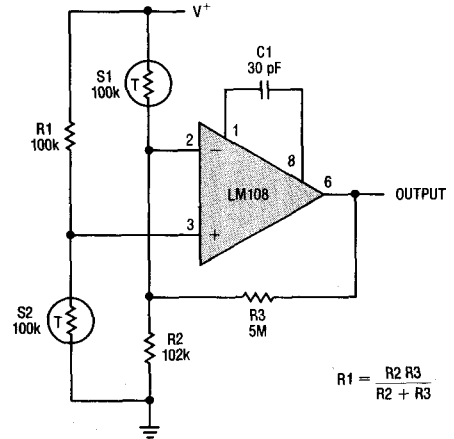
Sample and Hold



* Teflon, polyethylene or polycarbonate dielectric capacitor.

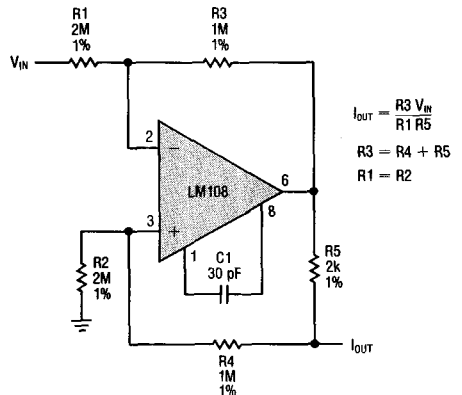
Worst case drift less than 2.5 mV/sec.

Amplifier For Bridge Transducers



$$R_1 = \frac{R_2 R_3}{R_2 + R_3}$$

Bilateral Current Source

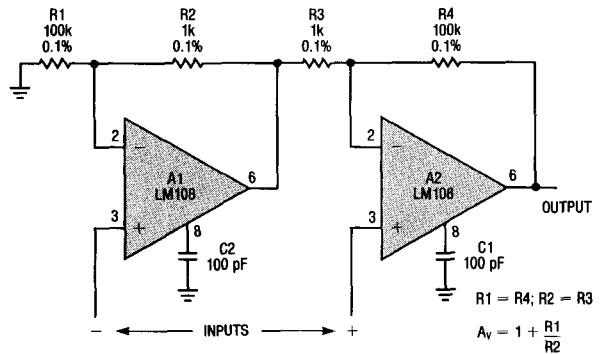


$$I_{OUT} = \frac{R_3 V_{IN}}{R_1 R_5}$$

$$R_3 = R_4 + R_5$$

$$R_1 = R_2$$

Differential Input Instrumentation Amplifier



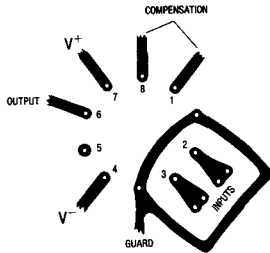
$$R_1 = R_4; R_2 = R_3$$

$$A_v = 1 + \frac{R_1}{R_2}$$

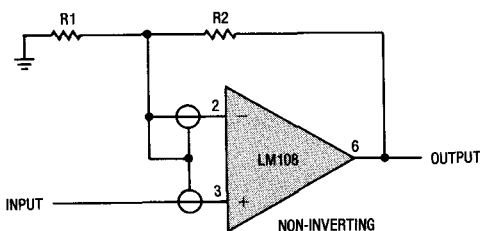
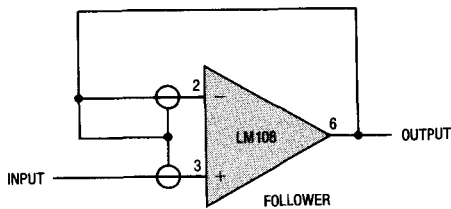
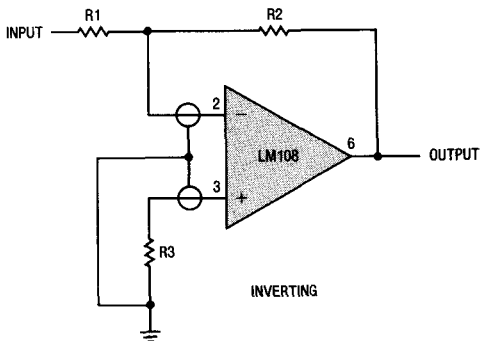
APPLICATIONS INFORMATION

Input guarding

Input guarding is used to reduce surface leakage. Guarding both sides of the board is required. Bulk leakage reduction is less and depends on the guard ring width.

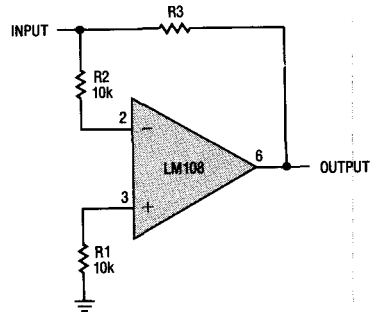


The guard ring is connected to a low impedance point at same potential as the sensitive input leads. Connections for various op amp configurations are shown below.

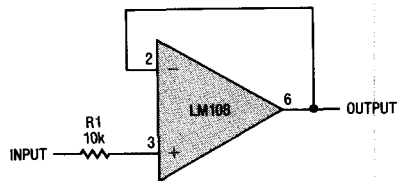


Input protection

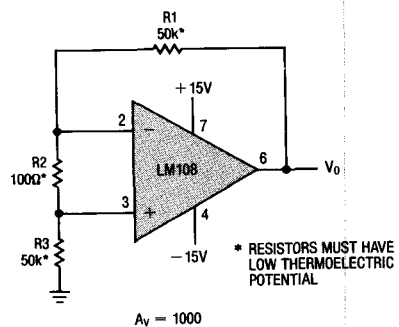
Current is limited by R2 even when input is connected to a voltage source outside the common mode range. If one supply reverses, current is controlled by R1. These resistors do not affect normal operation.



The input resistor controls the current when the input exceeds the supply voltages, when the power for the op amp is turned off, or when the output is shorted.



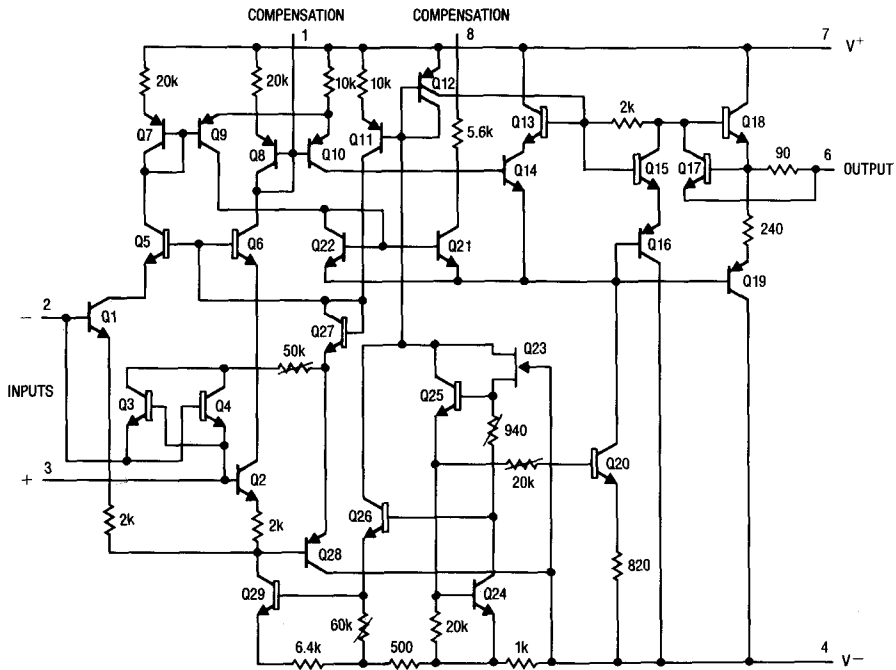
Offset Voltage Test Circuit†



† THIS CIRCUIT IS ALSO USED AS THE BURN-IN CONFIGURATION WITH SUPPLY VOLTAGES EQUAL TO $\pm 20V$, $R_1 = R_3 = 10k$, $R_2 = 200k$, $A_v = 100$.

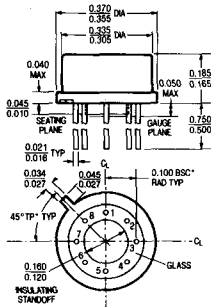
LM108A/LM308A LM108/LM308

SCHEMATIC DIAGRAM



PACKAGE DESCRIPTION

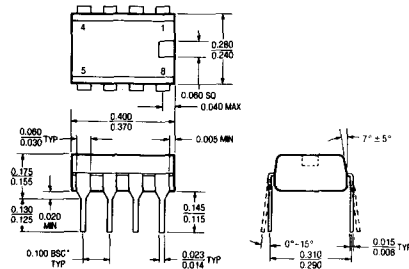
H Package
Metal Can



NOTE: DIMENSIONS IN INCHES

T_j max	θ_{ja}	θ_{jc}
150°C	150°C/W	45°C/C/W

N8 Package
8 Lead Plastic



NOTE: DIMENSIONS IN INCHES UNLESS OTHERWISE NOTED.
*LEADS WITHIN 0.007 OF TRUE POSITION (TP) AT GAUGE PLANE.

T_j max	θ_{ja}
100°C	130°C/W

FEATURES

- *Guaranteed* 1.0mV Max. Input Offset Voltage
- *Guaranteed* 100,000 Min. Gain
- *Guaranteed* 50V/ μ s Slew Rate
- *Guaranteed* 20nA Max. Input Offset Current
- 15MHz Bandwidth
- Unity Gain Stable

APPLICATIONS

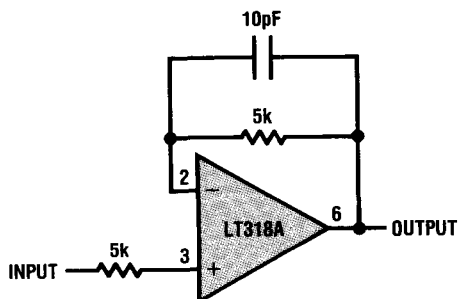
- Wideband Amplifiers
- High Frequency Absolute Value Circuits
- D/A Converter Amplifiers
- Fast Integrators

DESCRIPTION

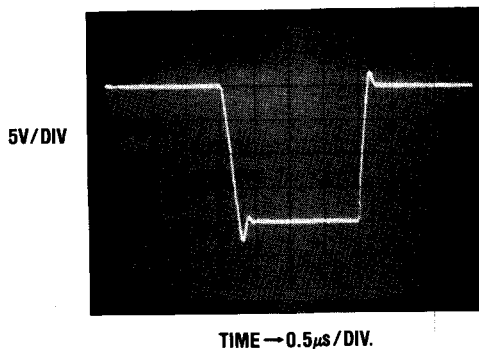
The LT118A is an improved version of the industry standard LM118. The LT118A features lower input offset voltage, lower input offset currents, higher gain and higher common mode and power supply rejection. Because of these enhancements, the LT118A will improve the accuracy of most applications. Unlike many wideband amplifiers, the LT118A is unity gain stable and has a slew rate of 50V/ μ s. When used in inverting amplifier applications, feedforward compensation can be used to achieve slew rates in excess of 150V/ μ s. Linear Technology Corporation's advanced processing techniques make the LT118A an ideal choice for high speed applications.

2

Voltage Follower



Voltage Follower Pulse Response



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±20V
Differential Input Current (Note 1)	±10mA
Input Voltage (Note 2)	±20V
Output Short Circuit Duration	Indefinite
Operating Temperature Range	
LT118A/LM118	-55°C to 125°C
LT318A/LM318	0°C to 70°C
Storage Temperature Range	
All Devices	-65°C to 150°C
Lead Temperature (Soldering, 10 sec.)	300°C

PACKAGE/ORDER INFORMATION

TOP VIEW	ORDER PART NUMBER
<p>METAL CAN H PACKAGE</p>	<p>LT118AH LM118H LT318AH LM318H</p>
<p>HERMETIC DIP J8 PACKAGE PLASTIC DIP N8 PACKAGE</p>	<p>LT118AJ8 LM118J8 LT318AJ8 LM318J8 LT318AN8 LM318N8</p>

ELECTRICAL CHARACTERISTICS (Note 3)

SYMBOL	PARAMETER	CONDITIONS	LT118A			LM118			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V _{OS}	Input Offset Voltage			0.5	1	2	4	6	mV
			●	1	2				
I _{OS}	Input Offset Current			6	20	6	50	100	nA
			●	10	30				
I _B	Input Bias Current			120	250	120	250	500	nA
			●		500				
R _{IN}	Input Resistance		1	3	1	3		MΩ	
A _V	Large Signal Voltage Gain	V _S = ±15V, V _{OUT} = ±10V, R _L ≥ 2kΩ	●	100	500	50	200		V/mV
				100		25		V/mV	
SR	Slew Rate	V _S = ±15V, A _V = 1		50	70	50	70		V/μs
GBW	Gain Bandwidth Product	V _S = ±15V		15		15			MHz
	Output Voltage Swing	V _S = ±15V, R _L = 2kΩ	●	±12	±13	±12	±13		V
	Input Voltage Range	V _S = ±15V	●	±11.5		±11.5			V
I _S	Supply Current	T _A = 125°C		5	8	5	8	8	mA
			●		4.5				
CMRR	Common Mode Rejection Ratio		●	86	100	80	100		dB
PSRR	Power Supply Rejection Ratio		●	86	100	70	80		dB

ELECTRICAL CHARACTERISTICS (Note 3)

SYMBOL	PARAMETER	CONDITIONS	LT318A			LM318			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage		●	0.5	1 2		4	10 15	mV mV
I_{OS}	Input Offset Current		●	10	20 30		30	200 750	nA nA
I_B	Input Bias Current		●	150	250 500		150	500 750	nA nA
R_{IN}	Input Resistance			0.5	3		0.5	3	MΩ
A_V	Large Signal Voltage Gain	$V_S = \pm 15V, V_{OUT} = \pm 10V, R_L \geq 2k\Omega$	●	100 100	500		25 20	200	V/mV V/mV
SR	Slew Rate	$V_S = \pm 15V, A_V = 1$		50	70		50	70	V/ μ S
GBW	Gain Bandwidth Product	$V_S = \pm 15V$			15			15	MHz
	Output Voltage Swing	$V_S = \pm 15V, R_L = 2k\Omega$	●	± 12	± 13		± 12	± 13	V
	Input Voltage Range	$V_S = \pm 15V$	●	± 11.5			± 11.5		V
I_S	Supply Current			5	10		5	10	mA
CMRR	Common Mode Rejection Ratio		●	86	100		70	100	dB
PSRR	Power Supply Rejection Ratio		●	86	100		65	80	dB

The ● denotes those specifications which apply over the full operating temperature range.

The shaded electrical specifications indicate those parameters which have been improved or guaranteed test limits provided for the first time.

Note 1: The inputs are shunted with back-to-back zeners for overvoltage protection. Excessive current will flow if a differential voltage greater than 5V is applied to the inputs.

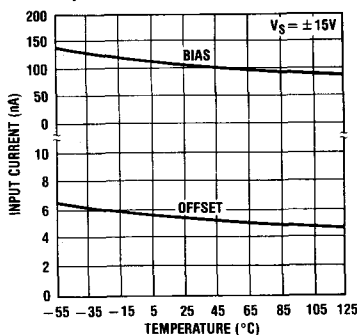
Note 2: For supply voltages less than $\pm 15V$, the maximum input voltage is equal to the supply voltage.

Note 3: These specifications apply for $\pm 5V \leq V_S \leq \pm 20V$. The power supplies must be bypassed with a 0.1 μ F or greater disc capacitor within 4 inches of the device.

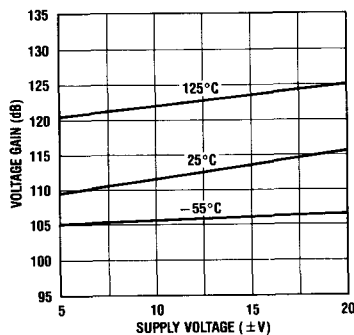
2

TYPICAL PERFORMANCE CHARACTERISTICS

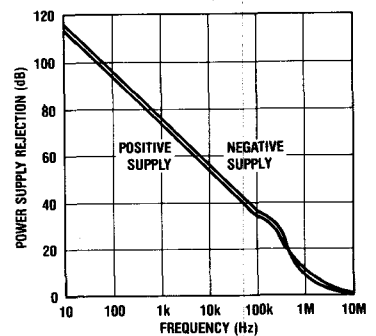
Input Current



Voltage Gain

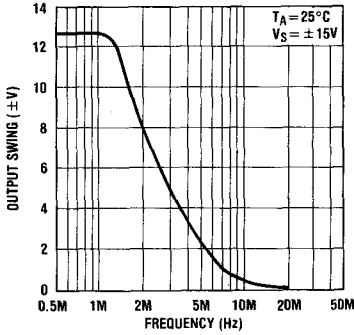


Power Supply Rejection

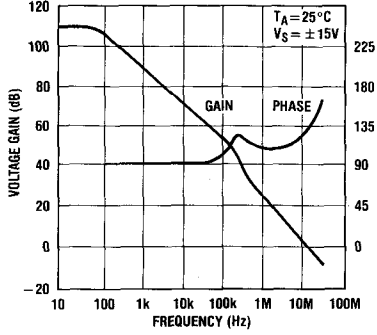


TYPICAL PERFORMANCE CHARACTERISTICS

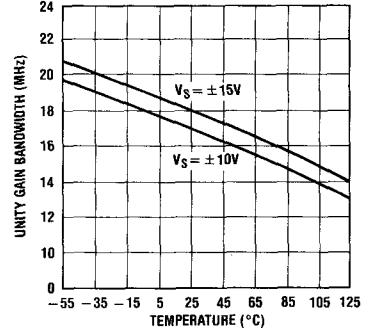
Large Signal Frequency Response



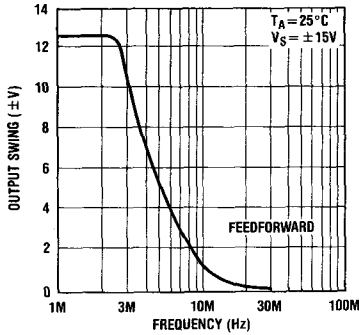
Open Loop Frequency Response



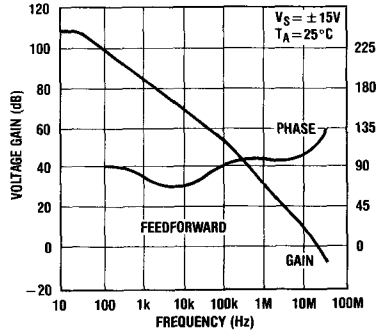
Unity Gain Bandwidth



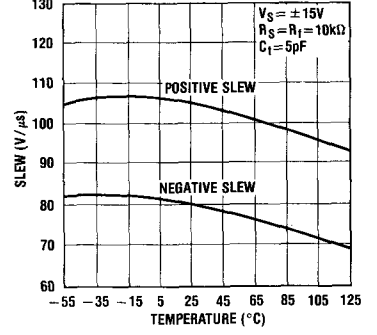
Large Signal Frequency Response



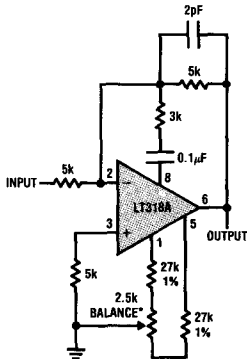
Open Loop Frequency Response



Voltage Follower Slew Rate

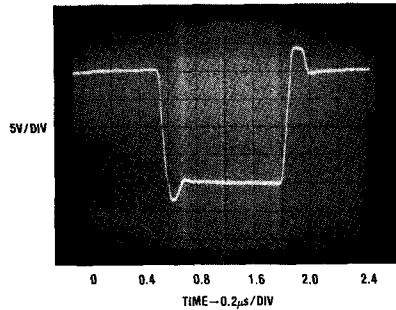


Feedforward Compensation for Slew Rates of 150V/μs

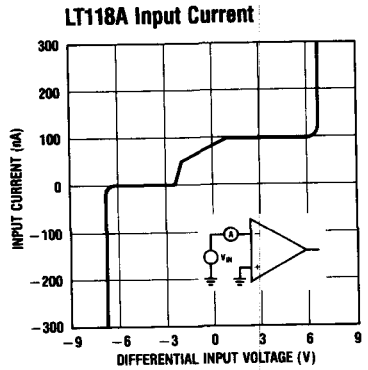
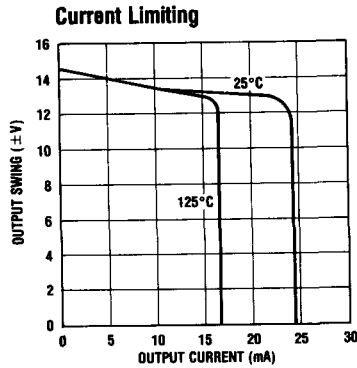
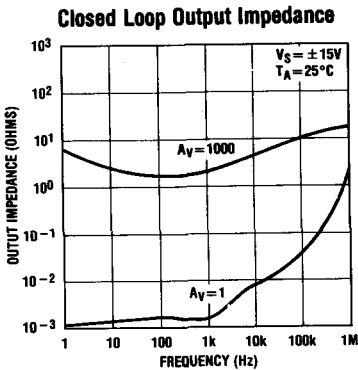
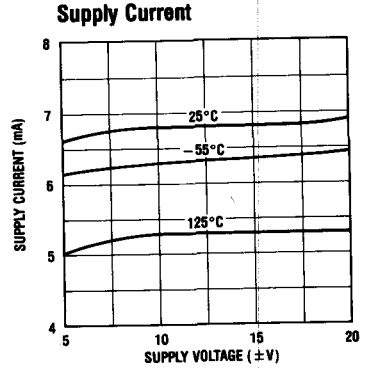
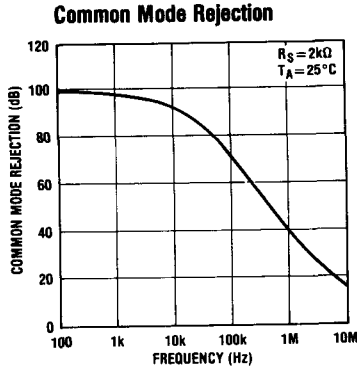
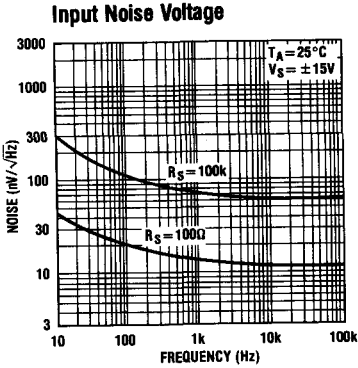


*BALANCE CIRCUIT NECESSARY FOR INCREASED SLEW RATE

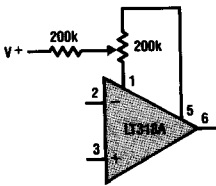
Pulse Response of Feedforward Inverter



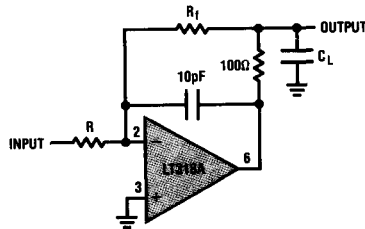
TYPICAL PERFORMANCE CHARACTERISTICS



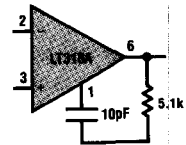
Offset Balancing



Isolating Large Capacitive Loads

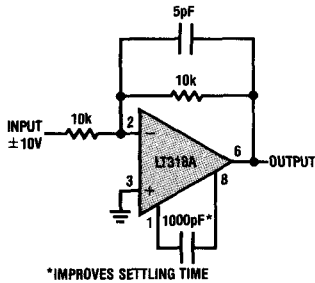


Overcompensation for Increased Stability

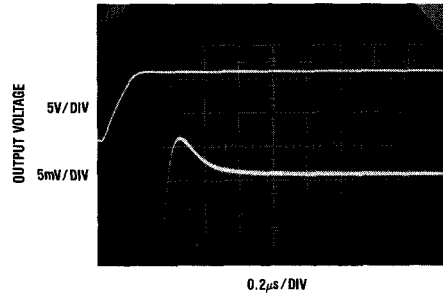


SETTLING TIME CIRCUITS

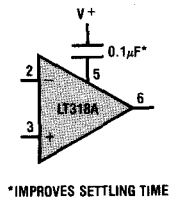
Settling Time Test Circuit



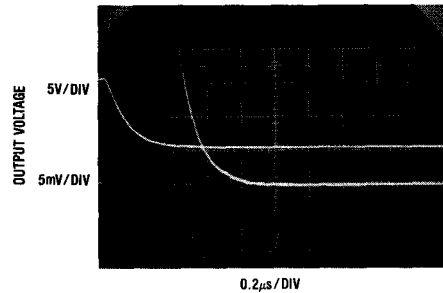
Settling Time



Alternate Compensation for Improved Settling Time



Settling Time



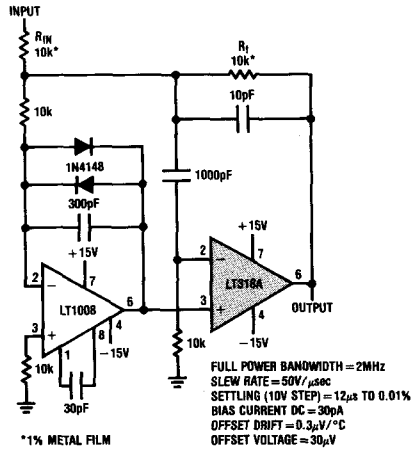
APPLICATIONS INFORMATION

Because of their wider bandwidth, the LT118A and LM118 operational amplifiers require more application care than most general purpose low frequency amplifiers. One of the most critical requirements is that power supplies should be bypassed with a 0.1µF (or larger) disc ceramic capacitor within an inch of the device. Also, stray capacitance at either the input or output can cause oscillation. While input capacitance can be compensated by placing a capacitor across the feedback resistor, load capacitance must be minimized or isolated as shown. Even the 50pF input capacitance of a 1X scope probe can alter the response of the device.

Settling time, an important parameter in many high speed amplifier applications, is difficult to measure and optimize. Settling time is very "application dependent" and is influenced by external components, layout and the amplifier. In general, the settling time to 0.01% can be minimized by using a circuit similar to that shown. In addition to the compensation network shown, a capacitor is needed across the feedback resistor to minimize ringing.

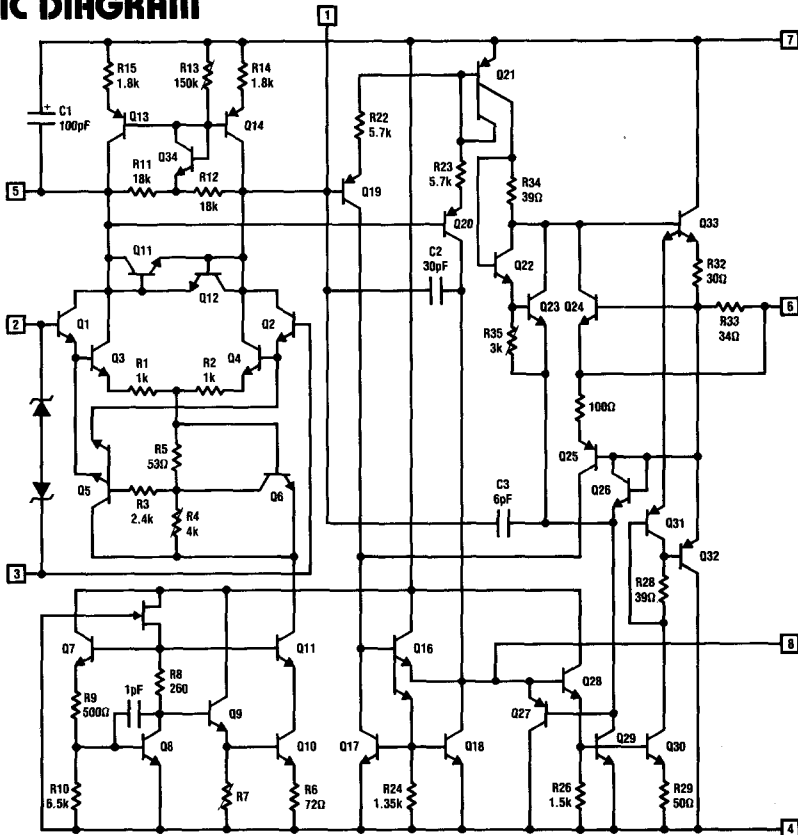
Power supply bypassing can also affect settling time. The amplifier has low power supply rejection ratio at high frequencies, so transients and ringing on the supply leads can appear at the output. Large (22µF) solid tantalum capacitors are preferred to minimize supply aberrations.

Precision Inverting Amplifier



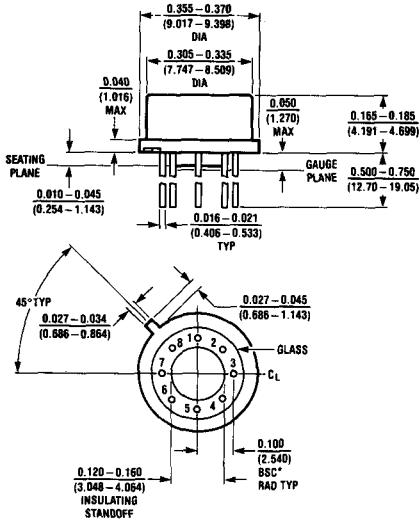
2

SCHEMATIC DIAGRAM



PACKAGE DESCRIPTION

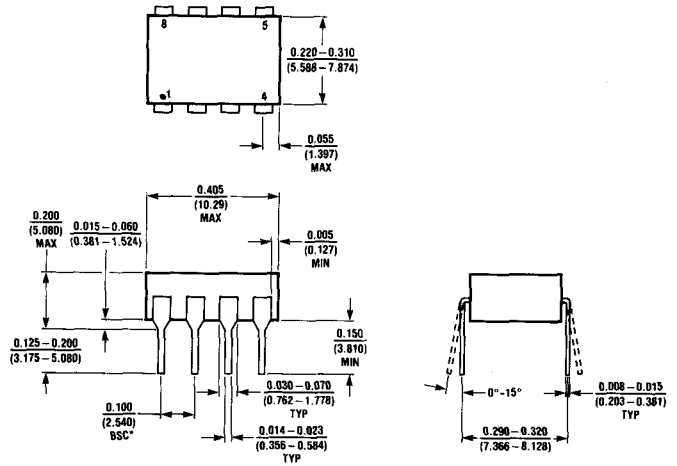
H Package
Metal Can



NOTE: DIMENSIONS IN INCHES

T _{fmax}	θ _{ja}	θ _{jc}
150°C	150°C/W	45°C/W

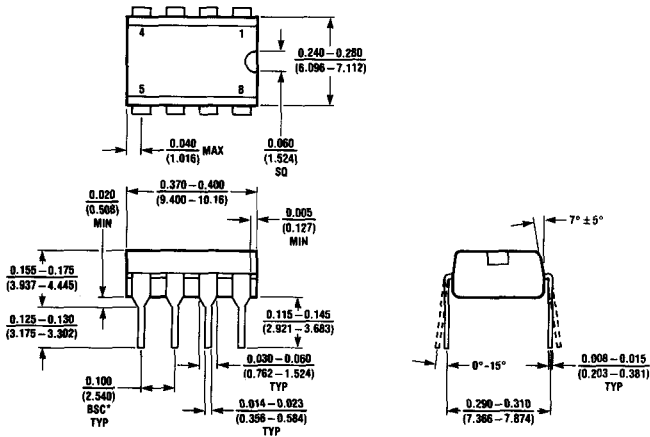
J8 Package
8 Lead Hermetic DIP



NOTE: DIMENSIONS IN INCHES UNLESS OTHERWISE NOTED
*LEADS WITHIN 0.007 OF TRUE POSITION (TP) AT GAUGE PLANE

T _{fmax}	θ _{ja}
150°C	100°C/W

N8 Package
8 Lead Plastic



NOTE: DIMENSIONS IN INCHES UNLESS OTHERWISE NOTED
*LEADS WITHIN 0.007 OF TRUE POSITION (TP) AT GAUGE PLANE

T _{fmax}	θ _{ja}
100°C	130°C/W

FEATURES

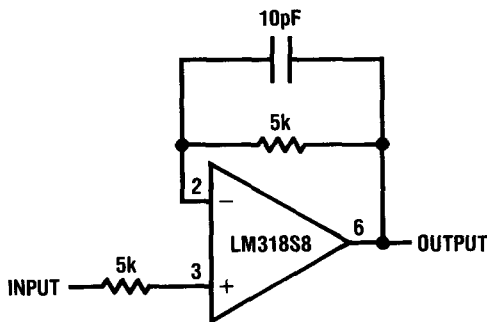
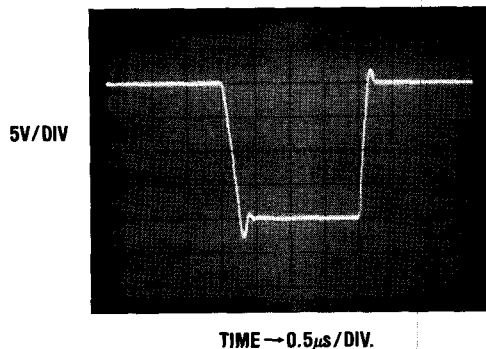
- 4mV Typ. Input Offset Voltage
- *Guaranteed* 25,000 Min. Gain
- *Guaranteed* 50V/μs Slew Rate
- 30nA Typ. Input Offset Current
- 15MHz Bandwidth
- Unity Gain Stable

APPLICATIONS

- Wideband Amplifiers
- High Frequency Absolute Value Circuits
- D/A Converter Amplifiers
- Fast Integrators

DESCRIPTION

The LM318 is a high speed, unity gain stable operational amplifier designed for applications requiring high slew rate and wide bandwidth. Although the device is internally compensated for unity gain operation, external compensation can be added for increased stability in reduced bandwidth applications. With a single capacitor, the 0.1% settling time is reduced to under 1μs. Feedforward compensation can be used in inverting applications to increase slew rate to over 150V/μs and almost double the bandwidth.

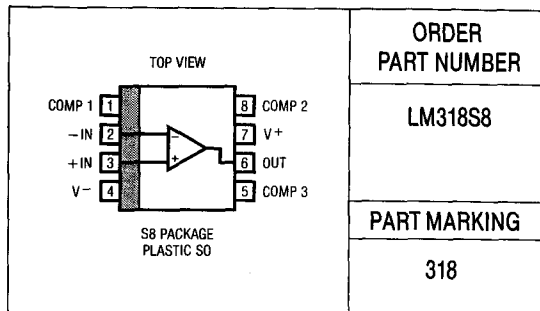
Voltage Follower

Voltage Follower Pulse Response


LM318S8

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	$\pm 20V$
Differential Input Current (Note 1)	$\pm 10mA$
Input Voltage (Note 2)	$\pm 20V$
Output Short Circuit Duration	Indefinite
Operating Temperature Range	$0^{\circ}C$ to $70^{\circ}C$
Storage Temperature Range	$-65^{\circ}C$ to $150^{\circ}C$
Lead Temperature (Soldering, 10 sec.)	$300^{\circ}C$

PACKAGE/ORDER INFORMATION



ELECTRICAL CHARACTERISTICS (Note 3)

SYMBOL	PARAMETER	CONDITIONS	LM318			UNITS
			MIN	TYP	MAX	
V_{os}	Input Offset Voltage			4	10	mV
I_{os}	Input Offset Current			30	200	nA
I_B	Input Bias Current			150	500	nA
R_{IN}	Input Resistance		0.5	3		M Ω
A_V	Large Signal Voltage Gain	$V_S = \pm 15V, V_{OUT} = \pm 10V, R_L \geq 2k\Omega$		25	200	V/mV
SR	Slew Rate	$V_S = \pm 15V, A_V = 1$		20		V/mV
GBW	Gain Bandwidth Product	$V_S = \pm 15V$		50	70	V/ μ s
	Output Voltage Swing	$V_S = \pm 15V, R_L = 2k\Omega$			15	MHz
	Input Voltage Range	$V_S = \pm 15V$		± 12	± 13	V
I_S	Supply Current					V
CMRR	Common-Mode Rejection Ratio			5	10	mA
PSRR	Power Supply Rejection Ratio			70	100	dB
				65	80	dB

The ● denotes those specifications which apply over the full operating temperature range.

Note 1: The inputs are shunted with back-to-back zeners for overvoltage protection. Excessive current will flow if a differential voltage greater than 5V is applied to the inputs.

Note 2: For supply voltages less than $\pm 15V$, the maximum input voltage is equal to the supply voltage.

Note 3: These specifications apply for $\pm 5V \leq V_S \leq \pm 20V$. The power supplies must be bypassed with a 0.1 μ F or greater disc capacitor within 4 inches of the device.

FEATURES

- *Guaranteed max. 0.5μV/°C Drift*
- *Guaranteed max. 0.6μV pk-pk Noise*
- *Guaranteed max. 2nA Bias Current*
- *Guaranteed minimum 114dB CMRR*

APPLICATIONS

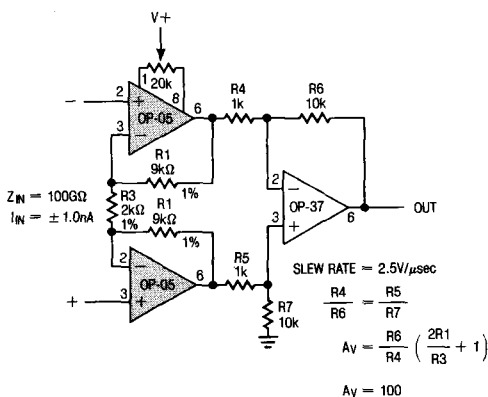
- Strain Gauges
- Thermocouple Amplifiers
- Instrumentation Amplifiers
- Medical Instruments

DESCRIPTION

The OP-05 is an internally compensated op-amp which provides excellent input offset voltage, low bias current, very high common mode rejection, and low offset voltage drift with temperature when the input offset voltage is externally trimmed to zero. Direct replacement of similar devices in existing systems can result in significant system performance improvement without redesign. The OP-05 is particularly well suited for instrumentation and low signal level applications where precision and stability over time and temperature are important. Internal frequency compensation enhances the OP-05's versatility for a wide variety of precision op-amp uses. Linear's advanced design, process and test techniques ensure device performance as well as reliability. An instrumentation amplifier application is shown below. For higher performance requirements see the LT1001 single precision op amp and the LT1002 dual matched precision op amp series.

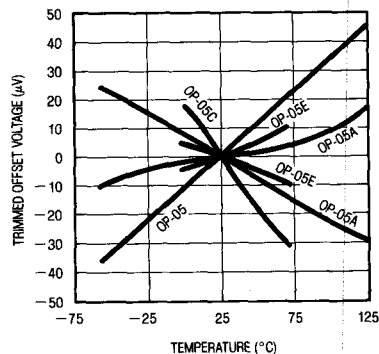
2

Instrumentation Amplifier



Trimmed Offset Voltage with Temperature of Six Representative Units

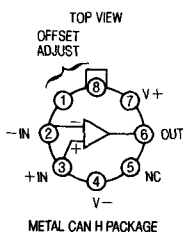
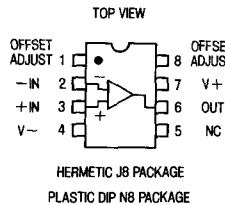
(Offset Trimmed to Zero at 25°C with 20kΩ Pot)



ABSOLUTE MAXIMUM RATINGS

Supply Voltage $\pm 22V$
 Differential Input Voltage $\pm 30V$
 Input Voltage Equal to Supply Voltage
 Output Short Circuit Duration Indefinite
 Operating Temperature Range
 OP-05/OP-05A $-55^{\circ}C$ to $125^{\circ}C$
 OP-05E/OP-05C $0^{\circ}C$ to $70^{\circ}C$
 Storage Temperature Range
 All Devices $-65^{\circ}C$ to $150^{\circ}C$
 Lead Temperature (Soldering, 10 sec.) $300^{\circ}C$

PACKAGE/ORDER INFORMATION

 <p>TOP VIEW OFFSET ADJUST 1 8 7 V+ -IN 2 + 3 +IN 3 4 V- 6 OUT 5 NC</p> <p>METAL CAN H PACKAGE</p>	ORDER PART NO.	OFFSET VOLTAGE MAX
	OP-05AH OP-05H OP-05EH OP-05CH	0.15mV 0.5mV 0.5mV 1.3mV
 <p>TOP VIEW OFFSET ADJUST 1 -IN 2 +IN 3 V- 4 8 7 V+ 6 OUT 5 NC</p> <p>HERMETIC J8 PACKAGE PLASTIC DIP N8 PACKAGE</p>	OP-05AJ8 OP-05J8 OP-05EJ8 OP-05CJ8 OP-05EN8 OP-05CN8	0.15mV 0.5mV 0.5mV 1.3mV 0.5mV 1.3mV

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V, T_A = 25^{\circ}C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	OP-05A			OP-05			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage			0.07	0.15		0.2	0.5	mV
$\frac{\Delta V_{OS}}{\Delta Time}$	Long Term Input Offset Voltage Stability	(Notes 1 and 2)		0.2	1.0		0.2	1.0	$\mu V/$ Month
I_{OS}	Input Offset Current			0.7	2.0		1.0	2.8	nA
I_B	Input Bias Current			± 0.7	± 2.0		± 1.0	± 3.0	nA
e_n	Input Noise Voltage	0.1Hz to 10Hz (Note 2)		0.35	0.6		0.35	0.6	μV_{p-p}
	Input Noise Voltage Density	$f_o = 10Hz$ $f_o = 100Hz$ (Note 2) $f_o = 1000Hz$		10.3 10.0 9.6	18.0 13.0 11.0		10.3 10.0 9.6	18.0 13.0 11.0	nV/\sqrt{Hz}
i_n	Input Noise Current	0.1Hz to 10Hz (Note 2)		14	30		14	30	pA_{p-p}
	Input Noise Current Density	$f_o = 10Hz$ $f_o = 100Hz$ (Note 2) $f_o = 1000Hz$		0.32 0.14 0.12	0.80 0.23 0.17		0.32 0.14 0.12	0.80 0.23 0.17	pA/\sqrt{Hz}
R_{in}	Input Resistance Differential Mode	(Note 3)	30	80		20	60		$M\Omega$
	Input Resistance Common Mode			200			200		$G\Omega$
	Input Voltage Range		± 13.5	± 14.0		± 13.5	± 14.0		V
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 13.5V$	114	126		114	126		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 3V$ to $\pm 18V$	100	108		100	108		dB
A_{VOL}	Large Signal Voltage Gain	$R_L \geq 2k\Omega, V_O = \pm 10V$ $R_L \geq 500\Omega, V_O = \pm 0.5V$ $V_S = \pm 3V$ (Note 3)	300 150	500 500		200 150	500 500		V/mV
V_{OUT}	Maximum Output Voltage Swing	$R_L \geq 10k\Omega$ $R_L \geq 2k\Omega$ $R_L \geq 1k\Omega$	± 12.5 ± 12.0 ± 10.5	± 13.0 ± 12.8 ± 12.0		± 12.5 ± 12.0 ± 10.5	± 13.0 ± 12.8 ± 12.0		V
SR	Slew Rate	$R_L \geq 2k\Omega$ (Note 2)	0.1	0.3		0.1	0.3		V/ μS
GBW	Closed Loop Bandwidth	$A_{VOL} = +1$ (Note 2)	0.4	0.6		0.4	0.6		MHz
Z_o	Open Loop Output Impedance	$V_O = 0, I_O = 0, f = 10Hz$		60			60		Ω
P_d	Power Dissipation	No load		90	120		90	120	mW
		$V_S = \pm 3V$, No load		4	6		4	6	
	Offset Adjustment Range	Null Pot = $20k\Omega$		± 4			± 4		mV

See Notes on page 2-324

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $-55^\circ C \leq T_A \leq 125^\circ C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	OP-05A			OP-05			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage		●	0.10	0.24	0.3	0.7	mV	
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Input Offset Voltage Drift Without External Trim	Null Pot = 20k Ω (Note 2)	●	0.3	0.9	0.7	2.0	$\mu V/^\circ C$	
	With External Trim		●	0.2	0.5	0.3	1.0		
I_{OS}	Input Offset Current		●	1.0	4.0	1.8	5.6	nA	
$\frac{\Delta I_{OS}}{\Delta Temp}$	Average Input Offset Current Drift	(Note 2)	●	5	25	8	50	pA/°C	
I_B	Input Bias Current		●	± 1.0	± 4.0	± 2.0	± 6.0	nA	
$\frac{\Delta I_B}{\Delta Temp}$	Average Input Bias Current Drift	(Note 2)	●	8	25	13	50	pA/°C	
	Input Voltage Range		●	± 13.0	± 13.5	± 13.0	± 13.5	V	
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 13V$	●	110	123	110	123	dB	
PSRR	Power Supply Rejection Ratio	$V_S = \pm 3V$ to $\pm 18V$	●	94	106	94	106	dB	
A_{VOL}	Large Signal Voltage Gain	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	●	200	400	150	400	V/mV	
V_{OUT}	Output Voltage Swing	$R_L \geq 2k\Omega$	●	± 12.0	± 12.6	± 12.0	± 12.6	V	

2

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $T_A = 25^\circ C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	OP-05E			OP-05C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage			0.2	0.5	0.3	1.3	mV	
$\frac{\Delta V_{OS}}{\Delta Time}$	Long Term Input Offset Voltage Stability	(Notes 1 and 2)		0.3	1.5	0.4	2.0	$\mu V/Month$	
I_{OS}	Input Offset Current			1.2	3.8	1.8	6.0	nA	
I_B	Input Bias Current			± 1.2	± 4.0	± 1.8	± 7.0	nA	
e_n	Input Noise Voltage	0.1Hz to 10Hz (Note 2)		0.35	0.6	0.38	0.65	μV_{P-P}	
	Input Noise Voltage Density	$f_o = 10Hz$ $f_o = 100Hz$ (Note 2) $f_o = 1000Hz$		10.3	18.0	10.5	20.0	nV/ \sqrt{Hz}	
				10.0	13.0	10.2	13.5		
i_n	Input Noise Current	0.1Hz to 10Hz (Note 2)		14	30	15	35	pA $_{P-P}$	
	Input Noise Current Density	$f_o = 10Hz$ $f_o = 100Hz$ (Note 2) $f_o = 1000Hz$		0.32	0.80	0.35	0.90	pA/ \sqrt{Hz}	
				0.14	0.23	0.15	0.27		
				0.12	0.17	0.13	0.18		
R_{in}	Input Resistance Differential Mode	(Note 3)		15	50	8	33	M Ω	
	Input Resistance Common Mode				160		120	G Ω	
	Input Voltage Range			± 13.5	± 14.0	± 13.5	± 14.0	V	
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 13.5V$		110	123	100	120	dB	
PSRR	Power Supply Rejection Ratio	$V_S = \pm 3V$ to $\pm 18V$		94	106	90	104	dB	
A_{VOL}	Large Signal Voltage Gain	$R_L \geq 2k\Omega$, $V_O = \pm 10V$		200	500	120	400	V/mV	
		$R_L \geq 500\Omega$, $V_O = \pm 0.5V$		150	500	100	400		
		$V_S = \pm 3V$ (Note 3)							
V_{OUT}	Maximum Output Voltage Swing	$R_L \geq 10k\Omega$		± 12.5	± 13.0	± 12.0	± 13.0	V	
		$R_L \geq 2k\Omega$		± 12.0	± 12.8	± 11.5	± 12.8		
		$R_L \geq 1k\Omega$		± 10.5	± 12.0		± 12.0		
SR	Slew Rate	$R_L \geq 2k\Omega$ (Note 2)		0.1	0.3	0.1	0.3	V/ μs	
GBW	Closed Loop Bandwidth	$A_{VCL} = +1$ (Note 2)		0.4	0.6	0.4	0.6	MHz	
Z_o	Open Loop Output Impedance	$V_O = 0$, $I_O = 0$, $f = 10Hz$		60		60		Ω	
P_d	Power Dissipation	No load		90	120	95	150	mW	
		$V_S = \pm 3V$, No load		4	6	4	8		
	Offset Adjustment Range	Null Pot = 20k Ω		± 4		± 4		mW	

See Notes on page 2-324

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V, 0^\circ C \leq T_A \leq 70^\circ C$.

SYMBOL	PARAMETER	CONDITIONS	OP-05E			OP-05C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage		●	0.25	0.6		0.35	1.6	mV
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Input Offset Voltage Drift Without External Trim With External Trim	Null Pot = 20k Ω (Note 2)	● ●	0.7 0.2	2.0 0.6		1.3 0.4	4.5 1.5	$\mu V/^\circ C$
I_{OS}	Input Offset Current		●	1.4	5.3		2.0	8.0	nA
$\frac{\Delta I_{OS}}{\Delta Temp}$	Average Input Offset Current Drift	(Note 2)	●	8	35		12	50	pA/ $^\circ C$
I_B	Input Bias Current		●	± 1.5	± 5.5		± 2.2	± 9.0	nA
$\frac{\Delta I_B}{\Delta Temp}$	Average Input Bias Current Drift	(Note 2)	●	13	35		18	50	pA/ $^\circ C$
	Input Voltage Range		●	± 13.0	± 13.5		± 13.0	± 13.5	V
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 13V$	●	107	123		97	120	dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 3V$ to $\pm 18V$	●	90	103		86	100	dB
A_{VOL}	Large Signal Voltage Gain	$R_L \geq 2k\Omega, V_o = \pm 10V$	●	180	450		100	400	V/mV
V_{OUT}	Output Voltage Swing	$R_L \geq 2k\Omega$	●	± 12.0	± 12.6		± 11.0	± 12.6	V

The ● denotes the specifications which apply over the full operating temperature range.

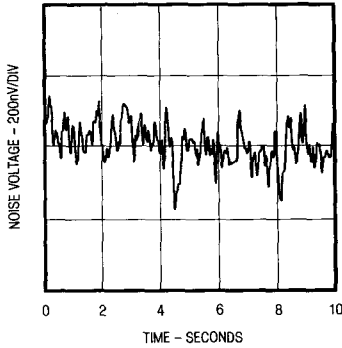
Note 1: Long term offset voltage stability is the average value of offset voltage vs. time plotted over extended periods following 30 days of operation. Values for time under 30 days of operation are typically 2.5 μV following the first hour of operation.

Note 2: This parameter is sample tested.

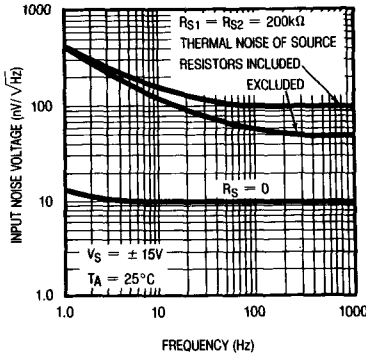
Note 3: This parameter is guaranteed by design.

TYPICAL PERFORMANCE CHARACTERISTICS

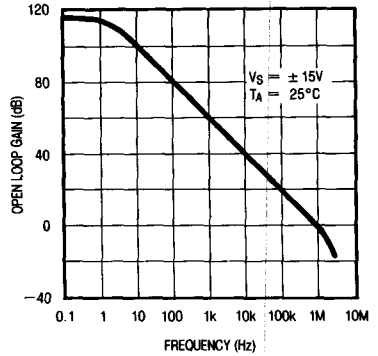
**Low Frequency Noise
(Closed Loop Gain = 25,000)**



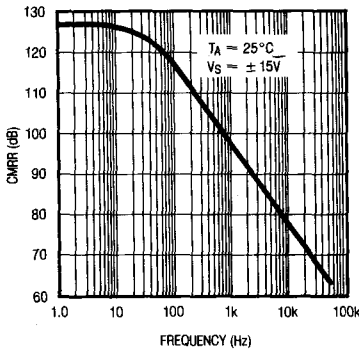
**Total Input Noise Voltage
vs Frequency**



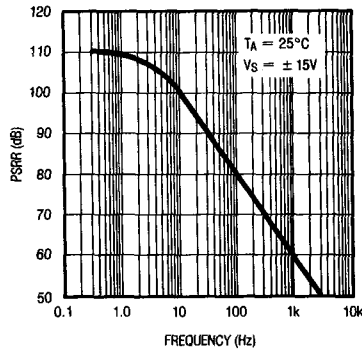
**Open-Loop
Frequency Response**



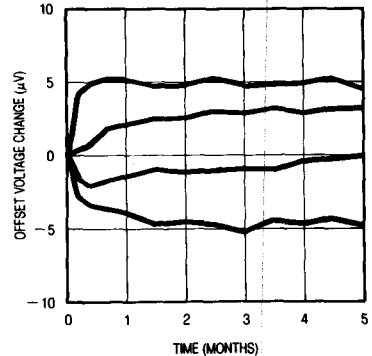
**Common Mode Rejection Ratio
vs Frequency**



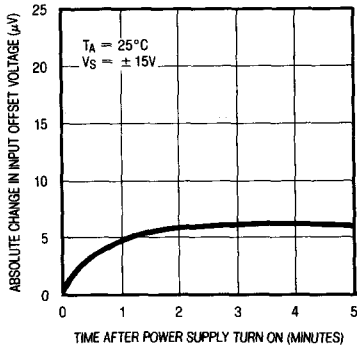
**Power Supply Rejection Ratio
vs Frequency**



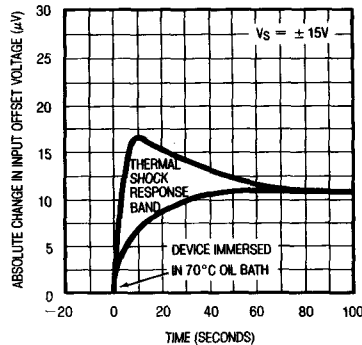
**Long Term Stability of Four
Representative Units**



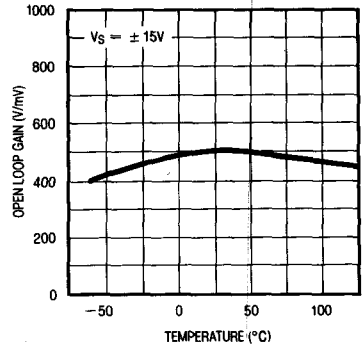
Warm-Up Drift



**Offset Voltage Change Due
to Thermal Shock**

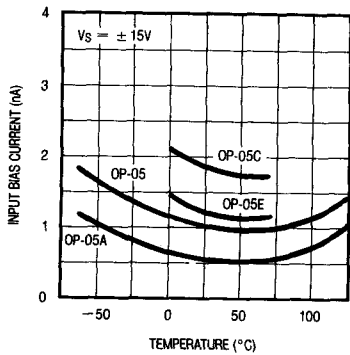


**Open-Loop Gain vs
Temperature**

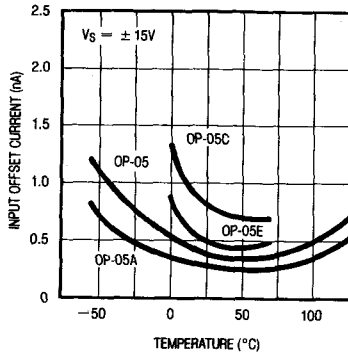


TYPICAL PERFORMANCE CHARACTERISTICS

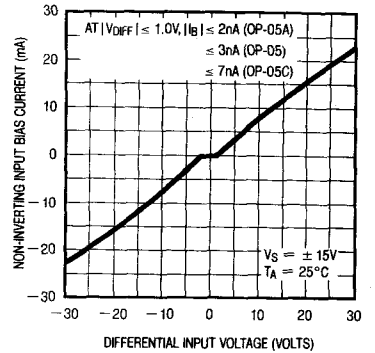
Input Bias Current vs Temperature



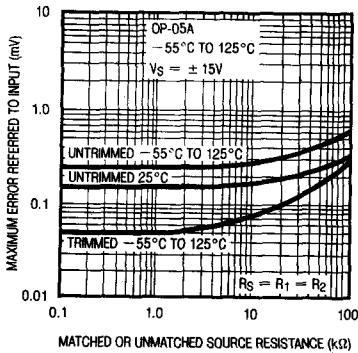
Input Offset Current vs Temperature



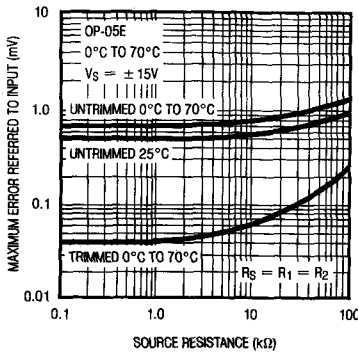
Input Bias Current vs Differential Input Voltage



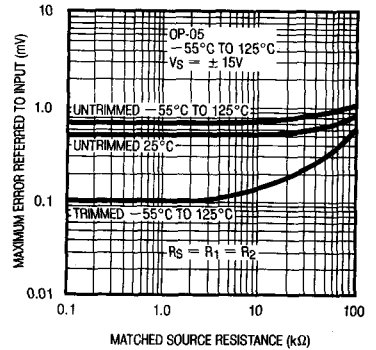
Maximum Error vs Source Resistance



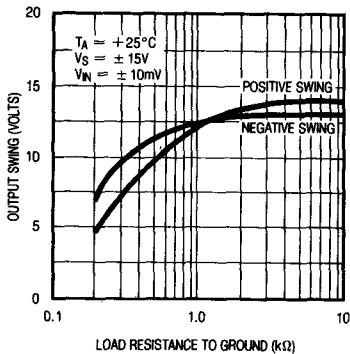
Maximum Error vs Source Resistance



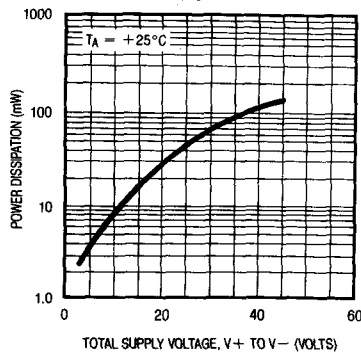
Maximum Error vs Source Resistance



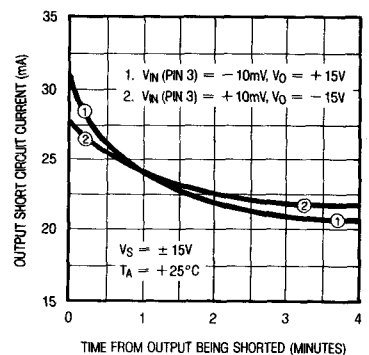
Output Voltage vs Load Resistance



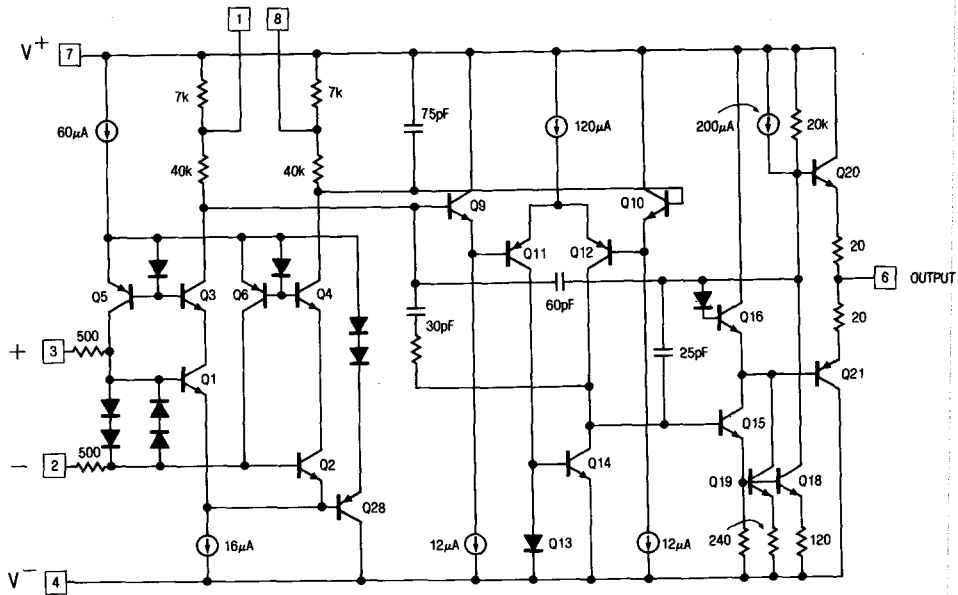
Power Consumption vs Power Supply



Output Short-Circuit Current vs Time



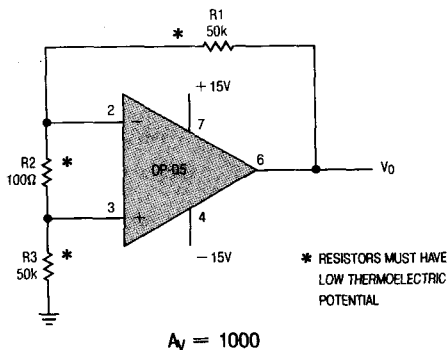
SCHEMATIC DIAGRAM



2

TEST CIRCUIT DIAGRAMS

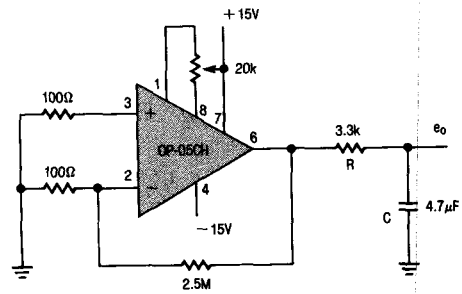
Offset Voltage Test Circuit †



* RESISTORS MUST HAVE LOW THERMOELECTRIC POTENTIAL

† This circuit is also used as the burn-in configuration with supply voltages changed to $\pm 20V$, $R1 = R3 = 10k$, $R2 = 200k$, $A_v = 100$.

Offset Nulling and Low Frequency Noise Test Circuit



NOTES:

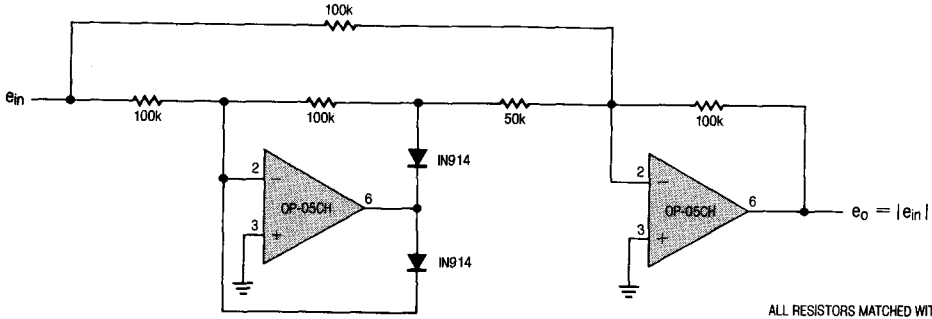
- 1) RC APPROXIMATELY 10Hz FILTER
 - 2) OBSERVE OUTPUT FOR 10 SECONDS
- $A_v = 25000$

Application Tip

When the OP-05 is used as a replacement in 725, 108/108A, 308/308A applications, removal of external compensation is optional. For conventionally nulled 741 type applications, external trimming should be removed. Care should be taken to avoid thermocouple voltages caused by temperature variations between the input terminals or dissimilar metals.

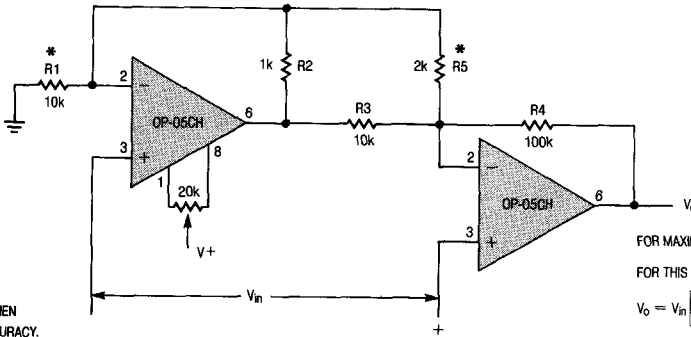
TYPICAL APPLICATIONS

Precision Absolute Value Circuit



ALL RESISTORS MATCHED WITHIN 0.1%

Two Op-Amp Instrumentation Amplifier



* ADJUST R1 FOR CMRR. THEN
ADJUST R5 FOR GAIN ACCURACY.
R5 DOES NOT AFFECT CMRR.

FOR MAXIMUM CMRR, $\frac{R2}{R1} = \frac{R3}{R4}$

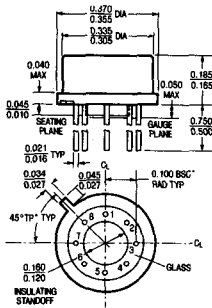
FOR THIS CONDITION,

$$V_o = V_{in} \left[\frac{R4}{R3} \right] \left[1 + \frac{R2}{R1} + \frac{R2 + R3}{R5} \right]$$

$$\frac{V_o}{V_{in}} = 210 \text{ FOR VALUES SHOWN}$$

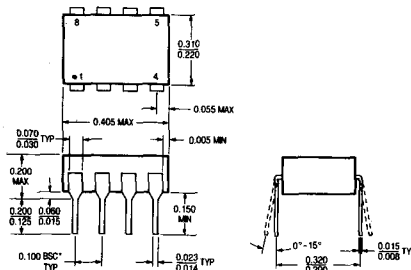
PACKAGE DESCRIPTION

**H Package
Metal Can**



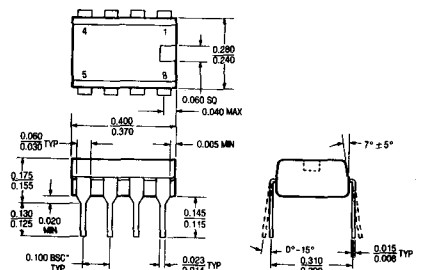
T_{jmax}	θ_{ja}	θ_{jc}
150°C	150°C/W	45°C/W

**J8 Package
8 Lead Hermetic Dip**



T_{jmax}	θ_{ja}
150°C	100°C/W

**N8 Package
8 Lead Plastic**



T_{jmax}	θ_{ja}
100°C	130°C/W

FEATURES

- *Guaranteed 25 μ V max. Offset Voltage*
- *Guaranteed 0.6 μ V/ $^{\circ}$ C max. Offset Voltage Drift with Temperature*
- *Excellent 1.0 μ V/Month max. Long Term Stability*
- *Guaranteed 0.6 μ V_{p-p} max. Noise*
- *Guaranteed 2.0nA max. Input Bias Current*

APPLICATIONS

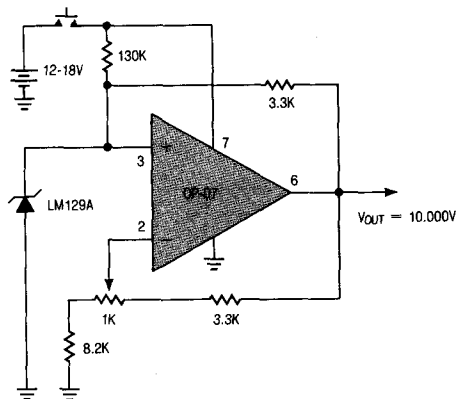
- Thermocouple Amplifiers
- Strain Gauge Amplifiers
- Low Level Signal Processing
- Medical Instrumentation

DESCRIPTION

The OP-07 offers excellent performance in applications requiring low offset voltage, low drift with time and temperature and very low noise. Linear's OP-07 is interchangeable with many of the precision op-amp device types. The OP-07 also offers a wide input voltage range, high common mode rejection and low input bias current. These features result in optimum performance for small signal level and low frequency applications. Use of advanced design, processing and testing techniques make Linear's OP-07 a superior choice over similar products. A buffered reference application is shown below. For single op amp applications requiring higher performance, see the LT1001 and for matched dual precision applications see the LT1002.

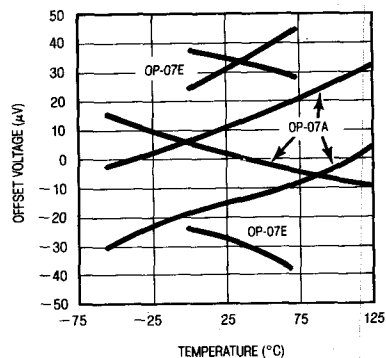
2

Precision Buffered Single Supply Reference



The OP-07 contributes less than 5% of the total drift with temperature, noise and long term drift of the reference application.

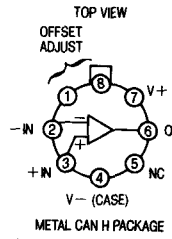
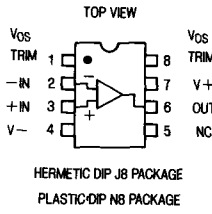
**Offset Voltage Drift With Temperature
Of Representative Units**



ABSOLUTE MAXIMUM RATINGS

Supply Voltage..... ± 22V
 Differential Input Voltage..... ± 30V
 Input Voltage Equal to Supply Voltage
 Output Short Circuit Duration..... Indefinite
 Operating Temperature Range
 OP-07/OP-07A..... -55°C to 125°C
 OP-07E/OP-07C..... 0°C to 70°C
 Storage Temperature Range
 All Devices..... -65°C to 150°C
 Lead Temperature (Soldering, 10 sec.)..... 300°C

PACKAGE/ORDER INFORMATION

 <p>TOP VIEW OFFSET ADJUST METAL CAN H PACKAGE</p>	ORDER PART NO.	OFFSET VOLTAGE (MAX)
	OP-07AH OP-07H OP-07EH OP-07CH	25µV 75µV 75µV 150µV
 <p>TOP VIEW HERMETIC DIP J8 PACKAGE PLASTIC-DIP N8 PACKAGE</p>	ORDER PART NO.	OFFSET VOLTAGE (MAX)
	OP-07AJ8 OP-07J8 OP-07EJ8 OP-07CJ8 OP-07EN8 OP-07CN8	25µV 75µV 75µV 150µV 75µV 150µV

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $T_A = 25^\circ C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	OP-07A			OP-07			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	(Note 1)		10	25		30	75	µV
$\frac{\Delta V_{OS}}{\Delta Time}$	Long Term Input Offset Voltage Stability	(Notes 2 and 3)		0.2	1.0		0.2	1.0	µV/Month
I_{OS}	Input Offset Current			0.3	2.0		0.4	2.8	nA
I_B	Input Bias Current			± 0.7	± 2.0		± 1.0	± 3.0	nA
e_n	Input Noise Voltage	0.1Hz to 10Hz (Note 2)		0.35	0.6		0.35	0.6	µV _{rms}
	Input Noise Voltage Density	$f_o = 10Hz$ $f_o = 100Hz$ (Note 2) $f_o = 1000Hz$		10.3 10.0 9.6	18.0 13.0 11.0		10.3 10.0 9.6	18.0 13.0 11.0	nV/√Hz
i_n	Input Noise Current	0.1Hz to 10Hz (Note 2)		14	30		14	30	pA _{rms}
	Input Noise Current Density	$f_o = 10Hz$ $f_o = 100Hz$ (Note 2) $f_o = 1000Hz$		0.32 0.14 0.12	0.80 0.23 0.17		0.32 0.14 0.12	0.80 0.23 0.17	pA/√Hz
R_{in}	Input Resistance Differential Mode	(Note 4)	30	80		20	60		MΩ
	Input Resistance Common Mode			200			200		GΩ
	Input Voltage Range		± 13.5	± 14.0		± 13.5	± 14.0		V
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 13V$	110	126		110	126		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 3V$ to ± 18V	100	108		100	108		dB
A_{VOL}	Large Signal Voltage Gain	$R_L \geq 2k\Omega$, $V_O = \pm 10V$ $R_L \geq 500\Omega$, $V_O = \pm 0.5V$ $V_S = \pm 3V$ (Note 4)	300 150	500 400		200 150	500 400		V/mV
V_{OUT}	Maximum Output Voltage Swing	$R_L \geq 10k\Omega$ $R_L \geq 2k\Omega$ $R_L \geq 1k\Omega$	± 12.5 ± 12.0 ± 10.5	± 13.0 ± 12.8 ± 12.0		± 12.5 ± 12.0 ± 10.5	± 13.0 ± 12.8 ± 12.0		V
SR	Slew Rate	$R_L \geq 2k\Omega$ (Note 4)	0.1	0.25		0.1	0.25		V/µs
GBW	Closed Loop Bandwidth	$A_{VOL} = +1$ (Note 4)	0.4	0.6		0.4	0.6		MHz
Z_o	Open Loop Output Impedance	$V_O = 0$, $I_O = 0$, $f = 10Hz$		60			60		Ω
P_d	Power Dissipation	$V_S = \pm 15V$		75	120		75	120	mW
		$V_S = \pm 3V$		4	6		4	6	
	Offset Adjustment Range	Null Pot = 20kΩ		± 4			± 4		mV

See Notes on page 2-332

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $-55^\circ C \leq T_A \leq 125^\circ C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	OP-07A			OP-07			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	(Note 1)	●	25	60	60	200	μV	
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Input Offset Voltage Drift Without External Trim With External Trim	Null Pot = 20k Ω (Note 2)	●	0.2	0.6	0.3	1.3	$\mu V/^\circ C$	
I_{OS}	Input Offset Current		●	0.8	4.0	1.2	5.6	nA	
$\frac{\Delta I_{OS}}{\Delta Temp}$	Average Input Offset Current Drift	(Note 2)	●	5	25	8	50	pA/°C	
I_B	Input Bias Current		●	± 1.0	± 4.0	± 2.0	± 6.0	nA	
$\frac{\Delta I_B}{\Delta Temp}$	Average Input Bias Current Drift	(Note 2)	●	8	25	13	50	pA/°C	
	Input Voltage Range		●	± 13.0	± 13.5	± 13.0	± 13.5	V	
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 13V$	●	106	123	106	123	dB	
PSRR	Power Supply Rejection Ratio	$V_S = \pm 3V$ to $\pm 18V$	●	94	106	94	106	dB	
A_{VOL}	Large Signal Voltage Gain	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	●	200	400	150	400	V/mV	
V_{OUT}	Output Voltage Swing	$R_L \geq 2k\Omega$	●	± 12.0	± 12.6	± 12.0	± 12.6	V	

2

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $T_A = 25^\circ C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	OP-07E			OP-07C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	(Note 1)		30	75	60	150	μV	
$\frac{\Delta V_{OS}}{\Delta Time}$	Long Term Input Offset Voltage Stability	(Notes 2 and 3)		0.3	1.5	0.4	2.0	$\mu V/$ Month	
I_{OS}	Input Offset Current			0.5	3.8	0.8	6.0	nA	
I_B	Input Bias Current			± 1.2	± 4.0	± 1.8	± 7.0	nA	
e_n	Input Noise Voltage	0.1Hz to 10Hz (Note 2)		0.35	0.6	0.35	0.65	μV_{P-P}	
	Input Noise Voltage Density	$f_o = 10Hz$ $f_o = 100Hz$ (Note 2) $f_o = 1000Hz$		10.3	18.0	10.5	20.0	nV/ \sqrt{Hz}	
i_n	Input Noise Current	0.1Hz to 10Hz (Note 2)		14	30	15	35	pA _{P-P}	
	Input Noise Current Density	$f_o = 10Hz$ $f_o = 100Hz$ (Note 2) $f_o = 1000Hz$		0.32	0.80	0.32	0.90	pA/ \sqrt{Hz}	
R_{in}	Input Resistance Differential Mode	(Note 4)		15	50	8	33	M Ω	
	Input Resistance Common Mode				160		120	G Ω	
	Input Voltage Range			± 13.5	± 14.0	± 13.0	± 14.0	V	
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 13V$		106	123	100	120	dB	
PSRR	Power Supply Rejection Ratio	$V_S = \pm 3V$ to $\pm 18V$		94	106	90	104	dB	
A_{VOL}	Large Signal Voltage Gain	$R_L \geq 2k\Omega$, $V_O = \pm 10V$ $R_L \geq 500\Omega$, $V_O = \pm 0.5V$ $V_S = \pm 3V$ (Note 4)		200	500	120	400	V/mV	
V_O	Maximum Output Voltage Swing	$R_L \geq 10k\Omega$ $R_L \geq 2k\Omega$ $R_L \geq 1k\Omega$		± 12.5	± 13.0	± 12.5	± 13.0	V	
SR	Slewing Rate	$R_L \geq 2k\Omega$ (Note 2)		0.1	0.25	0.1	0.25	V/ μS	
GBW	Closed Loop Bandwidth	$A_{VOL} = +1$ (Note 2)		0.4	0.6	0.4	0.6	MHz	
Z_o	Open Loop Output Impedance	$V_O = 0$, $I_O = 0$, $f = 10Hz$			60		60	Ω	
P_d	Power Dissipation	$V_S = \pm 15V$ $V_S = \pm 3V$		75	120	80	150	mW	
	Offset Adjustment Range	Null Pot = 20k Ω		± 4		± 4		mV	

See Notes on page 2-332

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $0^\circ C \leq T_A \leq 70^\circ C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	OP-07E			OP-07C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage		●	45	130		85	250	μV
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Input Offset Voltage Drift Without External Trim With External Trim	Null Pot = 20k Ω (Note 2)	●	0.3 0.3	1.3 1.3		0.5 0.4	1.8 1.6	$\mu V/^\circ C$
I_{OS}	Input Offset Current		●	0.9	5.3		1.6	8.0	nA
$\frac{\Delta I_{OS}}{\Delta Temp}$	Average Input Offset Current Drift	(Note 2)	●	8	35		12	50	$\mu A/^\circ C$
I_B	Input Bias Current		●	± 1.5	± 5.5		± 2.2	± 9.0	nA
$\frac{\Delta I_B}{\Delta Temp}$	Average Input Bias Current Drift	(Note 2)	●	13	35		18	50	$\mu A/^\circ C$
	Input Voltage Range		●	± 13.0	± 13.5		± 13.0	± 13.5	V
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 13V$	●	103	123		97	120	dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 3V$ to $\pm 18V$	●	90	104		86	100	dB
A_{VOL}	Large Signal Voltage Gain	$R_L \geq 2k\Omega$, $V_o = \pm 10V$	●	180	450		100	400	V/mV
V_{OUT}	Output Voltage Swing	$R_L \geq 2k\Omega$	●	± 12.0	± 12.6		± 11.0	± 12.6	V

The ● denotes the specifications which apply over full operating temperature range.

For MIL-STD components, please refer to LTC 883C data sheet for test listing and parameters.

Note 1: Offset voltage for the OP-07A is measured 60 seconds after power is applied. All other grades are measured with high speed test equipment, approximately 1 second after power is applied.

Note 2: This parameter is tested on a sample basis only.

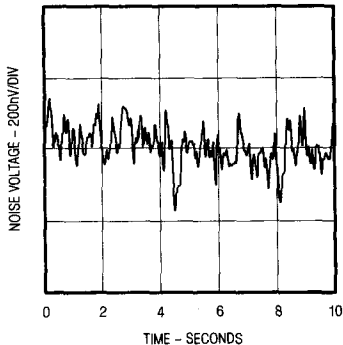
Note 3: Long term Input Offset Voltage Stability refers to the averaged trend line of V_{OS} versus Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically $2.5\mu V$.

Note 4: This parameter is guaranteed by design.

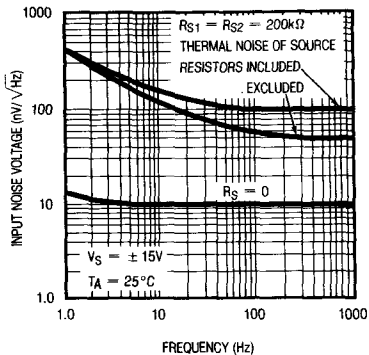
Note 5: The OP-07D is available by special request.

TYPICAL PERFORMANCE CHARACTERISTICS

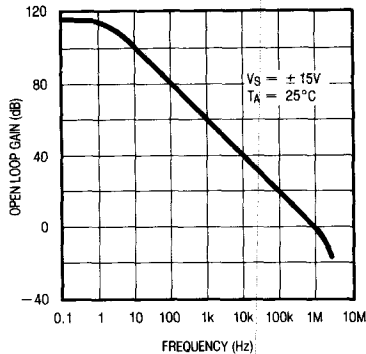
Low Frequency Noise
(Closed Loop Gain = 25,000)



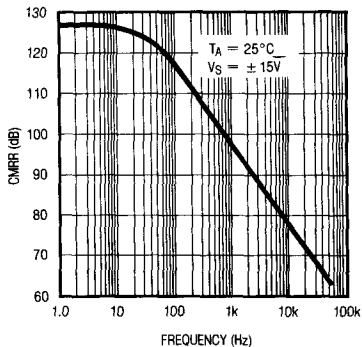
Total Input Noise Voltage vs Frequency



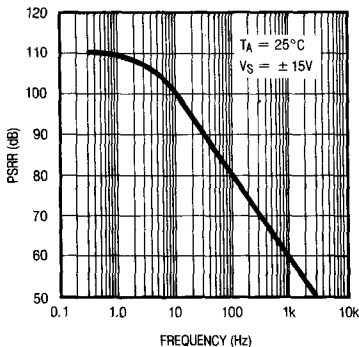
Open-Loop Frequency Response



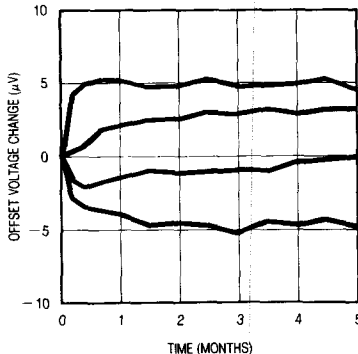
Common Mode Rejection Ratio vs Frequency



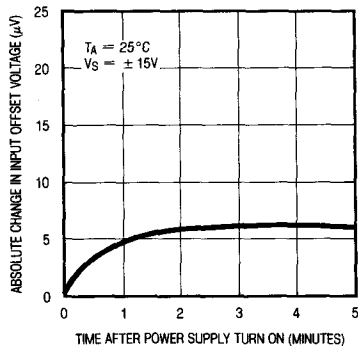
Power Supply Rejection Ratio vs Frequency



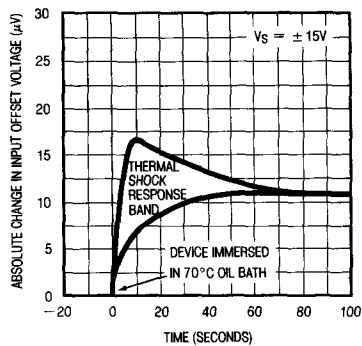
Long Term Stability of Four Representative Units



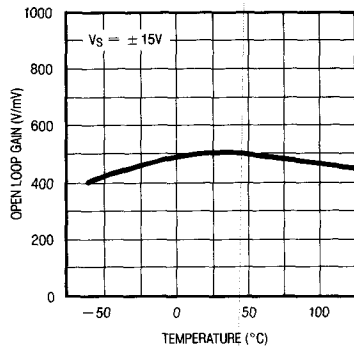
Warm-Up Drift



Offset Voltage Change Due to Thermal Shock



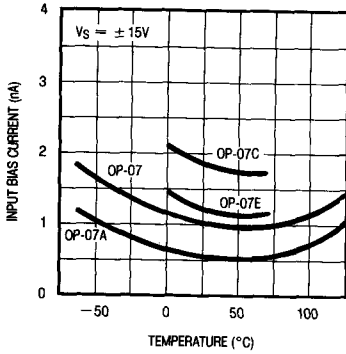
Open-Loop Gain vs Temperature



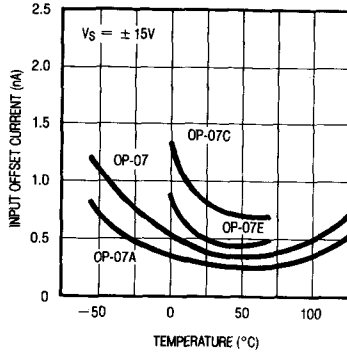
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TYPICAL PERFORMANCE CHARACTERISTICS

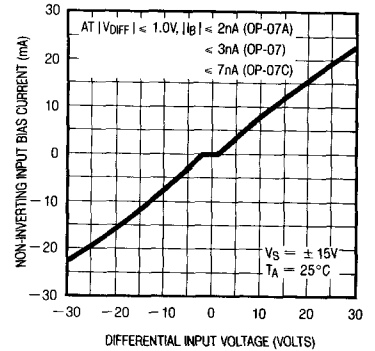
Input Bias Current vs Temperature



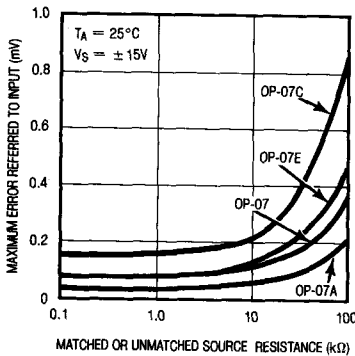
Input Offset Current vs Temperature



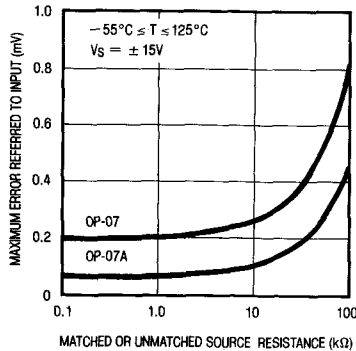
Input Bias Current vs Differential Input Voltage



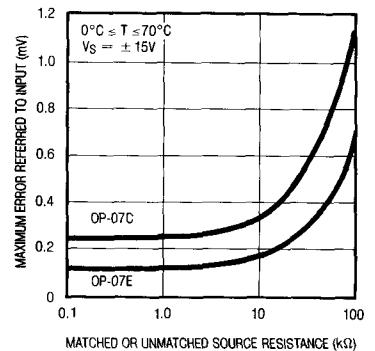
Maximum Error vs Source Resistance



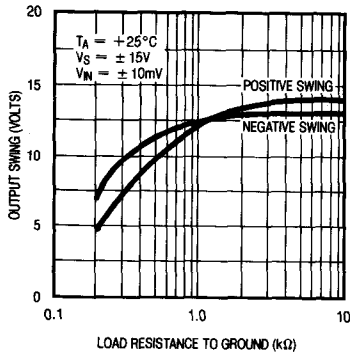
Maximum Error vs Source Resistance



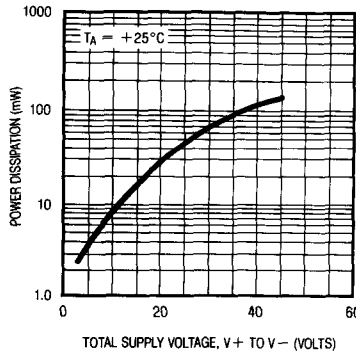
Maximum Error vs Source Resistance



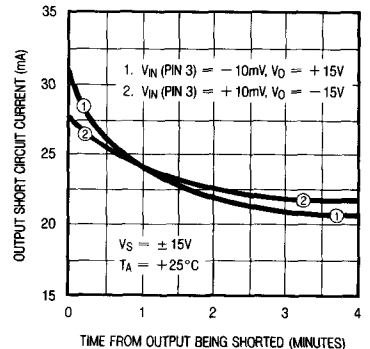
Output Voltage vs Load Resistance



Power Consumption vs Power Supply

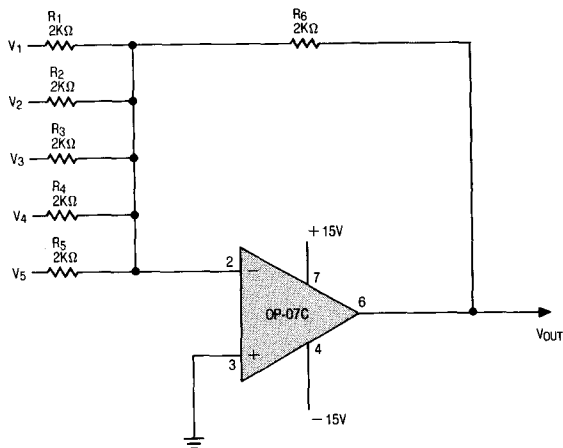


Output Short-Circuit Current vs Time

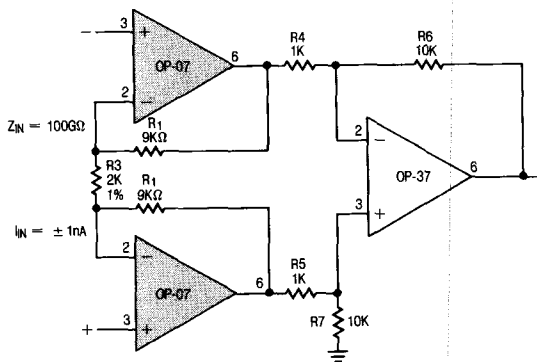


TYPICAL APPLICATIONS

Precision Summing Amplifier



Instrumentation Amplifier



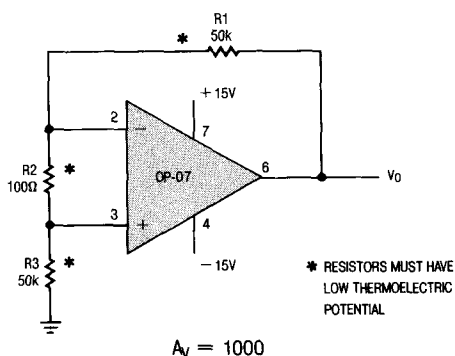
$$A_v = \frac{R6}{R4} \left(\frac{2R1}{R3} + 1 \right)$$

$$A_v = 100$$

2

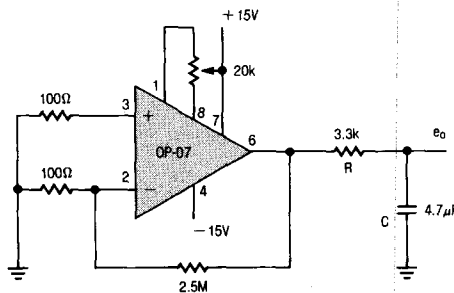
TEST CIRCUIT DIAGRAMS

Offset Voltage Test Circuit †



$$A_v = 1000$$

Offset Nulling and Low Frequency Noise Test Circuit



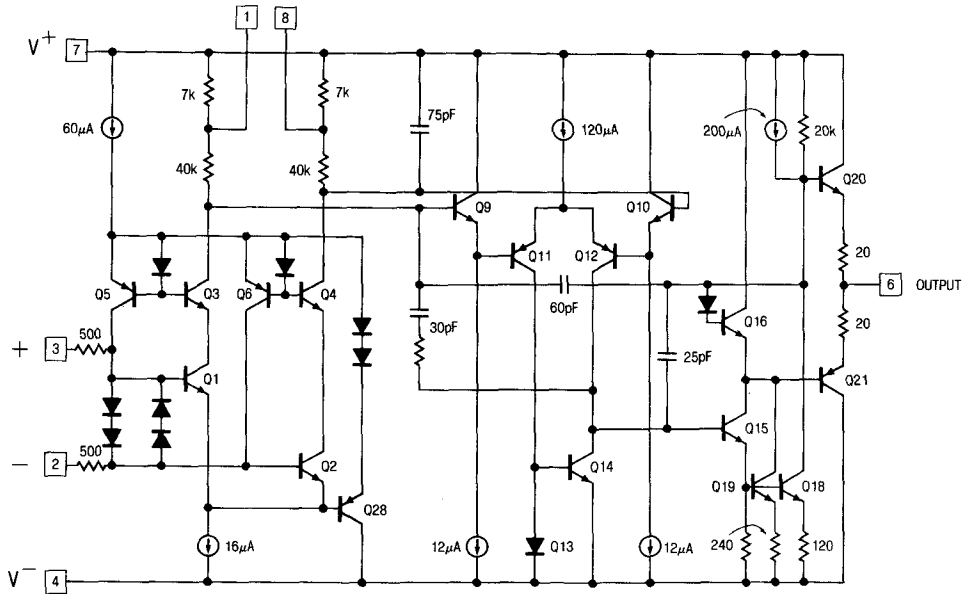
NOTES:

- 1) RC APPROXIMATELY 10Hz FILTER
 - 2) OBSERVE OUTPUT FOR 10 SECONDS
- $$A_v = 25000$$

Application Tip:

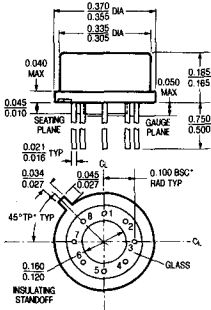
When the OP-07 is used as a replacement in 725, 108/108A, 308/308A applications, removal of external compensation is optional. For conventionally nulled 741 type applications, external trimming should be removed. Care should be taken to avoid thermocouple voltages caused by temperature variations between the input terminals or dissimilar metals.

SCHEMATIC DIAGRAM



PACKAGE DESCRIPTION

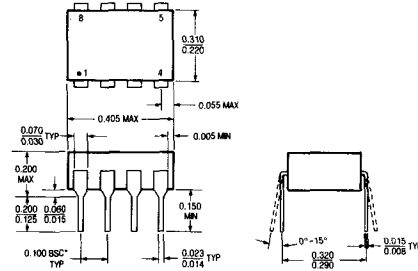
H Package
Metal Can



NOTE: DIMENSIONS IN INCHES

T_j max	θ_{ja}	θ_{jc}
150°C	150°C/W	45°C/W

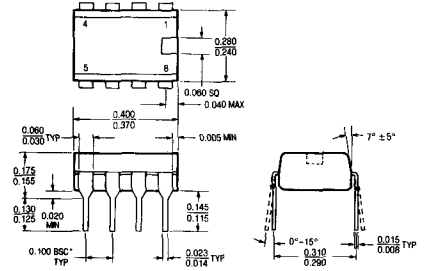
J8 Package
8 Lead Hermetic Dip



NOTE: DIMENSIONS IN INCHES UNLESS OTHERWISE NOTED.
*LEADS WITHIN 0.007 OF TRUE POSITION (TP) AT GAUGE PLANE

T_j max	θ_{ja}
150°C	100°C/W

N8 Package
8 Lead Plastic



NOTE: DIMENSIONS IN INCHES UNLESS OTHERWISE NOTED.
*LEADS WITHIN 0.007 OF TRUE POSITION (TP) AT GAUGE PLANE.

T_j max	θ_{ja}
100°C	130°C/W

FEATURES

- *Guaranteed 150 μ V max. Offset Voltage*
- *Guaranteed 1.8 μ V/ $^{\circ}$ C max. Offset Voltage Drift with Temperature*
- *Excellent 2.0 μ V/Month max. Long Term Stability*
- *Guaranteed 0.65 μ Vp-p max. Noise*
- *Guaranteed 7nA max. Input Bias Current*

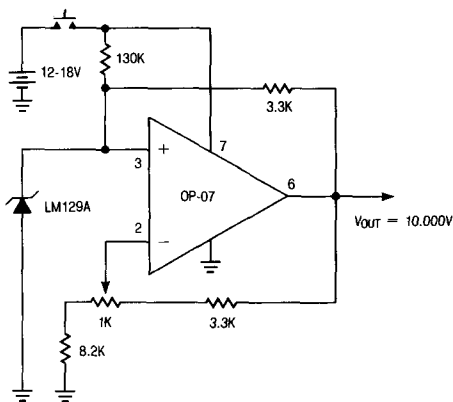
APPLICATIONS

- Thermocouple Amplifiers
- Strain Gauge Amplifiers
- Low Level Signal Processing
- Medical Instrumentation

DESCRIPTION

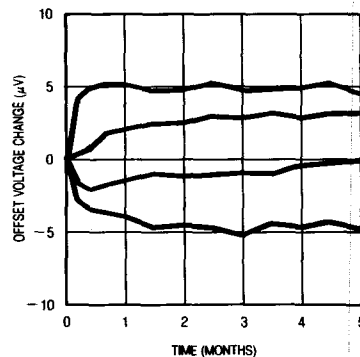
The OP-07 offers excellent performance in applications requiring low offset voltage, low drift with time and temperature and very low noise. Linear's OP-07 is interchangeable with many of the precision op amp device types. The OP-07 also offers a wide input voltage range, high common-mode rejection and low input bias current. These features result in optimum performance for small signal level and low frequency applications. Use of advanced design, processing and testing techniques make Linear's OP-07 a superior choice over similar products. A buffered reference application is shown below. For single op amp applications requiring higher performance in the SO package, see the LT1001CS8.

Precision Buffered Single Supply Reference



The OP-07 contributes less than 5% of the total drift with temperature, noise and long term drift of the reference application.

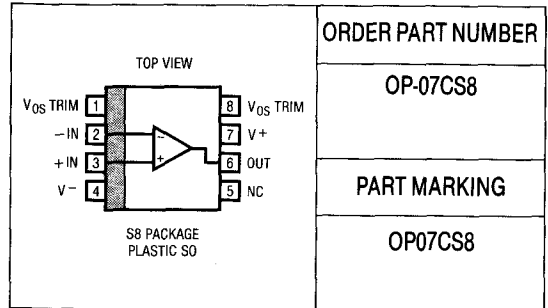
Long Term Stability of Four Representative Units



ABSOLUTE MAXIMUM RATINGS

Supply Voltage ± 22V
 Differential Input Voltage ± 30V
 Input Voltage Equal to Supply Voltage
 Output Short Circuit Duration Indefinite
 Operating Temperature Range 0°C to 70°C
 Storage Temperature Range
 All Devices - 65°C to 150°C
 Lead Temperature (Soldering, 10 sec.) 300°C

PACKAGE/ORDER INFORMATION



ELECTRICAL CHARACTERISTICS $V_S = \pm 15V, T_A = 25^\circ C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	OP-07CS8			UNITS
			MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	(Note 1)		60	150	μV
$\frac{\Delta V_{OS}}{\Delta Time}$	Long Term Input Offset Voltage Stability	(Notes 2 and 3)		0.4	2.0	$\mu V/$ Month
I_{OS}	Input Offset Current			0.8	6.0	nA
I_B	Input Bias Current			± 1.8	± 7.0	nA
e_n	Input Noise Voltage	0.1Hz to 10Hz (Note 2)		0.35	0.65	μV_{p-p}
	Input Noise Voltage Density	$f_O = 10Hz$		10.5	20.0	nV/ \sqrt{Hz}
		$f_O = 100Hz$ (Note 2)		10.2	13.5	nV/ \sqrt{Hz}
		$f_O = 1000Hz$		9.8	11.5	nV/ \sqrt{Hz}
I_n	Input Noise Current	0.1Hz to 10Hz (Note 2)		15	35	pA $_{p-p}$
	Input Noise Current Density	$f_O = 10Hz$		0.32	0.90	pA/ \sqrt{Hz}
		$f_O = 100Hz$ (Note 2)		0.15	0.27	pA/ \sqrt{Hz}
		$f_O = 1000Hz$		0.13	0.18	pA/ \sqrt{Hz}
R_{in}	Input Resistance Differential Mode	(Note 4)	8	33		M Ω
	Input Resistance Common-Mode			120		G Ω
	Input Voltage Range		± 13.0	± 14.0		V
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm 13V$	100	120		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 3V$ to $\pm 18V$	90	104		dB
A_{VOL}	Large Signal Voltage Gain	$R_L = 2k\Omega, V_O = \pm 10V$	120	400		V/mV
		$R_L = 500\Omega, V_O = \pm 0.5V$ $V_S = \pm 3V$ (Note 4)	100	400		V/mV
V_O	Maximum Output Voltage Swing	$R_L = 10k\Omega$	± 12.5	± 13.0		V
		$R_L \geq 2k\Omega$	± 11.5	± 12.8		V
		$R_L \geq 1k\Omega$		± 12.0		V
SR	Slewing Rate	$R_L \geq 2k\Omega$ (Note 2)	0.1	0.25		V/ μs
GBW	Closed Loop Bandwidth	$A_{VOL} = +1$ (Note 2)	0.4	0.6		MHz
Z_o	Open Loop Output Impedance	$V_O = 0, I_o = 0, f = 10Hz$		60		Ω
P_d	Power Dissipation	$V_S = \pm 15V$	80	150		mW
		$V_S = \pm 3V$	4	8		mW
	Offset Adjustment Range	Null Pot = 20k Ω		± 4		mV

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V, 0^\circ C \leq T_A \leq 70^\circ C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	OP-07CS8			UNITS
			MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	●		85	250	μV
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Input Offset Voltage Drift Without External Trim With External Trim	Null Pot = 20k Ω (Note 2) ●		0.5 0.4	1.8 1.6	$\mu V/^\circ C$ $\mu V/^\circ C$
I_{OS}	Input Offset Current	●		1.6	8.0	nA
$\frac{\Delta I_{OS}}{\Delta Temp}$	Average Input Offset Current Drift	(Note 2) ●		12	50	pA/°C
I_B	Input Bias Current	●		± 2.2	± 9.0	nA
$\frac{\Delta I_B}{\Delta Temp}$	Average Input Bias Current Drift	(Note 2) ●		18	50	pA/°C
	Input Voltage Range	●	± 13.0	± 13.5		V
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm 13V$ ●	97	120		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 3V$ to $\pm 18V$ ●	86	100		dB
A_{VOL}	Large Signal Voltage Gain	$R_L \geq 2k\Omega, V_o = \pm 10V$ ●	100	400		V/mV
V_{OUT}	Output Voltage Swing	$R_L \geq 2k\Omega$ ●	± 11.0	± 12.6		V

The ● denotes specifications which apply over the full operating temperature range.

Note 1: Offset voltage is measured with high speed test equipment, approximately 1 second after power is applied.

Note 2: This parameter is tested on a sample basis only.

Note 3: Long Term Input Offset Voltage Stability refers to the averaged trend line of V_{OS} versus Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically 2.5 μV .

Note 4: This parameter is guaranteed by design.

NOTES

FEATURES

- Improved Specifications Compared to LF155/156 Devices
- *Guaranteed* Low Offset Voltage 500 μ V Max.
- *Guaranteed* Low Offset Drift 5 μ V/ $^{\circ}$ C Max.
- *Guaranteed* Bias Current Fully Warmed-Up over Temperature
- OP-15: LF156 Speed with LF155 Power Dissipation
 - Guaranteed* Supply Current 4mA Max.
 - Guaranteed* Slew Rate 10V/ μ s Min.
- OP-16:
 - Guaranteed* Faster Slew Rate 18V/ μ s Min.
 - No High Frequency Oscillation at Cold Temperatures
- No Phase Reversal when Negative Common-Mode Limit is Exceeded

APPLICATIONS

- Long Term Precision Integration
- Current to Voltage Conversion
- Medical Instrumentation—CAT Scanner
- High Speed, Precision Sample and Hold

DESCRIPTION

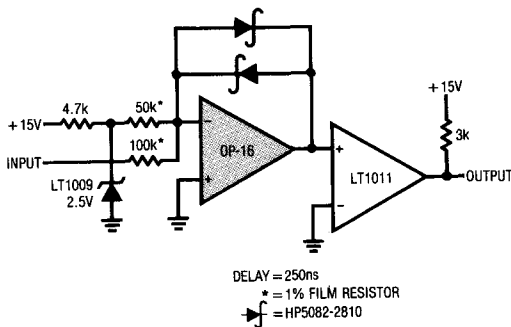
The OP-15/16 series devices feature distinct advantages over other JFET-input operational amplifiers, in particular compared to LF155/156 types.

The OP-15 has the speed of the LF156 design with the low power dissipation of the slower LF155. The OP-16 is considerably faster. Both devices offer offset voltages as low as 0.5mV, with guaranteed drift of 5 μ V/ $^{\circ}$ C. Input bias current at 125 $^{\circ}$ C is just a few nanoamperes.

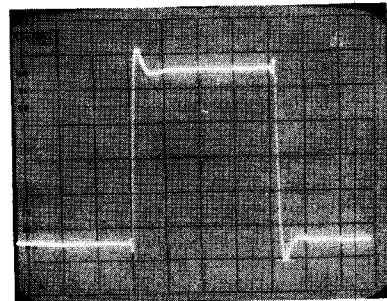
Other manufacturers' OP-15/16 (and LF155/156) exhibit phase reversal at the output when the negative common-mode limit at the input is exceeded; i.e., driving from -12V to -15V with \pm 15V supplies. This can cause lock-up in servo systems. As shown in the application section, Linear Technology's OP-15/16 does not have this problem due to unique phase reversal protection circuitry.

In addition, Linear's OP-16 is free from high frequency oscillation problems at cold temperatures, as is illustrated in the "Voltage Follower Small Signal Pulse Response" photo. For applications requiring higher performance, see the LT1022, LT1055 and LT1056 data sheets.

Fast, 12-Bit Current Comparator



Voltage Follower Small Signal Pulse Response
 $T_A = -55^{\circ}\text{C}$



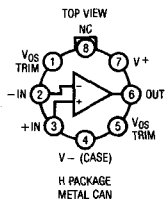
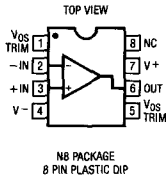
$C_L = 100\text{pF}$
VERTICAL SCALE = 20mV/DIV
HORIZONTAL SCALE = 0.2 μ s/DIV

OP-15/OP-16

ABSOLUTE MAXIMUM RATINGS

Supply Voltage		
A, B, E, F Grades	± 22V
C, G Grades	± 18V
Internal Power Dissipation	500mW
Operating Temperature Range		
A, B, C Grades	-55°C to 125°C
E, F, G Grades	0°C to 70°C
Junction Temperature	150°C
Differential Input Voltage		
A, B, E, F Grades	± 40V
C, G Grades	± 30V
Input Voltage (Note 4)		
A, B, E, F Grades	± 20V
C, G Grades	± 16V
Output Short Circuit Duration	Indefinite
Storage Temperature Range	-65°C to 150°C
Lead Temperature (Soldering, 10 sec.)	300°C

PACKAGE/ORDER INFORMATION

		ORDER PART NUMBER	
 <p>TOP VIEW NC (8) V_{OS} TRIM (1) -IN (2) +IN (3) V_S TRIM (5) V- (CASE) (4) V+ (7) OUT (6)</p>	OP-15AH	OP-16AH	
	OP-15BH	OP-16BH	
	OP-15CH	OP-16CH	
	OP-15EH	OP-16EH	
	OP-15FH	OP-16FH	
	OP-15GH	OP-16GH	
 <p>TOP VIEW V_{OS} TRIM (1) -IN (2) +IN (3) V- (4) NC (8) V+ (7) OUT (6) V_S TRIM (5)</p>	OP-15GN8	OP-16GN8	
	V _{OS} is adjusted with a potentiometer ranging from 10k to 1M. The wiper is connected to V ⁺		

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V, T_A = 25^\circ C$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	OP-15A/E OP-16A/E			OP-15B/F OP-16B/F			OP-15C/G OP-16C/G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V _{OS}	Input Offset Voltage	R _S = 50Ω	—	0.2	0.5	—	0.4	1.0	—	0.5	3.0	mV
I _{OS}	Input Offset Current	T _J = 25°C (Note 1) Warmed-Up	—	3	10	—	6	20	—	12	50	pA
		OP-15	—	5	22	—	10	40	—	20	100	pA
		OP-16	—	5	25	—	10	50	—	20	125	pA
I _B	Input Bias Current	T _J = 25°C (Note 1) Warmed-Up	—	± 15	± 50	—	± 30	± 100	—	± 60	± 200	pA
		OP-15	—	± 18	± 110	—	± 40	± 200	—	± 80	± 400	pA
		OP-16	—	± 20	± 130	—	± 40	± 250	—	± 80	± 500	pA
R _{IN}	Input Resistance		—	10 ¹²	—	—	10 ¹²	—	—	10 ¹²	—	Ω
A _{VOL}	Large Signal Voltage Gain	R _L ≥ 2kΩ V _O = ± 10V	100	240	—	75	220	—	50	200	—	V/mV
V _O	Output Voltage Swing	R _L = 10kΩ R _L = 2kΩ	± 12	± 13	—	± 12	± 13	—	± 12	± 13	—	V
			± 11	± 12.7	—	± 11	± 12.7	—	± 11	± 12.7	—	V
I _S	Supply Current	OP-15	—	2.7	4.0	—	2.7	4.0	—	2.8	5.0	mA
		OP-16	—	4.6	7.0	—	4.6	7.0	—	4.8	8.0	mA
SR	Slew Rate	A _{VCL} = +1	10	13	—	7.5	11	—	5	9	—	V/μs
		OP-16	18	20	—	12	18	—	9	16	—	V/μs
GBW	Gain Bandwidth Product	(Note 3)	4.0	6.0	—	3.5	5.7	—	3.0	5.4	—	MHz
		OP-16	—	8.0	—	—	7.6	—	—	7.2	—	MHz
	Settling Time (Note 2)	to 0.01%	—	4.5	—	—	4.5	—	—	4.7	—	μs
		to 0.10%	—	1.2	—	—	1.2	—	—	1.3	—	μs
		to 0.01%	—	3.8	—	—	3.8	—	—	4.0	—	μs
		to 0.10%	—	0.9	—	—	0.9	—	—	1.0	—	μs
	Input Voltage Range		± 10.5	—	—	± 10.5	—	—	± 10.3	—	—	V
CMRR	Common-Mode Rejection Ratio	V _{CM} = ± 10.5V V _{CM} = ± 10.3V	86	100	—	86	100	—	—	—	—	dB
			—	—	—	—	—	—	82	96	—	dB
PSRR	Power Supply Rejection Ratio	V _S = ± 10V to ± 18V V _S = ± 10V to ± 15V	—	10	51	—	10	51	—	—	—	μV/V
			—	—	—	—	—	—	—	10	80	μV/V
e _n	Input Noise Voltage Density	f ₀ = 100Hz f ₀ = 1000Hz	—	20	—	—	20	—	—	20	—	nV/√Hz
			—	15	—	—	15	—	—	15	—	nV/√Hz
i _n	Input Noise Current Density	f ₀ = 100Hz f ₀ = 1000Hz	—	0.01	—	—	0.01	—	—	0.01	—	pA/√Hz
			—	0.01	—	—	0.01	—	—	0.01	—	pA/√Hz
C _{IN}	Input Capacitance		—	3	—	—	3	—	—	3	—	pF

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V, -55^\circ C \leq T_A \leq 125^\circ C$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	OP-15A OP-16A			OP-15B OP-16B			OP-15C OP-16C			UNITS	
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
V_{OS}	Input Offset Voltage	$R_S = 50\Omega$	●	—	0.4	0.9	—	0.7	2.0	—	0.9	4.5	mV
TCV_{OS}	Average Input Offset Voltage Drift Without External Trim		●	—	2	5	—	3	10	—	4	15	$\mu V/^\circ C$
			TCV_{OSn}	With External Trim	$R_P = 100k\Omega$	●	—	2	—	—	3	—	4
I_{OS}	Input Offset Current	$T_J = 125^\circ C$ (Note 1) $T_A = 125^\circ C$, Warmed-Up OP-15 OP-16	●	—	0.6	4.0	—	0.8	6.0	—	1.0	9.0	nA
			●	—	0.8	7.0	—	1.2	11	—	1.5	17	nA
			●	—	1.0	8.5	—	1.3	14.5	—	1.7	22	nA
I_B	Input Bias Current	$T_J = 125^\circ C$ (Note 1) $T_A = 125^\circ C$, Warmed-Up OP-15 OP-16	●	—	± 1.2	± 5.0	—	± 1.5	± 7.5	—	± 1.8	± 10	nA
			●	—	± 1.7	± 9.0	—	± 2.2	± 14	—	± 2.7	± 19	nA
			●	—	± 2.0	± 11	—	± 2.5	± 18	—	± 3.0	± 25	nA
	Input Voltage Range		●	± 10.4	—	—	± 10.4	—	—	± 10.25	—	—	V
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm 10.4V$ $V_{CM} = \pm 10.25V$	●	85	97	—	85	97	—	—	—	—	dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 10V$ to $\pm 18V$ $V_S = \pm 10V$ to $\pm 15V$	●	—	15	57	—	15	57	—	—	—	$\mu V/V$
			●	—	—	—	—	—	—	—	23	100	$\mu V/V$
A_{VOL}	Large Signal Voltage Gain	$R_L \geq 2k\Omega$ $V_O \geq 10V$	●	35	120	—	30	110	—	25	100	—	V/mV
V_O	Output Voltage Swing	$R_L \geq 10k\Omega$	●	± 12	± 13	—	± 12	± 13	—	± 12	± 13	—	V

2

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V, 0^\circ C \leq T_A \leq 70^\circ C$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	OP-15E OP-16E			OP-15F OP-16F			OP-15G OP-16G			UNITS	
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
V_{OS}	Input Offset Voltage	$R_S = 50\Omega$	●	—	0.3	0.75	—	0.55	1.5	—	0.7	3.8	mV
TCV_{OS}	Average Input Offset Voltage Drift Without External Trim		●	—	2	5	—	3	10	—	4	15	$\mu V/^\circ C$
			TCV_{OSn}	With External Trim	$R_P = 100k\Omega$	●	—	2	—	—	3	—	4
I_{OS}	Input Offset Current	$T_J = 70^\circ C$ (Note 1) $T_A = 70^\circ C$, Warmed-Up OP-15 OP-16	●	—	0.04	0.30	—	0.06	0.45	—	0.08	0.65	nA
			●	—	0.06	0.55	—	0.08	0.80	—	0.10	1.2	nA
			●	—	0.07	0.70	—	0.10	1.1	—	0.15	1.7	nA
I_B	Input Bias Current	$T_J = 70^\circ C$ (Note 1) $T_A = 70^\circ C$, Warmed-Up OP-15 OP-16	●	—	± 0.10	± 0.40	—	± 0.12	± 0.60	—	± 0.14	± 0.80	nA
			●	—	± 0.13	± 0.75	—	± 0.16	± 1.1	—	± 0.19	± 1.5	nA
			●	—	± 0.15	± 0.90	—	± 0.20	± 1.4	—	± 0.25	± 2.0	nA
	Input Voltage Range		●	± 10.4	—	—	± 10.4	—	—	± 10.25	—	—	V
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm 10.4V$ $V_{CM} = \pm 10.25V$	●	85	98	—	85	98	—	—	—	—	dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 10V$ to $\pm 18V$ $V_S = \pm 10V$ to $\pm 15V$	●	—	13	57	—	13	57	—	—	—	$\mu V/V$
			●	—	—	—	—	—	—	—	20	100	$\mu V/V$
A_{VO}	Large Signal Voltage Gain	$R_L \geq 2k\Omega$ $V_O \geq 10V$	●	65	200	—	50	180	—	35	160	—	V/mV
V_O	Output Voltage Swing	$R_L \geq 10k\Omega$	●	± 12	± 13	—	± 12	± 13	—	± 12	± 13	—	V

The ● denotes the specifications which apply over full operating temperature range.

For MIL-STD components, please refer to LTC 883C data sheet for test listing and parameters.

Note 1: Input bias current is specified for two different conditions. The T_J specification is with the junction at ambient temperature; the warmed-up specification is with the device operating in a warmed-up condition at the ambient temperature specified. I_B and I_{OS} are measured at $V_{CM} = 0$.

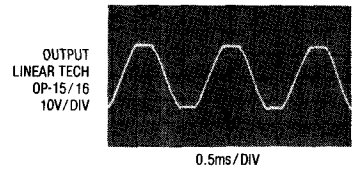
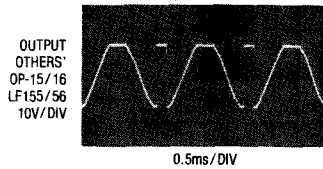
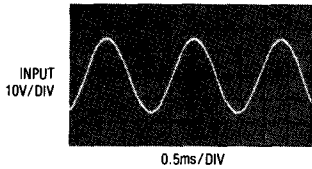
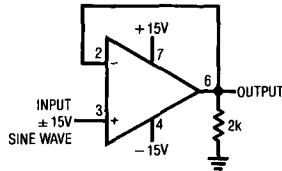
Note 2: Settling time is defined here for a unity gain inverter connection using $2k\Omega$ resistors. It is the time required for the error voltage (the voltage at the inverting input pin on the amplifier) to settle to within a specified percentage of its final value from the time a $10V$ step input is applied to the inverter.

Note 3: Sample tested.

Note 4: Unless otherwise specified, the absolute maximum negative input voltage is equal to the negative power supply voltage.

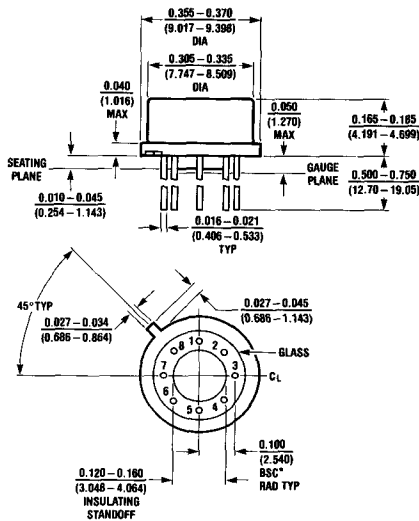
APPLICATIONS

Voltage Follower with Input Exceeding the Negative Common-Mode Range



PACKAGE DESCRIPTION

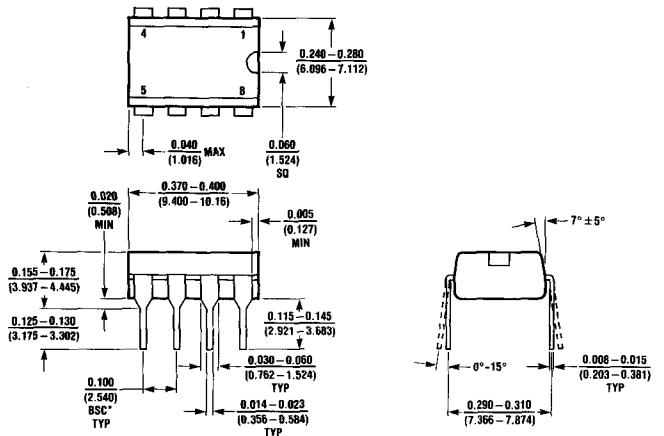
**H Package
Metal Can**



NOTE: DIMENSIONS IN INCHES

T_{jmax}	θ_{ja}	θ_{jc}
150°C	150°C/W	45°C/W

**N8 Package
8 Lead Plastic**



NOTE: DIMENSIONS IN INCHES UNLESS OTHERWISE NOTED
*LEADS WITHIN 0.007 OF TRUE POSITION (TP) AT GAUGE PLANE

T_{jmax}	θ_{ja}
100°C	130°C/W

FEATURES

- *Guaranteed* 3.8nV/ $\sqrt{\text{Hz}}$ max 1kHz Noise
- *Guaranteed* 5.5nV/ $\sqrt{\text{Hz}}$ max 10Hz Noise
- Very Low Peak-to-Peak Noise, 80nV Typical
- *Guaranteed* 25 μV max Offset Voltage
- *Guaranteed* 0.6 $\mu\text{V}/^\circ\text{C}$ max Drift with Temperature
- *Guaranteed* 11V/ μsec min Slew Rate (OP-37)
- *Guaranteed* 1 Million min Voltage Gain

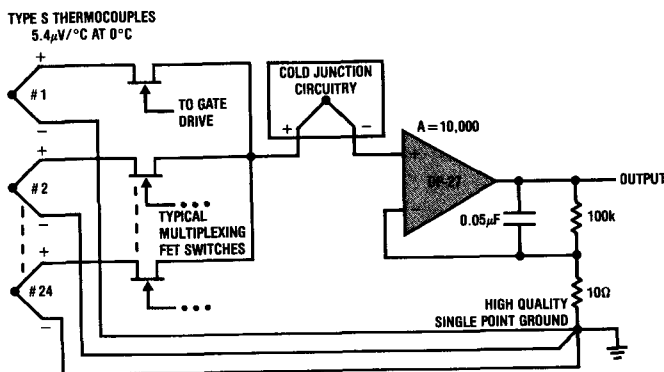
APPLICATIONS

- Low Level Transducer Amplifiers
- Precision Threshold Detectors
- Tape Head Preamplifiers
- Microphone Preamplifiers
- Direct Coupled Audio Gain Stages

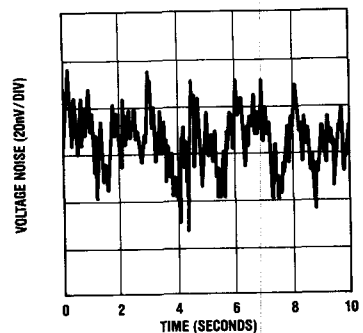
DESCRIPTION

The OP-27/OP-37 series of operational amplifiers combine outstanding noise performance with excellent precision and high speed specifications. The wideband noise is only 3nV/ $\sqrt{\text{Hz}}$, and with the 1/f noise corner at 2.7Hz, low noise is maintained for all low frequency instrumentation applications. Precision DC specifications match or exceed the best available op amps: offset voltage is 10 μV , drift with temperature and time are 0.2 $\mu\text{V}/^\circ\text{C}$ and 0.2 $\mu\text{V}/\text{month}$, respectively; common mode rejection is 126dB, voltage gain is two million. The unity gain compensated OP-27 is an order of magnitude faster than other precision op amps. The decompensated OP-37 is even faster at a gain-bandwidth product of 63MHz and 17V/ μsec slew rate. These characteristics plus Linear Technology's advanced process and test techniques make the OP-27/37 an excellent choice for performance and reliability in all low noise, precision amplifier applications. In addition, Linear's OP-37 is completely latch-up free in high gain, large capacitive feedback configurations. The accurate, microvolt, low noise signal handling capabilities of the OP-27/37 are taken advantage of in the multiplexed thermocouple application shown.

For applications requiring higher performance, see the LT1007 and LT1037 data sheets.

Low Noise, Multiplexed Thermocouple Amplifier


If 24 channels are multiplexed per second, and the output is required to settle to 0.1% accuracy, the amplifier's bandwidth cannot be limited to less than 30Hz. Yet the noise contribution of the OP-27 will still be only 0.11 $\mu\text{Vp-p}$, which is equivalent to an error of only 0.02 $^\circ\text{C}$.

0.1Hz to 10Hz Noise


ABSOLUTE MAXIMUM RATINGS

Supply Voltage	± 22V
Internal Power Dissipation	500mW
Input Voltage	Equal to Supply Voltage
Output Short Circuit Duration	Indefinite
Differential Input Current (Note 8)	± 25mA
Lead Temperature (Soldering, 10 sec.)	300°C
Operating Temperature Range	
OP-27/OP-37 A, C	-55°C to 125°C
OP-27/OP-37 E, G	-25°C to 85°C
Junction Temperature Range	
OP-27/OP-37 A, C	-55°C to 150°C
OP-27/OP-37 E, G	-25°C to 125°C
Storage Temperature Range	
OP-27/OP-37 A, C, E, G	-65°C to 150°C

PACKAGE/ORDER INFORMATION

TOP VIEW V _{OS} TRIM	ORDER PART NUMBER	
		OP-27AH OP-27CH OP-27EH OP-27GH
TOP VIEW		
	OP-27AJ8 OP-27CJ8 OP-27EJ8 OP-27GJ8 OP-37AJ8 OP-37CJ8	OP-37EJ8 OP-37GJ8 OP-27EN8 OP-27GN8 OP-37EN8 OP-37GN8

ELECTRICAL CHARACTERISTICS V_S = ± 15V, T_A = 25°C, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	OP-27A,E/OP-37A,E			OP-27C,G/OP-37C,G			UNITS	
			MIN	TYP	MAX	MIN	TYP	MAX		
V _{OS}	Input Offset Voltage	(Note 1)		10	25		30	100	μV	
$\frac{\Delta V_{OS}}{\Delta \text{Time}}$	Long Term Offset Voltage Stability	(Note 2)		0.2	1.0		0.4	2.0	μV/Mo	
I _{OS}	Input Offset Current			7	35		12	75	nA	
I _B	Input Bias Current			± 10	± 40		± 15	± 80	nA	
e _n	Input Noise Voltage	0.1Hz to 10Hz (Notes 3 and 5)		0.08	0.18		0.09	0.25	μVp-p	
	Input Noise Voltage Density	f _o = 10Hz (Note 3)		3.5	5.5		3.8	8.0	nV/√Hz	
		f _o = 30Hz (Note 3)		3.1	4.5		3.3	5.6	nV/√Hz	
		f _o = 1000Hz (Note 3)		3.0	3.8		3.2	4.5	nV/√Hz	
i _n	Input Noise Current Density	f _o = 10Hz (Notes 3 and 6)		1.7	4.0		1.7		pA/√Hz	
		f _o = 30Hz (Notes 3 and 6)		1.0	2.3		1.0		pA/√Hz	
		f _o = 1000Hz (Notes 3 and 6)		0.4	0.6		0.4	0.6	pA/√Hz	
	Input Resistance—Common Mode			3		2		GΩ		
	Input Voltage Range			± 11.0	± 12.3		± 11.0	± 12.3	V	
CMRR	Common Mode Rejection Ratio	V _{CM} = ± 11V	114	126		100	120		dB	
PSRR	Power Supply Rejection Ratio	V _S = ± 4V to ± 18V	100	120		94	118		dB	
A _{VOL}	Large Signal Voltage Gain	R _L ≥ 2kΩ, V _O = ± 10V	1000	1800		700	1500		V/mV	
		R _L ≥ 1kΩ, V _O = ± 10V	800	1500			1500		V/mV	
		R _L = 600Ω, V _O = ± 1V	250	700		200	500		V/mV	
		V _S = ± 4V (Note 4)								
V _{OUT}	Maximum Output Voltage Swing	R _L ≥ 2kΩ	± 12.0	± 13.8		± 11.5	± 13.5		V	
		R _L ≥ 600Ω	± 10.0	± 11.5		± 10.0	± 11.5		V	
SR	Slew Rate	OP-27	1.7	2.8		1.7	2.8		V/μs	
		OP-37	11	17		11	17		V/μs	
GBW	Gain-Bandwidth Product	OP-27	5.0	8.0		5.0	8.0		MHz	
		OP-37	f _o = 10kHz (Note 4)	45	63		45	63		MHz
			f _o = 1MHz (A _{VCL} ≥ 5)		40			40		MHz
Z _O	Open Loop Output Resistance	V _O = 0, I _O = 0		70		70		Ω		
P _d	Power Dissipation			90	140		100	170	mW	

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V, -55^\circ C \leq T_A \leq 125^\circ C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	OP-27A/OP-37A			OP-27C/OP-37C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	(Note 1)	•	30	60	70	300	μV	
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Input Offset Drift	(Note 7)	•	0.2	0.6	0.4	1.8	$\mu V/^\circ C$	
I_{OS}	Input Offset Current		•	15	50	30	135	nA	
I_B	Input Bias Current		•	± 20	± 60	± 35	± 150	nA	
	Input Voltage Range		•	± 10.3	± 11.5	± 10.2	± 11.5	V	
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 10V$	•	108	122	94	116	dB	
PSRR	Power Supply Rejection Ratio	$V_S = \pm 4.5V$ to $\pm 18V$	•	96	116	86	110	dB	
A_{VOL}	Large Signal Voltage Gain	$R_L \geq 2k\Omega, V_O = \pm 10V$	•	600	1200	300	800	V/mV	
V_{OUT}	Maximum Output Voltage Swing	$R_L \geq 2k\Omega$	•	± 11.5	± 13.5	± 10.5	± 13.0	V	

2

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V, -25^\circ C \leq T_A \leq 85^\circ C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	OP-27E/OP-37E			OP-27G/OP-37G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	(Note 1)	•	20	50	55	220	μV	
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Input Offset Drift	(Note 7)	•	0.2	0.6	0.4	1.8	$\mu V/^\circ C$	
I_{OS}	Input Offset Current		•	10	50	20	135	nA	
I_B	Input Bias Current		•	± 14	± 60	± 25	± 150	nA	
	Input Voltage Range		•	± 10.5	± 11.8	± 10.5	± 11.8	V	
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 10V$	•	110	124	96	118	dB	
PSRR	Power Supply Rejection Ratio	$V_S = \pm 4.5V$ to $\pm 18V$	•	97	118	90	114	dB	
A_{VOL}	Large Signal Voltage Gain	$R_L \geq 2k\Omega, V_O = \pm 10V$	•	750	1500	450	1000	V/mV	
V_{OUT}	Maximum Output Voltage Swing	$R_L \geq 2k\Omega$	•	± 11.7	± 13.6	± 11.0	± 13.3	V	

The ● denotes the specifications which apply over full operating temperature range.

Note 1: Input Offset Voltage measurements are performed by automatic test equipment approximately 0.5 seconds after application of power. A and E grades are guaranteed fully warmed up.

Note 2: Long Term Input Offset Voltage Stability refers to the average trend line of Offset Voltage vs Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 days are typically $2.5\mu V$ —refer to typical performance curve.

Note 3: Sample tested. Contact factory for 100% testing of 10Hz voltage noise.

Note 4: Parameter is guaranteed by design and is not tested.

Note 5: See test circuit and frequency response curve for 0.1Hz to 10Hz tester in Applications Information section.

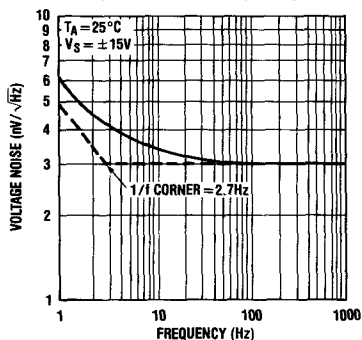
Note 6: See test circuit for current noise measurement in Applications Information section.

Note 7: The Average Input Offset Drift performance is within the specifications unnullled or when nullled with a pot having a range of $8k\Omega$ to $20k\Omega$.

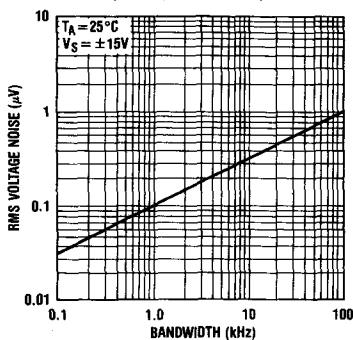
Note 8: The OP-27/37's inputs are protected by back-to-back diodes. Current limiting resistors are not used in order to achieve low noise. If differential input voltage exceeds $\pm 0.7V$, the input current should be limited to 25mA.

TYPICAL PERFORMANCE CHARACTERISTICS

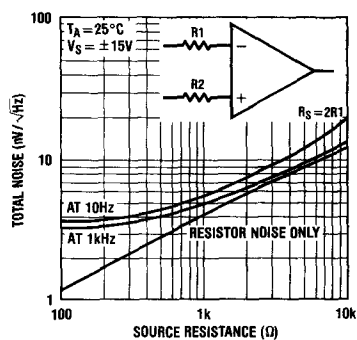
Voltage Noise vs Frequency



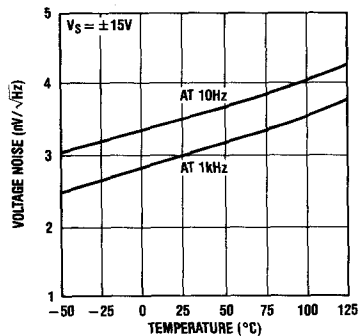
Input Wideband Voltage Noise vs Bandwidth (0.1Hz to Frequency Indicated)



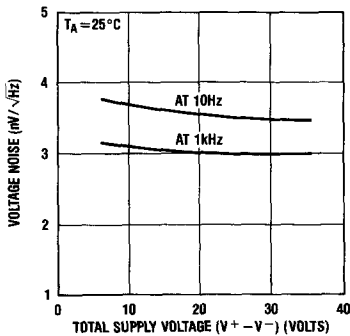
Total Noise vs Source Resistance



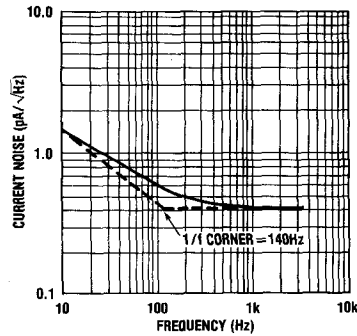
Voltage Noise vs Temperature



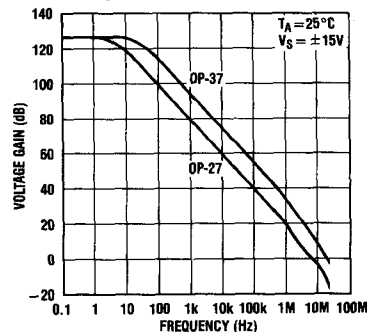
Voltage Noise vs Supply Voltage



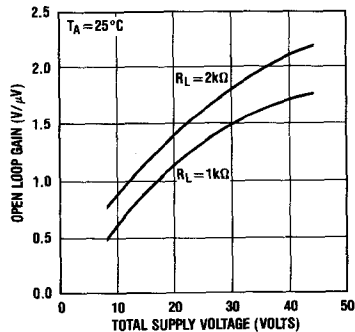
Current Noise vs Frequency



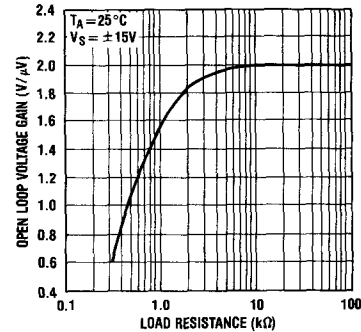
Voltage Gain vs Frequency



Open Loop Voltage Gain vs Supply Voltage

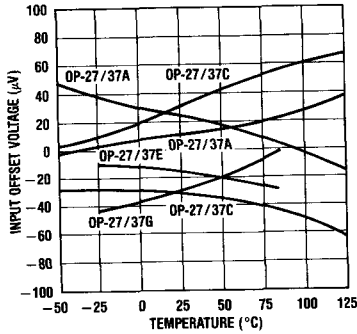


Open Loop Voltage Gain vs Load Resistance

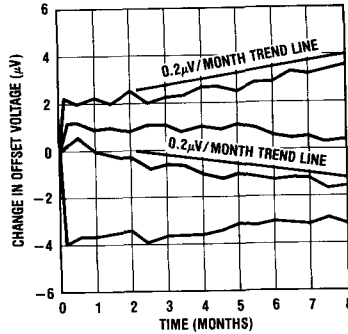


TYPICAL PERFORMANCE CHARACTERISTICS

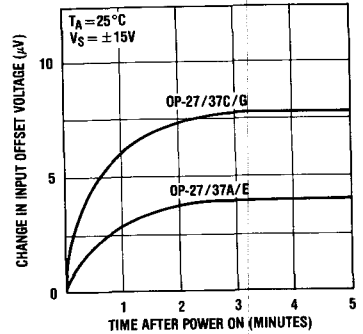
Offset Voltage Drift of Representative Units



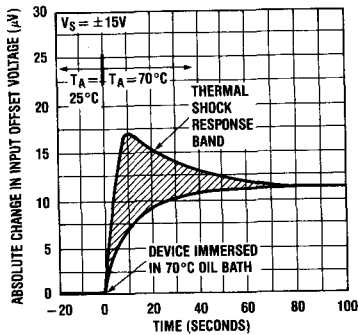
Long Term Drift of Representative Units



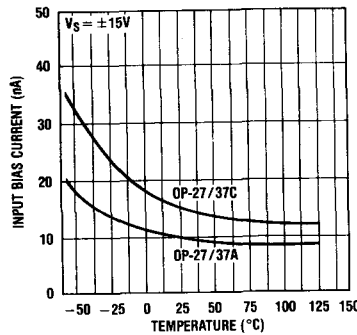
Warm-Up Drift



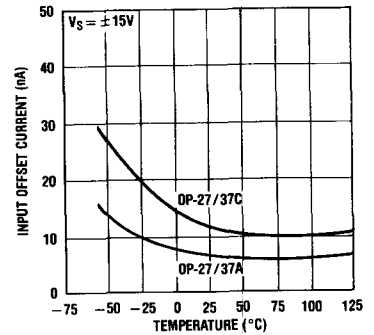
Offset Voltage Change Due to Thermal Shock



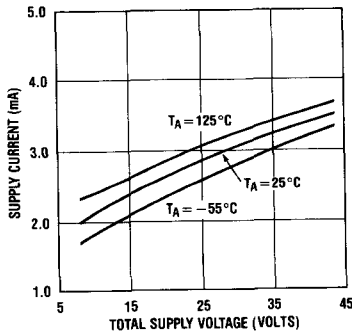
Input Bias Current vs Temperature



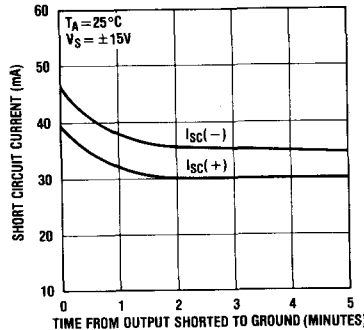
Input Offset Current vs Temperature



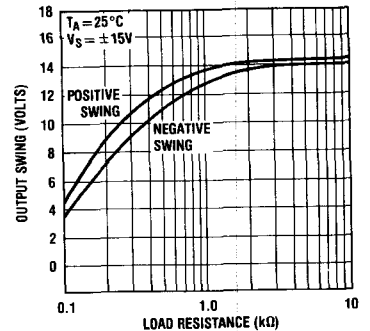
Supply Current vs Supply Voltage



Short Circuit Current vs Time



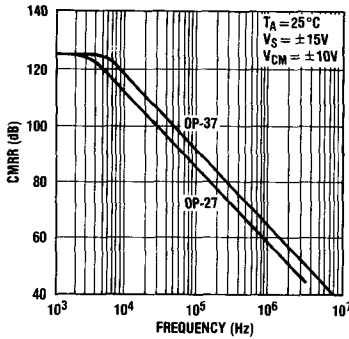
Maximum Output Swing vs Resistive Load



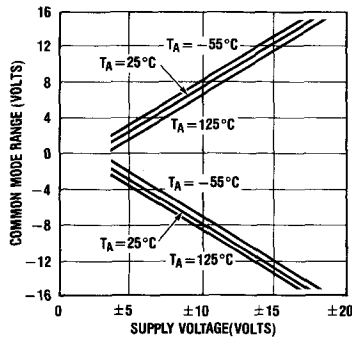
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TYPICAL PERFORMANCE CHARACTERISTICS

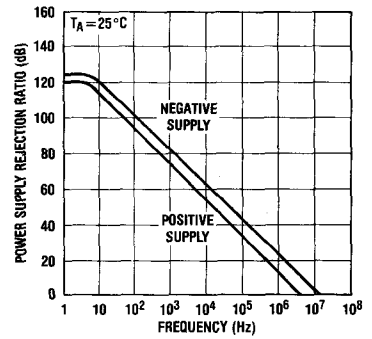
Common Mode Rejection vs Frequency



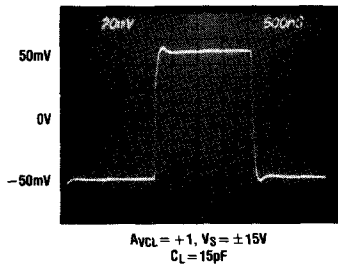
Common Mode Input Range vs Supply Voltage



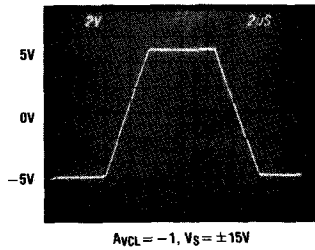
PSRR vs Frequency



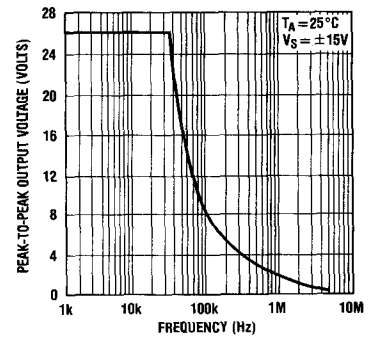
OP-27 Small Signal Transient Response



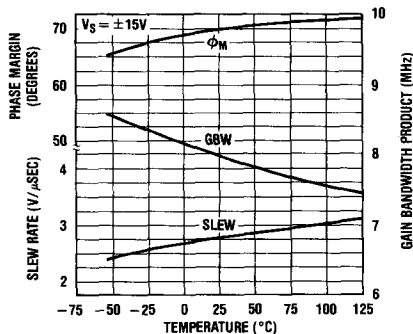
OP-27 Large Signal Transient Response



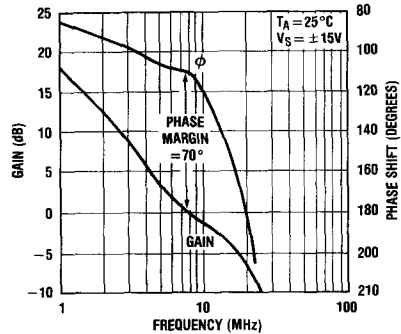
OP-27 Maximum Undistorted Output vs Frequency



OP-27 Slew Rate, Gain Bandwidth Product, Phase Margin vs Temperature

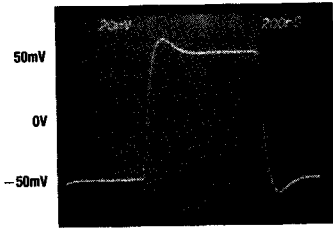


OP-27 Gain, Phase Shift vs Frequency



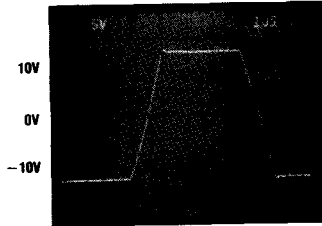
TYPICAL PERFORMANCE CHARACTERISTICS

OP-37 Small Signal Transient Response



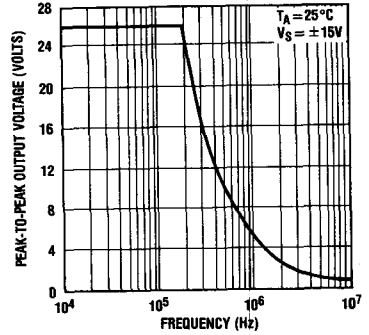
$A_{vCL} = +5$, $V_S = \pm 15V$
 $C_L = 15pF$

OP-37 Large Signal Response



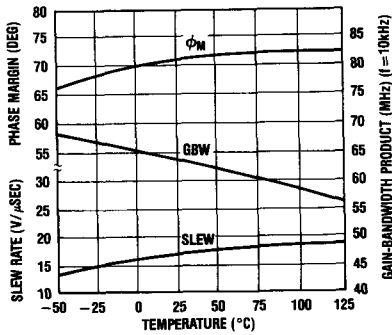
$A_{vCL} = +5$, $V_S = \pm 15V$

OP-37 Maximum Undistorted Output vs Frequency

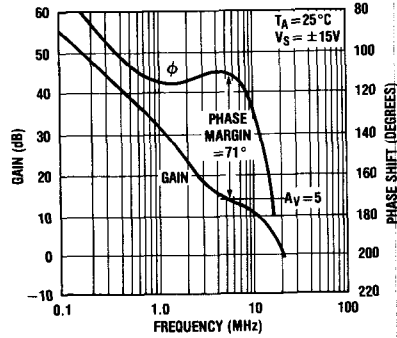


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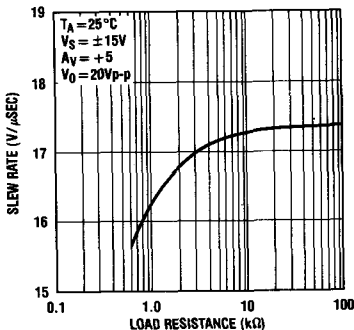
OP-37 Slew Rate, Gain Bandwidth Product, Phase Margin vs Temperature



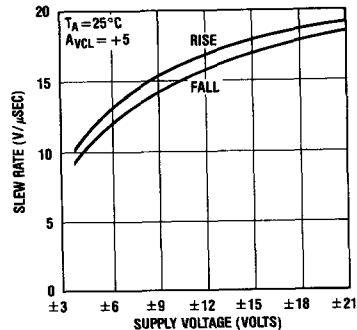
OP-37 Gain, Phase Shift vs Frequency



OP-37 Slew Rate vs Load



OP-37 Slew Rate vs Supply Voltage



APPLICATIONS INFORMATION

General

The OP-27/37 series devices may be inserted directly into OP-07, OP-05, 725, and 5534 sockets with or without removal of external compensation or nulling components. In addition, the OP-27/37 may be fitted to 741 sockets with the removal or modification of external nulling components.

Noise Testing

The 0.1Hz to 10Hz peak-to-peak noise of the OP-27/OP-37 is measured in the test circuit shown. The frequency response of this noise tester indicates that the 0.1Hz corner is defined by only one zero. The test time to measure 0.1Hz to 10Hz noise should not exceed 10 seconds, as this time limit acts as an additional zero to eliminate noise contributions from the frequency band below 0.1Hz.

Measuring the typical 80nV peak-to-peak noise performance of the OP-27/37 requires special test precautions:

- (a) The device should be warmed up for at least five minutes. As the op amp warms up, its offset voltage changes typically 4μV due to its chip temperature increasing 10°C to 20°C from the moment the power supplies are turned on. In the 10 second measurement interval these temperature-induced effects can easily exceed tens of nanovolts.

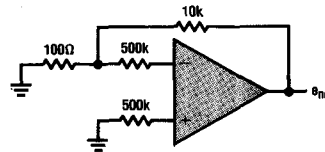
- (b) For similar reasons, the device must be well shielded from air currents to eliminate the possibility of thermoelectric effects in excess of a few nanovolts, which would invalidate the measurements.

- (c) Sudden motion in the vicinity of the device can also "feedthrough" to increase the observed noise.

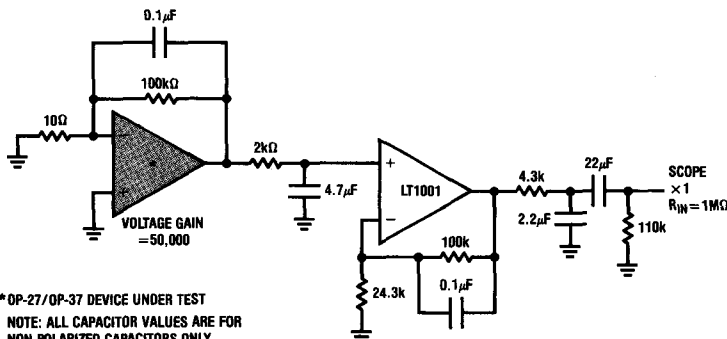
A noise-voltage density test is recommended when measuring noise on a large number of units. A 10Hz noise-voltage density measurement will correlate well with a 0.1Hz to 10Hz peak-to-peak noise reading since both results are determined by the white noise and the location of the 1/f corner frequency.

Current noise is measured and calculated by the following formula:

$$i_n = \frac{[e^2_{no} - (130nV)^2]^{1/2}}{1M\Omega \times 100}$$

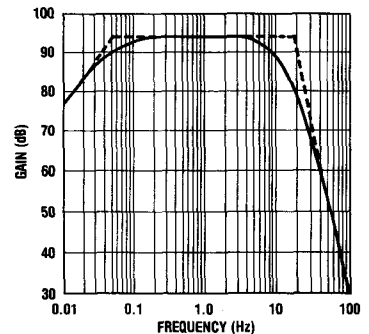


0.1Hz to 10Hz Noise Test Circuit



* OP-27/OP-37 DEVICE UNDER TEST
NOTE: ALL CAPACITOR VALUES ARE FOR NON-POLARIZED CAPACITORS ONLY.

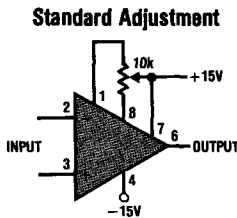
0.1Hz to 10Hz p-p Noise Tester Frequency Response



APPLICATIONS INFORMATION

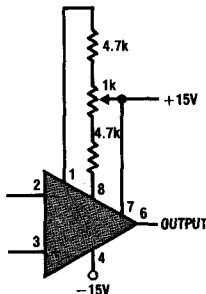
Offset Voltage Adjustment

The input offset voltage of the OP-27/37, and its drift with temperature, are permanently trimmed at wafer testing to a low level. However, if further adjustment of V_{OS} is necessary, the use of a 10k nulling potentiometer will not degrade drift with temperature. Trimming to a value other than zero creates a drift of $(V_{OS}/300) \mu V/^{\circ}C$, e.g., if V_{OS} is adjusted to $300 \mu V$, the change in drift will be $1 \mu V/^{\circ}C$.



The adjustment range with a 10k pot is approximately $\pm 2.5mV$. If less adjustment range is needed, the sensitivity and resolution of the nulling can be improved by using a smaller pot in conjunction with fixed resistors. The example has an approximate null range of $\pm 200 \mu V$.

Improved Sensitivity Adjustment

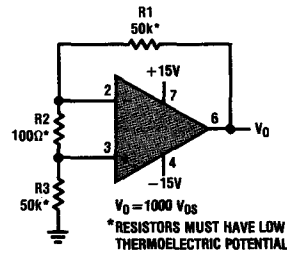


Offset Voltage and Drift

Thermocouple effects, caused by temperature gradients across dissimilar metals at the contacts to the input terminals, can exceed the inherent drift of the amplifier unless proper care is exercised. Air currents should be minimized, package leads should be short, the two input leads should be close together and maintained at the same temperature.

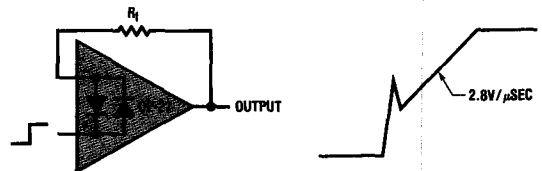
The circuit shown to measure offset voltage is also used as the burn-in configuration for the OP-27/37, with the supply voltages increased to $\pm 20V$, $R_1 = R_3 = 10k$, $R_2 = 200\Omega$, $A_V = 100$.

Test Circuit for Offset Voltage and Offset Voltage Drift with Temperature



Unity Gain Buffer Applications (OP-27 Only)

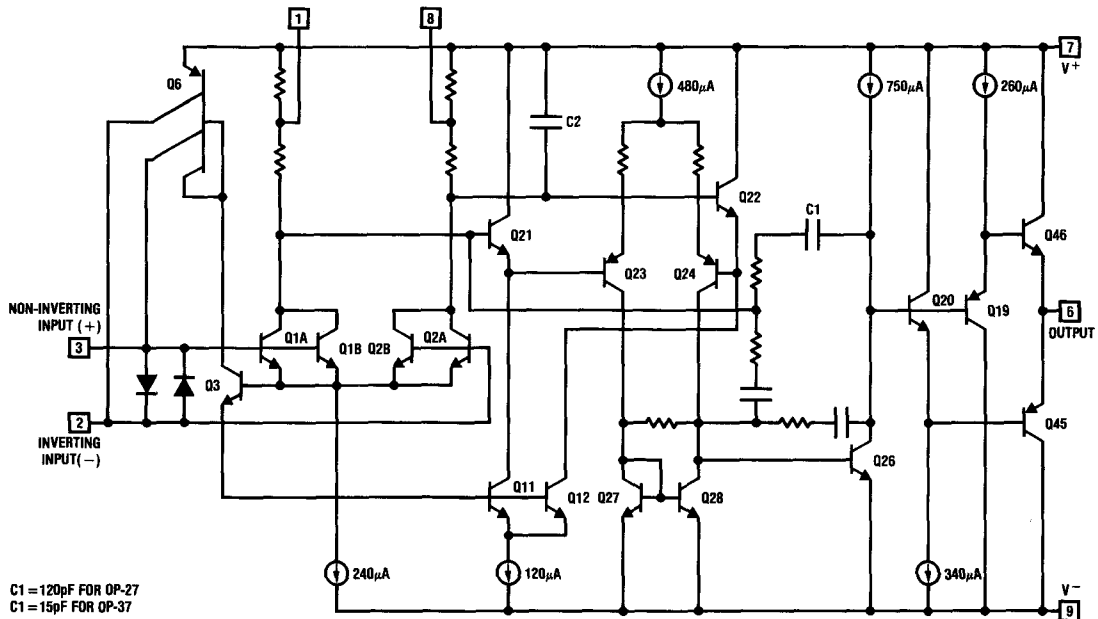
When $R_f \leq 100\Omega$ and the input is driven with a fast, large signal pulse ($> 1V$), the output waveform will look as shown in the pulsed operation diagram.



During the fast feedthrough-like portion of the output, the input protection diodes effectively short the output to the input and a current, limited only by the output short circuit protection, will be drawn by the signal generator. With $R_f \geq 500\Omega$, the output is capable of handling the current requirements ($I_L \leq 20mA$ at $10V$) and the amplifier stays in its active mode and a smooth transition will occur.

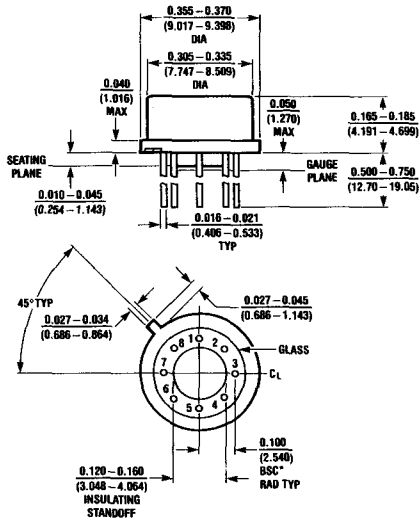
As with all operational amplifiers when $R_f > 2k\Omega$, a pole will be created with R_f and the amplifier's input capacitance, creating additional phase shift and reducing the phase margin. A small capacitor ($20pF$ to $50pF$) in parallel with R_f will eliminate this problem.

SCHEMATIC DIAGRAM



PACKAGE DESCRIPTION

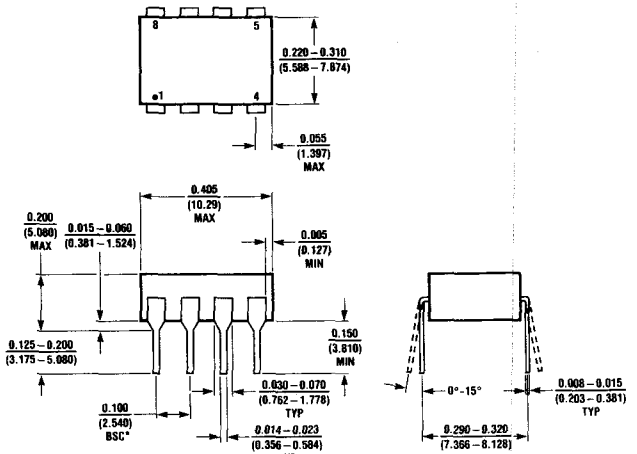
H Package
Metal Can



NOTE: DIMENSIONS IN INCHES (MILLIMETERS)

T _{max}	θ _{ja}	θ _{jc}
150°C	150°C/W	45°C/W

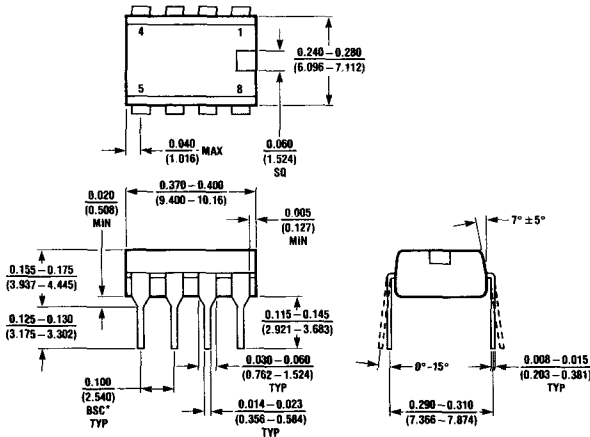
J8 Package
8 Lead Hermetic DIP



NOTE: DIMENSIONS IN INCHES (MILLIMETERS) UNLESS OTHERWISE NOTED
*LEADS WITHIN 0.007 OF TRUE POSITION (TP) AT GAUGE PLANE

T _{max}	θ _{ja}
150°C	100°C/W

N8 Package
8 Lead Plastic



NOTE: DIMENSIONS IN INCHES UNLESS OTHERWISE NOTED
*LEADS WITHIN 0.007 OF TRUE POSITION (TP) AT GAUGE PLANE

T _{max}	θ _{ja}
100°C	130°C/W

NOTES

Dual Matched Low Noise Precision Op Amp and Dual High Speed Low Noise Precision Op Amp

FEATURES

- *Guaranteed* 80 μ V Max. V_{OS}
- *Guaranteed* 6.0nV/ $\sqrt{\text{Hz}}$ 10Hz Voltage Noise Density
- *Guaranteed* 3.9nV/ $\sqrt{\text{Hz}}$ 1kHz Voltage Noise Density
- *Guaranteed* 1 μ V/ $^{\circ}$ C Max. V_{OS} Drift
- *Guaranteed* 1 Million Min. Voltage Gain
- *Guaranteed* Matching Characteristics
- *Guaranteed* 10V/ μ s Min. Slew Rate (OP-237)

APPLICATIONS

- Instrumentation Amplifiers
- Low Level Signal Processing
- Low Noise Audio Amplifiers
- Strain Gauge Amplifiers

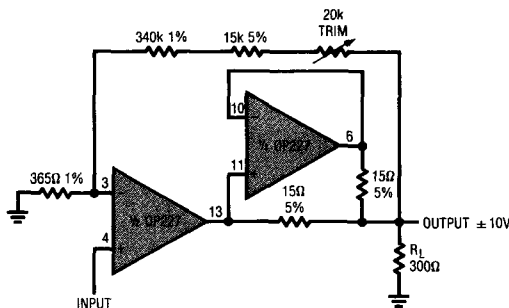
DESCRIPTION

The OP-227 is a dual matched precision op amp which combines low offset, low noise, and high gain with excellent matching characteristics. Typical individual amplifier specifications of 20 μ V V_{OS} , 0.2 μ V/ $^{\circ}$ C drift, 10nA I_B and 2.8nV/ $\sqrt{\text{Hz}}$ 10Hz noise voltage density make the OP-227 an impressive performer in terms of single amplifiers. Matching characteristics are specified with guaranteed limits on all critical parameters including V_{OS} , V_{OS} drift, I_{BIAS} and CMRR (see the Features section), which make the OP-227 an ideal choice for two and three op amp instrumentation amplifier applications.

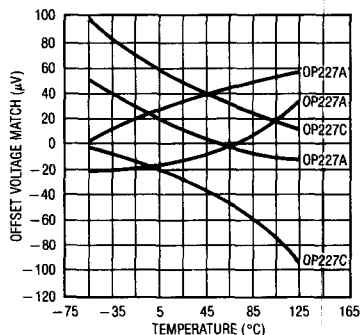
The OP-237 offers DC specifications identical to the OP-227 and is decompensated for higher speed operation at inverting gains greater than 5.

2

Precision Amplifier Drives 300 Ω Load to \pm 10V with 0.05% Accuracy



Matching Characteristic; Drift of Offset Voltage Match of Representative Units



OP-227/OP-237

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (Note 9)	± 22V
Internal Power Dissipation	500mW
Input Voltage	Equal to Supply Voltage
Output Short-Circuit Duration	Indefinite
Differential Input Current (Note 8)	± 25mA
Storage Temperature Range	- 65°C to + 150°C
Operating Temperature	
OP-227A/237A/227C/237C	- 55°C to + 125°C
OP-227E/237E/227G/237G	- 25°C to + 85°C
Lead Temperature Range (Soldering, 10 sec.)	300°C

PACKAGE/ORDER INFORMATION

TOP VIEW

J PACKAGE N PACKAGE
14 PIN HERMETIC 14 PIN PLASTIC

NOTE: DEVICE MAY BE OPERATED EVEN IF INSERTION IS REVERSED, THIS IS DUE TO INHERENT SYMMETRY OF PIN LOCATIONS OF AMPLIFIERS A AND B (NOTE 9).

ORDER
PART NUMBER

OP-227AJ OP-237AJ
OP-227CJ OP-237CJ
OP-227EJ OP-237EJ
OP-227GJ OP-237GJ
OP-227EN OP-237EN
OP-227GN OP-237GN

ELECTRICAL CHARACTERISTICS Individual Amplifiers

$V_S = \pm 15V$, $T_A = 25^\circ C$, unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS	OP-227A, E OP-237A, E			OP-227C, G OP-237C, G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	(Note 1)	—	20	80	—	60	180	μV
$\frac{\Delta V_{OS}}{\Delta Time}$	Long Term V_{OS} Stability	(Notes 2, 3)	—	0.2	1.0	—	0.2	2.0	$\mu V/Mo$
I_{OS}	Input Offset Current		—	7	35	—	12	75	nA
I_B	Input Bias Current		—	± 10	± 40	—	± 15	± 80	nA
e_{np-p}	Input Noise Voltage	0.1Hz to 10Hz (Notes 3, 5)	—	0.06	0.20	—	0.06	0.28	$\mu Vp-p$
e_n	Input Noise Voltage Density	$f_0 = 10Hz$ (Note 3)	—	2.8	6.0	—	2.8	9.0	nV/\sqrt{Hz}
		$f_0 = 30Hz$ (Note 3)	—	2.6	4.7	—	2.6	5.9	nV/\sqrt{Hz}
		$f_0 = 1000Hz$ (Note 3)	—	2.5	3.9	—	2.5	4.6	nV/\sqrt{Hz}
i_n	Input Noise Current Density	$f_0 = 10Hz$ (Notes 3, 6)	—	1.5	4.5	—	1.5	—	pA/\sqrt{Hz}
		$f_0 = 30Hz$ (Notes 3, 6)	—	1.0	2.5	—	1.0	—	pA/\sqrt{Hz}
		$f_0 = 1000Hz$ (Notes 3, 6)	—	0.4	0.7	—	0.4	0.7	pA/\sqrt{Hz}
	Input Resistance— Common Mode		—	7	—	—	5	—	G Ω
	Input Voltage Range		± 11.0	± 12.5	—	± 11.0	± 12.5	—	V
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 11V$	114	126	—	100	126	—	dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 4V$ to $\pm 18V$	—	1	10	—	2	20	$\mu V/V$
A_{VOL}	Large-Signal Voltage Gain	$R_L \geq 2k\Omega$, $V_O = \pm 12V$	3	20	—	2	20	—	$V/\mu V$
		$R_L \geq 600\Omega$, $V_O = \pm 10V$	1	12	—	0.8	12	—	$V/\mu V$
V_{OUT}	Output Voltage Swing	$R_L \geq 2k\Omega$	± 12.0	± 13.8	—	± 11.5	± 13.5	—	V
		$R_L \geq 600\Omega$	± 10.0	± 12.5	—	± 10.0	± 12.5	—	V
SR	Slew Rate	OP-227 $R_L \geq 2k\Omega$	1.7	2.8	—	1.7	2.8	—	$V/\mu s$
		OP-237 $A_{VCL} \geq 5$	10	15	—	10	15	—	$V/\mu s$
GBW	Gain Bandwidth Prod.	OP-227 $f_0 = 100kHz$ (Note 4)	5	8	—	5	8	—	MHz
		OP-237 $f_0 = 10kHz$ (Note 4)	35	63	—	35	63	—	MHz
		OP-237 $f_0 = 1MHz$ ($A_{VCL} \geq 5$)	—	40	—	—	40	—	MHz
Z_0	Open-Loop Output Resistance	$V_O = 0$, $I_O = 0$	—	70	—	—	70	—	Ω
P_d	Power Consumption	Each Amplifier	—	80	140	—	90	170	mW
	Offset Adjustment Range	$R_p = 10k\Omega$	—	± 4	—	—	± 4	—	mV

ELECTRICAL CHARACTERISTICS Individual Amplifiers

$V_S = \pm 15V$, $-25^\circ C \leq T_A \leq 85^\circ C$, unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS		OP-227E OP-237E			OP-227G OP-237G			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	(Note 1)	●	—	40	140	—	85	280	μV
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Input Offset Drift	(Note 7)	●	—	0.2	1.0	—	0.3	1.8	$\mu V/^\circ C$
I_{OS}	Input Offset Current		●	—	15	50	—	20	135	nA
I_B	Input Bias Current		●	—	± 20	± 60	—	± 35	± 150	nA
	Input Voltage Range		●	± 10.5	± 11.5	—	± 10.5	± 11.5	—	V
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 10V$	●	110	124	—	96	118	—	dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 4.5V$ to $\pm 18V$	●	—	2	15	—	2	32	$\mu V/V$
A_{VOL}	Large Signal Voltage Gain	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	●	1	14	—	0.8	14	—	$V/\mu V$
V_{OUT}	Output Voltage Swing	$R_L \geq 2k\Omega$	●	± 11.7	± 13.6	—	± 11.0	± 13.3	—	V

2

ELECTRICAL CHARACTERISTICS Individual Amplifiers

$V_S = \pm 15V$, $-55^\circ C \leq T_A \leq 125^\circ C$, unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS		OP-227A OP-237A			OP-227C OP-237C			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	(Note 1)	●	—	60	180	—	110	350	μV
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Input Offset Drift	(Note 7)	●	—	0.2	1.0	—	0.3	1.8	$\mu V/^\circ C$
I_{OS}	Input Offset Current		●	—	15	50	—	30	135	nA
I_B	Input Bias Current		●	—	± 20	± 60	—	± 35	± 150	nA
	Input Voltage Range		●	± 10.5	± 11.8	—	± 10.2	± 11.8	—	V
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 10V$	●	108	122	—	94	116	—	dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 4.5V$ to $\pm 18V$	●	—	2	16	—	4	51	$\mu V/V$
A_{VOL}	Large Signal Voltage Gain	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	●	1	14	—	0.8	14	—	V
V_{OUT}	Output Voltage Swing	$R_L \geq 2k\Omega$	●	± 11.5	± 13.5	—	± 10.5	± 13.0	—	V

The ● denotes the specifications which apply over the full operating temperature range.

For MIL-STD components, please refer to LTC 883C data sheet for test listing and parameters.

Note 1: Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.

Note 2: Long-Term Input Offset Voltage Stability refers to the average trend line of V_{OS} vs Time over extended periods after the first 30 days of operation.

Note 3: Sample tested.

Note 4: Parameter is guaranteed by design.

Note 5: See test circuit and frequency response curve for 0.1Hz to 10Hz tester.

Note 6: See test circuit for current noise measurement.

Note 7: The input offset drift performance is within the specifications un-nulled or when nulled with $R_P = 8k\Omega$ to $20k\Omega$.

Note 8: The inputs are protected by back-to-back diodes. Current limiting resistors are not used in order to achieve low noise. If differential input voltage exceeds $\pm 0.7V$, the input current should be limited to 25mA.

Note 9: The V^+ supply terminals are completely independent and may be powered by separate supplies if desired (this approach, however, would sacrifice the advantages of the power supply rejection ratio matching). The V^- supply terminals are both connected to the common substrate and must be tied to the same voltage. Both V^- pins should be used.

OP-227/OP-237

MATCHING CHARACTERISTICS See notes on page 2-233.

at $V_S = \pm 15V$, $T_A = 25^\circ C$, unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS	OP-227A, E, OP-237A, E			OP-227C, G, OP-237C, G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
ΔV_{OS}	Input Offset Voltage Match		—	25	80	—	55	300	μV
I_B^+	Average Non-Inverting Bias Current		—	± 10	± 40	—	± 15	± 90	nA
I_{OS}^+	Non-Inverting Offset Current		—	± 12	± 60	—	± 20	± 130	nA
I_{OS}^-	Inverting Offset Current		—	± 12	± 60	—	± 20	± 130	nA
$\Delta CMRR$	Common Mode Rejection Ratio Match	$V_{CM} = \pm 11V$	110	123	—	97	117	—	dB
$\Delta PSRR$	Power Supply Rejection Ratio Match	$V_S = \pm 4V$ to $\pm 18V$	—	2	10	—	2	20	$\mu V/V$
	Channel Separation	(Note 4)	126	154	—	126	154	—	dB
ΔA_{VOL}	Gain Match	$f_0 = 100kHz$ (Note 4) $R_L \geq 2k\Omega$, $V_0 = \pm 10V$	—	1.5	6.0	—	2.0	9.0	%

at $V_S = \pm 15V$, $-55^\circ C \leq T_A \leq 125^\circ C$, unless otherwise noted

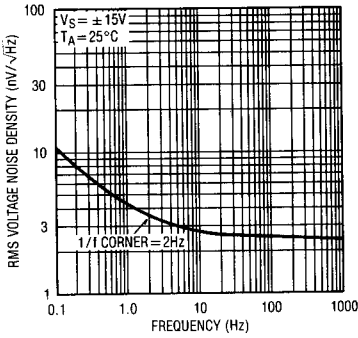
SYMBOL	PARAMETER	CONDITIONS	OP-227A, OP-237A			OP-227C, OP-237C			UNITS	
			MIN	TYP	MAX	MIN	TYP	MAX		
ΔV_{OS}	Input Offset Voltage Match		●	—	55	180	—	100	480	μV
$\frac{\Delta V_{OS}}{\Delta Temp}$	Input Offset Voltage Tracking	(Note 7)	●	—	0.3	1.0	—	0.5	1.8	$\mu V/^\circ C$
I_B^+	Average Non-Inverting Bias Current		●	—	± 20	± 60	—	± 35	± 170	nA
$\frac{\Delta I_B^+}{\Delta Temp}$	Average Drift of Non-Inverting Bias Current		●	—	100	—	—	200	—	$pA/^\circ C$
I_{OS}^+	Non-Inverting Offset Current		●	—	± 25	± 90	—	± 45	± 250	nA
$\frac{I_{OS}^+}{\Delta Temp}$	Average Drift of Non-Inverting Offset Current		●	—	130	—	—	250	—	$pA/^\circ C$
I_{OS}^-	Inverting Offset Current		●	—	± 25	± 90	—	± 45	± 250	nA
$\Delta CMRR$	Common Mode Rejection Ratio Match	$V_{CM} = \pm 10V$	●	105	118	—	90	110	—	dB
$\Delta PSRR$	Power Supply Rejection Ratio Match	$V_S = \pm 4.5V$ to $\pm 18V$	●	—	2	16	—	4	51	$\mu V/V$

at $V_S = \pm 15V$, $-25^\circ C \leq T_A \leq 85^\circ C$, unless otherwise noted

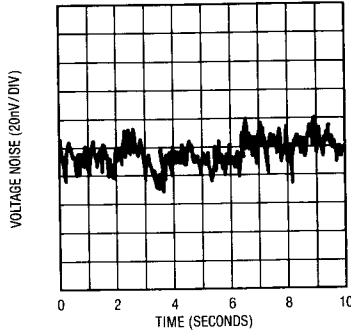
SYMBOL	PARAMETER	CONDITIONS	OP-227E, OP-237E			OP-227G, OP-237G			UNITS	
			MIN	TYP	MAX	MIN	TYP	MAX		
ΔV_{OS}	Input Offset Voltage Match		●	—	40	140	—	90	400	μV
$TC\Delta V_{OS}$	Input Offset Voltage Tracking	(Note 7)	●	—	0.3	1.0	—	0.5	1.8	$\mu V/^\circ C$
I_B^+	Average Non-Inverting Bias Current		●	—	± 14	± 60	—	± 25	± 170	nA
$\frac{\Delta I_B^+}{\Delta Temp}$	Average Drift of Non-Inverting Bias Current		●	—	80	—	—	180	—	$pA/^\circ C$
I_{OS}^+	Non-Inverting Offset Current		●	—	± 20	± 90	—	± 35	± 250	nA
$\frac{\Delta I_{OS}^+}{\Delta Temp}$	Average Drift of Non-Inverting Offset Current		●	—	130	—	—	250	—	$pA/^\circ C$
I_{OS}^-	Inverting Offset Current		●	—	± 20	± 90	—	± 35	± 250	nA
$\Delta CMRR$	Common Mode Rejection Ratio Match	$V_{CM} = \pm 10V$	●	106	120	—	90	112	—	dB
$\Delta PSRR$	Power Supply Rejection Ratio Match	$V_S = \pm 4.5V$ to $\pm 18V$	●	—	2	15	—	3	32	$\mu V/V$

TYPICAL PERFORMANCE CHARACTERISTICS

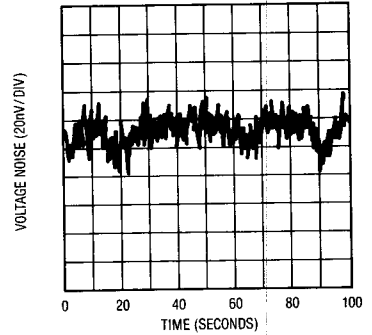
Voltage Noise vs Frequency



0.1Hz to 10Hz Noise

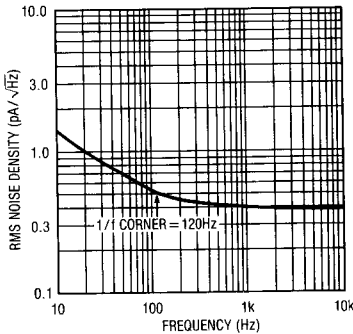


0.01Hz to 1Hz Peak-to-Peak Noise

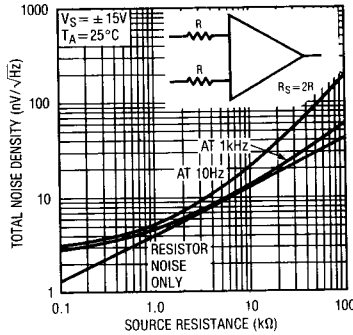


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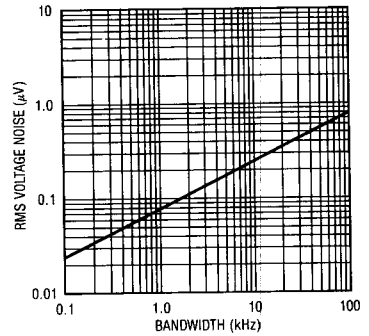
Current Noise vs Frequency



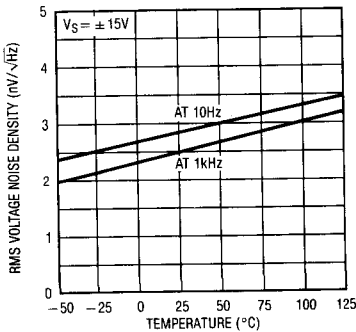
Total Noise vs Source Resistance



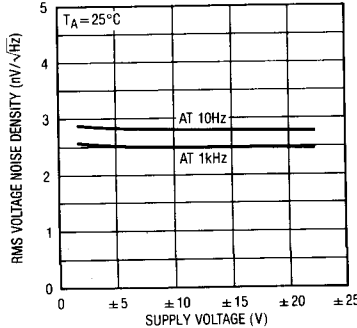
Wideband Voltage Noise (0.1Hz to Frequency Indicated)



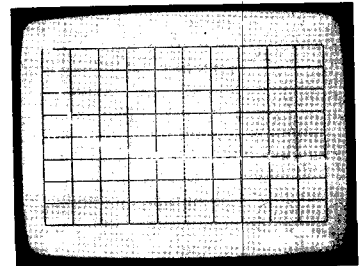
Voltage Noise vs Temperature



Voltage Noise vs Supply Voltage



0.02Hz to 10Hz RMS Noise. Gain = 50,000 (Measured on HP3582 Spectrum Analyzer)

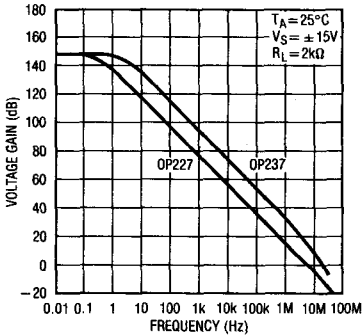


MARKER AT 2Hz (=1/f CORNER) =

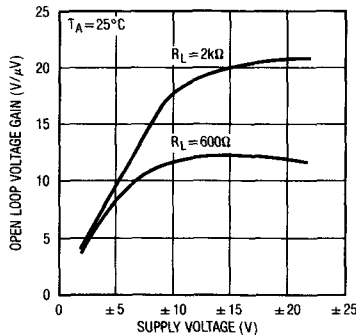
$$\frac{179 \mu\text{V}/\sqrt{\text{Hz}}}{50,000} = 3.59 \frac{\text{nV}}{\sqrt{\text{Hz}}}$$

TYPICAL PERFORMANCE CHARACTERISTICS

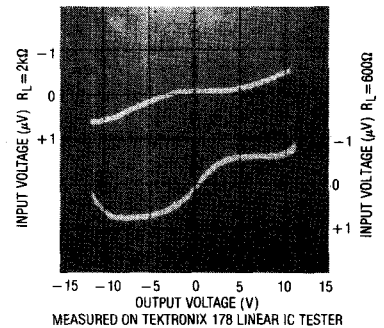
Voltage Gain vs Frequency



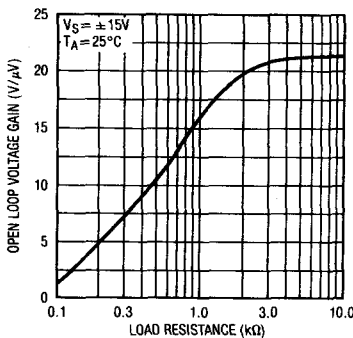
Voltage Gain vs Supply Voltage



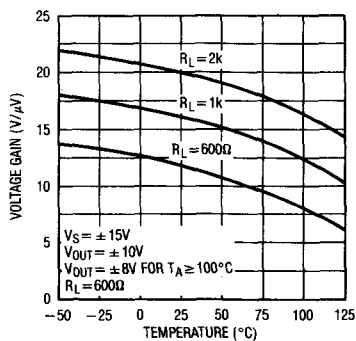
Voltage Gain, $R_L = 2k$ and 600Ω



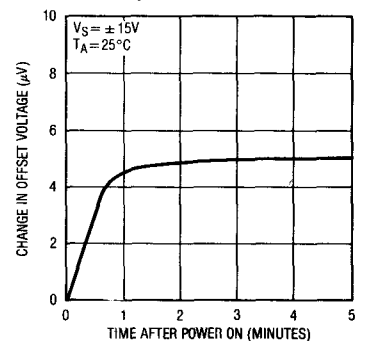
Voltage Gain vs Load Resistance



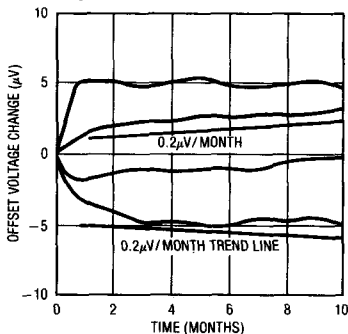
Voltage Gain vs Temperature



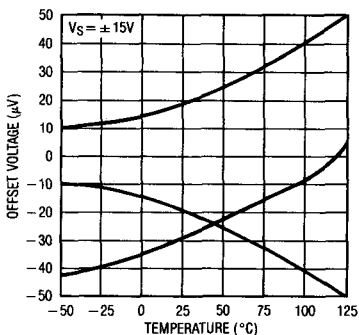
Warm-Up Drift



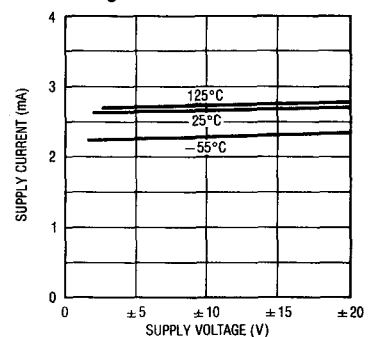
Long Term Stability of Four Representative Units



Offset Voltage Drift with Temperature of Representative Units

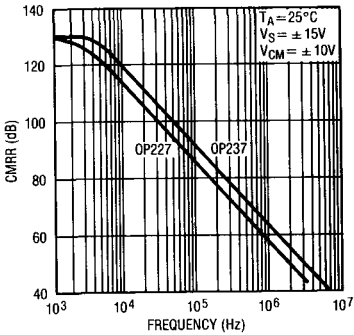


Supply Current vs Supply Voltage

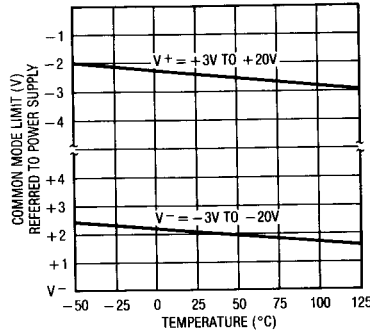


TYPICAL PERFORMANCE CHARACTERISTICS

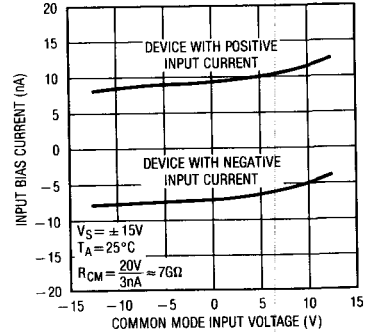
Common Mode Rejection vs Frequency



Common Mode Limit vs Temperature

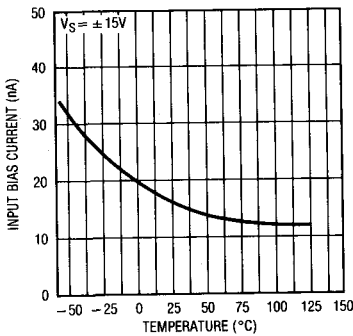


Input Bias Current Over the Common Mode Range

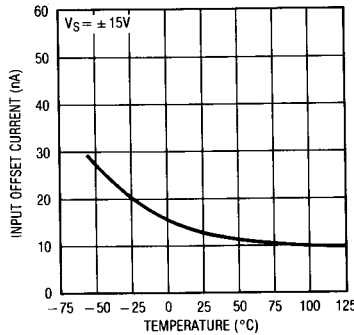


2

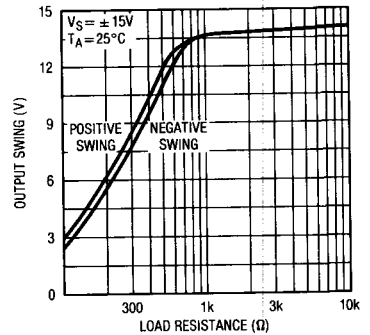
Input Bias Current vs Temperature



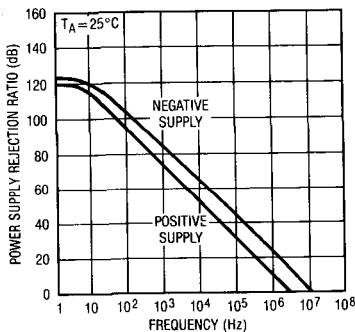
Input Offset Current vs Temperature



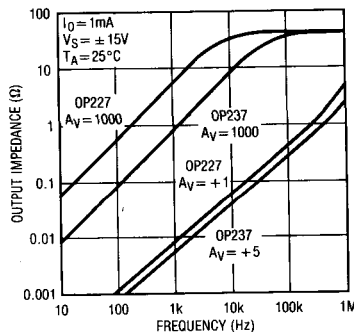
Output Swing vs Load Resistance



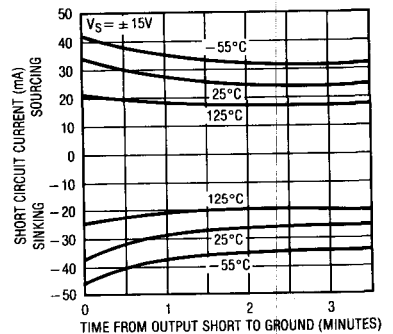
PSRR vs Frequency



Closed Loop Output Impedance

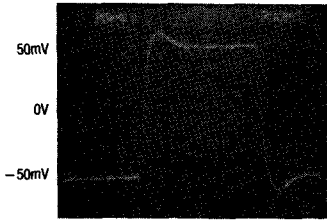


Output Short Circuit Current vs Time



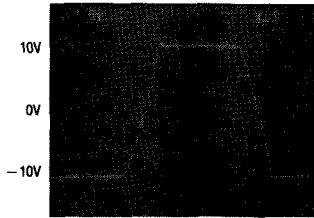
TYPICAL PERFORMANCE CHARACTERISTICS

OP-237 Small Signal Transient Response



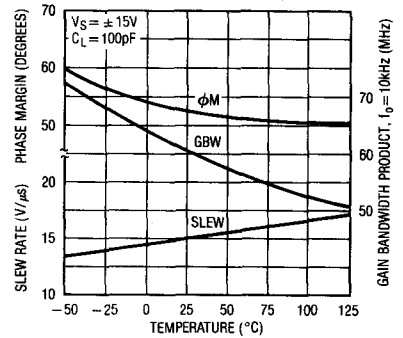
$A_{VCL} = +5V$, $V_S = \pm 15V$
 $C_L = 15pF$

OP-237 Large Signal Response

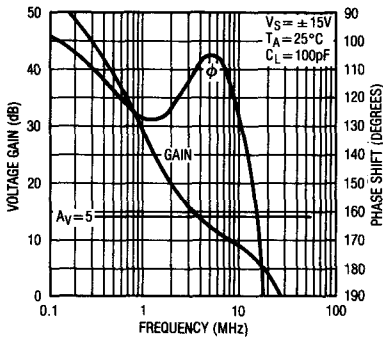


$A_{VCL} = +5$, $V_S = \pm 15V$

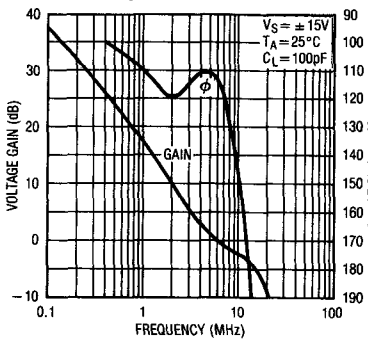
OP-237 Phase Margin, Gain Bandwidth Product, Slew Rate vs Temperature



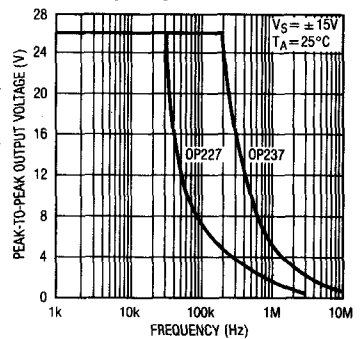
OP-237 Gain, Phase Shift vs Frequency



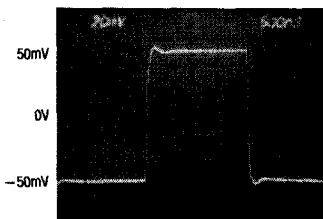
OP-227 Gain, Phase Shift vs Frequency



Maximum Undistorted Output vs Frequency

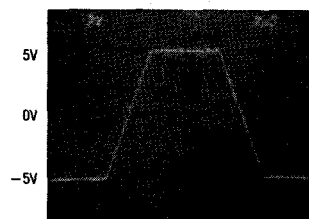


OP-227 Small Signal Transient Response



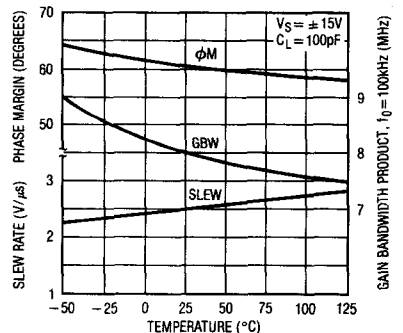
$A_{VCL} = +1$, $V_S = \pm 15V$
 $C_L = 15pF$

OP-227 Large Signal Response



$A_{VCL} = -1$, $V_S = \pm 15V$

OP-227 Phase Margin, Gain Bandwidth Product, Slew Rate vs Temperature



APPLICATIONS INFORMATION

Noise Testing

The 0.1Hz to 10Hz peak-to-peak noise of the OP-227/OP-237 is measured in the test circuit shown. The frequency response of this noise tester indicates that the 0.1Hz corner is defined by only one zero. The test time to measure 0.1Hz to 10Hz noise should not exceed 10 seconds, as this time limit acts as an additional zero to eliminate noise contributions from the frequency band below 0.1Hz.

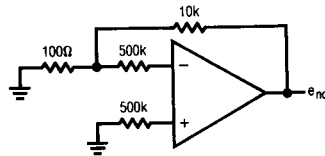
Measuring the typical 60nV peak-to-peak noise performance of the OP-227/OP-237 requires special test precautions:

- The device should be warmed up for at least five minutes. As the op amp warms up, its offset voltage changes typically 3 μ V due to its chip temperature increasing 10°C to 20°C from the moment the power supplies are turned on. In the 10 second measurement interval these temperature-induced effects can easily exceed tens of nanovolts.
- For similar reasons, the device must be well shielded from air currents to eliminate the possibility of thermoelectric effects in excess of a few nanovolts, which would invalidate the measurements.
- Sudden motion in the vicinity of the device can also "feed through" to increase the observed noise.

A noise-voltage density test is recommended when measuring noise on a large number of units. A 10Hz noise voltage density measurement will correlate well with a 0.1Hz to 10Hz peak-to-peak noise reading since both results are determined by the white noise and the location of the 1/f corner frequency.

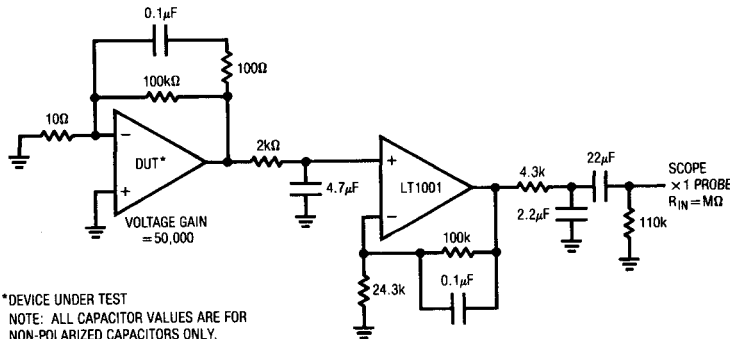
Current noise is measured in the circuit shown and calculated by the following formula:

$$i_n = \frac{[e_{no}^2 - (130nV)^2]^{1/2}}{1M\Omega \times 100}$$



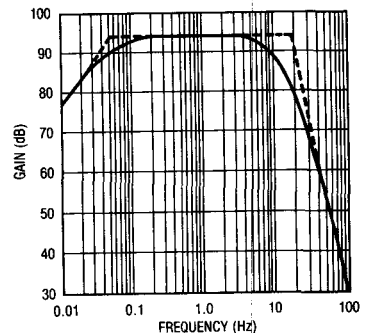
The OP-227/OP-237 achieves its low noise, in part, by operating the input stage at 120 μ A versus the typical 10 μ A of most other op amps. Voltage noise is inversely proportional, while current noise is directly proportional to the square root of the stage current. Therefore, the OP-227/OP-237 current noise will be relatively high. At low frequencies, the low 1/f current noise corner frequency (\approx 120Hz) minimizes current noise to some extent.

0.1Hz to 10Hz Noise Test Circuit



*DEVICE UNDER TEST
NOTE: ALL CAPACITOR VALUES ARE FOR NON-POLARIZED CAPACITORS ONLY.

0.1Hz to 10Hz p-p Noise Tester Frequency Response



APPLICATIONS INFORMATION

In most practical applications, however, current noise will not limit system performance. This is illustrated in the total noise versus source resistance plot, where total noise = $[(\text{voltage noise})^2 + (\text{current noise} \times R_S)^2 + (\text{resistor noise})^2]^{1/2}$.

Three regions can be identified as a function of source resistance:

- (i) $R_S \leq 400\Omega$ - Voltage noise dominates

- (ii) $400\Omega \leq R_S \leq 50k\Omega$ at 1kHz Resistor noise dominates
 $400\Omega \leq R_S \leq 8k\Omega$ at 10Hz dominates
- (iii) $R_S > 50k\Omega$ at 1kHz Current noise dominates
 $R_S > 8k\Omega$ at 10Hz dominates

Clearly the OP-227/OP-237 should not be used in region (iii), where total system noise is at least six times higher than the voltage noise of the op amp, i.e., the low voltage noise specification is completely wasted.

APPLICATIONS INFORMATION

OP AMP MATCHING

Advantages of Matched Dual Op Amps

In many applications the performance of a system depends on the matching between two operational amplifiers rather than the individual characteristics of the two op amps. Two or three op amp instrumentation amplifiers, tracking voltage references and low drift active filters are some of the circuits requiring matching between two op amps.

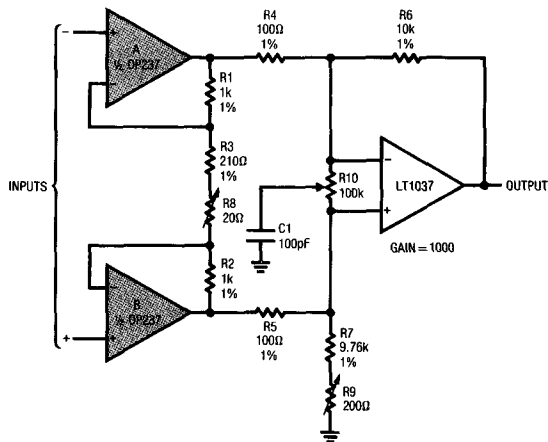
The well-known triple op amp configuration illustrates these concepts. Output offset is a function of the difference between the offsets of the two halves of the OP-227/OP-237. This error cancellation principle holds for a considerable number of input referred parameters in addition to offset voltage and its drift with temperature. Input bias current will be the average of the two non-inverting input currents (I_{B^+}). The difference between these two currents (I_{OS^+}) is the offset current of the instrumentation amplifier. The difference between the inverting input currents (I_{OS^-}) will cause errors flowing through R1, R2, and R3. Common mode and power supply rejections will be dependent only on the match between the two amplifiers (assuming perfect resistor matching).

The concepts of common mode and power supply rejection ratio match ($\Delta CMRR$ and $\Delta PSRR$) are best demonstrated with a numerical example:

Assume $CMRR_A = +1.0\mu V/V$ or 120dB, and $CMRR_B = +0.75\mu V/V$ or 122.5dB, then $\Delta CMRR = 0.25\mu V/V$ or 132dB; if $CMRR_B = -0.75\mu V/V$ which is still 122.5dB, then $\Delta CMRR = 1.75\mu V/V$ or 115dB.

Clearly, the OP-227/OP-237, by specifying and guaranteeing all of these matching parameters, can significantly improve the performance of matching dependent circuits.

Three Op Amp Instrumentation Amplifier



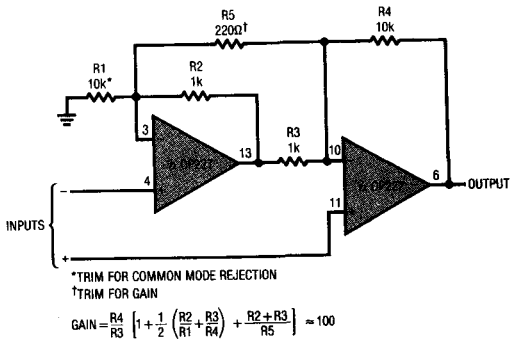
- Trim R8 for gain
- Trim R9 for DC common mode rejection
- Trim R10 for AC common mode rejection

Typical performance of the instrumentation amplifier:

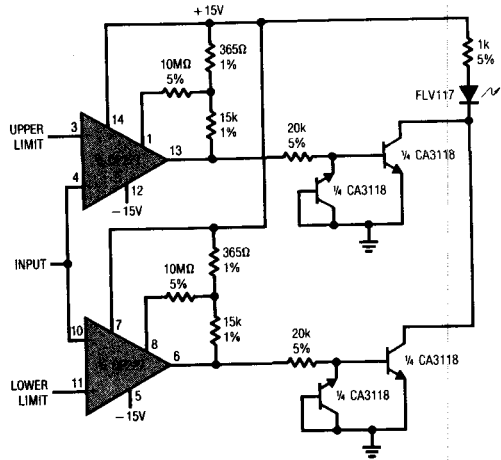
- Input offset voltage = $60\mu V$
- Input bias current = $\pm 15nA$
- Input offset current = $\pm 20nA$
- Input noise = $0.08\mu Vp-p$
- Power bandwidth ($V_O = \pm 10V$) = 250kHz

APPLICATIONS INFORMATION

Two Op Amp Instrumentation Amplifier

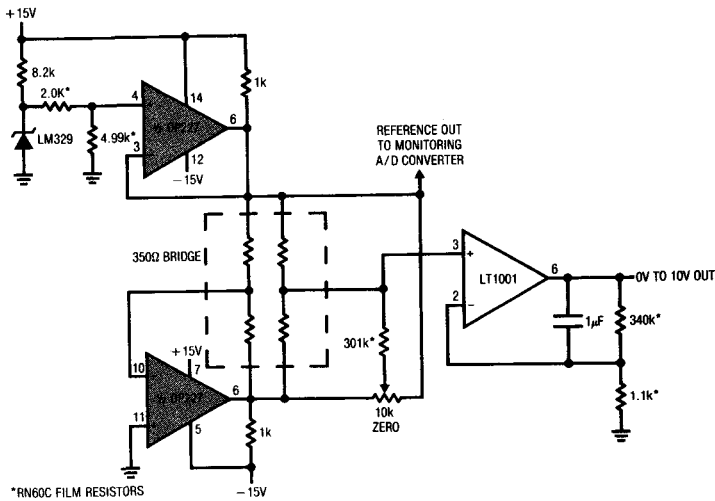


Dual Limit Microvolt Comparator



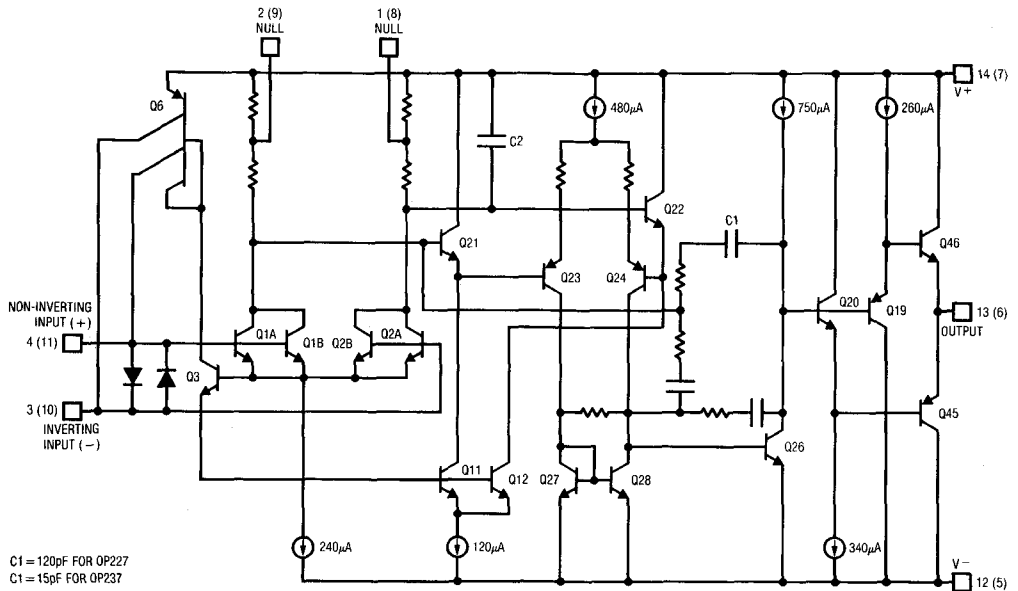
2

Strain Gauge Signal Conditioner with Bridge Excitation



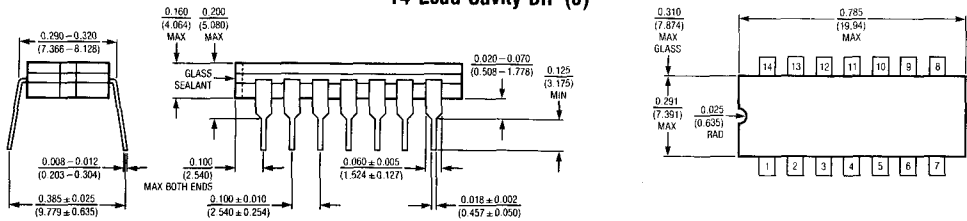
OP-227/OP-237

SCHEMATIC DIAGRAM

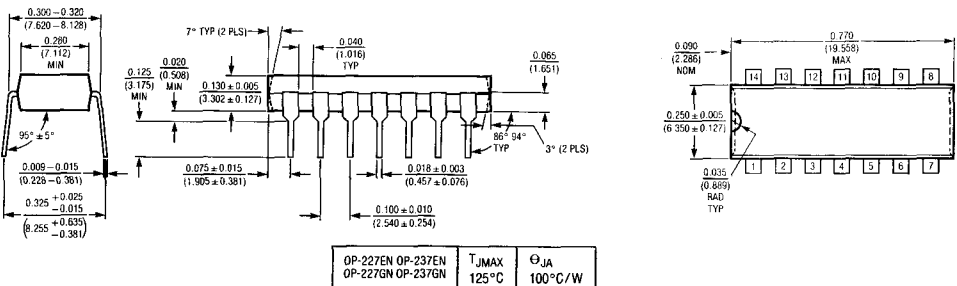


PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

14-Lead Cavity DIP (J)



14-Lead Molded DIP (N)



SECTION 3—VOLTAGE REFERENCES

3

SECTION 3—VOLTAGE REFERENCES

INDEX	3-2
SELECTION GUIDE	3-3
PROPRIETARY PRODUCTS	
<i>LTZ1000, Ultra Precision Reference</i>	3-9
<i>LTZ1000A, Ultra Precision Reference</i>	3-9
<i>LT1004, Micropower Voltage Reference</i>	3-17
<i>LT1004CS8-1.2/LT1004CS8-2.5, Micropower Voltage References</i>	3-25
<i>LT1009 Series, 2.5 Volt Reference</i>	3-27
<i>LT1009S8, 2.5 Volt Reference</i>	3-31
<i>LT1019, Precision Reference</i>	3-33
<i>LT1021, Precision Reference</i>	3-41
<i>LT1021DCS8, Precision Reference</i>	3-57
<i>LT1027, Precision 5V Reference</i>	13-8
<i>LT1029, 5V Bandgap Reference</i>	3-61
<i>LT1031, Precision 10V Reference</i>	3-65
<i>LT1034-1.2/LT1034-2.5, Micropower Dual Reference</i>	3-77
<i>LT1034CS8-1.2/LT1034CS8-2.5, Micropower Dual Reference</i>	3-81
<i>LT1431, Programmable Reference</i>	13-72
ENHANCED AND SECOND SOURCE PRODUCTS	
<i>LH0070, Precision 10V Reference</i>	3-65
<i>LM129/LM329, 6.9V Precision Voltage Reference</i>	3-83
<i>LM134 Series, Constant Current Source and Temperature Sensor</i>	3-87
<i>LM334S8, Constant Current Source and Temperature Sensor</i>	3-99
<i>LM136-2.5/LM336-2.5, 2.5 Volt Reference</i>	3-101
<i>LM185-1.2/LM385-1.2, Micropower Voltage Reference</i>	3-105
<i>LM185-2.5/LM385-2.5, Micropower Voltage Reference</i>	3-109
<i>LM385S8-1.2/LM385S8-2.5, Micropower Voltage Reference</i>	3-113
<i>LM199/LM399/LM199A/LM399A, Precision Reference</i>	3-115
<i>LT580, Precision Reference</i>	3-121
<i>LT581, Precision Reference</i>	3-121
<i>REF-01/REF-02, Precision Voltage References</i>	3-125

MILITARY
 -55°C to +125°C

VOLTAGE V_Z (VOLTS)	VOLTAGE TOLERANCE MAXIMUM $T_A = 25^\circ\text{C}$	DEVICE	TEMPERATURE DRIFT, ppm/°C OR mV CHANGE	OPERATING CURRENT RANGE (OR SUPPLY CURRENT)	MAXIMUM DYNAMIC IMPEDANCE (Ω)	MAJOR FEATURE
1.235	$\pm 0.32\%$	LT1004M-1.2	20ppm (typ)	10 μ A to 20mA	1.5	Micropower
	$\pm 1\%$	LM185-1.2	20ppm (typ)	10 μ A to 20mA	1.5	Micropower
	$\pm 1\%$	LT1034BM-1.2	20ppm (max)	20 μ A to 20mA	1.5	Low TC Micropower with 7V Aux. Reference
	$\pm 1\%$	LT1034M-1.2	40ppm (max)	20 μ A to 20mA	1.5	Low TC Micropower with 7V Aux. Reference
2.5	$\pm 0.5\%$	LT1004M-2.5	20ppm (typ)	20 μ A to 20mA	1.5	Micropower
	$\pm 0.2\%$	LT1009M	18mV (max)	400 μ A to 10mA	1.0	Precision
	$\pm 0.2\%$	LT1019M-2.5	25ppm (max)	1.2mA	N/A	Precision Bandgap
	$\pm 2\%$	LM136-2.5	18mV (max)	400 μ A to 10mA	1.0	General Purpose
	$\pm 1\%$	LM136A-2.5	18mV (max)	400 μ A to 10mA	1.0	General Purpose
	$\pm 1.5\%$	LM185-2.5	20ppm (typ)	20 μ A to 20mA	1.5	Micropower
	$\pm 1\%$	LT580S	55ppm (max)	1.5mA	N/A	3 Terminal Low Drift
	$\pm 0.4\%$	LT580T	25ppm (max)	1.5mA	N/A	3 Terminal Low Drift
$\pm 0.4\%$	LT580U	10ppm (max)	1.5mA	N/A	3 Terminal Low Drift	
4.5	$\pm 0.2\%$	LT1019M-4.5	25ppm(max)	1.2mA	N/A	Precision Bandgap
5.0	$\pm 0.2\%$	LT1019M-5	25ppm (max)	1.2mA	N/A	Precision Bandgap
	$\pm 1\%$	LT1021BM-5	5ppm (max)	1.2mA	0.1	Very Low Drift
	$\pm 0.05\%$	LT1021CM-5	20ppm (max)	1.2mA	0.1	Very Low Initial Tolerance
	$\pm 1\%$	LT1021DM-5	20ppm (max)	1.2mA	0.1	Low Cost, High Performance
	$\pm 0.2\%$	LT1029AM	20ppm (max)	100 μ A to 10mA	0.6	Precision Bandgap
	$\pm 1\%$	LT1029M	40ppm (max)	700 μ A to 10mA	0.6	Precision Bandgap
	$\pm 0.3\%$	REF02A	8.5ppm (max)	1.4mA	N/A	Precision Bandgap
$\pm 0.5\%$	REF02	25ppm (max)	1.4mA	N/A	Precision Bandgap	
6.9	$\pm 3\%$	LM129A	50ppm (max)	100 μ A to 15mA	0.8 (typ)	Low Drift
	$\pm 3\%$	LM129B	20ppm (max)	600 μ A to 15mA	0.8 (typ)	Low Drift
	$\pm 3\%$	LM129C	50ppm (max)	600 μ A to 15mA	0.8 (typ)	Low Cost
6.95	$\pm 0.1\%$	LM199A	5ppm (max) -55°C to +85°C	500 μ A to 10mA	1.0	Ultra Low Drift
	$\pm 2\%$	LM199	1ppm (max) +85°C to +125°C 1ppm (max) -55°C to +85°C 15ppm (max) +85°C to +125°C	500 μ A to 10mA	1.0	Ultra Low Drift
7.0	$\pm 0.7\%$	LT1021BM-7	5ppm (max)	1.0mA	0.2	Low Drift/Noise, Exc. Stability
	$\pm 0.7\%$	LT1021DM-7	20ppm (max)	1.0mA	0.2	Low Cost, High Performance
10.0	$\pm 0.2\%$	LT1019M-10	25ppm (max)	1.2mA	N/A	Precision Bandgap
	$\pm 0.5\%$	LT1021BM-10	5ppm (max)	1.7mA	0.25	Very Low Drift
	$\pm 0.05\%$	LT1021CM-10	20ppm (max)	1.7mA	0.25	Very Tight Initial Tolerance
	$\pm 0.5\%$	LT1021DM-10	20ppm (max)	1.7mA	0.25	Low Cost, High Performance
	$\pm 0.05\%$	LT1031BM	5ppm (max)	1.7mA	0.25	Very Low Drift
	$\pm 0.1\%$	LT1031CM	15ppm (max)	1.7mA	0.25	Very Tight Initial Tolerance
	$\pm 0.2\%$	LT1031DM	25ppm (max)	1.7mA	0.25	Low Cost, High Performance
	$\pm 0.3\%$	LT581J	30ppm (max)	1.0mA	N/A	3 Terminal Low Drift
	$\pm 0.1\%$	LT581T	15ppm (max)	1.0mA	N/A	3 Terminal Low Drift
	$\pm 0.05\%$	LH0070-2	6.7ppm (max)	5.0mA	0.6	Low Drift
	$\pm 0.1\%$	LH0070-1	17ppm (max)	5.0mA	0.6	Good Initial Tolerance
	$\pm 0.1\%$	LH0070-0	33ppm (max)	5.0mA	0.6	Low Cost, High Performance
	$\pm 0.3\%$	REF01A	8.5ppm (max)	1.4mA	N/A	Precision Bandgap
	$\pm 0.5\%$	REF01	25ppm (max)	1.4mA	N/A	Precision Bandgap

REFER TO TABLE OF CONTENTS
FOR REVISED DATA LOCATION

3

VOLTAGE REFERENCE SELECTION GUIDE

COMMERCIAL

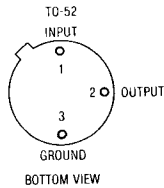
0°C to +70°C

VOLTAGE V_Z (VOLTS)	VOLTAGE TOLERANCE MAXIMUM $T_A = 25^\circ\text{C}$	DEVICE	TEMPERATURE DRIFT, ppm/°C OR mV CHANGE	OPERATING CURRENT RANGE (OR SUPPLY CURRENT)	MAXIMUM DYNAMIC IMPEDANCE (Ω)	MAJOR FEATURE
1.235	$\pm 0.32\%$	LT1004C-1.2	20ppm (typ)	10 μA to 20mA	1.5	Micropower
	$\pm 0.32\%$	LT1004CS8-1.2	20ppm (typ)	10 μA to 20mA	1.5	Micropower
	$\pm 1\%$	LT1034BC-1.2	20ppm (max)	20 μA to 20mA	1.5	Low TC Micropower with 7V Aux. Reference
	$\pm 1\%$	LT1034C-1.2	40ppm (max)	20 μA to 20mA	1.5	Low TC Micropower with 7V Aux. Reference
	$\pm 2\%$	LM385-1.2	20ppm (typ)	15 μA to 20mA	1.5	Micropower
2.5	$\pm 0.5\%$	LT1004C-2.5	20ppm (typ)	20 μA to 20mA	1.5	Micropower
	$\pm 0.8\%$	LT1004CS8-2.5	20ppm (typ)	20 μA to 30mA	1.5	Micropower
	$\pm 0.2\%$	LT1009C	6mV (max)	400 μA to 10mA	1.4	Precision
	$\pm 2.5\%$	LT1009S8	25ppm (max)	400 μA to 20mA	0.6	Precision
	$\pm 0.2\%$	LT1019C-2.5	20ppm (max)	1.2mA	N/A	Precision Bandgap
	$\pm 4\%$	LM336-2.5	6mV (max)	400 μA to 10mA	1.4	General Purpose
	$\pm 2\%$	LM336B-2.5	6mV (max)	400 μA to 10mA	1.4	General Purpose
	$\pm 3\%$	LM385-2.5	20ppm (typ)	20 μA to 20mA	1.5	Micropower
	$\pm 1.5\%$	LM385B-2.5	20ppm (typ)	20 μA to 20mA	1.5	Micropower
	$\pm 3\%$	LT580J	85 (max)	1.5mA	N/A	3 Terminal Low Drift
	$\pm 1\%$	LT580K	40 (max)	1.5mA	N/A	3 Terminal Low Drift
	$\pm 0.4\%$	LT580L	25 (max)	1.5mA	N/A	3 Terminal Low Drift
	$\pm 0.4\%$	LT580M	10 (max)	1.5mA	N/A	3 Terminal Low Drift
4.5	$\pm 0.2\%$	LT1019C-4.5	20ppm(max)	1.2mA	N/A	Precision Bandgap
5.0	$\pm 0.2\%$	LT1019C-5	20ppm(max)	1.2mA	N/A	Precision Bandgap
	$\pm 1\%$	LT1021BC-5	20ppm(max)	1.2mA	0.1	Very Low Drift
	$\pm 0.05\%$	LT1021CC-5	20ppm(max)	1.2mA	0.1	Very Tight Initial Tolerance
	$\pm 1\%$	LT1021DC-5	20ppm(max)	1.2mA	0.1	Low Cost, High Performance
	$\pm 1\%$	LT1021BCB	20ppm(max)	1.2mA	0.1	Low Cost, High Performance
	$\pm 0.2\%$	LT1029AC	25ppm(max)	700 μA to 10mA	0.6	Precision Bandgap
	$\pm 0.3\%$	LT1029C	25ppm(max)	700 μA to 10mA	0.6	Precision Bandgap
	$\pm 0.5\%$	REF02E	8.5ppm(max)	1.4mA	N/A	Precision Bandgap
	$\pm 1\%$	REF02C	25ppm(max)	1.4mA	N/A	Precision Bandgap
	$\pm 1\%$	REF02D	65ppm(max)	1.6mA	N/A	Precision Bandgap
6.9	$\pm 0.5\%$	LM329A	10ppm(max)	600 μA to 15mA	1.0 (typ)	Low Drift
	$\pm 5\%$	LM329B	20ppm(max)	600 μA to 15mA	1.0 (typ)	Low Drift
	$\pm 5\%$	LM329C	50ppm(max)	600 μA to 15mA	1.0 (typ)	General Purpose
	$\pm 5\%$	LM329D	100ppm(max)	600 μA to 15mA	1.0 (typ)	General Purpose
	$\pm 4\%$	LTZ1000	0.1ppm/°C	4mA	20.0	Ultra Low Drift, 2ppm Long Term Stability*
6.95	$\pm 5\%$	LM399	2ppm(max)	500 μA to 10mA	1.5	Ultra Low Drift
	$\pm 5\%$	LM399A	1ppm(max)	500 μA to 10mA	1.5	Ultra Low Drift
7.0	$\pm 0.7\%$	LT1021BC-7	5ppm(max)	1.0mA	0.2	Low Drift/Noise, Exc. Stability
	$\pm 0.7\%$	LT1021DC-7	20ppm(max)	1.0mA	0.2	Low Cost, High Performance
10.0	$\pm 0.2\%$	LT1019C-10	20ppm(max)	1.2mA	N/A	Precision Bandgap
	$\pm 0.5\%$	LT1021BC-10	5ppm(max)	1.7mA	0.25	Very Low Drift
	$\pm 0.05\%$	LT1021CC-10	20ppm(max)	1.7mA	0.25	Very Tight Initial Tolerance
	$\pm 0.5\%$	LT1021DC-10	20ppm(max)	1.7mA	0.25	Low Cost, High Performance
	$\pm 0.5\%$	LT1031BC	5ppm(max)	1.7mA	0.25	Very Low Drift
	$\pm 0.1\%$	LT1031CC	15ppm(max)	1.7mA	0.25	Very Tight Initial Tolerance
	$\pm 0.2\%$	LT1031DC	25ppm(max)	1.7mA	0.25	Low Cost, High Performance
	$\pm 0.3\%$	LT581J	30ppm(max)	1.0mA	N/A	3 Terminal Low Drift
	$\pm 0.1\%$	LT581K	15ppm(max)	1.0mA	N/A	3 Terminal Low Drift
	$\pm 0.3\%$	REF01E	8.5ppm(max)	1.4mA	N/A	Precision Bandgap
	$\pm 0.5\%$	REF01H	25ppm(max)	1.4mA	N/A	Precision Bandgap
	$\pm 1\%$	REF01C	65ppm(max)	1.6mA	N/A	Precision Bandgap

*LTZ1000 requires external control and biasing circuits.

VOLTAGE REFERENCE SELECTION GUIDE

LT580



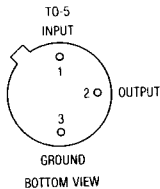
- FEATURES -

- 2.5V Output
- Direct Replacement for Analog Devices
- Selected Parts with 10ppm/°C TC
- Low Quiescent Current

- MINI DESCRIPTION -

Alternate source for industry standard 2.5V 3 terminal reference.

LT581



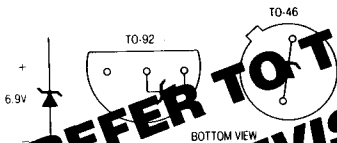
- FEATURES -

- 10V Output
- Direct Replacement for Analog Devices
- Low Quiescent Current

- MINI DESCRIPTION -

Alternate source for industry standard 10V 3-terminal reference.

LM129/329



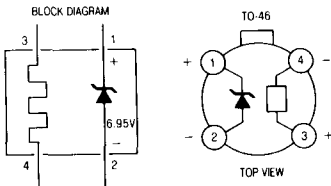
- FEATURES -

- Very Low Noise
- Low Cost
- Max Temperature Drift 50ppm/°C
- Stable over 10, 20, 50 and 100ppm/°C
- Wide Operating Current Range

- MINI DESCRIPTION -

Subsurface zener reference with wide operating current range from 600µA to 15mA. Similar to LM199/399 without stabilizing heater on the die.

LM199A/199
LM399A/399



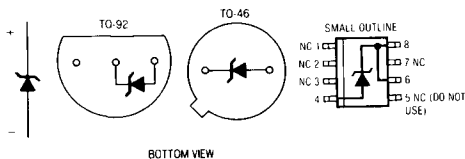
- FEATURES -

- Ultra Low Drift
- Very Low Noise
- Wide Operating Current Range
- Provided with Thermal Shield
- Excellent Long Term Stability
- Low Hysteresis
- Guaranteed Long Term Stability Available

- MINI DESCRIPTION -

An on board stabilizing heater keeps the die at constant temperature. Reference is a low noise subsurface zener. Excellent long term stability.

LT1004
LM185/385



- FEATURES -

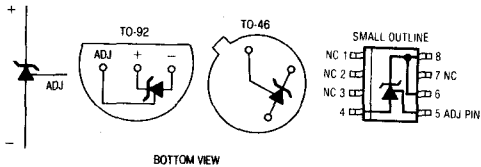
- Micropower
- 1.235V and 2.5V Available
- Low Dynamic Impedance
- Wide Operating Current Range
- Very Tight Tolerance

- MINI DESCRIPTION -

Bandgap reference with operating current range as low as 10µA. Low noise and good long term stability.

VOLTAGE REFERENCE SELECTION GUIDE

LT1009 LM136/336



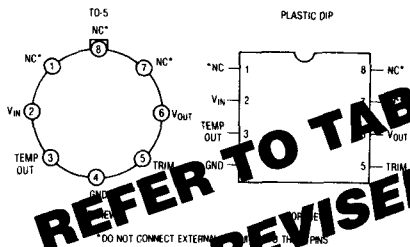
- FEATURES -

- No Adjustment Needed on LT1009
- Temperature Coefficient or Voltage Easily Adjusted on LM136
- Wide Operating Current Range
- Low Cost
- 2.5V
- Very Tight Tolerance

- MINI DESCRIPTION -

General purpose reference using bandgap circuit. Low cost, medium performance.

LT1019



- FEATURES -

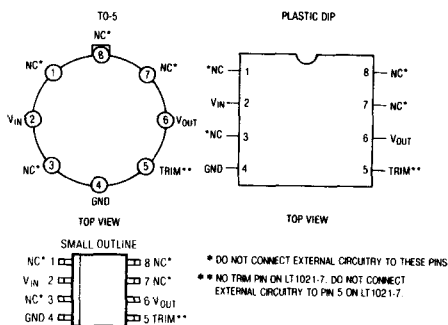
- 2.5V, 4.5V, 5V and 10V Versions
- Plus In-Place Adjustment for Many Devices
- Series or Shunt Operation
- Low Trim - 30 ppm/°C Typ.
- Very Low Noise Tested
- Optional Chip Heater Can Be Used for Lower Drift
- Temperature Output

- MINI DESCRIPTION -

Curvature corrected bandgap design for low trim and tight initial tolerance. Replaces and upgrades REF01, REF02, MC14XX and other popular series type references.

REFER TO TABLE OF CONTENTS FOR REVISED DATA LOCATION

LT1021



- FEATURES -

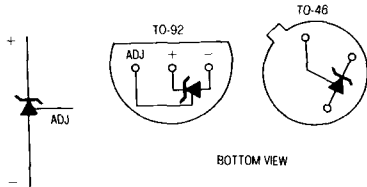
- Ultra Low Drift
- Trimmed Output Voltage
- Very Low Noise
- Operates in Series or Shunt Mode
- Replaces REF01, REF02, LM368, MC1400 and MC1404 with Improved Stability, Noise and Drift

- MINI DESCRIPTION -

Trimmed voltage reference with ultra low drift. Reference is a low noise subsurface zener. Available in 5V, 7V and 10V versions. The 7V and 10V versions can be used as 2-terminal shunt regulators as well as series references.

VOLTAGE REFERENCE SELECTION GUIDE

LT1029



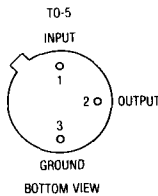
- FEATURES -

- 0.2% Output Tolerance
- 0.05Ω Shunt Impedance
- 700μA to 10mA Operating Current
- Pin Compatible with LM138-5
- 20ppm/°C Max. Drift Output Voltage Trim does not Affect Drift
- Can be Used as Positive or Negative Reference

- MINI DESCRIPTION -

Precision 3 terminal shunt 5V bandgap reference. Very low drift and tight initial output tolerance.

LT1031/LH0070



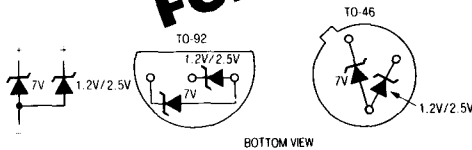
- FEATURES -

- 10V Output
- Ultra Low Drift
- Very Low Noise
- Trimmed Output Voltage
- Operates in Series or Shunt Mode
- Pin Compatible with AD581
- LT1031 is a Direct Replacement for MSC LH0070

- MINI DESCRIPTION -

Very low tempco is achieved without chip heater. TO-5 LT1031 can replace AD581 with low supply voltages.

LT1034



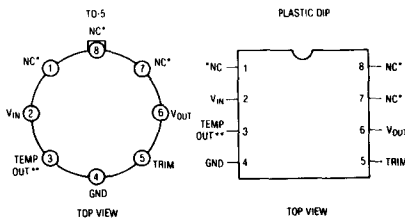
- FEATURES -

- 1.2V and 2.5 Versions
- *Guaranteed* Drift of 20ppm/°C and 40ppm/°C
- 1.2V and 7V Reference
- 1.2V Reference Operates 20μA to 20mA
- 1% Tolerance on 1.2V Reference
- 7V Reference Operates 100μA to 20mA
- Compatible with the LM385 and LT1004

- MINI DESCRIPTION -

The LT1034 is a bandgap 1.2V or 2.5V reference with low operating current and low temperature coefficient, combined with a 7V subsurface zener reference on the same chip.

REF01/REF02



- FEATURES -

- Direct Replacement for PMI Devices
- Low Drift
- High Line Rejection
- Low Supply Current
- Temperature Output on REF02

- MINI DESCRIPTION -

Industry standard 5V and 10V bandgap voltage references.

*DO NOT CONNECT EXTERNAL CIRCUITRY TO THESE PINS
**REF02 ONLY.

REFER TO TABLE OF CONTENTS FOR REVISED DATA LOCATION

NOTES

FEATURES

- 1.2 μ Vp-p Noise
- 2 μ V Long Term Stability
- Very Low Hysteresis
- 0.05ppm/ $^{\circ}$ C Drift
- Temperature Stabilized

APPLICATIONS

- Voltmeters
- Calibrators
- Standard Cells
- Scales
- Low Noise RF Oscillators

DESCRIPTION

The LTZ1000 and LTZ1000A are ultra stable temperature controllable references. They are designed to provide 7V outputs with temperature drifts of 0.05ppm/ $^{\circ}$ C, about 1.2 μ Vp-p of noise and long term stabilities of 2 μ V per month.

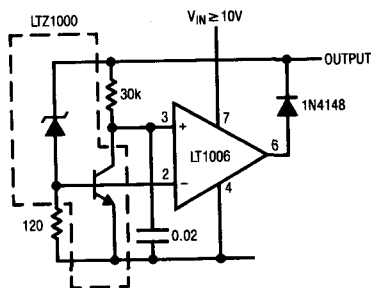
Included on the chip is a subsurface zener reference, heater resistor for temperature stabilization, and a temperature sensing transistor. External circuitry is used to set operating currents and to temperature stabilize the reference. This allows maximum flexibility and best long term stability and noise.

The LTZ1000 and LTZ1000A references can provide superior performance to older references such as the LM199 at the expense of increased circuit complexity and thermal layout considerations. The LTZ1000 is packaged in a standard TO-99 package while the LTZ1000A utilizes a proprietary high thermal resistance die attach which eases thermally insulating the reference.

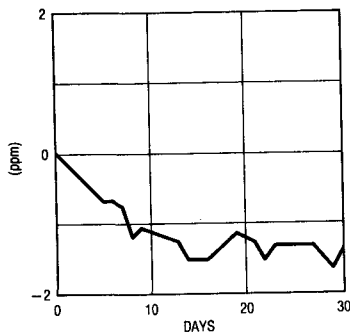
3

TYPICAL APPLICATION

Low Noise Reference



Long Term Stability



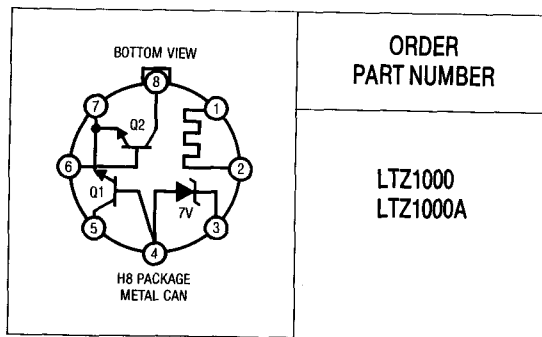
LONG TERM STABILITY OF A TYPICAL DEVICE FROM TIME = 0
 WITH NO PRECONDITIONING OR AGING

LTZ1000/LTZ1000A

ABSOLUTE MAXIMUM RATINGS

Heater to Substrate	35V
Collector Emitter Breakdown Q1	15V
Collector Emitter Breakdown Q2	35V
Emitter Base Reverse Bias	2V
Operating Temperature Range	$-55^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$
Storage Temperature Range	$-65^{\circ}\text{C} \leq T_A \leq 150^{\circ}\text{C}$
Substrate Forward Bias	0.1V

PACKAGE/ORDER INFORMATION



ORDER
PART NUMBER

LTZ1000
LTZ1000A

PRECONDITIONING

150°C Burn-In

ELECTRICAL CHARACTERISTICS (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Zener Voltage	$I_Z = 5\text{mA}$, $(V_Z + V_{BE_{Q1}})$ $I_{Q1} = 100\mu\text{A}$ $I_Z = 1\text{mA}$, $(V_Z + V_{BE_{Q1}})$ $I_{Q1} = 100\mu\text{A}$	7.0 6.9	7.2 7.15	7.5 7.45	V V
Zener Change with Current	$1\text{mA} \leq I_Z < 5\text{mA}$		80	240	mV
Zener Leakage Current	$V_Z = 5\text{V}$		20	200	μA
Zener Noise	$I_Z = 5\text{mA}$, $0.1\text{Hz} < f < 10\text{Hz}$ $I_{Q1} = 100\mu\text{A}$		1.2	2	$\mu\text{Vp-p}$
Heater Resistance	$I_L \leq 100\mu\text{A}$	200	300	420	Ω
Heater Breakdown Voltage		35			V
Transistor Q1 Breakdown	$I_C = 10\mu\text{A}$, LVCEO	15	20		V
Transistor Q2 Breakdown	$I_C = 10\mu\text{A}$, LVCEO	35	50		V
Q1, Q2 Current Gain	$I_C = 100\mu\text{A}$	80	200	450	
Thermal Resistance	LTZ1000 Time = 5 Minutes LTZ1000A Time = 5 Minutes		80 400		$^{\circ}\text{C/W}$ $^{\circ}\text{C/W}$
Long Term Stability	$T = 65^{\circ}\text{C}$		2		$\mu\text{V}/\sqrt{\text{KHR}}$

Note 1: All testing is done at 25°C. Pulse testing is used for LTZ1000A to minimize temperature rise during testing. LTZ1000 and LTZ1000A devices are QA tested at -55°C and 125°C.

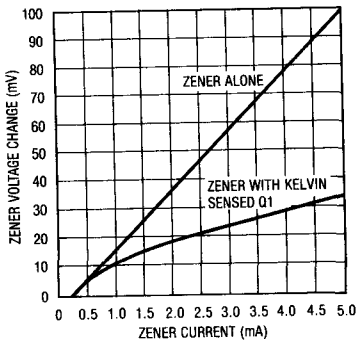
PIN FUNCTIONS

- Pin 1:** Heater positive. Must be more positive than Pin 4 and less than 40V.
- Pin 2:** Heater negative. Must be more positive than Pin 4 and less than 40V.
- Pin 3:** Zener positive. Must be more positive than Pin 4.
- Pin 4:** Substrate and Zener negative. Must be more positive than pin 7. If Q1 is Zenered (about 7V) a permanent degradation in beta will result.

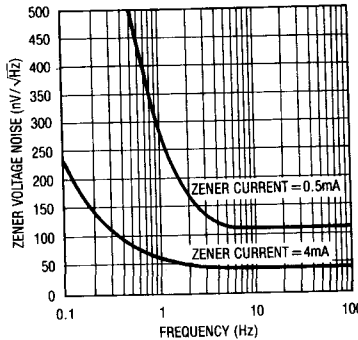
- Pin 5:** Temperature compensating transistor collector.
- Pin 6:** Temperature sensing transistor base. If the base emitter junction is Zenered (about 7V) the transistor will suffer permanent beta degradation.
- Pin 7:** Emitter of sensing and compensating transistors.
- Pin 8:** Collector of sensing transistor.

TYPICAL PERFORMANCE CHARACTERISTICS

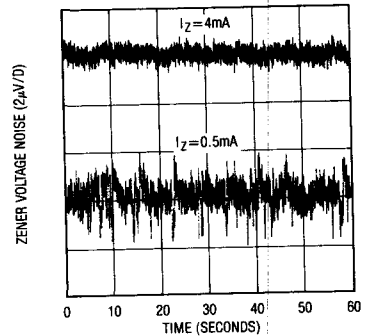
Zener Voltage vs Current



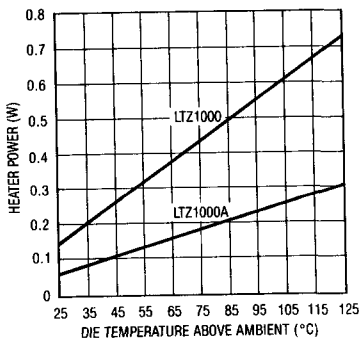
Zener Voltage Noise Spectrum



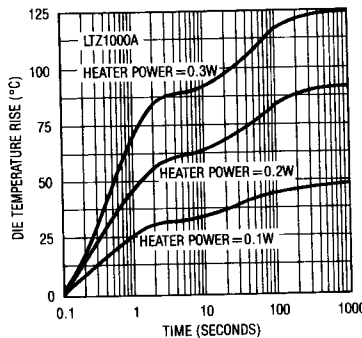
Zener Noise



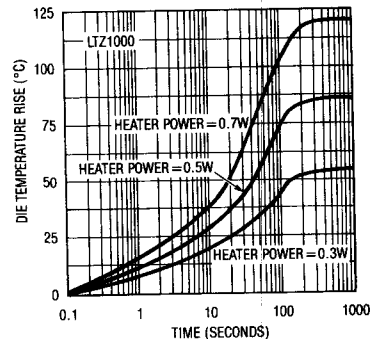
Die Temperature Rise vs Heater Power



Die Temperature Rise vs Time



Die Temperature Rise vs Time



APPLICATION HINTS

LTZ1000 and LTZ1000A are capable of providing ultimate voltage reference performance. Temperature drifts of better than $0.03\text{ppm}/^\circ\text{C}$ and long term stability on the order of $1\mu\text{V}$ per month can be achieved. Noise of about 0.15ppm can also be obtained. This performance is at the expense of circuit complexity, since external influences can easily cause output voltage shifts of more than 1ppm .

Thermocouple effects are one of the worst problems and can give apparent drifts of many $\text{ppm}/^\circ\text{C}$ as well as cause low frequency noise. The kovar input leads of the TO-5 package form thermocouples when connected to copper PC boards. These thermocouples generate outputs of $35\mu\text{V}/^\circ\text{C}$. It is mandatory to keep the zener and transistor leads at the same temperature, otherwise 1 to 5ppm shifts in the output voltage can easily be expected from these thermocouples.

Air currents blowing across the leads can also cause small temperature variations, especially since the package is heated. This will look like 1 to 5ppm of low frequency noise occurring over a several minute period. For best results, the device should be located in an enclosed area and well shielded from air currents.

Certainly, any temperature gradient externally generated, say from a power supply, should not appear across the critical circuitry. The leads to the transistor and zener should be connected to equal size PC traces to equalize the heat loss and maintain them at similar temperatures. The bottom portion of the PC board should be shielded against air currents as well.

Resistors, as well as having resistance temperature coefficients, can generate thermocouple effects. Some types of resistors can generate hundreds of microvolts of thermocouple voltage. These thermocouple effects in the resistor can also interfere with the output voltage. Wire wound resistors usually have the lowest thermocouple voltage, while tin oxide type resistors have very high thermocouple voltage. Film resistors, especially Vishay precision film resistors, can have low thermocouple voltage.

Ordinary breadboarding techniques are not good enough to give stable output voltage with the LTZ1000 family devices. For breadboarding, it is suggested that a small printed circuit board be made up using the reference, the amplifier, and wire wound resistors. Care must be taken to ensure that heater current does not flow through the same ground lead as the negative side of the reference (emitter of Q1). Current changes in the heater could add to or subtract from the reference voltage causing errors with temperature. Single point grounding using low resistance wiring is suggested.

Setting Control Temperature

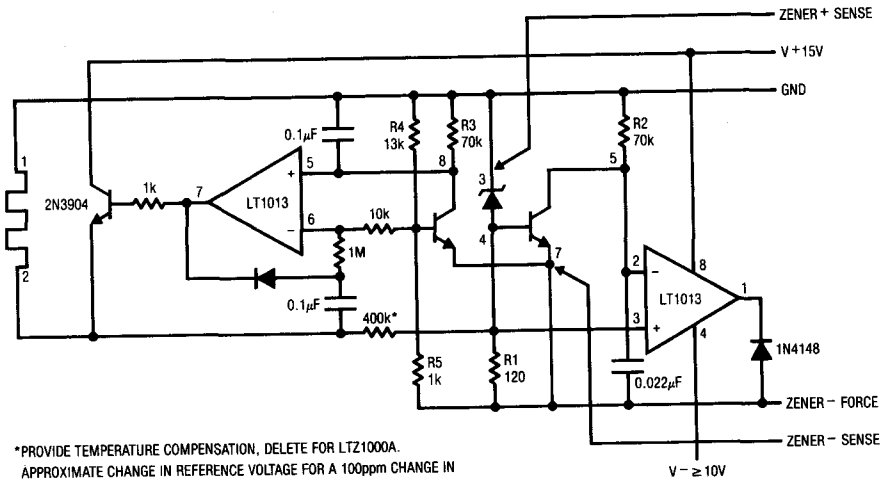
The emitter-base voltage of the control transistor sets the stabilization temperature for the LTZ1000. With the values given in the applications, temperature is normally 60°C . Production variations in emitter-base voltage will typically cause about $\pm 10^\circ\text{C}$ variation. Since the emitter-base voltage changes about $2\text{mV}/^\circ\text{C}$ and is very predictable, other temperatures are easily set.

The lowest temperature consistent with the operating environment should be used. Higher temperatures accelerate aging and decrease long term stability. The LTZ1000A should be set about 10°C higher than the LTZ1000. This is because normal operating power dissipation in the LTZ1000A causes a temperature rise of about 10°C . Of course both types of devices should be insulated from ambient. Several minutes of warm-up is usual.

For applications not requiring the extreme precision or the low noise of the LTZ1000, Linear Technology makes a broad line of voltage references. Devices like the LT1021 can provide drifts as low as $2\text{ppm}/^\circ\text{C}$ and devices such as the LM399A can provide drifts of $1\text{ppm}/^\circ\text{C}$. Only applications requiring the very low noise or low drift with time of the LTZ1000 should use this device. Application help is available from Linear Technology.

TYPICAL APPLICATIONS

Negative Voltage Reference



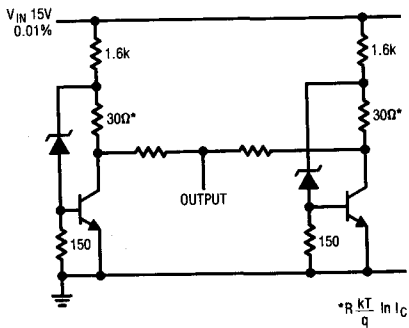
*PROVIDE TEMPERATURE COMPENSATION. DELETE FOR LTZ1000A.
 APPROXIMATE CHANGE IN REFERENCE VOLTAGE FOR A 100ppm CHANGE IN RESISTOR VALUES:

	$100\text{ppm} = \Delta R(\Omega)$	ΔV_Z
R1	0.012 Ω	1ppm
R2	7 Ω	0.3ppm
R3	7 Ω	0.2ppm
R4/R5 RATIO	$\Delta R = 0.01\%$	1ppm

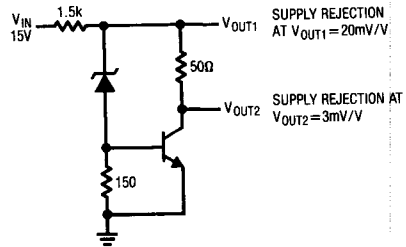
BOTH A1 AND A2 CONTRIBUTE LESS THAN 2 μV OF OUTPUT DRIFT OVER A 50°C RANGE.

3

Averaging Reference Voltages for Lower Noise and Better Stability

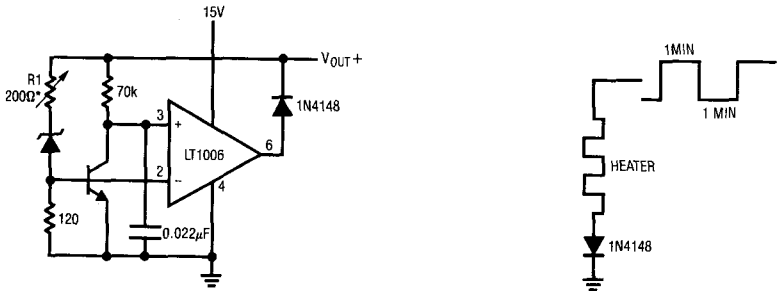


Improving Supply Rejection



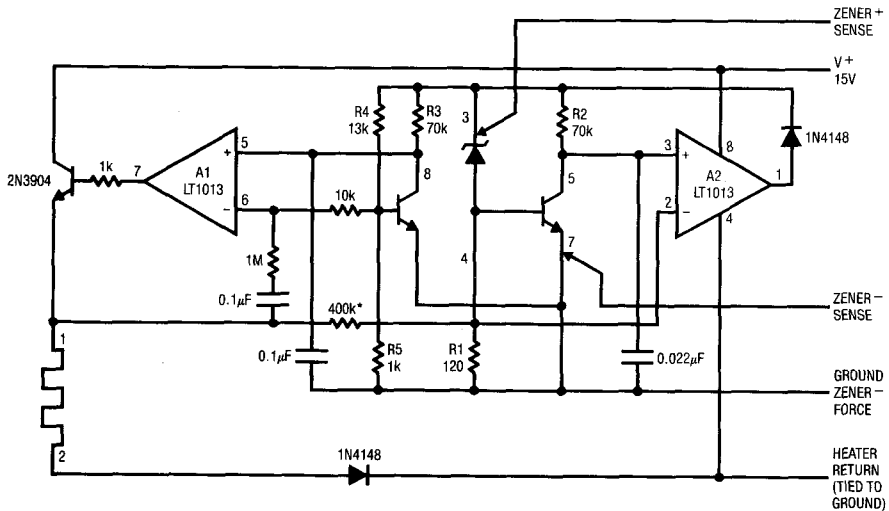
TYPICAL APPLICATIONS

Adjusting Temperature Coefficient in Unstabilized Applications



*PULSE HEATER ON AND OFF TO HEAT AND COOL THE REFERENCE. ADJUST R1 FOR MINIMUM VOLTAGE CHANGE THROUGH A TEMPERATURE CYCLE.

7V Positive Reference Circuit



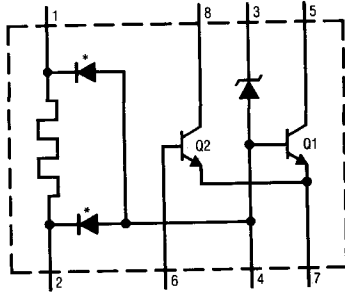
*PROVIDES TC COMPENSATION, DELETE FOR LTZ1000A.

APPROXIMATE CHANGE IN REFERENCE VOLTAGE FOR A 100ppm (0.01%) CHANGE IN RESISTOR VALUES:

	$\Delta R(\Omega)$	ΔV_2
R1	0.012 Ω	1ppm
R2	7 Ω	0.3ppm
R3	7 Ω	0.2ppm
R4/R5 RATIO	$\Delta R=0.01\%$	1ppm

BOTH A1 AND A2 CONTRIBUTE LESS THAN 2 μ V OF OUTPUT DRIFT OVER A 50°C RANGE.

BLOCK DIAGRAM

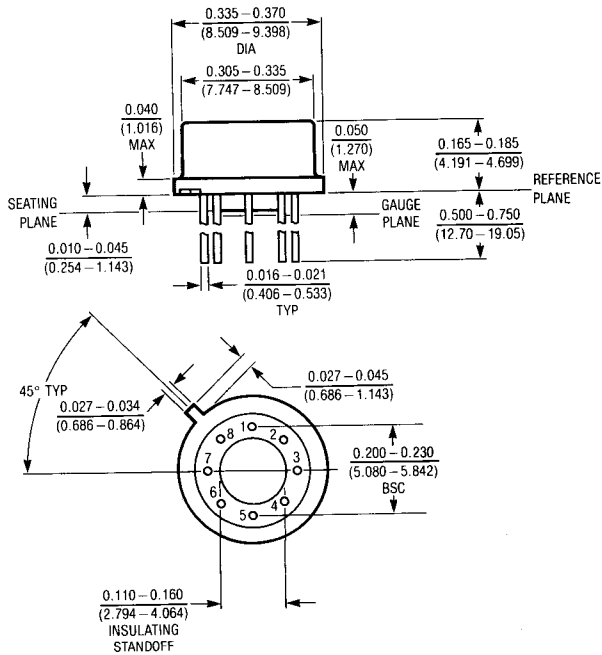


*SUBSTRATE DIODES-DO NOT FORWARD BIAS

PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

3

**H8 Package
Metal Can**



NOTE: LEAD DIAMETER IS UNCONTROLLED BETWEEN THE REFERENCE PLANE AND SEATING PLANE.

H8188

LTZ1000	θ_{JA}
LTZ1000A	80°C/W
	400°C/W

NOTES

FEATURES

- *Guaranteed* $\pm 4\text{mV}$ initial accuracy LT1004-1.2
- *Guaranteed* $\pm 20\text{mV}$ accuracy LT1004-2.5
- *Guaranteed* $10\mu\text{A}$ operating current
- *Guaranteed* temperature performance
- Operates up to 20mA
- Very low dynamic impedance

APPLICATIONS

- Portable meter references
- Portable test instruments
- Battery operated systems
- Current loop instrumentation

DESCRIPTION

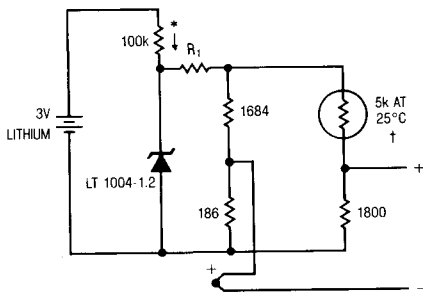
The LT1004 Micropower Voltage References are two terminal bandgap reference diodes designed to provide high accuracy and excellent temperature characteristics at very low operating currents. Optimization of the key parameters in the design, processing and testing of the device results in accuracy specifications previously attainable only with selected units. Below is a distribution plot of reference voltage for a typical lot of LT1004-1.2. Virtually all of the units fall well within the prescribed limits of $\pm 4\text{mV}$.

The LT1004 is a pin for pin replacement for the LM185/385 series of references with improved accuracy specifications. More important, the LT1004 is an attractive device for use in systems where accuracy was previously obtained at the expense of power consumption and trimming.

For a low drift micropower reference with guaranteed temperature coefficient, see the LT1034 data sheet.

3

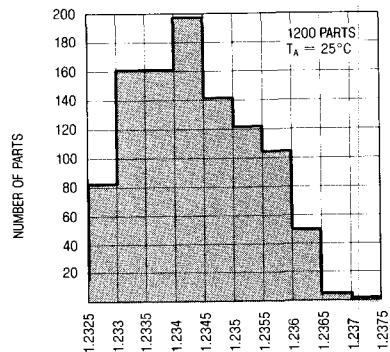
Micropower Cold Junction Compensation For Thermocouples



THERMOCOUPLE TYPE	R_1
J	233k
K	299k
T	300k
S	2.1M

* QUIESCENT CURRENT $\approx 15\mu\text{A}$
 † YELLOW SPRINGS INST. CO.
 PART #44007
 COMPENSATES WITHIN
 $\pm 1^\circ\text{C}$ FROM 0°C TO 60°C

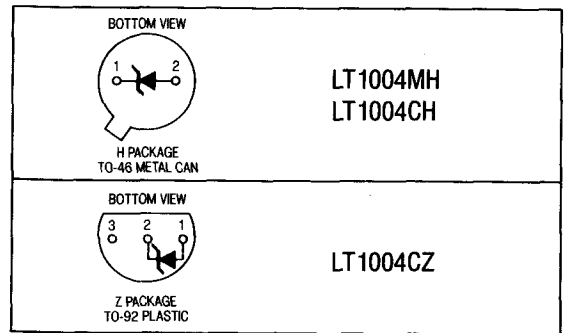
Typical Distribution of Reference Voltage (LT1004-1.2)



ABSOLUTE MAXIMUM RATINGS

Reverse Breakdown Current 30mA
 Forward Current 10mA
 Operating Temperature Range
 LT1004M -55°C to 125°C
 LT1004C 0°C to 70°C
 Storage Temperature Range
 LT1004M -65°C to 150°C
 LT1004C -65°C to 150°C
 Lead Temperature (Soldering, 10 sec.) 300°C

PACKAGE/ORDER INFORMATION



ELECTRICAL CHARACTERISTICS (See Note 1)

SYMBOL	PARAMETER	CONDITIONS	LT1004-1.2			LT1004-2.5			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_Z	Reverse Breakdown Voltage	$I_R = 100\mu A$	1.231	1.235	1.239	2.480	2.500	2.520	V
		LT1004M $-55^\circ C \leq T_A \leq 125^\circ C$	1.220	1.230	1.245	2.460	2.500	2.535	V
		LT1004M/C $0^\circ C \leq T_A \leq 70^\circ C$	1.225	1.235	1.245	2.470	2.500	2.530	V
$\frac{\Delta V_Z}{\Delta Temp}$	Average Temperature Coefficient	$I_{min} \leq I_R \leq 20mA$ (Note 2)	20			20			ppm/°C
I_{min}	Minimum Operating Current		8 10			12 20			μA
$\frac{\Delta V_Z}{\Delta I_R}$	Reverse Breakdown Voltage Change with Current	$I_{min} \leq I_R \leq 1mA$				1 1.5			mV
		$1mA \leq I_R \leq 20mA$				10 10			mV
						20 20			mV
									mV
r_Z	Reverse Dynamic Impedance	$I_R = 100\mu A$	0.2 0.6			0.2 0.6			Ω
			1.5			1.5			Ω
e_n	Wide Band Noise (RMS)	$I_R = 100\mu A$ $10Hz \leq f \leq 10kHz$	60			120			μV
$\frac{\Delta V_Z}{\Delta Time}$	Long Term Stability	$I_R = 100\mu A$ $T_A = 25^\circ C \pm 0.1^\circ C$	20			20			ppm/kHr

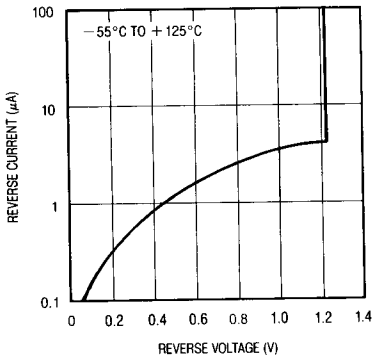
The ● denotes the specifications which apply over the full operating temperature range.

Note 1: All specifications are for $T_A = 25^\circ C$ unless otherwise noted.

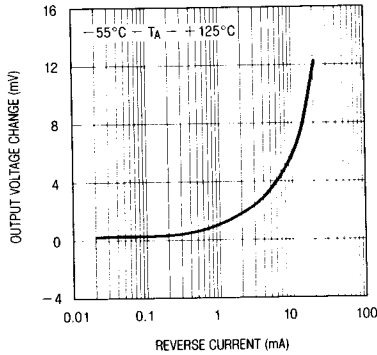
Note 2: Selected devices with guaranteed maximum temperature coefficient are available upon request.

TYPICAL PERFORMANCE CHARACTERISTICS 1.2 VOLT

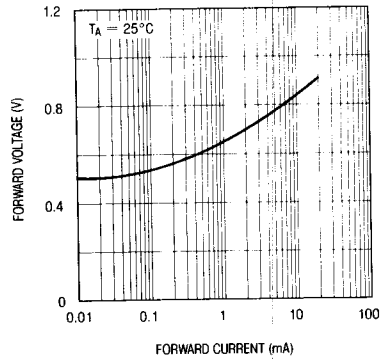
Reverse Characteristics



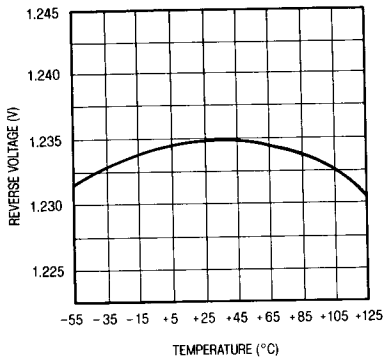
Reverse Voltage Change



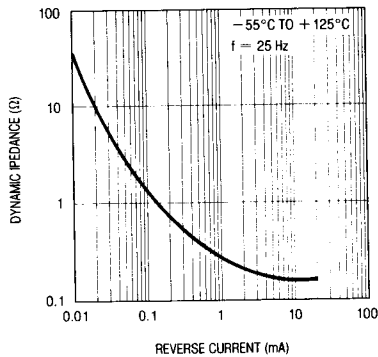
Forward Characteristics



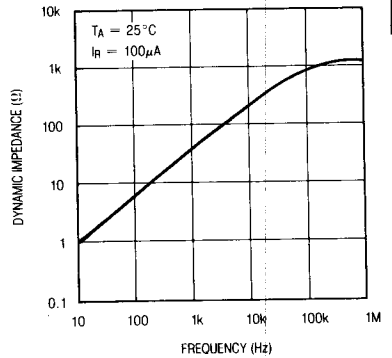
Temperature Drift



Reverse Dynamic Impedance

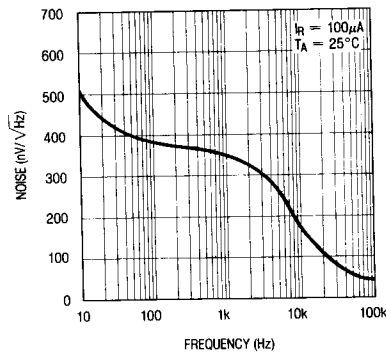


Reverse Dynamic Impedance

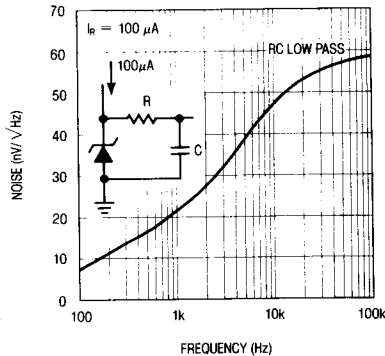


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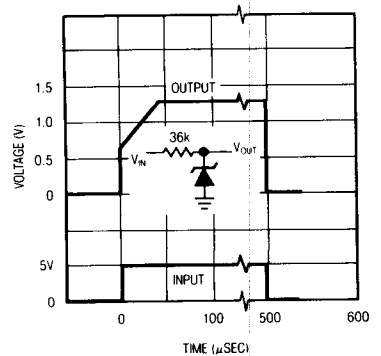
Noise Voltage



Filtered Output Noise

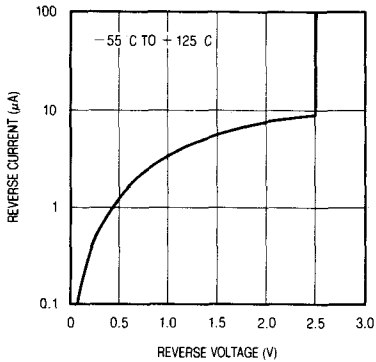


Response Time

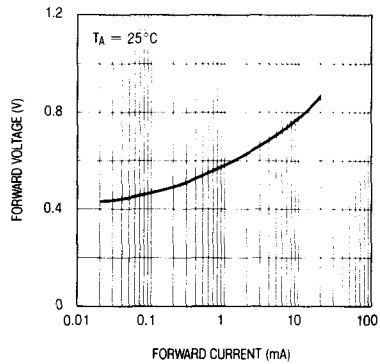


TYPICAL PERFORMANCE CHARACTERISTICS 2.5 VOLT

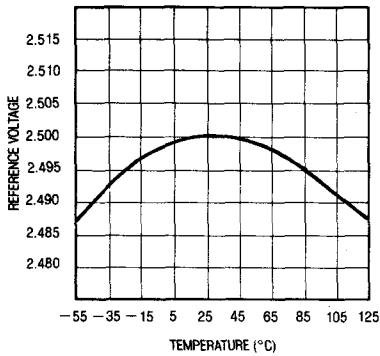
Reverse Characteristics



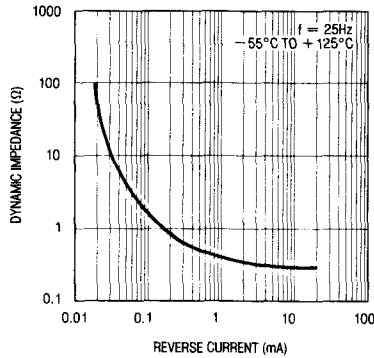
Forward Characteristics



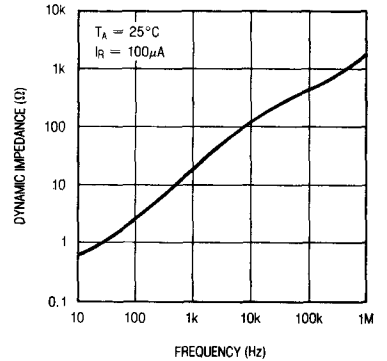
Temperature Drift



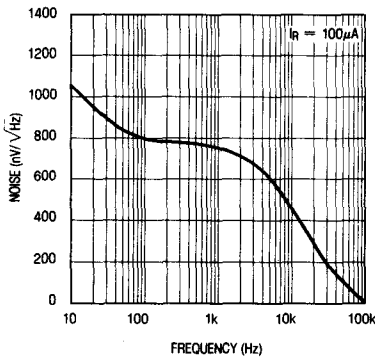
Reverse Dynamic Impedance



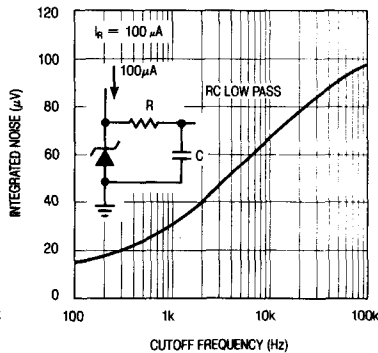
Reverse Dynamic Impedance



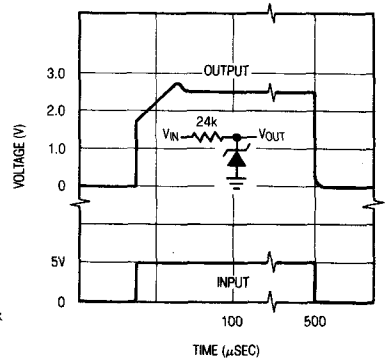
Noise Voltage



Filtered Output Noise

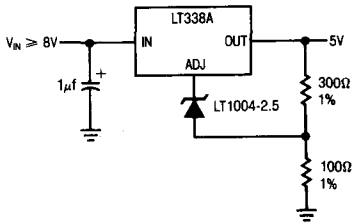


Response Time

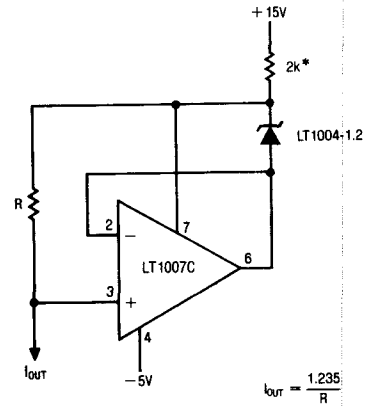


TYPICAL APPLICATIONS

High Stability 5V Regulator



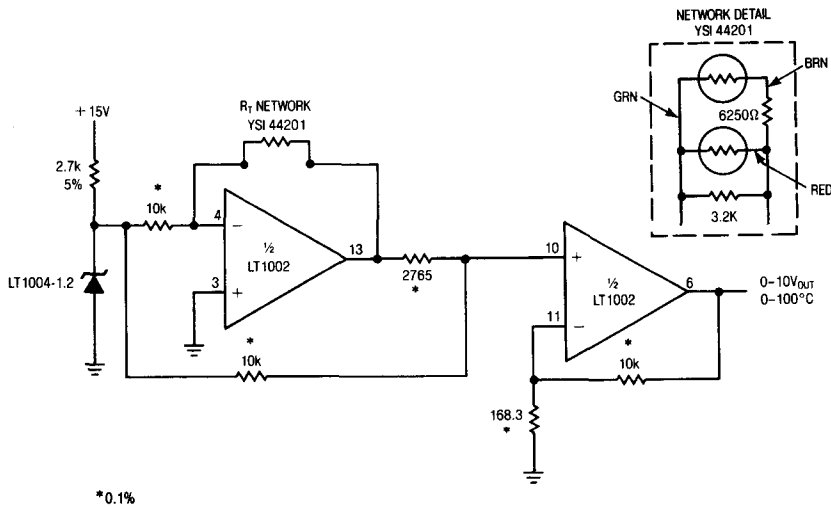
Ground Referenced Current Source



* MAY BE INCREASED FOR SMALL OUTPUT CURRENTS
 $R \approx \frac{2V}{I_{OUT} + 10\mu A}$

$$I_{OUT} = \frac{1.235}{R}$$

0-100°C Linear Output Thermometer

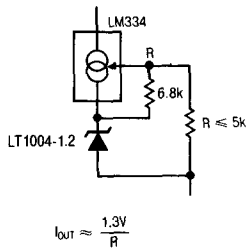


* 0.1%

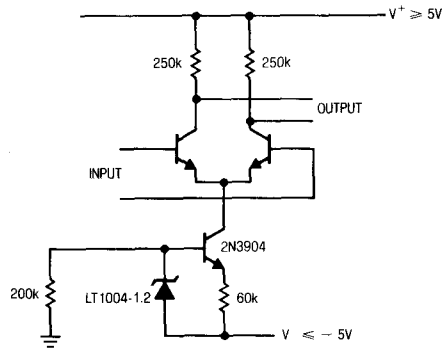
3

TYPICAL APPLICATIONS

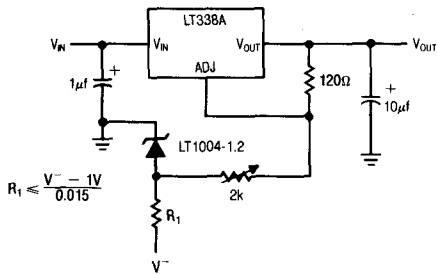
**Low Temperature Coefficient
2 Terminal Current Source**



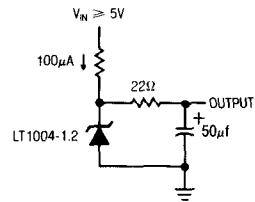
**Constant Gain Amplifier
Over Temperature**



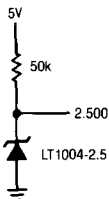
Variable Output Supply



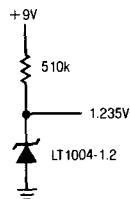
Low Noise Reference



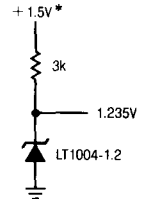
2.5V Reference



**Micropower Reference
from 9V Battery**



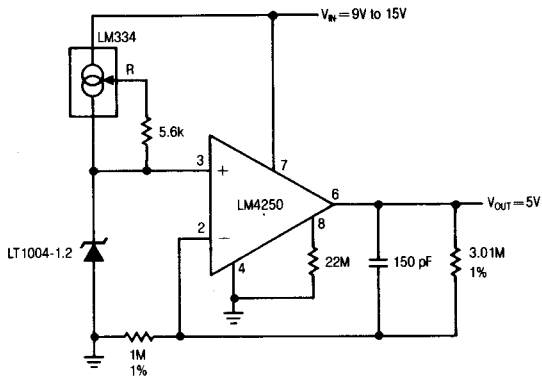
1.2V Reference from 1.5V Battery



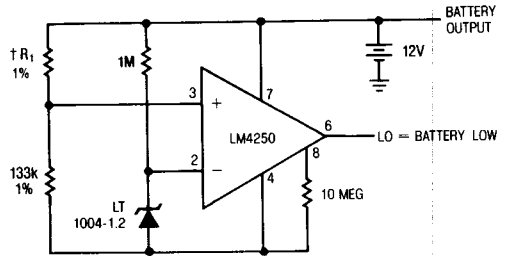
* OUTPUT REGULATES
DOWN TO 1.285V
FOR $I_{out} = 0$

TYPICAL APPLICATIONS

Micropower 5V Reference



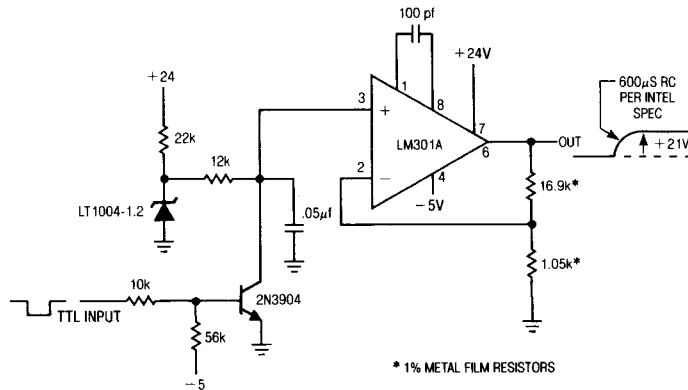
Lead Acid Low Battery Detector



† R₁ SETS TRIP POINT, 60.4K PER CELL FOR 1.8V/CELL

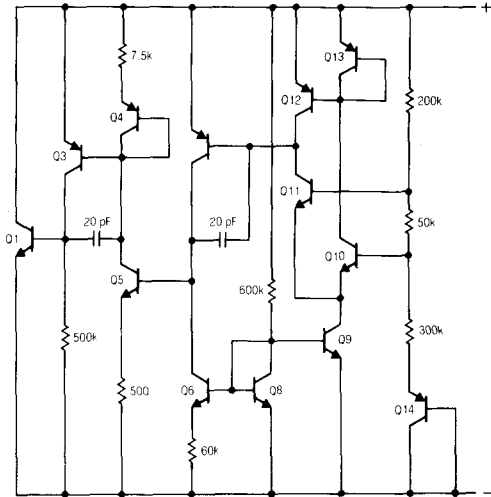
3

V_{pp} Generator for Eproms — No Trim Required

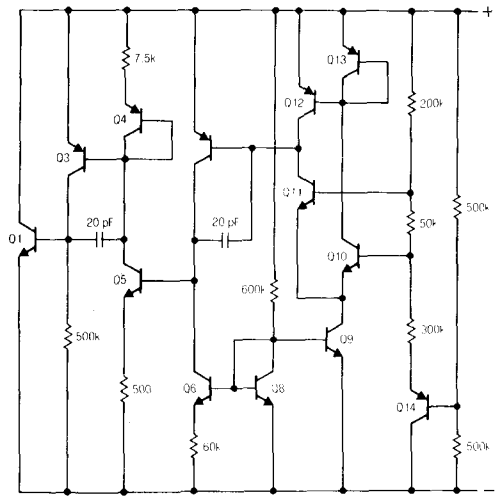


SCHEMATIC DIAGRAM

LT1004-1.2

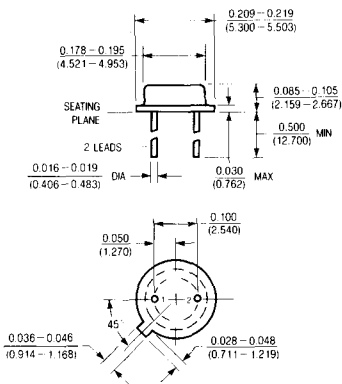


LT1004-2.5



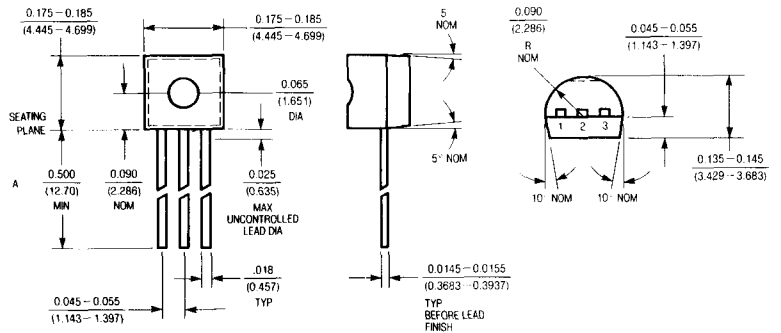
PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

H Package, 2 Lead TO-46 Metal Can



T_{max}	θ_{ja}	θ_{jc}
150°C	440°C/W	80°C/W

Z Package, 3 Lead TO-92 Plastic



T_{max}	θ_{ja}
100°C	160°C/W

FEATURES

- *Guaranteed* $\pm 4\text{mV}$ initial accuracy LT1004-1.2
- *Guaranteed* $\pm 20\text{mV}$ accuracy LT1004-2.5
- *Guaranteed* $10\mu\text{A}$ operating current
- *Guaranteed* temperature performance
- Operates up to 20mA
- Very low dynamic impedance

APPLICATIONS

- Portable meter references
- Portable test instruments
- Battery operated systems
- Current loop instrumentation

DESCRIPTION

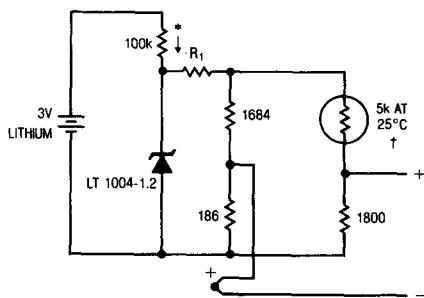
The LT1004 Micropower Voltage References are two terminal bandgap reference diodes designed to provide high accuracy and excellent temperature characteristics at very low operating currents. Optimization of the key parameters in the design, processing and testing of the device results in accuracy specifications previously attainable only with selected units. Below is a distribution plot of reference voltage for a typical lot of LT1004-1.2. Virtually all of the units fall well within the prescribed limits of $\pm 4\text{mV}$.

The LT1004 is a pin for pin replacement for the 385 series of references with improved accuracy specifications. More important, the LT1004 is an attractive device for use in systems where accuracy was previously obtained at the expense of power consumption and trimming.

For a low drift micropower reference with guaranteed temperature coefficient, see the LT1034CS8 data sheet.

3

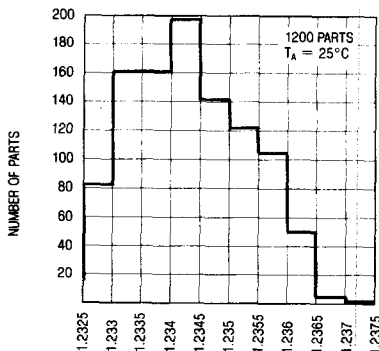
Micropower Cold Junction Compensation For Thermocouples



THERMOCOUPLE TYPE	R_1
J	233k
K	299k
T	300k
S	2.1M

* QUIESCENT CURRENT $\approx 15\mu\text{A}$
 † YELLOW SPRINGS INST. CO.
 PART #44007
 COMPENSATES WITHIN
 $\pm 1^\circ\text{C}$ FROM 0°C TO 60°C

Typical Distribution of
 Reference Voltage (LT1004-1.2)



LT1004CS8-1.2/
LT1004CS8-2.5

ABSOLUTE MAXIMUM RATINGS

Reverse Breakdown Current 30mA
 Forward Current 10mA
 Operating Temperature Range 0°C to 70°C
 Storage Temperature Range -65°C to 150°C
 Lead Temperature (Soldering, 10 sec.) 300°C

PACKAGE/ORDER INFORMATION

<p>TOP VIEW</p> <p>NC 1 2 3 4</p> <p>8 7 6 5</p> <p>NC (DO NOT USE)</p> <p>S8 PACKAGE PLASTIC SO</p>	ORDER PART NUMBER
	LT1004CS8-1.2 LT1004CS8-2.5
	PART MARKING
	0412 (1.2V VERSION) 0425 (2.5V VERSION)

ELECTRICAL CHARACTERISTICS (See Note 1)

SYMBOL	PARAMETER	CONDITIONS	LT1004-1.2			LT1004-2.5			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_Z	Reverse Breakdown Voltage	$I_R = 100\mu A$ LT1004C 0°C ≤ T _A ≤ 70°C	● 1.231	1.235	1.239	2.480	2.500	2.520	V
$\frac{\Delta V_Z}{\Delta \text{Temp}}$	Average Temperature Coefficient	$I_{min} \leq I_R \leq 20mA$		20			20		ppm/°C
I_{min}	Minimum Operating Current		● 8	10		12	20		μA
$\frac{\Delta V_Z}{\Delta I_R}$	Reverse Breakdown Voltage Change with Current	$I_{min} \leq I_R \leq 1mA$ $1mA \leq I_R \leq 20mA$	●		1 1.5 10 20		1 1.5 10 20		mV mV mV mV
r_Z	Reverse Dynamic Impedance	$I_R = 100\mu A$	●	0.2	0.6 1.5		0.2	0.6 1.5	Ω
e_n	Wide Band Noise (RMS)	$I_R = 100\mu A$ 10Hz ≤ f ≤ 10kHz		60			120		μV
$\frac{\Delta V_Z}{\Delta \text{Time}}$	Long Term Stability	$I_R = 100\mu A$ T _A = 25°C ± 0.1°C		20			20		ppm/kHr

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: All specifications are for T_A = 25°C unless otherwise noted.

FEATURES

- 0.2% Initial Tolerance Max
- *Guaranteed* Temperature Stability
- Maximum 0.6Ω Dynamic Impedance
- Wide Operating Current Range
- Directly Interchangeable with LM136 for Improved Performance
- No Adjustments Needed for Minimum Temperature Coefficient

APPLICATIONS

- Reference for 5V Systems
- 8 Bit A/D and D/A Reference
- Digital Voltmeters
- Current Loop Measurement and Control Systems
- Power Supply Monitor

DESCRIPTION

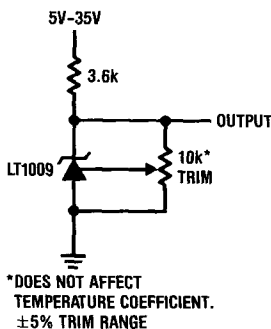
The LT1009 is a precision trimmed 2.500 Volt shunt regulator diode featuring a maximum initial tolerance of only $\pm 5\text{mV}$. The low dynamic impedance and wide operating current range enhances its versatility. The 0.2% reference tolerance is achieved by on-chip trimming which not only minimizes the initial voltage tolerance but also minimizes the temperature drift.

Even though no adjustments are needed with the LT1009, a third terminal allows the reference voltage to be adjusted $\pm 5\%$ to calibrate out system errors. In many applications, the LT1009 can be used as a pin-to-pin replacement of the LM136H-2.5 and the external trim network eliminated.

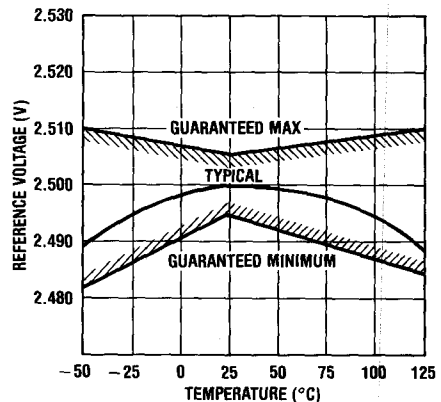
For a lower drift 2.5V reference, see the LT1019 data sheet.

3

2.5 Volt Reference




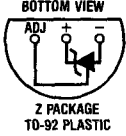
Output Voltage



ABSOLUTE MAXIMUM RATINGS

Reverse Current 20mA
 Forward Current 10mA
 Operating Temperature Range
 LT1009M -55°C to 125°C
 LT1009C 0°C to 70°C
 Storage Temperature Range
 LT1009M and C -65°C to 150°C
 Lead Temperature (Soldering, 10 sec.) 300°C

PACKAGE/ORDER INFORMATION

 <p>BOTTOM VIEW H PACKAGE TO-46 METAL CAN</p>	ORDER PART NUMBER
	LT1009MH LT1009CH
 <p>BOTTOM VIEW Z PACKAGE TO-92 PLASTIC</p>	LT1009CZ

ELECTRICAL CHARACTERISTICS

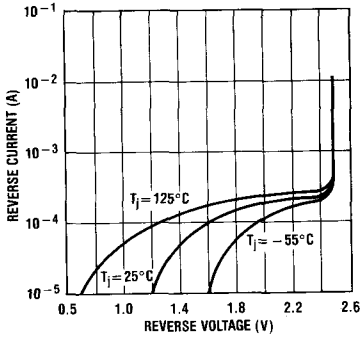
SYMBOL	PARAMETER	CONDITIONS	LT1009M			LT1009C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_Z	Reverse Breakdown Voltage	$T_A = 25^\circ\text{C}, I_R = 1\text{mA}$	2.495	2.500	2.505	2.495	2.500	2.505	V
$\frac{\Delta V_Z}{\Delta I_R}$	Reverse Breakdown Change with Current	$400\mu\text{A} \leq I_R \leq 10\text{mA}$	•	2.6 3	6 10	2.6 3	10 12		mV mV
r_Z	Reverse Dynamic Impedance	$I_R = 1\text{mA}$	•	0.2 0.4	0.6 1	0.2 0.4	1.0 1.4		Ω Ω
$\frac{\Delta V_Z}{\Delta \text{Temp}}$	Temperature Stability Average Temperature Coefficient	$T_{\text{MIN}} \leq T_A \leq T_{\text{MAX}}$ $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$ $-55^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$ (Note 1)	•		15 25 35		1.8 15 25	4 25	mV ppm/°C ppm/°C
$\frac{\Delta V_Z}{\Delta \text{Time}}$	Long Term Stability	$T_A = 25^\circ\text{C} \pm 0.1^\circ\text{C}, I_R = 1\text{mA}$		20		20			ppm/kHr

The ● denotes the specifications which apply over full operating temperature range.

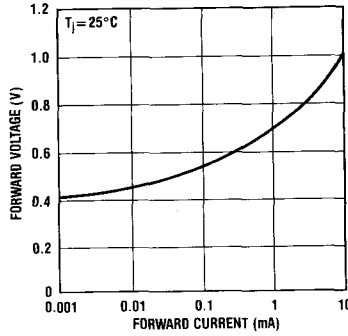
Note 1: Average temperature coefficient is defined as the total voltage change divided by the specified temperature range.

TYPICAL PERFORMANCE CHARACTERISTICS

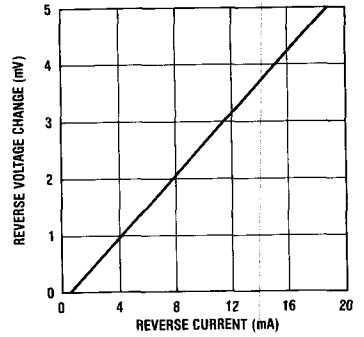
Reverse Characteristics



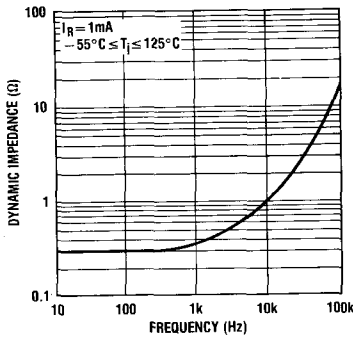
Forward Characteristics



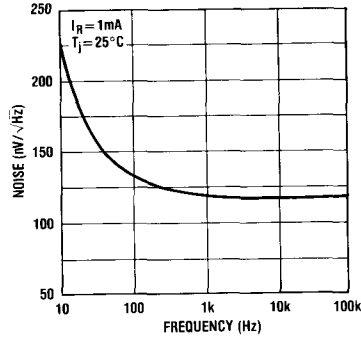
Reverse Voltage Change



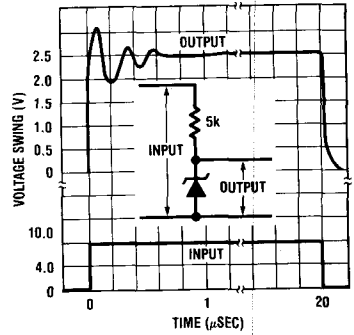
Dynamic Impedance



Zener Noise Voltage

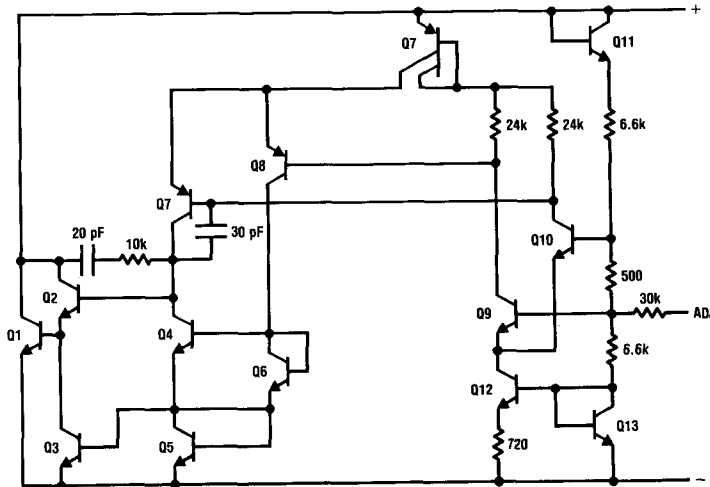


Response Time



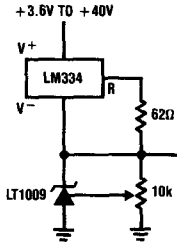
3

SCHEMATIC DIAGRAM

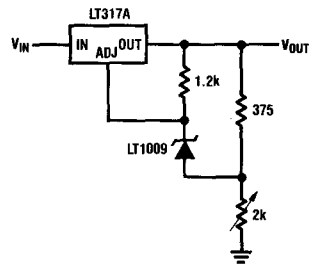


TYPICAL APPLICATIONS

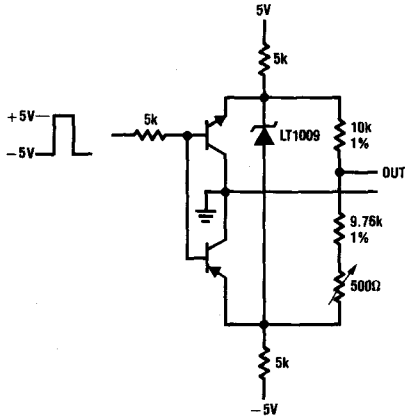
Wide Supply Range, Adjustable Reference



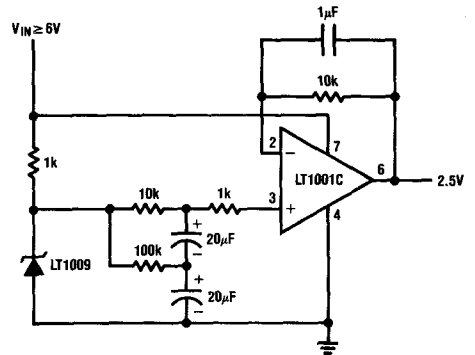
Low Temperature Coefficient Power Regulator



Switchable ±1.25V Bipolar Reference

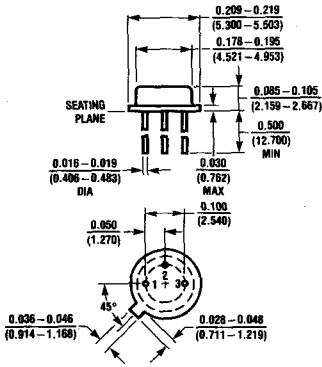


Low Noise 2.5V Buffered Reference



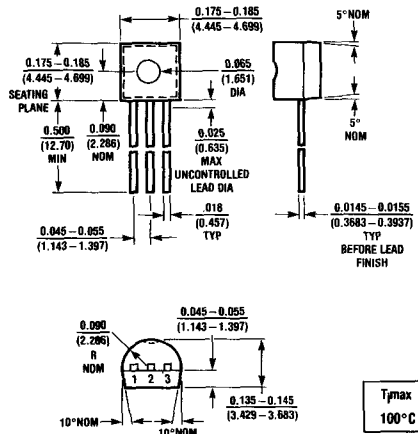
PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

**H Package
Metal Can**



T _{max}	θ _{jc}	θ _{ja}
150°C	440°C/W	80°C/W

**Z Package
Plastic**



T _{max}	θ _{ja}
100°C	160°C/W

FEATURES

- 0.4% Initial Tolerance Max
- *Guaranteed* Temperature Stability
- Maximum 0.6Ω Dynamic Impedance
- Wide Operating Current Range
- Directly Interchangeable with LM336 for Improved Performance
- No Adjustments Needed for Minimum Temperature Coefficient

APPLICATIONS

- Reference for 5V Systems
- 8 Bit A/D and D/A Reference
- Digital Voltmeters
- Current Loop Measurement and Control Systems
- Power Supply Monitor

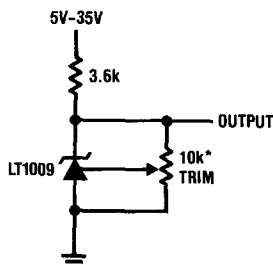
DESCRIPTION

The LT1009 is a precision trimmed 2.500 Volt shunt regulator diode featuring a maximum initial tolerance of only $\pm 10\text{mV}$. The low dynamic impedance and wide operating current range enhances its versatility. The 0.4% reference tolerance is achieved by on-chip trimming which not only minimizes the initial voltage tolerance but also minimizes the temperature drift.

Even though no adjustments are needed with the LT1009, a third terminal allows the reference voltage to be adjusted $\pm 5\%$ to calibrate out system errors. In many applications, the LT1009 can be used as a pin-to-pin replacement of the LM336-2.5 and the external trim network eliminated.

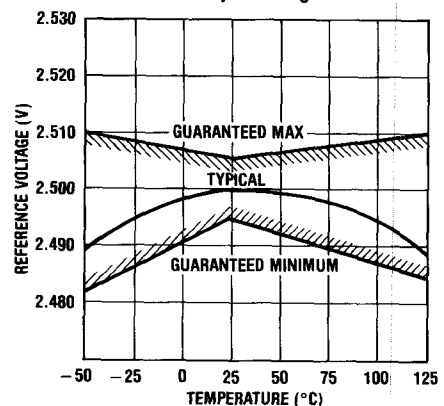
3

2.5 Volt Reference



*DOES NOT AFFECT
 TEMPERATURE COEFFICIENT.
 $\pm 5\%$ TRIM RANGE

Output Voltage



ABSOLUTE MAXIMUM RATINGS

Reverse Current	20mA
Forward Current	10mA
Operating Temperature Range	0°C to 70°C
Storage Temperature Range	-65°C to 150°C
Lead Temperature (Soldering, 10 sec.)	300°C

PACKAGE/ORDER INFORMATION

	ORDER PART NUMBER
	LT1009S8
	PART MARKING
	1009

ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	LT1009S8			UNITS
			MIN	TYP	MAX	
V_Z	Reverse Breakdown Voltage	$T_A = 25^\circ\text{C}, I_R = 1\text{mA}$	2.490	2.500	2.510	V
$\frac{\Delta V_Z}{\Delta I_R}$	Reverse Breakdown Change with Current	$400\mu\text{A} \leq I_R \leq 10\text{mA}$	●	2.6 3	10 12	mV mV
r_Z	Reverse Dynamic Impedance	$I_R = 1\text{mA}$	●	0.2 0.4	1.0 1.4	Ω Ω
$\frac{\Delta V_Z}{\Delta \text{Temp}}$	Temperature Stability Average Temperature Coefficient	$T_{\text{MIN}} \leq T_A \leq T_{\text{MAX}}$ $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$ (Note 1)	●	1.8 15	4 25	mV ppm/°C
$\frac{\Delta V_Z}{\Delta \text{Time}}$	Long Term Stability	$T_A = 25^\circ\text{C} \pm 0.1^\circ\text{C}, I_R = 1\text{mA}$		20		ppm/kHr

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: Average temperature coefficient is defined as the total voltage change divided by the specified temperature range.

FEATURES

- Available at 2.5V, 4.5V, 5V, and 10V
- Plug-In Replacement for Present References
- Ultra Low Drift—3ppm/°C Typical
- Curvature Corrected
- Series or Shunt Operation
- Ultra High Line Rejection $\approx 1/2$ ppm/V
- Low Output Impedance $\approx 0.02\Omega$
- Tight Initial Output Voltage $< 0.05\%$
- Can be Heated for Drifts below 2ppm/°C
- 100% Noise Tested
- Temperature Output

APPLICATIONS

- A to D and D to A Converters
- Precision Regulators
- Constant Current Sources
- V to F Converters
- Bridge Excitation

DESCRIPTION

The LT1019 is a third generation bandgap voltage reference utilizing thin film technology and a greatly improved curvature correction technique. Wafer level trimming of both reference and output voltage combines to produce units with high yields to very low TC and tight initial tolerance of output voltage.

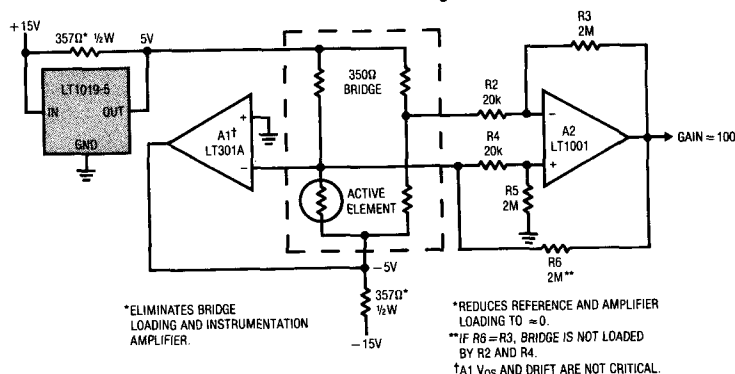
The LT1019 can both sink and source up to 10mA and can be used in either the series or shunt mode. This allows the reference to be used for both positive and negative output voltages without external components. Minimum input-output voltage is less than 1V in the series mode, providing improved tolerance of low line conditions.

The LT1019 is available in four voltages: 2.5V, 4.5V, 5V, and 10V. It is a direct replacement for most bandgap references presently available including AD580, AD581, REF-01, REF-02, MC1400, MC1404 and LM168.

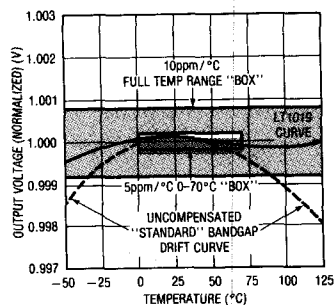
For ultra low drift applications (< 2 ppm/°C), the LT1019 can be operated in a heated mode by driving an internal resistor with an external amplifier. Chip temperature can be externally set for minimum power consumption.

For a 6.2V version of the LT1019, consult the factory.

Ultralinear Strain Gauge*



Output Voltage Drift



ABSOLUTE MAXIMUM RATINGS

Input Voltage	40V
Output Voltage (Note 1)	
LT1019-5, LT1019-10	16V
LT1019-2.5, LT1019-4.5	7V
Output Short Circuit Duration (Note 1)	
$V_{IN} \geq 20V$	Indefinite
$20V \leq V_{IN} \leq 35V$	10 sec
Trim Pin Voltage	$\pm 30V$
Temp Pin Voltage	5V
Heater Voltage	
(Continuous)	18V
(Intermittent—30 sec.)	32V

PACKAGE/ORDER INFORMATION

TOP VIEW		ORDER PART NUMBER	
<p>METAL CAN H PACKAGE *INTERNALLY CONNECTED. DO NOT CONNECT EXTERNALLY.</p>		LT1019AMH-10	LT1019AMH-4.5
		LT1019MH-10	LT1019MH-4.5
		LT1019ACH-10	LT1019ACH-4.5
		LT1019CH-10	LT1019CH-4.5
		LT1019AMH-5	LT1019AMH-2.5
		LT1019MH-5	LT1019MH-2.5
		LT1019ACH-5	LT1019ACH-2.5
		LT1019CH-5	LT1019CH-2.5
<p>PLASTIC DIP N8 PACKAGE *INTERNALLY CONNECTED. DO NOT CONNECT EXTERNALLY.</p>		LT1019ACN8-10	LT1019ACN8-4.5
		LT1019CN8-10	LT1019CN8-4.5
		LT1019ACN8-5	LT1019ACN8-2.5
		LT1019CN8-5	LT1019CN8-2.5
AVAILABLE IN SO PACKAGE			

ELECTRICAL CHARACTERISTICS $V_{IN} - V_{OUT} = 5V$, $I_{OUT} = 0$, $T_J = 25^\circ C$ unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS	LT1019A			LT1019			UNITS	
			MIN	TYP	MAX	MIN	TYP	MAX		
	Output Voltage Tolerance			0.002	0.05		0.02	0.2	%	
T_C	Output Voltage Temperature Coefficient (Note 2)	LT1019C (0°C to 70°C)	●	3	5		5	20	ppm/°C	
		LT1019M (-55°C to +125°C)	●	5	10		8	25	ppm/°C	
$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	Line Regulation (Note 3)	$(V_{OUT} + 1.5V) \leq V_{IN} \leq 40V$	●	0.5 1	3 5		0.5 1	3 5	ppm/V ppm/V	
RR	Ripple Rejection	50Hz $\leq f \leq 400$ Hz	●	90	110		90	110	dB dB	
			●	84			84			
$\frac{\Delta V_{OUT}}{\Delta I_{OUT}}$	Load Regulation Series Mode (Notes 3 and 4)	$0 \leq I_{OUT} \leq 10mA^*$	●	0.02	0.05 0.08		0.02	0.05 0.08	mV/mA (Ω) mV/mA (Ω)	
	Load Regulation, Shunt Mode	$1mA \leq I_{SHUNT} \leq 10mA$ 2.5V, 4.5V, 5V, 10V	●	0.1	0.4 0.8		0.1	0.4 0.8	mV/mA (Ω) mV/mA (Ω)	
	Thermal Regulation (Note 6)	$\Delta P = 200mW$ $t = 50ms$		0.1	0.5		0.1	0.5	ppm/mW	
I_Q	Quiescent Current Series Mode		●	0.65	1 1.3		0.65	1.2 1.5	mA mA	
			●		0.5	0.8		0.5		0.8
	Minimum Shunt Current (Note 7)		●	0.5	0.8		0.5	0.8	mA	
	Minimum Input-Output Voltage Differential	$I_{OUT} \leq 1mA$ $I_{OUT} = 10mA$	●	0.9	1.1 1.3		0.9	1.1 1.3	V V	
	Trim Range	LT1019-2.5 LT1019-5 LT1019-10		± 4 ± 4 ± 4	± 6 +5, -13 +5, -27		± 4 ± 4 ± 4	± 6 +5, -13 +5, -27	% % %	
	Heater Resistance			300	400	500	300	400	500	Ω
I_{SC}	Short Circuit Current Output Connected to Ground	$2V \leq V_{IN} \leq 35V$	●	15	25	50	15	25	50	mA mA
			●	10			10			
e_n	Output Voltage Noise (Note 9)	10Hz $\leq f \leq 1kHz$ 0.1Hz $\leq f \leq 10Hz$		2.5	4		2.5	4	ppm (Rms) ppm (p-p)	
					2.5			2.5		

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: These are high power conditions and are therefore guaranteed only at temperatures equal to or below 70°C. Input is either floating, tied to output, or held higher than output.

Note 2: Output voltage drift is measured using the box method. Output voltage is recorded at T_{MIN} , 25°C, and T_{MAX} . The lowest of these three readings is subtracted from the highest and the resultant difference is divided by $(T_{MAX} - T_{MIN})$.

Note 3: Line regulation and load regulation are measured on a pulse basis with low duty cycle. Effects due to die heating must be taken into account separately. See thermal regulation and application section.

Note 4: Load regulation is measured at a point $\frac{1}{8}$ " below the base of the package with Kelvin contacts.

Note 5: Shunt regulation is measured with the input floating. This parameter is also guaranteed with the input connected ($V_{IN} - V_{OUT}$) > 1V. $0mA \leq I_{SINK} \leq 10mA$. Shunt and sink current flow into the output.

Note 6: Thermal regulation is caused by die temperature gradients created by load current or input voltage changes. This effect must be added to normal line or load regulation.

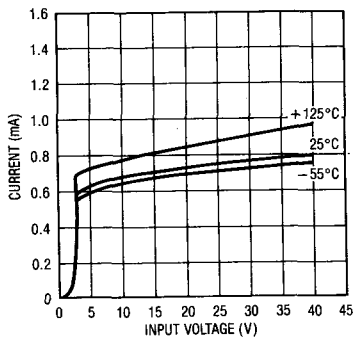
Note 7: Minimum shunt current is measured with shunt voltage held 20mV below value measured at 1mA shunt current.

Note 8: Minimum input-output voltage is measured by holding input voltage 0.5V above the nominal output voltage, while measuring $V_{IN} - V_{OUT}$.

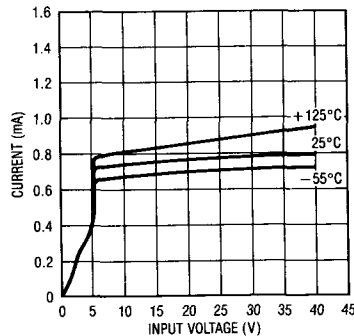
Note 9: RMS noise is measured with a single high pass filter at 10Hz and a 2-pole low pass filter at 1kHz. The resulting output is full wave rectified and then integrated for a fixed period, making the final reading an average as opposed to RMS. A correction factor of 1.1 is used to convert from average to RMS, and a second correction of 0.88 is used to correct for the non-ideal bandpass of the filters.

TYPICAL PERFORMANCE CHARACTERISTICS

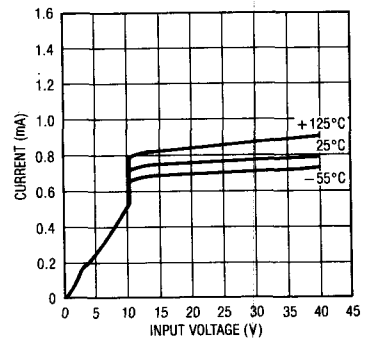
Quiescent Current (LT1019-2.5)



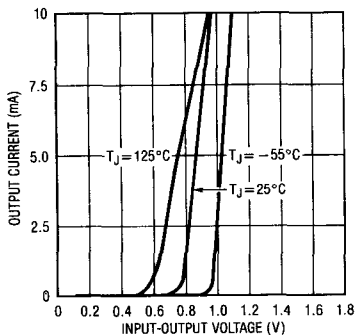
Quiescent Current (LT1019-4.5, 5)



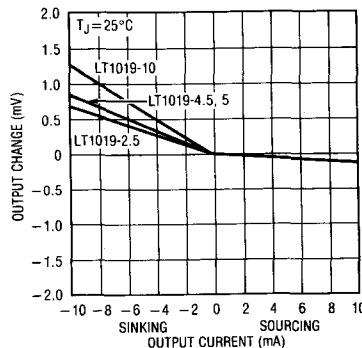
Quiescent Current (LT1019-10)



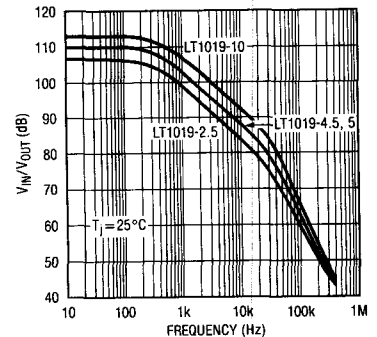
Minimum Input-Output Voltage Differential



Load Regulation

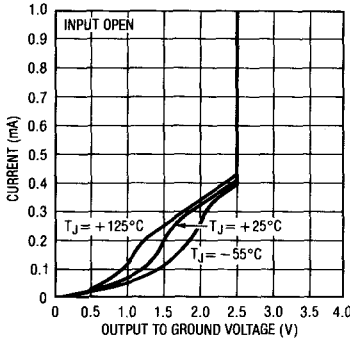


Ripple Rejection

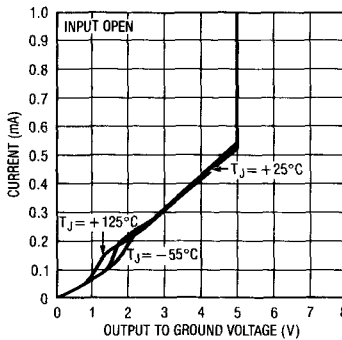


TYPICAL PERFORMANCE CHARACTERISTICS

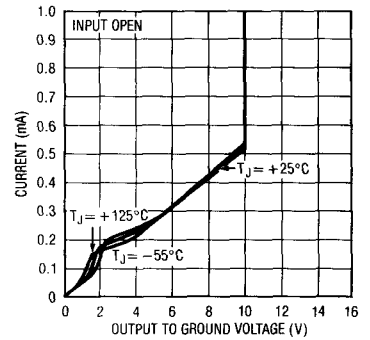
Shunt Mode Characteristics (LT1019-2.5V)



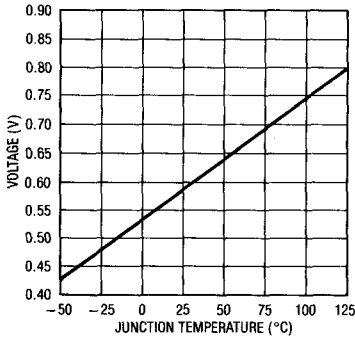
Shunt Mode Characteristics (LT1019-5)



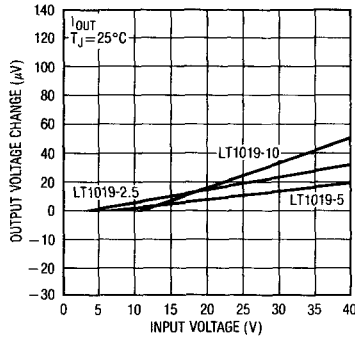
Shunt Mode Characteristics (LT1019-10)



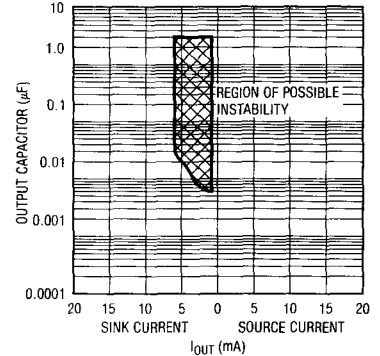
Temp Pin Voltage



Line Regulation



LT1019-2.5* Stability with Output Capacitance



*LT1019-4, 5, 10 Are Stable With All Load Capacitance.

APPLICATIONS INFORMATION

Line and Load Regulation

Line regulation on the LT1019 is nearly perfect. A 10V change in input voltage causes a typical output shift of less than 5ppm. Load regulation (sourcing current) is nearly as good. A 5mA change in load current shifts output voltage by only 100µV. These are *electrical* effects, measured with low duty cycle pulses to eliminate heating effects. In real world applications, the *thermal* effects of load and line changes must be considered.

Two separate thermal effects are evident in monolithic circuits. One is a gradient effect, where power dissipation on the die creates temperature gradients. These gradients can cause output voltage shifts *even if the overall temperature coefficient of the reference is zero*. The LT1019, unlike previous references, specifies thermal regulation caused by die temperature gradients. The specification is 0.5ppm/mW. To calculate the effect on

APPLICATIONS INFORMATION

output voltage, simply multiply the *change* in device power dissipation by the thermal regulation specification. Example: a 10V device with a nominal input voltage of 15V and load current of 5mA. Find the effect of an input voltage change of 1V and a load current change of 2mA.

$$\begin{aligned}\Delta P (\text{line change}) &= (\Delta V_{IN})(I_{LOAD}) = (1V)(5mA) = 5mW \\ \Delta V_{OUT} &= (0.5\text{ppm/mW})(5mW) = 2.5\text{ppm}\end{aligned}$$

$$\begin{aligned}\Delta P (\text{load change}) &= (\Delta I_{LOAD})(V_{IN} - V_{OUT}) \\ &= (2mA)(5V) = 10mW\end{aligned}$$

$$\Delta V_{OUT} = (0.5\text{ppm/mW})(10mW) = 5\text{ppm}$$

Even though these effects are small, they should be taken into account in critical applications, especially where input voltage or load current is high.

The second thermal effect is overall die temperature change. The magnitude of this change is the product of change in power dissipation times the thermal resistance (Θ_{JA}) of the IC package $\approx (100^{\circ}\text{C/W} - 150^{\circ}\text{C/W})$. The effect on reference output is calculated by multiplying die temperature change by the temperature drift specification of the reference. Example: same conditions as above with $\Theta_{JA} = 150^{\circ}\text{C/W}$ and an LT1019 with 20ppm/ $^{\circ}\text{C}$ drift specification.

$$\begin{aligned}\Delta P (\text{line change}) &= 5mW \\ \Delta V_{OUT} &= (5mW)(150^{\circ}\text{C/W})(20\text{ppm}/^{\circ}\text{C}) \\ &= 15\text{ppm}\end{aligned}$$

$$\begin{aligned}\Delta P (\text{load change}) &= 10mW \\ \Delta V_{OUT} &= (10mW)(150^{\circ}\text{C/W})(20\text{ppm}/^{\circ}\text{C}) \\ &= 30\text{ppm}\end{aligned}$$

These calculations show that thermally induced output voltage variations can easily exceed the electrical effects. In critical applications where shifts in power dissipation are expected, a small clip-on heat sink can significantly improve these effects by reducing overall die temperature change. Alternately, an LT1019A can be used with 4 times lower TC. If warm-up drift is of concern, these measures will also help. With warm-up drift, *total* device

power dissipation must be considered. In the example given, warm-up drift (worst-case) is equal to:

$$\text{Warm-up drift} = [(V_{IN})(I_Q) + (V_{IN} - V_{OUT})(I_{LOAD})] \\ [(\Theta_{JA})(TC)]$$

$$\begin{aligned}\text{with } I_Q (\text{quiescent current}) &= 0.6mA, \\ \text{warm-up drift} &= [(15V)(0.6mA) + (5V)(5mA)] \\ & \quad [(150^{\circ}\text{C/W})(25\text{ppm}/^{\circ}\text{C})] \\ &= 127.5\text{ppm}\end{aligned}$$

Note that 74% of the warm-up drift is due to load current times input-output differential. This emphasizes the importance of keeping both these numbers low in critical applications. With heavy loads, warm-up drift can also be improved using the technique described under "Driving Loads Above 10mA", or by heat sinking.

Note that line regulation is now affected by reference output impedance. R1 should have a wattage rating high enough to withstand full input voltage if output shorts must be tolerated. Even with load currents below 10mA, R1 can be used to reduce power dissipation in the LT1019 for lower warm-up drift, etc.

Output Trimming

Output voltage trimming on the LT1019 is nominally accomplished with a potentiometer connected from output to ground with the wiper tied to the trim pin. The LT1019 was made compatible with existing references, so the trim range is large; +6%, -6% for the LT1019-2.5, +5%, -13% for the LT1019-5, and +5%, -27% for the LT1019-10. This large trim range makes precision trimming rather difficult. One solution is to insert resistors in series with both ends of the potentiometer. This has the disadvantage of potentially poor tracking between the fixed resistors and the potentiometer. A second method of reducing trim range is to insert a resistor in series with the wiper of the potentiometer. This works well only for very small trim range because of the mismatch in TCs between the series resistor and the internal thin film resistors. These film resistors can have a TC as high as 500ppm/ $^{\circ}\text{C}$. That same TC is then transferred to the change in output voltage; a 1% shift in output voltage

APPLICATIONS INFORMATION

causes a (500ppm) (1%) = 5ppm/°C change in output voltage drift. The worst-case error in initial output voltage for the LT1019 is 0.2%, so a series resistor is satisfactory if the output is simply trimmed to nominal value. 1ppm/°C TC shift would be the maximum expected.

Using the Temp Pin

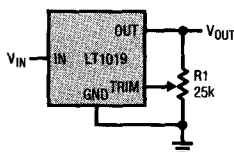
The LT1019 has a TEMP pin like several other bandgap references. The voltage on this pin is directly proportional to absolute temperature (PTAT) with a slope of $\approx 2.1\text{mV}/^\circ\text{C}$. Room temperature voltage is therefore $\approx (295^\circ\text{K})(2.1\text{mV}/^\circ\text{C}) = 620\text{mV}$. Previous bandgap references have been very sensitive to any loading on the TEMP pin because it is an integral part of the reference "core" itself. The LT1019 "taps" the core at a special point which has much less effect on the reference. The relationship between TEMP pin loading and a change in reference output voltage is less than $0.05\%/\mu\text{A}$, about 10 times improvement over previous references.

The TEMP pin can be used to sense chip temperature in applications where the chip is forced to constant temperature (see "Heated Mode") or to sense ambient temper-

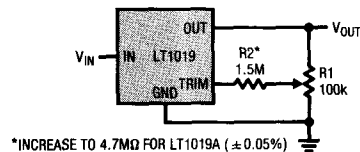
ature in applications where the temperature difference between chip and ambient is tolerable or can be calibrated out. Typical chip temperature rise over ambient is $\approx 2^\circ\text{C}$ with no output load and 15V input voltage, but it could be as high as 6°C with a 5mA load and 5V input-output differential. A Centigrade thermometer is shown in the application circuits. This particular configuration has the advantage of trimming "zero" and "slope" simultaneously. The PTAT nature of the TEMP pin output has a known predictable relationship between initial zero error and slope. This circuit takes advantage of that relationship by trimming at a point that corrects the zero and slope errors simultaneously.

A simple over-temp circuit is also shown in the application section using an LT1011 comparator. This circuit is intended to be an *ambient* sensor, so temperature rise in the reference must be considered when setting trip level. R2B is adjusted by connecting a DVM across the inputs of the comparator and setting the DVM to read 2.1mV for each degree above room temperature. A 70°C trip would require $(2.1\text{mV})(70^\circ\text{C} - 22^\circ\text{C}) = 101\text{mV}$. R3 provides about 1°C hysteresis to prevent oscillations.

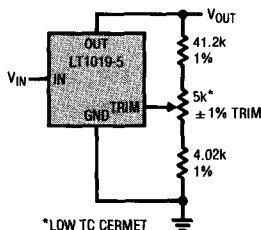
Wide Range Trim $\geq \pm 5\%$



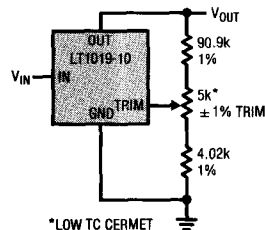
Narrow Trim Range ($\pm 0.2\%$)



Trimming LT1019-5 Output to 5.120V

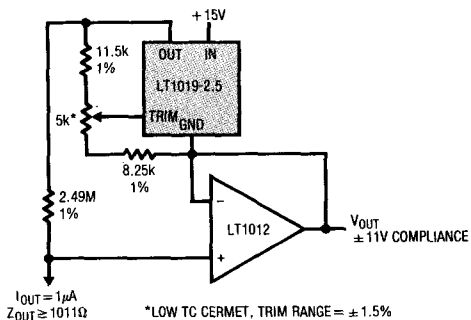


Trimming LT1019-10 Output to 10.240V

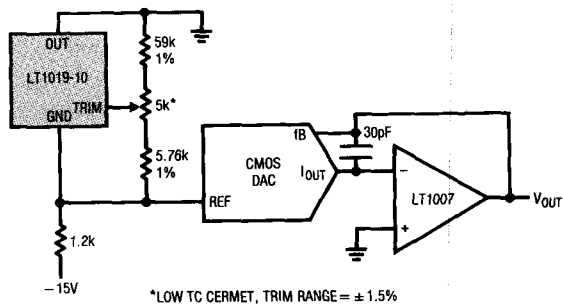


APPLICATIONS INFORMATION

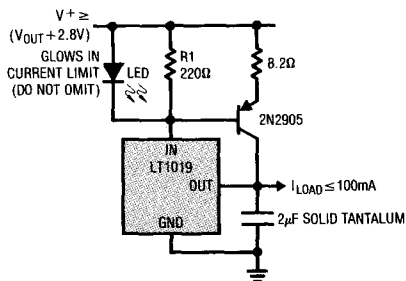
Precision 1μA Current Source



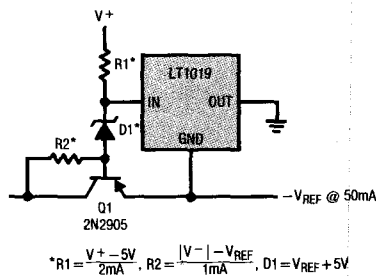
Negative 10V Reference for CMOS DAC



Output Current Boost with Current Limit

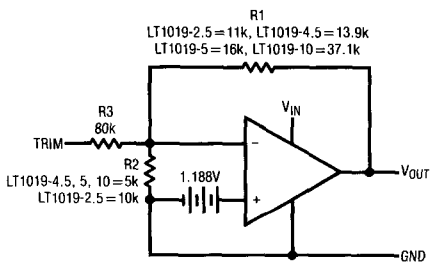


Negative Series Reference

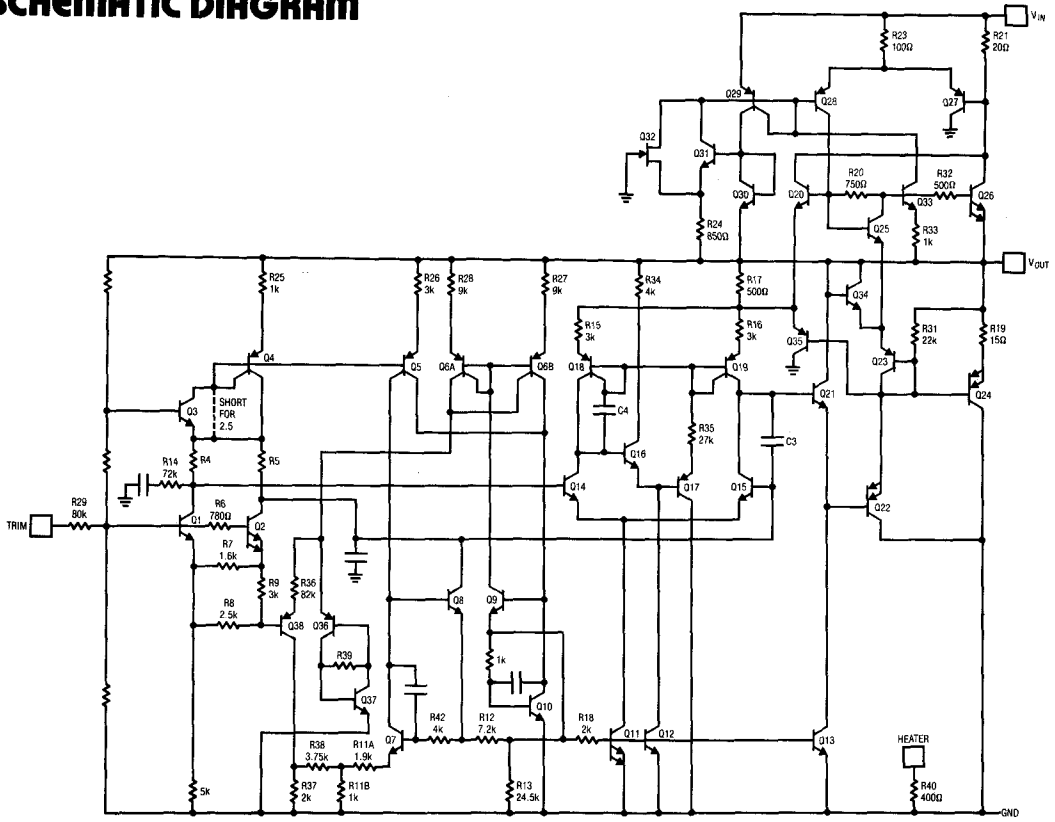


3

BLOCK DIAGRAM

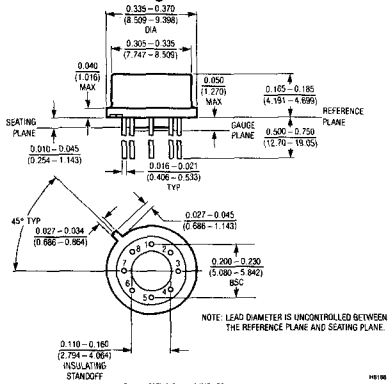


SCHEMATIC DIAGRAM



PACKAGE DESCRIPTION

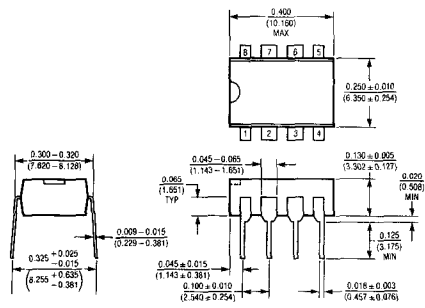
H Package Metal Can



NOTE: DIMENSIONS IN INCHES

T _{max}	θ _{jc}	θ _{ja}
150°C	150°C/W	45°C/W

N8 Package 8 Lead Plastic



T _{max}	θ _{jc}
100°C	130°C/W

FEATURES

- Pin Compatible with Most Bandgap Reference Applications, Including Ref 01, Ref 02, LM368, MC1400, and MC1404, with Greatly Improved Stability, Noise, and Drift
- Ultra Low Drift—2ppm/°C Max Slope
- Trimmed Output Voltage
- Operates in Series or Shunt Mode
- Output Sinks and Sources in Series Mode
- Very Low Noise < 1ppm p-p (0.1Hz to 10Hz)
- >100dB Ripple Rejection
- Minimum Input-Output Differential of 1V
- 100% Noise Tested

APPLICATIONS

- A to D and D to A Converters
- Precision Regulators
- Digital Voltmeters
- Inertial Navigation Systems
- Precision Scales
- Portable Reference Standard

DESCRIPTION

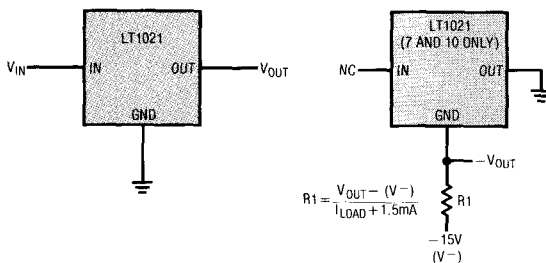
The LT1021 is a precision reference with ultra low drift and noise, extremely good long term stability, and almost total immunity to input voltage variations. The reference output will both source and sink up to 10mA. Three voltages are available; 5V, 7V and 10V. The 7V and 10V units can be used as shunt regulators (two terminal zeners) with the same precision characteristics as the three terminal connection. Special care has been taken to minimize thermal regulation effects and temperature induced hysteresis.

The LT1021 references are based on a buried zener diode structure which eliminates noise and stability problems associated with surface breakdown devices. Further, a subsurface zener exhibits better temperature drift and time stability than even the best band-gap references.

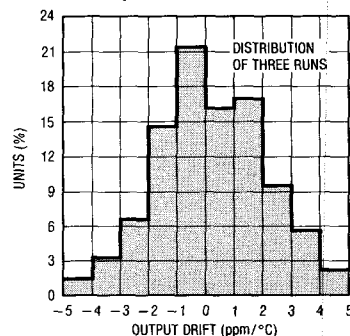
Unique circuit design makes the LT1021 the first IC reference to offer ultra low drift without the use of high power on-chip heaters.

The LT1021-7 uses no resistive divider to set output voltage, and therefore exhibits the best long term stability and temperature hysteresis. The LT1021-5 and LT1021-10 are intended for systems requiring a precise 5V or 10V reference, with an initial tolerance as low as $\pm 0.05\%$.

Basic Positive and Negative Connections



Typical Distribution of Temperature Drift—LT1021



LT1021

ABSOLUTE MAXIMUM RATINGS

Input Voltage	40V
Input-Output Voltage Differential	35V
Output to Ground Voltage (Shunt Mode Current Limit)	
LT1021-5	10V
LT1021-7	10V
LT1021-10	16V
Trim Pin to Ground Voltage	
Positive	Equal to V_{OUT}
Negative	-20V
Output Short Circuit Duration	
$V_{IN} = 35V$	10 sec
$V_{IN} \leq 20V$	Indefinite
Operating Temperature Range	
LT1021 Mil	-55°C to 125°C
LT1021 Comm	0°C to 70°C
Storage Temperature Range	
All Devices	-65°C to 150°C
Lead Temperature (Soldering, 10 sec.)	300°C

PACKAGE/ORDER INFORMATION

		ORDER PART NUMBER	
<p>TOP VIEW</p> <p>METAL CAN H PACKAGE</p> <p>*CONNECTED INTERNALLY. DO NOT CONNECT EXTERNAL CIRCUITRY TO THESE PINS.</p> <p>**NO TRIM PIN ON LT1021-7. DO NOT CONNECT EXTERNAL CIRCUITRY TO PIN 5 ON LT1021-7.</p>	LT1021BMH-5	LT1021AMH-10	
	LT1021CMH-5	LT1021BMH-10	
	LT1021DMH-5	LT1021CMH-10	
	LT1021BCH-5	LT1021DMH-10	
	LT1021CCH-5	LT1021ACH-10	
	LT1021DCH-5	LT1021BCH-10	
		LT1021CCH-10	
		LT1021DCH-10	
		LT1021AMH-7	
		LT1021BMH-7	
	LT1021DMH-7		
	LT1021ACH-7		
	LT1021BCH-7		
	LT1021DCH-7		
<p>TOP VIEW</p> <p>PLASTIC DIP N8 PACKAGE</p> <p>*CONNECTED INTERNALLY. DO NOT CONNECT EXTERNAL CIRCUITRY TO THESE PINS.</p> <p>**NO TRIM PIN ON LT1021-7. DO NOT CONNECT EXTERNAL CIRCUITRY TO PIN 5 ON LT1021-7.</p>	LT1021BCN8-5	LT1021BCN8-7	
	LT1021CCN8-5	LT1021DCN8-5	
		LT1021BCN8-7	
		LT1021DCN8-7	
		LT1021BCN8-10	
		LT1021CCN8-10	
		LT1021DCN8-10	

ELECTRICAL CHARACTERISTICS LT1021-5

$V_{IN} = 10V$, $I_{OUT} = 0$, $T_A = 25^\circ C$, Mil or Comm version, unless otherwise noted

PARAMETER	CONDITIONS	LT1021-5			UNITS
		MIN	TYP	MAX	
Output Voltage (Note 1)	LT1021C-5 LT1021B-5, D-5	4.9975 4.95	5.000 5.00	5.0025 5.05	V V
Output Voltage Temperature Coefficient (Note 2)	$T_{MIN} \leq T_J \leq T_{MAX}$ LT1021B-5 LT1021C-5, D-5		2 3	5 20	ppm/°C ppm/°C
Line Regulation (Note 3)	$7.2V \leq V_{IN} \leq 10V$ $10V \leq V_{IN} \leq 40V$	● ●	4	12	ppm/V
				20	ppm/V
			2	6	ppm/V
		●		10	ppm/V
Load Regulation (Sourcing Current)	$0 \leq I_{OUT} \leq 10mA$ (Note 3)	● ●	10	20	ppm/mA
				35	ppm/mA
Load Regulation (Sinking Current)	$0 \leq I_{OUT} \leq 10mA$ (Note 3)	● ●	60	100	ppm/mA
				150	ppm/mA
Supply Current		● ●	0.8	1.2	mA
				1.5	mA
Output Voltage Noise (Note 5)	$0.1Hz \leq f \leq 10Hz$ $10Hz \leq f \leq 1kHz$		3		μV_p-p
			2.2	3.5	μV_{RMS}
Long Term Stability of Output Voltage (Note 6)	$\Delta t = 1000$ Hrs Non-Cumulative		15		ppm
Temperature Hysteresis of Output	$\Delta T = \pm 25^\circ C$		10		ppm

ELECTRICAL CHARACTERISTICS LT1021-7

$V_{IN} = 12V$, $I_{OUT} = 0$, $T_A = 25^\circ C$, Mil or Comm version, unless otherwise noted

PARAMETER	CONDITIONS	LT1021-7			UNITS
		MIN	TYP	MAX	
Output Voltage (Note 1)		6.95	7.00	7.05	V
Output Voltage Temperature Coefficient (Note 2)	$T_{MIN} \leq T_J \leq T_{MAX}$ LT1021A-7 LT1021B-7 LT1021D-7		1 2 3	2 5 20	ppm/°C ppm/°C ppm/°C
Line Regulation (Note 3)	$8.5V \leq V_{IN} \leq 12V$		1 2	4 8	ppm/V ppm/V
	$12V \leq V_{IN} \leq 40V$	• •	0.5 1	2 4	ppm/V ppm/V
Load Regulation (Sourcing Current)	$0 \leq I_{OUT} \leq 10mA$ (Note 3)	•	12	25 40	ppm/mA ppm/mA
Load Regulation (Shunt Mode)	$1.2mA \leq I_{SHUNT} \leq 10mA$ (Notes 3, 4)	•	50	100 150	ppm/mA ppm/mA
Supply Current (Series Mode)		•	0.75	1.2 1.5	mA mA
Minimum Current (Shunt Mode)	V_{IN} is Open	•	0.7	1.0 1.2	mA mA
Output Voltage Noise (Note 5)	$0.1Hz \leq f \leq 10Hz$		4		$\mu Vp-p$
	$10Hz \leq f \leq 1kHz$		2.5	4	$\mu Vrms$
Long Term Stability of Output Voltage (Note 6)	$\Delta t = 1000$ Hrs Non-Cumulative		7		ppm
Temperature Hysteresis of Output	$\Delta T = \pm 25^\circ C$		3		ppm

3

ELECTRICAL CHARACTERISTICS LT1021-10

$V_{IN} = 15V$, $I_{OUT} = 0$, $T_A = 25^\circ C$, Mil or Comm version, unless otherwise noted

PARAMETER	CONDITIONS	LT1021-10			UNITS
		MIN	TYP	MAX	
Output Voltage (Note 1)	LT1021C-10 LT1021A-10, B-10, D-10	9.995 9.95	10.00	10.005 10.05	V V
Output Voltage Temperature Coefficient (Note 2)	$T_{MIN} \leq T_J \leq T_{MAX}$ LT1021A-10 LT1021B-10 LT1021C-10, D-10		1 2 5	2 5 20	ppm/°C ppm/°C ppm/°C
Line Regulation (Note 3)	$11.5V \leq V_{IN} \leq 14.5V$		1	4 6	ppm/V ppm/V
	$14.5V \leq V_{IN} \leq 40V$	• •	0.5	2 4	ppm/V ppm/V
Load Regulation (Sourcing Current)	$0 \leq I_{OUT} \leq 10mA$ (Note 3)	•	12	25 40	ppm/mA ppm/mA
Load Regulation (Shunt Mode)	$1.7mA \leq I_{SHUNT} \leq 10mA$ (Notes 3, 4)	•	50	100 150	ppm/mA ppm/mA
Series Mode Supply Current		•	1.2	1.7 2.0	mA mA
Shunt Mode Minimum Current	V_{IN} is Open	•	1.1	1.5 1.7	mA mA
Output Voltage Noise (Note 5)	$0.1Hz \leq f \leq 10Hz$		6		$\mu Vp-p$
	$0.1Hz \leq f \leq 1kHz$		3.5	6	$\mu Vrms$
Long Term Stability of Output Voltage (Note 6)	$\Delta t = 1000$ Hrs Non-Cumulative		15		ppm
Temperature Hysteresis of Output	$\Delta T = \pm 25^\circ C$		5		ppm

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: Output voltage is measured immediately after turn-on. Changes due to chip warm-up are typically less than 0.005%.

Note 2: Temperature coefficient is measured by dividing the change in output voltage over the temperature range by the change in temperature. Separate tests are done for hot and cold; T_{MIN} to 25°C, and 25°C to T_{MAX} . **Incremental slope is also measured at 25°C.** For the "A" version only, a box method is used from 0°C to 70°C with a height of $2\text{ppm}/^{\circ}\text{C} \times 70^{\circ}\text{C} = 140\text{ppm}$. Military "A" grades receive an additional -55°C to $+125^{\circ}\text{C}$ test to $\pm 5\text{ppm}/^{\circ}\text{C}$.

Note 3: Line and load regulation are measured on a pulse basis. Output changes due to die temperature change must be taken into account separately. Package thermal resistance is $150^{\circ}\text{C}/\text{W}$ for TO-5 (H), and $130^{\circ}\text{C}/\text{W}$ for N.

Note 4: Shunt mode regulation is measured with the input open. With the input connected, shunt mode current can be reduced to 0mA. Load regulation will remain the same.

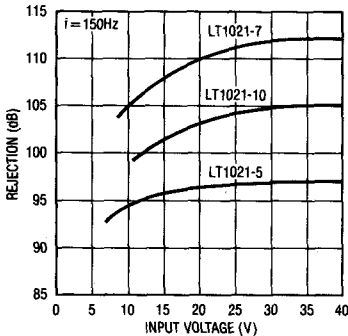
Note 5: RMS noise is measured with a single high pass filter at 10Hz and a 2-pole low pass filter at 1kHz. The resulting output is full wave rectified and then integrated for a fixed period, making the final reading an average as opposed to RMS. A correction factor of 1.1 is used to convert from average to RMS, and a second correction of 0.88 is used to correct for the non-ideal bandpass of the filters.

Peak-to-peak noise is measured with a single high pass filter at 0.1Hz and a 2-pole low pass filter at 10Hz. The unit is enclosed in a still-air environment to eliminate thermocouple effects on the leads. Test time is 10 seconds.

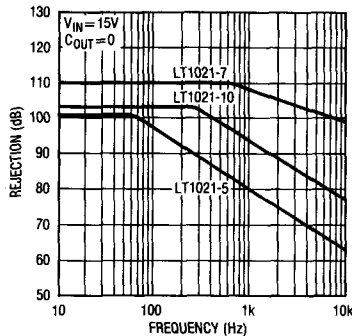
Note 6: Consult factory for units with long term stability data.

TYPICAL PERFORMANCE CHARACTERISTICS

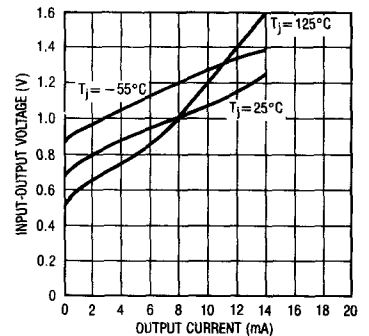
Ripple Rejection



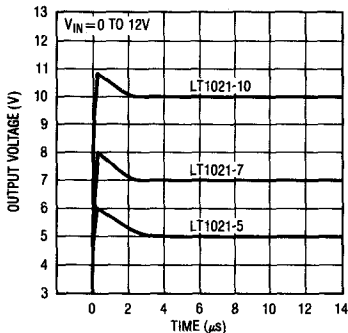
Ripple Rejection



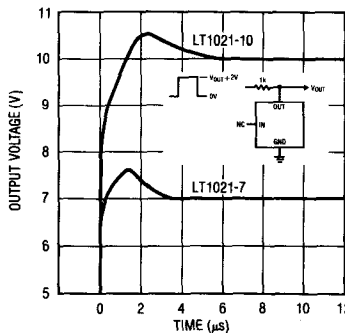
Minimum Input-Output Differential LT1021-7 and LT1021-10



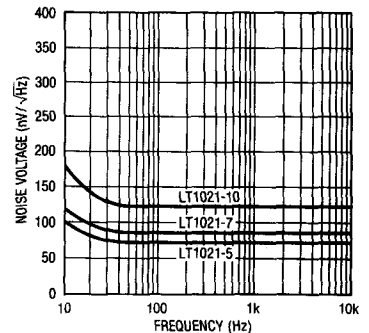
Start-Up (Series Mode)



Start-Up (Shunt Mode) LT1021-7 and LT1021-10

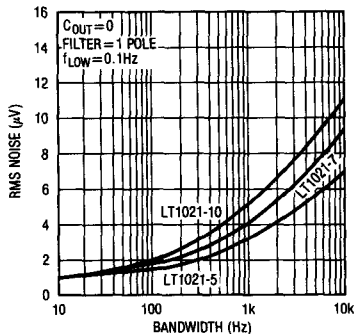


Output Voltage Noise Spectrum

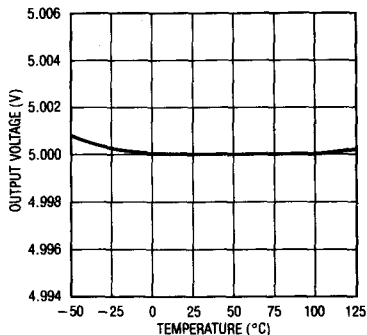


TYPICAL PERFORMANCE CHARACTERISTICS

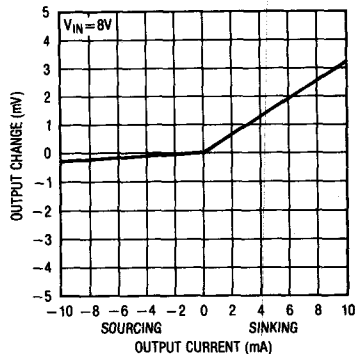
Output Voltage Noise



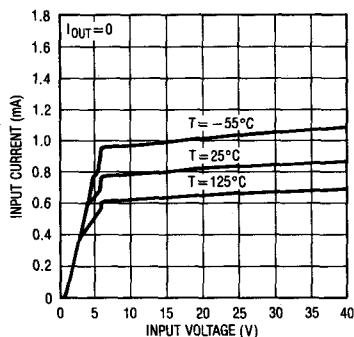
Output Voltage Temperature Drift LT1021-5



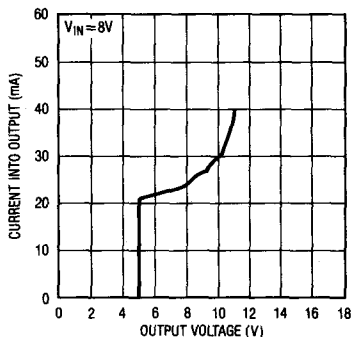
Load Regulation LT1021-5



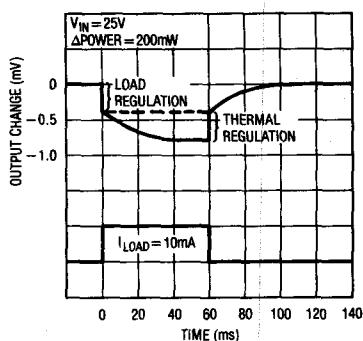
Quiescent Current LT1021-5



Sink Mode* Current Limit LT1021-5

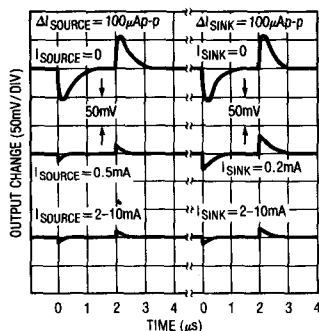


Thermal Regulation LT1021-5

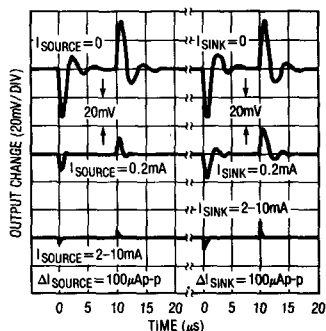


*NOTE THAT AN INPUT VOLTAGE IS REQUIRED FOR 5V UNITS.

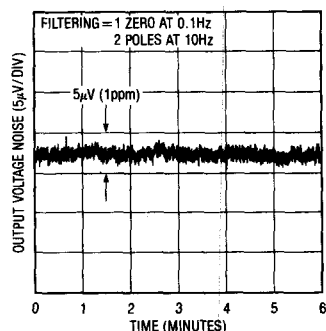
Load Transient Response LT1021-5, C_{LOAD} = 0



Load Transient Response LT1021-5, C_{LOAD} = 1000pF



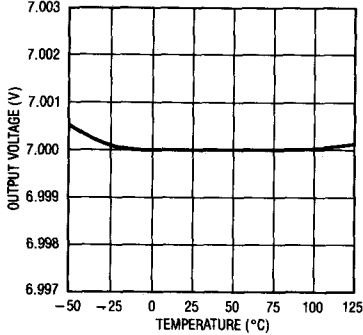
Output Noise 0.1Hz to 10Hz LT1021-5



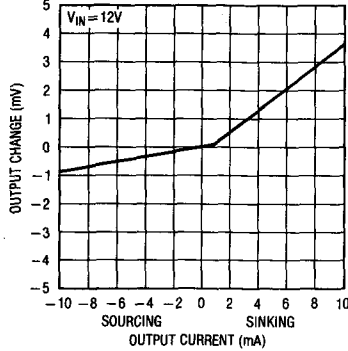
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TYPICAL PERFORMANCE CHARACTERISTICS

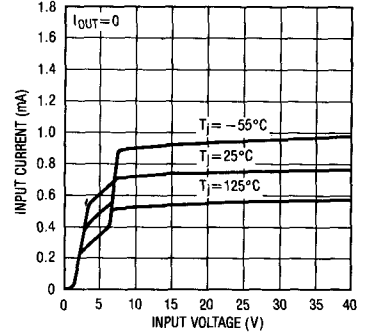
Output Voltage Temperature Drift LT1021-7



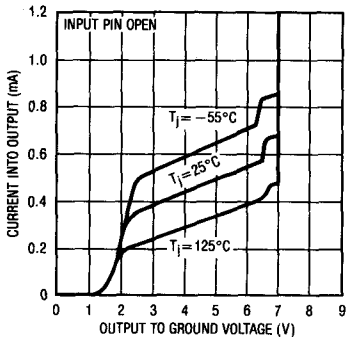
Load Regulation LT1021-7, 10



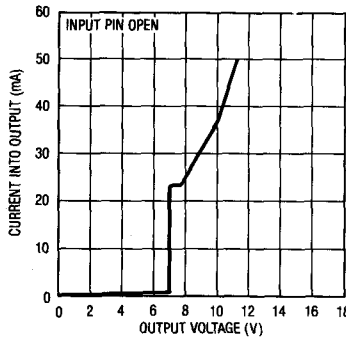
Quiescent Current LT1021-7



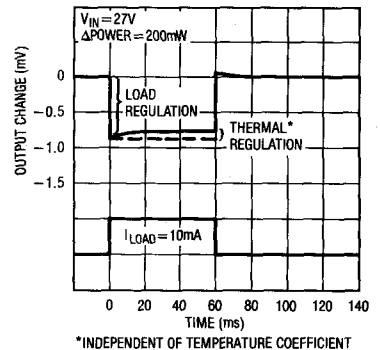
Shunt Characteristics LT1021-7



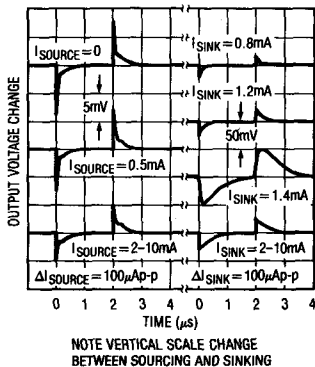
Shunt Mode Current Limit LT1021-7



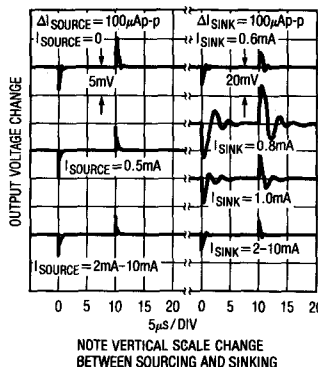
Thermal Regulation LT1021-7



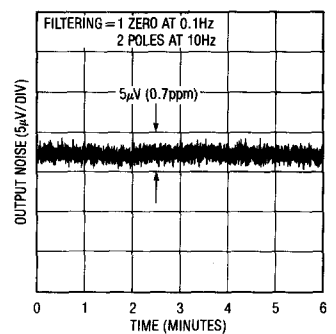
Load Transient Response LT1021-7, CLOAD = 0



Load Transient Response LT1021-7, CLOAD = 1000pF

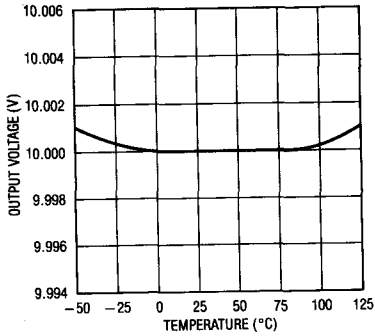


Output Noise 0.1Hz to 10Hz LT1021-7

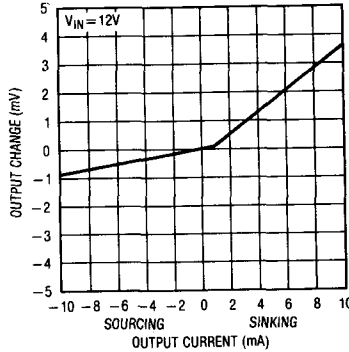


TYPICAL PERFORMANCE CHARACTERISTICS

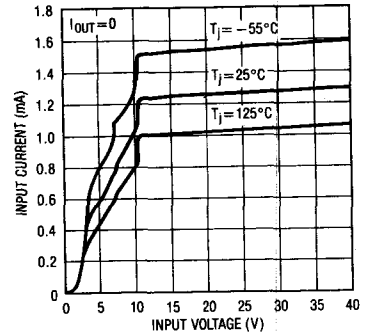
Output Voltage Temperature Drift LT1021-10



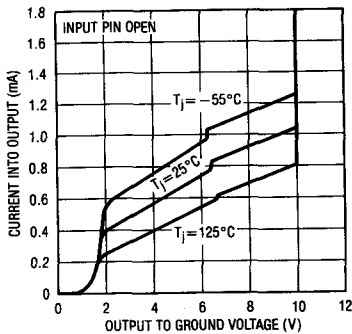
Load Regulation LT1021-7, 10



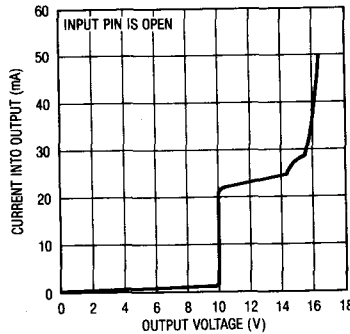
Input Supply Current LT1021-10



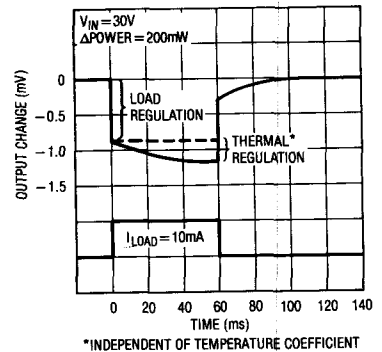
Shunt Characteristics LT1021-10



Shunt Mode Current Limit LT1021-10

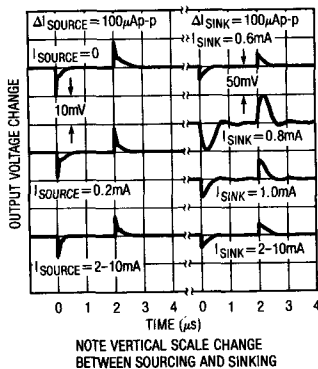


Thermal Regulation LT1021-10

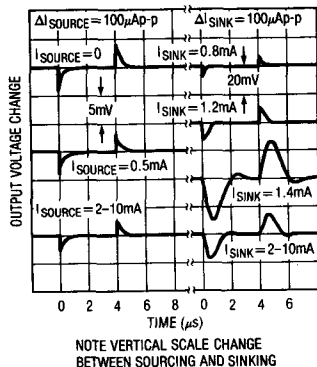


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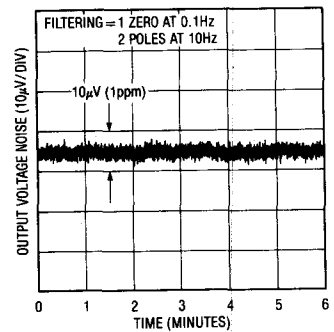
Load Transient Response LT1021-10, CLOAD = 0



Load Transient Response LT1021-10, CLOAD = 1000pF



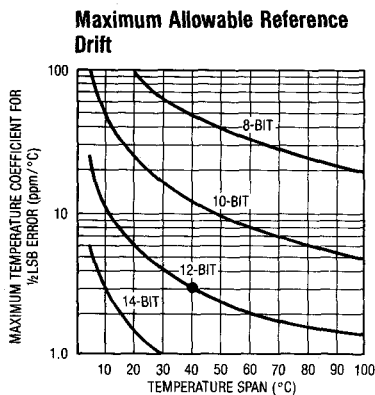
Output Noise 0.1Hz to 10Hz LT1021-10



APPLICATIONS INFORMATION

Effect of Reference Drift on System Accuracy

A large portion of the temperature drift error budget in many systems is the system reference voltage. This graph indicates the maximum temperature coefficient allowable if the reference is to contribute no more than $\frac{1}{2}$ LSB error to the overall system performance. The example shown is a 12-bit system designed to operate over a temperature range from 25°C to 65°C. Assuming the system calibration is performed at 25°C, the temperature span is 40°C. It can be seen from the graph that the temperature coefficient of the reference must be no worse than 3ppm/°C if it is to contribute less than $\frac{1}{2}$ LSB error. For this reason, the LT1021 family has been optimized for low drift.



Trimming Output Voltage

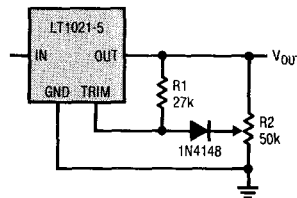
LT1021-10

The LT1021-10 has a trim pin for adjusting output voltage. The impedance of the trim pin is about 12kΩ with a nominal open circuit voltage of 5V. It is designed to be driven from a source impedance of 3kΩ or less to minimize changes in the LT1021 TC with output trimming. Attenuation between the trim pin and the output is 70:1. This allows ± 70 mV trim range when the trim pin is tied to the wiper of a potentiometer connected between the output and ground. A 10kΩ potentiometer is recommended, preferably a 20 turn cermet type with stable characteristics over time and temperature.

The LT1021-10 "C" version is pre-trimmed to ± 5 mV and therefore can utilize a restricted trim range. A 75kΩ resistor in series with a 20kΩ potentiometer will give ± 10 mV trim range. Effect on output TC will be only 1ppm/°C for the ± 5 mV trim needed to set the "C" device to 10.000V.

LT1021-5

The LT1021-5 does have an output voltage trim pin, but the TC of the nominal 4V open circuit voltage at this pin is about -1.7 mV/°C. For the voltage trimming not to affect reference output TC, the external trim voltage must track the voltage on the trim pin. Input impedance of the trim pin is about 100kΩ and attenuation to the output is 13:1. The technique shown below is suggested for trimming the output of the LT1021-5 while maintaining minimum shift in output temperature coefficient. The R1/R2 ratio is chosen to minimize interaction of trimming and TC shifts, so the exact values shown should be used.

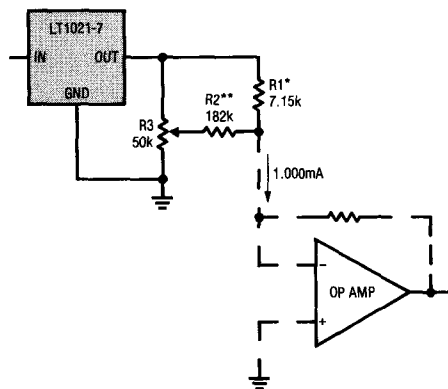
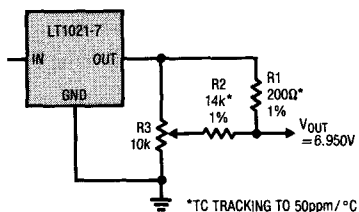


LT1021-7

The 7V version of the LT1021 has no trim pin because the internal architecture does not have a point which could be driven conveniently from the output. Trimming must therefore be done externally, as is the case with ordinary reference diodes. Unlike these diodes, however, the output of the LT1021 can be loaded with a trim potentiometer. The following trim techniques are suggested; one for voltage output, and one for current output. The voltage output is trimmed for 6.95V. Current output is 1mA, as shown, into a summing junction, but all resistors may be scaled for currents up to 10mA.

APPLICATIONS INFORMATION

Both of these circuits use the trimmers in a true potentiometric mode to reduce the effects of trimmer TC. The voltage output has a 200Ω impedance, so loading must be minimized. In the current output circuit, R1 determines output current. It should have a TC commensurate with the LT1021 or track closely with the feedback resistor around the op amp.



*RESISTOR TC DETERMINES I_{OUT} TC
 **TC $\leq 10 \times R1$ TC. R2 AND R3 SCALE WITH R1 FOR DIFFERENT OUTPUT CURRENTS.

Capacitive Loading and Transient Response

The LT1021 is stable with all capacitive loads, but for optimum settling with load transients, output capacitance should be under 1000pF. The output stage of the reference is class AB with a fairly low idling current. This makes transient response worst-case at light load currents. Because of

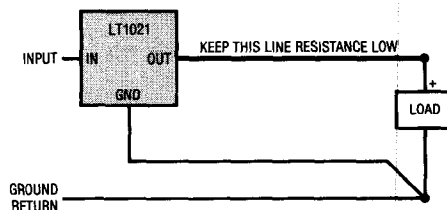
internal current drain on the output, actual worst-case occurs at $I_{LOAD} = 0$ on LT1021-5, $I_{LOAD} = -0.8\text{mA}$ (sinking) on LT1021-7, and $I_{LOAD} = 1.4\text{mA}$ (sinking) on LT1021-10. Significantly better load transient response is obtained by moving slightly away from these points. See Load Transient Response curves for details. In general, best transient response is obtained when the output is sourcing current. In critical applications, a 10μF solid tantalum capacitor with several ohms in series provides optimum output bypass.

Kelvin Connections

Although the LT1021 does not have true force/sense capability at its outputs, significant improvements in ground loop and line loss problems can be achieved with proper hook-up. In series mode operation, the ground pin of the LT1021 carries only $\approx 1\text{mA}$ and can be used as a sense line, greatly reducing ground loop and loss problems on the low side of the reference. The high side supplies load current so line resistance must be kept low. Twelve feet of #22 gauge hook up wire or 1 foot of 0.025 inch printed circuit trace will create 2mV loss at 10mA output current. This is equivalent to 1LSB in a 10V, 12-bit system.

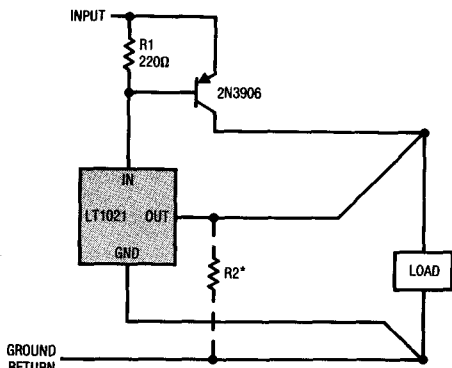
The circuits below show proper hook up to minimize errors due to ground loops and line losses. Losses in the output lead can be greatly reduced by adding a PNP boost transistor if load currents are 5mA or higher. R2 can be added to further reduce current in the output sense lead.

Standard Series Mode



APPLICATIONS INFORMATION

Series Mode with Boost Transistor



*OPTIONAL—REDUCES CURRENT IN OUTPUT SENSE LEAD
 R2 = 2.4k (LT1021-5), 3k (LT1021-7), 5.6k (LT1021-10)

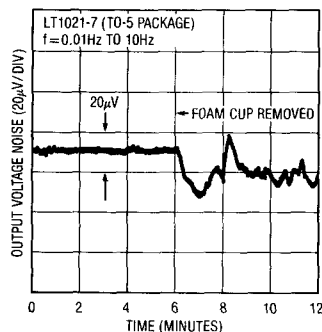
shielded from ambient air with a small foam cup. The cup was then removed for the second half of the trace. Ambient in both cases was a lab environment with no excessive air turbulence from air conditioners, opening/closing doors, etc. Removing the foam cup increases the output noise by almost an order of magnitude in the 0.01Hz to 1Hz band! The kovar leads of the TO-5 (H) package are the primary culprit. Alloy 42 and copper lead frames used on dual-in-line packages are not nearly as sensitive to thermally generated noise because they are intrinsically matched.

There is nothing magical about foam cups—any enclosure which blocks air flow from the reference will do. Smaller enclosures are better since they do not allow the build-up of internally generated air movement. Naturally, heat generating components external to the reference itself should not be included inside the enclosure.

Effects of Air Movement on Low Frequency Noise

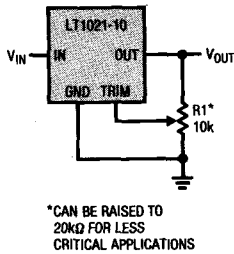
The LT1021 has very low noise because of the buried zener used in its design. In the 0.1Hz to 10Hz band, peak-to-peak noise is about 0.5ppm of the DC output. To achieve this low noise, however, care must be taken to shield the reference from ambient air turbulence. Air movement can create noise because of thermoelectric differences between IC package leads (especially kovar lead TO-5) and printed circuit board materials and/or sockets. Power dissipation in the reference, even though it rarely exceeds 20mW, is enough to cause small temperature gradients in the package leads. Variations in thermal resistance, caused by uneven air flow, create differential lead temperatures, thereby causing thermoelectric voltage noise at the output of the reference. The XY plotter trace shown below dramatically illustrates this effect. The first half of the plot was done with the LT1021

Noise Induced by Air Turbulence (TO-5 Package)

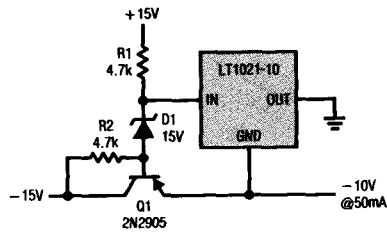


APPLICATION CIRCUITS

LT1021-10 Full Trim Range ($\pm 0.7\%$)

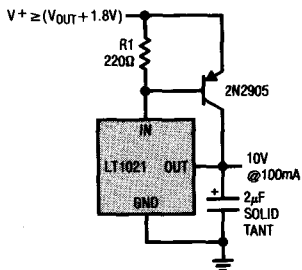


Negative Series Reference

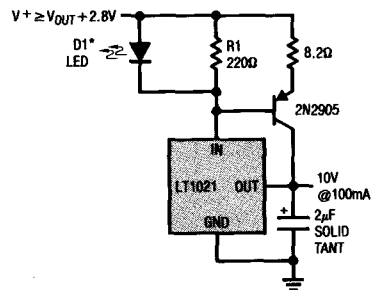


3

Boosted Output Current With No Current Limit

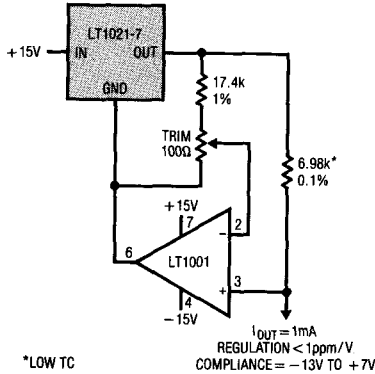


Boosted Output Current With Current Limit



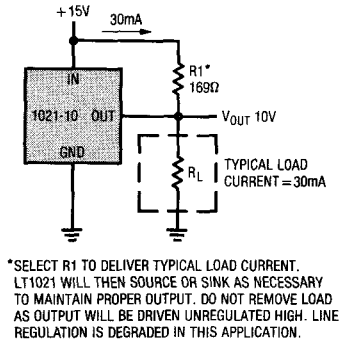
APPLICATION CIRCUITS

Ultra Precise Current Source

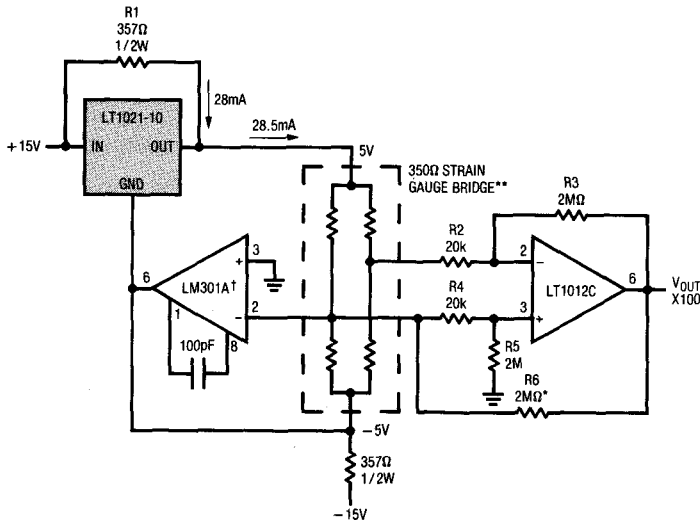


*LOW TC

Handling Higher Load Currents



Strain Gauge Conditioner for 350Ω Bridge



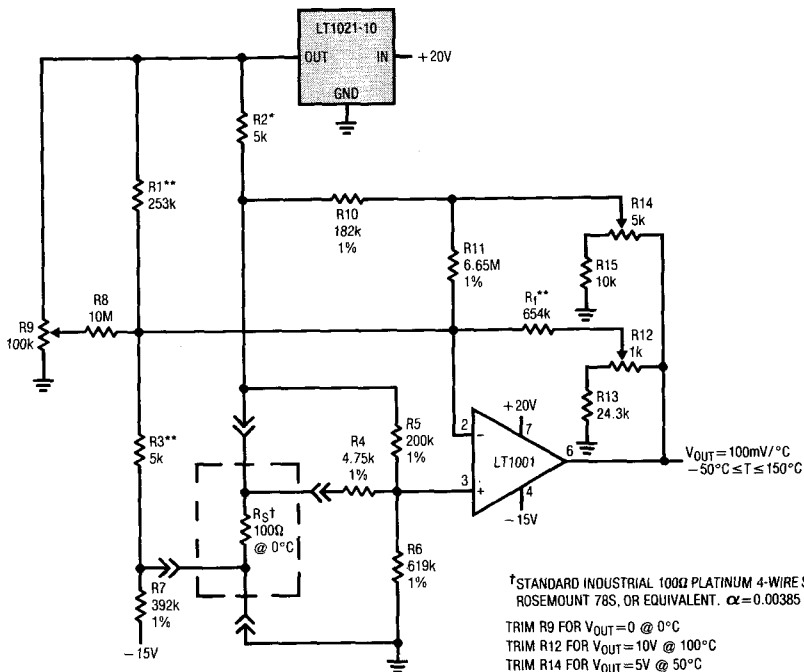
*THIS RESISTOR PROVIDES POSITIVE FEEDBACK TO THE BRIDGE TO ELIMINATE LOADING EFFECT OF THE AMPLIFIER. EFFECTIVE Z_{IN} OF AMPLIFIER STAGE IS $\approx 1\text{M}\Omega$. IF R2-R5 ARE CHANGED, SET R6 = R3.

**BRIDGE IS ULTRA LINEAR WHEN ALL LEGS ARE ACTIVE, TWO IN COMPRESSION AND TWO IN TENSION, OR WHEN ONE SIDE IS ACTIVE WITH ONE COMPRESSED AND ONE TENSIONED LEG.

†OFFSET AND DRIFT OF LM301A ARE VIRTUALLY ELIMINATED BY DIFFERENTIAL CONNECTION OF LT1012C.

APPLICATION CIRCUITS

Ultra Linear Platinum Temperature Sensor*



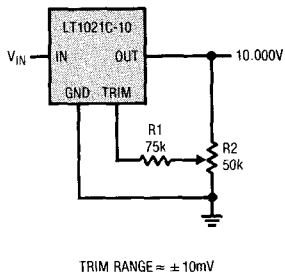
*STANDARD INDUSTRIAL 100Ω PLATINUM 4-WIRE SENSOR, ROSEMOUNT 78S, OR EQUIVALENT. $\alpha = 0.00385$

TRIM R9 FOR $V_{OUT} = 0$ @ 0°C
 TRIM R12 FOR $V_{OUT} = 10V$ @ 100°C
 TRIM R14 FOR $V_{OUT} = 5V$ @ 50°C
 USE TRIM SEQUENCE AS SHOWN. TRIMS ARE NON-INTERACTIVE SO THAT ONLY ONE TRIM SEQUENCE IS NORMALLY REQUIRED.

*FEEDBACK LINEARIZES OUTPUT TO $\pm 0.005^\circ C$ FROM $-50^\circ C$ TO $+150^\circ C$

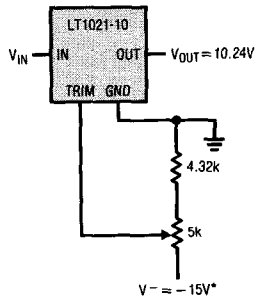
**WIREWOUND RESISTORS WITH LOW TC

Restricted Trim Range for Improved Resolution, 10V, 'C' Version Only



TRIM RANGE = $\pm 10mV$

Trimming 10V Units to 10.24V

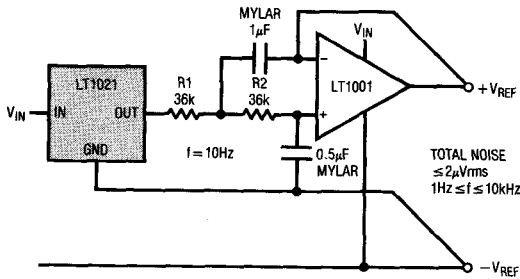


*MUST BE WELL REGULATED
 $\frac{dV_{OUT}}{dV} = \frac{15mV}{V}$

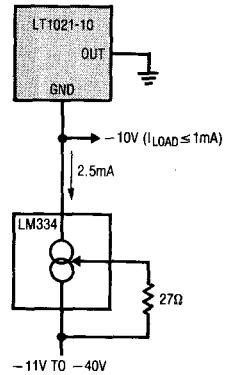
3

APPLICATION CIRCUITS

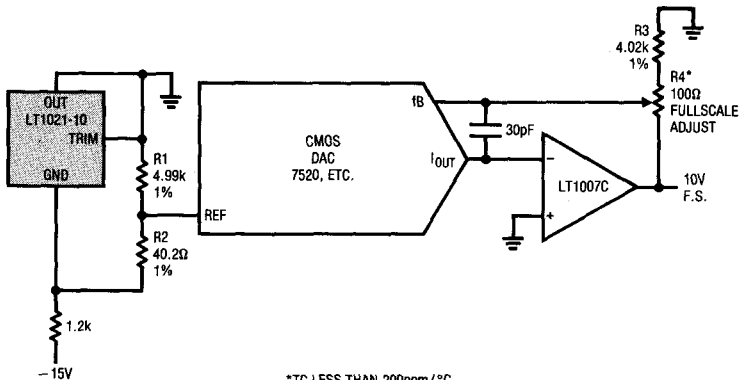
2-Pole Low Pass Filtered Reference



Negative Shunt Reference Driven by Current Source



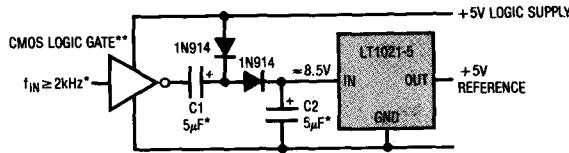
CMOS DAC with Low-Drift Full Scale Trimming**



*TC LESS THAN 200ppm/°C
 **NO ZERO ADJUST REQUIRED
 WITH LT1007 ($V_{OS} \leq 60\mu V$)

APPLICATION CIRCUITS

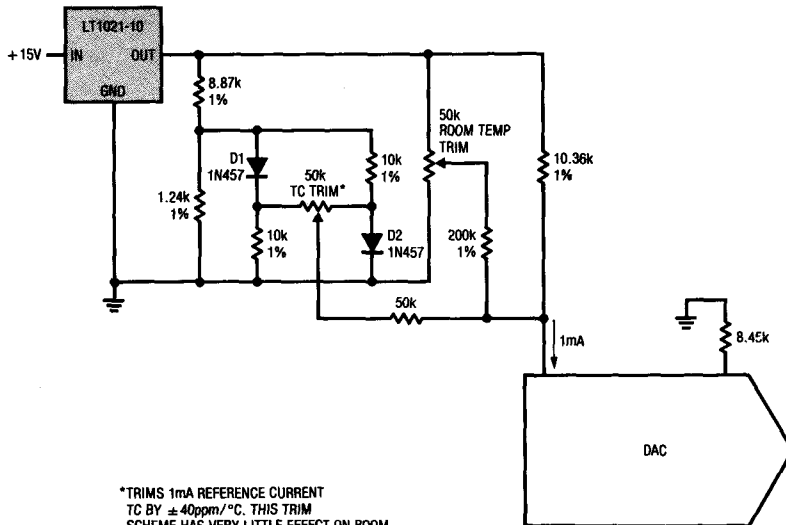
Operating 5V Reference from 5V Supply



*FOR HIGHER FREQUENCIES C1 AND C2 MAY BE DECREASED.
 **PARALLEL GATES FOR HIGHER REFERENCE CURRENT LOADING.

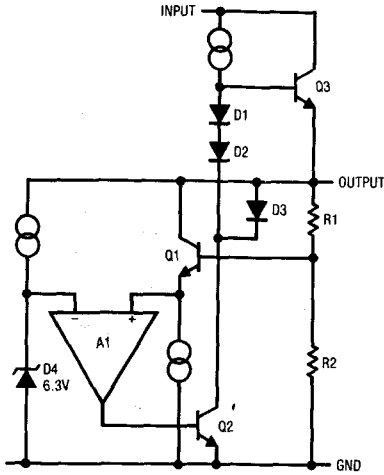
3

Precision DAC Reference with System TC Trim



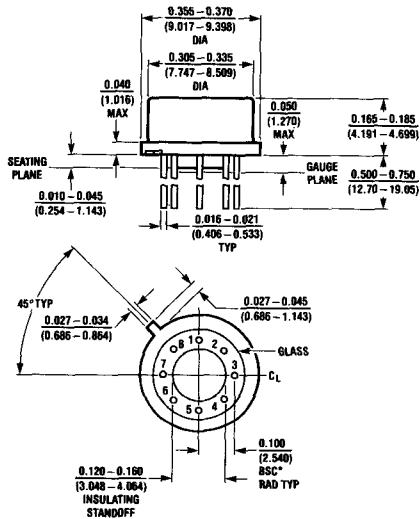
*TRIMS 1mA REFERENCE CURRENT
 TC BY ± 40ppm/°C. THIS TRIM
 SCHEME HAS VERY LITTLE EFFECT ON ROOM
 TEMPERATURE CURRENT TO MINIMIZE ITERATIVE
 TRIMMING.

EQUIVALENT SCHEMATIC



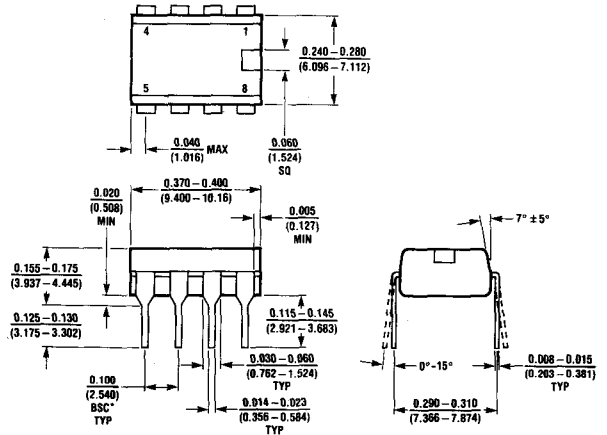
PACKAGE DESCRIPTION

**H Package
Metal Can**



T_{max} 150°C	θ_{ja} 150°C/W	θ_{jc} 45°C/W
--------------------	--------------------------	-------------------------

**N8 Package
8 Lead Plastic**



NOTE: DIMENSIONS IN INCHES UNLESS OTHERWISE NOTED
*LEADS WITHIN 0.007 OF TRUE POSITION (TP) AT GAUGE PLANE

T_{max} 100°C	θ_{ja} 130°C/W
--------------------	--------------------------

FEATURES

- Low Drift—20ppm/°C Max Slope*
- Trimmed Output Voltage*
- Operates in Series or Shunt Mode
- Output Sinks and Sources in Series Mode
- Very Low Noise <1ppm p-p (0.1Hz to 10Hz)
- >100dB Ripple Rejection
- Minimum Input-Output Differential of 1V
- 100% Noise Tested

APPLICATIONS

- A to D and D to A Converters
- Precision Regulators
- Digital Voltmeters
- Inertial Navigation Systems
- Precision Scales
- Portable Reference Standard

*Units specified at 10ppm/°C maximum drift and 0.1% output voltage tolerance are available on request.

DESCRIPTION

The LT1021 is a precision reference with ultra low drift and noise, extremely good long term stability, and almost total immunity to input voltage variations. The reference output will both source and sink up to 10mA. Three voltages are available; 5V, 7V and 10V. The 7V and 10V units can be used as shunt regulators (two terminal zeners) with the same precision characteristics as the three terminal connection. Special care has been taken to minimize thermal regulation effects and temperature induced hysteresis.

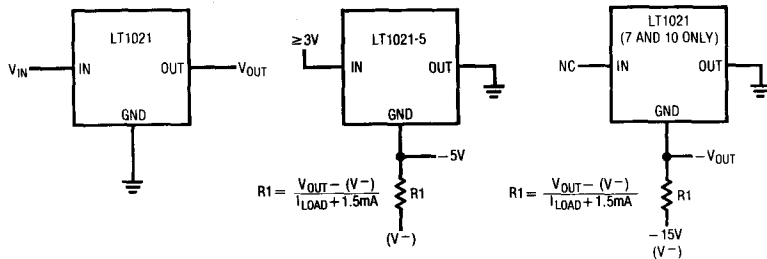
The LT1021 references are based on a buried zener diode structure which eliminates noise and stability problems associated with surface breakdown devices. Further, a subsurface zener exhibits better temperature drift and time stability than even the best band-gap references.

Unique circuit design makes the LT1021 the first IC reference to offer ultra low drift without the use of high power on-chip heaters.

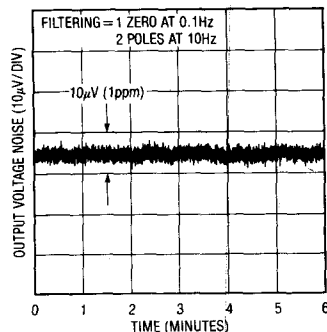
The LT1021-7 uses no resistive divider to set output voltage, and therefore exhibits the best long term stability and temperature hysteresis. The LT1021-5 and LT1021-10 are intended for systems requiring a precise 5V or 10V reference, with an initial tolerance as low as 0.05%.*

3

Basic Positive and Negative Connections



Output Noise 0.1Hz to 10Hz—LT1021-10



LT1021DCS8

ABSOLUTE MAXIMUM RATINGS

Input Voltage	40V
Input-Output Voltage Differential	35V
Output to Ground Voltage (Shunt Mode Current Limit)	
LT1021-5	10V
LT1021-7	10V
LT1021-10	16V
Trim Pin to Ground Voltage	
Positive	Equal to V_{OUT}
Negative	-20V
Output Short Circuit Duration	
$V_{IN} = 35V$	10 sec
$V_{IN} \leq 20V$	Indefinite
Operating Temperature Range	0°C to 70°C
Storage Temperature Range	
All Devices	-65°C to 150°C
Lead Temperature (Soldering, 10 sec.)	300°C

PACKAGE/ORDER INFORMATION

<p>S8 PACKAGE PLASTIC SO</p> <p>*CONNECTED INTERNALLY. DO NOT CONNECT EXTERNAL CIRCUITRY TO THESE PINS. **NO TRIM PIN ON LT1021-7. DO NOT CONNECT EXTERNAL CIRCUITRY TO PIN 5 ON LT1021-7.</p>	ORDER PART NUMBER
	LT1021DCS8-5 LT1021DCS8-7 LT1021DCS8-10
	PART MARKING
	2105 (5V VERSION) 2107 (7V VERSION) 2110 (10V VERSION)

ELECTRICAL CHARACTERISTICS LT1021-5 $V_{IN} = 10V, I_{OUT} = 0, T_A = 25^\circ C$, unless otherwise noted

PARAMETER	CONDITIONS	LT1021-5			UNITS
		MIN	TYP	MAX	
Output Voltage (Note 1)		4.95	5.00	5.05	V
Output Voltage Temperature Coefficient (Note 2)	$0^\circ C \leq T_J \leq 70^\circ C$		5	20	ppm/°C
Line Regulation (Note 3)	$7.2V \leq V_{IN} \leq 10V$	●	4	12	ppm/V
	$10V \leq V_{IN} \leq 40V$	●	2	6	ppm/V
Load Regulation (Sourcing Current)	$0 \leq I_{OUT} \leq 10mA$ (Note 3)	●	10	20	ppm/mA
		●		35	ppm/mA
Load Regulation (Sinking Current)	$0 \leq I_{OUT} \leq 10mA$ (Note 3)	●	60	100	ppm/mA
		●		150	ppm/mA
Supply Current		●	0.8	1.2	mA
		●		1.5	mA
Output Voltage Noise (Note 5)	$0.1Hz \leq f \leq 10Hz$		3		μV_{p-p}
	$10Hz \leq f \leq 1kHz$		2.2	3.5	μV_{rms}
Long Term Stability of Output Voltage			15		ppm/√khrs
Temperature Hysteresis of Output	$\Delta T = \pm 25^\circ C$		10		ppm

ELECTRICAL CHARACTERISTICS LT1021-7 $V_{IN} = 12V, I_{OUT} = 0, T_A = 25^\circ C$, unless otherwise noted

PARAMETER	CONDITIONS	LT1021-7			UNITS
		MIN	TYP	MAX	
Output Voltage (Note 1)		6.95	7.00	7.05	V
Output Voltage Temperature Coefficient (Note 2)	$T_{MIN} \leq T_J \leq T_{MAX}$		5	20	ppm/°C

ELECTRICAL CHARACTERISTICS LT1021-7 $V_{IN} = 12V, I_{OUT} = 0, T_A = 25^\circ C$, unless otherwise noted

PARAMETER	CONDITIONS	LT1021D-7			UNITS
		MIN	TYP	MAX	
Line Regulation (Note 3)	$8.5V \leq V_{IN} \leq 12V$	•	1	4	ppm/V
	$12V \leq V_{IN} \leq 40V$	•	2	8	ppm/V
Load Regulation (Sourcing Current)	$0 \leq I_{OUT} \leq 10mA$ (Note 3)	•	0.5	2	ppm/V
		•	1	4	ppm/V
Load Regulation (Shunt Mode)	$1.2mA \leq I_{SHUNT} \leq 10mA$ (Notes 3, 4)	•	12	25	ppm/mA
		•	50	40	ppm/mA
Supply Current (Series Mode)		•	0.75	1.2	mA
		•		1.5	mA
Minimum Current (Shunt Mode)	V_{IN} is Open	•	0.7	1.0	mA
		•		1.2	mA
Output Voltage Noise (Note 5)	$0.1Hz \leq f \leq 10Hz$ $10Hz \leq f \leq 1kHz$		4		$\mu Vp-p$
			2.5	4	$\mu Vrms$
Long Term Stability of Output Voltage			7		ppm/ \sqrt{khrs}
Temperature Hysteresis of Output	$\Delta T = \pm 25^\circ C$		3		ppm

ELECTRICAL CHARACTERISTICS LT1021-10 $V_{IN} = 15V, I_{OUT} = 0, T_A = 25^\circ C$, unless otherwise noted

PARAMETER	CONDITIONS	LT1021D-10			UNITS	
		MIN	TYP	MAX		
Output Voltage (Note 1)			9.95	10.00	10.05	V
Output Voltage Temperature Coefficient (Note 2)	$T_{MIN} \leq T_J \leq T_{MAX}$		5	20		ppm/ $^\circ C$
Line Regulation (Note 3)	$11.5V \leq V_{IN} \leq 14V.5$	•	1	4	6	ppm/V
	$14.5V \leq V_{IN} \leq 40V$	•	0.5	2	4	ppm/V
Load Regulation (Sourcing Current)	$0 \leq I_{OUT} \leq 10mA$ (Note 3)	•	12	25	40	ppm/mA
		•	50	100	150	ppm/mA
Load Regulation (Shunt Mode)	$1.7mA \leq I_{SHUNT} \leq 10mA$ (Notes 3, 4)	•	1.2	1.7	2.0	mA
		•		2.0		mA
Series Mode Supply Current			1.1	1.5	1.7	mA
Shunt Mode Minimum Current	V_{IN} is Open	•		1.7		mA
Output Voltage Noise (Note 5)	$0.1Hz \leq f \leq 10Hz$ $0.1Hz \leq f \leq 1kHz$		6			$\mu Vp-p$
			3.5	6		$\mu Vrms$
Long Term Stability of Output Voltage	$\Delta t = 1000 Hrs$ Non-Cumulative		15			ppm/ \sqrt{khrs}
Temperature Hysteresis of Output	$\Delta T = \pm 25^\circ C$		5			ppm

The • denotes the specifications which apply over the full operating temperature range.

Note 1: Output voltage is measured immediately after turn-on. Changes due to chip warm-up are typically less than 0.005%.

Note 2: Temperature coefficient is guaranteed as a slope from room temperature (25°C) to 0°C and 70°C, also known as a "butterfly" specification.

Note 3: Line and load regulation are measured on a pulse basis. Output changes due to die temperature change must be taken into account separately. Package thermal resistance is 110°C/W.

Note 4: Shunt mode regulation is measured with the input open. With the input connected, shunt mode current can be reduced to 0mA. Load regulation will remain the same.

Note 5: RMS noise is measured with a single high pass filter at 10Hz and a 2-pole low pass filter at 1 kHz. The resulting output is full wave rectified and then integrated for a fixed period, making the final reading an average as opposed to RMS. A correction factor of 1.1 is used to convert from average to RMS, and a second correction of 0.88 is used to correct for the non-ideal bandpass of the filters.

Peak-to-peak noise is measured with a single high pass filter at 0.1Hz and a 2-pole low pass filter at 10Hz. The unit is enclosed in a still-air environment to eliminate thermocouple effects on the leads. Test time is 10 seconds.

3

NOTES

FEATURES

- 0.2% Output Tolerance
- 0.5Ω Shunt Impedance
- 600μA to 10mA Operating Current
- Pin Compatible with LM136-5
- 20ppm/°C Max. Drift
- Output Voltage Trim does not Affect Drift
- Can be Used as Positive or Negative Reference

APPLICATIONS

- A-to-D and D-to-A Converters
- Precision Regulators
- Precision Current Sources
- V to F and F to V Converters

DESCRIPTION

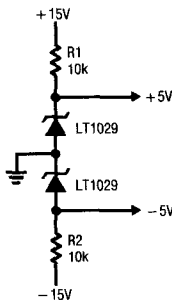
The LT1029 is a 5V bandgap reference intended for use in the shunt or "zener" mode, allowing it to be used as either a positive or negative reference. The output is pretrimmed to $\pm 0.2\%$ accuracy with 20ppm/°C maximum temperature drift. A trim pin allows additional output adjustment for even more precise output voltage.

Operating current range for the LT1029 is 600μA to 10mA. Extremely low dynamic impedance allows excellent output regulation even with fluctuating operating current.

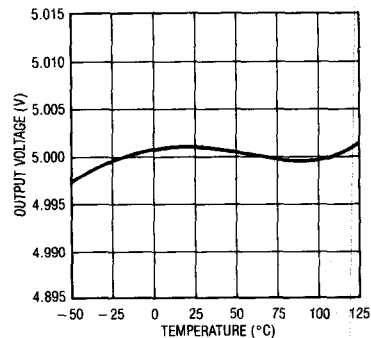
The LT1029 will replace an LM136-5 or LM336-5 and simplify circuits using the "minimum temperature coefficient" trim network. The LT1029 does not require this special network to meet its temperature drift specification and these application network components are simply removed. If output trimming is required for initial accuracy, the diodes in the trim network should be replaced with jumpers.

3

TYPICAL APPLICATION



Output Voltage Drift

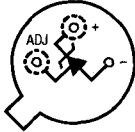
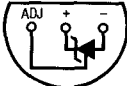


LT1029/LT1029A

ABSOLUTE MAXIMUM RATINGS

Reverse Current	15mA
Forward Current	10mA
Operating Temperature Range	
LT1029M/LT1029AM	-55°C to +125°C
LT1029C/LT1029AC	0°C to +70°C
Storage Temperature	-65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°C

PACKAGE/ORDER INFORMATION

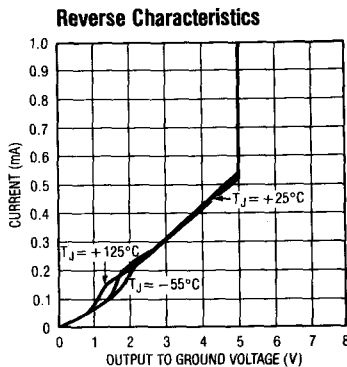
 <p>H PACKAGE TO-46 METAL CAN BOTTOM VIEW</p>	ORDER PART NUMBER
	LT1029AMH LT1029MH LT1029ACH LT1029CH
 <p>Z PACKAGE TO-92 PLASTIC BOTTOM VIEW</p>	LT1029ACZ LT1029CZ

ELECTRICAL CHARACTERISTICS

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Reverse Breakdown Voltage	$I_R = 1\text{mA}$ LT1029AM, LT1029AC LT1029M, LT1029C	4.99	5.00	5.01	V
		4.95	5.00	5.05	V
Reverse Breakdown Change with Current	$600\mu\text{A} \leq I_R \leq 10\text{mA}$	●	2	5	mV
		●	3	8	mV
Reverse Dynamic Impedance	$I_R = 1\text{mA}$	●	0.2	0.6	Ω
		●	0.3	1.0	Ω
Temperature Stability	$I_R = 1\text{mA}$ LT1029AC LT1029C LT1029AM LT1029M	●	3	7	mV
		●	5	12	mV
		●	7	18	mV
		●	10	36	mV
Equivalent Temperature Drift	LT1029AM, LT1029AC LT1029C LT1029M	●	8	20	ppm/°C
		●	12	34	ppm/°C
		●	15	40	ppm/°C
Long Term Stability			20		ppm/kHr
Trim Range		± 3	+5, -13		%

The ● denotes the specifications which apply over the full operating temperature range.

TYPICAL PERFORMANCE CHARACTERISTICS



3

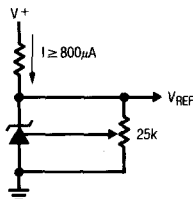
APPLICATIONS INFORMATION

Output Trimming

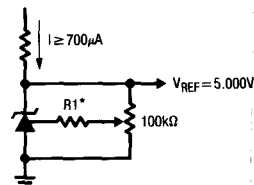
Output voltage trimming on the LT1029 is nominally accomplished with a potentiometer connected from output to ground with the wiper tied to the trim pin. The LT1029 was made compatible with existing references, so the trim range is large; +5%, -13%. This large trim range makes precision trimming rather difficult. One solution is to insert resistors in series with both ends of the potentiometer. This has the disadvantage of potentially poor tracking between the fixed resistors and the potentiometer. A second method of reducing trim range is to insert a resistor in series with the wiper of the potentiometer. This works well only for a very

small trim range because of the mismatch in TCs between the series resistor and the internal thin film resistors. These film resistors can have a TC as high as 500ppm/°C. That same TC is then transferred to the change in output voltage; a 1% shift in output voltage causes a (500ppm) (1%) = 5ppm/°C change in output voltage drift. The worst-case error in initial output voltage for the LT1029A is 0.2% and for the LT1029 is 1%, so a series resistor is satisfactory if the output is simply trimmed to nominal value. 1ppm/°C TC shift would be the maximum expected for the LT1029A and 5ppm/°C for the LT1029.

Wide Trim Range (+5%, -13%)



Narrow Trim Range



TRIM RANGE
 0.4% — LT1029A, R1 = 750k
 1.2% — LT1029, R1 = 250k

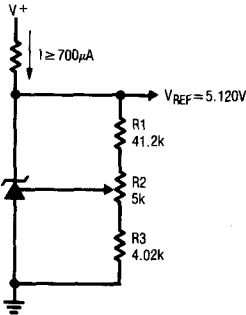
APPLICATIONS INFORMATION

Shunt Capacitance

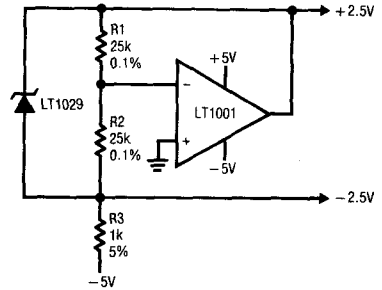
The LT1029 is stable with all values of shunt capacitance, but values between 300pF and 0.01 μ F are not recommended because they cause longer settling following a

transient in operating current. A 1 μ F solid tantalum capacitor is suggested for most situations where bypassing is desirable.

Trimming Output to 5.120V



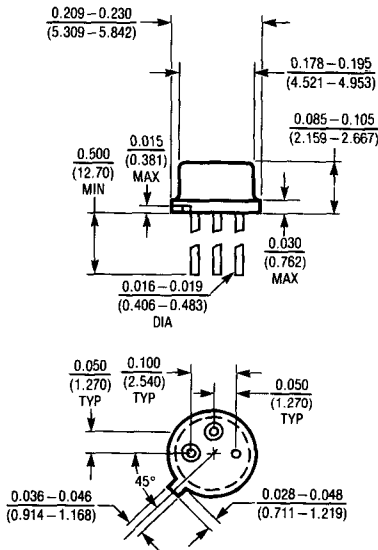
Split $\pm 2.5V$ References



PACKAGE DESCRIPTION

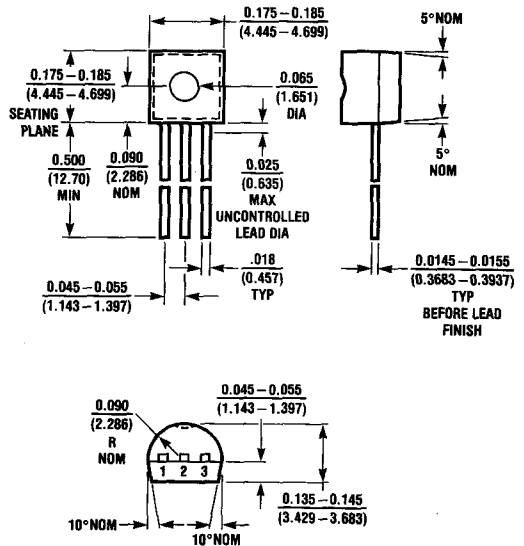
Dimensions in inches (millimeters) unless otherwise noted.

H Package
TO-46 Metal Can



T_{jmax}	θ_{JA}	θ_{JC}
150°C	440°C/W	80°C/W

Z Package
TO-92 Plastic



T_{jmax}	θ_{JA}
100°C	160°C/W

FEATURES

- Pin Compatible with LH0070 and AD581*
- Ultra Low Drift—5ppm/°C Max Slope
- Trimmed Output Voltage
- Operates in Series or Shunt Mode
- Output Sinks and Sources in Series Mode
- Very Low Noise < 1ppm p-p 0.1Hz to 10Hz
- > 100dB Ripple Rejection
- Minimum Input Voltage of 11V

APPLICATIONS

- A to D and D to A Converters
- Precision Regulators
- Digital Voltmeters
- Inertial Navigation Systems
- Precision Scales
- Portable Reference Standard

*See LH0070 Electrical Characteristics table and AD581 cross reference guide.

DESCRIPTION

The LT1031 is a precision 10V reference with ultra low drift and noise, extremely good long term stability, and almost total immunity to input voltage variations. The reference output will both source and sink up to 10mA and can be used as a shunt regulator (two terminal zener) with the same precision characteristics as the three terminal connection. Special care has been taken to minimize thermal regulation effects and temperature induced hysteresis.

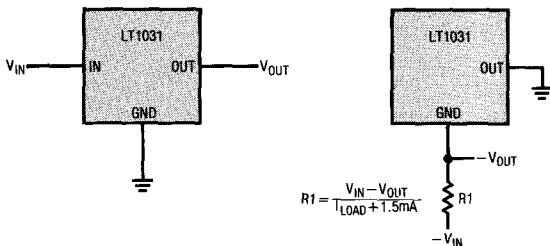
The LT1031 reference is based on a buried zener diode structure which eliminates noise and stability problems associated with surface breakdown devices. Further, a subsurface zener exhibits better temperature drift and time stability than even the best band-gap references.

Unique circuit design makes the LT1031 the first three terminal IC reference to offer ultra low drift without the use of high power on-chip heaters. Output voltage is pre-trimmed to 0.05% accuracy.

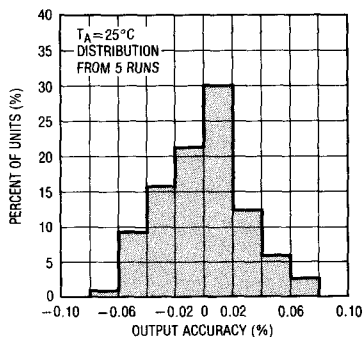
The LT1031 can be used as a plug-in replacement for the AD581 and LH0070*, with improved electrical and thermal performance.

3

Basic Positive and Negative Connections



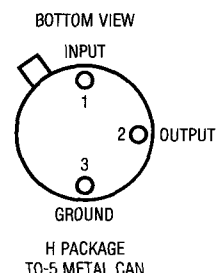
Distribution of Output Accuracy



ABSOLUTE MAXIMUM RATINGS

Input Voltage	40V
Input-Output Voltage Differential	35V
Output to Ground Voltage (Shunt Mode Current Limit)	16V
Trim Pin to Ground Voltage	
Positive	Equal to V_{OUT}
Negative	-20V
Output Short Circuit Duration	
$V_{IN} = 35V$	10 sec
$V_{IN} \leq 20V$	Indefinite
Operating Temperature Range	
LT1031 (Mil)	-55°C to 125°C
LT1031 (Comm)	0°C to 70°C
Storage Temperature Range	-65°C to 150°C
Lead Temperature (Soldering, 10 sec.)	300°C

PACKAGE/ORDER INFORMATION

	ORDER PART NUMBER
	LH0070-0H LH0070-1H LH0070-2H LT1031BMH LT1031CMH LT1031DMH LT1031BCH LT1031CCH LT1031DCH

ELECTRICAL CHARACTERISTICS LT1031

$V_{IN} = 15V$, $I_{OUT} = 0$, $T_A = 25^\circ C$, Mil or Comm version, unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS	LT1031			UNITS	
			MIN	TYP	MAX		
V_R	Output Voltage (Note 1)	LT1031B	9.995	10.000	10.005	V	
		LT1031C	9.990	10.000	10.010	V	
		LT1031D	9.980	10.000	10.020	V	
$\frac{\Delta V_R}{\Delta T}$	Output Voltage Temperature Coefficient (Note 2)	$T_{MIN} \leq T_J \leq T_{MAX}$					
		LT1031B	●	3	5	ppm/°C	
		LT1031C	●	6	15	ppm/°C	
		LT1031D	●	10	25	ppm/°C	
$\frac{\Delta V_R}{\Delta V_{IN}}$	Line Regulation (Note 3)	$11.5V \leq V_{IN} \leq 14.5V$	●	1	4	ppm/V	
		$14.5V \leq V_{IN} \leq 40V$	●	0.5	6	2	ppm/V
			●		4		ppm/V
$\frac{\Delta V_R}{\Delta I_O}$	Load Regulation (Sourcing Current)	$0 \leq I_{OUT} \leq 10mA$ (Note 3)	●	12	25	ppm/mA	
					40	ppm/mA	
$\frac{\Delta V_R}{\Delta I_O}$	Load Regulation (Shunt Mode)	$1.7mA \leq I_{SHUNT} \leq 10mA$ (Notes 3, 4)	●	50	100	ppm/mA	
					150	ppm/mA	
I_O	Series Mode Supply Current		●	1.2	1.7	mA	
					2.0	mA	
I_{MIN}	Shunt Mode Minimum Current	V_{IN} is Open	●	1.1	1.5	mA	
					1.7	mA	
	Output Short Circuit Current	$11V \leq V_{IN} \leq 35V$		30		mA	
	Minimum Input Voltage (Note 6)	$I_{OUT} \leq 1mA$		10.8	11.0	V	
e_n	Output Voltage Noise	$0.1Hz \leq f \leq 10Hz$		6		$\mu Vp-p$	
		$0.1Hz \leq f \leq 10kHz$		11		$\mu Vrms$	
$\frac{\Delta V_R}{\Delta Time}$	Long Term Stability of Output Voltage	$\Delta t = 1000$ Hrs Non-Cumulative		15		ppm	
		Temperature Hysteresis of Output	$\Delta T = 50^\circ C$		5		ppm

ELECTRICAL CHARACTERISTICS LH0070

$V_{IN} = 15V$, $R_L = 10k\Omega$, $-55^\circ C \leq T_A \leq +125^\circ C$ unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_R	Output Voltage	$T_A = 25^\circ C$		10.000		V
ΔV_R	Output Accuracy -0, -1 -2	$T_A = 25^\circ C$		± 0.03 ± 0.02	± 0.1 ± 0.05	% %
ΔV_R	Output Accuracy -0, -1 -2	$T_A = -55^\circ C, 125^\circ C$	●		± 0.3 ± 0.2	% %
$\frac{\Delta V_R}{\Delta T}$	Output Voltage Change with Temperature -0 -1 -2	Note 5	● ● ●	± 0.02 ± 0.01	± 0.2 ± 0.1 ± 0.04	% % %
$\frac{\Delta V_R}{\Delta V_{IN}}$	Line Regulation -0, -1 -2	$13V \leq V_{IN} \leq 33V$, $T_A = 25^\circ C$		0.006 0.006	0.1 0.03	% %
	Input Voltage Range		●	11.4	40	V
$\frac{\Delta V_R}{\Delta I_O}$	Load Regulation	$0mA \leq I_{OUT} \leq 5mA$	●	0.01	0.03	%
I_Q	Quiescent Current	$13V \leq V_{IN} \leq 33V$	●	1.2	5	mA
$\frac{\Delta I_Q}{\Delta V_{IN}}$	Change in Quiescent Current	$\Delta V_{IN} = 20V$ from 13V to 33V	●	0.1	1.5	mA
e_n	Output Noise Voltage			6		μV_{p-p}
	Ripple Rejection	$f = 120Hz$	●	0.001		%/V _{p-p}
r_o	Output Resistance		●	0.2	0.6	Ω
$\frac{\Delta V_Z}{\Delta Time}$	Long Term Stability -0, -1 -2	$T_A = 25^\circ C$ (Note 7)			± 0.2 ± 0.05	%/Yr %/Yr

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: Output voltage is measured immediately after turn-on. Changes due to chip warm-up are typically less than 0.005%.

Note 2: Temperature coefficient is measured by dividing the change in output voltage over the temperature range by the change in temperature. Separate tests are done for hot and cold; T_{MIN} to 25°C, and 25°C to T_{MAX} . **Incremental slope is also measured at 25°C.** For LT1031BMH, the 5ppm/°C drift specification is for -25°C to 85°C. Drift over the full -55°C to +125°C range is guaranteed to 7ppm/°C.

Note 3: Line and load regulation are measured on a pulse basis. Output changes due to die temperature change must be taken into account separately. Package thermal resistance is 150°C/W.

Note 4: Shunt mode regulation is measured with the input open. With the input connected, shunt mode current can be reduced to 0mA. Load regulation will remain the same.

Note 5: Temperature drift is guaranteed from -25°C to +85°C on LH0070.

Note 6: See curve for guaranteed minimum V_{IN} versus I_{OUT} .

Note 7: Guaranteed by design.

CROSS REFERENCE

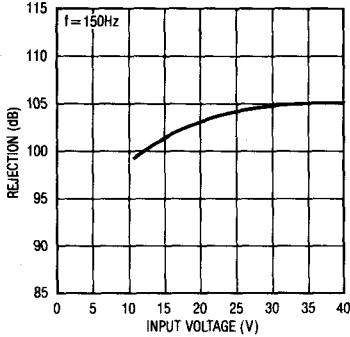
The following cross reference guide may be used to select LT1031 grades which meet or exceed output voltage, temperature drift, load and line regulation, and output current specifications of the AD581 reference. Parameters such as noise, hysteresis, and long term stability will be significantly better for all LT1031 grades compared to the AD581.

Cross Reference Guide—LT1031 to AD581

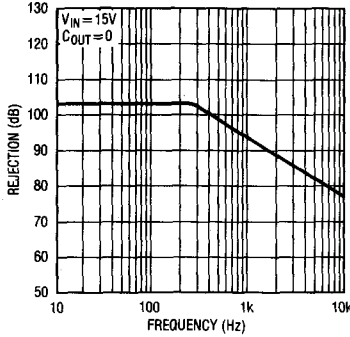
AD581J	order	LT1031DCH
AD581K	order	LT1031CCH
AD581L	order	LT1031BCH
AD581S	order	LT1031DMH
AD581T	order	LT1031CMH
AD581U	order	LT1031BMH

TYPICAL PERFORMANCE CHARACTERISTICS

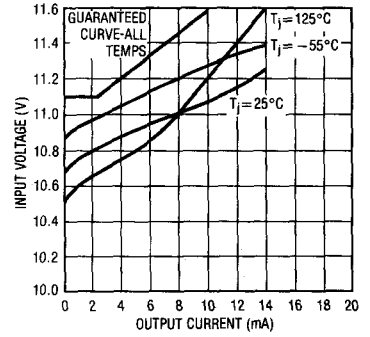
Ripple Rejection



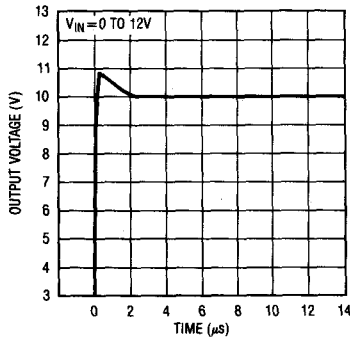
Ripple Rejection



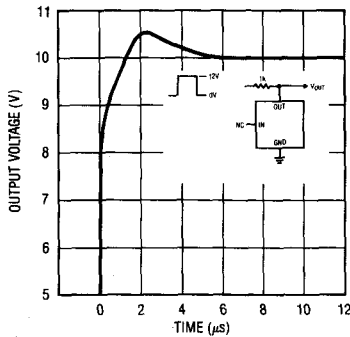
Minimum Input Voltage



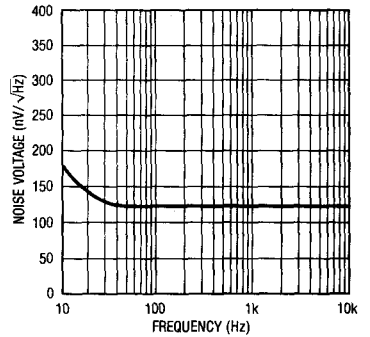
Start-Up (Series Mode)



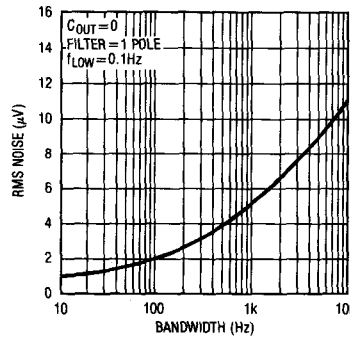
Start-Up (Shunt Mode)



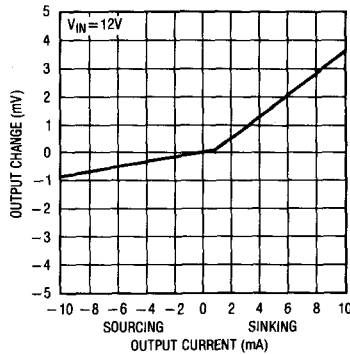
Output Voltage Noise Spectrum



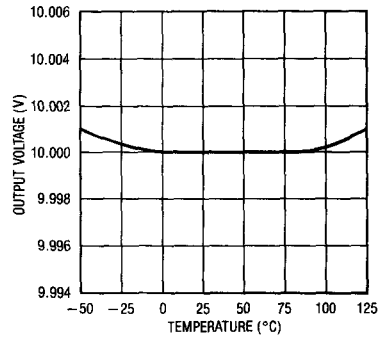
Output Voltage Noise



Load Regulation

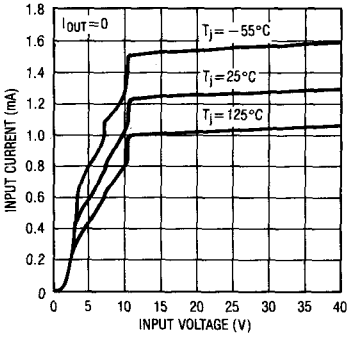


Output Voltage Temperature Drift

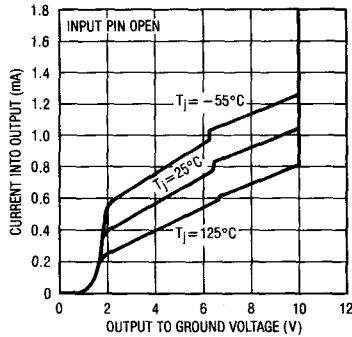


TYPICAL PERFORMANCE CHARACTERISTICS

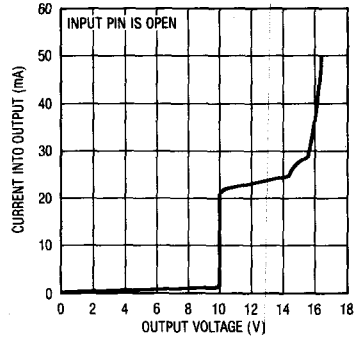
Input Supply Current



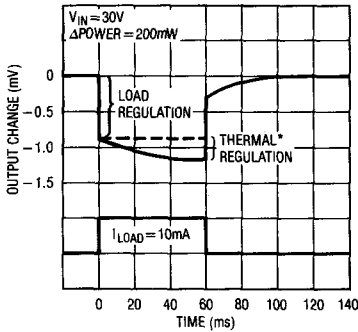
Shunt Characteristics



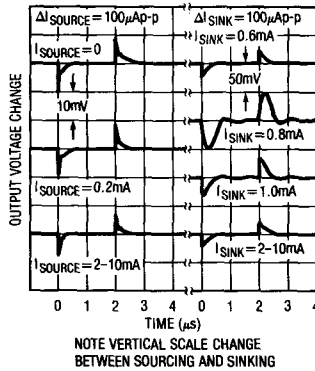
Shunt Mode Current Limit



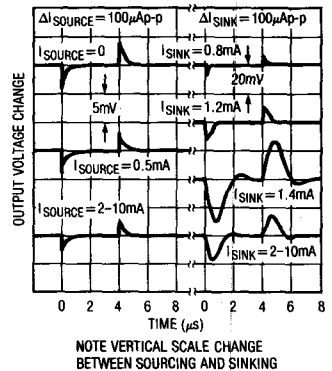
Thermal Regulation



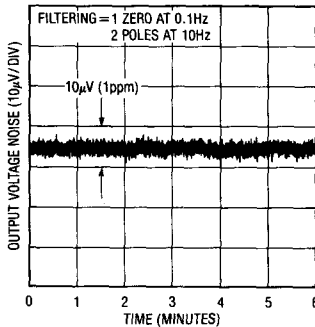
Load Transient Response $C_{LOAD} = 0$



Load Transient Response $C_{LOAD} = 1000\text{pF}$



Output Noise 0.1Hz to 10Hz



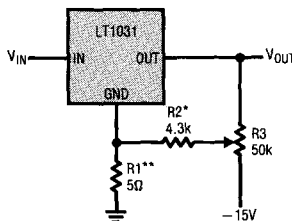
3

APPLICATIONS INFORMATION

Trimming Output Voltage

The LT1031 output can be trimmed by driving the ground pin. The suggested method is shown in the accompanying figure. A 5Ω resistor is inserted in series with the ground pin and the top of the resistor is supplied current from a trim potentiometer. This technique requires fairly high trim current—up to 1.5mA from the LT1031 or 3.5mA from the -15V supply, but it is necessary to maintain low drift in the reference. Ground pin current changes in the LT1031 (with temperature) could be as high as $4\mu\text{A}/^\circ\text{C}$. This, coupled with the 5Ω external resistor, creates up to $2\text{ppm}/^\circ\text{C}$ drift in the reference ($5\Omega \times 4\mu\text{A}/^\circ\text{C} = 20\mu\text{V}/^\circ\text{C} = 2\text{ppm}/^\circ\text{C}$). If induced drift higher than this can be tolerated, all resistor values in the trim circuit can be raised proportionately to reduce current drain.

Output Voltage Trimming

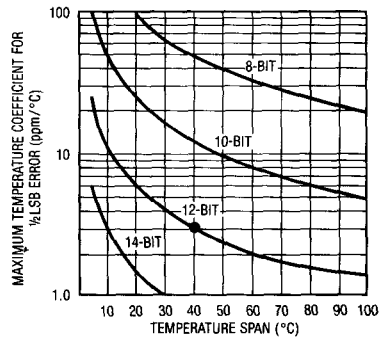


*CAN BE INCREASED TO 5.6k FOR
LT1031B AND LH0070-2
**INCREASE TO 10Ω FOR LT1031D

Effect of Reference Drift on System Accuracy

A large portion of the temperature drift error budget in many systems is the system reference voltage. This graph indicates the maximum temperature coefficient allowable if the reference is to contribute no more than $\frac{1}{2}$ LSB error to the overall system performance. The example shown is a 12-bit system designed to operate over a temperature range from 25°C to 65°C . Assuming the system calibration is performed at 25°C , the temperature span is 40°C . It can be seen from the graph that the temperature coefficient of the reference must be no worse than $3\text{ppm}/^\circ\text{C}$ if it is to contribute less than $\frac{1}{2}$ LSB error. For this reason, the LT1031 has been optimized for low drift.

Maximum Allowable Reference Drift



Capacitive Loading and Transient Response

The LT1031 is stable with all capacitive loads, but for optimum settling with load transients, output capacitance should be under 1000pF . The output stage of the reference is class AB with a fairly low idling current. This makes transient response worst-case at light load currents. Because of internal current drain on the output, actual worst-case occurs at $I_{\text{LOAD}} = 1.4\text{mA}$ (sinking). Significantly better load transient response is obtained by moving slightly away from these points. See Load Transient Response curves for details. In general, best transient response is obtained when the output is sourcing current. In critical applications, a $10\mu\text{F}$ solid tantalum capacitor with several ohms in series provides optimum output bypass.

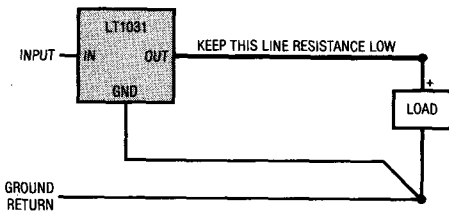
Kelvin Connections

Although the LT1031 does not have true force/sense capability at its outputs, significant improvements in ground loop and line loss problems can be achieved with proper hook-up. In series mode operation, the ground pin of the LT1031 carries only $\approx 1\text{mA}$ and can be used as a sense line, greatly reducing ground loop and loss problems on the low side of the reference. The high side supplies load current so line resistance must be kept low. Twelve feet of #22 gauge hook up wire or 1 foot of 0.025 inch printed circuit trace will create 2mV loss at 10mA output current. This is equivalent to 1LSB in a 10V , 12-bit system.

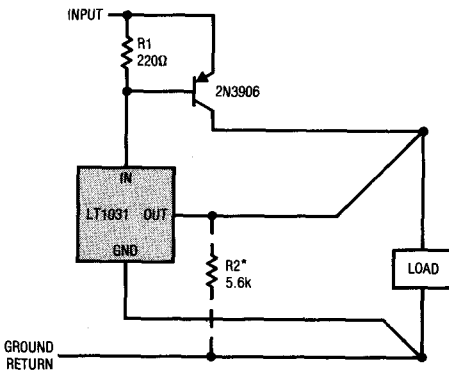
APPLICATIONS INFORMATION

The circuits below show proper hook up to minimize errors due to ground loops and line losses. Losses in the output lead can be greatly reduced by adding a PNP boost transistor if load currents are 5mA or higher. R2 can be added to further reduce current in the output sense lead.

Standard Series Mode



Series Mode with Boost Transistor



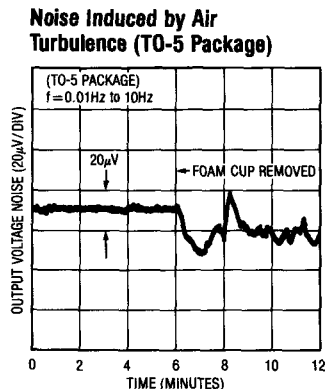
*OPTIONAL—REDUCES CURRENT IN OUTPUT SENSE LEAD

Effects of Air Movement on Low Frequency Noise

The LT1031 has very low noise because of the buried zener used in its design. In the 0.1Hz to 10Hz band, peak-to-peak noise is about 0.5ppm of the DC output. To achieve this low noise, however, care must be taken to shield the reference from ambient air turbulence. Air

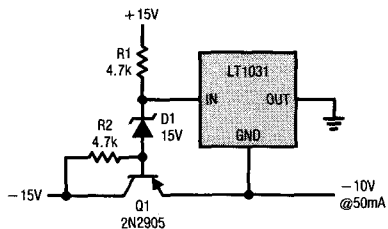
movement can create noise because of thermoelectric differences between IC package leads (especially kovar lead TO-5) and printed circuit board materials and/or sockets. Power dissipation in the reference, even though it rarely exceeds 20mW, is enough to cause small temperature gradients in the package leads. Variations in thermal resistance, caused by uneven air flow, create differential lead temperatures, thereby causing thermoelectric voltage noise at the output of the reference. The XY plotter trace shown below dramatically illustrates this effect. The first half of the plot was done with the LT1031 shielded from ambient air with a small foam cup. The cup was then removed for the second half of the trace. Ambient in both cases was a lab environment with no excessive air turbulence from air conditioners, opening/closing doors, etc. Removing the foam cup increases the output noise by almost an order of magnitude in the 0.01Hz to 1Hz band! The kovar leads of the TO-5 (H) package are the primary culprit. Alloy 42 and copper lead frames used on dual-in-line packages are not nearly as sensitive to thermally generated noise because they are intrinsically matched.

There is nothing magical about foam cups—any enclosure which blocks air flow from the reference will do. Smaller enclosures are better since they do not allow the build-up of internally generated air movement. Naturally, heat generating components external to the reference itself should not be included inside the enclosure.

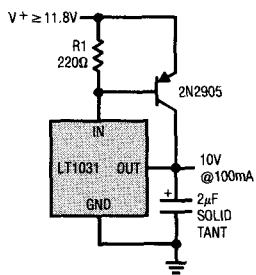


APPLICATION CIRCUITS

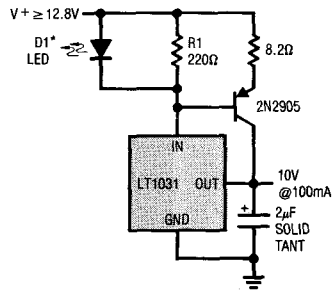
Negative Series Reference



Boosted Output Current With No Current Limit



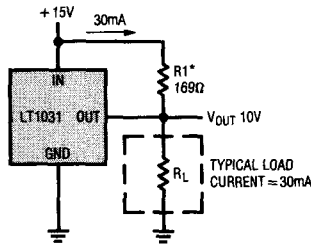
Boosted Output Current With Current Limit



*GLOWS IN CURRENT LIMIT.
DO NOT OMIT.

APPLICATION CIRCUITS

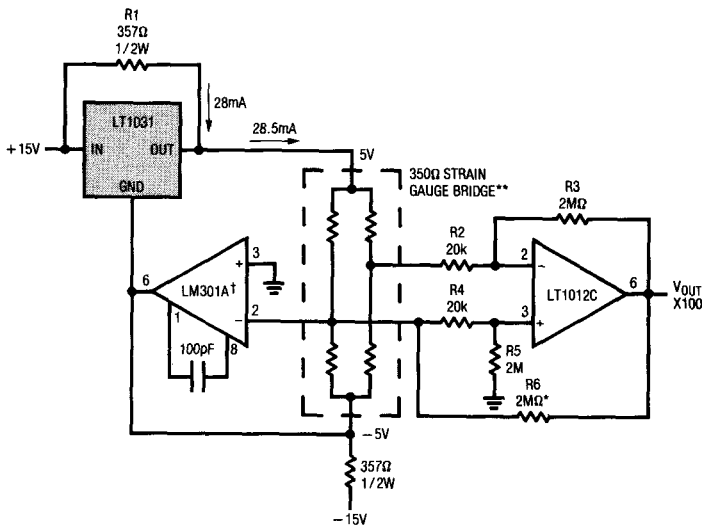
Handling Higher Load Currents



*SELECT R1 TO DELIVER TYPICAL LOAD CURRENT. LT1031 WILL THEN SOURCE OR SINK AS NECESSARY TO MAINTAIN PROPER OUTPUT. DO NOT REMOVE LOAD AS OUTPUT WILL BE DRIVEN UNREGULATED HIGH. LINE REGULATION IS DEGRADED IN THIS APPLICATION.

3

Strain Gauge Conditioner for 350Ω Bridge



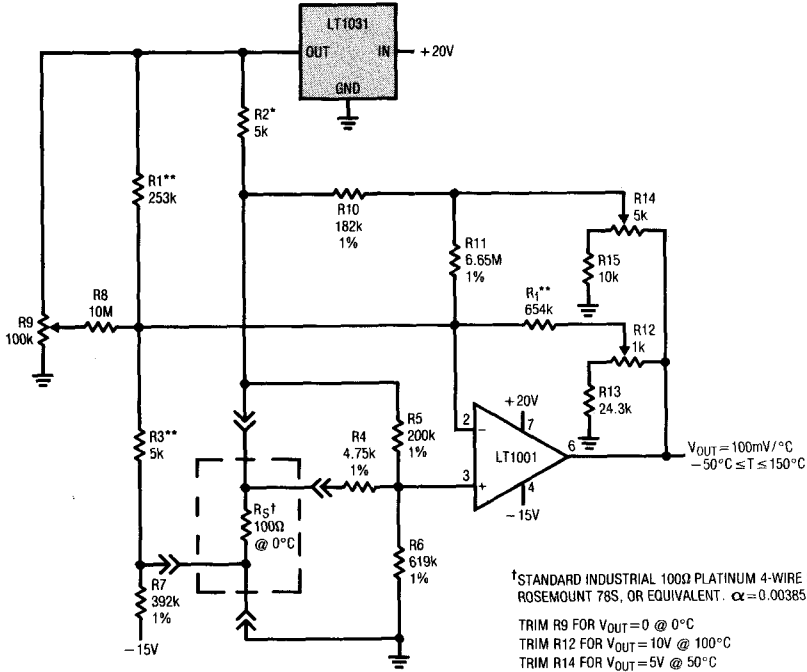
*THIS RESISTOR PROVIDES POSITIVE FEEDBACK TO THE BRIDGE TO ELIMINATE LOADING EFFECT OF THE AMPLIFIER. EFFECTIVE Z_{IN} OF AMPLIFIER STAGE IS $\geq 1M\Omega$. IF R2-R5 ARE CHANGED, SET R6=R3.

**BRIDGE IS ULTRA LINEAR WHEN ALL LEGS ARE ACTIVE, TWO IN COMPRESSION AND TWO IN TENSION, OR WHEN ONE SIDE IS ACTIVE WITH ONE COMPRESSED AND ONE TENSIONED LEG.

[†]OFFSET AND DRIFT OF LM301A ARE VIRTUALLY ELIMINATED BY DIFFERENTIAL CONNECTION OF LT1012C.

APPLICATION CIRCUITS

Ultra Linear Platinum Temperature Sensor*



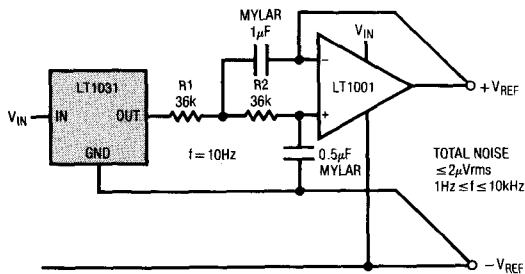
†STANDARD INDUSTRIAL 100Ω PLATINUM 4-WIRE SENSOR, ROSEMOUNT 78S, OR EQUIVALENT. $\alpha = 0.00385$

TRIM R9 FOR $V_{OUT} = 0$ @ 0°C
 TRIM R12 FOR $V_{OUT} = 10\text{V}$ @ 100°C
 TRIM R14 FOR $V_{OUT} = 5\text{V}$ @ 50°C
 USE TRIM SEQUENCE AS SHOWN. TRIMS ARE NON-INTERACTIVE SO THAT ONLY ONE TRIM SEQUENCE IS NORMALLY REQUIRED.

*FEEDBACK LINEARIZES OUTPUT TO $\pm 0.005^\circ\text{C}$ FROM -50°C TO $+150^\circ\text{C}$

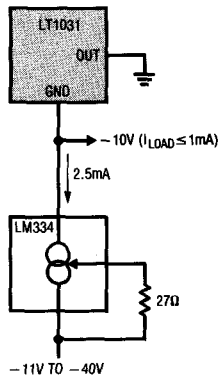
**WIREWOUND RESISTORS WITH LOW TC

2-Pole Low Pass Filtered Reference



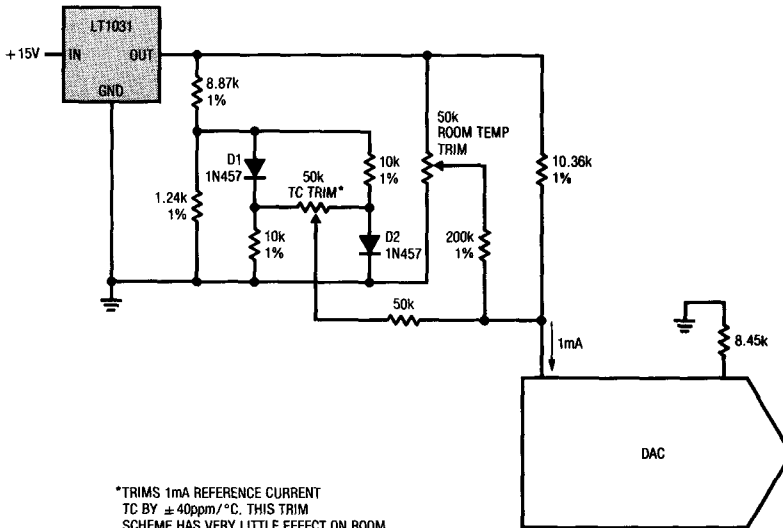
APPLICATION CIRCUITS

Negative Shunt Reference Driven by Current Source



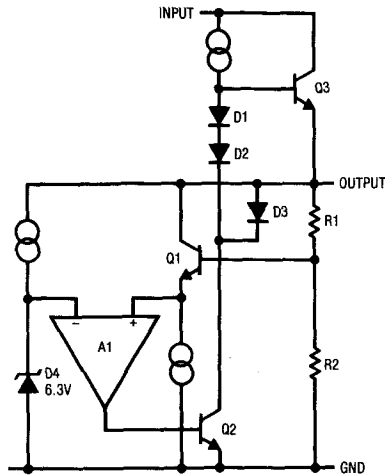
3

Precision DAC Reference with System TC Trim



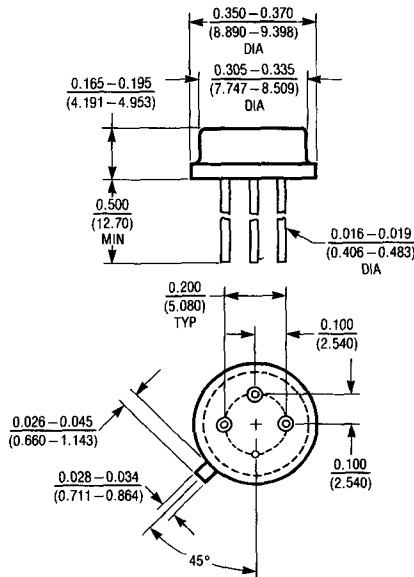
*TRIMS 1mA REFERENCE CURRENT
 TC BY $\pm 40\text{ppm}/^\circ\text{C}$. THIS TRIM
 SCHEME HAS VERY LITTLE EFFECT ON ROOM
 TEMPERATURE CURRENT TO MINIMIZE ITERATIVE
 TRIMMING.

EQUIVALENT SCHEMATIC



PACKAGE DESCRIPTION

T0-5



	T_{jmax}	θ_{JA}	θ_{JC}
LH0070	150°C	150°C/W	45°C/W
LT1031M	150°C	150°C/W	45°C/W
LT1031C	85°C	150°C/W	45°C/W

FEATURES

- Guaranteed 20 ppm/°C Drift
- 1.2V 1% Initial Tolerance
- 20 μ A to 20mA Operation
- 1 Ω Dynamic Impedance
- 7V, 100 μ A Reference

APPLICATIONS

- Portable Meters
- Precision Regulators
- Calibrators

DESCRIPTION

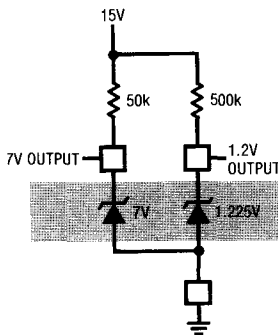
The LT1034 is a micropower, precision 1.2V/2.5V reference combined with a 7V auxiliary reference. The 1.2V/2.5V reference is a trimmed, thin-film, band-gap voltage reference with 1% initial tolerance and guaranteed 20ppm/°C temperature drift. Operating on only 20 μ A, the LT1034 offers guaranteed drift, low temperature cycling hysteresis and good long term stability. The low dynamic impedance makes the LT1034 easy to use from unregulated supplies. The 7V reference is a subsurface band-gap device for less demanding applications.

The LT1034 reference can be used as a high performance substitute for the LM385 or LM100, where guaranteed temperature drift is desired.

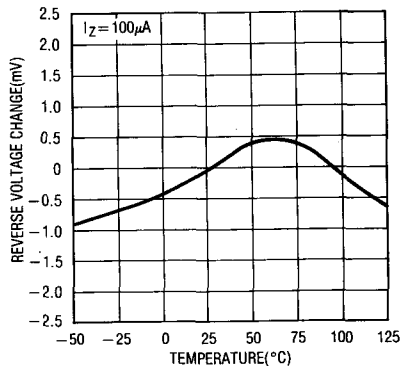
REFER TO TABLE OF CONTENTS
FOR REVISED DATA LOCATION

3

TYPICAL APPLICATION



Temperature Drift LT1034C-1.2

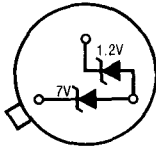
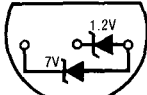


LT1034-1.2/LT1034-2.5

ABSOLUTE MAXIMUM RATINGS

Operating Current.....	20mA
Forward Current (Note 1)	20mA
Operating Temperature Range	
LT1034BM, M.....	-55°C to 125°C
LT1034BC, C.....	0°C to 70°C
Storage Temperature	-65°C to 150°C
Lead Temperature (Soldering, 10 sec.).....	300°C

PACKAGE/ORDER INFORMATION

 <p>H PACKAGE TO-46 METAL CAN BOTTOM VIEW</p>	ORDER PART NUMBER
	LT1034BMH-1.2, LT1034MH-1.2 LT1034BCH-1.2, LT1034CH-1.2 LT1034BMH-2.5, LT1034MH-2.5 LT1034BCH-2.5, LT1034CH-2.5
 <p>Z PACKAGE TO-92 PLASTIC BOTTOM VIEW</p>	LT1034BCZ-1.2 LT1034CZ-1.2 LT1034BCZ-2.5 LT1034CZ-2.5

Available in SO Package

ELECTRICAL CHARACTERISTICS

PARAMETER	CONDITIONS		LT1034C-1.2			LT1034C-2.5			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Reverse Breakdown Voltage	$I_R = 100\mu A$	25°C	1.210	1.225	1.240	2.46	2.5	2.54	V
		●	1.205	1.225	1.245	2.43	2.5	2.57	V
Reverse Breakdown Change with Current	Note 3 $2mA \leq I_R \leq 20mA$	25°C		0.5	2.0		1	3	mV
		●		1.0	4.0		1.5	6	mV
		25°C		4	8.0		6	16	mV
		●		6.0	15.0		10	20	mV
Minimum Operating Current		●		10	20		15	30	μA
Temperature Coefficient	$I_R = 100\mu A$	●		20	40		20	40	ppm/°C
Reverse Dynamic Impedance (Note 2)	$I_R = 100\mu A$	25°C		0.25	1.0		0.5	1.5	Ω
		●		0.50	2.0		1	2.5	Ω
Low Frequency Noise	$I_R = 100\mu A, 0.1Hz \leq F \leq 10Hz$	●		4			6		$\mu Vp-p$
Long Term Stability	$I_R = 100\mu A, T = 25^\circ C$	25°C		20			20		ppm/ \sqrt{khrs}

ELECTRICAL CHARACTERISTICS 7V Reference

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Reverse Breakdown Voltage	$I_R = 100\mu A$	25°C	6.8	7.0	7.3	V
		●	6.75	7.0	7.4	V
Reverse Breakdown Change with Current	$100\mu A \leq I_R \leq 1mA$ $100\mu A \leq I_R \leq 1mA$ $1mA \leq I_R \leq 20mA$ $1mA \leq I_R \leq 20mA$	25°C		90	140	mV
		●		100	190	mV
		25°C		160	250	mV
		●		200	350	mV
Temperature Coefficient	$I_R = 100\mu A$	●		40		ppm/°C
Long Term Stability	$I_R = 100\mu A$	25°C		20		ppm

The ● denotes specifications that apply over the operating temperature range.

Note 1: Forward biasing either diode will affect the operation of the other diode.

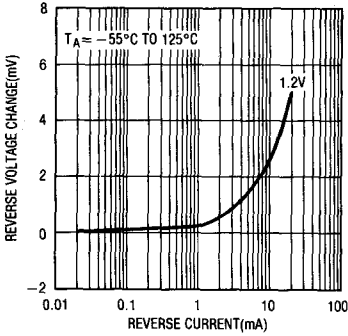
Note 2: This parameter guaranteed by "reverse breakdown change with current" test.

Note 3: For the LT1034C-1.2, $20\mu A \leq I_R \leq 2mA$. For the LT1034C-2.5, $30\mu A \leq I_R \leq 2mA$.

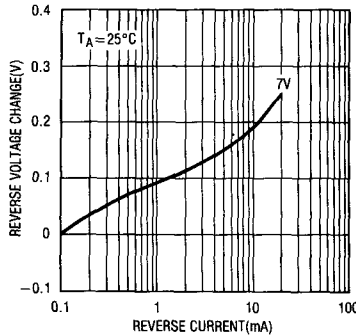
TYPICAL PERFORMANCE CHARACTERISTICS

3

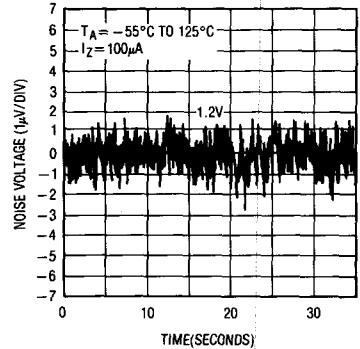
Reverse Voltage Change 1.2V



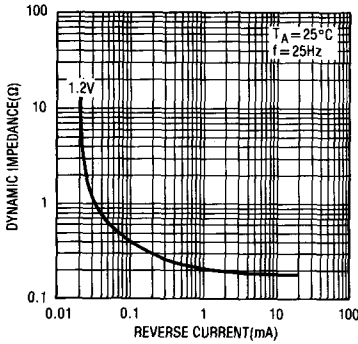
Reverse Voltage Change 7V



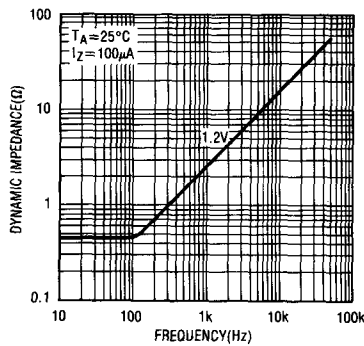
0.1Hz to 10Hz Noise 1.2V



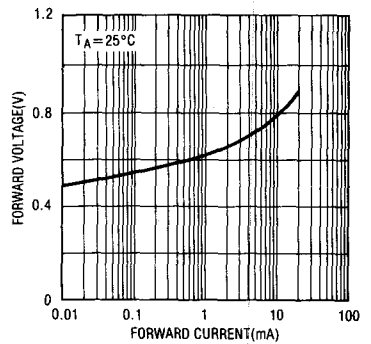
Reverse Dynamic Impedance 1.2V



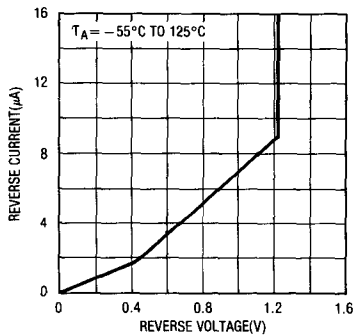
Reverse Dynamic Impedance 7V



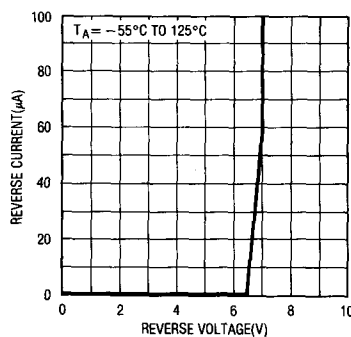
Forward Characteristics



Reverse Characteristics

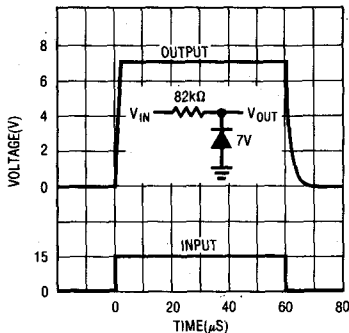


Reverse Characteristics

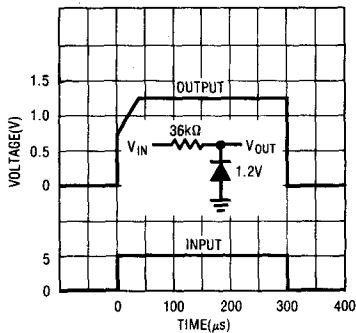


TYPICAL PERFORMANCE CHARACTERISTICS

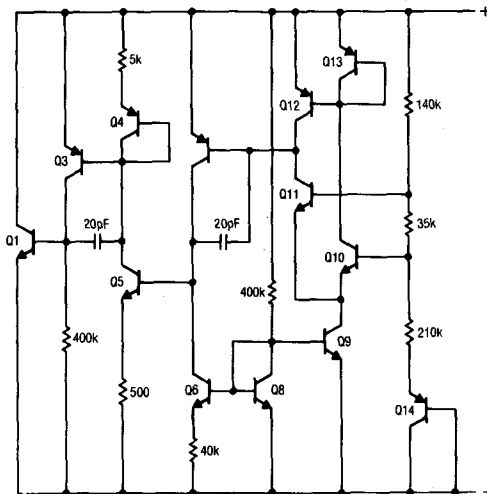
Response Time



Response Time



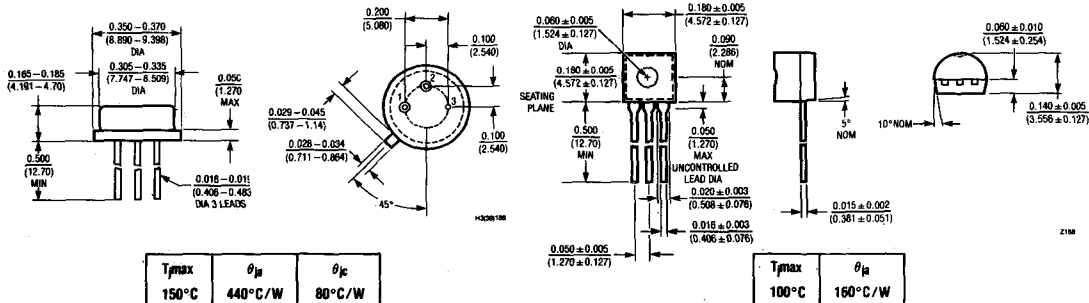
SCHEMATIC DIAGRAM



PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

H Package Metal Can

Z Package Plastic



FEATURES

- Guaranteed 40 ppm/°C Drift
- 20 μ A to 20mA Operation (1.2V)
- 1 Ω Dynamic Impedance
- 7V, 100 μ A Reference

APPLICATIONS

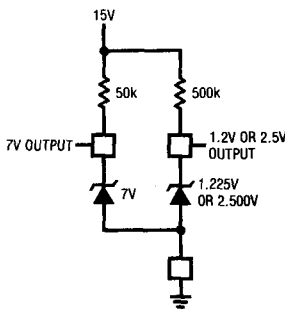
- Portable Meters
- Precision Regulators
- Calibrators

DESCRIPTION

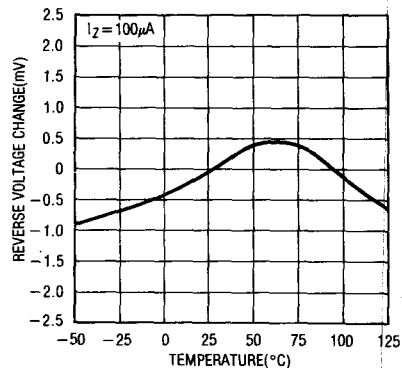
The LT1034 is a micropower, precision 1.2V/2.5V reference combined with a 7V auxiliary reference. The 1.2V/2.5V reference is a trimmed, thin-film, band-gap voltage reference with 1% initial tolerance and guaranteed 20ppm/°C temperature drift. Operating on only 20 μ A, the LT1034 offers guaranteed drift, low temperature cycling hysteresis and good long term stability. The low dynamic impedance makes the LT1034 easy to use from unregulated supplies. The 7V reference is a subsurface zener device for less demanding applications.

The LT1034 reference can be used as a high performance upgrade of the LM385 or LT1001 when a guaranteed temperature drift is desired.

TYPICAL APPLICATIONS



Temperature Drift
 LT1034CS8-1.2



ABSOLUTE MAXIMUM RATINGS

Operating Current 20mA
 Forward Current (Note 1) 20mA
 Operating Temperature Range 0°C to 70°C
 Storage Temperature -65°C to 150°C
 Lead Temperature (Soldering, 10 sec.) 300°C

PACKAGE/ORDER INFORMATION

ORDER PART NUMBER	
LT1034CS8-1.2	LT1034CS8-2.5
PART MARKING	
3401 (1.2V VERSION)	3402 (2.5V VERSION)

ELECTRICAL CHARACTERISTICS

PARAMETER	CONDITIONS		LT1034CS8-1.2			LT1034CS8-2.5			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Reverse Breakdown Voltage	$I_R = 100\mu A$	25°C	1.210	1.225	1.240	2.46	2.5	2.54	V
		●	1.205	1.225	1.245	2.43	2.5	2.57	V
Reverse Breakdown Change with Current	Note 3 $2mA \leq I_R \leq 20mA$	25°C		0.5	2.0	1	3		mV
		●		1.0	4.0	1.5	6		mV
		25°C		4	8.0	6	16		mV
		●		6.0	15.0	10	20		mV
Minimum Operating Current		●		10	20		15	30	μA
Temperature Coefficient	$I_R = 100\mu A$	●		20	40		20	40	ppm/°C
Reverse Dynamic Impedance (Note 2)	$I_R = 100\mu A$	25°C		0.25	1.0		0.5	1.5	Ω
		●		0.50	2.0		1	2.5	Ω
Low Frequency Noise	$I_R = 100\mu A, 0.1Hz \leq F \leq 10Hz$	●		4			6		$\mu Vp-p$
Long Term Stability	$I_R = 100\mu A, T = 25^\circ C$	25°C		20			20		ppm/ \sqrt{khrs}

ELECTRICAL CHARACTERISTICS 7V Reference

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Reverse Breakdown Voltage	$I_R = 100\mu A$	25°C	6.8	7.0	7.3	V
		●	6.75	7.0	7.4	V
Reverse Breakdown Change with Current	$100\mu A \leq I_R \leq 1mA$ $100\mu A \leq I_R \leq 1mA$ $1mA \leq I_R \leq 20mA$ $1mA \leq I_R \leq 20mA$	25°C		90	140	mV
		●		100	190	mV
		25°C		160	250	mV
		●		200	350	mV
Temperature Coefficient	$I_R = 100\mu A$	●		40		ppm/°C
Long Term Stability	$I_R = 100\mu A$	25°C		20		ppm/ \sqrt{khrs}

The ● denotes specifications that apply over the operating temperature range.

Note 1: Forward biasing either diode will affect the operation of the other diode.

Note 2: This parameter guaranteed by "reverse breakdown change with current" test.

Note 3: For the LT1034CS8-1.2, $20\mu A \leq I_R \leq 2mA$. For the LT1034CS8-2.5, $30\mu A \leq I_R \leq 2mA$.

FEATURES

- *Guaranteed* 10 ppm/°C temperature coefficient
- *Guaranteed* 1.0Ω max. dynamic impedance
- *Guaranteed* 20μV max. wideband noise
- Wide operating current range 0.6mA to 15mA

APPLICATIONS

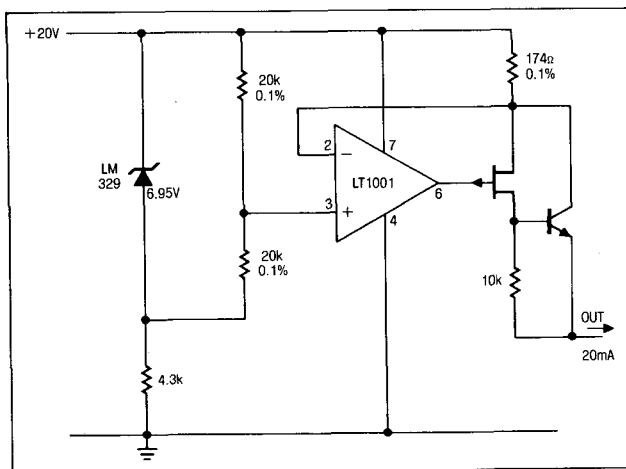
- Transducers
- A/D and D/A Converters
- Calibration Standards
- Instrumentation Reference

DESCRIPTION

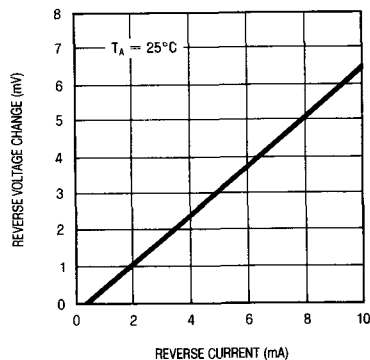
The LM129 temperature compensated 6.9 Volt zener references provide excellent stability over time and temperature, very low dynamic impedance and a wide operating current range. The device achieves low dynamic impedance by incorporating a high gain shunt regulator around the zener. The excellent noise performance of the device is achieved by using a "buried zener" design which eliminates surface noise phenomenon associated with ordinary zeners. To serve a wide variety of applications, the LM129 is available in several temperature coefficient grades and two package styles. A 20mA positive current source application is shown below.

3

20mA Positive Current Source



Reverse Voltage Change

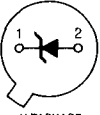
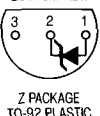


LM129/LM329

ABSOLUTE MAXIMUM RATINGS

Reverse Breakdown Current	30mA
Forward Current	2mA
Operating Temperature Range	
LM129	-55°C to 125°C
LM329	0°C to 70°C
Storage Temperature Range	
LM129	-65°C to 150°C
LM329	-65°C to 150°C
Lead Temperature (Soldering, 10 sec.)	300°C

PACKAGE/ORDER INFORMATION

 <p>BOTTOM VIEW H PACKAGE TO-46 METAL CAN</p>	LM129AH LM329AH
	LM129BH LM329BH
 <p>BOTTOM VIEW Z PACKAGE TO-92 PLASTIC</p>	LM129CH LM329CH
	LM329DH
	LM329AZ
	LM329BZ
	LM329CZ
	LM329DZ

ELECTRICAL CHARACTERISTICS (See Note 1)

SYMBOL	PARAMETER	CONDITIONS	LM129A,B,C			LM329A,B,C,D			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_Z	Reverse Breakdown Voltage	$T_A = 25^\circ\text{C}$ $0.6\text{mA} \leq I_R \leq 15\text{mA}$	6.7	6.9	7.2	6.6	6.9	7.25	V
$\frac{\Delta V_Z}{\Delta I_R}$	Reverse Breakdown Voltage Change with Current	$T_A = 25^\circ\text{C}$ $0.6\text{mA} \leq I_R \leq 15\text{mA}$		9	14		9	20	mV
$\frac{\Delta V_Z}{\Delta I_R}$	Reverse Breakdown Voltage Change with Current	$1\text{mA} \leq I_R \leq 15\text{mA}$	●	12			12		mV
$\frac{\Delta V_Z}{\Delta \text{Temp}}$	Temperature Coefficient	$I_R = 1\text{mA}$	●	6	10		6	10	ppm/°C
		LM129A/LM329A	●	15	20		15	20	ppm/°C
		LM129B/LM329B	●	30	50		30	50	ppm/°C
		LM129C/LM329C	●	50	100		50	100	ppm/°C
	Change in Temperature Coefficient	$1\text{mA} \leq I_R \leq 15\text{mA}$	●	1			1		ppm/°C
r_Z	Dynamic Impedance (Note 2)	$T_A = 25^\circ\text{C}$, $I_R = 1\text{mA}$ ($10\text{Hz} \leq f \leq 100\text{Hz}$)		0.6	1		0.8	2	Ω
r_Z	Dynamic Impedance (Note 2)	$1\text{mA} \leq I_R \leq 15\text{mA}$ ($10\text{Hz} \leq f \leq 100\text{Hz}$)	●	0.8			1		Ω
e_n	RMS Noise	$T_A = 25^\circ\text{C}$, $10\text{Hz} \leq f \leq 10\text{kHz}$		7	20		7	100	μV
$\frac{\Delta V_Z}{\Delta \text{Time}}$	Long Term Stability	$T_A = 45^\circ\text{C} \pm 0.1^\circ\text{C}$ $I_R = 1\text{mA} \pm 0.3\%$		20			20		ppm/khr

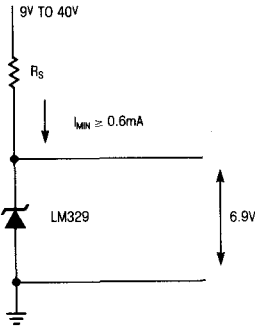
The ● denotes the specifications which apply over full operating temperature range.

Note 1: These specifications apply over the full operating temperature range unless otherwise noted. To determine the junction temperature as a function of the ambient temperature, see θ_{JA} for each package.

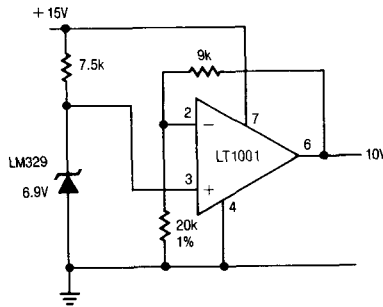
Note 2: Dynamic impedance guaranteed by "Reverse Breakdown Voltage Change with Current".

TYPICAL APPLICATIONS

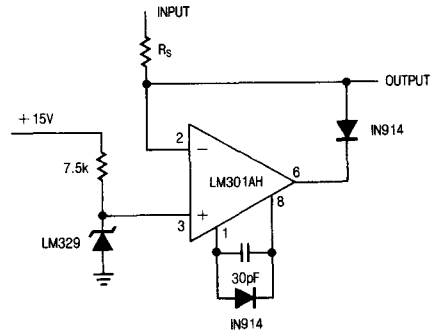
Common Reference



Buffered Reference Using a Single Supply



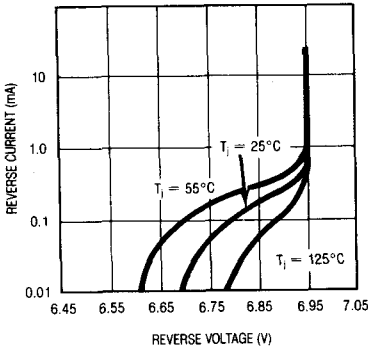
Precision Clamp



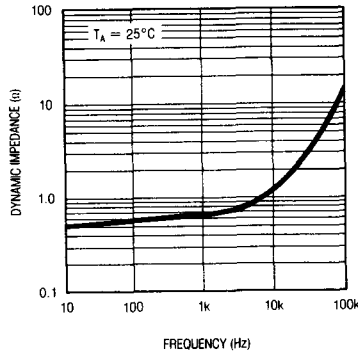
TYPICAL PERFORMANCE CHARACTERISTICS

3

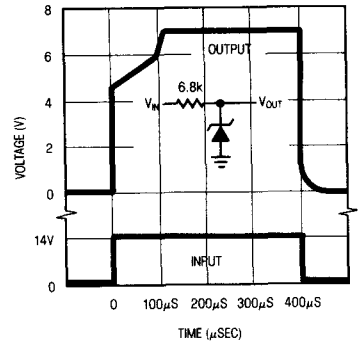
Reverse Characteristics



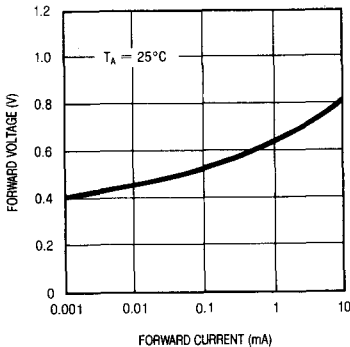
Dynamic Impedance



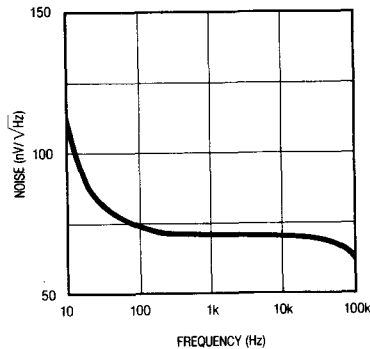
Response Time



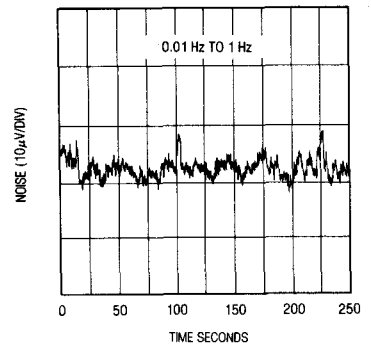
Forward Characteristics



Noise Voltage

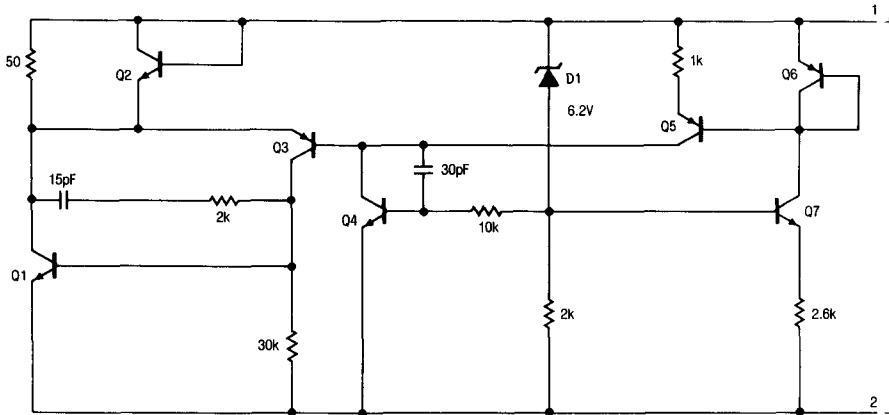


Low Frequency Noise Voltage



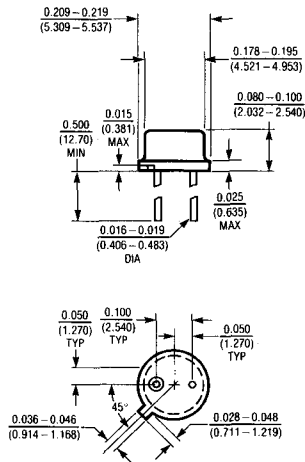
LM129/LM329

SCHEMATIC DIAGRAM



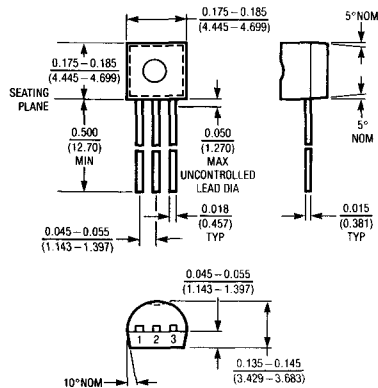
PACKAGE DESCRIPTION

H Package, 2 Lead TO-46 Metal Can



T_{jmax}	θ_{ja}	θ_{jc}
150°C	440°C/W	80°C/W

Z Package, 3 Lead TO-92 Plastic



T_{jmax}	θ_{ja}
100°C	160°C/W

Constant Current Source and Temperature Sensor

FEATURES

- 1 μ A to 10mA Operation
- 0.02%/V Regulation
- 0.8V to 40V Operating Voltage
- Can be Used as Linear Temperature Sensor
- Draws No Reverse Current
- Supplied in Standard Transistor Packages

APPLICATIONS

- Current Mode Temperature Sensing
- Constant Current Source for Shunt References
- Cold Junction Compensation
- Constant-Gain Bias for Bipolar Differential Stage
- Micropower Bias Networks
- Buffer for Photoconductive Cell
- Current Limiter

DESCRIPTION

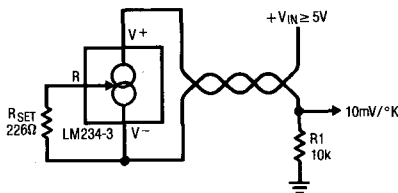
The LM134 is a three-terminal current source designed to operate at current levels from 1 μ A to 10mA, as set by an external resistor. The device operates as a true two-terminal current source, requiring no extra power connections or input signals. Regulation is typically 0.02%/V and terminal-to-terminal voltage can range from 800mV to 40V.

Because the operating current is *directly proportional to absolute temperature* in degrees Kelvin, the device will also find wide applications as a temperature sensor. The temperature dependence of the operating current is +0.336%/°C at room temperature. For example, a device operating at 298 μ A will have a temperature coefficient of +1 μ A/°C. The temperature dependence is extremely accurate and repeatable. Devices specified as temperature sensors in the 100 μ A to 1mA range are the LM134-3, LM234-3 and the LM134-6, LM234-6, with the dash numbers indicating $\pm 3^\circ\text{C}$ and $\pm 6^\circ\text{C}$ accuracies, respectively.

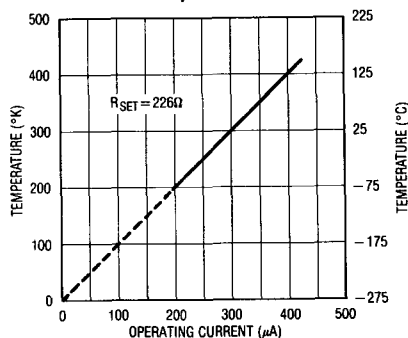
If a zero temperature coefficient current source is required, this is easily achieved by adding a diode and a resistor.

3

**Remote Temperature Sensor
with Voltage Output**



**Operating Current vs
Temperature**

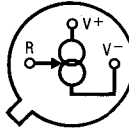
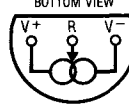


LM134 Series

ABSOLUTE MAXIMUM RATINGS

V^+ to V^- Forward Voltage	
LM134	40V
LM134-3/LM134-6/LM234-3/ LM234-6/LM334	30V
V^+ to V^- Reverse Voltage	20V
R Pin to V^- Voltage	5V
Set Current	10mA
Power Dissipation	200mW
Operating Temperature Range	
LM134/LM134-3/LM134-6	-55°C to 125°C
LM234-3/LM234-6	-25°C to 100°C
LM334	0°C to 70°C
Lead Temperature (Soldering, 10 sec.)	300°C

PACKAGE/ORDER INFORMATION

	ORDER PART NUMBER	
	CURRENT SOURCE	TEMP SENSOR
<p>BOTTOM VIEW</p>  <p>H PACKAGE TO-46 METAL CAN</p>	LM134H LM334H	LM134H-3 LM234H-3 LM134H-6 LM234H-6
<p>BOTTOM VIEW</p>  <p>Z PACKAGE TO-92 PLASTIC</p>	LM334Z	LM234Z-3 LM234Z-6

ELECTRICAL CHARACTERISTICS CURRENT SOURCE (Note 1)

SYMBOL	PARAMETER	CONDITIONS	LM134			LM334			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
ΔI_{SET}	Set Current Error, $V^+ = 2.5V$ (Note 2)	$10\mu A \leq I_{SET} \leq 1mA$			3			6	%
		$1mA < I_{SET} \leq 5mA$			5			8	%
		$2\mu A \leq I_{SET} < 10\mu A$			8			12	%
	Ratio of Set Current to V^- Current	$10\mu A \leq I_{SET} \leq 1mA$ $1mA \leq I_{SET} \leq 5mA$ $2\mu A \leq I_{SET} \leq 10\mu A$	14	18	23	14	18	26	
V_{MIN}	Minimum Operating Voltage	$2\mu A \leq I_{SET} \leq 100\mu A$		0.8			0.8		V
		$100\mu A < I_{SET} \leq 1mA$		0.9			0.9		V
		$1mA < I_{SET} \leq 5mA$		1.0			1.0		V
$\frac{\Delta I_{SET}}{\Delta V_{IN}}$	Average Change in Set Current with Input Voltage	$1.5V \leq V^+ \leq 5V$	0.02	0.05		0.02	0.1		%/V
		$2\mu A \leq I_{SET} \leq 1mA$							
		$5V \leq V^+ \leq V_{MAX}$ (Note 4)	0.01	0.03		0.01	0.05		%/V
		$1.5V \leq V^+ \leq 5V$		0.03			0.03		%/V
	Temperature Dependence of Set Current (Note 3)	$25\mu A \leq I_{SET} \leq 1mA$	0.96T	T	1.04T	0.96T	T	1.04T	
C_S	Effective Shunt Capacitance			15			15		pF

ELECTRICAL CHARACTERISTICS TEMPERATURE SENSOR (Note 1)

SYMBOL	PARAMETER	CONDITIONS	LM134-3, LM234-3			LM134-6, LM234-6			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
ΔI_{SET}	Set Current Error, $V^+ = 2.5V$ (Note 2)	$100\mu A \leq I_{SET} \leq 1mA$ $T_j = 25^\circ C$			± 1			± 2	%
	Equivalent Temperature Error				± 3			± 6	$^\circ C$
	Ratio of Set Current to V^- Current	$100\mu A \leq I_{SET} \leq 1mA$	14	18	26	14	18	26	
V_{MIN}	Minimum Operating Voltage	$100\mu A \leq I_{SET} \leq 1mA$		0.9			0.9		V
$\frac{\Delta I_{SET}}{\Delta V_{IN}}$	Average Change in Set Current with Input Voltage	$1.5V \leq V^+ \leq 5V$ $100\mu A \leq I_{SET} \leq 1mA$ $5V \leq V^+ \leq 30V$		0.02	0.05		0.02	0.1	%/V
	Temperature Dependence of Set Current (Note 3)	$100\mu A \leq I_{SET} \leq 1mA$	0.98T	T	1.02T	0.97T	T	1.03T	
	Equivalent Slope Error			± 2			± 3		%
C_S	Effective Shunt Capacitance			15			15		pF

Note 1: Unless otherwise specified, tests are performed at $T_j = 25^\circ C$ with pulse testing so that junction temperature does not change during test.

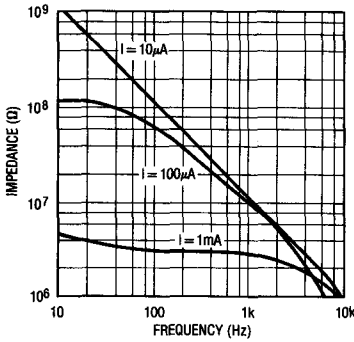
Note 2: Set current is the current flowing into the V^+ pin. It is determined by the following formula: $I_{SET} = 67.7mV/R_{SET}$ (@ $25^\circ C$). Set current error is expressed as a percent deviation from this amount. I_{SET} increases at $0.336\%/^\circ C$ @ $T_j = 25^\circ C$.

Note 3: I_{SET} is directly proportional to absolute temperature ($^\circ K$). I_{SET} at any temperature can be calculated from: $I_{SET} = I_0 (T/T_0)$ where I_0 is I_{SET} measured at T_0 ($^\circ K$).

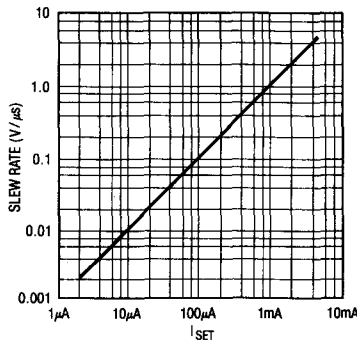
Note 4: $V_{MAX} = 40V$ for LM134 and $30V$ for other grades.

TYPICAL PERFORMANCE CHARACTERISTICS

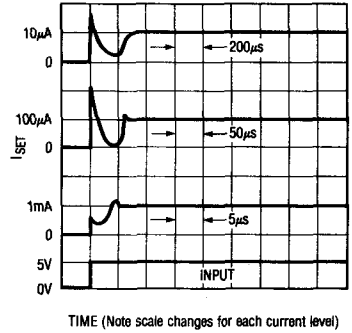
Output Impedance



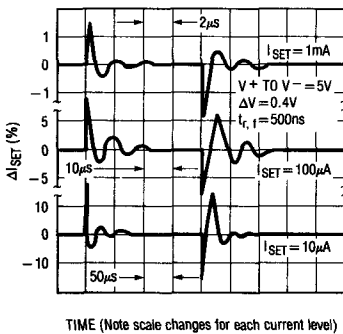
Maximum Slew Rate for Linear Operation



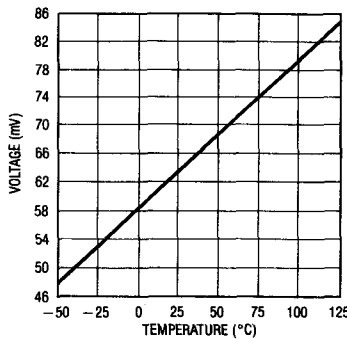
Start-Up



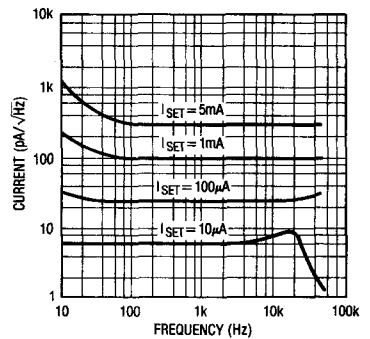
Transient Response



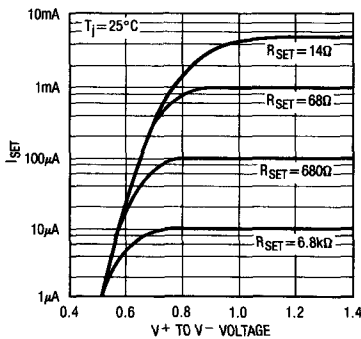
Voltage Across R_SET



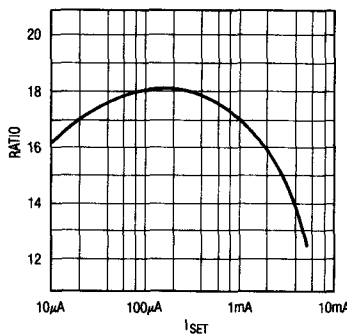
Current Noise



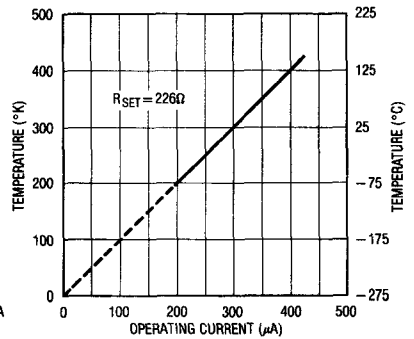
Turn-On Voltage



Ratio of I_SET to V- Current



Operating Current vs Temperature



APPLICATIONS INFORMATION

Basic Theory of Operation

The equivalent circuit of the LM134 is shown in Figure 1. A reference voltage of 64mV is applied to the minus input of A1 with respect to the V^- pin. A1 serves the drive to Q2 to keep the R pin at 64mV, independent of the value of R_{SET} . Transistor Q1 is matched to Q2 at a 17:1 ratio so that the current flowing out of the V^- pin is always 1/18 of the total current into the V^+ pin. This total current is called I_{SET} and is equal to

$$\left(\frac{64\text{mV}}{R_{SET}}\right) \left(\frac{18}{17}\right) = \frac{67.7\text{mV}}{R_{SET}}$$

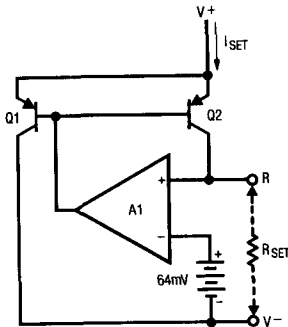


Figure 1

The 67.7mV equivalent reference voltage is directly proportional to absolute temperature in degrees Kelvin (see curve, "Operating Current vs Temperature"). This means that the reference voltage can be plotted as a straight line going from 0mV at absolute zero temperature to 67.7mV at 298°K (25°C). The slope of this line is $67.7\text{mV}/298 = 227\mu\text{V}/^\circ\text{C}$.

The accuracy of the device is specified as a percent error at room temperature, or in the case of the -3 and -6 devices, as both a percent error and an equivalent temperature error. The LM134 operating current changes at a percent rate equal to $(100)(227\mu\text{V}/^\circ\text{C})/(67.7\text{mV}) = 0.336\%/^\circ\text{C}$ at 25°C, so each 1% operating current error is equivalent to $\approx 3^\circ\text{C}$ temperature error when the device is used as a temperature sensor. The slope accuracy (temperature coefficient) of the LM134 is expressed as a

ratio compared to unity. The LM134-3, for instance, is specified at 0.98T to 1.02T, indicating that the maximum slope error of the device is $\pm 2\%$ when the room temperature current is set to the exact desired value.

Supply Voltage Slew Rate

At slew rates above a given threshold (see curve), the LM134 may exhibit non-linear current shifts. The slewing rate at which this occurs is directly proportional to I_{SET} . At $I_{SET} = 10\mu\text{A}$, maximum dv/dt is $0.01\text{V}/\mu\text{s}$; at $I_{SET} = 1\text{mA}$, the limit is $1\text{V}/\mu\text{s}$. Slew rates above the limit do not harm the LM134, or cause large currents to flow.

Thermal Effects

Internal heating can have a significant effect on current regulation for I_{SET} greater than $100\mu\text{A}$. For example, each 1V increase across the LM134 at $I_{SET} = 1\text{mA}$ will increase junction temperature by $\approx 0.4^\circ\text{C}$ in still air. Output current (I_{SET}) has a temperature coefficient of $\approx 0.33\%/^\circ\text{C}$, so the change in current due to temperature rise will be $(0.4)(0.33) = 0.132\%$. This is a 10:1 degradation in regulation compared to true electrical effects. Thermal effects, therefore, must be taken into account when DC regulation is critical and I_{SET} exceeds $100\mu\text{A}$. Heat sinking of the TO-46 package or the TO-92 leads can reduce this effect by more than 3:1.

Shunt Capacitance

In certain applications, the 15pF shunt capacitance of the LM134 may have to be reduced, either because of loading problems or because it limits the AC output impedance of the current source. This can be easily accomplished by buffering the LM134 with an FET, as shown in the applications. This can reduce capacitance to less than 3pF and improve regulation by at least an order of magnitude. DC characteristics (with the exception of minimum input voltage) are not affected.

APPLICATIONS INFORMATION

Noise

Current noise generated by the LM134 is approximately 4 times the shot noise of a transistor. If the LM134 is used as an active load for a transistor amplifier, input referred noise will be increased by about 12dB. In many cases, this is acceptable and a single stage amplifier can be built with a voltage gain exceeding 2000.

Lead Resistance

The sense voltage which determines the operating current of the LM134 is less than 100mV. At this level, thermocouple or lead resistance effects should be minimized by locating the current setting resistor physically close to the device. Sockets should be avoided if possible. It takes only 0.7 Ω contact resistance to reduce output current by 1% at the 1mA level.

Start-Up Time

The LM134 is designed to operate at currents as low as 1 μ A. This requires that internal biasing current be well below that level because the device achieves its wide operating current range by using part of the operating current as bias current for the internal circuitry. To ensure start-up, however, a fixed trickle current must be provided internally. This is typically in the range of 20nA–200nA and is provided by the special ultra-low I_{DSS} FETs shown in the Schematic Diagram as Q7 and Q8. The start-up time of the LM134 is determined by the I_{DSS} of these FETs and the capacitor C1. This capacitor must charge to approximately 500mV before Q3 turns on to start normal circuit operation. This takes as long as (500mV) (50pF)/(20nA) = 1.25ms for very low I_{DSS} values.

Using the LM134 as a Temperature Sensor

Because it has a highly linear output characteristic, the LM134 makes a good temperature sensor. It is particularly useful in remote sensing applications because it is a current output device and is therefore not affected by long wire runs. It is easy to calibrate, has good long term stability, and can be interfaced directly with most data acquisition systems, eliminating the expensive preamplifiers required for thermocouples and platinum sensors.

A typical temperature sensor application is shown in Figure 2. The LM134 operating current at 25°C is set at 298 μ A by the 226 Ω resistor, giving an output of 1 μ A/°K. The current flows through the twisted pair sensor leads to the 10k Ω termination resistor, which converts the current output to a voltage of 10mV/°K referred to ground. The voltage across the 10k Ω resistor will be 2.98V at 25°C, with a slope of 10mV/°C. The simplest way to convert this signal to a Centigrade scale is to subtract a constant 2.73V in software. Alternately, a hardware conversion can be used, as shown in Figure 3, using an LT1009 as a level shifter to offset the output to a Centigrade scale.

The resistor (R_{SET}) used to set the operating current of the LM134 in temperature sensing applications should have low temperature coefficient and good long term stability.

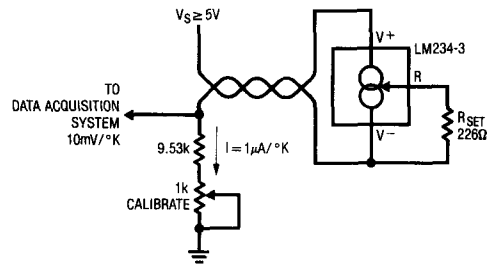


Figure 2. Kelvin Temperature Sensor

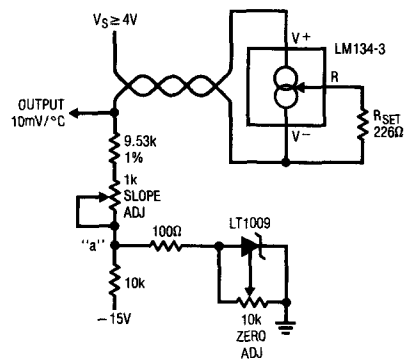


Figure 3. Centigrade Temperature Sensor

APPLICATIONS INFORMATION

30ppm/°C drift in the resistor will change the slope of the temperature sensor by 1%, assuming that the resistor is at the same temperature as the sensor, which is usually the case since the resistor should be located physically close to the LM134 to prevent errors due to wire resistance. A long term shift of 0.3% in the resistor will create a 1°C temperature error. The long term drift of the LM134 is typically much better than this, so stable resistors must be used for best long term performance.

Calibration of the LM134 as a temperature sensor is extremely easy. Referring to Figure 2, calibration is achieved by trimming the termination resistor. *This theoretically trims both zero and slope simultaneously for Centigrade and Fahrenheit applications.* The initial errors in the LM134 are directly proportional to absolute temperature, just like the actual output. This allows the sensor to be trimmed at any temperature and have the slope error be corrected at the same time. Residual slope error is typically less than 1% after this single trim is completed.

The two trims shown in Figure 3 are still intended to be a "one point" temperature calibration, where the zero and the slope are trimmed at a single temperature. The LT1009 reference is adjusted to give 2.700V at node "a" at $T_{\text{SENSOR}} = 25^{\circ}\text{C}$. The 1k trimmer then adjusts the output for 0.25V, completing the calibration. If the calibration is to be done at a temperature other than 25°C, trim the LT1009 for $2.7025 - (1\mu\text{A})[T_{\text{SENSOR}} (^{\circ}\text{C})](100\Omega)$ at node "a", then adjust the 1k trimmer for proper output.

If higher accuracy is required, a two point calibration technique can be used. In Figure 4, separate zero and slope trims are provided. Residual non-linearity is now the limitation on accuracy. Non-linearity of the LM134 in a 100°C span is typically less than 0.5°C. This particular method of trimming has the advantage that the slope trim does not interact with the zero trim. Trim procedure is to adjust for zero output with $T_{\text{SENSOR}} = 0^{\circ}\text{C}$, then trim slope for proper output at some convenient second temperature. No further trimming is required.

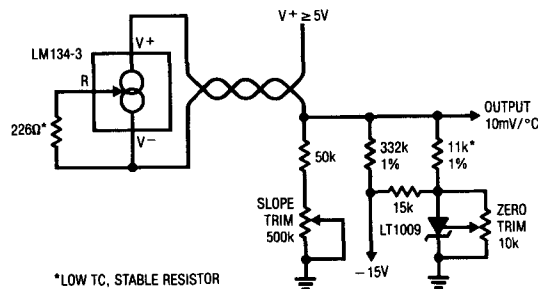
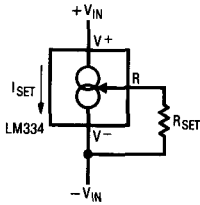


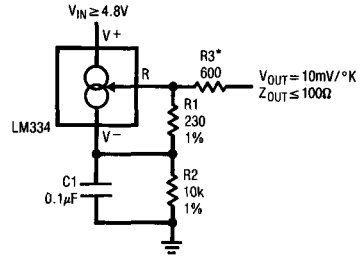
Figure 4. Centigrade Temperature Sensor with 2 Point Trim

TYPICAL APPLICATIONS

Basic 2-Terminal Current Source



Low Output Impedance Thermometer (Kelvin Output)

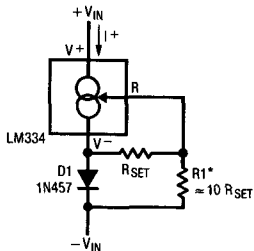


*OUTPUT IMPEDANCE OF THE LM134 AT THE "R" PIN IS

APPROXIMATELY $-\frac{R_0}{16}$ Ω , WHERE R_0 IS THE EQUIVALENT

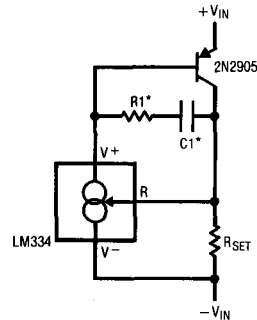
EXTERNAL RESISTANCE CONNECTED TO THE V- PIN. THIS NEGATIVE RESISTANCE CAN BE REDUCED BY A FACTOR OF 5 OR MORE BY INSERTING AN EQUIVALENT RESISTOR IN SERIES WITH THE OUTPUT.

Zero Temperature Coefficient Current Source



*SELECT RATIO OF R_1 TO R_{SET} TO OBTAIN ZERO DRIFT. $I^+ \approx 2 I_{SET}$.

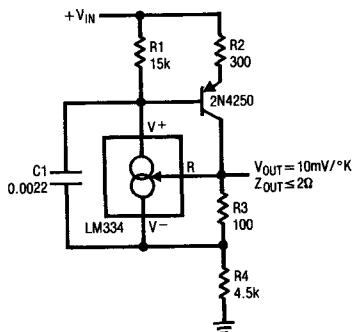
Higher Output Current



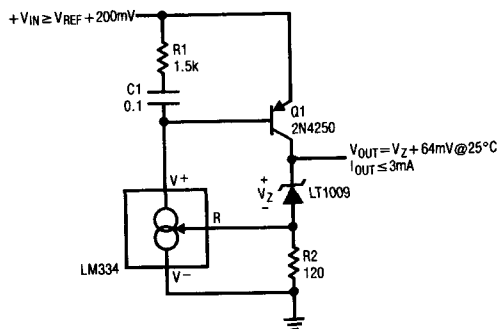
*SELECT R_1 AND C_1 FOR OPTIMUM STABILITY

TYPICAL APPLICATIONS

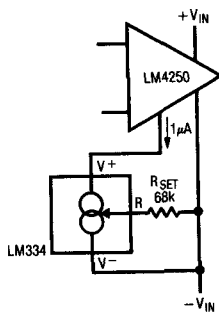
Low Output Impedance Thermometer



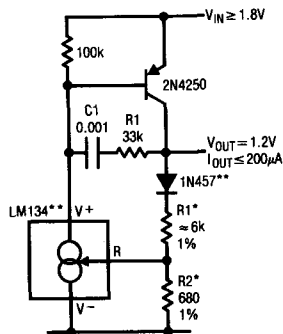
Low Input Voltage Reference Driver



Micropower Bias

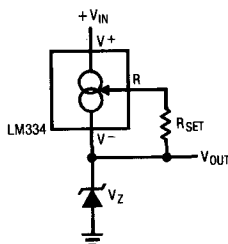


1.2V Regulator with 1.8V Minimum Input



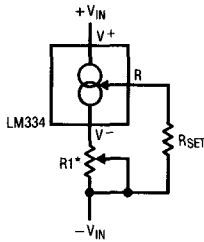
*SELECT RATIO OF R1 TO R2 FOR ZERO TEMPERATURE DRIFT
**LM134 AND DIODE SHOULD BE ISOTHERMAL

Zener Biasing



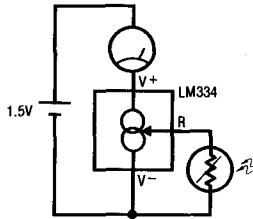
TYPICAL APPLICATIONS

Alternate Trimming Technique

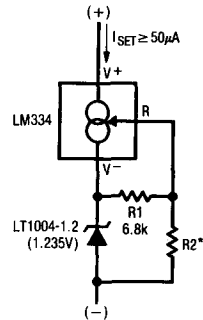


*FOR $\pm 10\%$ ADJUSTMENT, SELECT R_{SET}
10% HIGH AND MAKE $R_1 = 3R_{SET}$

Buffer for Photoconductive Cell

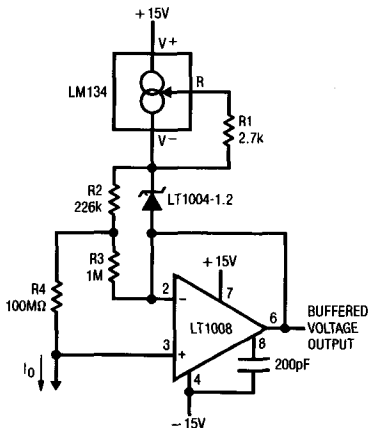


High Precision Low TC Current Source



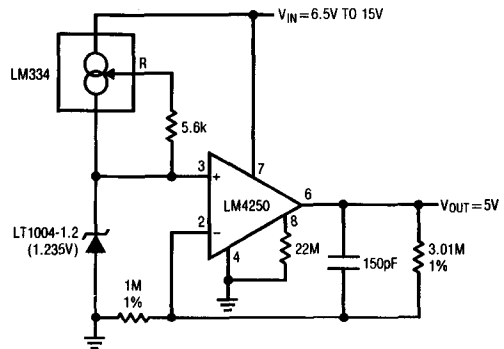
* $I_{SET} = \frac{1.37V}{R_2} + 10\mu A$
 $I_{SET} TC = 0.016\%/^{\circ}C + 33nA/^{\circ}C$
REGULATION = 0.001%/V

Precision 10nA Current Source



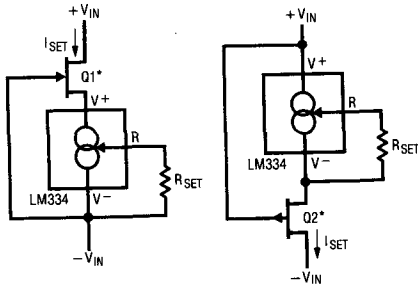
$I_0 = 10nA$
 $Z_0 \approx 10^{12}\Omega$
COMPLIANCE = -14V TO +12.5V

Micropower 5V Reference



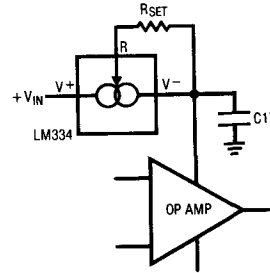
TYPICAL APPLICATIONS

FET Cascoding for Low Capacitance and/or Ultra High Output Impedance



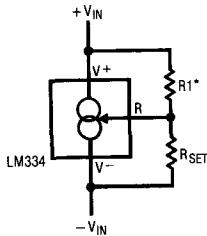
*SELECT Q1 OR Q2 TO ENSURE AT LEAST 1V ACROSS THE LM134. $V_p(1 - I_{SET}/I_{DSS}) \geq 1.2V$.

In-Line Current Limiter



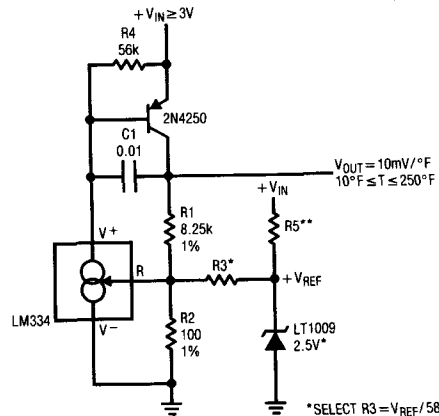
*USE MINIMUM VALUE REQUIRED TO ENSURE STABILITY OF PROTECTED DEVICE. THIS MINIMIZES INRUSH CURRENT TO A DIRECT SHORT.

Generating Negative Output Impedance



* $Z_{OUT} = -16 \cdot R1 (R1/V_{IN})$ MUST NOT EXCEED I_{SET} .

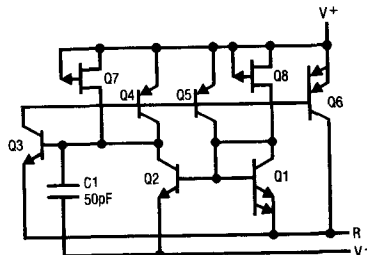
Ground Referred Fahrenheit Thermometer



*SELECT $R3 = V_{REF} / 583\mu A$.
**SELECT FOR 1.2mA

3

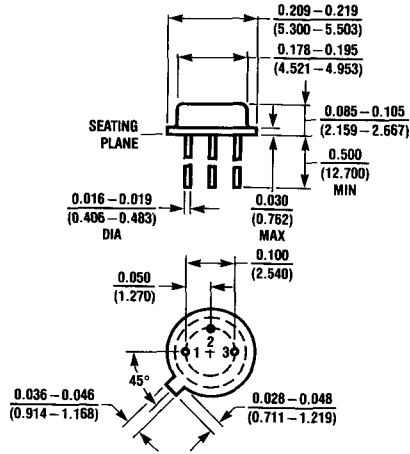
SCHEMATIC DIAGRAM



LM134 Series

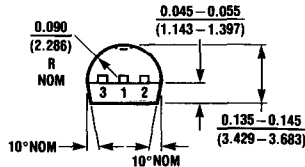
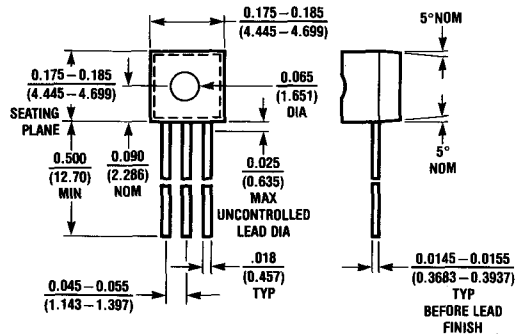
PACKAGE DESCRIPTION

H Package Metal Can



T_{max}	θ_{ja}	θ_{jc}
150°C	440°C/W	80°C/W

Z Package Plastic



T_{max}	θ_{ja}
100°C	160°C/W

FEATURES

- 1 μ A to 10mA Operation
- 0.02%/V Regulation
- 0.8V to 30V Operating Voltage
- Can Be Used as Linear Temperature Sensor
- Draws No Reverse Current

APPLICATIONS

- Current Mode Temperature Sensing
- Constant Current Source for Shunt References
- Cold Junction Compensation
- Constant-Gain Bias for Bipolar Differential Stage
- Micropower Bias Networks
- Buffer for Photoconductive Cell
- Current Limiter

DESCRIPTION

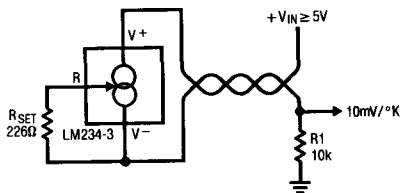
The LM334 is a three-terminal current source designed to operate at current levels from 1 μ A to 10mA, as set by an external resistor. The device operates as a true two-terminal current source, requiring no extra power connections or input signals. Regulation is typically 0.02%/V and terminal-to-terminal voltage can range from 800mV to 30V.

Because the operating current is *directly proportional to absolute temperature* in degrees Kelvin, the device will also find wide applications as a temperature sensor. The temperature dependence of the operating current is +0.336%/ $^{\circ}$ C at room temperature. For example, a device operating at 298 μ A will have a temperature coefficient of +1 μ A/ $^{\circ}$ C. The temperature dependence is extremely accurate and repeatable.

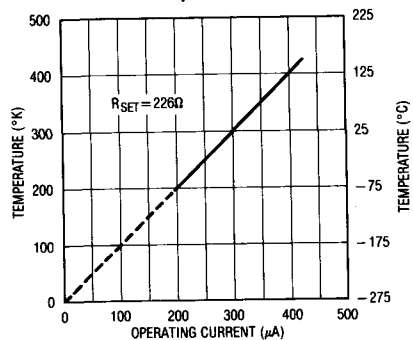
If a zero temperature coefficient current source is required, this is easily achieved by adding a diode and a resistor.

3

**Remote Temperature Sensor
with Voltage Output**



**Operating Current vs
Temperature**



LM334S8

ABSOLUTE MAXIMUM RATINGS

V ⁺ to V ⁻ Forward Voltage	30V
V ⁺ to V ⁻ Reverse Voltage	20V
R Pin to V ⁻ Voltage	5V
Set Current	10mA
Power Dissipation	200mW
Operating Temperature Range	0°C to 70°C
Lead Temperature (Soldering, 10 sec.)	300°C

PACKAGE/ORDER INFORMATION

	ORDER PART NUMBER
	LM334S8
	PART MARKING
	334

ELECTRICAL CHARACTERISTICS CURRENT SOURCE (Note 1)

SYMBOL	PARAMETER	CONDITIONS	LM334		UNITS	
			MIN	TYP		MAX
ΔI_{SET}	Set Current Error, V ⁺ = 2.5V (Note 2)	$10\mu A \leq I_{SET} \leq 1mA$			6	%
		$1mA < I_{SET} \leq 5mA$			8	%
		$2\mu A \leq I_{SET} < 10\mu A$			12	%
	Ratio of Set Current to V ⁻ Current	$10\mu A \leq I_{SET} \leq 1mA$ $1mA \leq I_{SET} \leq 5mA$ $2\mu A \leq I_{SET} \leq 10\mu A$	14	18 14 18	26 26	
V _{MIN}	Minimum Operating Voltage	$2\mu A \leq I_{SET} \leq 100\mu A$		0.8		V
		$100\mu A < I_{SET} \leq 1mA$		0.9		V
		$1mA < I_{SET} \leq 5mA$		1.0		V
$\frac{\Delta I_{SET}}{\Delta V_{IN}}$	Average Change in Set Current with Input Voltage	$1.5V \leq V^+ \leq 5V$		0.02	0.1	%/V
		$2\mu A \leq I_{SET} \leq 1mA$				
		$5V \leq V^+ \leq 30V$		0.01	0.05	%/V
		$1.5V \leq V \leq 5V$		0.03		%/V
		$1mA < I_{SET} \leq 5mA$				
		$5V \leq V \leq 30V$		0.02		%/V
	Temperature Dependence of Set Current (Note 3)	$25\mu A \leq I_{SET} \leq 1mA$	0.96T	T	1.04T	
C _S	Effective Shunt Capacitance			15		pF

Note 1: Unless otherwise specified, tests are performed at T_j = 25°C with pulse testing so that junction temperature does not change during test.

Note 2: Set current is the current flowing into the V⁺ pin. It is determined by the following formula: I_{SET} = 67.7mV/R_{SET} (@25°C). Set current error is expressed as a percent deviation from this amount. I_{SET} increases at 0.336%/°C @ T_j = 25°C.

Note 3: I_{SET} is directly proportional to absolute temperature (°K). I_{SET} at any temperature can be calculated from: I_{SET} = I₀(T/T₀) where I₀ is I_{SET} measured at T₀ (°K).

FEATURES

- *Guaranteed* Temperature Stability
- Maximum 0.6Ω Dynamic Impedance
- Adjustable for Minimum Temperature Coefficient
- Wide Operating Current Range

APPLICATIONS

- Reference for 5V Systems
- 8 Bit A/D and D/A Reference
- Digital Voltmeters
- Current Loop Measurement and Control Systems
- Power Supply Monitor

DESCRIPTION

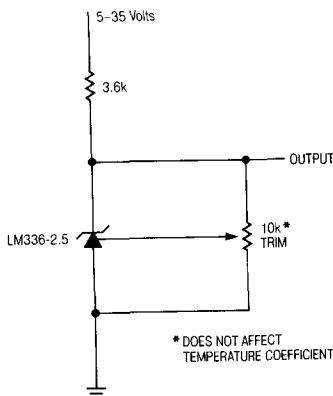
The LM136-2.5 is a general purpose shunt regulator diode designed to operate over a wide current range while maintaining good stability with time and temperature. The third terminal allows either the temperature coefficient to be minimized or the reference voltage to be adjusted without changing the temperature coefficient. Because it operates as a shunt regulator it can be used equally well as a positive or negative reference.

The LM136-2.5 is available with initial tolerances as low as 1% in either a TO-46 metal can for hermetic requirements or a low cost TO-92 plastic package.

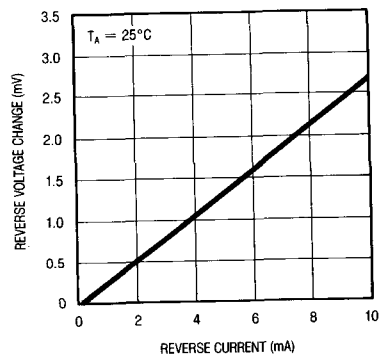
Linear's advanced design, test and process techniques have optimized the LM136-2.5 to achieve superior performance and reliability over previous designs. For more demanding precision reference applications requiring very low initial tolerance and temperature coefficients, consult the LT1009 data sheet. A typical 2.5 Volt reference with trim is shown below.

3

2.5 Volt Reference



Reverse Voltage Change



LM136-2.5/LM336-2.5

ABSOLUTE MAXIMUM RATINGS

Reverse Current	15mA
Forward Current	10mA
Operating Temperature Range	
LM136-2.5	-55°C to 125°C
LM336-2.5	0°C to 70°C
Storage Temperature Range	
LM136-2.5	-65°C to 150°C
LM336-2.5	-65°C to 150°C
Lead Temperature (Soldering, 10 sec.)	300°C

PACKAGE/ORDER INFORMATION

<p>BOTTOM VIEW H PACKAGE TO-46 METAL CAN</p>	<p>LM136H-2.5 LM136AH-2.5 LM336H-2.5 LM336BH-2.5 *SEE NOTE 1</p>
<p>BOTTOM VIEW Z PACKAGE TO-92 PLASTIC</p>	<p>LM336Z-2.5 LM336BZ-2.5 *SEE NOTE 1</p>

ELECTRICAL CHARACTERISTICS (See Note 1)

SYMBOL	PARAMETER	CONDITIONS	LM136A/LM136			LM336B/LM336			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_Z	Reverse Breakdown Voltage	$T_A = 25^\circ\text{C}$, $I_R = 1\text{mA}$ LM136/LM336 LM136A/LM336B	2.440	2.490	2.540	2.390	2.490	2.590	V
$\frac{\Delta V_Z}{\Delta I_R}$	Reverse Breakdown Change with Current	$400\mu\text{A} \leq I_R \leq 10\text{mA}$ $T_A = 25^\circ\text{C}$ $T_{\min} \leq T_A \leq T_{\max}$	●	2.6	6	2.6	10		mV
r_z	Reverse Dynamic Impedance	$I_R = 1\text{mA}$ $T_A = 25^\circ\text{C}$ $T_{\min} \leq T_A \leq T_{\max}$	●	3	10	3	12		mV
$\frac{\Delta V_Z}{\Delta \text{Temp}}$	Temperature Stability	V_R adjusted to 2.490V, $I_R = 1\text{mA}$ $T_{\min} \leq T_A \leq T_{\max}$ LM136A/LM136 LM336B/LM336 (See Figure 1.)	●	12	18	●	1.8	6	mV
$\frac{\Delta V_Z}{\Delta \text{Time}}$	Long Term Stability	$T_A = 25^\circ\text{C} \pm 0.1^\circ\text{C}$, $I_R = 1\text{mA}$		20			20		ppm/kHr

The ● denotes the specifications which apply over full operating temperature range.

Note 1: The LT1009 is an improved, low cost, pin for pin replacement for the "A" and "B" versions. For further information consult the LT1009 data sheet.

Adjusting the LM336 for minimum temperature coefficient

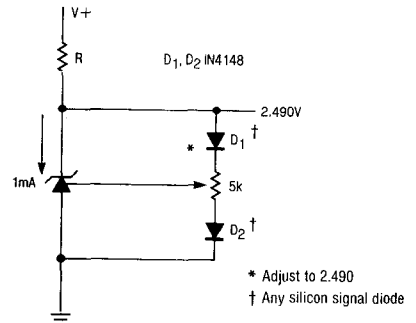
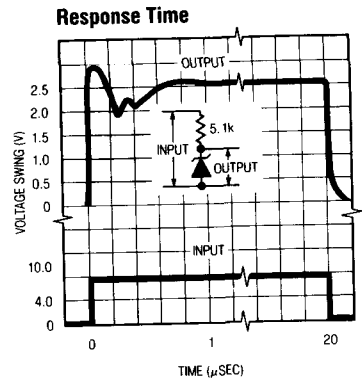
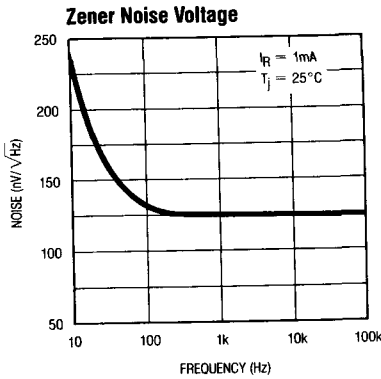
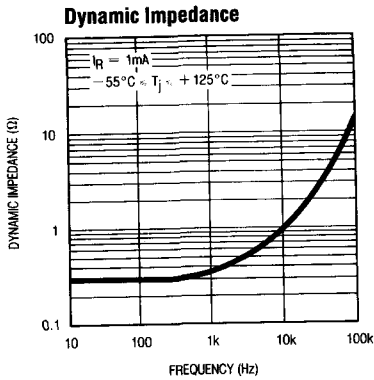
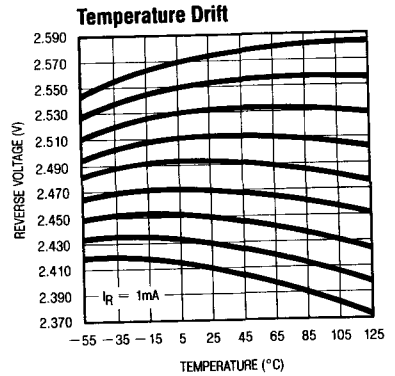
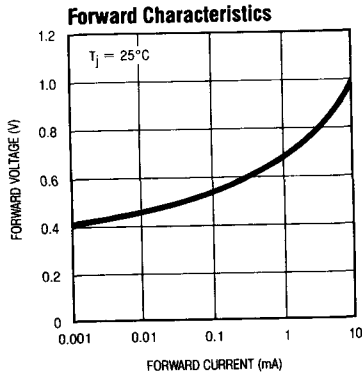
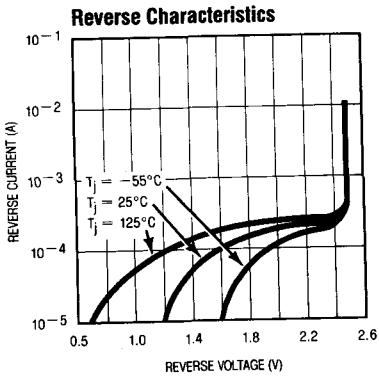


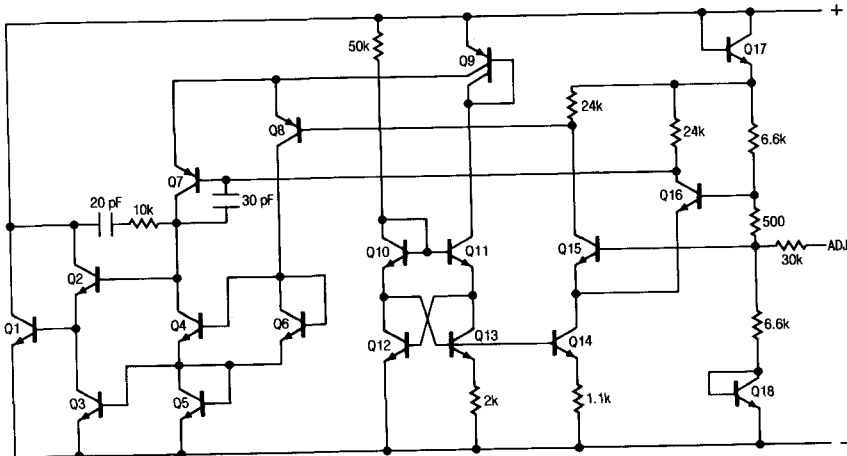
Figure 1

TYPICAL PERFORMANCE CHARACTERISTICS



3

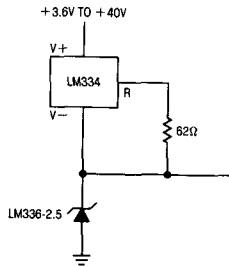
SCHEMATIC DIAGRAM



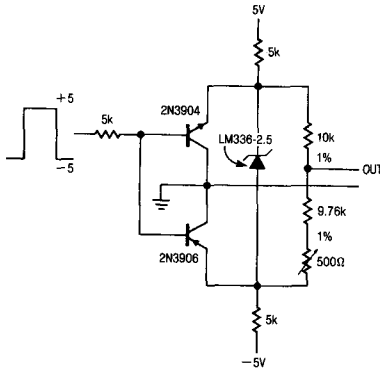
LM136-2.5/LM336-2.5

TYPICAL APPLICATIONS

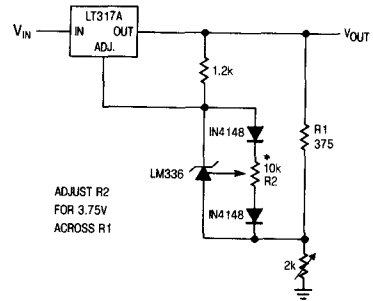
Wide Supply Range, Reference



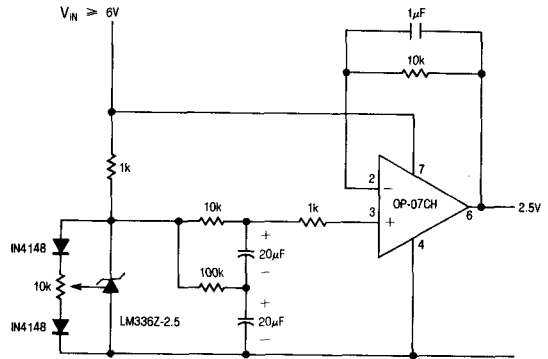
Switchable $\pm 1.25V$ Bipolar Reference



Low Temperature Coefficient Power Regulator

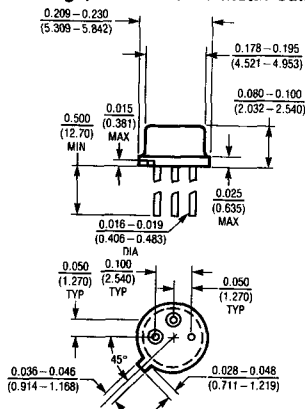


Low Noise 2.5V Buffered Reference



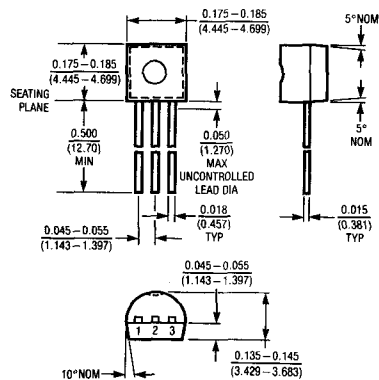
PACKAGE DESCRIPTION

H Package, 3 Lead TO-46 Metal Can



T_{max}	θ_{ja}	θ_{jc}
150°C	440°C/W	80°C/W

Z Package, 3 Lead TO-92 Plastic



T_{max}	θ_{ja}
100°C	160°C/W

FEATURES

- 10 μ A to 20mA operating range
- *Guaranteed* 1% initial voltage tolerance
- *Guaranteed* 1 Ω dynamic impedance
- Very low power consumption

APPLICATIONS

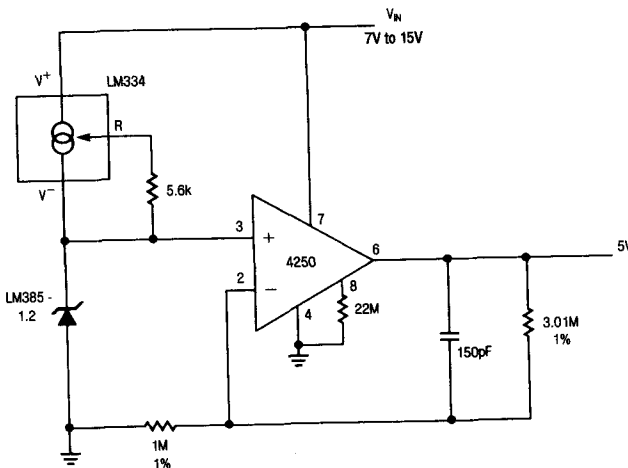
- Portable meter references
- Portable test instruments
- Battery operated systems
- Current loop instrumentation

DESCRIPTION

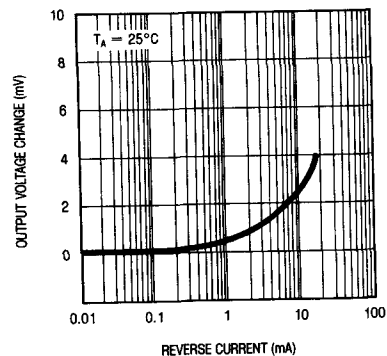
The LM185-1.2 is a two terminal band gap reference diode that has been designed for applications which require precision performance with micropower operation. The device provides guaranteed operating specifications at currents as low as 10 μ A. The nominal voltage is 1.235V with both 1% and 2% tolerances available. Some additional features are: maximum dynamic impedance of 1 Ω , low noise and excellent stability over time and temperature. Advanced design, processing and testing techniques make Linear's LM185-1.2 a superior choice over previous designs. A micro-power 5V reference application is shown below. For guaranteed TC, micropower references, see the LT1034 data sheet.

3

Micro-power 5V Reference



**Reverse Voltage Change
with Current**

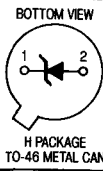
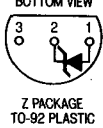


LM185-1.2/LM385-1.2

ABSOLUTE MAXIMUM RATINGS

Reverse Breakdown Current	30mA
Forward Current	10mA
Operating Temperature Range	
LM185-1.2	-55°C to 125°C
LM385-1.2	0°C to 70°C
Storage Temperature Range	
LM185-1.2	-65°C to 150°C
LM385-1.2	-65°C to 150°C
Lead Temperature (Soldering, 10 sec.)	300°C

PACKAGE/ORDER INFORMATION

 BOTTOM VIEW H PACKAGE TO-46 METAL CAN	ORDER PART NUMBER	
		LM185H-1.2
	LM385BH-1.2	(NOTE 3)
 BOTTOM VIEW Z PACKAGE TO-92 PLASTIC	LM385Z-1.2	LM385BZ-1.2
		(NOTE 3)

ELECTRICAL CHARACTERISTICS (See Note 1)

SYMBOL	PARAMETER	CONDITIONS	LM185-1.2			LM385-1.2/385B-1.2			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_Z	Reverse Breakdown Voltage	$T_A = 25^\circ\text{C}$, $I_{\min} \leq I_R \leq 20\text{mA}$ LM185-1.2 LM385-1.2 LM385B-1.2 (Note 3)	1.223	1.235	1.247	1.205	1.235	1.260	V
$\frac{\Delta V_Z}{\Delta \text{Temp}}$	Average Temperature Coefficient	$I_{\min} \leq I_R \leq 20\text{mA}$ (Note 2 and Note 3)	20			20			ppm/°C
I_{\min}	Minimum Operating Current	$T_{\min} \leq T_A \leq T_{\max}$	●	8	10	8	15		μA
$\frac{\Delta V_Z}{\Delta I_R}$	Reverse Breakdown Voltage Change with Current	$I_{\min} \leq I_R \leq 1\text{mA}$ $T_A = 25^\circ\text{C}$ $T_{\min} \leq T_A \leq T_{\max}$	●	1		1			mV
				1.5		1.5			mV
		$1\text{mA} \leq I_R \leq 20\text{mA}$ $T_A = 25^\circ\text{C}$ $T_{\min} \leq T_A \leq T_{\max}$	●	10		20			mV
			●	20		25			mV
r_z	Reverse Dynamic Impedance	$I_R = 100\mu\text{A}$ $T_A = 25^\circ\text{C}$ $T_{\min} \leq T_A \leq T_{\max}$	●	0.2	0.6	0.4	1		Ω
e_n	Wide Band Noise (RMS)	$I_R = 100\mu\text{A}$ $10\text{Hz} \leq f \leq 10\text{kHz}$		60		60			μV
$\frac{\Delta V_Z}{\Delta \text{Time}}$	Long Term Stability	$I_R = 100\mu\text{A}$ $T_A = 25^\circ\text{C} \pm 0.1^\circ\text{C}$		20		20			ppm/kHr

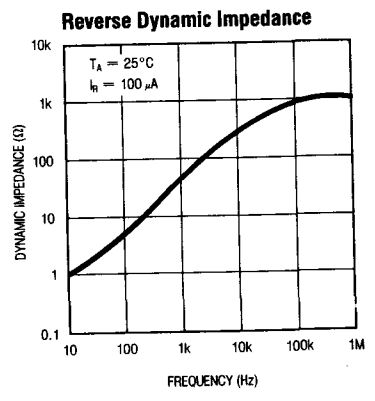
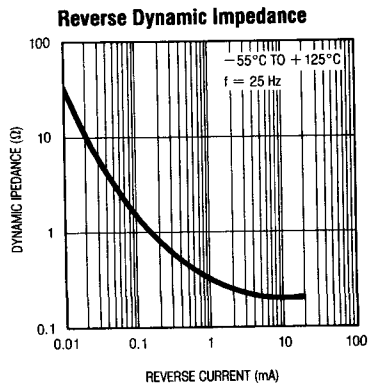
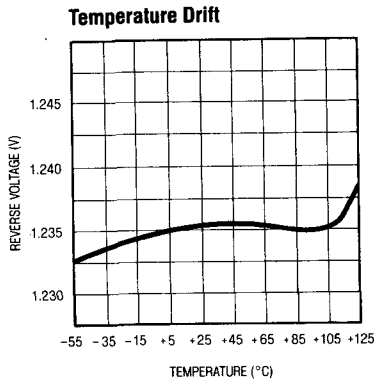
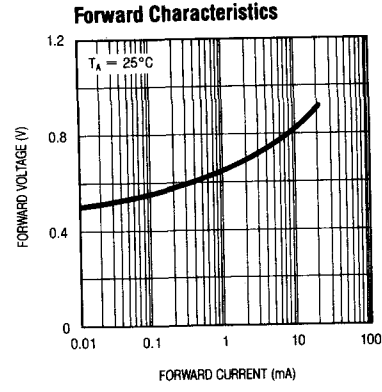
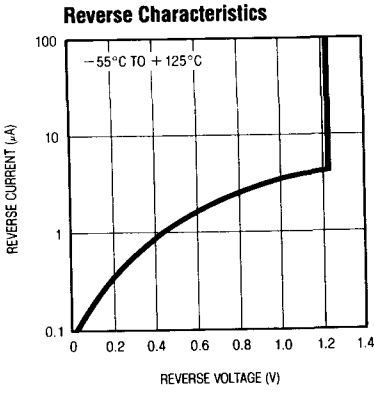
The ● denotes the specifications which apply over full operating temperature range.

Note 1: All specifications are for $T_A = 25^\circ\text{C}$ unless otherwise noted. For the LM185-1.2 $T_{\min} = -55^\circ\text{C}$ and $T_{\max} = +125^\circ\text{C}$. For LM385-1.2 $T_{\min} = 0^\circ\text{C}$ and $T_{\max} = +70^\circ\text{C}$.

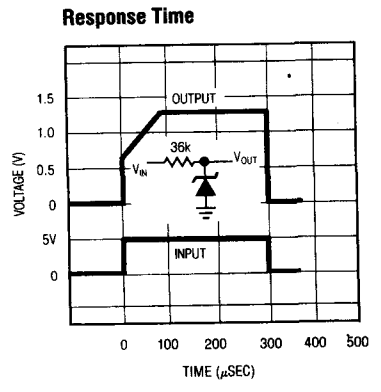
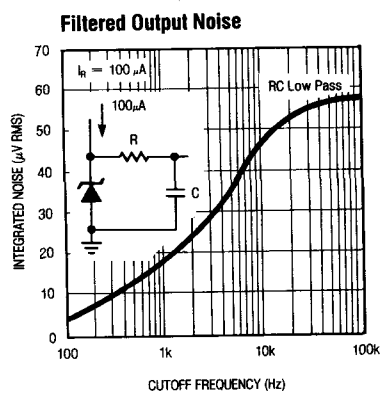
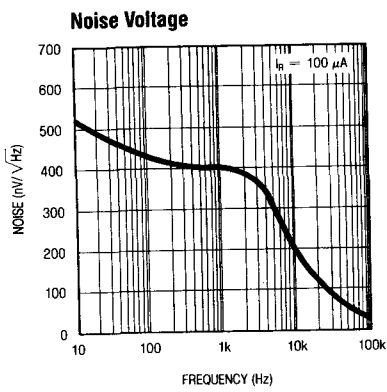
Note 2: Selected devices with guaranteed maximum temperature coefficient are available upon request.

Note 3: For applications requiring low initial tolerance guaranteed over temperature consult LT1004 data sheet. The LT1004 is a low cost pin for pin substitution device.

TYPICAL PERFORMANCE CHARACTERISTICS



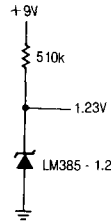
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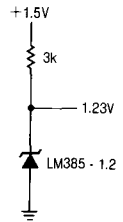
LM185-1.2/LM385-1.2

TYPICAL APPLICATIONS

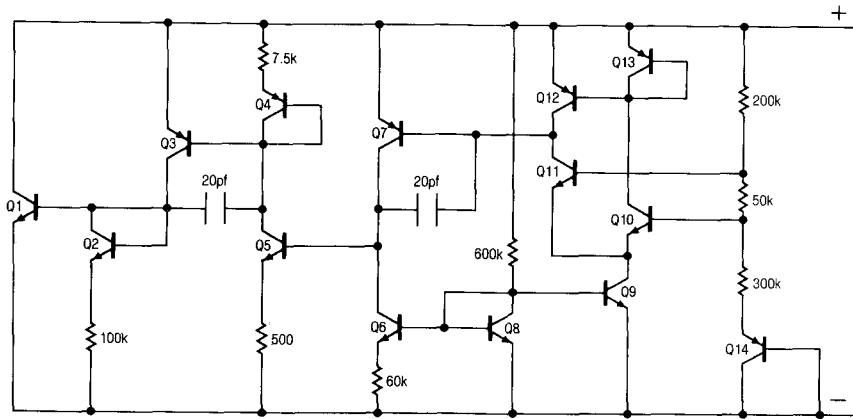
Micropower Reference for 9V Battery



1.2V Reference from 1.5V Battery

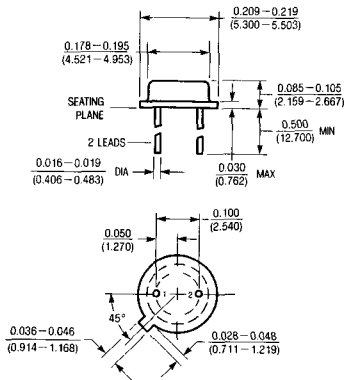


SCHEMATIC DIAGRAM



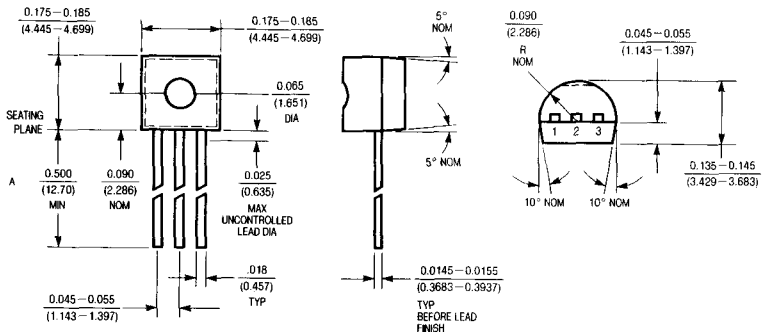
PACKAGE DESCRIPTION

H Package, 2 Lead TO-46 Metal Can



T_{max}	θ_{ja}	θ_{jc}
150°C	440°C/W	80°C/W

Z Package, 3 Lead TO-92 Plastic



T_{max}	θ_{ja}
150°C	160°C/W

FEATURES

- 20 μ A to 20mA operating range
- *Guaranteed* 1% initial voltage tolerance
- *Guaranteed* 1 Ω dynamic impedance
- Very low power consumption

APPLICATIONS

- Portable meter references
- Portable test instruments
- Battery operated systems
- Panel meters
- Current loop instrumentation

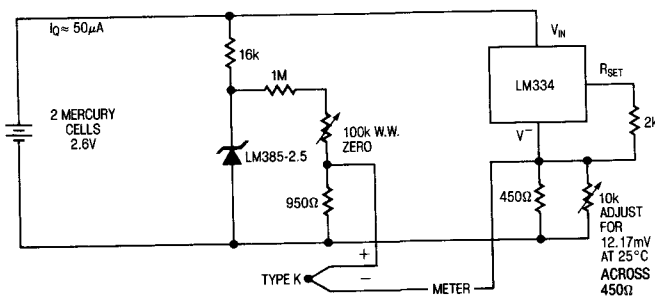
DESCRIPTION

The LM185-2.5 is a two terminal band gap reference diode that has been designed for applications which require precision performance with micropower operation. The device provides guaranteed operating specifications at currents as low as 20 μ A. The nominal voltage is 2.5V with both 1% and 2% tolerances available. Some additional features are: maximum dynamic impedance of 1 Ω , low noise and excellent stability over time and temperature. The advanced design, processing and testing techniques make Linear's LM185-2.5 a superior choice over previous designs. A circuit for cold junction compensation of a thermocouple is show below.

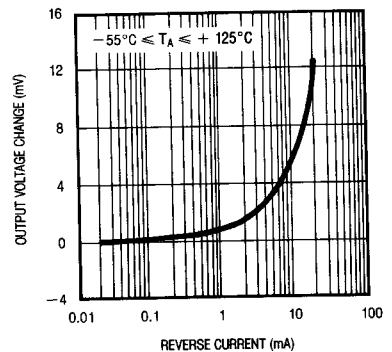
For applications requiring guaranteed temperature drift, see the LT1034 data sheet.

3

Thermocouple Cold Junction Compensator



Reverse Voltage Change

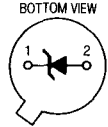
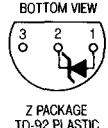


LM185-2.5/LM385-2.5

ABSOLUTE MAXIMUM RATINGS

Reverse Breakdown Current.....	30mA
Forward Current.....	10mA
Operating Temperature Range	
LM185-2.5.....	-55°C to 125°C
LM385-2.5.....	0°C to 70°C
Storage Temperature Range	
LM185-2.5.....	-65°C to 150°C
LM385-2.5.....	-65°C to 150°C
Lead Temperature (Soldering, 10 sec.).....	300°C

PACKAGE/ORDER INFORMATION

 BOTTOM VIEW H PACKAGE TO-46 METAL CAN	ORDER PART NUMBER	
		LM185H-2.5
	LM385BH-2.5	(NOTE 2)
 BOTTOM VIEW Z PACKAGE TO-92 PLASTIC	LM385Z-2.5	
	LM385BZ-2.5	
	(NOTE 2)	

ELECTRICAL CHARACTERISTICS (See Note 1)

SYMBOL	PARAMETER	CONDITIONS	LM185-2.5			LM385-2.5/385B-2.5			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_Z	Reverse Breakdown Voltage	$T_A = 25^\circ\text{C}$, $20\mu\text{A} \leq I_R \leq 20\text{mA}$ LM185-2.5 LM385-2.5 LM385B-2.5 (Note 2)	2.462	2.5	2.538	2.425	2.5	2.575	V
$\frac{\Delta V_Z}{\Delta \text{Temp}}$	Average Temperature Coefficient	$20\mu\text{A} \leq I_R \leq 20\text{mA}$ (Note 2)	20			20			ppm/°C
I_{min}	Minimum Operating Current	$T_{\text{min}} \leq T_A \leq T_{\text{max}}$	●	8	20	8	20		μA
$\frac{\Delta V_Z}{\Delta I_R}$	Reverse Breakdown Voltage Change with Current	$20\mu\text{A} \leq I_R \leq 1\text{mA}$ $T_A = 25^\circ\text{C}$ $T_{\text{min}} \leq T_A \leq T_{\text{max}}$	●	1	1.5	2	2.5		mV mV
		$1\text{mA} \leq I_R \leq 20\text{mA}$ $T_A = 25^\circ\text{C}$ $T_{\text{min}} \leq T_A \leq T_{\text{max}}$	●	10	20	20	25		mV mV
r_Z	Reverse Dynamic Impedance	$I_R = 100\mu\text{A}$ (Note 3) $T_A = 25^\circ\text{C}$ $T_{\text{min}} \leq T_A \leq T_{\text{max}}$	●	0.2	0.6	0.4	1	1.5	Ω Ω
e_n	Wide Band Noise (RMS)	$10\text{Hz} \leq f \leq 10\text{kHz}$, $I_R = 100\mu\text{A}$		120		120			μV
$\frac{\Delta V_Z}{\Delta \text{Time}}$	Long Term Stability	$T_A = 25^\circ\text{C} \pm 0.1^\circ\text{C}$, $I_R = 100\mu\text{A}$		20		20			ppm/kHr

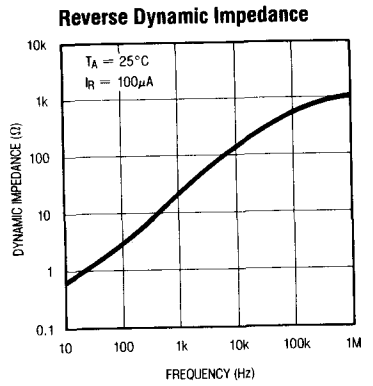
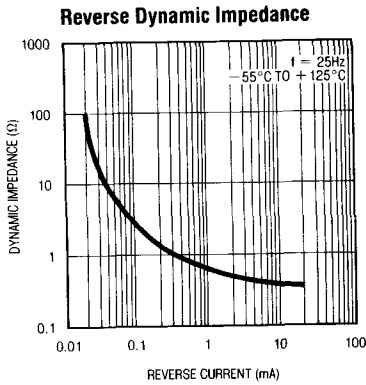
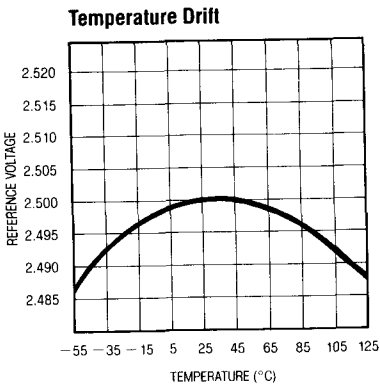
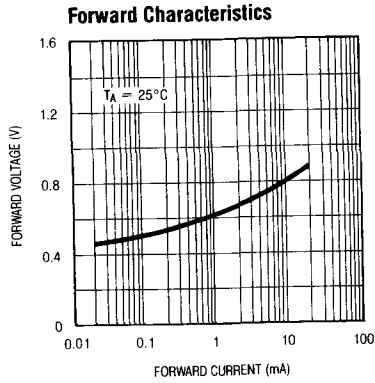
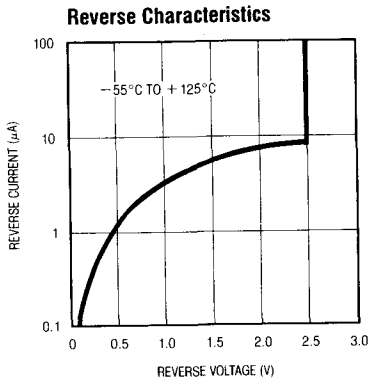
The ● denotes the specifications which apply over full operating temperature range.

Note 1: All specifications are for $T_A = 25^\circ\text{C}$ unless otherwise noted. For the LM185-2.5 $T_{\text{min}} = -55^\circ\text{C}$ and $T_{\text{max}} = +125^\circ\text{C}$. For LM385-2.5 $T_{\text{min}} = 0^\circ\text{C}$ and $T_{\text{max}} = +70^\circ\text{C}$.

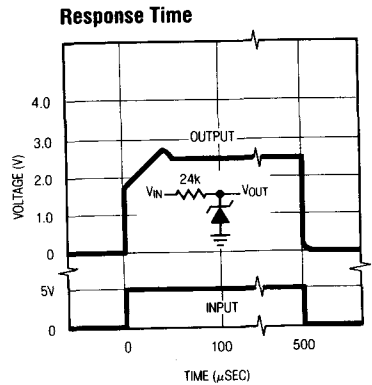
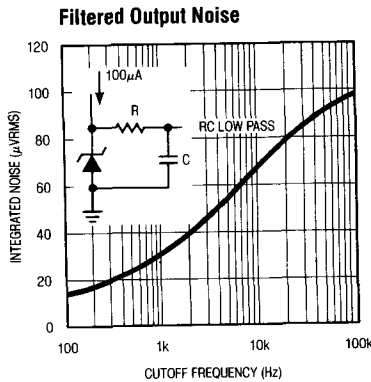
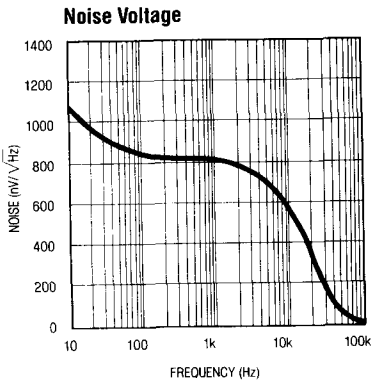
Note 2: For very low initial tolerance, consult LT1004 data sheet. The LT1004 is a low cost, pin for pin substitution device. For guaranteed temperature coefficient consult the LT1034-2.5 data sheet.

Note 3: Guaranteed but not tested.

TYPICAL PERFORMANCE CHARACTERISTICS

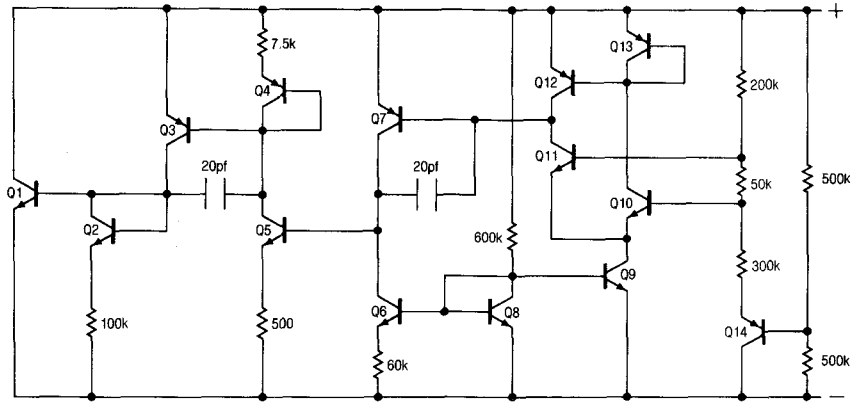


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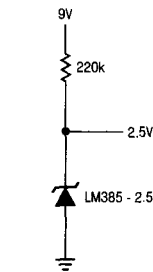


LM185-2.5/LM385-2.5

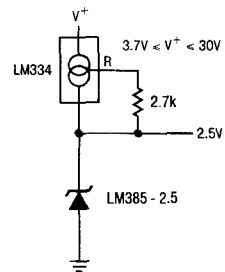
SCHEMATIC DIAGRAM



TYPICAL APPLICATIONS



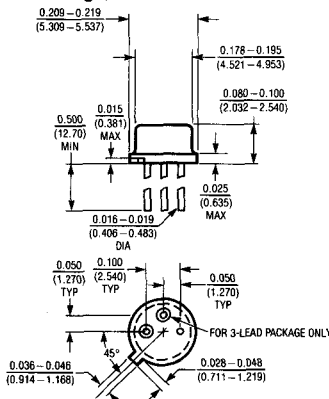
REFERENCE FROM A 9V BATTERY



OPERATION OVER A WIDE SUPPLY RANGE

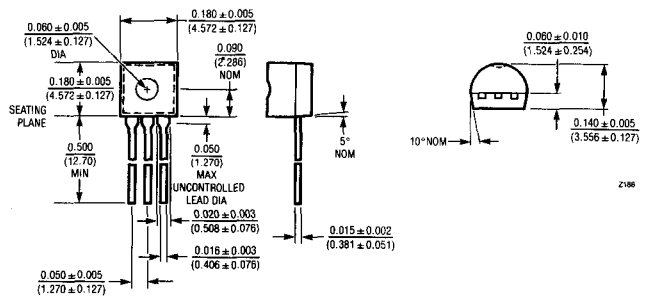
PACKAGE DESCRIPTION

H Package, 2 Lead TO-46 Metal Can



T_{max}	θ_{ja}	θ_{jc}
150°C	440°C/W	80°C/W

Z Package, 3 Lead TO-92 Plastic



T_{max}	θ_{ja}
150°C	160°C/W

FEATURES

- 15 μ A to 20mA Operating Range—1.2V Version
- 20 μ A to 20mA Operating Range—2.5V Version
- *Guaranteed* 1 Ω Dynamic Impedance
- Very Low Power Consumption

APPLICATIONS

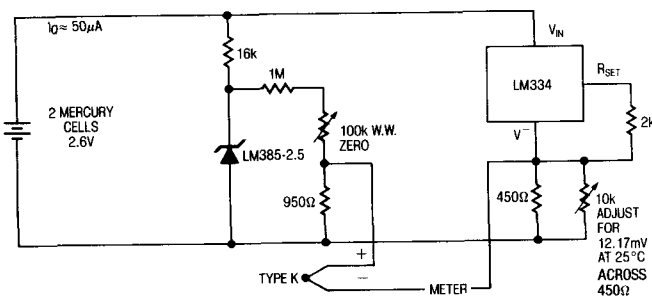
- Portable Meter References
- Portable Test Instruments
- Battery Operated Systems
- Panel Meters
- Current Loop Instrumentation

DESCRIPTION

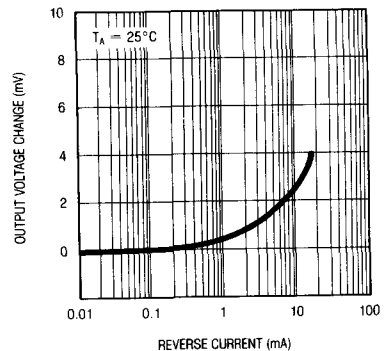
The LM385 series are two terminal band gap reference diodes that have been designed for applications which require precision performance with micropower operation. The devices provide guaranteed operating specifications at currents as low as 15 μ A. Some additional features are: maximum dynamic impedance of 1 Ω , low noise and excellent stability over time and temperature. The advanced design, processing and testing techniques make Linear's LM385 series a superior choice over previous designs. A circuit for cold junction compensation of a thermocouple is shown below.

3

Thermocouple Cold Junction Compensator



Reverse Voltage Change with Current (LM385-1.2)



LM385S8-1.2/LM385S8-2.5

ABSOLUTE MAXIMUM RATINGS

Reverse Breakdown Current	30mA
Forward Current	10mA
Operating Temperature Range	0°C to 70°C
Storage Temperature Range	-65°C to 150°C
Lead Temperature (Soldering, 10 sec.).....	300°C

PACKAGE/ORDER INFORMATION

ORDER PART NUMBER
LM385S8-1.2 LM385S8-2.5
PART MARKING
3851 (1.2V VERSION) 3852 (2.5V VERSION)

ELECTRICAL CHARACTERISTICS (See Note 1)

SYMBOL	PARAMETER	CONDITIONS	LM385-1.2			LM385-2.5			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_Z	Reverse Breakdown Voltage	$T_A = 25^\circ\text{C}$, $20\mu\text{A} \leq I_R \leq 20\text{mA}$	1.205	1.235	1.260	2.425	2.5	2.575	V
$\frac{\Delta V_Z}{\Delta \text{Temp}}$	Average Temperature Coefficient	$I_{\text{MIN}} \leq I_R \leq 20\text{mA}$ (Note 2)	20			20			ppm/°C
I_{min}	Minimum Operating Current	$T_{\text{min}} \leq T_A \leq T_{\text{max}}$	●	8	15	8	20		μA
$\frac{\Delta V_Z}{\Delta I_R}$	Reverse Breakdown Voltage Change with Current	$I_{\text{min}} \leq I_R \leq 1\text{mA}$ $T_A = 25^\circ\text{C}$ $T_{\text{min}} \leq T_A \leq T_{\text{max}}$	●	1		2		2.5	mV
		$1\text{mA} \leq I_R \leq 20\text{mA}$ $T_A = 25^\circ\text{C}$ $T_{\text{min}} \leq T_A \leq T_{\text{max}}$	●	20		20		25	mV
			●	25		25			mV
r_Z	Reverse Dynamic Impedance	$I_R = 100\mu\text{A}$ $T_A = 25^\circ\text{C}$ $T_{\text{min}} \leq T_A \leq T_{\text{max}}$	●	0.4	1	0.4	1	1.5	Ω
e_n	Wide Band Noise (RMS)	$10\text{Hz} \leq f \leq 10\text{kHz}$, $I_R = 100\mu\text{A}$		60		120			μV
$\frac{\Delta V_Z}{\Delta \text{Time}}$	Long Term Stability	$T_A = 25^\circ\text{C} \pm 0.1^\circ\text{C}$, $I_R = 100\mu\text{A}$		20		20			ppm/kHr

The ● denotes the specifications which apply over full operating temperature range.

Note 1: All specifications are for $T_A = 25^\circ\text{C}$ unless otherwise noted. $T_{\text{min}} = 0^\circ\text{C}$ and $T_{\text{max}} = +70^\circ\text{C}$.

Note 2: For guaranteed TC and very low initial tolerance, consult LT1034CS8 data sheet. The LT1034CS8 is a low cost, pin for pin substitution device.

FEATURES

- *Guaranteed* 0.5 ppm/°C temperature coefficient
- *Guaranteed* 1.0 Ω *max.* dynamic impedance
- *Guaranteed* 20μV RMS *max.* noise
- *Guaranteed* initial tolerance of 2%
- Wide operating current range

APPLICATIONS

- Precision voltage reference for multimeters
- Calibration equipment voltage standards
- Laboratory measurement equipment
- Industrial monitor/control instruments
- High accuracy data converters

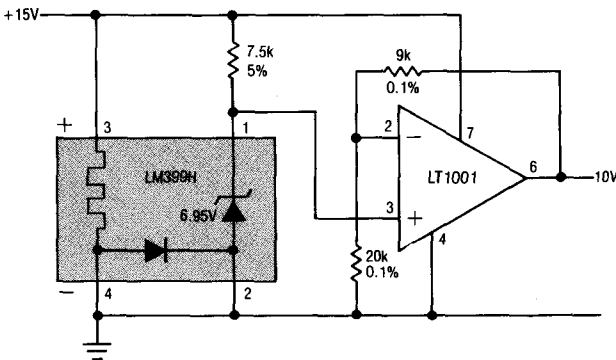
DESCRIPTION

The LM199/399 precision reference features excellent temperature stability over a wide range of voltage, temperature, and operating current conditions. A stabilizing heater is incorporated with the active zener on a monolithic substrate which nearly eliminates changes in voltage with temperature. The subsurface zener operates over a current range of 0.5mA to 10mA, and offers minimal noise and excellent long term stability.

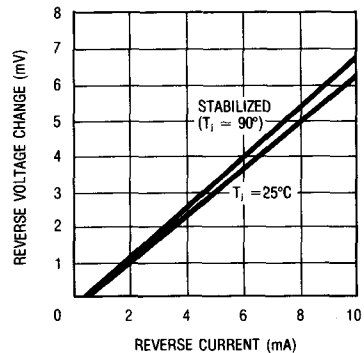
Ideal applications for the LM199/399 include digital voltmeters, precision calibration equipment, current sources and a variety of other precision low cost references. A 10 volt buffered reference application is shown below.

3

10 Volt Buffered Reference



Reverse Voltage Change



LM199/LM399 LM199A/LM399A

ABSOLUTE MAXIMUM RATINGS

Temperature Stabilizer	40V
Reverse Breakdown Current	20mA
Forward Current	1mA
Reference to Substrate Voltage $V_{(RS)}$, (Note 1). —0.1V	
Operating Temperature Range	
LM199/199A	–55°C to 125°C
LM399/399A	0°C to 70°C
Storage Temperature Range	
LM199/199A	–65°C to 150°C
LM399/399A	–65°C to 150°C
Lead Temperature (Soldering, 10 sec.)	300°C

PACKAGE/ORDER INFORMATION

TOP VIEW
H PKG.
TO-46 METAL CAN INSIDE THERMAL SHIELD

ORDER PART NO.
LM199H, LM199AH
LM399H, LM399AH
LM199AH-20, LM399AH-50

FUNCTIONAL BLOCK DIAGRAM

ELECTRICAL CHARACTERISTICS (See Note 2)

SYMBOL	PARAMETER	CONDITIONS	LM199/199A			LM399/399A			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_Z	Reverse Breakdown Voltage	$0.5\text{mA} \leq I_R \leq 10\text{mA}$	● 6.8	6.95	7.1	6.75	6.95	7.3	V
ΔV_Z	Reverse Breakdown Voltage Change with Current	$0.5\text{mA} \leq I_R \leq 10\text{mA}$	●	6	9		6	12	mV
r_Z	Reverse Dynamic Impedance	$I_R = 1\text{mA}$ (Note 5) ($10 \leq f \leq 100\text{Hz}$)	●	0.5	1		0.5	1.5	Ω
$\frac{\Delta V_Z}{\Delta \text{Temp}}$	Temperature Coefficient LM199/LM399	$-55^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$ $+85^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$ $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$		0.3 5	1 15		0.3	2	ppm/°C ppm/°C ppm/°C
	LM199A/LM399A	$-55^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$ $+85^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$ $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$		0.2 5	0.5 10		0.3	1	ppm/°C ppm/°C ppm/°C
e_n	RMS Noise	$10\text{Hz} \leq f \leq 10\text{kHz}$	●	7	20		7	50	μV
$\frac{\Delta V_Z}{\Delta \text{Time}}$	Long Term Stability	Stabilized, $22^\circ\text{C} \leq T_A \leq 28^\circ\text{C}$ 1000 Hours, $I_R = 1\text{mA} \pm 0.1\%$		8	Note 3		8	Note 3	ppm/ $\sqrt{\text{kH}}$
I_H	Temperature Stabilizer Supply Current	$T_A = +25^\circ\text{C}$, Still Air, $V_H = +30\text{V}$ $T_A = -55^\circ\text{C}$ (Note 4)		8.5 22	14 28		8.5	15	mA
V_H	Temperature Stabilizer Supply Voltage		●	9	40		9	40	V
	Warm-up Time to $\pm 0.05\% V_Z$	$V_H = 30\text{V}$, $T_A = 25^\circ\text{C}$		3			3		Seconds
	Initial Turn-on Current	$9\text{V} \leq V_H \leq 40\text{V}$, $T_A = 25^\circ\text{C}$, (See Note 4)		140	200		140	200	mA

The ● denotes the specifications which apply over full operating temperature range.

Note 1: The substrate is electrically connected to the negative terminal of the temperature stabilizer. The voltage that can be applied to either terminal of the reference is 40V more positive or 0.1V more negative than the substrate.

Note 2: These specifications apply for 30V applied to the temperature stabilizer and $-55^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$ for the LM199; and $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$ for the LM399.

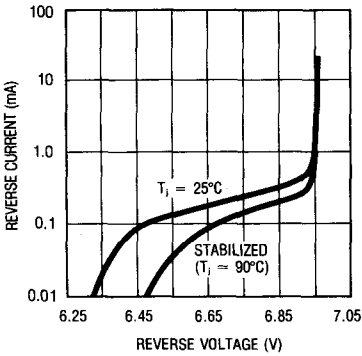
Note 3: Devices with maximum guaranteed long term stability of 20 ppm/ $\sqrt{\text{kH}}$ are available. Drift decreases with time.

Note 4: This initial current can be reduced by adding an appropriate resistor and capacitor to the heater circuit. See the performance characteristic graphs to determine values.

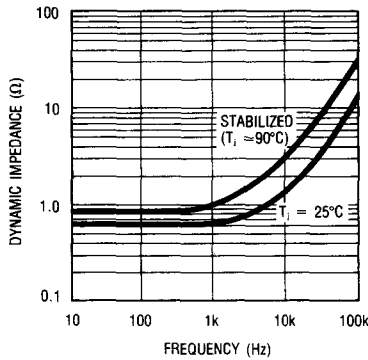
Note 5: Guaranteed by "Reverse Breakdown Change with Current."

TYPICAL PERFORMANCE CHARACTERISTICS

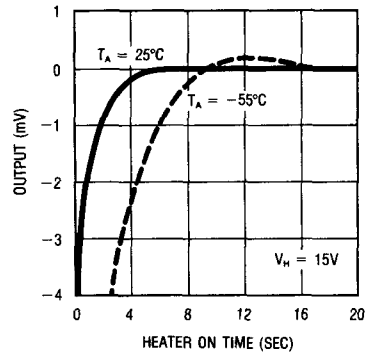
Reverse Characteristics



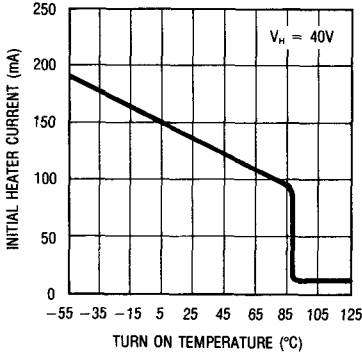
Dynamic Impedance



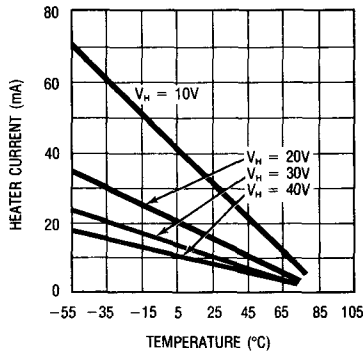
Stabilization Time



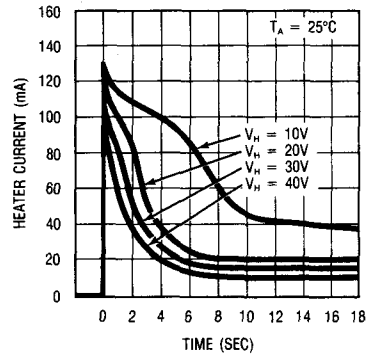
Initial Heater Current



Heater Current

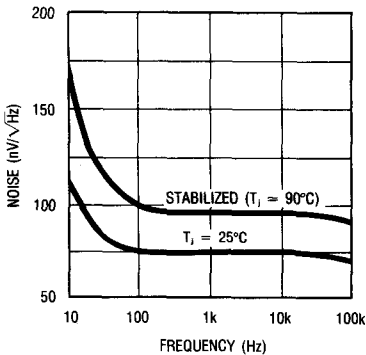


Heater Current

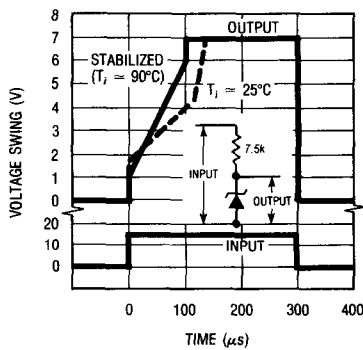


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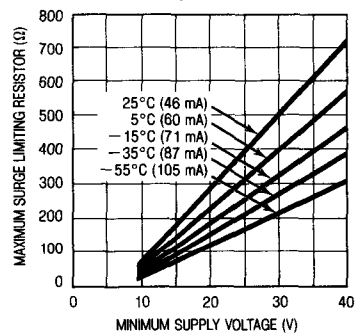
Zener Noise Voltage



Response Time



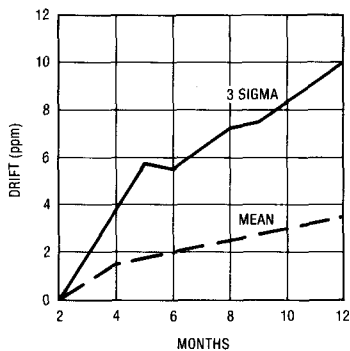
Limiting Surge Current



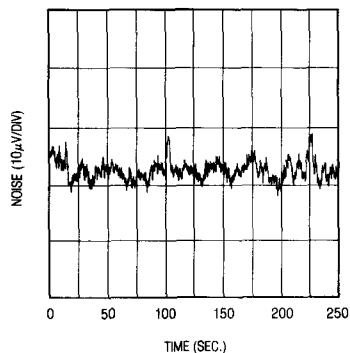
* Heater must be bypassed with a $2\ \mu\text{F}$ or larger tantalum capacitor if resistors are used.

TYPICAL PERFORMANCE CHARACTERISTICS

Long Term Reference Performance
44 Units Tested

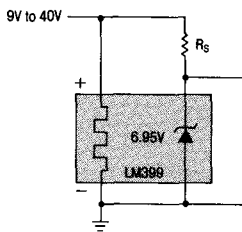


Low Frequency Noise Voltage

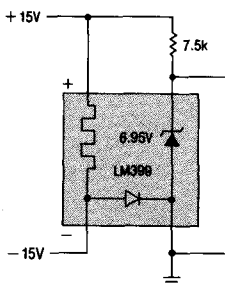


TYPICAL APPLICATIONS

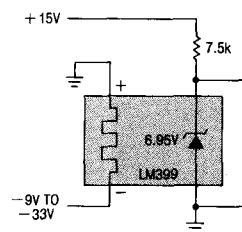
Single Supply Operation



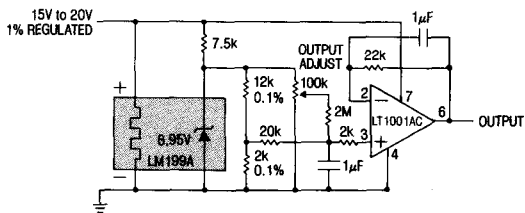
Split Supply Operation



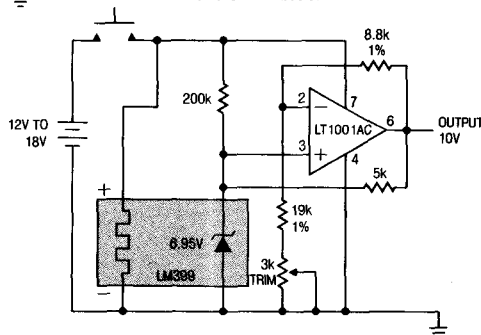
Negative Heater Supply with Positive Reference



Standard Cell Replacement

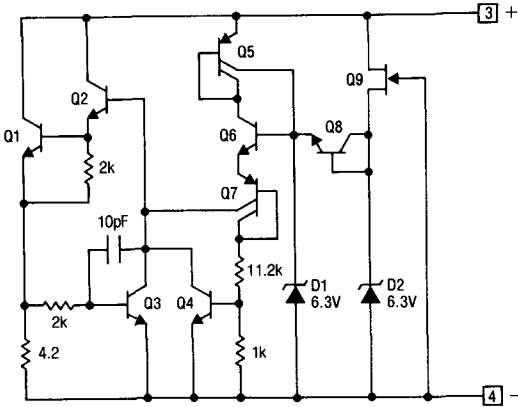


Portable Calibrator

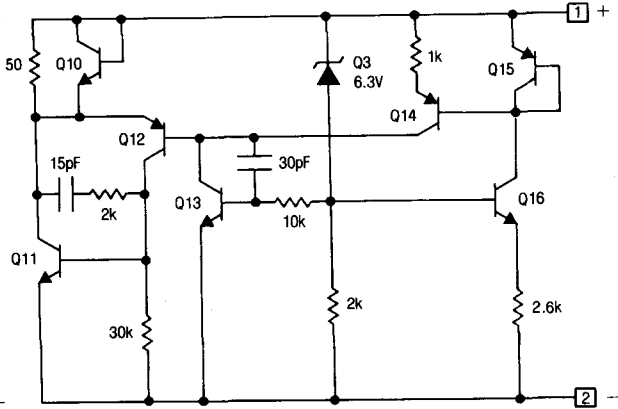


SCHEMATIC DIAGRAMS

Temperature Stabilizer



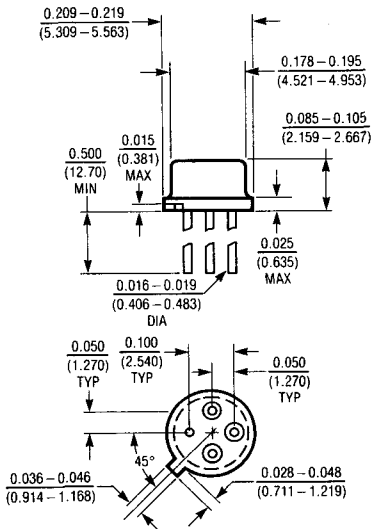
Reference



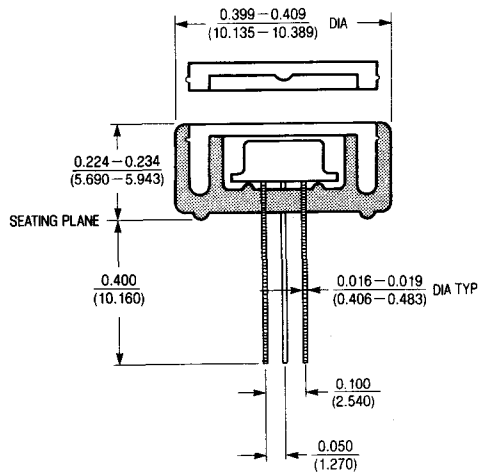
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PACKAGE DESCRIPTION

H Package, 4 Lead
TO-46 Metal Can



Thermal Shield*
For TO-46, H Package



*Thermal Shield Material is Valox™
Valox is a registered trademark of General Electric

NOTES

FEATURES

- Direct Replacement for Present References
- Ultra Low Drift—3ppm/°C Typ.
- Curvature Corrected
- Series or Shunt Operation
- Ultra High Line Rejection $\approx 1/2$ ppm/V
- Low Output Impedance $\approx 0.02\Omega$
- Tight Initial Output Voltage
- 100% Noise Tested

APPLICATIONS

- A to D and D to A Converters
- Precision Regulators
- Constant Current Sources
- V to F Converters
- Bridge Excitation

DESCRIPTION

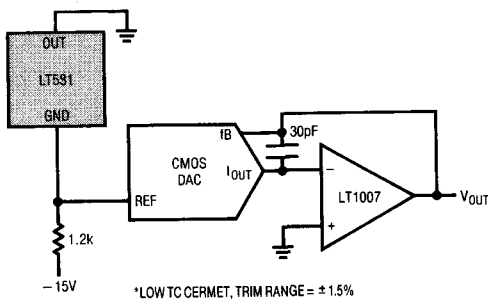
The LT580/LT581 are bandgap voltage references utilizing thin film technology and a greatly improved curvature correction technique. Wafer level trimming of both reference and output voltage combines to produce units with high yields to very low TC and tight initial tolerance of output voltage.

The LT580/LT581 can both sink and source up to 10mA and can be used in either the series or shunt mode. This allows the reference to be used for both positive and negative output voltages without external components. Minimum input-output voltage is less than 1V in the series mode, providing improved tolerance of low line conditions.

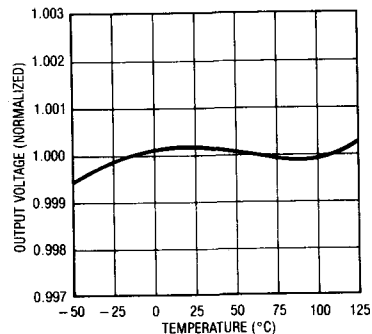
For voltage references with improved specifications, please see the LT1019, LT1021, and LT1031 data sheets.

3

Negative 10V Reference for CMOS DAC



Output Voltage Drift



LT580/LT581

ABSOLUTE MAXIMUM RATINGS

Input Voltage	40V
Storage Temperature Range	-65°C to 175°C
Lead Temperature (Soldering, 10 sec.)	300°C
Operating Temperature Range	
J, K, L, M Grades	0°C to 70°C
S, T, U Grades	-55°C to 125°C

PACKAGE/ORDER INFORMATION

BOTTOM VIEW	ORDER PART NUMBER
<p>H PACKAGE TO-52 METAL CAN</p>	LT580JH LT580KH LT580LH LT580MH LT580SH LT580TH LT580UH
<p>H PACKAGE TO-39 METAL CAN</p>	LT581JH LT581KH LT581LH LT581SH LT581TH LT581UH

LT580 ELECTRICAL CHARACTERISTICS $V_{IN} = +15V, T_A = 25^\circ C$ unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS	LT580			UNITS
			MIN	TYP	MAX	
V_R	Output Voltage	LT580J	2.425	2.500	2.575	V
		LT580K, S	2.475	2.500	2.525	V
		LT580L, M, T, U	2.490	2.500	2.510	V
TC	Output Voltage Change Over Temperature in mV and (ppm/°C)	LT580J (0°C to 70°C)	•		15 (85)	mV (ppm/°C)
		LT580K (0°C to 70°C)	•		7 (40)	mV (ppm/°C)
		LT580L (0°C to 70°C)	•		4.3 (25)	mV (ppm/°C)
		LT580M (0°C to 70°C)	•		1.75 (10)	mV (ppm/°C)
		LT580S (-55°C to +125°C)	•		25 (55)	mV (ppm/°C)
		LT580T (-55°C to +125°C)	•		11 (25)	mV (ppm/°C)
		LT580U (-55°C to +125°C)	•		4.5 (10)	mV (ppm/°C)
ΔV_{OUT} ΔV_{IN}	Line Regulation	$7V \leq V_{IN} \leq 30V$ LT580J, S		0.5	6	mV
		LT580K		0.5	4	mV
		LT580L, M, T, U		0.5	2	mV
		$4.5V \leq V_{IN} \leq 7V$ LT580J, S		0.1	3	mV
		LT580K		0.1	2	mV
		LT580L, M, T, U		0.1	1	mV
ΔV_{OUT} ΔI_{OUT}	Load Regulation (Sourcing) Shunt Mode	$0 \leq I_{OUT} \leq 10mA$		1	10	mV
		$1.5mA \leq I_{SHUNT} \leq 10mA$		2	10	mV
I_Q	Quiescent Current			0.75	1.5	mA
e_n	Output Noise (Note 1)	0.1Hz to 10Hz		10		μV_{p-p}
		Output Voltage Stability with Time	Per Month		25	μV
		Long Term		250		μV

LT581 ELECTRICAL CHARACTERISTICS $V_{IN} = +15V, T_A = 25^\circ C$ unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS	LT581			UNITS
			MIN	TYP	MAX	
V_R	Output Voltage	LT581S, J	9.970	10.000	10.030	V
		LT581T, K	9.990	10.000	10.010	V
		LT581U, L	9.995	10.000	10.005	V
TC	Output Voltage Change, Maximum Deviation from 25°C in mV and (ppm/°C)	LT581J (0°C to 70°C)	•		13.5 (30)	mV (ppm/°C)
		LT581K (0°C to 70°C)	•		6.75 (15)	mV (ppm/°C)
		LT581L (0°C to 70°C)	•		2.25 (5)	mV (ppm/°C)
		LT581S (-55°C to +125°C)	•		30 (30)	mV (ppm/°C)
		LT581T (-55°C to +125°C)	•		15 (15)	mV (ppm/°C)
LT581U (-55°C to +125°C)	•		10 (10)	mV (ppm/°C)		
ΔV_{OUT} ΔV_{IN}	Line Regulation	$15V \leq V_{IN} \leq 30V$		0.5	3	mV
		$13V \leq V_{IN} \leq 15V$		0.1	1	mV
ΔV_{OUT} ΔI_{OUT}	Load Regulation (Sourcing)	$0 \leq I_{OUT} \leq 5mA$		50	500	$\mu V/mA$
		Shunt Mode $1mA \leq I_{SHUNT} \leq 5mA$		100	500	$\mu V/mA$
I_Q	Quiescent Current			0.75	1.0	mA
e_n	Output Noise (Note 1)	0.1Hz to 10Hz		30		$\mu Vp-p$
		Long Term Stability	Non-Cumulative		25	
I_{SC}	Short Circuit Current			30		mA
I_{OUT}	Output Current	Sourcing	•	10	25	mA
		Sourcing	•	5		mA
		Sinking	•	5		mA

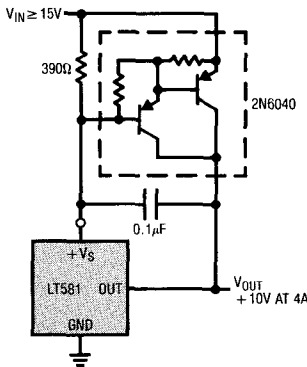
The • denotes the specifications which apply over the full operating temperature range.

Note 1: Although 0.1Hz to 10Hz noise is not a standard production test, Linear Technology does 100% test 10Hz to 1kHz noise. Consult factory for details.

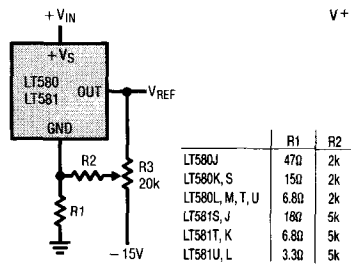
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TYPICAL APPLICATIONS

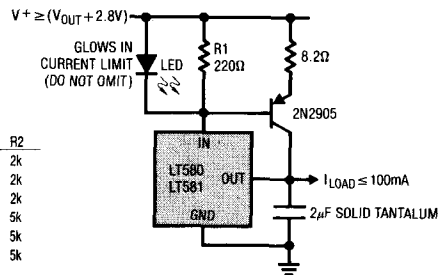
High Current Precision Supply



Suggested Output Trim

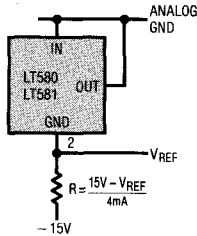


Output Current Boost with Current Limit

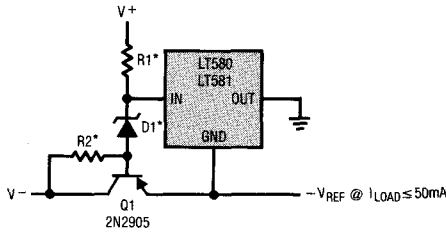


TYPICAL APPLICATIONS

Two-Terminal Negative Reference

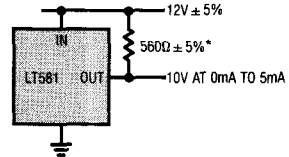


Negative Series Reference



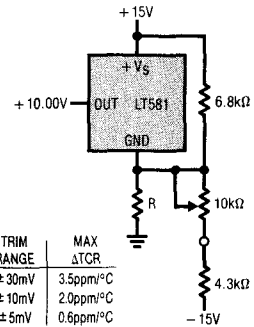
$$*R1 = \frac{V+ - 5V}{2mA}, R2 = \frac{|V-| - |VREF|}{1mA}, D1 = VREF + 5V$$

12V Supply Connection



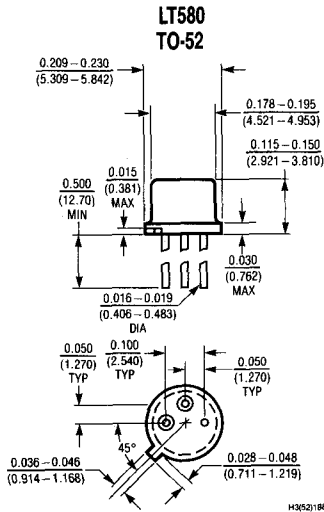
*NOT REQUIRED ON LTC LT580 OR LT581

Optional Trim Configuration

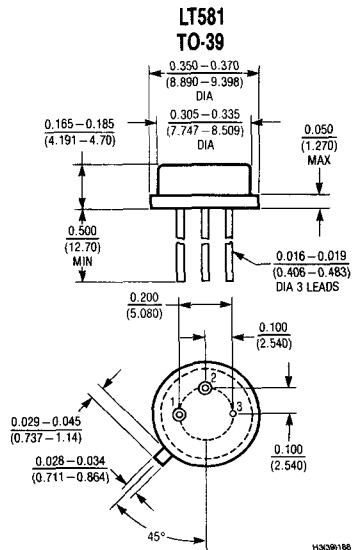


R	TRIM RANGE	MAX ΔTCR
22Ω	±30mV	3.5ppm/°C
12Ω	±10mV	2.0ppm/°C
3.9Ω	±5mV	0.6ppm/°C

PACKAGE DESCRIPTION



Tjmax	θJA
150°C	360°C/W



Tjmax	θJA
150°C	150°C/W

FEATURES

- Trimmed Output $\pm 0.3\%$
- Low Drift— $5\text{ppm}/^\circ\text{C}$ Typical
- Low Noise— 3ppm (μp)
- High Line Rejection
- Temperature Output—REF-02
- Low Supply Current 1.4mA Max.

APPLICATIONS

- A to D and D to A Converters
- Precision Regulators
- Constant Current Sources
- V to F Converters
- Bridge Excitation

DESCRIPTION

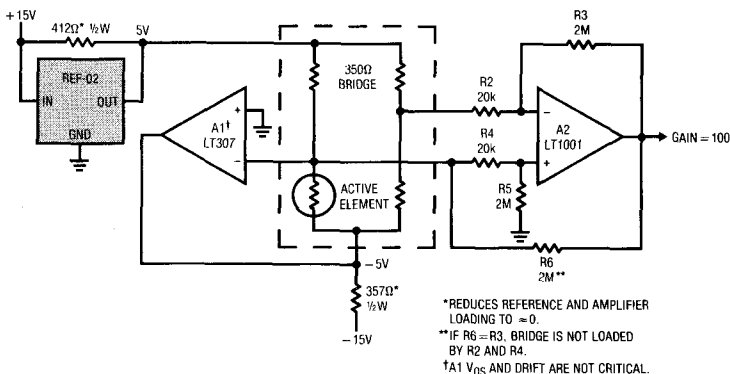
The REF-01/REF-02 are precision 10V and 5V bandgap references which provide stable output voltages over a wide range of operating conditions. Output voltage is accurate to $\pm 0.3\%$ with a low $5\text{ppm}/^\circ\text{C}$ typical temperature coefficient. The REF-01 and REF-02 are excellent choices for applications where low drift, moderate accuracy, low power consumption and low cost are considerations.

The REF-02 includes a temperature output pin which provides a linear voltage proportional to absolute temperature.

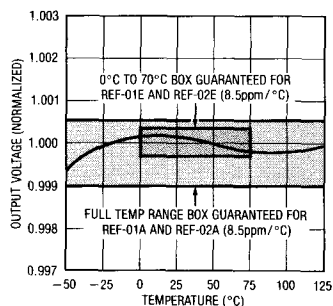
For lower drift and higher accuracy references, please see the LT1019 and LT1021 data sheets.

3

Ultra Linear Strain Gauge Amplifier



Output Voltage Temperature Drift



REF-01/REF-02

ABSOLUTE MAXIMUM RATINGS

REF-01/02, A, E, H	40V
REF-01C/02C	30V
Power Dissipation	500mW
Output Short Circuit Duration	
To Ground	Indefinite
To $V_{IN} \leq 16V$	Indefinite
To $V_{IN} > 16V$	Not Allowed
Storage Temperature	-65°C to 150°C
Operating Temperature	
REF-01/02, REF-01A/02A	-55°C to 125°C
REF-01E/02E, REF-01H/02H,	
REF-01C/02C, REF-01D/02D	0°C to 70°C

PACKAGE/ORDER INFORMATION

TOP VIEW		ORDER PART NUMBER	
<p>METAL CAN H PACKAGE *INTERNALLY CONNECTED. DO NOT CONNECT EXTERNALLY. **DO NOT CONNECT ON REF-01.</p>		REF-01AH	REF-02AH
		REF-01H	REF-02H
		REF-01EH	REF-02EH
		REF-01HH	REF-02HH
		REF-01CH	REF-02CH
			REF-02DH
<p>PLASTIC DIP N8 PACKAGE 8 PIN HERMETIC DIP *INTERNALLY CONNECTED. DO NOT CONNECT EXTERNALLY. **DO NOT CONNECT ON REF-01.</p>		REF-01EJ8	REF-02EJ8
		REF-01HJ8	REF-02HJ8
		REF-01CJ8	REF-02CJ8
		REF-01EN8	REF-02DJ8
		REF-01HN8	REF-02EN8
		REF-01CN8	REF-02HN8
			REF-02CN8
			REF-02DN8

ELECTRICAL CHARACTERISTICS

$V_{IN} = +15V$, $T_A = 25^\circ C$ unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS	REF-01A/E REF-02A/E			REF-01/H REF-02/H			UNITS	
			MIN	TYP	MAX	MIN	TYP	MAX		
V_O	Output Voltage	$I_L = 0$	REF-01 9.97	10.00	10.03	REF-01/H 9.95	10.00	10.05	V	
			REF-02 4.985	5.000	5.015	REF-02/H 4.975	5.000	5.025	V	
	Output Adjustment Range	$R_p = 10k\Omega$	REF-01 ± 3.0	+5, -27	—	REF-01/H ± 3.0	+5, -27	—	%	
			REF-02 ± 3.0	+5, -13	—	REF-02/H ± 3.0	+5, -13	—	%	
e_{np-p}	Output Voltage Noise	0.1Hz to 10Hz (Note 6)	REF-01 —	20	—	REF-01/H —	20	—	$\mu Vp-p$	
			REF-02 —	10	—	REF-02/H —	10	—	$\mu Vp-p$	
V_{IN}	Input Voltage Range		REF-01 12	—	40	REF-01/H 12	—	40	V	
			REF-02 7	—	40	REF-02/H 7	—	40	V	
$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	Line Regulation (Note 1)	$(V_{OUT} + 3V) \leq V_{IN} \leq 33V$	—	0.0001	0.010	—	0.0001	0.010	%/V	
$\frac{\Delta V_{OUT}}{\Delta I_{OUT}}$	Load Regulation (Note 1)	$I_L = 0mA$ to 10mA	REF-01	—	0.0005	0.008	—	0.0005	0.010	%/mA
			REF-02	—	0.0010	0.010	—	0.001	0.010	%/mA
I_Q	Quiescent Supply Current	No Load	—	0.65	1.4	—	0.65	1.4	mA	
I_{OUT}	Load Current		10	20	—	10	20	—	mA	
	Sink Current		-0.3	-20	—	-0.3	-20	—	mA	
I_{SC}	Short Circuit Current	$V_O = 0$	—	25	—	—	25	—	mA	
V_T	Temperature Voltage Output	(Note 2)	REF-02 Only	—	620	—	—	620	mV	

ELECTRICAL CHARACTERISTICS $V_{IN} = +15V$, $T_A = 25^\circ C$ unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS	REF-01C REF-02C			REF-02D			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_O	Output Voltage	$I_L = 0mA$	REF-01 4.950	REF-02 10.00 5.000	10.10 5.050	4.900	5.000	5.100	V V
	Output Adjustment Range	$R_P = 10k\Omega$	REF-01 ± 2.7	REF-02 +5, -27 +5, -13	—	—	—	—	% %
e_{np-p}	Output Voltage Noise	0.1Hz to 10Hz (Note 6)	REF-01 —	REF-02 30 12	—	—	12	—	μV_{p-p} μV_{p-p}
$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	Line Regulation (Note 1)	$(V_{OUT} + 3V) \leq V_{IN} \leq 33V$	—	0.0001	0.015	—	0.0001	0.04	%/V
$\frac{\Delta V_{OUT}}{\Delta I_{OUT}}$	Load Regulation (Note 1)	$I_L = 0mA$ to 8mA	—	0.0005	0.015	—	—	—	%/mA
		$I_L = 0mA$ to 4mA	—	—	—	—	0.001	0.04	%/mA
I_Q	Quiescent Supply Current	No Load	—	0.65	1.6	—	0.65	2.0	mA
I_{OUT}	Load Current		8	20	—	8	20	—	mA
	Sink Current		-0.2	20	—	-0.2	20	—	mA
I_{SC}	Short Circuit Current	$V_O = 0$	—	25	—	—	25	—	mA
V_T	Temperature Voltage Output	(Note 2)	REF-02 Only	—	620	—	—	620	mV

3

ELECTRICAL CHARACTERISTICS $V_{IN} = +15V$, $-55^\circ C \leq T_A \leq \pm 125^\circ C$ for REF-01A/02A and REF-01/REF-02, $0^\circ C \leq T_A \leq +70^\circ C$ for REF-01E/02E and REF-01H/02H, $I_L = 0mA$ unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS	REF-01A/E REF-02A/E			REF-01/H REF-02/H			UNITS	
			MIN	TYP	MAX	MIN	TYP	MAX		
$\frac{\Delta V}{\Delta T}$	Output Voltage Change with Temperature (Notes 3 and 4)	$0^\circ C \leq T_A \leq +70^\circ C$	●	—	0.02	0.06	—	0.035	0.17	%
		$-55^\circ C \leq T_A \leq +125^\circ C$	●	—	0.09	0.15	—	0.144	0.45	%
TC	Output Voltage Temperature Coefficient	(Note 5)	●	—	5	8.5	—	8	25	ppm/ $^\circ C$
	Change in V_O Temperature Coefficient with Output Adjustment	$R_P = 10k\Omega$	●	—	0.5	—	—	0.5	—	ppm/%
$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	Line Regulation ($V_{IN} = 8V$ to 33V) (Note 1)	$0^\circ C \leq T_A \leq +70^\circ C$	●	—	0.0001	0.012	—	0.0001	0.012	%/V
		$-55^\circ C \leq T_A \leq +125^\circ C$	●	—	0.0001	0.015	—	0.0001	0.015	%/V
$\frac{\Delta V_{OUT}}{\Delta I_{OUT}}$	Load Regulation ($I_L = 0mA$ to 8mA) (Note 1)	$0^\circ C \leq T_A \leq +70^\circ C$	●	—	0.002	0.010	—	0.002	0.012	%/mA
		$-55^\circ C \leq T_A \leq +125^\circ C$	●	—	0.002	0.012	—	0.002	0.015	%/mA
	Temperature Voltage Output Temperature Coefficient	(Note 2) REF-02	●	—	2.1	—	—	2.1	—	mV/ $^\circ C$

The ● denotes the specifications which apply over the full operating temperature range.

ELECTRICAL CHARACTERISTICS

$V_{IN} = +15V$, $0^{\circ}C \leq T_A \leq 70^{\circ}C$ and $I_L = 0mA$ unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS	REF-01C REF-02C			REF-02D			UNITS	
			MIN	TYP	MAX	MIN	TYP	MAX		
$\frac{\Delta V}{\Delta T}$	Output Voltage Change with Temperature	(Notes 3 and 4)	●	—	0.45	—	—	1.7	%	
TC	Output Voltage Temperature Coefficient	(Note 5)	●	—	8	65	—	8	250	ppm/°C
	Change in V_O Temperature Coefficient with Output Adjustment	$R_p = 10k\Omega$	●	—	0.5	—	—	0.5	—	ppm/%
$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	Line Regulation (Note 1)	$V_{IN} = 8V$ to $30V$	●	—	0.0001	0.018	—	0.0001	0.05	%/V
$\frac{\Delta V_{OUT}}{\Delta I_{OUT}}$	Load Regulation (Note 1)	$I_L = 0mA$ to $5mA$	●	—	0.002	0.018	—	0.002	0.05	%/mA
	Temperature Voltage Output Temperature Coefficient	(Note 2) REF-02	●	—	2.1	—	—	2.1	—	mV/°C

Note 1: Line and load regulation specifications include the effect of self heating.

Note 2: Limit current in or out of pin 3 to 50nA and capacitance on pin 3 to 30pF.

Note 3: ΔV is defined as the absolute difference between the maximum output voltage and the minimum output voltage over the specified temperature range expressed as a percentage of nominal output.

$$\Delta V = \left| \frac{V_{MAX} - V_{OUT}}{V_{OUT}} \right| \times 100$$

Note 4: ΔV specification applies trimmed or untrimmed.

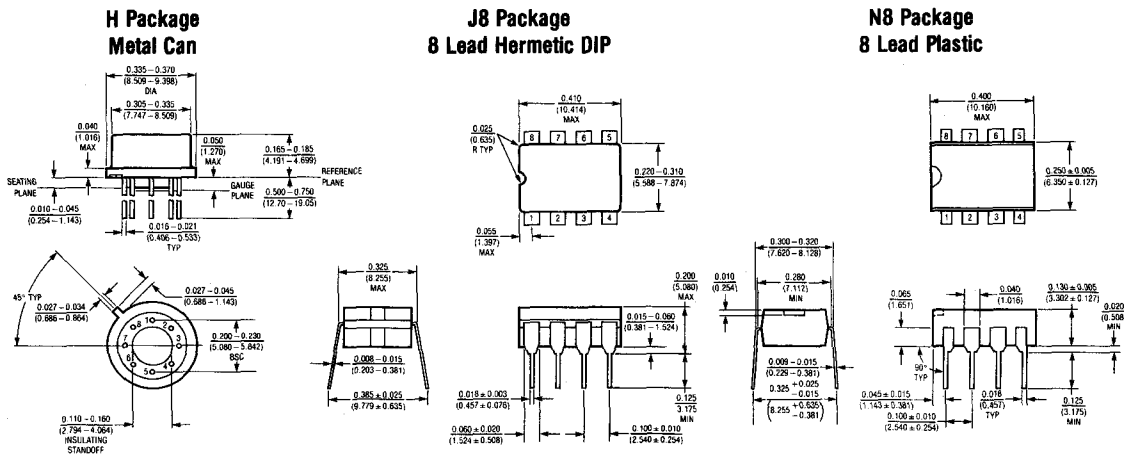
Note 5: TC is defined as ΔV divided by the temperature range, i.e.,

$$TC = \frac{\Delta V}{T_{MAX} - T_{MIN}}$$

Note 6: 0.1Hz to 10Hz noise cannot be 100% tested on modern high speed test equipment, so Linear Technology does not put a guaranteed maximum specification on this parameter for standard units. 100% bench testing of 0.1Hz to 10Hz noise is available on special request. To ensure low output noise, Linear Technology does 100% test 10Hz to 1kHz noise. Consult factory for details.

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.



*LEADS WITHIN 0.007 OF TRUE POSITION (TP) AT GAUGE PLANE

*LEADS WITHIN 0.007 OF TRUE POSITION (TP) AT GAUGE PLANE

T_{jmax}	$\theta_{j\alpha}$	$\theta_{j\epsilon}$
150°C	150°C/W	45°C/W

T_{jmax}	$\theta_{j\alpha}$
150°C	100°C/W

T_{jmax}	$\theta_{j\alpha}$
100°C	130°C/W

SECTION 4—VOLTAGE REGULATORS

SECTION 4—VOLTAGE REGULATORS

INDEX	4-2
SELECTION GUIDE	4-3
PROPRIETARY PRODUCTS	
<i>LT1003, 5 Volt, 5 Amp Voltage Regulator</i>	4-9
<i>LT1005, Logic Controlled Regulator</i>	4-17
<i>LT1020, Micropower Regulator and Comparator</i>	4-29
<i>LT1020CS, Micropower Regulator and Comparator</i>	4-45
<i>LT1033, 3A Negative Adjustable Regulator</i>	4-49
<i>LT1035, Logic Controlled Regulator</i>	4-57
<i>LT1036, Logic Controlled Regulator</i>	4-69
<i>LT1038, 10 Amp Positive Adjustable Voltage Regulator</i>	4-77
<i>LT1083, 7.5A Low Dropout Positive Adjustable Regulator</i>	4-89
<i>LT1083-5, 7.5A Low Dropout Positive Fixed 5V Regulator</i>	4-101
<i>LT1083-12, 7.5A Low Dropout Positive Fixed 12V Regulator</i>	4-101
<i>LT1084, 5A Low Dropout Positive Adjustable Regulator</i>	4-89
<i>LT1084-5, 5A Low Dropout Positive Fixed 5V Regulator</i>	4-101
<i>LT1084-12, 5A Low Dropout Positive Fixed 12V Regulator</i>	4-101
<i>LT1085, 3A Low Dropout Positive Adjustable Regulator</i>	4-89
<i>LT1085-5, 3A Low Dropout Positive Fixed 5V Regulator</i>	4-101
<i>LT1085-12, 3A Low Dropout Positive Fixed 12V Regulator</i>	4-101
<i>LT1086, 1.5A Low Dropout Positive Adjustable Regulator</i>	4-113
<i>LT1086-5, 1.5A Low Dropout Positive Fixed 5V Regulator</i>	4-113
<i>LT1086-12, 1.5A Low Dropout Positive Fixed 12V Regulator</i>	4-113
<i>LT1087 Adjustable Low Dropout Regulator with Kelvin-Sense Inputs</i>	13-28
<i>LT1120, Micropower Regulator with Comparator and Shutdown</i>	4-125
ENHANCED AND SECOND SOURCE PRODUCTS	
<i>LM117/LM317, Positive Adjustable Regulator</i>	4-137
<i>LT117A/LT317A, Improved LM117</i>	4-137
<i>LM117HV/LM317HV, High Voltage Positive Adjustable Regulator</i>	4-145
<i>LT117AHV/LT317AHV, Improved LM117HV</i>	4-145
<i>LM123/LM323, 5 Volt, 3 Amp Regulator</i>	4-149
<i>LT123A/LT323A, Improved LM123</i>	4-149
<i>LM137/LM337, Negative Adjustable Regulator</i>	4-157
<i>LT137A/LT337A, Improved LM137</i>	4-157
<i>LM137HV/LM337HV, High Voltage Negative Adjustable Regulator</i>	4-165
<i>LT137AHV/LT337AHV, Improved LM137HV</i>	4-165
<i>LM138/LM338, 5 Amp Positive Adjustable Regulator</i>	4-169
<i>LT138A/LT338A, Improved LM138</i>	4-169
<i>LM150/LM350, 3 Amp Positive Adjustable Regulator</i>	4-177
<i>LT150A/LT350A, Improved LM150</i>	4-177

MILITARY

I _O OUTPUT CURRENT (AMPS)*	POSITIVE OR NEGATIVE OUTPUT*	PART NUMBER	PACKAGE TYPE	V _{IN} MAX (V)	V _O NOMINAL REGULATED OUTPUT VOLTAGE (V)	FEATURES/COMMENTS
10.0	Pos. Adj.	LT1038MK	Steel TO-3	35	1.2 to 33	0.8% V _{OUT} Tol., Plug In Compatible with 117, 150, 138.
7.5	Pos. Fixed	LT1083MK-5	Steel TO-3	35	5	Low Dropout (1.2V), 1% V _{OUT} Tol.
		LT1083MK-12	Steel TO-3	35	12	Low Dropout (1.2V), 1% V _{OUT} Tol.
	Pos. Adj.	LT1083MK	Steel TO-3	35	1.2 to 34	Low Dropout (1.2V), 1% V _{REF} Tol. Pin Compatible with 117, 150, 138 Types
5.0	Pos. Fixed	LT1084MK-5	Steel TO-3	35	5	Low Dropout (1.2V), 1% V _{OUT} Tol.
		LT1084MK-12	Steel TO-3	35	12	Low Dropout (1.2V), 1% V _{OUT} Tol.
		LT1003MK	Steel TO-3	20	5	2% V _{OUT} Tol.
	Pos. Adj.	LT138AK LM138K	Steel TO-3	35	1.2 to 33	LT138A Has 1% V _{REF} Tol.
		LT1084MK	Steel TO-3	35	1.2 to 34	Low Dropout (1.2V), 1% V _{REF} Tol. Pin Compatible with 117, 150, 138 Types
Switching	LT1070MK LT1070HVMK	Steel TO-3 Steel TO-3	40 60	* *	Self Contained PWM and 5 Amp Switch in a 5-Pin Package	
3.0	Pos. Fixed	LT1085MK-5	Steel TO-3	35	5	Low Dropout (1.2V), 1% V _{OUT} Tol.
		LT1085MK-12	Steel TO-3	35	12	Low Dropout (1.2V), 1% V _{OUT} Tol.
		LT123AK LM123K	Steel TO-3	20	5	LT123A Has 1% V _{OUT} Tol.
	Pos. Adj.	LT150AK LM150K	Steel TO-3	35	1.2 to 33	LT150A Has 1% V _{REF} Tol.
		LT1085MK	Steel TO-3	35	1.2 to 34	Low Dropout (1.2V), 1% V _{REF} Tol. Pin Compatible with 117, 150 Types
	Neg. Adj.	LT1033MK	Steel TO-3	40	- 1.2 to - 37	2% V _{REF} Tol.
	Dual Pos. Fixed	LT1035MK	Steel TO-3	20	Two 5V Outputs	Logic Controlled 12V, 3A Output, 5V, 30mA Auxiliary Output
2.5	Switching	LT1071MK LT1071HVMK	Steel TO-3 Steel TO-3	40 60	12.5	Self Contained PWM and 2.5 Amp Switch in a 5-Pin Package
		1.5	Pos. Fixed	LT1086MK-5	Steel TO-3	5
LT1086MK-12	Steel TO-3			12	Low Dropout (1.2V), 1% V _{OUT} Tol.	
	Pos. Adj.	LT1086MK	Steel TO-3	35	1.2 to 34	Low Dropout (1.2V), 1% V _{REF} Tol. Pin Compatible with 117 Types.
0.5 to 1.5	Pos. Adj.	LT117AK LM117K	Steel TO-3	40	1.2 to 37	LT117A Has 1% V _{REF} Tol.
		LT117H LM117H	TO-39	60	1.2 to 37	
	Neg. Adj.	LT137AK LM137K	Steel TO-3	40	- 1.2 to - 37	LT137A Has 1% V _{REF} Tol.
		LT137AH LM137H	TO-39	40	- 1.2 to - 37	
	Pos. Adj. High Voltage	LT117AHVK LM117HVH	Steel TO-3 TO-39	60 60	1.2 to 57	LT117AHV Has 1% V _{REF} Tol.
	Neg. Adj. High Voltage	LT137AHVK LM137HVK	Steel TO-3 TO-39	50 50	- 1.2 to - 47	LT137AHV Has 1% V _{REF} Tol.
1.25	Switching	LT1072MK	Steel TO-3	40	*	Self Contained 40kHz PWM and 1.25 Amp Switch in a 5-Pin Package
		LT1072HVMK	Steel TO-3	60	*	
		LT1172MK	Steel TO-3	40	*	Self Contained 100kHz PWM and 1.25 Amp Switch in a 5-Pin Package
		LT1172HVMK	Steel TO-3	60	*	
1.0	Dual Pos. Fixed	LT1005MK	Steel TO-3	20	Two 5V Outputs	Logic Controlled 1 Amp Main Output Voltage, 35mA Auxiliary Output
125mA	Positive	LT1020MJ	14 Pin Cerdip	36	4 to 30	Dropout Voltage = 0.5V, 40mA I _O , Reference and Comparator
40mA to 100mA	Switched Capacitor	LT1026MJ8	CERDIP	10	**	Voltage Converter, 10mA Output
		LT1026MH	TO-5 Can	10	**	
		LTC1044MJ8	CERDIP	9.5	**	Voltage Converter, 40mA Output, 5kHz Switching Rate
		LTC1044MH	TO-5 Can	9.5	**	
		LT1054MJ	CERDIP	16	††	Voltage Converter and Regulator, 100mA Output, 25kHz Switching Rate
		LT1054MH	TO-5 Can	16	††	

* The I_O values for the LT1070, LT1071, LT1072, and LT1172 are switch current values. Actual output current, voltage and polarity depends on the type of switching regulator employed.

** These devices are non-regulating converters.

†† The available output voltage range is dependent upon the mode of operation selected.

4

REGULATOR SELECTION GUIDE

COMMERCIAL

I _O OUTPUT CURRENT (AMPS)*	POSITIVE OR NEGATIVE OUTPUT*	PART NUMBER	PACKAGE TYPE	V _{IN} MAX (V)	V _O NOMINAL REGULATED OUTPUT VOLTAGE (V)	FEATURES/COMMENTS	
10.0	Pos. Adj.	LT1038CK	Steel TO-3	35	1.2 to 33	2% V _{OUT} Tol., Plug In Compatible with 317, 350, 338.	
7.5	Pos. Fixed	LT1083CK-5	Steel TO-3	35	5	Low Dropout (1.2V), 1% V _{OUT} Tol.	
		LT1083CP-5	Plastic TO-3P	35	5	Low Dropout (1.2V), 1% V _{OUT} Tol.	
		LT1083CK-12	Steel TO-3	35	12	Low Dropout (1.2V), 1% V _{OUT} Tol.	
		LT1083CP-12	Plastic TO-3P	35	12	Low Dropout (1.2V), 1% V _{OUT} Tol.	
	Pos. Adj.	LT1083CK	Steel TO-3	30	1.2 to 29	Low Dropout (1.2V) Pin Compatible with 317, 350, 338 Types	
		LT1083CP	Plastic TO-3P	30	1.2 to 29		
5.0	Pos. Fixed	LT1003CK	Steel TO-3	20	5	2% V _{OUT} Tol. Low Dropout (1.2V), 1% V _{OUT} Tol. Low Dropout (1.2V), 1% V _{OUT} Tol. Low Dropout (1.2V), 1% V _{OUT} Tol. Low Dropout (1.2V), 1% V _{OUT} Tol. Low Dropout (1.2V), 1% V _{OUT} Tol.	
		LT1084CK-5	Steel TO-3	35	5		
		LT1084CP-5	Plastic TO-3P	35	5		
		LT1084CK-12	Steel TO-3	35	12		
		LT1084CP-12	Plastic TO-3P	35	12		
		Pos. Adj.	LT338AK LM338K	Steel TO-3	35		1.2 to 33
	LT1084CK		Steel TO-3	30	1.2 to 29		
	LT1084CP		Plastic TO-3P	30	1.2 to 29		
	Switching	LT1070CK	Steel TO-3	40	*	Self Contained PWM and 5 Amp Switch in a 5-Pin Package.	
		LT1070CT	TO-220	40	*		
		LT1070HVCK	Steel TO-3	60	*		
		LT1070HVCT	TO-220	60	*		
3.0	Pos. Fixed	LT323AK LM323K	Steel TO-3	20	5	LT323A Has 1% V _{REF} Tol. Low Dropout (1.2V), 1% V _{OUT} Tol. Low Dropout (1.2V), 1% V _{OUT} Tol. Low Dropout (1.2V), 1% V _{OUT} Tol. Low Dropout (1.2V), 1% V _{OUT} Tol. Low Dropout (1.2V), 1% V _{OUT} Tol.	
		LT323AT	TO-220	20	5		
		LT1085CK-5	Steel TO-3	35	5		
		LT1085CT-5	TO-220	35	5		
		LT1085CK-12	Steel TO-3	35	12		
		LT1085CT-12	TO-220	35	12		
	Pos. Adj.	LT350AK LM350K	Steel TO-3	35	1.2 to 33	LT350A Has 1% V _{REF} Tol. Low Dropout (1.2V) Pin Compatible with 317, 350 Types	
		LT350AT LM350T	TO-220	35	1.2 to 33		
		LT1085CK	Steel TO-3	30	1.2 to 29		
	Neg. Adj.	LT1033CK	Steel TO-3	40	-1.2 to -37	2% V _{REF} Tol.	
		LT1033CT	TO-220	40	-1.2 to -37		
		LT1035CK	Steel TO-3	20	Two 5V Outputs		Logic Controlled Main Output Voltage, 75mA Auxiliary Output
	LT1035CT	TO-220	20	Two 5V Outputs			
	Dual Pos. Fixed	LT1036CK	Steel TO-3	30	12, 5	Logic Controlled 12V, 3A Output, 5V, 75mA Auxiliary Output	
		LT1036CT	TO-220	30	12, 5		
2.5	Switching	LT1071CK	Steel TO-3	40	*	Self Contained PWM and 2.5 Amp Switch in a 5-Pin Package	
		LT1071CT	TO-220	40	*		
		LT1071HVCK	Steel TO-3	60	*		
		LT1071HVCT	TO-220	60	*		
	Pos. Fixed	LT1086CK-5	Steel TO-3	35	5	Low Dropout (1.2V), 1% V _{OUT} Tol. Low Dropout (1.2V), 1% V _{OUT} Tol. Low Dropout (1.2V), 1% V _{OUT} Tol. Low Dropout (1.2V), 1% V _{OUT} Tol.	
		LT1086CT-5	TO-220	35	5		
		LT1086CK-12	Steel TO-3	35	12		
		LT1086CT-12	TO-220	35	12		
	0.5 to 1.5	Pos. Adj.	LT317AK LM317K	Steel TO-3	40	1.2 to 37	LT317A Has 1% V _{REF} Tol. Low Dropout (1.2V), 1% V _{REF} Tol. Pin Compatible with 317 Types
			LT317AH LM317H	TO-39	40	1.2 to 34	
			LT317AT LM317T	TO-220	40	1.2 to 34	
			LT1086CK	Steel TO-3	35	1.2 to 34	
LT1086CT			TO-220	35	1.2 to 34		
Neg. Adj.		LT337AK LM337K	Steel TO-3	40	-1.2 to -37	LT337A Has 1% V _{REF} Tol.	
		LT337AH LM337H	TO-39	40	-1.2 to -37		
		LT337AT LM337H	TO-220	40	-1.2 to -37		
Pos. Adj. High Voltage		LT317AHVK LM317HVH	Steel TO-3	60	1.2 to 57	LT317HV Has 1% V _{REF} Tol.	
		LT317AHVH LM317HVH	TO-39	60	1.2 to 57		
Neg. Adj. High Voltage	LT337AHVK LM337HVH	Steel TO-3	50	-1.2 to -47	LT337HV Has 1% V _{REF} Tol.		
	LT337AHVH LM337HVH	TO-39	50	-1.2 to -47			

REFER TO TABLE OF CONTENTS FOR REVISED DATA LOCATION

REGULATOR SELECTION GUIDE

COMMERCIAL

I _O OUTPUT CURRENT (AMPS)*	POSITIVE OR NEGATIVE OUTPUT*	PART NUMBER	PACKAGE TYPE	V _{IN} MAX (V)	V _O NOMINAL REGULATED OUTPUT VOLTAGE (V)	FEATURES/COMMENTS	
1.25	Switching	LT1072CK	Steel TO-3	40	*	Self Contained 40kHz PWM and 1.25 Amp Switch in a 5-Pin Package	
		LT1072CT	Plastic TO-220	40	*		
		LT1072HVCK	Steel TO-3	60	*		
		LT1072HVCT	Plastic TO-220	60	*		
		LT1072CN8	8 Pin DIP	40	*		
		LT1172CK	Steel TO-3	40	*		Self Contained 100kHz PWM and 1.25 Amp Switch in a 5-Pin Package
		LT1172CT	Plastic TO-220	40	*		
		LT1172HVCK	Steel TO-3	60	*		
		LT1172HVCT	Plastic TO-220	60	*		
LT1172CN8	Plastic 8 Pin DIP	40	*				
1.0	Dual Pos. Fixed	LT1005CK	Steel TO-3	20	Two 5V Outputs	Logic Controlled Main Output Voltage	
		LT1005CT	TO-220	20			
125mA	Positive	LT1020CJ	14 Pin CERDIP	36	4 to 30	Dropout Voltage = 0.5V, 40µA I _O , Reference and Comparator	
		LT1020CN	14 Pin Plastic	36	4 to 30		
		LT1020CS	8 Pin Plastic SOL	36	4 to 30	Dropout Voltage = 0.2V, 40A I _O , Reference, Comparator, Shutdown, 8 Pin Package	
		LT1120CJ8	8 Pin CERDIP	36	4 to 30		
		LT1120CN8	8 Pin Plastic DIP	36	4 to 30		
		LT1120CH	8 Pin TO-5	36	4 to 30		
40mA to 100mA	Switched Capacitor	LT1026CJ8	CERDIP	10	**	Voltage Converter, 100mA Output, 25kHz Switching Rate	
		LT1026CN8	Plastic DIP	10	**		
		LT1026CH	TO-5 Can	10	**	Voltage Converter, 40mA Output, 25kHz Switching Rate	
		LTC1044CJ8	CERDIP	9.5	**		
		LTC1044CN8	Plastic DIP	9.5	**		
		LTC1044CH	TO-5 Can	9.5	**		
		LTC1044CS8	Plastic SO	9.5	**	Voltage Converter and Regulator, 100mA Output, 25kHz Switching Rate	
		LT1054CJ8	CERDIP	16	††		
		LT1054CN8	Plastic DIP	16	††		
		LT1054CH	TO-5 Can	16	††		
LT1054CS8	Plastic SOL	16	††				
LT1054SOL	Plastic SOL	16	††				

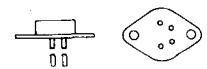
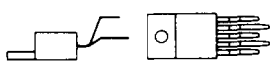
* The I_O values are based on LT1071, LT1072, and LT1172 series current values. Actual output current, voltage and polarity depends on the type of switching regulator employed.

** These devices are non-regulating converters.

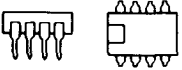
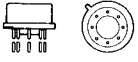
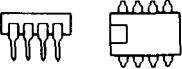
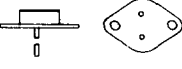

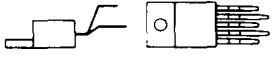
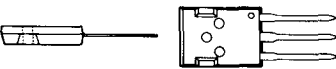
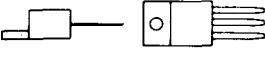
†† The available output voltage ranges depend upon the mode of operation selected.

REFER TO TABLE OF CONTENTS FOR REVISED DATA LOCATION

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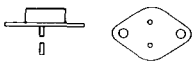
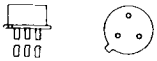
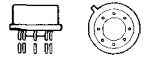

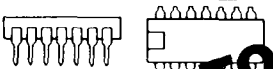


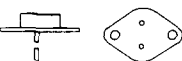


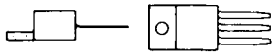
	MILITARY	COMMERCIAL	FEATURES
	LT1070MK LT1070HVMK	LT1070CK LT1070HVCK	Current Mode 40kHz PWM with Self-Protected 5 Amp Switch on the Same Chip, Capable of Operation in Flyback, Boost, Buck-Boost, and 'CUK Converters.
	LT1071MK LT1071HVMK	LT1071CK LT1071HVCK	Current Mode 40kHz PWM with Self-Protected 2.5 Amp Switch on the Same Chip, Capable of Operation in Flyback, Boost, Buck-Boost, and 'CUK Converters.
	LT1072MK LT1072HVMK	LT1072CK LT1072HVCK	Current Mode 40kHz PWM with Self-Protected 1.25 Amp Switch on the Same Chip, Capable of Operation in Flyback, Boost, Buck-Boost, and 'CUK Converters.
	LT1172MK LT1172HVMK	LT1172CK LT1172HVCK	Current Mode 100kHz PWM with Self-Protected 1.25 Amp Switch on the Same Chip, Capable of Operation in Boost, Buck-Boost, and CUK Converters.
		LT1070CT LT1070HVCT	Current Mode 40kHz PWM with Self-Protected 5 Amp Switch on the Same Chip, Capable of Operation in Flyback, Boost, Buck-Boost, and 'CUK Converters.
		LT1071CT LT1071HVCT	Current Mode 40kHz PWM with Self-Protected 2.5 Amp Switch on the Same Chip, Capable of Operation in Flyback, Boost, Buck-Boost, and 'CUK Converters.
		LT1072CT LT1072HVCT	Current Mode 40kHz PWM with Self-Protected 1.25 Amp Switch on the Same Chip, Capable of Operation in Flyback, Boost, Buck-Boost, and 'CUK Converters.
		LT1172CT LT1172HVCT	Current Mode 100kHz PWM with Self-Protected 1.25 Amp Switch on the Same Chip, Capable of Operation in Boost, Buck-Boost, and CUK Converters.

REGULATOR SELECTION GUIDE

	MILITARY	COMMERCIAL	FEATURES
SWITCHING REGULATORS		LT1072	Current Mode 40kHz PWM with Self-Protected 1.25 Amp Switch on the Same Chip, Capable of Operation in Boost, Buck-Boost, and CUK Converters in an 8-pin miniDIP package.
		LT1172CN8	Current Mode 100kHz PWM with Self-Protected 1.25 Amp Switch on the Same Chip, Capable of Operation in Boost, Buck-Boost, and CUK Converters in an 8-pin miniDIP package.
SWITCHED CAPACITOR CONVERTER/REGULATORS	LT1026MH	LT1026CH	10mA Output
	LT1044MH	LTC1044CH	40mA Output, 5kHz Switching Rate
	LT1054MH	LT1054CH	100mA, 25kHz Switching Rate, Voltage Regulated Output
	LT1026MJ	LT1026CJ8	10mA Output
		LT1026CN8	
	LTC1044MJ	LTC1044CJ8	40mA Output, 5kHz Switching Rate
		LTC1044CN8	
	LT1054MJ	LT1054CJ8	100mA Output, 25kHz Switching Rate
POSITIVE FIXED	LT1083MK-5	LT1083CK-5	5V, 7.5A Low Dropout
	LT1083MK-12	LT1083CK-12	12V, 7.5A Low Dropout
	LT1084MK-5	LT1084CK-5	5V, 5A Low Dropout
	LT1084MK-12	LT1084CK-12	12V, 5A Low Dropout
	LT1085MK-5	LT1085CK-5	5V, 3A Low Dropout
	LT1085MK-12	LT1085CK-12	12V, 3A Low Dropout
	LT1086MK-5	LT1086CK-5	5V, 1.5A Low Dropout
	LT1086MK-12	LT1086CK-12	12V, 1.5A Low Dropout
	LT1003MK	LT1003CK	5V ± 2%, 5 Amp
	LT323AK	LT323CK	5V ± 1%, 3 Amp
	LT323K	LT323CK	5V ± 3%, 3 Amp
	LT1005MK	LT1005CK	Dual Output Regulator with 5V 1 Amp Logic Switchable Output and Auxiliary 5V 35mA Output
	LT1035MK	LT1035CK	Dual Output Regulator with 5V 3 Amp Logic Switchable Output and Auxiliary 5V 75mA Output
	LT1036MK	LT1036CK	Dual Output Regulator with 12V 3 Amp Logic Switchable Output and Auxiliary 5V 75mA Output
		LT1005CT	Dual Output Regulator with 5V 1 Amp Logic Switchable Output and Auxiliary 5V 35mA Output
		LT1035CT	Dual Output Regulator with 5V 3 Amp Logic Switchable Output and Auxiliary 5V 75mA Output
		LT1036CT	Dual Output Regulator with 12V 3 Amp Logic Switchable Output and Auxiliary 5V 75mA Output
		LT1083CP-5	5V, 7.5A Low Dropout
		LT1083CP-12	12V, 7.5A Low Dropout
		LT1084CP-5	5V, 5A Low Dropout
		LT1084CP-12	12V, 5A Low Dropout
		LT1003CP	5V ± 2%, 5 Amp
		LT323AP	5V ± 1%, 3 Amp
		LM323P	5V ± 3%, 3 Amp
		LT1085CT-5	5V, 3A Low Dropout
		LT1085CT-12	12V, 3A Low Dropout
		LT1086CT-5	5V, 1.5A Low Dropout
		LT1086CT-12	12V, 1.5A Low Dropout
		LT323AT	5V ± 1%, 3 Amp

REFER TO TABLE OF CONTENTS FOR REVISED DATA LOCATION

REGULATOR SELECTION GUIDE

	MILITARY	COMMERCIAL	FEATURES
POSITIVE ADJUSTABLES			
	LT1038MK LT1083MK LT1084MK LT138AK LM138K LT1085MK LT150AK LM150K LT1086MK LM117AK LM117K LT117AHVK LM117AHVK	LT1038CK LT1083CK LT1084CK LT338AK LM338K LT1085CK LT350AK LM350K LT1086CK LT317AK LM317K LT317AHVK LM317AHVK	10 Amp 7.5 Amp Low Dropout 5 Amp Low Dropout 5 Amp 1% Reference 5 Amp 3 Amp Low Dropout 3 Amp 1% Reference 3 Amp 1.5 Amp Low Dropout 1.5 Amp 1% Reference 1.5 Amp 1.5 Amp 1% Reference, Hi Voltage 1.5 Amp, Hi Voltage
	LT117AH LM117H LM117AHVH LM117HVH	LT317AH LM317H LT317AHVH LM317HVH	0.5 Amp 1% Reference 0.5 Amp 0.5 Amp 1% Reference, Hi Voltage 0.5 Amp, Hi Voltage
		LT1120CH LT1120CS	Micropower, Ultra Low Dropout Regulator with 2.5V Independent Reference and Comparator, and Output Shutdown in 8 Pin Package
		LT1083CP LT1084CP LT338AP LM338P LT1085CP LM350P	7.5 Amp Low Dropout 5 Amp Low Dropout 5 Amp 1% Reference 5 Amp 3 Amp 1% Reference 3 Amp
		LT1020CJ LT1020CV	Very Low Dropout Voltage, 40 μ A Supply Current, 2.5V Independent Reference, and Voltage Comparator on Same Chip.
		LT1120CJ8 LT1120CN8	Micropower, Ultra Low Dropout Regulator with 2.5V Independent Reference and Comparator, and Output Shutdown in 8 Pin Package
		LT1085CT LT350AT LM350T LT1086CT LT317AT LM317T	3 Amp Low Dropout 3 Amp 1% Reference 3 Amp 1.5 Amp Low Dropout 1.5 Amp 1% Reference 1.5 Amp
NEGATIVE ADJUSTABLES			
	LT137AK LM137K LT137AHVK LM137HVK LT1033MK	LT337K LM337K LT337AHVK LT337HVK LT1033CK	1.5 Amp 1% Reference 1.5 Amp 1.5 Amp 1% Reference, Hi Voltage 1.5 Amp, Hi Voltage 3 Amp 2% Reference
	LT137AH LM137H LT137AHVH LM137HVH	LT337AH LM337H LT337AHVH LM337HVH	0.5 Amp 1% Reference 0.5 Amp 0.5 Amp 1% Reference, Hi Voltage 0.5 Amp, Hi Voltage
		LT1033CP	3 Amp 2% Reference
		LT337AT LM337T LT1033CT	1.5 Amp 1% Reference 1.5 Amp 3 Amp 2% Reference

REFER TO TABLE OF CONTENTS FOR REVISED DATA LOCATION

NOTES

FEATURES

- *Guaranteed 2%* Initial Tolerance of output voltage
- 5 Amp Output Current
- 40 Watt Capability
- Full Internal Overload Protection
- 100% Burn-in in Thermal Limit

APPLICATIONS

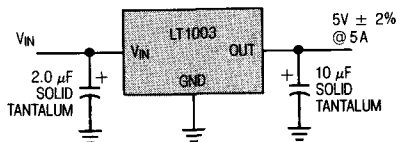
- Local 5V Regulators
- On Card Regulation
- Lab Supplies
- Instrumentation Supplies

DESCRIPTION

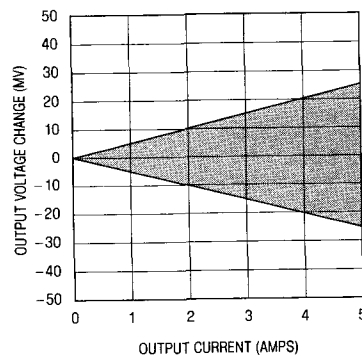
The LT1003 is a 5 amp version of the popular LM123 5V regulator. In addition to higher output current, it offers improved line regulation and an initial output voltage tolerance of $\pm 2\%$. These tightened specifications ease design and application problems several ways: safety margin is improved, error budgets on other parts of the system are expanded, and output voltage loss due to long supply runs can be better tolerated.

The LT1003 incorporates Linear Technology's advanced design, process and test techniques for improved quality and reliability over similar device types. Specifically, all devices are burned in by shorting the outputs, thereby forcing the regulator into its current limit and eventually, thermal limit mode. This ensures that all device protection features are working.

Standard 5 Volt Regulator



Load Regulation *

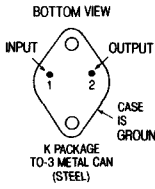


* The LT1003 has load compensation to cancel the effects of voltage loss in the output lead. This results in a nominal "zero" load regulation. The shaded band shows typical production spread.

ABSOLUTE MAXIMUM RATINGS

Input Voltage 20 Volts
 Power Dissipation Internally Limited
 Operating Junction Temperature Range
 LT1003M -55°C to 150°C
 LT1003C 0°C to 125°C
 Storage Temperature Range
 LT1003M -65°C to 150°C
 LT1003C -65°C to 150°C
 Lead Temperature (Soldering, 10 sec.) 300°C

PACKAGE/ORDER INFORMATION



BOTTOM VIEW

INPUT OUTPUT

1 2

CASE IS GROUND

K PACKAGE TO-3 METAL CAN (STEEL)

ORDER PART NO.

LT1003CK

LT1003MK

PRECONDITIONING

100% Burn-In in Thermal Limit

ELECTRICAL CHARACTERISTICS (See Note 1)

SYMBOL	PARAMETER	CONDITIONS	LT1003M			LT1003C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V _{OUT}	Output Voltage	T _J = 25°C, V _{IN} = 7.5V, I _{OUT} = 0	4.9	5.0	5.1	4.9	5.0	5.1	V
		7.5V ≤ V _{IN} ≤ 15V 0 ≤ I _{OUT} ≤ 5A, P ≤ 30W	● 4.8		5.2	4.8		5.2	V
$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	Line Regulation	T _J = 25°C, V _{IN} = 7.5V (See Note 1)		5	15		5	15	mV
$\frac{\Delta V_{OUT}}{\Delta I_{OUT}}$	Load Regulation	T _J = 25°C, V _{IN} = 7.5V 0 ≤ I _{OUT} ≤ 5A (See Note 1)		25	100		25	100	mV
	Thermal Regulation	T _J = 25°C, 20 msec pulse		0.005	0.02		0.005	0.02	%/W
I _Q	Quiescent Current	7.5V ≤ V _{IN} ≤ 15V, 0 ≤ I _{OUT} ≤ 5A	● 12	20		12	20		mA
e _n	Output Noise Voltage	T _J = 25°C, 10Hz ≤ f ≤ 100kHz		40			40		μV _{rms}
I _{SC}	Short Circuit Current Limit	T _J = 25°C, V _{IN} = 15V V _{IN} = 7.5V		5	8		5	8	A
				7	9		7	9	A
	Long Term Stability of Output Voltage			35		35		mV	
θ _{JC}	Thermal Resistance Junction to Case	K Package		1	1.5		1	1.5	°C/W

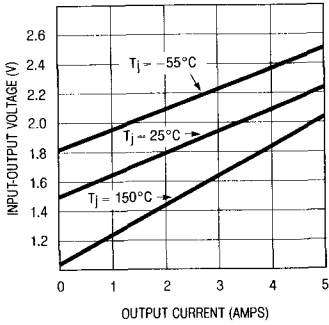
The ● denotes the specifications which apply over the full operating temperature range.

Note 1: Load and line regulation are tested with pulsed low duty cycle techniques where pulse width ≤ 1msec and duty cycle ≤ 5%.

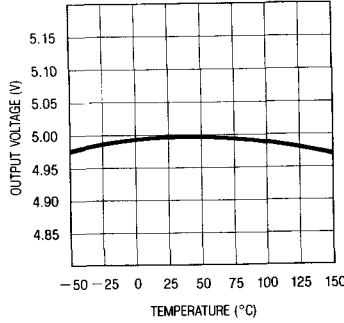
Note 2: T_{min} = -55°C for the LT1003MK and 0°C for LT1003CK.
 T_{max} = 150°C for LT1003MK and 125°C for LT1003CK.

TYPICAL PERFORMANCE CHARACTERISTICS

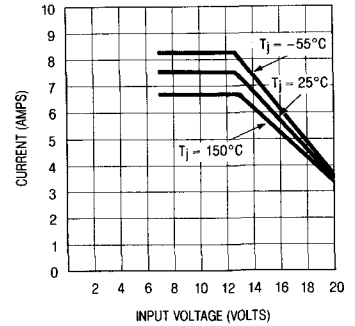
Minimum Input-Output Voltage Differential



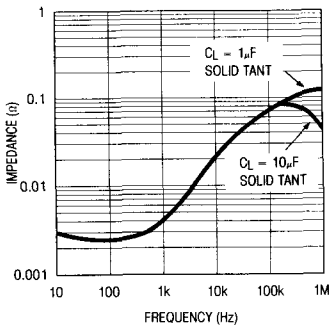
Output Voltage Temperature Drift



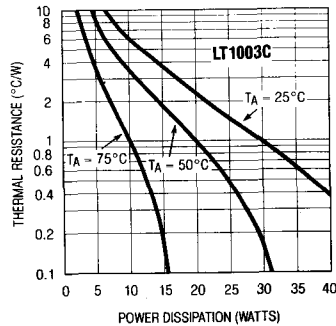
Peak Available Output Current



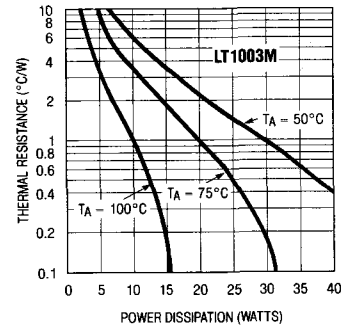
Output Impedance



Suggested Heat Sink Thermal Resistance (LT1003C)

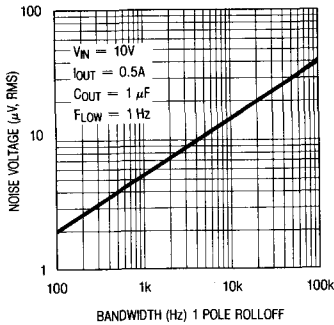


Suggested Heat Sink Thermal Resistance (LT1003M)

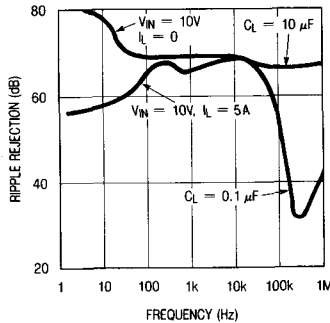


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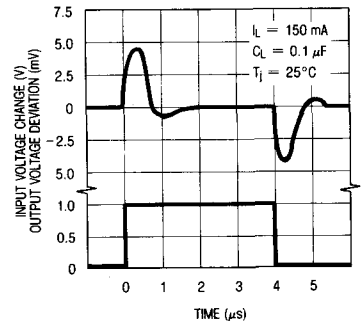
Output Noise Voltage



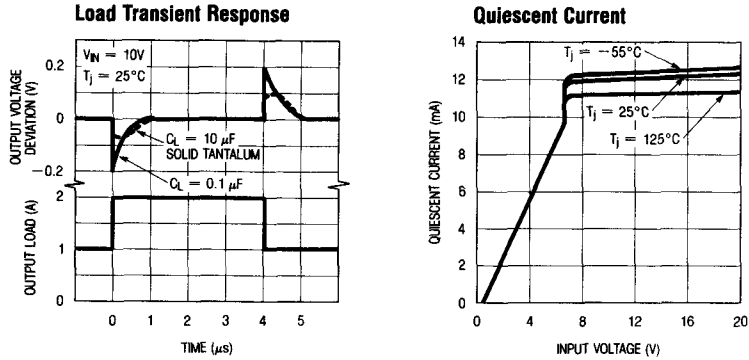
Ripple Rejection



Line Transient Response

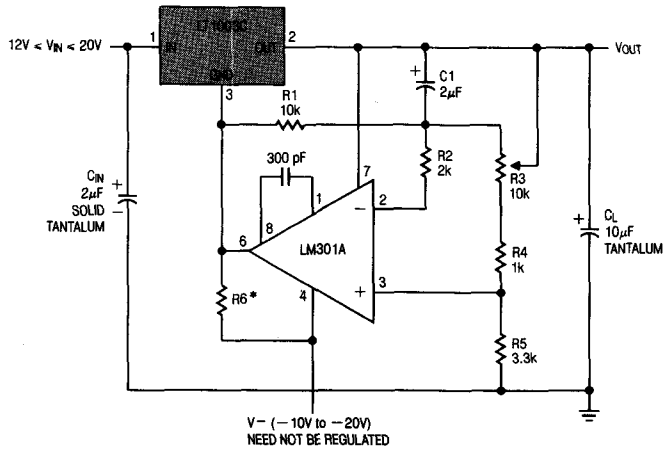


TYPICAL PERFORMANCE CHARACTERISTICS



TYPICAL APPLICATIONS

Adjustable Regulator 0-10V @ 5A

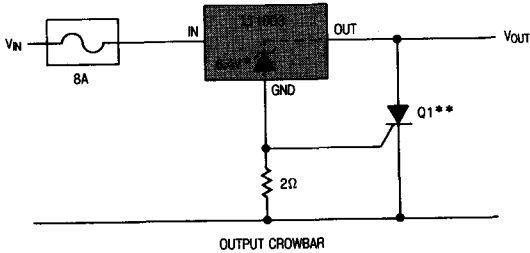


$$* R_6 = \frac{V^-}{12 \text{ mA}}$$

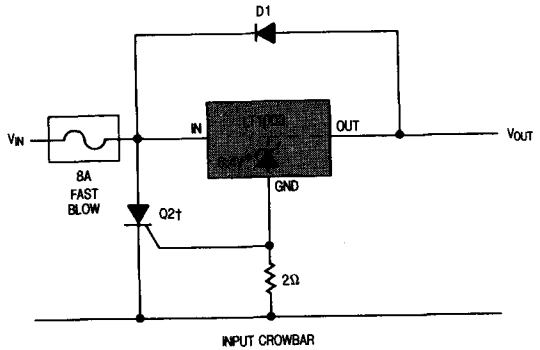
C_1 = OPTIONAL — IMPROVES RIPPLE REJECTION, NOISE AND TRANSIENT RESPONSE

TYPICAL APPLICATIONS

Crowbar Protection††



OUTPUT CROWBAR



INPUT CROWBAR

- * THE 6.4V ZENER IS INTERNAL TO THE LT1003.
- ** Q1 MUST BE ABLE TO WITHSTAND CONTINUOUS CURRENTS OF 8A IF ADDITIONAL SYSTEM SHUTDOWN IS NOT USED.

- † Q2 MUST WITHSTAND LARGE SURGE CURRENTS UNTIL THE 8A FUSE BLOWS. PEAK SURGE CURRENT IS LIMITED ONLY BY FUSE, WIRING, AND FILTER CAP RESISTANCE.

- †† TRIP POINT IS APPROXIMATELY 7.3V.

Bypass Capacitors

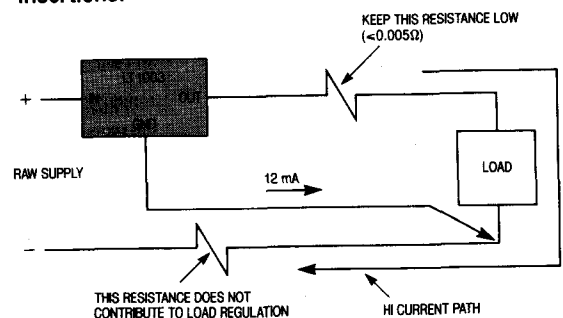
The LT1003 does not require an output capacitor for resistive loads. For almost all applications, however, a 1 μ F or larger solid tantalum capacitor is used on the output within 2" of the regulator. This greatly improves the output impedance of the regulator at high frequencies. For critical applications where very low impedance is required at high frequencies, a 10 μ F solid tantalum output capacitor is recommended. Total output capacitance may be increased without limit, either local or distributed.

A 2 μ F or larger input capacitor (solid tantalum) must be added if the regulator is more than 4" away from the large filter capacitor in the input supply. A 25 μ F aluminum capacitor may be substituted for the tantalum unit.

Avoiding Ground Loops

For best regulation, the ground pin of the LT1003 should be tied directly to the load point as shown below. This prevents excess drop in load voltage caused by load current flowing through the ground return lead. This is essentially a Kelvin connection for the

low side of the regulator. A Kelvin connection cannot be made for the high output of the regulator because only three pins are available on the package. Therefore, every attempt should be made to minimize the resistance between the output pin of the regulator and the load. #18 gauge hookup wire has a resistance of 0.006 ohms per foot. This translates to 0.6% change in load voltage at full load current. The LT1003 is specified at 2% maximum load regulation, so one foot of wire represents a significant loss of regulation. If connectors are used, careful consideration must be given to contact resistance, especially if the connector is subjected to nasty ambients, vibration, or multiple insertions.



TYPICAL APPLICATIONS

Raw Supply

Transformer, diode, and capacitor selection for the raw supply to the LT1003 is very important because of the conflicting requirements for reliability, efficiency, and resistance to "brown-out" conditions. High secondary voltage on the transformer will cause unnecessarily high power dissipation in the regulator. Too low a secondary voltage will cause the regulator output to drop out of regulation with only a small reduction in AC mains voltage. The following formula gives a good starting point for transformer selection. This formula assumes a full-wave center tapped transformer, using two rectifier diodes.

$$V_{RMS} = \left(\frac{V_{OUT} + V_{DO} + V_{RECT} + V_{RIP}}{\sqrt{2}} \right) \left(\frac{V_{NOM}}{V_{LOW}} \right) \quad (1.1^*)$$

(secondary
each side)

$$I_{RMS} = (I_{OUT}) \quad (1.2)$$

where:

$$V_{OUT} = 5V$$

$$V_{DO} = \text{Minimum input-output differential of the regulator}$$

*1.1 is a nominal load regulation factor for the transformer

$$V_{RECT} = \text{Rectifier forward drop at } 3I_{OUT}$$

$$V_{RIP} = \frac{1}{2} \text{ p-p capacitor ripple voltage}$$

$$V_{RIP} \approx \frac{(5.3 \times 10^{-3}) (I_{OUT})}{2C}$$

$$V_{NOM} = \text{Rated line voltage for the transformer (RMS)}$$

$$V_{LOW} = \text{Lowest expected line voltage (RMS)}$$

$$I_{OUT} = \text{DC output current}$$

$$\text{Example: } I_{OUT} = 4A, V_{OUT} = 5V$$

$$\text{Assume: } V_{DO} = 2.5V, V_{RECT} = 1.1V, C = 12,000\mu F$$

$$V_{NOM} = 115V, V_{LOW} = 105V$$

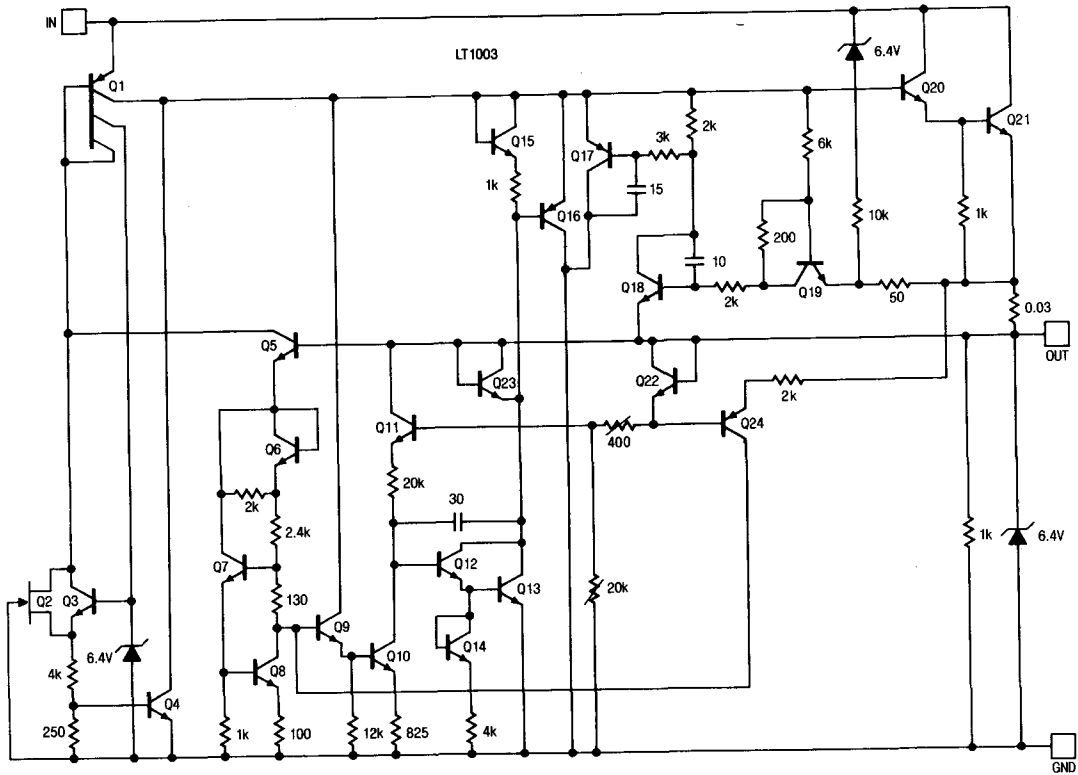
$$V_{RIP} = \frac{(5.3 \times 10^{-3}) (4)}{2 (12 \times 10^{-3})} = 0.88V$$

$$V_{RMS} = \left(\frac{5 + 2.5 + 1.1 + 0.88}{\sqrt{2}} \right) \left(\frac{115}{105} \right) \quad (1.1)$$

$$= 8.08 V_{RMS}$$

The filter capacitor should be at *least* 2000 μ F per amp of load current to minimize capacitor heating and ripple voltage. The diodes should be rated at 8–10 amps even though their average current is only 2.5A at full rated load current. The reason for this is that although the *average* current is 2.5A, the RMS current is typically twice this value. In addition, the diode must withstand very high surge currents during power turn-on. This surge can be 10–20 times the DC rating of the supply, depending on capacitor size and wiring resistance and inductance.

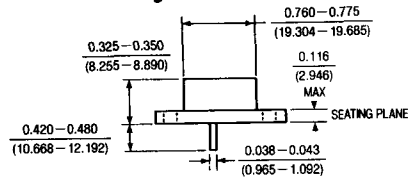
SCHEMATIC DIAGRAM



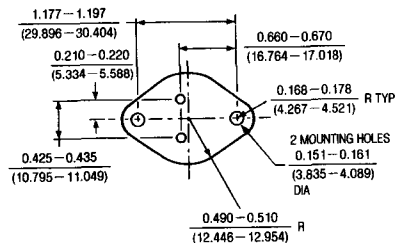
4

PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

K Package TO-3 STEEL Metal Can



	T _j max.	θ _{ja}	θ _{jc}
LT1003MK	150°C	35°C/W	1.5°C/W
LT1003CK	125°C	35°C/W	1.5°C/W



NOTES

FEATURES

- Two Regulated Outputs
 - +5V at 1 amp
 - +5V at 35mA
- 2% Output Voltage Tolerance
- 66 dB Ripple Rejection
- 0.5% Load Regulation
- TTL and CMOS Compatible Logic Control
- 100% Thermal Burn-in On All Devices

APPLICATIONS

- Power Supply Sequencing
- Remote On/Off Power Control
- Selective System Power During Emergency Power Operation
- Memory Power Supply With Back-Up

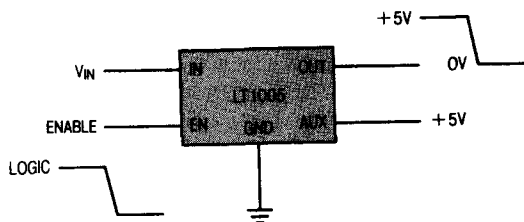
DESCRIPTION

The LT1005 features two positive 5 volt regulators in the same package. The main regulator offers excellent performance while supplying load currents up to 1 amp, and the auxiliary regulator provides similar performance while supplying lighter loads of 35mA. The main regulator has the additional feature of being under the shutdown control of a logic signal. When the enable pin is taken to a low logic level, the main regulator shuts down and its output voltage goes to near zero volts. During this command, the auxiliary output is unaffected by the main regulator's condition and continues to provide a 5 volt output.

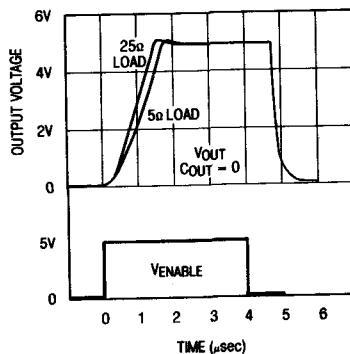
The main output has current and power limiting combined with thermal shutdown to make it virtually blow-out proof. The auxiliary output is not affected by the thermal shutdown mechanism or the state of the main output, allowing it to be used as a back-up in case of overloads or shorts on the main supply.

The logic input of the LT1005 (enable pin) has a 1.6V threshold and can be driven from a high source impedance. This allows it to be driven by most logic families, including TTL & CMOS.

Functional Diagram



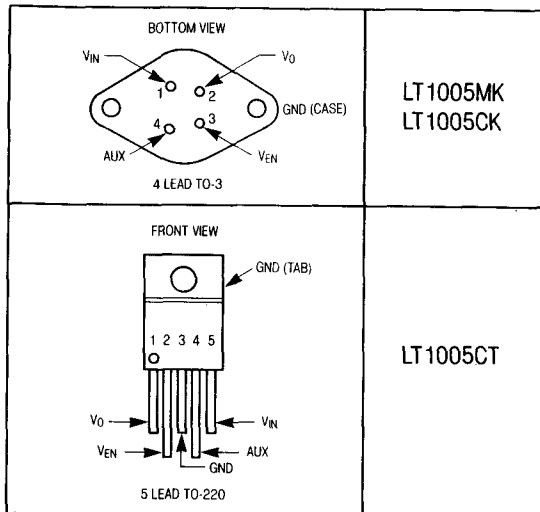
Switching Characteristics



ABSOLUTE MAXIMUM RATINGS

Power Dissipation Internally Limited
 Input Voltage (V_{IN}) 20V
 Enable Voltage (V_{EN}) 20V
 Operating Junction Temperature
 LT1005M -55°C to 150°C
 LT1005C 0°C to 125°C
 Storage -65°C to 150°C
 Lead Temperature (Soldering, 10 sec.) 300°C

PACKAGE/ORDER INFORMATION



PRECONDITIONING:

100% Burn-in in thermal limit

ELECTRICAL CHARACTERISTICS — MAIN REGULATOR (See Note 1)

SYMBOL	PARAMETER	CONDITIONS	LT1005M			LT1005C			UNITS	
			MIN	TYP	MAX	MIN	TYP	MAX		
V_0	Output Voltage	$T_j = 25^\circ\text{C}$	4.9	5.0	5.1	4.9	5.0	5.1	V	
		High $7.4\text{V} \leq V_{IN} \leq 20\text{V}$ $P_d \leq 10\text{W}$ $0\text{mA} \leq I_0 \leq 1\text{A}$	●	4.8	5.0	5.2	4.8	5.0	5.2	V
		Low $7.2\text{V} \leq V_{IN} \leq 20\text{V}$ $I_0 = 0$	●		0.1	0.3		0.1	0.3	V
$\frac{\Delta V_0}{\Delta I_0}$	Load Regulation	$7.5\text{V} \leq V_{IN} \leq 15\text{V}$ $0\text{mA} \leq I_0 \leq 1\text{A}$ (Note 2)	●	5	25		5	25	mV	
$\frac{\Delta V_0}{\Delta V_{IN}}$	Line Regulation	$7.4\text{V} \leq V_{IN} \leq 20\text{V}$ (Note 2)		0.3	2		0.3	2	mV/V	
	Ripple Rejection	$50\text{Hz} \leq f \leq 500\text{Hz}$		66			66		dB	
	Thermal Regulation	$\Delta P_d \leq 10\text{W}$ (Note 4)		0.005	0.02		0.005	0.02	%/W	
I_0	Available Load Current	$7.4\text{V} \leq V_{IN} \leq 15\text{V}$ $V_{IN} = 20\text{V}$	1	1.7		1	1.7		A	
			0.7	1.3		0.7	1.0		A	
I_{sc}	Short Circuit Current	$7.0\text{V} \leq V_{IN} \leq 15\text{V}$ $V_{IN} = 20\text{V}$		1.5	2.5		1.5	2.5	A	
				1.2	2.0		1.2	2.0	A	
V_{IN}	Minimum Input Voltage to Maintain Regulation	(Note 5) $I_0 = 0.2\text{A}$	●	7.0	6.5		6.9	6.5	V	
		$I_0 = 1.0\text{A}$	●	7.5	7.0		7.5	7.0	V	
I_0	Quiescent Current	Output High		2	4		2	4	mA	
		Output Low		1.5	3		1.5	4	mA	
θ_{JC}	Thermal Resistance Junction to Case	TO-3		3	4		3	4	$^\circ\text{C}/\text{W}$	
		TO-220					3	5	$^\circ\text{C}/\text{W}$	

ELECTRICAL CHARACTERISTICS — AUXILIARY REGULATOR (See Note 1)

SYMBOL	PARAMETER	CONDITIONS	LT1005M			LT1005C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_O	Output Voltage	$T_j = 25^\circ\text{C}$	4.9	5.0	5.1	4.9	5.0	5.1	V
		$7.0\text{V} \leq V_{IN} \leq 20\text{V}$ $0\text{mA} \leq I_O \leq 35\text{mA}$	● 4.8	5.0	5.2	4.8	5.0	5.2	V
$\frac{\Delta V_O}{\Delta I_O}$	Load Regulation	$7.0\text{V} \leq V_{IN} \leq 20\text{V}$ $0\text{mA} \leq I_O \leq 35\text{mA}$ (Note 2)	●	5	15	5	15	mV	
$\frac{\Delta V_O}{\Delta V_{IN}}$	Line Regulation	$7.0\text{V} \leq V_{IN} \leq 20\text{V}$ (Note 2)		0.2	1	0.2	1	mV/V	
	Ripple Rejection	$50\text{Hz} \leq f \leq 500\text{Hz}$		74		74		dB	
I_{SC}	Short Circuit Current	$7.0\text{V} \leq V_{IN} \leq 20\text{V}$		90	150	90	150	mA	
V_{IN}	Minimum Input Voltage to Maintain Regulation	(Note 5) $I_O = 1\text{mA}$	● 6.5	6.1		6.5	6.1	V	
		$I_O = 35\text{mA}$	● 6.9	6.5		6.9	6.5	V	

4

ELECTRICAL CHARACTERISTICS — LOGIC CONTROL (See Note 1)

SYMBOL	PARAMETER	CONDITIONS	LT1005M			LT1005C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{EN}	Enable Threshold Voltage	$7.0\text{V} \leq V_{IN} \leq 20\text{V}$ $T_j = 25^\circ\text{C}$	● 1.45	1.6	1.75	1.45	1.6	1.75	V
			1.3	1.6	1.85	1.3	1.6	1.85	V
	Enable Pin Current	$V_{EN} \leq 1\text{V}$ (See Note 3)		0	150	0		150	μA
		$V_{EN} \geq 2.4\text{V}$		0	1	0	1	μA	

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: Unless otherwise indicated, these specifications apply for $V_{IN} = 10\text{V}$, $I_O = 0\text{mA}$, and $T_j = 25^\circ\text{C}$.

Note 2: Line and load regulation are measured using a low duty cycle pulse, causing little change in the junction temperature. Effects due to thermal gradients and device heating must be taken into account separately.

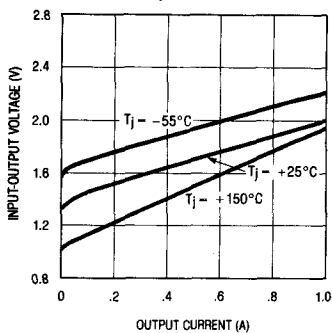
Note 3: When the enable pin is at a low logic level, current flows out of the enable pin.

Note 4: Pulse length for this measurement is 20msec.

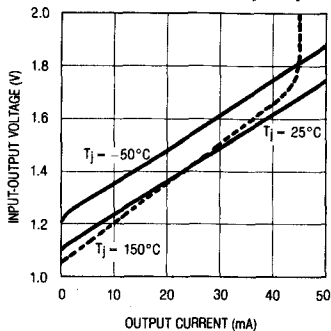
Note 5: Input Voltage is reduced until output drops by 100mV from its initial value.

TYPICAL PERFORMANCE CHARACTERISTICS

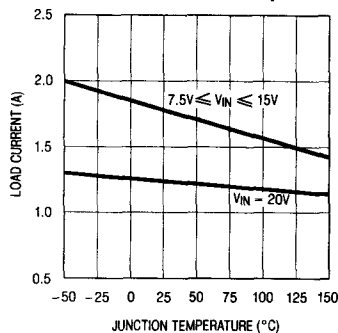
Minimum Input-Output Differential of Main Output



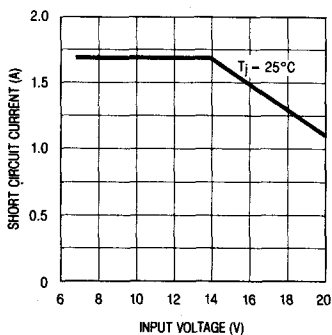
Minimum Input-Output Differential of Auxiliary Output



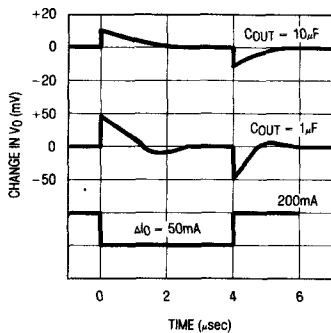
Maximum Available Load Current—Main Output



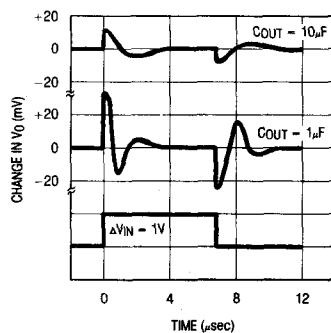
Short Circuit Output Current



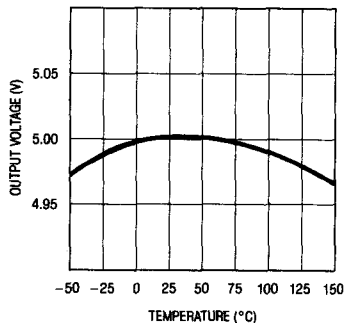
Load Transient Response of Main Output



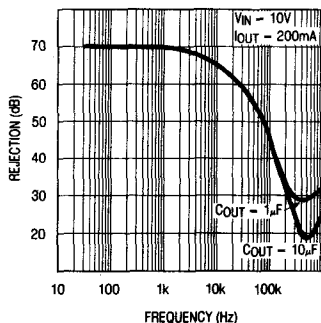
Line Transient Response of Main Output



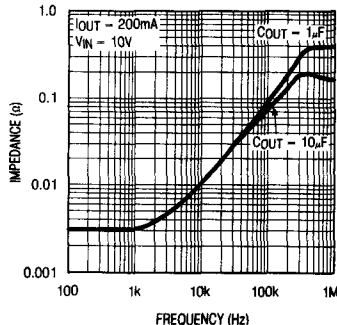
Output Voltage as Function of Temperature



Ripple Rejection

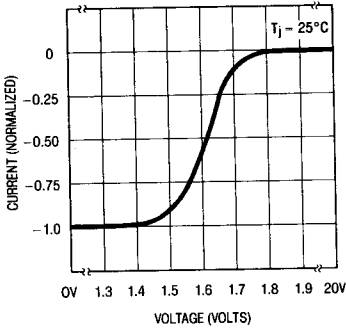


Output Impedance

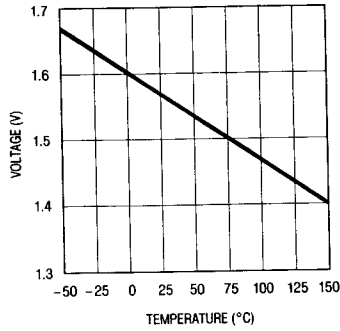


TYPICAL PERFORMANCE CHARACTERISTICS

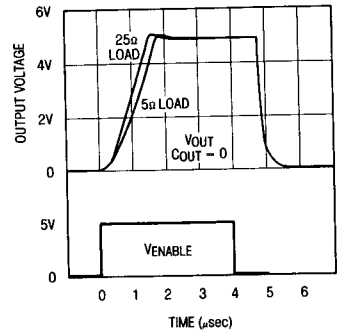
Enable Pin Characteristics



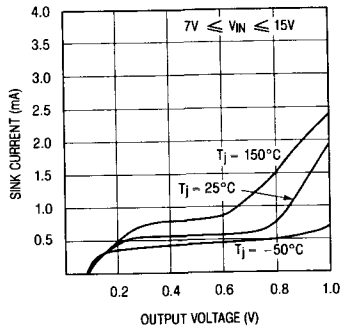
Enable Threshold



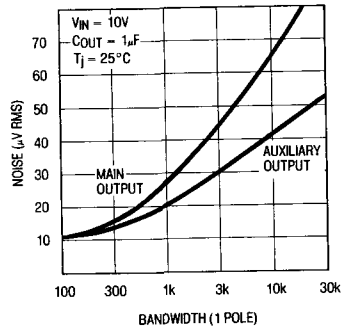
Switching Characteristics



Output Characteristics in Low State



Output Noise



APPLICATIONS INFORMATION

General Information

The LT1005 is a dual output 5V regulator. The main output is capable of delivering up to 1 amp of load current and can be shut down with a logic signal. The auxiliary output supplies a minimum of 35mA and is unaffected by the logic signal. The outputs are trimmed to $\pm 2\%$ initial tolerance and exhibit excellent line and load regulation.

The logic control feature makes the LT1005 ideal for many system applications where it is desirable to power up a portion of the system for a period of time and then power the system down during a standby operation. As an example, the LT1005 could be used to activate various memory space locations only as needed, thus saving substantial power dissipation and other cooling costs. The LT1005 could also be used to power micro-computers, such as the 8048 series. The auxiliary supply can be used for RAM keep-alive during power down operation. Additional power savings can be accomplished by using the LT1005 to power PROM, EPROM, and E²PROM devices. During program load, or look-up table operations the ROM type device can be activated and its' contents placed in RAM, and then the ROM power can be removed. Or for high speed but low power data acquisition systems, the power could be applied to fast memory, then the data transferred to CMOS memory. The main regulator can then be shutdown and the CMOS memory can be powered by the auxiliary for lower power dissipation. Other applications, such as multiple power supply sequencing, elimination of expensive AC and DC power switches, delayed start applications, switching 5V DC loads, and many others are now easily accomplished.

Timing functions can also be performed directly at the enable pin, such as delayed power-up or power-down.

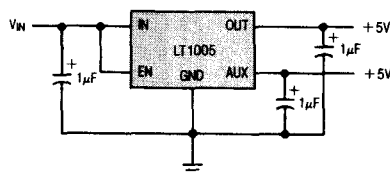
Because a logic low on the enable pin shuts down the main regulator, feedback from output to enable can be used to generate hysteresis or latching functions.

The low quiescent current drain of the LT1005 makes it useful in battery powered or battery back-up appli-

cations. The enable pin can be used as a "low battery" detector or to shut down major portions of system power, allowing memory portions to continue to operate from the auxiliary output. At low output currents, the auxiliary output will regulate with input voltage typically as low as 6.1V, giving maximum battery life.

Good design practice with all regulators is to bypass the input and output terminals. A 1 μ F solid tantalum at the input and at both outputs is suggested. For the applications which follow, the bypass capacitors are still recommended, but are not shown on the diagram for simplicity. It is also recommended that for maximum noise immunity, the voltage enable pin be tied high if it is unused. It can be tied directly to V_{IN} as shown in Figure 1, or to the auxiliary output. If the enable pin is left open, it will float to a high logic level of approximately 1.6V and the main output regulator will be at 5V.

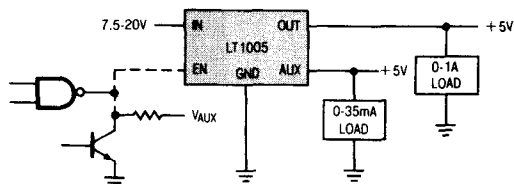
Figure 1.



The enable pin is fully protected against input voltages up to 20 volts, even if the power input voltage is zero.

The basic shutdown control circuit uses a direct gate drive or an open collector driver and a pull-up resistor which is tied to V_{AUX} as shown in Figure 2.

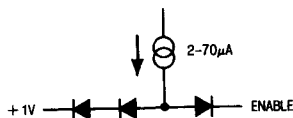
Figure 2.



Driving the Enable Pin

The enable pin equivalent schematic is shown in Fig. 3. Basically, enable pin current is zero above the threshold, and between 2 and 70 μ A below the threshold, flowing out of the pin. Standard logic, such as TTL & CMOS will interface directly to the enable pin, even if the logic output swing is higher than the input voltage (V_{IN}) to the regulator. 15V CMOS can be used to drive the enable pin even if the regulator is not powered up, without loading the CMOS output.

Figure 3.



Timing functions, such as delayed power-up or power-down can be implemented by driving the enable pin with an RC network. The current flowing out of the enable pin should not be used as the timing current in delayed power up applications, as it is temperature sensitive and varies somewhat from device to device. Instead, a resistor tied to the auxiliary output, the input, or to a logic signal should be used. The timing resistor chosen should provide at least 500 μ A of current to "swamp-out" the effects of the internal current.

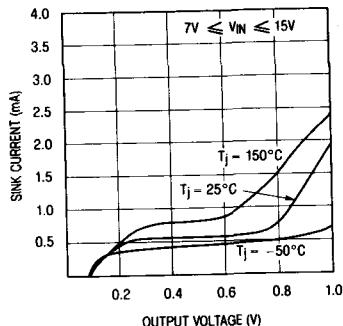
Main Output Current/Voltage Characteristics

Following a high to low transition at the enable pin, the main regulator output will begin to drop after a delay of approximately 1 μ sec. With no capacitive load, the output will fall to zero in approximately 0.5 μ sec ($R_L = 5-100\Omega$). With a capacitive load, fall time is limited by the RC product of the load and the output capacitance. For light loads ($R_L > 100\Omega$), the discharge time is controlled by an internal equivalent load of 200 Ω for output voltages down to 1 volt. Below 1 volt, the output decays linearly, with a slope equivalent to the load capacitance and a pull down current of approximately 0.5mA. The DC output voltage in the shutdown mode is approximately 0.1 volt for input voltages (V_{IN}) up to

15V. If V_{IN} is 20V, the output during shutdown will be approximately 0.2V due to an internal current path in the regulator (see Figure 4).

Figure 4.

Output Characteristics in Low State



The user should note that the output in the low state can only sink about 0.5mA. If current is forced into the output, the output voltage will rise to 0.8V at 1mA and above 1V at 10mA. With no output capacitor, the rise time of the main output is about 1.5 μ s. With an output capacitor, rise time is limited by the short circuit current of the LT1005 and the load capacitance; $t_r \approx (C)(5V)/(1.5A)$. A 1 μ F output capacitor slows the output rise time to approximately 3 μ s and a 10 μ F output capacitor slows the output rise time to 30 μ s.

Output Current

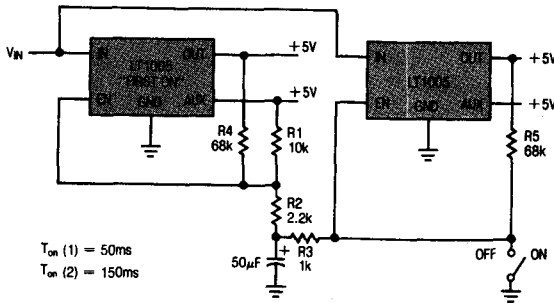
The main output current limits at about 1.7A for input voltages below 19V. Internal foldback, or "power limiting" circuitry detects the input-output voltage differential and reduces current limit for input to output voltages exceeding 14V. With 20V input, for instance, short circuit current is reduced to $\approx 1.1A$.

An additional feature of the LT1005 is that the auxiliary supply does not incorporate nor is it affected by thermal shutdown. Any fault condition of the main regulator will not affect the auxiliary output voltage.

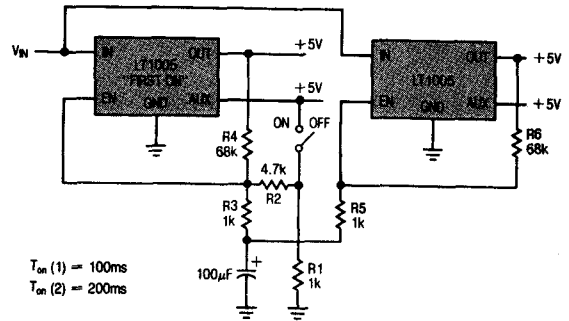
The following applications circuits will serve to indicate the versatility of the LT1005.

TYPICAL APPLICATIONS

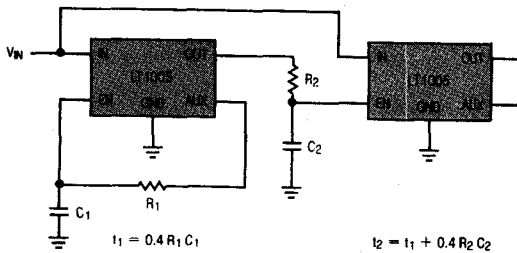
First-On, Last-Off Sequencing



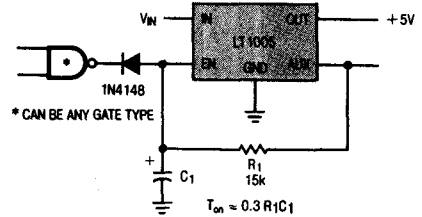
First-On, First-Off Sequencing



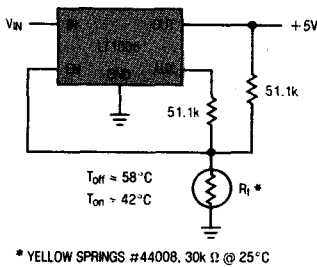
Power Supply Turn-On Sequencing



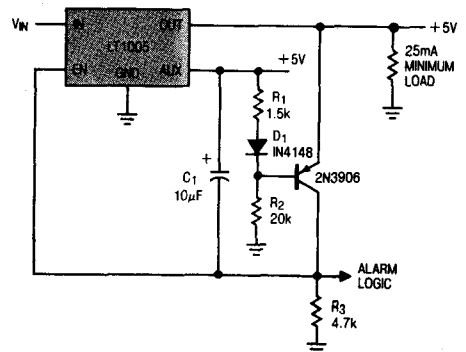
Fast Turn-Off, Delayed Turn-On



Thermal Cutoff at High Ambient Temperature

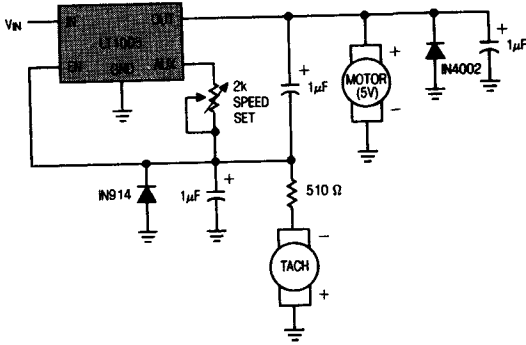


Latch-Off for $V_{OUT} \leq 4.7\text{V}$

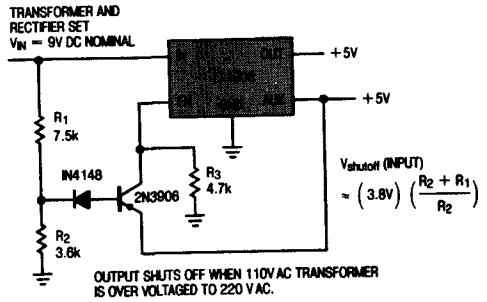


TYPICAL APPLICATIONS

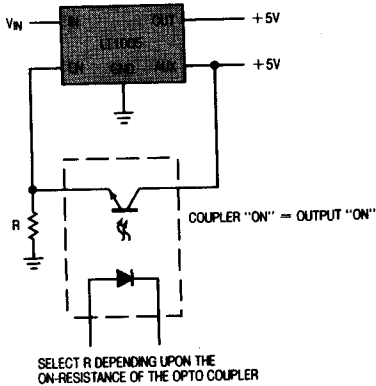
Proportional Motor Speed Controller



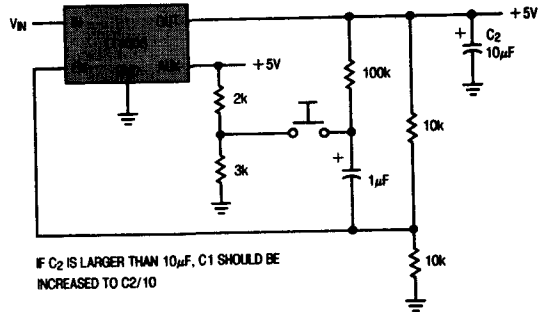
High Input Voltage Detection



Opto-Coupled Output Control

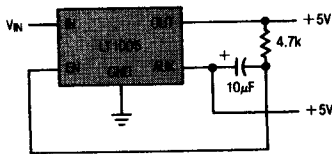


Push-On, Push-Off

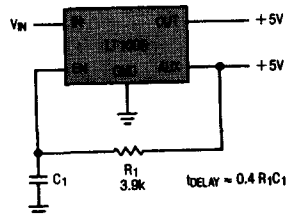


4

Latch-Off When Output Short

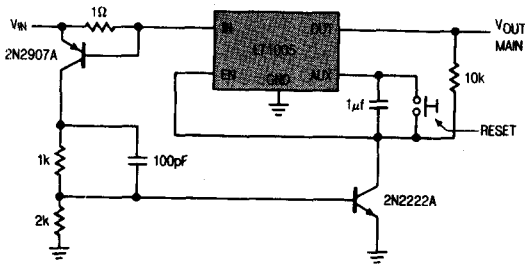


Delayed Power Up

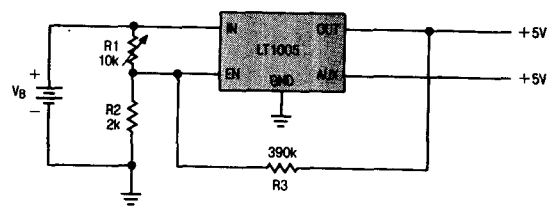


TYPICAL APPLICATIONS

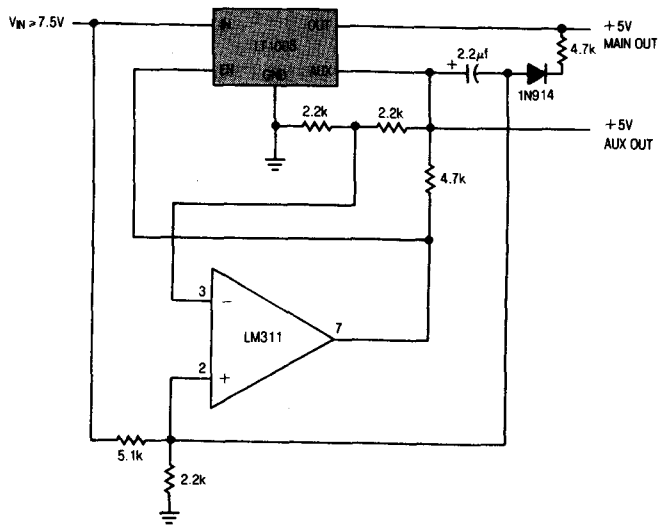
Fast Electronic Circuit Breaker



Battery Voltage Sensing Circuit



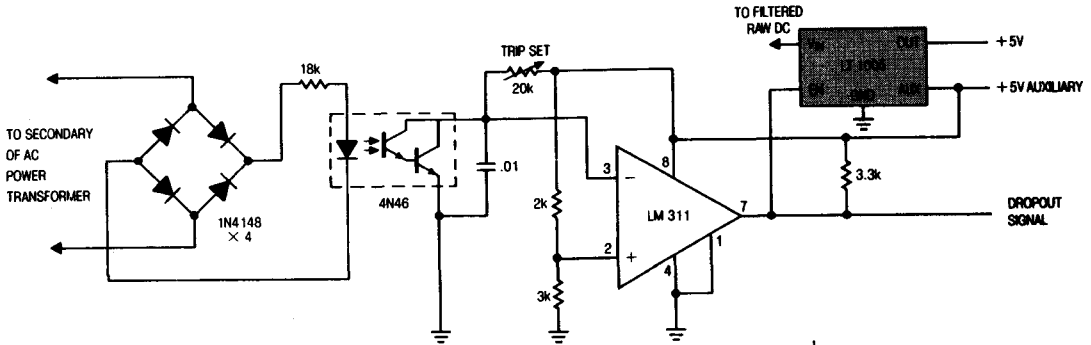
Memory Save-on-Power-Down



The auxiliary output powers the memory, while the main output powers the system and is connected to the memory store pin. When power goes down, the main output goes low, commanding the memory to store. The auxiliary output then drops out.

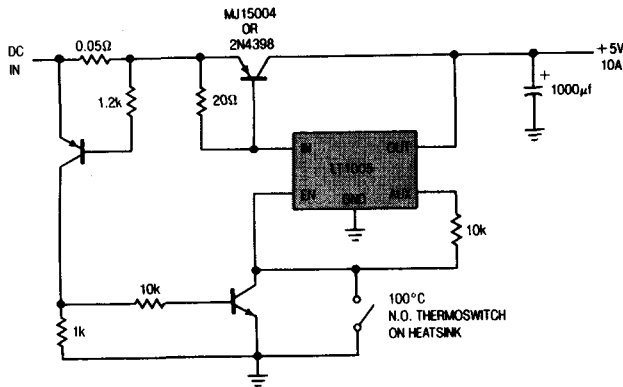
TYPICAL APPLICATIONS

Line Dropout Detector

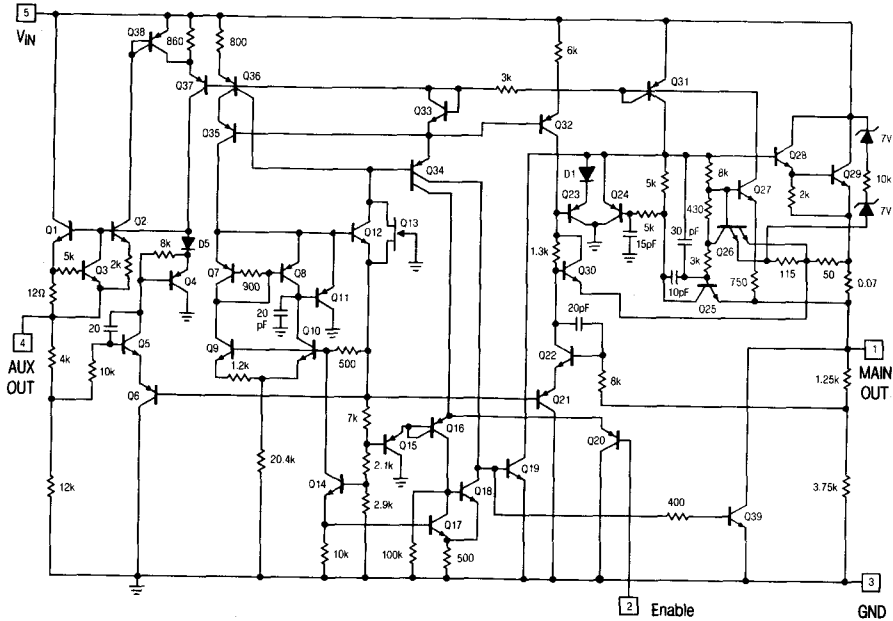


4

10 Amp Regulator with Current and Thermal Protection

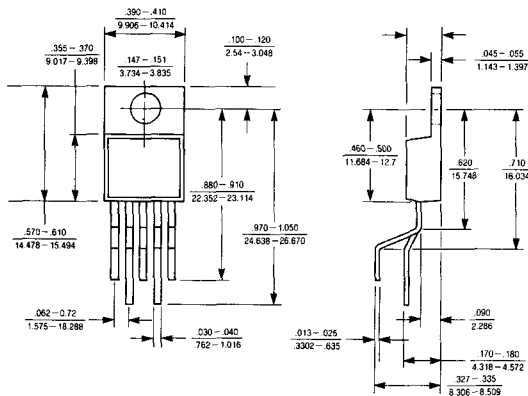


SCHEMATIC DIAGRAM

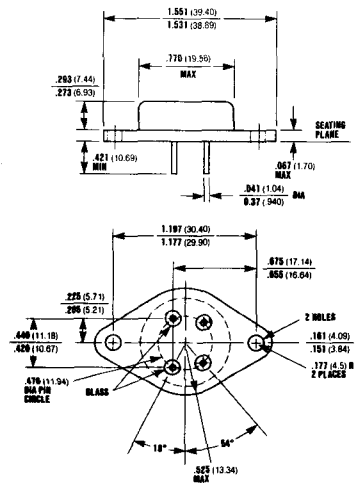


PACKAGE DESCRIPTION

TO-220 PACKAGE (5 LEAD)



4-Pin Metal Package Similar to JEDEC TO-3



All dimensions in inches bold and millimeters (parentheses)

	T _{JMAX}	θ _{JC}
LT1005C	125°C	5°C/W

	T _{JMAX}	θ _{JC}
LT1005M	150°C	4°C/W
LT1005C	125°C	4°C/W

FEATURES

- 40 μ A Supply Current
- 125mA Output Current
- 2.5V Reference Voltage
- Reference Output Sources 1mA and Sinks 0.5mA
- Dual Output Comparator
- Comparator Sinks 10mA
- Dropout Detector
- 0.2V Dropout Voltage
- Thermal Limiting
- Available in SO Package

APPLICATIONS

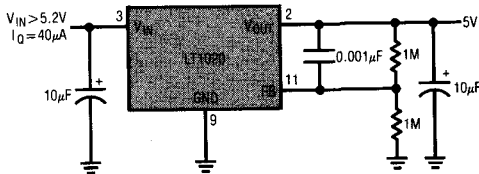
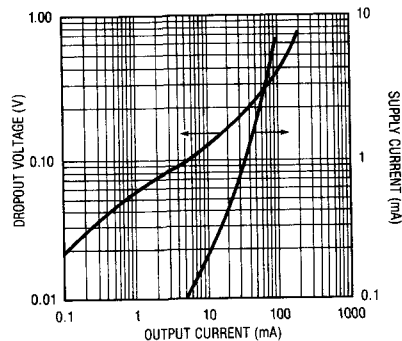
- Battery Systems
- Battery Backup System
- Portable Terminals
- Portable Instruments

DESCRIPTION

The LT1020 is a combination micropower positive regulator and free collector comparator on a single monolithic chip. With only 40 μ A supply current, the LT1020 can supply over 125mA of output current. Input voltage range is from 4.5V to 36V and dropout voltage is 0.6V at 125mA. Dropout voltage decreases with lower load currents. Also included on the chip is a class B output 2.5V reference that can either source or sink current. A dropout detector provides an output current to indicate when the regulator is about to drop out of regulation.

The dual output comparator can be used as a comparator for system or battery monitoring. For example, the comparator can be used to warn of low system voltage while the dropout detector shuts down the system to prevent abnormal operation. Frequency compensation of the comparator for amplifier applications can be obtained by adding external output capacitance. Dual output or positive and negative regulators can also be made.

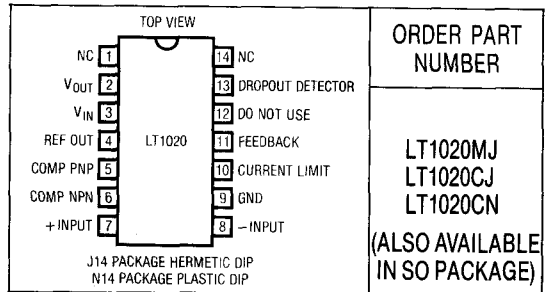
The 2.5V reference will source or sink current. This allows it to be used as a supply splitter or auxiliary output.

4
5V Regulator

Dropout Voltage and Supply Current


ABSOLUTE MAXIMUM RATINGS

Input Voltage	36V
NPN Collector Voltage	36V
PNP Collector Voltage	Supply – 36V
Output Short Circuit Duration	Indefinite
Power Dissipation	Internally Limited
Operating Temperature Range	
LT1020C	0°C to 100°C
LT1020M	– 55°C to 125°C
Storage Temperature Range	
LT1020C,M	– 65°C to 150°C

PACKAGE/ORDER INFORMATION



ELECTRICAL CHARACTERISTICS $T_j = 25^\circ\text{C}$

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Reference					
Reference Voltage	$4.5\text{V} \leq V_{IN} \leq 36\text{V}$	2.46	2.50	2.54	V
Line Regulation	$4.5\text{V} \leq V_{IN} \leq 36\text{V}$		0.01	0.015	%/V
Load Regulation	$-0.5\text{mA} \leq I_{REF} \leq 1\text{mA}, V_{IN} = 12\text{V}$		0.2	0.3	%
Output Source Current	$V_{IN} = 5\text{V}$	1	4		mA
Output Sink Current	$V_{IN} = 5\text{V}$	0.5	2		mA
Temperature Stability			1		%
Regulator					
Supply Current	$V_{IN} = 6\text{V}, I_{OUT} \leq 100\mu\text{A}$ $V_{IN} = 36\text{V}, I_{OUT} \leq 100\mu\text{A}$ $V_{IN} = 12\text{V}, I_{OUT} = 125\text{mA}$		45 75 11	80 120 20	μA
Output Current	$(V_{IN} - V_{OUT}) \geq 1\text{V}, V_{IN} \geq 6\text{V}$	125			mA
Load Regulation	$(V_{IN} - V_{OUT}) \geq 1\text{V}, V_{IN} \geq 6\text{V}$		0.2	0.5	%
Line Regulation	$6\text{V} \leq V_{IN} \leq 36\text{V}$		0.01	0.015	%/V
Dropout Voltage	$I_{OUT} = 100\mu\text{A}$ $I_{OUT} = 125\text{mA}$		0.02 0.4	0.05 0.65	V
Feedback Sense Voltage	$V_{IN} = 12\text{V}$	2.44	2.5	2.56	V
Dropout Detector Current	$\Delta V_{OUT} = -0.05\text{V}$	3	20		μA
Feedback Bias Current			15	40	nA
Minimum Load Current	$V_{IN} = 36\text{V}$		1	5	μA
Short Circuit Current	$V_{IN} = 36\text{V}$ Pin 9 and Pin 10 shorted, $V_{IN} = 4.5\text{V}$	3	250 30	360	mA
Comparator					
Offset Voltage	$0\text{V} \leq V_{CM} \leq 35\text{V}, V_{IN} = 36\text{V}$		3	7	mV
Bias Current	$0\text{V} \leq V_{CM} \leq 35\text{V}, V_{IN} = 36\text{V}$		15	40	nA
Offset Current	$0\text{V} \leq V_{CM} \leq 35\text{V}, V_{IN} = 36\text{V}$		4	15	nA
Gain-NPN Pulldown	$\Delta V_{OUT} = 29\text{V}, R_L = 20\text{k}$	2000	10000		V/V
Common Mode Rejection	$0\text{V} \leq V_{CM} \leq 35\text{V}, V_{IN} = 36\text{V}$	80	94		dB

ELECTRICAL CHARACTERISTICS

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Comparator					
Power Supply Rejection	$4.5V \leq V_S \leq 36V$	80	96		dB
Output Sink Current	$V_{IN} = 4.5V$	10	18		mA
NPN Saturation Voltage	$I_{OUT} = 1mA$		0.4	0.6	V
Output Source Current		60	200		μA
Input Voltage Range		0		$V_{IN} - 1$	V
Response Time			5		μS
Leakage Current (NPN)				2	μA

ELECTRICAL CHARACTERISTICS

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Reference					
Reference Voltage	$4.5V \leq V_{IN} \leq 36V$	● 2.40	2.50	2.55	V
Line Regulation	$4.5V \leq V_{IN} \leq 36V$	●	0.01	0.02	%/V
Load Regulation	$-0.5mA \leq I_{REF} \leq 1mA, V_{IN} = 12V$	●	0.3	0.4	%
Output Source Current	$V_{IN} = 5V$	● 1			mA
Output Sink Current	$V_{IN} = 5V$	● 0.5			mA
Regulator					
Supply Current	$V_{IN} = 6V, I_{OUT} \leq 100\mu A$	●		65	μA
	$V_{IN} = 36V, I_{OUT} \leq 100\mu A$	●		85	μA
	$V_{IN} = 12V, I_{OUT} = 125mA$	●		11	20
Output Current	$(V_{IN} - V_{OUT}) \geq 1V, V_{IN} \geq 6V$	● 125			mA
Load Regulation	$(V_{IN} - V_{OUT}) \geq 1V, V_{IN} \geq 6V$	●		1	%
Line Regulation	$6V \leq V_{IN} \leq 36V$	●		0.02	%/V
Dropout Voltage	$I_{OUT} = 100\mu A$	●		0.06	V
	$I_{OUT} = 125mA$	●		0.85	V
Feedback Sense Voltage	$V_{IN} = 12V$	● 2.38	2.5	2.57	V
Dropout Detector Current	$\Delta V_{OUT} = -0.05V$	● 3			μA
Feedback Bias Current		●		50	nA
Minimum Load Current	$V_{IN} = 36V$	●		50	μA
Short Circuit Current	$V_{IN} = 36V$	●	240	360	mA
	Pin 9 and Pin 10 shorted, $V_{IN} = 4.5V$	● 2.5	30		mA
Comparator					
Offset Voltage	$0V \leq V_{CM} \leq 35V, V_{IN} = 36V$	●		10	mV
Bias Current	$0V \leq V_{CM} \leq 35V, V_{IN} = 36V$ (Note 1)	●	15	60	nA
Offset Current	$0V \leq V_{CM} \leq 35V, V_{IN} = 36V$	●		20	nA
Gain-NPN Pulldown	$\Delta V_{OUT} = 29V, R_L = 20k$	● 1000			V/V
Common Mode Rejection	$0V \leq V_{CM} \leq 35V, V_{IN} = 36V$	● 80			dB
Power Supply Rejection	$4.5V \leq V_S \leq 36V$	● 80			dB
Output Sink Current	$V_{IN} = 4.5V$ (Note 2)	● 5	10		mA
Output Source Current		● 40	120		μA
Input Voltage Range		● 0		$V_{IN} - 1$	V
Leakage Current (NPN)	$V_{IN} = 36V$	●		8	μA

The ● denotes the specifications which apply over full operating temperature range.

Note 1: For $0V \leq V_{CM} \leq 0.1V$ and $T > 85^\circ C$ I bias max is 100nA.

Note 2: For $T_A \leq -40^\circ C$ output sink current min is 2.5mA.

PIN FUNCTIONS

Pins 1, 12, 14—No internal connection.

Pin 2—**Regulator Output.** Main output, requires 10 μ F output capacitor. Can be shorted to V_{IN} or ground without damaging device.

Pin 3—**Input Supply.** Bypass with 10 μ F cap. Must always be more positive than ground.

Pin 4—**Reference.** 2.5V can source or sink current. May be shorted to ground or up to 5V. Voltages in excess of 5V can damage the device.

Pin 5—**Comparator PNP Output.** Pull up current source for the comparator. May be connected to any voltage from V_{IN} to 36V more negative than V_{IN} (operates below ground). Short circuit protected. For example, if V_{IN} is 6V then pin 5 will operate to -30V.

Pin 6—**Comparator NPN Output.** May be connected to any voltage from ground to 36V more positive than ground (operates above V_{IN}). Short circuit protected.

Pins 7, 8—**Comparator Inputs.** Operates from ground to $V_{IN} - 1V$. Comparator inputs will withstand 36V even with V_{IN} of 0V.

Pin 9—**Ground.**

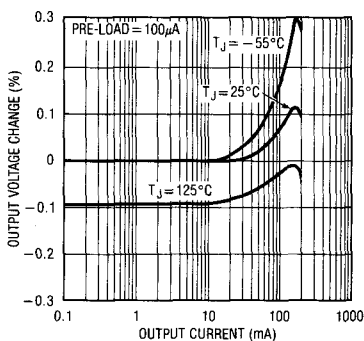
Pin 10—**Current Limit.** Connecting this pin to ground decreases the regulator current limit to 3mA min. Leave open when not used.

Pin 11—**Feedback.** This is the feedback point of the regulator. When operating, it is nominally at 2.5V. Optimum source resistance is 200k to 500k. The feedback pin should not be driven below ground or more positive than 5V.

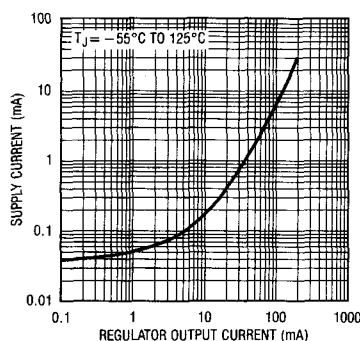
Pin 13—**Dropout Detector.** This pin acts like a current source from V_{IN} which turns on when the output transistor goes into saturation. The magnitude of the current depends on the magnitude of the output current and the input-output voltage differential. Pin current ranges from 5 μ A to about 300 μ A.

TYPICAL PERFORMANCE CHARACTERISTICS

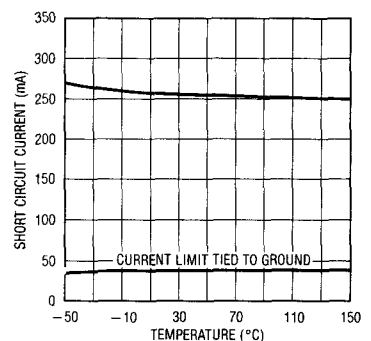
Regulator Load Regulation



Supply Current

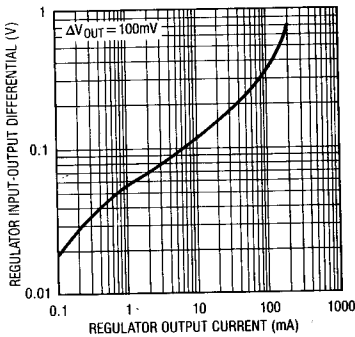


Regulator Short Circuit Current

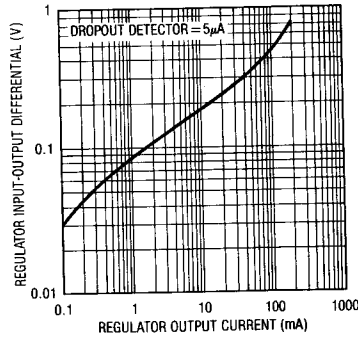


TYPICAL PERFORMANCE CHARACTERISTICS

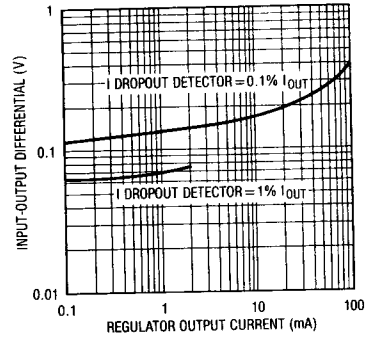
Dropout Voltage



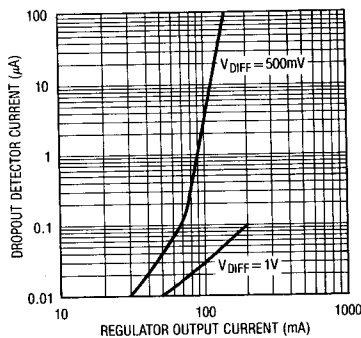
Dropout Voltage



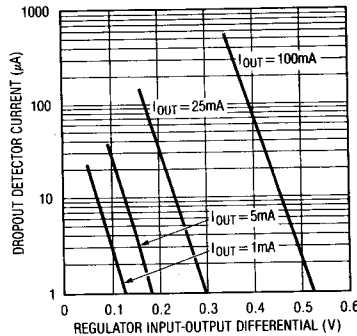
Dropout Voltage



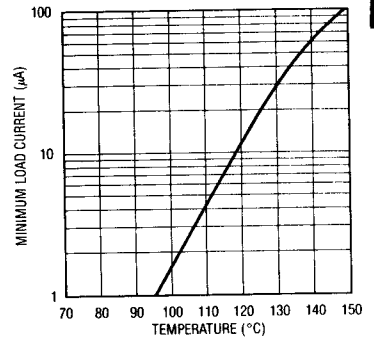
Dropout Detector Current



Dropout Detector Current

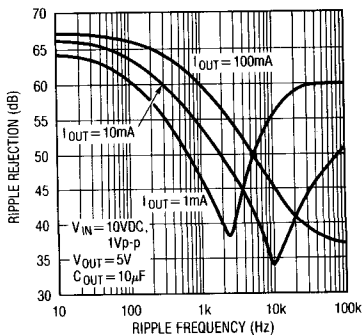


Regulator Minimum Load Current

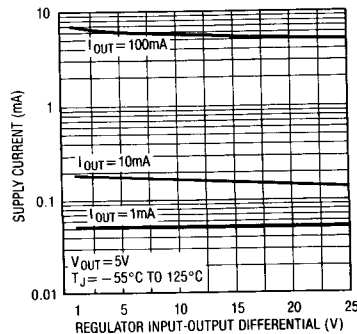


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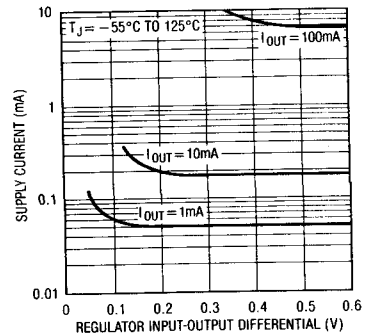
Regulator Ripple Rejection



Supply Current

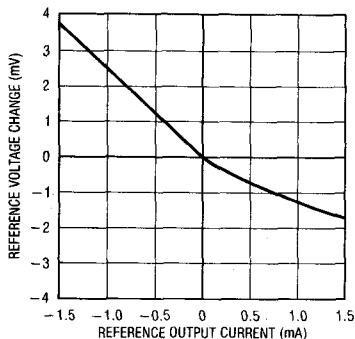


Supply Current at Dropout

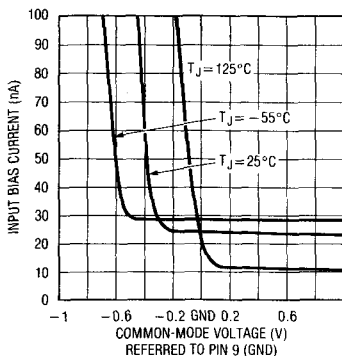


TYPICAL PERFORMANCE CHARACTERISTICS

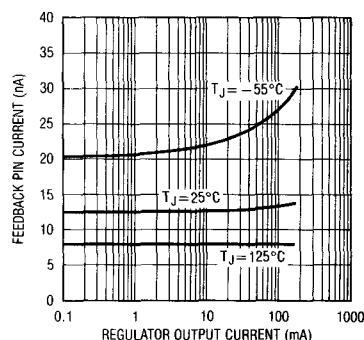
Reference Regulation



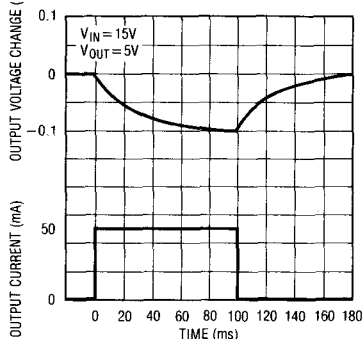
Comparator Input Bias Current



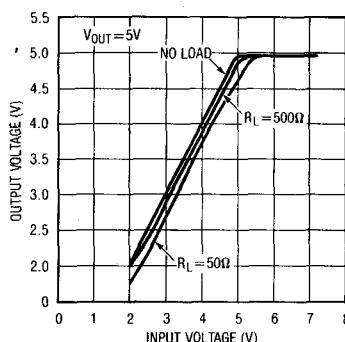
Feedback Pin Current



Regulator Thermal Regulation



LT1020 Turn-On Characteristic



APPLICATION HINTS

The LT1020 is especially suited for micropower system applications. For example, the comparator section of the LT1020 may be used as a battery checker to provide an indication of low battery. The dropout detector can shut-down the system when the battery voltage becomes too low to regulate. Another type of system application for the LT1020 would be to generate the equivalent of split supplies off of a single power input. The regulator section provides regulated output voltage and the reference, which can both source and sink current is then an artificial system ground providing a split supply for the system.

For many applications the comparator can be frequency compensated to operate as an amplifier. Compensation

values for various gains are given in the datasheet. The comparator gain is purposely low to make it easier to frequency compensate as an amplifier. Two outputs are available on the comparator, the NPN output is capable of sinking 10mA and can drive loads connected to voltages in excess of the positive power supply. This is useful for driving switches or linear regulators off of a higher input voltage. The PNP output, which is capable of sourcing 100 μA can drive loads below ground. It can be used to make negative regulators with the addition of an external pass transistor. Both outputs can be tied together to provide an output that swings from rail-to-rail for comparator or amplifier applications. Although it is not specified, the gain for the PNP output is about 500-1000.

APPLICATION HINTS

If the PNP output is being used, to maximize the gain, a $1\text{-}5\mu\text{A}$ load should be placed upon the NPN output collector. This is easily done by connecting a resistor between the NPN collector and the reference output. (Providing this operating current to the NPN side increases the internal emitter base voltages and maximizes the gain of the PNP stage.) Without this loading on the NPN collector, at temperatures in excess of 75°C , the gain of the PNP collector can decrease by a factor of 2 or 3.

Reference

Internal to the LT1020 is a 2.5V trimmed class B output reference. The reference was designed to be able to source or sink current so it could be used in supply splitting applications as well as a general purpose reference for external circuitry. The design of the reference allows it to source typically 4 or 5mA and sink 2mA . The available source and sink current decreases as temperature increases. It is sometimes desirable to decrease the AC output impedance by placing an output capacitor on them. The reference in the LT1020 becomes unstable with large capacitive loads placed directly on it. When using an output capacitor, about 20Ω should be used to isolate the capacitor from the reference pin. This 20Ω resistor can be placed directly in series with the capacitor or alternatively the reference line can have 20Ω placed in series with it and then a capacitor to ground. This is shown in Figure 1. Other than placing large capacitive loads on the reference, no other precautions are necessary and the reference is stable with nominal stray capacitances.

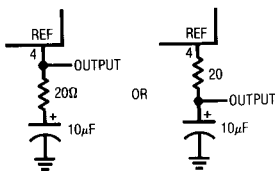


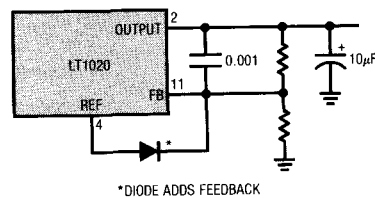
Figure 1. Bypassing Reference

Overload Protection

The main regulator in the LT1020 is current limited at approximately 250mA . The current limit is stable with both input voltage and temperature. A current limit pin, when strapped to ground, decreases the output current. This allows the output current to be set to a lower value than 250mA . The output current available with the current limit pin strapped to ground is not well controlled so if precise current limiting is desired it should be provided externally as is shown in some of the application circuits.

If the device is overloaded for long periods of time, thermal shutdown turns the output off. In thermal shutdown, there may be some oscillations which can disturb external circuitry. A diode connected between the reference and feedback terminal provides hysteresis under thermal shutdown, so that the device turns on and off with about a 5 second period and there are no higher frequency oscillations. This is shown in Figure 2. This diode is recommended for most applications. Thermal shutdown temperature is set at approximately 145° .

Like most other IC regulators, a minimum load is required on the output of the LT1020 to maintain regulation. For most standard regulators this is normally specified at 5mA . Of course, for a micropower regulator this would be a tremendously large current. The output current must be large enough to absorb all the leakage current of the pass transistor at the maximum operating temperature. It also affects the transient response; low output currents have long recovery times from load transients. At high operating temperatures the minimum load current increases and



*DIODE ADDS FEEDBACK

Figure 2. Minimizing Oscillation in Thermal Shutdown

4

APPLICATION HINTS

having too low of a load current may cause the output to go unregulated. Devices are tested for minimum load current at high temperature. The output voltage setting resistors to the feedback terminal can usually be used to provide the minimum load current.

Frequency Compensation

The LT1020 is frequency compensated by a dominant pole on the output. An output capacitor of $10\mu\text{F}$ is usually large enough to provide good stability. Increasing the output capacitor above $10\mu\text{F}$ further improves stability. In order to insure stability, a feedback capacitor is needed between the output pin and the feedback pin. This is because stray capacitance can form another pole with the large value of feedback resistors used with the LT1020. Also, a feedback capacitor minimizes noise pickup and improves ripple rejection.

With the large dynamic operating range of the output current, 10000:1, frequency response changes widely. Low AC impedance capacitors are needed to insure stability. While solid tantalum are best, aluminum electrolytics can be used but larger capacitor values may be needed.

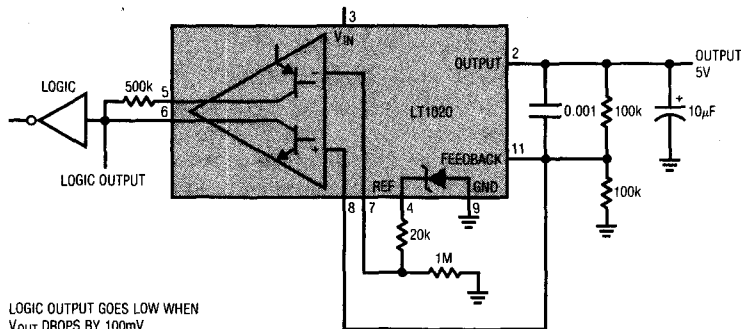
The CURRENT LIMIT pin allows one of the internal nodes to be rolled off with a $0.05\mu\text{F}$ capacitor to ground. With this capacitor, lower values of regulator output capacitance can be used (down to $1\mu\text{F}$) for low (<20mA) output currents. Values of capacitance greater than $0.05\mu\text{F}$ degrade the transient response, so are not recommended.

If the CURRENT LIMIT pin is connected to GND, the current limit is decreased and only a $1\mu\text{F}$ output capacitor is needed.

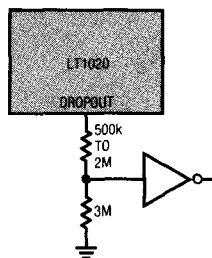
When bypassing the reference, a 20Ω resistor must be connected in series with the capacitor.

TYPICAL APPLICATIONS

Regulator With Output Voltage Monitor

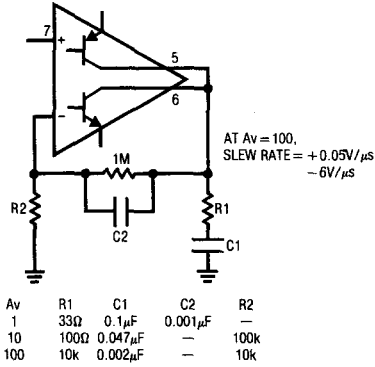


Driving Logic With Dropout Detector

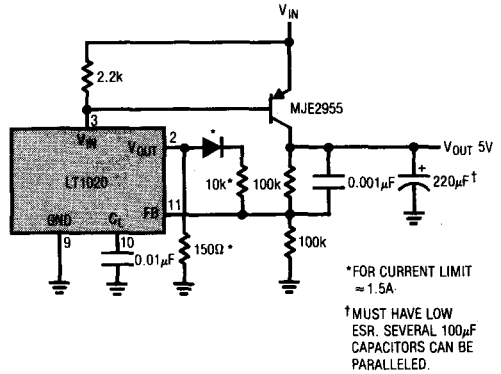


TYPICAL APPLICATIONS

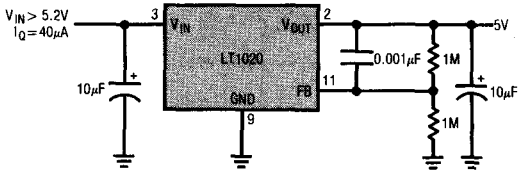
Compensating the Comparator as an Op Amp



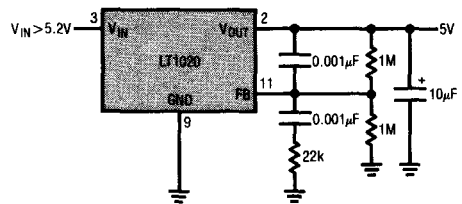
1 Amp Low Dropout Regulator



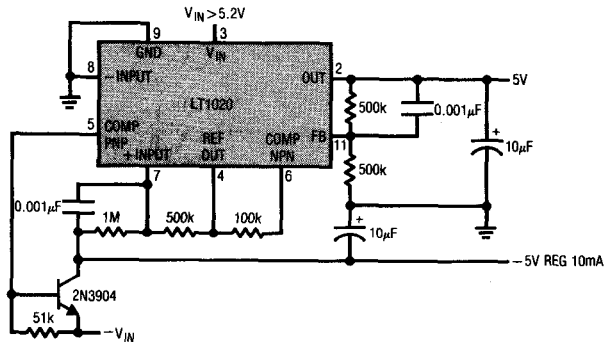
5V Regulator



Regulator with Improved Transient Response

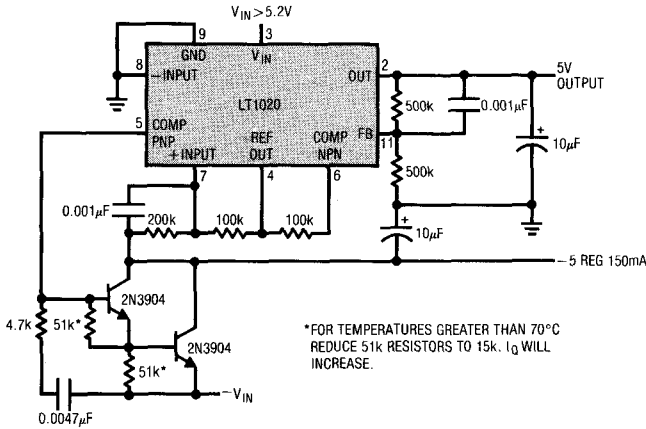


Dual Output Regulator

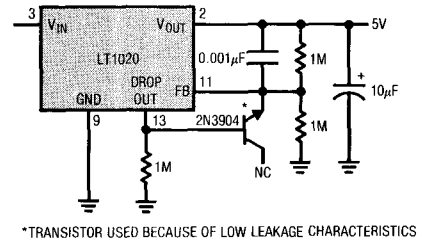


TYPICAL APPLICATIONS

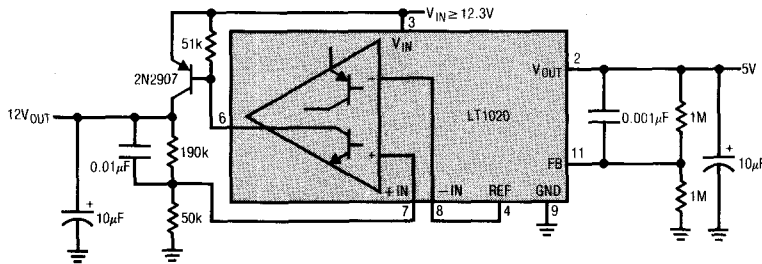
Dual Output 150mA Regulator



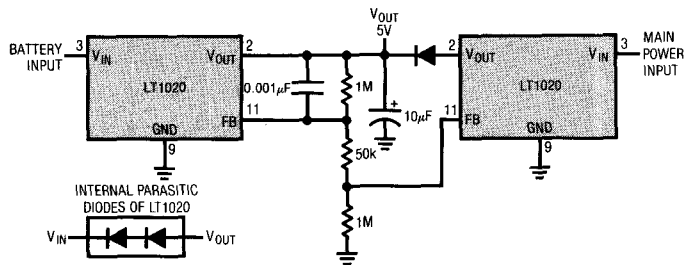
Maintaining Lowest I_Q at Dropout



Dual Output Positive Regulator

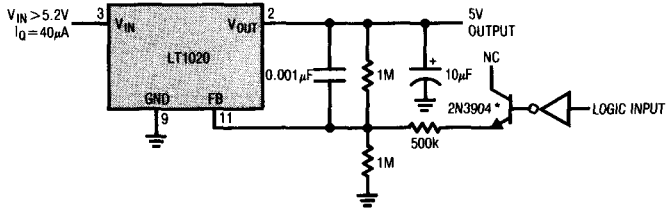


Battery Backup Regulator



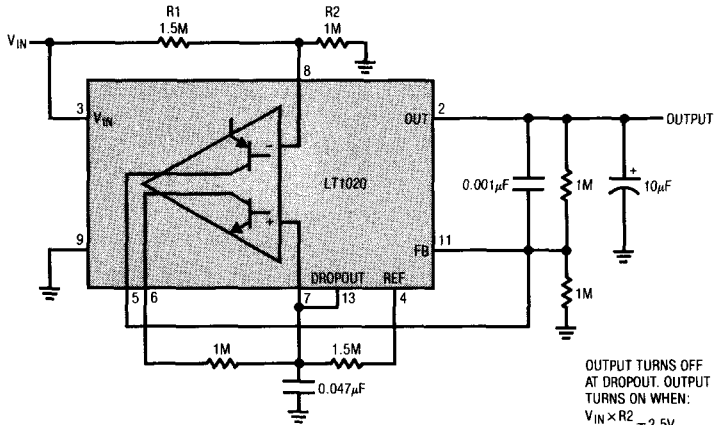
TYPICAL APPLICATIONS

5V Regulator with Shutdown



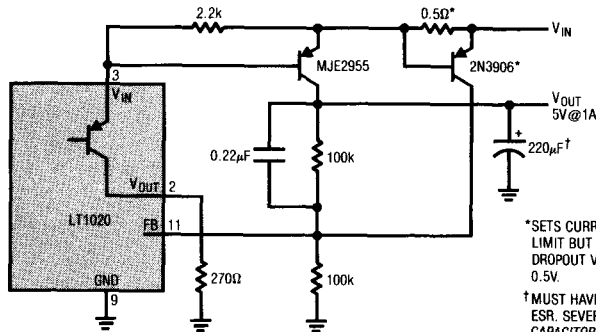
*TRANSISTOR USED BECAUSE OF LOW LEAKAGE CHARACTERISTICS.
TO TURN OFF THE OUTPUT OF THE LT1020
FORCE FB (PIN 11) > 2.5V.

Turn Off at Dropout



OUTPUT TURNS OFF
AT DROPOUT. OUTPUT
TURNS ON WHEN:
 $\frac{V_{IN} \times R2}{R1 + R2} = 2.5V$

Current Limited 1 Amp Regulator



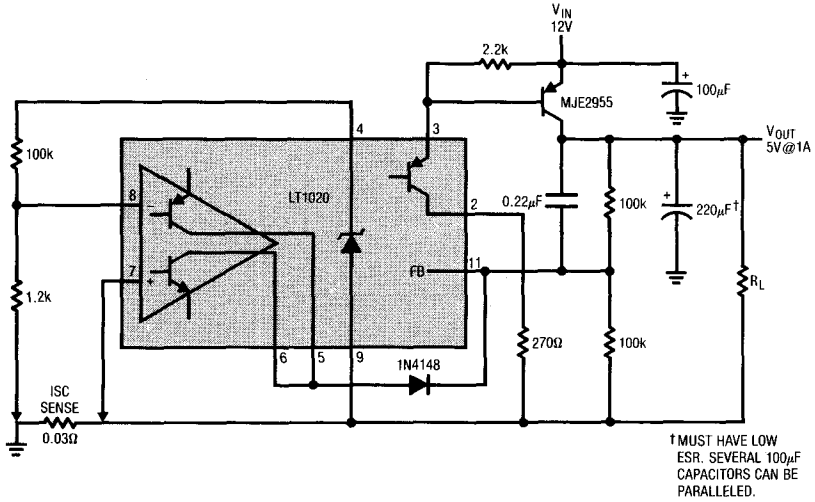
*SETS CURRENT
LIMIT BUT INCREASES
DROPOUT VOLTAGE BY
0.5V.

† MUST HAVE LOW
ESR. SEVERAL 100µF
CAPACITORS CAN BE
PARALLELED.

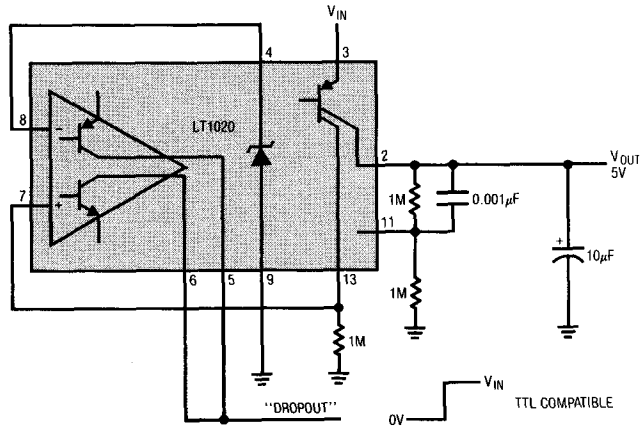
4

TYPICAL APPLICATIONS

1 Amp Regulator with Current Limit

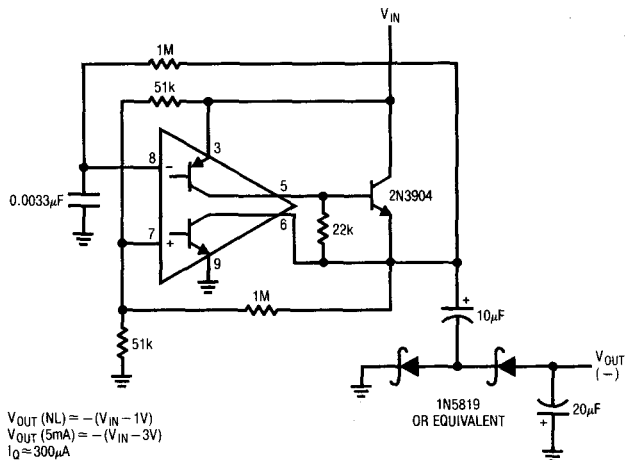


Logic Output on Dropout



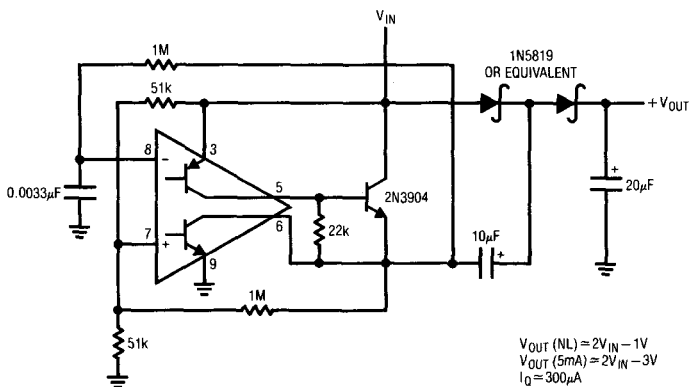
TYPICAL APPLICATIONS

Charge-Pump Negative Voltage Generator



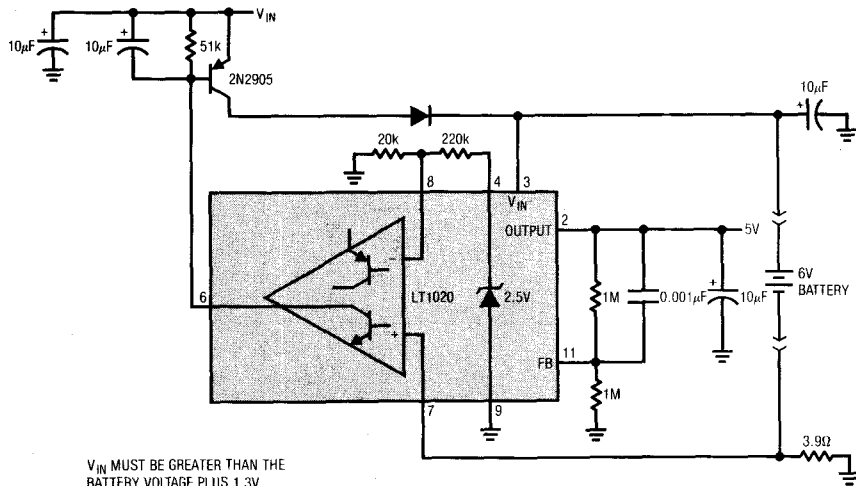
4

Charge-Pump Voltage Doubler



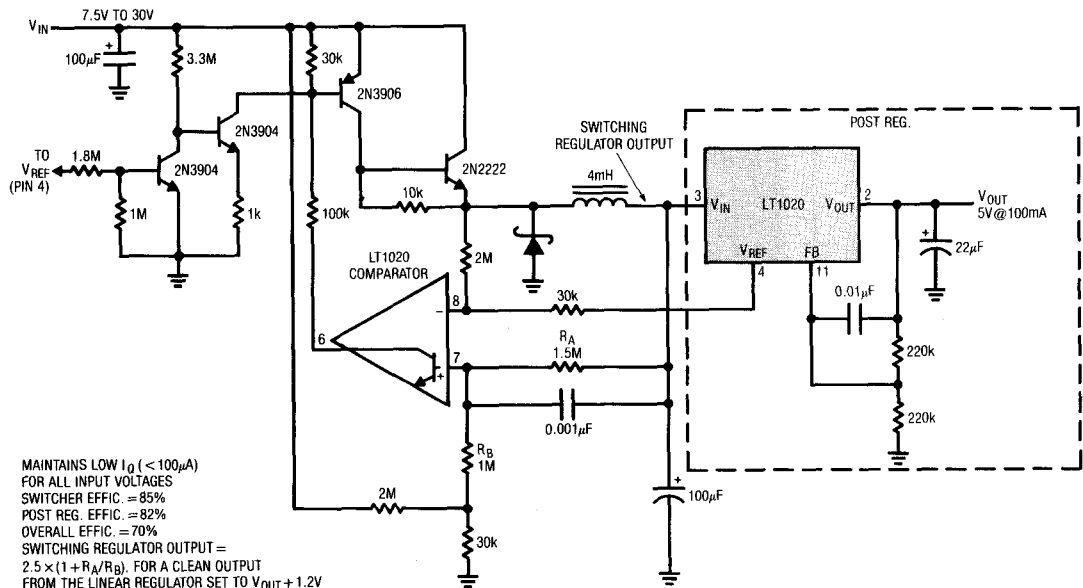
TYPICAL APPLICATIONS

50mA Battery Charger and Regulator



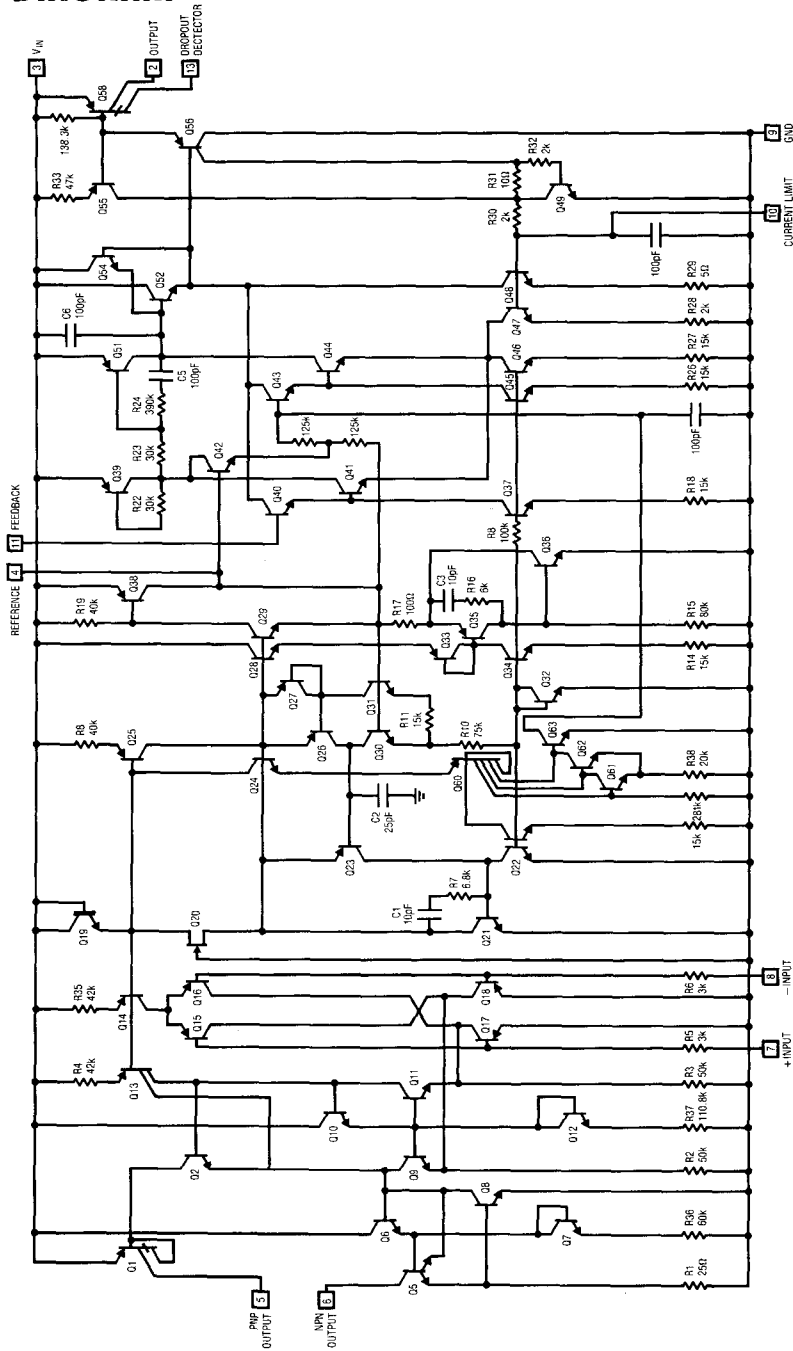
V_{IN} MUST BE GREATER THAN THE BATTERY VOLTAGE PLUS 1.3V

Switching Preregulator for Wide Input Voltage Range



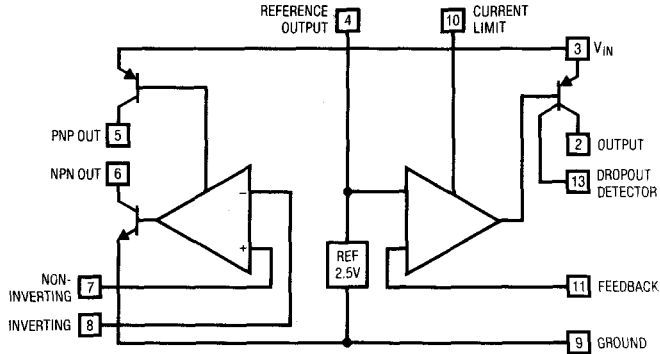
MAINTAINS LOW I_Q ($< 100\mu A$)
 FOR ALL INPUT VOLTAGES
 SWITCHER EFFIC. = 85%
 POST REG. EFFIC. = 82%
 OVERALL EFFIC. = 70%
 SWITCHING REGULATOR OUTPUT =
 $2.5 \times (1 + R_A/R_B)$. FOR A CLEAN OUTPUT
 FROM THE LINEAR REGULATOR SET TO $V_{OUT} + 1.2V$

SCHEMATIC DIAGRAM



4

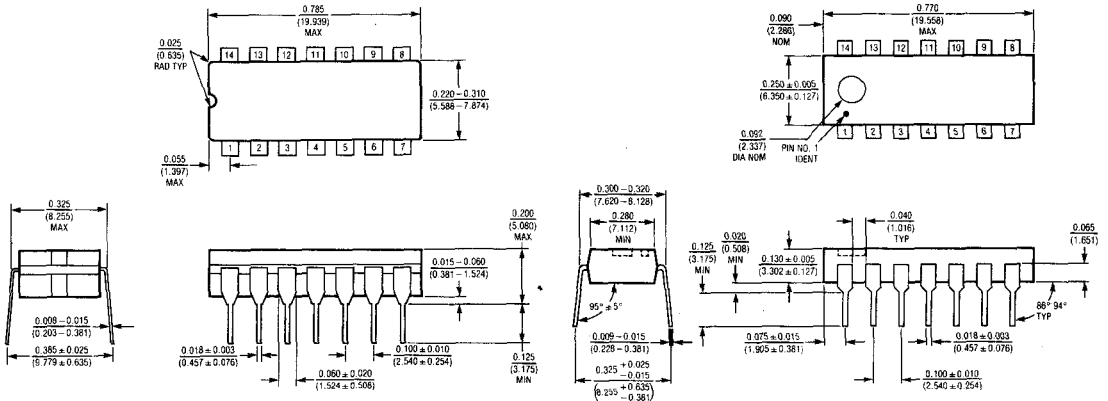
BLOCK DIAGRAM



PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

**J14 Package
Hermetic DIP**

**N14 Package
Plastic DIP**



T_{jmax} 150°C	Θ_{JA} 80°C/W
---------------------	-------------------------

T_{jmax} 110°C	Θ_{JA} 130°C/W
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FEATURES

- 40 μ A Supply Current
- 125mA Output Current
- 2.5V Reference Voltage
- Reference Output Sources 1mA and Sinks 0.5mA
- Dual Output Comparator
- Comparator Sinks 10mA
- Dropout Detector
- 0.2V Dropout Voltage
- Thermal Limiting
- Electrical Shutdown

APPLICATIONS

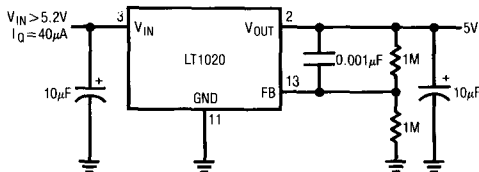
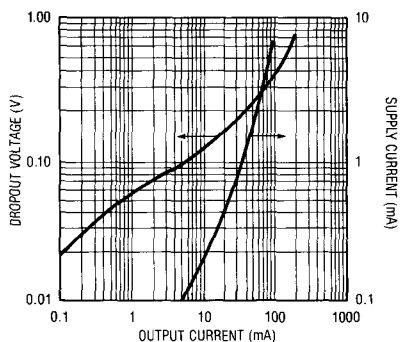
- Battery Systems
- Battery Backup System
- Portable Terminals
- Portable Instruments

DESCRIPTION

The LT1020 is a combination micropower positive regulator and free collector comparator on a single monolithic chip. With only 40 μ A supply current, the LT1020 can supply over 125mA of output current. Input voltage range is from 4.5V to 36V and dropout voltage is 0.6V at 125mA. Dropout voltage decreases with lower load currents. Also included on the chip is a class B output 2.5V reference that can either source or sink current. A dropout detector provides an output current to indicate when the regulator is about to drop out of regulation.

The dual output comparator can be used as a comparator for system or battery monitoring. For example, the comparator can be used to warn of low system voltage while the dropout detector shuts down the system to prevent abnormal operation. Frequency compensation of the comparator for amplifier applications can be obtained by adding external output capacitance. Dual output or positive and negative regulators can also be made.

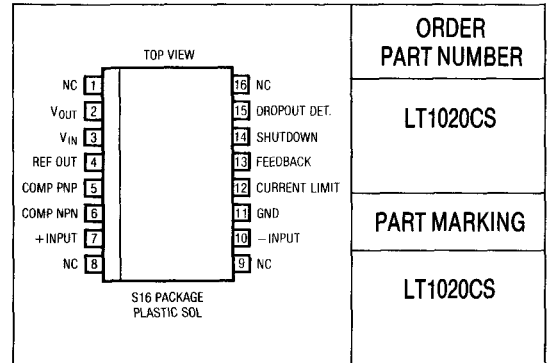
The 2.5V reference will source or sink current. This allows it to be used as a supply splitter or auxiliary output.

4
5V Regulator

Dropout Voltage and Supply Current


ABSOLUTE MAXIMUM RATINGS

Input Voltage 36V
 NPN Collector Voltage 36V
 PNP Collector Voltage Supply - 36V
 Output Short Circuit Duration Indefinite
 Power Dissipation Internally Limited
 Operating Temperature Range 0°C to 100°C
 Storage Temperature Range -65°C to 150°C

PACKAGE/ORDER INFORMATION



ELECTRICAL CHARACTERISTICS $T_j = 25^\circ\text{C}$

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Reference					
Reference Voltage	$4.5\text{V} \leq V_{IN} \leq 36\text{V}$	2.46	2.50	2.54	V
Line Regulation	$4.5\text{V} \leq V_{IN} \leq 36\text{V}$		0.01	0.015	%/V
Load Regulation	$-0.5\text{mA} \leq I_{REF} \leq 1\text{mA}, V_{IN} = 12\text{V}$		0.2	0.3	%
Output Source Current	$V_{IN} = 5\text{V}$	1	4		mA
Output Sink Current	$V_{IN} = 5\text{V}$	0.5	2		mA
Temperature Stability			1		%
Regulator					
Supply Current	$V_{IN} = 6\text{V}, I_{OUT} \leq 100\mu\text{A}$ $V_{IN} = 36\text{V}, I_{OUT} \leq 100\mu\text{A}$ $V_{IN} = 12\text{V}, I_{OUT} = 125\text{mA}$ $V_{IN} \leq 36\text{V}$ Shutdown		45 75 11 50	80 120 20	μA μA mA μA
Output Current	$(V_{IN} - V_{OUT}) \geq 1\text{V}, V_{IN} \geq 6\text{V}$	125			mA
Load Regulation	$(V_{IN} - V_{OUT}) \geq 1\text{V}, V_{IN} \geq 6\text{V}$		0.2	0.5	%
Line Regulation	$6\text{V} \leq V_{IN} \leq 36\text{V}$		0.01	0.015	%/V
Dropout Voltage	$I_{OUT} = 100\mu\text{A}$ $I_{OUT} = 125\text{mA}$		0.02 0.4	0.05 0.65	V V
Feedback Sense Voltage	$V_{IN} = 12\text{V}$	2.44	2.5	2.56	V
Dropout Detector Current	$\Delta V_{OUT} = -0.05\text{V}$	3	20		μA
Feedback Bias Current			15	40	nA
Minimum Load Current	$V_{IN} = 36\text{V}$		1	5	μA
Short Circuit Current	$V_{IN} = 36\text{V}$ Pin 11 and Pin 12 shorted, $V_{IN} = 4.5\text{V}$	3	250 30	360	mA mA
Comparator					
Offset Voltage	$0\text{V} \leq V_{CM} \leq 35\text{V}, V_{IN} = 36\text{V}$		3	7	mV
Bias Current	$0\text{V} \leq V_{CM} \leq 35\text{V}, V_{IN} = 36\text{V}$		15	40	nA
Offset Current	$0\text{V} \leq V_{CM} \leq 35\text{V}, V_{IN} = 36\text{V}$		4	15	nA
Gain-NPN Pulldown	$\Delta V_{OUT} = 29\text{V}, R_L = 20\text{k}$	2000	10000		V/V
Common Mode Rejection	$0\text{V} \leq V_{CM} \leq 35\text{V}, V_{IN} = 36\text{V}$	80	94		dB

ELECTRICAL CHARACTERISTICS $T_j = 25^\circ\text{C}$

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Comparator					
Power Supply Rejection	$4.5\text{V} \leq V_S \leq 36\text{V}$	80	96		dB
Output Sink Current	$V_{IN} = 4.5\text{V}$	10	18		mA
NPN Saturation Voltage	$I_{OUT} = 1\text{mA}$		0.4	0.6	V
Output Source Current		60	200		μA
Input Voltage Range		0		$V_{IN} - 1$	V
Response Time			5		μs
Leakage Current (NPN)				2	μA

ELECTRICAL CHARACTERISTICS

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Reference					
Reference Voltage	$4.5\text{V} \leq V_{IN} \leq 36\text{V}$	● 2.40	2.50	2.55	V
Line Regulation	$4.5\text{V} \leq V_{IN} \leq 36\text{V}$	●	0.01	0.02	%/V
Load Regulation	$-0.5\text{mA} \leq I_{REF} \leq 1\text{mA}, V_{IN} = 12\text{V}$	●	0.3	0.4	%
Output Source Current	$V_{IN} = 5\text{V}$	● 1			mA
Output Sink Current	$V_{IN} = 5\text{V}$	● 0.5			mA
Regulator					
Supply Current	$V_{IN} = 6\text{V}, I_{OUT} \leq 100\mu\text{A}$ $V_{IN} = 36\text{V}, I_{OUT} \leq 100\mu\text{A}$ $V_{IN} = 12\text{V}, I_{OUT} = 125\text{mA}$	●	65 85 11	95 120 20	μA μA mA
Output Current	$(V_{IN} - V_{OUT}) \geq 1\text{V}, V_{IN} \geq 6\text{V}$	● 125			mA
Load Regulation	$(V_{IN} - V_{OUT}) \geq 1\text{V}, V_{IN} \geq 6\text{V}$	●		1	%
Line Regulation	$6\text{V} \leq V_{IN} \leq 36\text{V}$	●		0.02	%/V
Dropout Voltage	$I_{OUT} = 100\mu\text{A}$ $I_{OUT} = 125\text{mA}$	●		0.06 0.85	V V
Feedback Sense Voltage	$V_{IN} = 12\text{V}$	● 2.38	2.5	2.57	V
Dropout Detector Current	$\Delta V_{OUT} = -0.05\text{V}$	● 3			μA
Feedback Bias Current		●		50	nA
Minimum Load Current	$V_{IN} = 36\text{V}$	●		50	μA
Short Circuit Current	$V_{IN} = 36\text{V}$ Pin 11 and Pin 12 shorted, $V_{IN} = 4.5\text{V}$	● 2.5	240 30	360	mA mA
Comparator					
Offset Voltage	$0\text{V} \leq V_{CM} \leq 35\text{V}, V_{IN} = 36\text{V}$	●		10	mV
Bias Current	$0\text{V} \leq V_{CM} \leq 35\text{V}, V_{IN} = 36\text{V}$ (Note 1)	●	15	60	nA
Offset Current	$0\text{V} \leq V_{CM} \leq 35\text{V}, V_{IN} = 36\text{V}$	●		20	nA
Gain-NPN Pull-down	$\Delta V_{OUT} = 29\text{V}, R_L = 20\text{k}$	● 1000			V/V
Common Mode Rejection	$0\text{V} \leq V_{CM} \leq 35\text{V}, V_{IN} = 36\text{V}$	● 80			dB
Power Supply Rejection	$4.5\text{V} \leq V_S \leq 36\text{V}$	● 80			dB
Output Sink Current	$V_{IN} = 4.5\text{V}$	● 5	10		mA
Output Source Current		● 40	120		μA
Input Voltage Range		● 0		$V_{IN} - 1$	V
Leakage Current (NPN)	$V_{IN} = 36\text{V}$	●		8	μA

The ● denotes the specifications which apply over full operating temperature range.

Note 1: For $0\text{V} \leq V_{CM} \leq 0.1\text{V}$ and $T > 85^\circ\text{C}$ I bias max is 100nA.

4

PIN FUNCTIONS

Pins 1, 8, 9, 16—No internal connection.

Pin 2—**Regulator Output.** Main output, requires 10 μ F output capacitor. Can be shorted to V_{IN} or ground without damaging device.

Pin 3—**Input Supply.** Bypass with 10 μ F cap. Must always be more positive than ground.

Pin 4—**Reference.** 2.5V can source or sink current. May be shorted to ground or up to 5V. Voltages in excess of 5V can damage the device.

Pin 5—**Comparator PNP Output.** Pull up current source for the comparator. May be connected to any voltage from V_{IN} to 36V more negative than V_{IN} (operates below ground). Short circuit protected. For example, if V_{IN} is 6V then pin 5 will operate to $-30V$.

Pin 6—**Comparator NPN Output.** May be connected to any voltage from ground to 36V more positive than ground (operates above V_{IN}). Short circuit protected.

Pins 7, 10—**Comparator Inputs.** Operates from ground to $V_{IN} - 1V$. Comparator inputs will withstand 36V even with V_{IN} of 0V.

Pin 11—**Ground.**

Pin 12—**Current Limit.** Connecting this pin to ground decreases the regulator current limit to 3mA min. Leave open when not used.

Pin 13—**Feedback.** This is the feedback point of the regulator. When operating, it is nominally at 2.5V. Optimum source resistance is 200k to 500k. The feedback pin should not be driven below ground or more positive than 5V.

Pin 14—**Shutdown.** Logic high turns the regulator output off. Shutdown threshold is 1.4V and impedance is 65k Ω .

Pin 15—**Dropout Detector.** This pin acts like a current source from V_{IN} which turns on when the output transistor goes into saturation. The magnitude of the current depends on the magnitude of the output current and the input-output voltage differential. Pin current ranges from 5 μ A to about 300 μ A.

FEATURES

- *Guaranteed* 1% Initial Voltage Tolerance
- *Guaranteed* 0.015%/V Line Regulation
- *Guaranteed* 0.02%/W Thermal Regulation
- 100% Burn-in in Thermal Limit

APPLICATIONS

- Adjustable Power Supplies
- System Power Supplies
- Precision Voltage/Current Regulators
- On-Card Regulators

DESCRIPTION

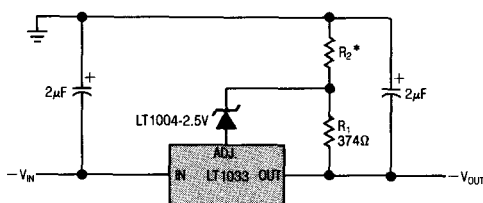
The LT1033 negative adjustable regulator will deliver up to 3 Amps output current over an output voltage range of -1.2V to -32V . Linear Technology has made significant improvements in these regulators compared to previous devices, such as better line and load regulation, and a maximum output voltage error of 1%.

The LT1033 is easy to use and difficult to damage. Internal current and power limiting as well as true thermal limiting prevents device damage due to overloads or shorts, even if the regulator is not fastened to a heat sink.

Maximum reliability is attained with Linear Technology's advanced processing techniques combined with a 100% burn-in in the thermal limit mode. This assures that all device protection circuits are working and eliminates field failures experienced with other regulators that receive only standard electrical testing.

4

Precision Regulator †



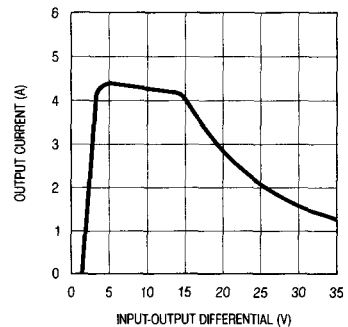
IMPROVED LINE & LOAD REGULATION **

$$* R_2 = \frac{R_1}{3.75} (V_{OUT} - 3.75)$$

$$** \text{REGULATION IS IMPROVED BY } \frac{V_{OUT}}{1.25}$$

 † EXTERNAL LT1004 REFERENCE IMPROVES
 LINE, LOAD, AND THERMAL REGULATION

Current Limit



LT1033

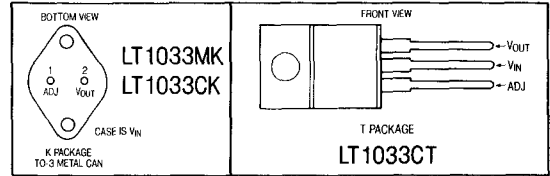
ABSOLUTE MAXIMUM RATINGS

Power Dissipation Internally Limited
 Input to Output Voltage Differential 35V
 Operating Junction Temperature Range
 LT1033M -55°C to 150°C
 LT1033C 0°C to 125°C
 Storage Temperature Range
 LT1033M -65°C to 150°C
 LT1033C -65°C to 150°C
 Lead Temperature (Soldering, 10 sec.) 300°C

PRECONDITIONING

100% THERMAL LIMIT BURN-IN

PACKAGE/ORDER INFORMATION



ELECTRICAL CHARACTERISTICS (See Note 1)

SYMBOL	PARAMETER	CONDITIONS	LT1033M			LT1033C			UNITS		
			MIN	TYP	MAX	MIN	TYP	MAX			
V_{REF}	Reference Voltage	$ V_{IN} - V_{OUT} = 5V, I_{OUT} = 5mA, T_J = 25^\circ C$	-1.238	-1.250	-1.262	-1.238	-1.250	-1.262	V		
$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	Load Regulation	$3V \leq V_{IN} - V_{OUT} \leq 35V$ $5mA \leq I_{OUT} \leq I_{MAX}, P \leq P_{MAX}$	●	-1.215	-1.250	-1.285	-1.200	-1.250	-1.300	V	
$\frac{\Delta V_{OUT}}{\Delta I_{OUT}}$	Line Regulation	$10mA \leq I_{OUT} \leq I_{MAX}$, (See Note 2) $T_J = 25^\circ C, V_{OUT} \leq 5V$		10	50		10	50	mV		
		$T_J = 25^\circ C, V_{OUT} \geq 5V$		0.2	1.0		0.2	1.0	%		
		$ V_{OUT} \leq 5V$	●	20	75		20	75	mV		
		$ V_{OUT} \geq 5V$	●	0.4	1.5		0.4	1.5	%		
$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	Line Regulation	$3V \leq V_{IN} - V_{OUT} \leq 35V$, (See Note 2) $T_J = 25^\circ C$	●		0.005	0.015		0.01	0.02	%/V	
	Ripple Rejection	$V_{OUT} = -10V, f = 120Hz$ $C_{ADJ} = 0$ $C_{ADJ} = 10\mu F$		56	66	70	80	66	60	77	dB
	Thermal Regulation	$T_J = 25^\circ C, 10msec$ Pulse			0.002	0.02		0.002	0.02	%/W	
I_{ADJ}	Adjust Pin Current		●	65	100		65	100	μA		
ΔI_{ADJ}	Adjust Pin Current Change	$10mA \leq I_{OUT} \leq I_{MAX}$ $3V \leq V_{IN} - V_{OUT} \leq 35V$	●	0.2	2		0.5	2	μA		
			●	1.0	5		2	5	μA		
I_{SC}	Current Limit	$ V_{IN} - V_{OUT} \leq 35V$		2.5	5.0		2.5	5.0	mA		
		$ V_{IN} - V_{OUT} \leq 10V$		1.2	3.0		1.2	3.0	mA		
I_{SC}	Current Limit	$ V_{IN} - V_{OUT} \leq 10V$, (See Note 2)		3	4.3	6		3	4.3	6	A
		$ V_{IN} - V_{OUT} = 35V, T_J = 25^\circ C$		0.5	1.3	2.5		.5	1.3	2.5	A
$\frac{\Delta V_{OUT}}{\Delta Temp}$	Temperature Stability of Output Voltage	$T_{MIN} \leq T \leq T_{MAX}$	●	0.6	1.5		0.6	1.5	%		
$\frac{\Delta V_{OUT}}{\Delta Time}$	Long Term Stability	$T_A = 125^\circ C, 1000$ Hours		0.3	1.0		0.3	1.0	%		
e_n	RMS Output Noise (% of V_{OUT})	$T_A = 25^\circ C, 10Hz \leq f \leq 10kHz$		0.003			0.003			%	
θ_{JC}	Thermal Resistance Junction to Case	T Package					4			$^\circ C/W$	
		K Package		1.2	2.0		1.2	2.0	$^\circ C/W$		

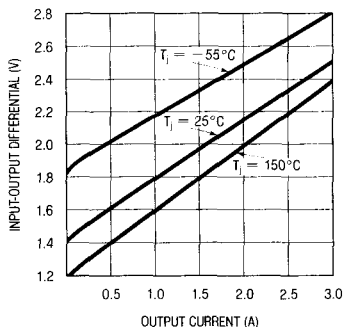
The ● denotes the specifications which apply over the full operating temperature range. Otherwise $T_J = 25^\circ C$.

Note 1: Unless otherwise indicated, these specifications apply: $|V_{IN} - V_{OUT}| = 5V$; and $I_{OUT} = 5mA$. Power dissipation is internally limited. However, these specifications apply for power dissipation up to 30W. See guaranteed minimum output current curve. $I_{MAX} = 3A$.

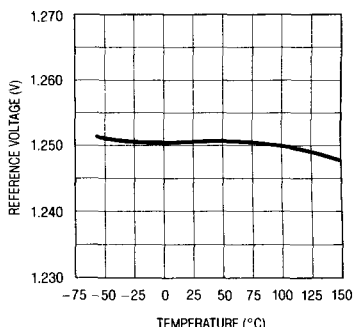
Note 2: Testing is done using a pulsed low duty cycle technique. See thermal regulation specifications for output changes due to heating effects. Load regulation is measured on the output pin at a point 1/8" below the base of the package.

TYPICAL PERFORMANCE CHARACTERISTICS

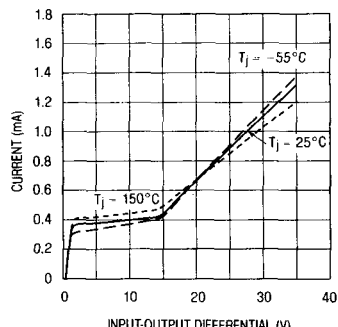
Dropout Voltage



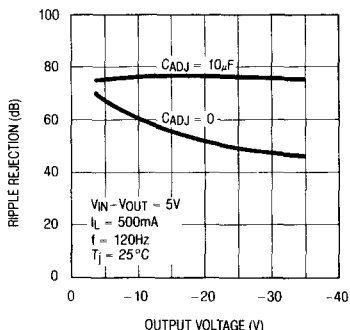
Temperature Stability



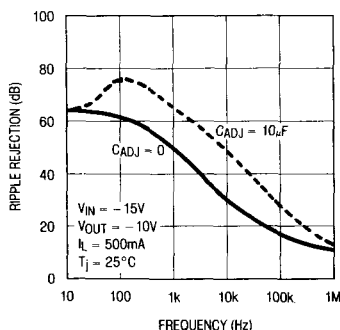
Minimum Load Current



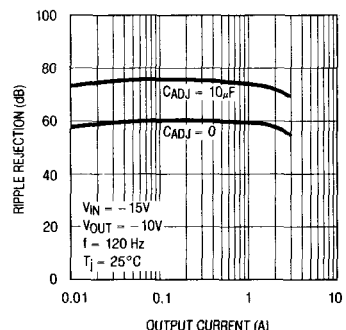
Ripple Rejection



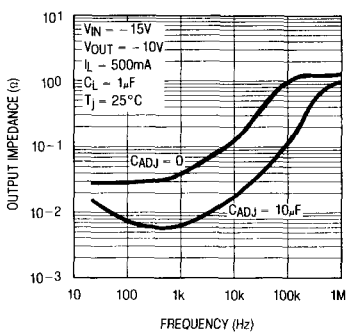
Ripple Rejection



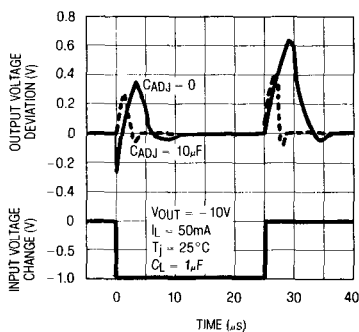
Ripple Rejection



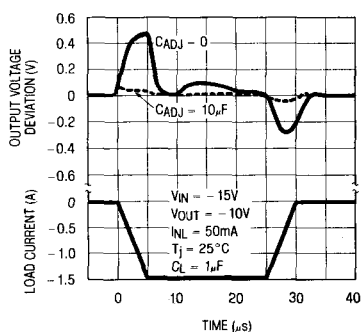
Output Impedance



Line Transient Response

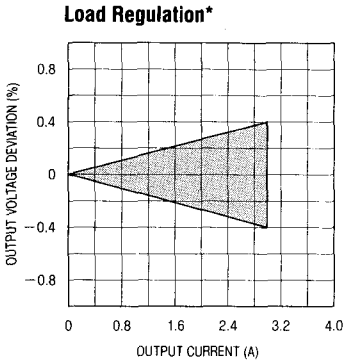


Load Transient Response

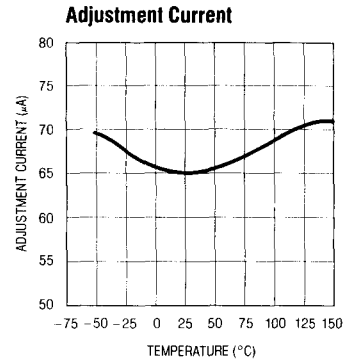
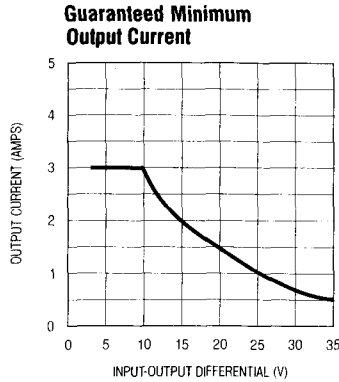


4

TYPICAL PERFORMANCE CHARACTERISTICS



* The LT1033 has load regulation compensation which makes the typical unit read close to zero. This band represents the typical production spread.



APPLICATION INFORMATION

Output Voltage: The output voltage is determined by two external resistors, R_1 & R_2 (see Figure 1). The exact formula for the output voltage is:

$$V_{OUT} = V_{REF} \left(1 + \frac{R_2}{R_1} \right) + I_{ADJ} (R_2)$$

Where: V_{REF} = Reference Voltage, I_{ADJ} = Adjustment Pin Current. In most applications, the second term is small enough to be ignored, typically about 0.5% of V_{OUT} . In more critical applications, the exact formula should be used, with I_{ADJ} equal to $65\mu A$. Solving for R_2 yields:

$$R_2 = \frac{V_{OUT} - V_{REF}}{\frac{V_{REF}}{R_1} - I_{ADJ}}$$

Smaller values of R_1 and R_2 will reduce the influence of I_{ADJ} on the output voltage, but the no-load current drain on the regulator will be increased. Typical values for R_1 are between 100Ω and 300Ω , giving $12.5mA$ and $4.2mA$ no-load current respectively. There is an additional consideration in selecting R_1 , the minimum load current specification of the regulator. The operating current of the LT1033 flows from input to-output. If this current is not absorbed by the load, the output of the regulator will rise above the regulated value. The current drawn by R_1 and R_2 is normally high enough to

absorb the current, but care must be taken in no-load situations where R_1 and R_2 have high values. The maximum value for the operating current, which must be absorbed, is $5mA$ for the LT1033. If input-output voltage differential is less than $10V$, the operating current that must be absorbed drops to $3mA$.

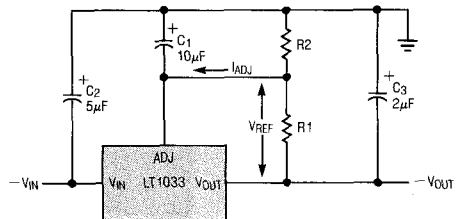


Figure 1

EXAMPLE:

1. A precision $10V$ regulator to supply up to $3A$ mp load current.

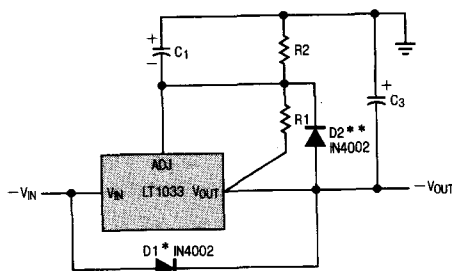
- a. Select $R_1 = 100\Omega$ to minimize effect of I_{ADJ}
- b. Calculate $R_2 = \frac{V_{OUT} - V_{REF}}{\frac{V_{REF}}{R_1} - I_{ADJ}} = \frac{10V - 1.25V}{\frac{1.25V}{100\Omega} - 65\mu A} = 704\Omega$

APPLICATION INFORMATION

Capacitors and Protection Diodes: An output capacitor, C3, is required to provide proper frequency compensation of the regulator feedback loop. A 2 μ F or larger solid tantalum capacitor is generally sufficient for this purpose if the 1MHz impedance of the capacitor is 1 Ω or less. High Q capacitors, such as Mylar, are not recommended because they tend to reduce the phase margin at light load currents. Aluminum electrolytic capacitors may also be used, but the minimum value should be 25 μ F to ensure a low impedance at 1MHz. The output capacitor should be located within a few inches of the regulator to keep lead impedance to a minimum. The following caution should be noted: if the output voltage is greater than 6V and an output capacitor greater than 20 μ F has been used, it is possible to damage the regulator if the input voltage becomes shorted, due to the output capacitor discharging into the regulator. This can be prevented by using diode D1 (see Figure 2) between the input and the output.

The input capacitor, C2, is only required if the regulator is more than 4 inches from the raw supply filter capacitor.

Bypassing the Adjustment Pin: The adjustment pin of the LT1033 may be bypassed with a capacitor to ground, C1, to reduce output ripple, noise, and impedance. These parameters scale directly with output voltage if the adjustment pin is not bypassed. A bypass capacitor reduces ripple, noise, and impedance to that of a 1.25V regulator. In a 15V regulator for example, these parameters are improved by $15V/1.25V = 12$ to 1. This improvement holds only for those frequencies where the impedance of the bypass capacitor is less than R1. Ten microfarads is generally sufficient for 60Hz power line applications where the ripple frequency is 120Hz, since $X_C = 130\Omega$. The capacitor should have a voltage rating at least as high as the output voltage of the regulator. Values larger than 10 μ F may be used, but if the output is larger than 25V, a diode, D2, should be added between the output and adjustment pins (see Figure 2).



* D1 protects the regulator from input shorts to ground. It is required only when C3 is larger than 20 μ F and VOUT is larger than 6V. ** D2 protects the adjust pin of the regulator from output shorts if C2 is larger than 10 μ F and VOUT is larger than -25V.

Figure 2

Proper Connection of Divider Resistors: The LT1033 has a load regulation specification of 0.8% and is measured at a point 1/8" from the bottom of the package. To prevent degradation of load regulation, the resistors which set output voltage, R1 and R2, must be connected as shown in Figure 3. Note that the positive side of the load has a true force and sense (Kelvin) connection, but the negative side of the load does not.

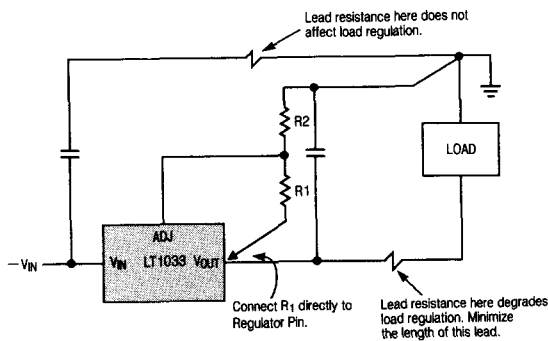


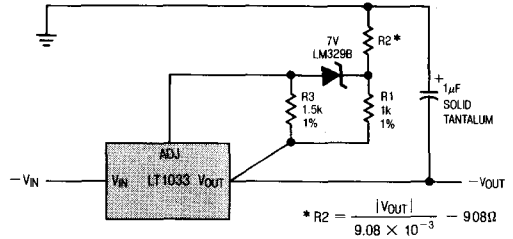
Figure 3

R1 should be connected *directly* to the output lead of the regulator, as close as possible to the specified point 1/8" from the case. R2 should be connected to the positive side of the load separately from the positive (ground) connection to the raw supply. With this arrangement, load regulation is degraded only by the resistance between the regulator output pin and the load. If R1 is connected to the load, regulation will be degraded.

TYPICAL APPLICATIONS

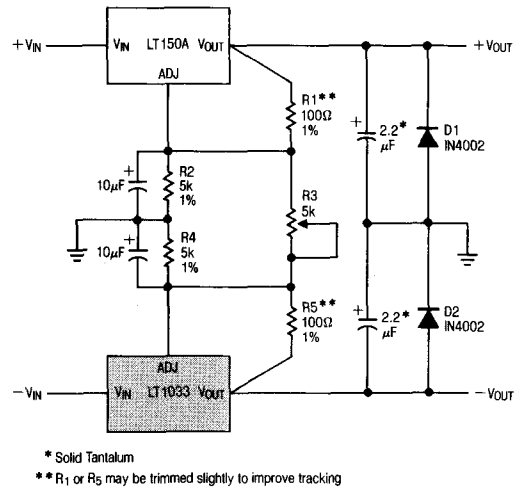
The output stability, load regulation, line regulation, thermal regulation, temperature drift, long term drift, and noise, can be improved by a factor of 6.6 over the standard regulator configuration. This assumes a zener whose drift and noise is considerably better than the regulator itself. The LM329B has 20PPM/°C maximum drift and about 10 times lower noise than the regulator.

High Stability Regulator

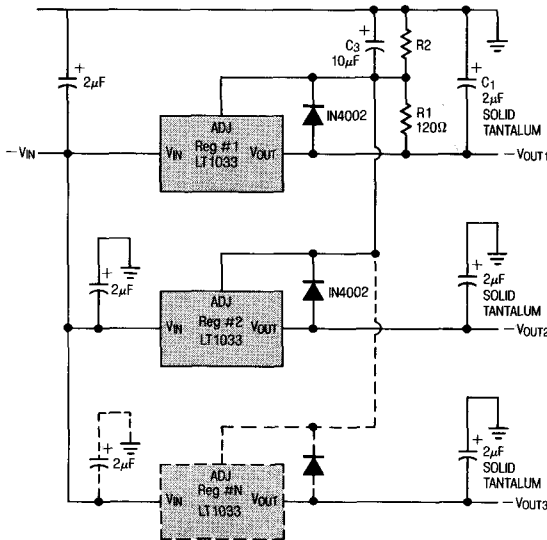


In the application shown below, regulators #2 to "N" will track regulator #1 to within ±24mV initially, and to ±60mV over all load, line, and temperature conditions. If any regulator output is shorted to ground, all other outputs will drop to ≈ -2V. Load regulation of regulators 2 to "N" will be improved by $V_{OUT}/1.25V$ compared to a standard regulator, so regulator #1 should be the one which has the lowest load current.

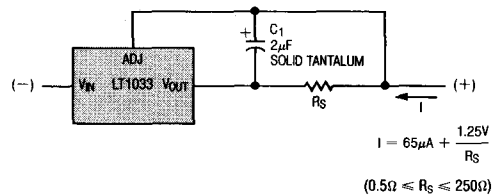
Dual Tracking 3A Supply ± 1.25V to ± 20V



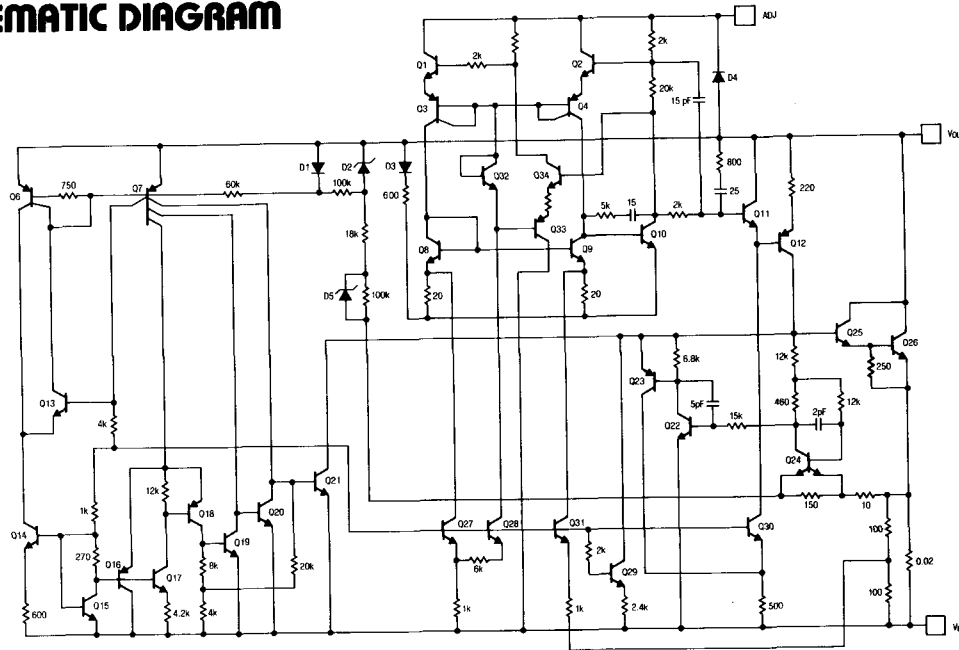
Multiple Tracking Regulators



Current Regulator



SCHEMATIC DIAGRAM

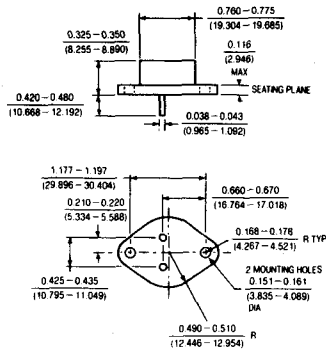


The following table allows convenient selection of program resistors from standard 1% values.

V_{OUT}	R_1	R_2	OUTPUT ERROR (%)
5	100	301	0.6
6	121	453	-0.7
8	115	619	0.6
10	115	806	0.6
12	118	1020	1
15	100	1100	0.5
18	150	2000	0.2
20	121	1820	0.8
22	130	2150	0.2
24	121	2210	0.9
28	115	2430	-0.7
30	121	2740	-0.9

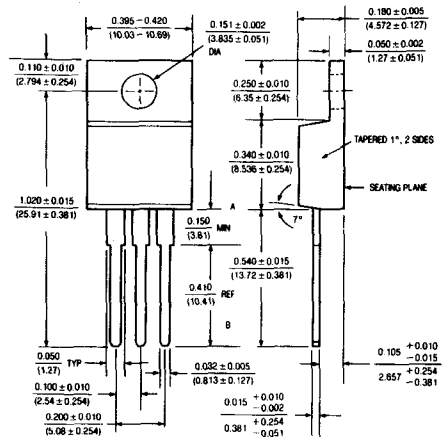
PACKAGE DESCRIPTION

K Package TO-3 STEEL Metal Can



	T _J MAX	θ _{JC}
LT1033M	150°C	2°C/W
LT1033C	125°C	2°C/W

T Package TO-220 Plastic



	T _J MAX	θ _{JC}
LT1033C	125°C	4°C/W

FEATURES

- Two Regulated Outputs
 - +5V at 3A
 - +5V at 75mA
- 2% Output Voltage Tolerance
- 66dB Ripple Rejection
- 0.7% Load Regulation
- TTL and CMOS Compatible Logic Control
- 100% Thermal Burn-In on All Devices

APPLICATIONS

- Power Supply Sequencing
- Remote On/Off Power Control
- Selective System Power during Emergency Power Operation
- Memory Power Supply with Back-Up

DESCRIPTION

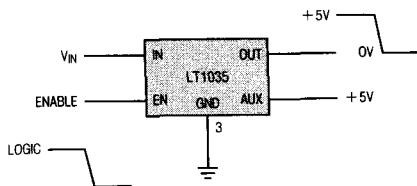
The LT1035 features two positive 5V regulators in the same package. The main regulator offers excellent performance while supplying load currents up to 3A, and the auxiliary regulator provides similar performance while supplying lighter loads of 75mA. The main regulator has the additional feature of being under the shutdown control of a logic signal. When the enable pin is taken to a low logic level, the main regulator shuts down and its output voltage goes to near 0V. During this command, the auxiliary output is unaffected by the main regulator's condition and continues to provide a 5V output.

The main output has current and power limiting combined with thermal shutdown to make it virtually blowout proof. The auxiliary output is not affected by the thermal shutdown mechanism or the state of the main output, allowing it to be used as a back-up in case of overloads or shorts on the main supply.

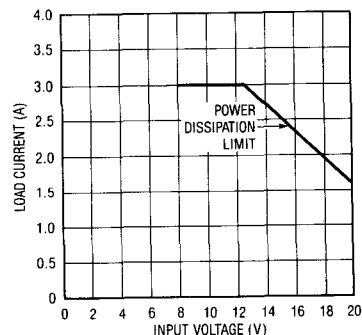
The logic input of the LT1035 (enable pin) has a 1.6V threshold and can be driven from a high source impedance. This allows it to be driven by most logic families, including TTL and CMOS.

For a 1A version of the LT1035, please see the LT1005 data sheet. For a 12V output voltage version, consult the factory.

Functional Diagram



Guaranteed Load Current



LT1035M/LT1035C

ABSOLUTE MAXIMUM RATINGS

Power Dissipation—Continuous	24W
Power Dissipation—Fault Conditions	Internally Limited
Input Voltage (V_{IN})	20V
Enable Voltage (V_{EN})	20V
Operating Junction Temperature	
LT1035M	-55°C to 150°C
LT1035C	0°C to 125°C
Storage	-65°C to 150°C
Lead Temperature (Soldering, 10 sec.)	300°C

PRECONDITIONING

100% Burn-In in Thermal Limit

PACKAGE/ORDER INFORMATION

<p>BOTTOM VIEW</p> <p>4 LEAD TO-3</p>	ORDER PART NUMBER
	LT1035MK LT1035CK
<p>FRONT VIEW</p> <p>5 LEAD TO-220</p>	LT1035CT

ELECTRICAL CHARACTERISTICS Main Regulator (See Note 1)

SYMBOL	PARAMETER	CONDITIONS	LT1035M			LT1035C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_0	Output Voltage High	$T_j = 25^\circ\text{C}$	4.9	5.0	5.1	4.9	5.0	5.1	V
		$7.7\text{V} \leq V_{IN} \leq 20\text{V}$ $P_D \leq 24\text{W}$ $0\text{mA} \leq I_O \leq 3\text{A}$	●	4.8	5.0	5.2	4.8	5.0	5.2
	Low	$7\text{V} \leq V_{IN} \leq 12.5\text{V}$ $V_{IN} = 20\text{V}$	●		0.1 0.1	0.2 0.3	●	0.1 0.1	0.2 0.3
$\frac{\Delta V_0}{\Delta I_O}$	Load Regulation (Note 6)	$8\text{V} \leq V_{IN} \leq 12.5\text{V}$ $0 \leq I_O \leq 3\text{A}$ (Note 2)	●	10	35		10	35	mV
$\frac{\Delta V_0}{\Delta V_{IN}}$	Line Regulation	$7.4\text{V} \leq V_{IN} \leq 20\text{V}$ (Note 2)		0.3	2		0.3	2	mV/V
	Ripple Rejection	$50\text{Hz} \leq f \leq 500\text{Hz}$	60	70		60	70		dB
	Thermal Regulation	$\Delta P_D = 20\text{W}$ (Note 4)		0.003	0.012		0.003	0.012	%/W
I_O	Available Load Current (Note 6)	$8\text{V} \leq V_{IN} \leq 12.5\text{V}$ $V_{IN} = 20\text{V}$	●	3	4		3	4	A
			●	1.6	2.4		1.6	2.4	A
I_{SC}	Short Circuit Current	$V_{IN} = 8\text{V}$		4	6		4	6	A
		$V_{IN} = 20\text{V}$		2.5	4		2.5	4	A
V_{IN}	Minimum Input Voltage to Maintain Regulation	(Note 5) $I_O = 1\text{A}$	●	7.2	6.7		7.2	6.7	V
		$I_O = 3\text{A}$	●	7.7	7.2		7.7	7.2	V
I_Q	Quiescent Current	Output High		3	5		3	5	mA
		Output Low		2	4		2	4	mA
θ_{JC}	Thermal Resistance, Junction to Case	TO-3		1.5	2.5		1.5	2.5	$^\circ\text{C}/\text{W}$
		TO-220					2	3	$^\circ\text{C}/\text{W}$

ELECTRICAL CHARACTERISTICS Auxiliary Regulator (See Note 1)

SYMBOL	PARAMETER	CONDITIONS	LT1035M			LT1035C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V _O	Output Voltage	T _J = 25°C	4.9	5.0	5.1	4.9	5.0	5.1	V
		7.2V ≤ V _{IN} ≤ 20V 0mA ≤ I _O ≤ 75mA	● 4.8	5.0	5.2	4.8	5.0	5.2	V
$\frac{\Delta V_O}{\Delta I_O}$	Load Regulation	7.2V ≤ V _{IN} ≤ 20V 0mA ≤ I _O ≤ 75mA (Note 2)	●	5	15	5	15	mV	
$\frac{\Delta V_O}{\Delta V_{IN}}$	Line Regulation	7.2V ≤ V _{IN} ≤ 20V (Note 2)	●	0.2	1 2	0.2	1 2	mV/V mV/V	
	Ripple Rejection	50Hz ≤ f ≤ 500Hz		74		74		dB	
I _{SC}	Short Circuit Current	7.0V ≤ V _{IN} = 20V		140	250	140	250	mA	
V _{IN}	Minimum Input Voltage to Maintain Regulation	(Note 5)	●	6.5	6.2	6.5	6.2	V	
		I _O = 10mA I _O = 75mA	●	7.2	6.8	7.2	6.8	V	

ELECTRICAL CHARACTERISTICS Logic Control (See Note 1)

4

SYMBOL	PARAMETER	CONDITIONS	LT1035M			LT1035C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V _{EN}	Enable Threshold Voltage	7.0V ≤ V _{IN} ≤ 20V T _J = 25°C	● 1.45	1.6	1.7	1.45	1.6	1.7	V
			1.3	1.6	1.8	1.3	1.6	1.8	V
	Enable Pin Current	V _{EN} ≤ 1V (Note 3)	0	1.5	6	0	1.5	6	μA
		V _{EN} ≥ 2.4V		0	1	0	1	μA	

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: Unless otherwise indicated, these specifications apply for V_{IN} = 10V, I_O = 0mA, and T_J = 25°C.

Note 2: Line and load regulation is measured using a low duty cycle pulse, causing little change in the junction temperature. Effects due to thermal gradients and device heating must be taken into account separately.

Note 3: When the enable pin is at a low logic level, current flows out of the enable pin.

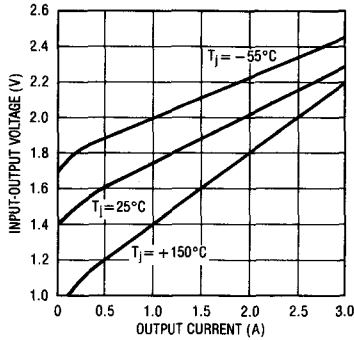
Note 4: Pulse length for this measurement is 20ms.

Note 5: Input voltage is reduced until output drops by 100mV from its initial value.

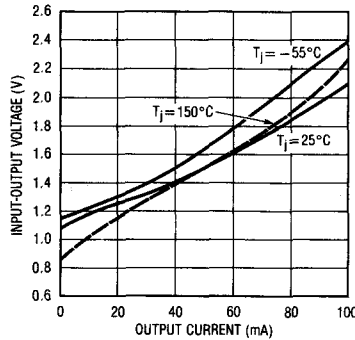
Note 6: See "Guaranteed Load Current" graph.

TYPICAL PERFORMANCE CHARACTERISTICS

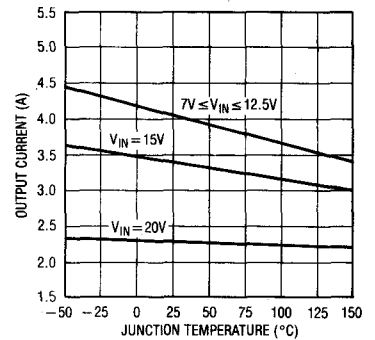
Minimum Input-Output Differential of Main Output



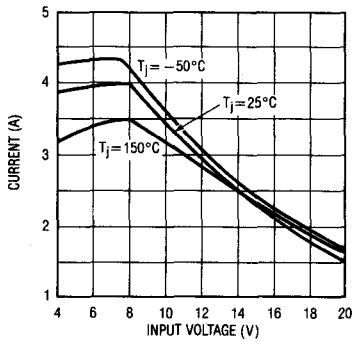
Minimum Input-Output Differential of Auxiliary Output



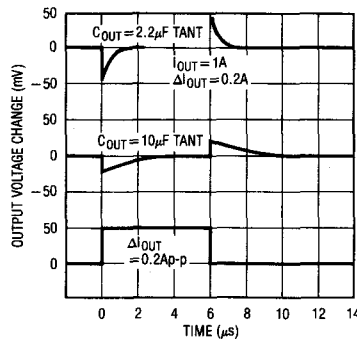
Maximum Available Load Current—Main Output



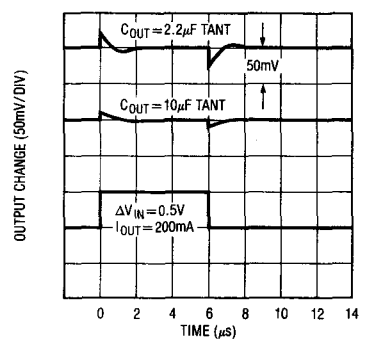
Short Circuit Output Current



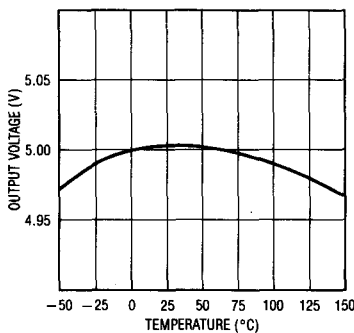
Load Transient Response



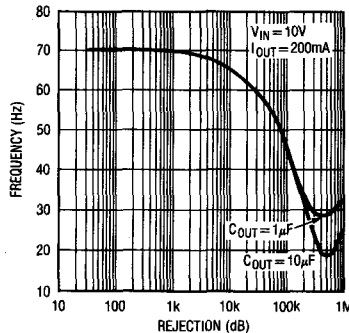
Line Transient Response



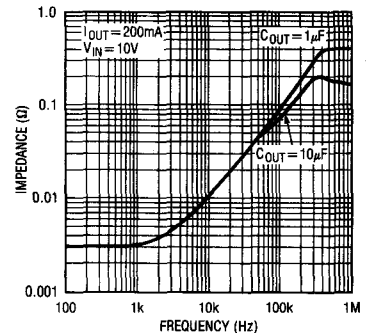
Output Voltage as Function of Temperature



Ripple Rejection

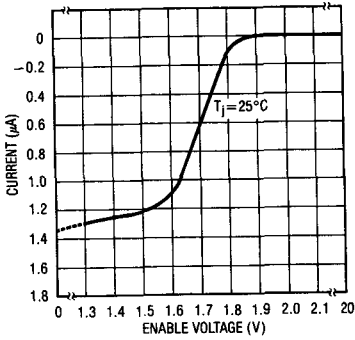


Output Impedance

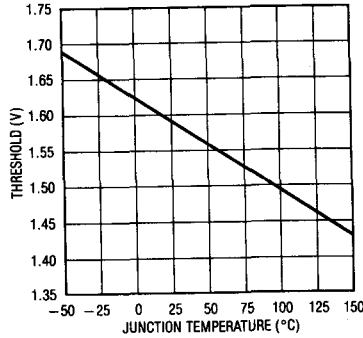


TYPICAL PERFORMANCE CHARACTERISTICS

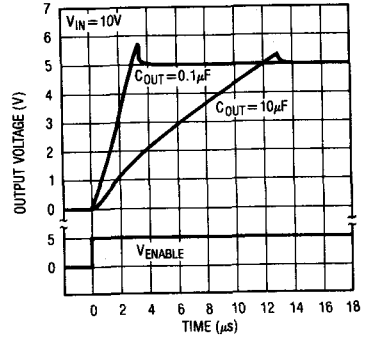
Enable Pin Characteristics



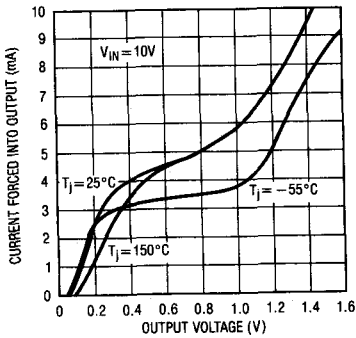
Enable Threshold



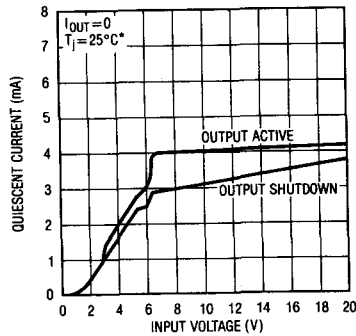
Output Switching Characteristics



Output Characteristics in Low State

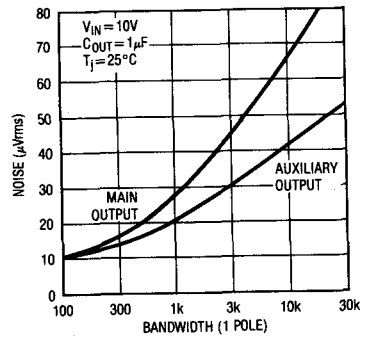


Quiescent Current



* I_Q IS NEARLY INDEPENDENT OF TEMPERATURE

Output Noise



4

APPLICATIONS INFORMATION

General Information

The LT1035 is a dual output 5V regulator. The main output is capable of delivering up to 3A of load current and can be shut down with a logic signal. The auxiliary output supplies a minimum of 75mA and is unaffected by the logic signal. The outputs are trimmed to $\pm 2\%$ initial tolerance and exhibit excellent line and load regulation.

The logic control feature makes the LT1035 ideal for many system applications where it is desirable to power-up a portion of the system for a period of time, and then power the system down during a standby operation. As an example, the LT1035 could be used to activate various memory space locations only as needed, thus saving substantial power dissipation and other cooling costs. The LT1035 could also be used to power microcomputers such as the 8048 series. The auxiliary supply can be used for RAM keep-alive during power-down operation. Additional power savings can be accomplished by using the LT1035 to power PROM, EPROM, and E²PROM devices. During program load or look-up table operations, the ROM type device can be activated and its contents placed in RAM, and then the ROM power can be removed. Or for high speed but low power data acquisition systems, the power could be applied to fast memory, then the data transferred to CMOS memory. The main regulator can then be shut down and the CMOS memory can be powered by the auxiliary for lower power dissipation. Other applications such as multiple power supply sequencing, elimination of expensive AC and DC power switches, delayed start applications, switching 5V DC loads, and many others are now easily accomplished.

Timing functions, such as delayed power-up or power-down, can also be performed directly at the enable pin.

Because a logic low on the enable pin shuts down the main regulator, feedback from output to enable can be used to generate hysteresis or latching functions.

The low quiescent current drain of the LT1035 makes it useful in battery-powered or battery back-up applications. The enable pin can be used as a "low battery" detector or to shut down major portions of system power,

allowing memory portions to continue to operate from the auxiliary output. At low output currents, the auxiliary output will regulate with input voltage typically as low as 6.1V, giving maximum battery life.

Good design practice with all regulators is to bypass the input and output terminals. A 2 μ F solid tantalum at the input and at both outputs is suggested. For the applications which follow, the bypass capacitors are still recommended, but for simplicity are not shown on the diagram. It is also recommended that for maximum noise immunity the voltage enable pin be tied high if it is unused. It can be tied directly to V_{IN}, as shown in Figure 1, or to the auxiliary output. If the enable pin is left open, it will float to a high logic level of approximately 1.6V and the main output regulator will be at 5V.

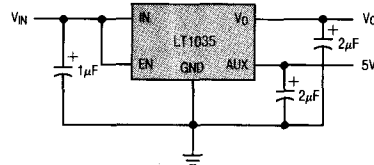


Figure 1

The enable pin is fully protected against input voltages up to 20V, even if the power input voltage is zero.

The basic shutdown control circuit uses a direct gate drive or an open collector driver and a pull-up resistor which are tied to V_{AUX}, as shown in Figure 2.

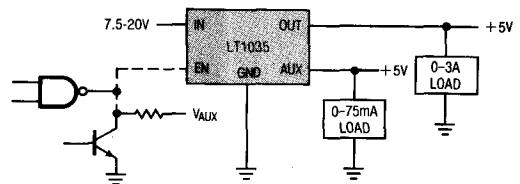


Figure 2

APPLICATIONS INFORMATION

Driving the Enable Pin

The enable pin equivalent schematic is shown in Figure 3. Basically, enable pin current is zero above the threshold and about $1.5\mu\text{A}$ below the threshold, flowing out of the pin. Standard logic, such as TTL and CMOS, will interface directly to the enable pin, even if the logic output swing is higher than the input voltage (V_{IN}) to the regulator. 15V CMOS can be used to drive the enable pin, even if the regulator is not powered up, without loading the CMOS output.

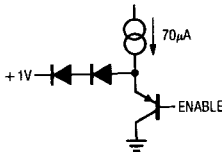


Figure 3

Timing functions, such as delayed power-up or power-down, can be implemented by driving the enable pin with an RC network. The current flowing out of the enable pin should not be used as the timing current in delayed power-up applications as it is temperature sensitive and varies somewhat from device to device. Instead, a resistor tied to the auxiliary output, the input, or to a logic signal should be used. The timing resistor chosen should provide at least $25\mu\text{A}$ of current to "swamp out" the effects of the internal current.

Main Output Current/Voltage Characteristics

Following a high to low transition at the enable pin, the main regulator output will begin to drop after a delay of approximately $0.4\mu\text{s}$. With no capacitive load, the output will fall to zero in approximately $0.8\mu\text{s}$ ($R_L = 2\Omega - 100\Omega$). With a capacitive load, fall time is limited by the RC product of the load and the output capacitance. For light loads ($R_L > 400\Omega$), the discharge time is controlled by an internal current pull-down of 15mA for output voltages down to 1.5V. Below 1.5V, the pull-down current drops to $\approx 4\text{mA}$. The DC output voltage in the shutdown mode is approximately 0.07V for input voltages (V_{IN}) up to 12V. If V_{IN} is 20V, the output during shutdown will be approximately 0.15V due to an internal current path in the regulator.

Output Characteristics in Low State

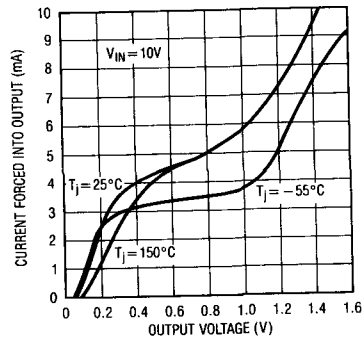


Figure 4

The user should note that the output in the low state can only sink about 3mA. If current is forced into the output, the output voltage will rise to 1V at 5mA and about 1.5V at 10mA. With no output capacitor, the rise time of the main output is about $3\mu\text{s}$. With an output capacitor, rise time is limited by the short circuit current of the LT1035 and the load capacitance; $t_r \approx (C)(5V)/4A$. A $10\mu\text{F}$ output capacitor slows the output rise time to approximately $12\mu\text{s}$.

Output Current

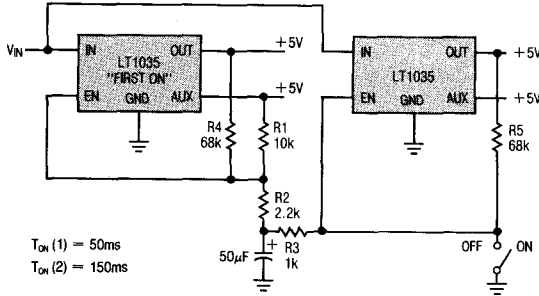
The main output current limits at about 4A for input voltages below 12.5V. Internal foldback, or "power limiting", circuitry detects the input-output voltage differential and reduces current limit for input to output voltages exceeding 7.5V. With 20V input, for instance, short circuit current is reduced to $\approx 2.4A$.

An additional feature of the LT1035 is that the auxiliary supply does not incorporate, nor is it affected by, thermal shutdown. Any fault condition of the main regulator will not affect the auxiliary output voltage.

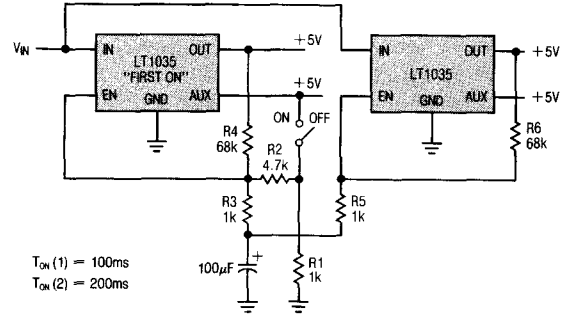
The following applications circuits will serve to indicate the versatility of the LT1035.

TYPICAL APPLICATIONS

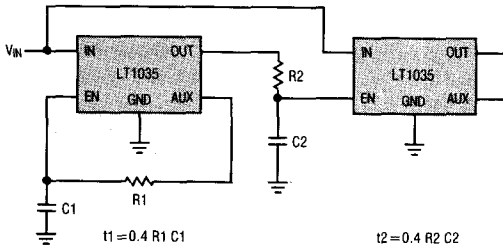
First-On, Last-Off Sequencing



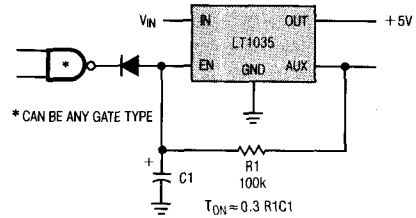
First-On, First-Off Sequencing



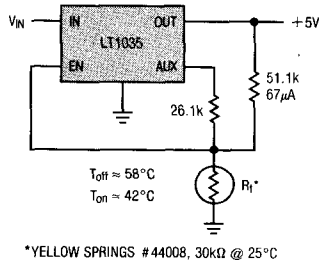
Power Supply Turn-On Sequencing



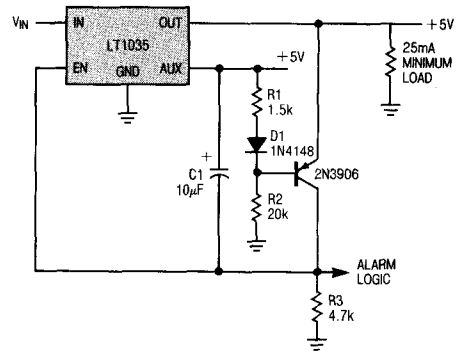
Fast Turn-Off, Delayed Turn-On



Thermal Cutoff at High Ambient Temperature

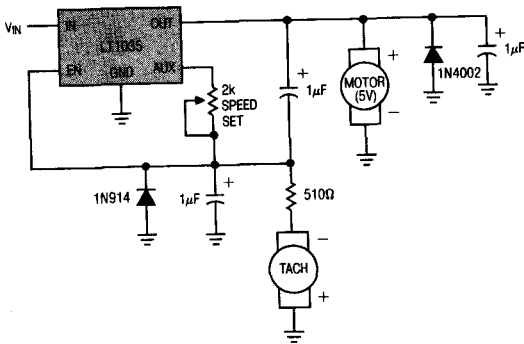


Latch-Off for $V_{OUT} \leq 4.7\text{V}$

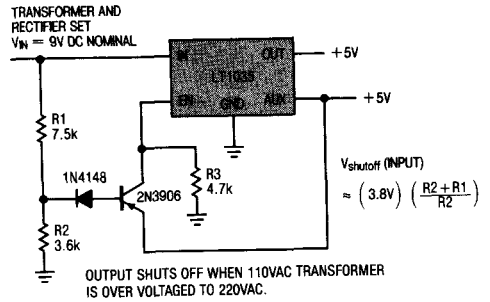


TYPICAL APPLICATIONS

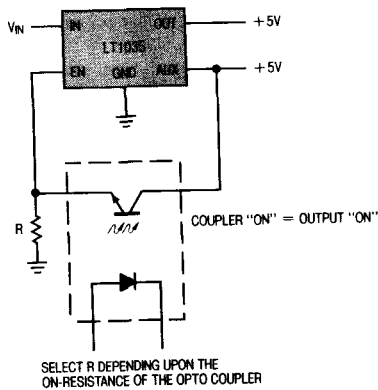
Proportional Motor Speed Controller



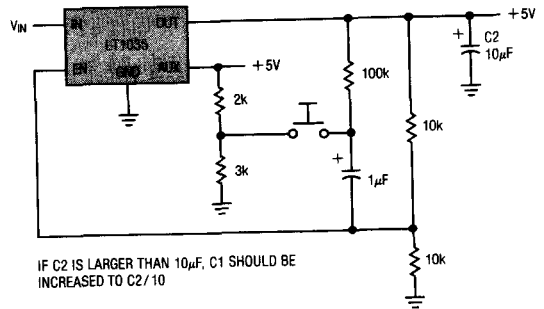
High Input Voltage Detection



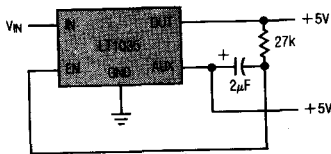
Opto-Coupled Output Control



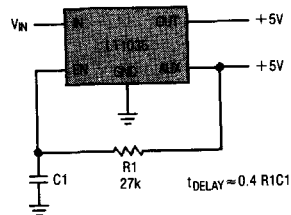
Push-On, Push-Off



Latch-Off when Output Short

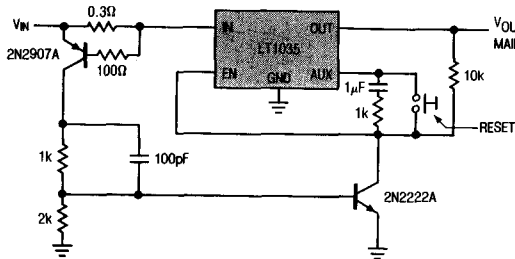


Delayed Power-Up

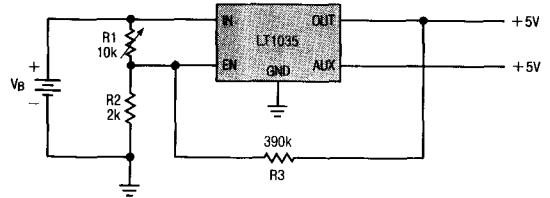


TYPICAL APPLICATIONS

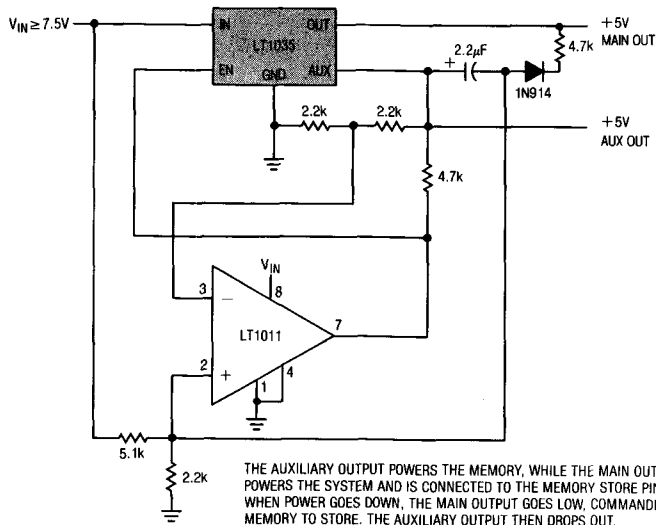
Fast Electronic Circuit Breaker



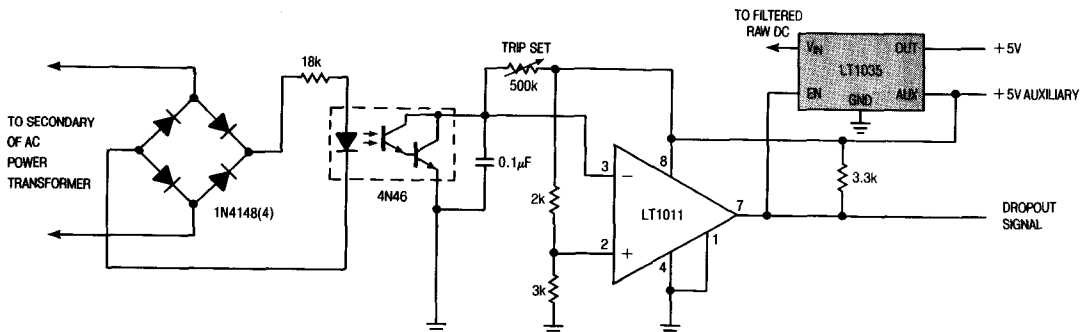
Battery Voltage Sensing Circuit



Memory Save on Power-Down

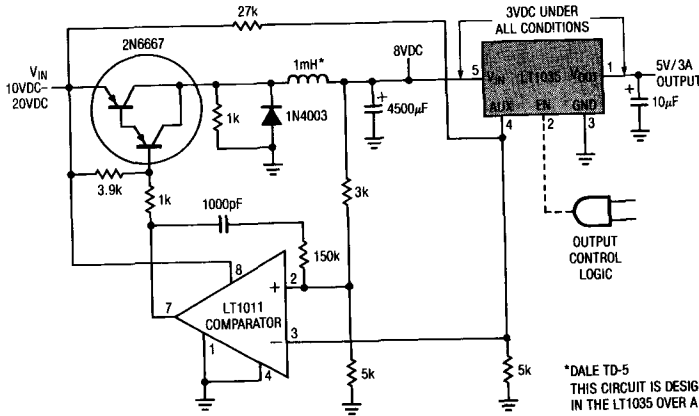


Line Dropout Detector



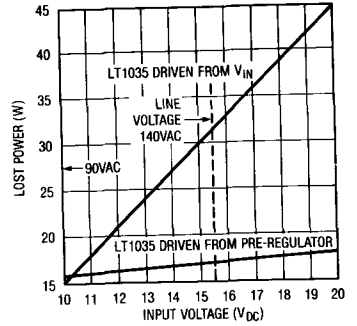
TYPICAL APPLICATIONS

Low Dissipation Regulator

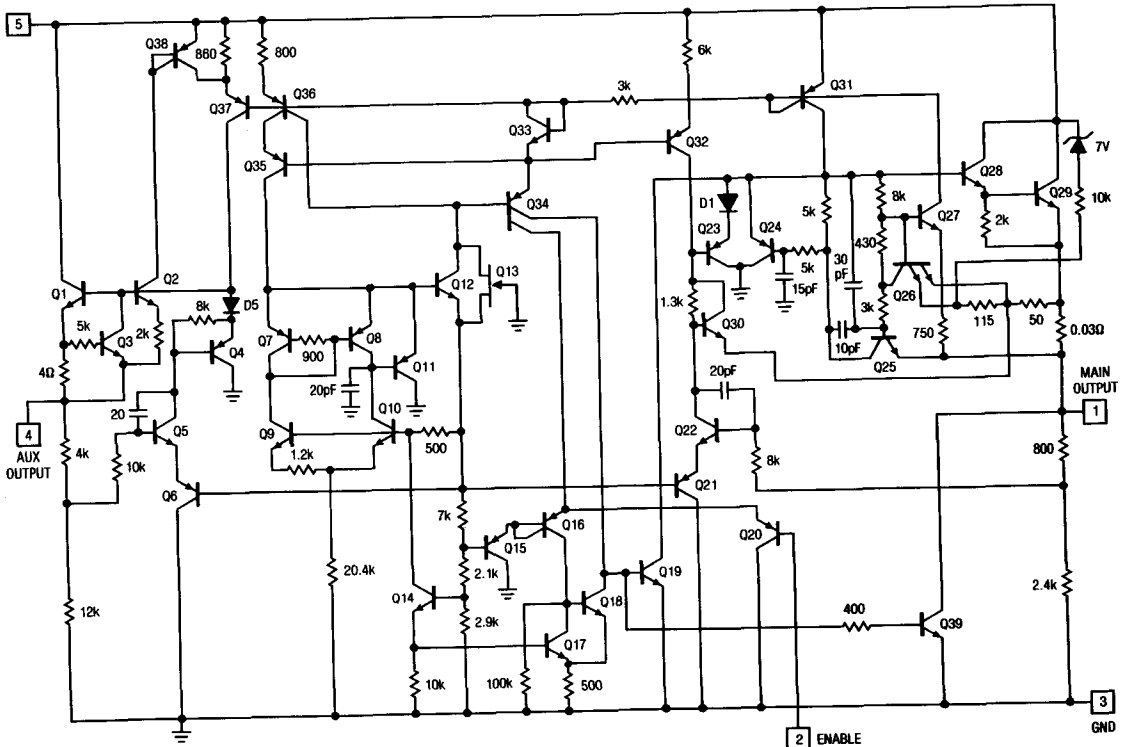


*DALE TD-5
THIS CIRCUIT IS DESIGNED TO REDUCE POWER DISSIPATION
IN THE LT1035 OVER A 90VAC-140VAC INPUT RANGE.

Regulator Losses at $I_{OUT} = 3A$



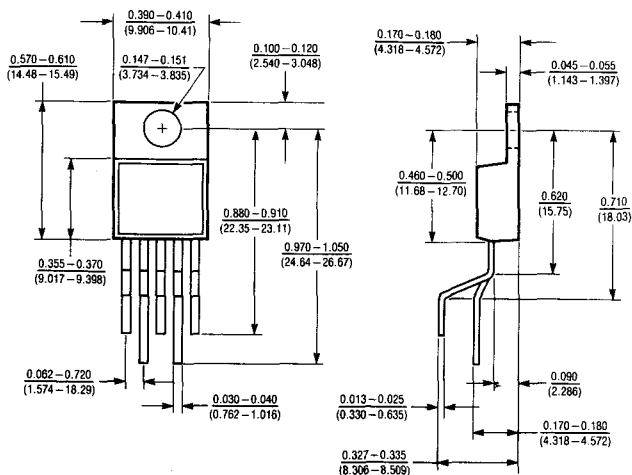
SCHEMATIC DIAGRAM



4

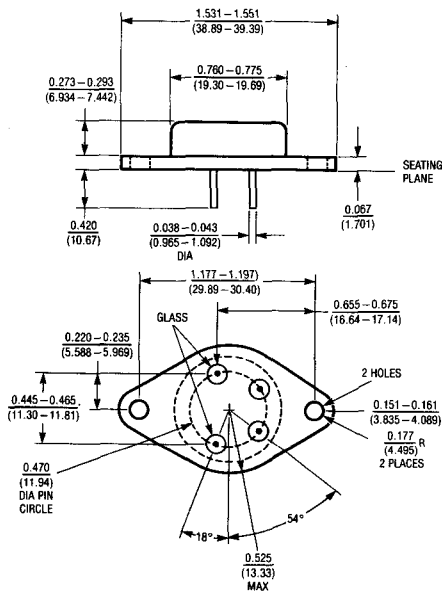
PACKAGE DESCRIPTION

T0-220 Package (5 Lead)



	T _{JMAX}	Θ _{JC}
LT1035C	125°C	3°C/W

4-Pin Metal Package Similar to JEDEC TO-3



	T _{JMAX}	Θ _{JC}
LT1035M	150°C	2.5°C/W
LT1035C	125°C	2.5°C/W

FEATURES

- Two Regulated Outputs
 - + 12V at 3A
 - + 5V at 75mA
- 2% Output Voltage Tolerance
- 60dB Ripple Rejection
- 0.7% Load Regulation
- TTL and CMOS Compatible Logic Control
- 100% Thermal Burn-In on All Devices

APPLICATIONS

- Power Supply Sequencing
- Remote On/Off Power Control
- Selective System Power during Emergency Power Operation
- Power Supply with Back-Up

DESCRIPTION

The LT1036 features two positive regulators in the same package. The 12V main regulator offers excellent performance while supplying load currents up to 3A, and the 5V auxiliary regulator provides similar performance while supplying lighter loads of 75mA. The main regulator has the additional feature of being under the shutdown control of a logic signal. When the enable pin is taken to a low logic level, the main regulator shuts down and its output voltage goes to near 0V. During this command, the auxiliary output is unaffected by the main regulator's condition and continues to provide a 5V output.

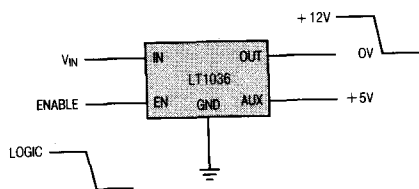
The main output has current and power limiting combined with thermal shutdown to make it virtually blowout proof. The auxiliary output is not affected by the thermal shutdown mechanism or the state of the main output, allowing it to be used as a back-up in case of overloads or shorts on the main supply.

The logic input of the LT1036 (enable pin) has a 1.6V threshold and can be driven from a high source impedance. This allows it to be driven by most logic families, including TTL and CMOS.

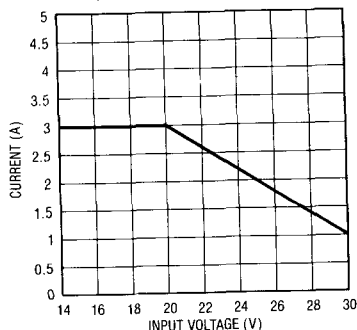
For a dual 5V version of the LT1036, please see the LT1035 data sheet.

4

Functional Diagram



Guaranteed Load Current, 12V Output



LT1036M/LT1036C

ABSOLUTE MAXIMUM RATINGS

Power Dissipation—Continuous (Note 6)	24W
Power Dissipation—Fault Conditions	Internally Limited
Input Voltage (V_{IN})	30V
Enable Voltage (V_{EN})	30V
Operating Junction Temperature	
LT1036M	-55°C to 150°C
LT1036C	0°C to 125°C
Storage	-65°C to 150°C
Lead Temperature (Soldering, 10 sec.)	300°C

PRECONDITIONING

100% Burn-In in Thermal Limit

PACKAGE/ORDER INFORMATION

<p>BOTTOM VIEW</p> <p>4 LEAD TO-3</p>	ORDER PART NUMBER
	LT1036MK LT1036CK
<p>FRONT VIEW</p> <p>5 LEAD TO-220</p>	LT1036CT

ELECTRICAL CHARACTERISTICS Main Regulator (See Note 1) $V_{IN} = 15V$ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	LT1036M/C			UNITS
			MIN	TYP	MAX	
V_O	Output Voltage	$T_J = 25^\circ C$	11.76	12	12.24	V
		$15V \leq V_{IN} \leq 30V$ $I_{OUT} \leq I_{MAX}$ (Note 6)	●	11.52	12.48	V
	High	$7V \leq V_{IN} \leq 30V$	●	0.1	0.3	V
$\frac{\Delta V_O}{\Delta I_O}$	Load Regulation (Note 6)	$V_{IN} = 16V$ $0 \leq I_O \leq 3A$ (Note 2)	●	10	80	mV
$\frac{\Delta V_O}{\Delta V_{IN}}$	Line Regulation	$15V \leq V_{IN} \leq 30V$ (Note 2)		1	4	mV/V
	Ripple Rejection	$50Hz \leq f \leq 500Hz$ (Note 8)	50	60		dB
	Thermal Regulation	$\Delta P_D = 20W$ (Note 4)		0.003	0.012	%/W
I_O	Available Load Current (Note 6)	$15V \leq V_{IN} \leq 20V$	●	3	4	A
		$V_{IN} = 25V$	●	2	2.7	A
I_{SC}	Short Circuit Current	$V_{IN} = 15V$		2.3	4	A
		$V_{IN} = 25V$		1	2	A
V_{IN}	Input Voltage to Maintain Regulation (Dropout Voltage)	(Note 5)				
		$I_O = 1A$	●	13.8	14.5	V
		$I_O = 3A$	●	14.4	15	V
I_Q	Quiescent Current	Output High		4	5.5	mA
		Output Low		3	4.5	mA
θ_{JC}	Thermal Resistance, Junction to Case	TO-3		1.5	2.5	$^\circ C/W$
		TO-220		2	3	$^\circ C/W$

ELECTRICAL CHARACTERISTICS Auxiliary Regulator (See Note 1)

SYMBOL	PARAMETER	CONDITIONS	LT1036M/C			UNITS
			MIN	TYP	MAX	
V _O	Output Voltage	T _J = 25°C	4.9	5.0	5.1	V
		7.2V ≤ V _{IN} ≤ 30V 0mA ≤ I _O ≤ 75mA	● 4.8	5.0	5.2	V
$\frac{\Delta V_O}{\Delta I_O}$	Load Regulation	7.2V ≤ V _{IN} ≤ 30V 0mA ≤ I _O ≤ 75mA (Note 2)	●	5	15	mV
$\frac{\Delta V_O}{\Delta V_{IN}}$	Line Regulation	7.2V ≤ V _{IN} ≤ 30V (Note 2)	●	0.2	1	mV/V mV/V
	Ripple Rejection	50Hz ≤ f ≤ 500Hz		74		dB
I _{SC}	Short Circuit Current (Note 7)	7.0V ≤ V _{IN} = 30V		140	250	mA
V _{IN}	Input Voltage to Maintain Regulation (Dropout Voltage)	(Note 5) I _O ≤ 10mA	●	6.2	6.5	V
		I _O = 75mA	●	6.8	7.2	V

ELECTRICAL CHARACTERISTICS Logic Control (See Note 1)

SYMBOL	PARAMETER	CONDITIONS	LT1036M/C			UNITS
			MIN	TYP	MAX	
V _{EN}	Enable Threshold Voltage	7.0V ≤ V _{IN} ≤ 30V T _J = 25°C	● 1.45	1.6	1.7	V
			1.3	1.6	1.8	V
	Enable Pin Current	V _{EN} ≤ 1V (Note 3)	● 0	1.5	12	μA
		V _{EN} ≥ 2.4V	●	0	6	μA

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: Unless otherwise indicated, these specifications apply for V_{IN} = 15V, I_O = 0mA, and T_J = 25°C.

Note 2: Line and load regulation is measured using a low duty cycle pulse, causing little change in the junction temperature. Effects due to thermal gradients and device heating must be taken into account separately.

Note 3: When the enable pin is at a low logic level, current flows out of the enable pin.

Note 4: Pulse length for this measurement is 20ms.

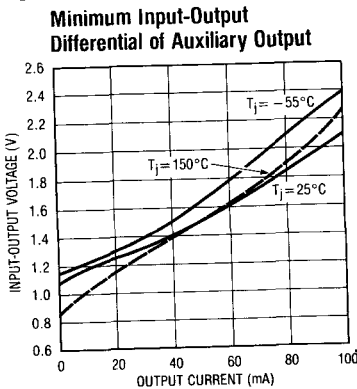
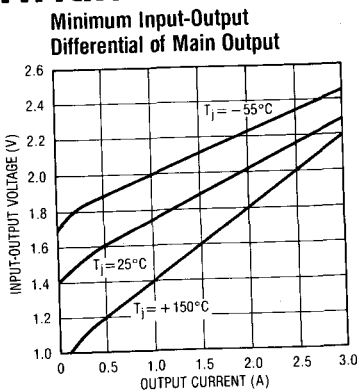
Note 5: Input voltage is reduced until output drops by 100mV from its initial value.

Note 6: See "Guaranteed Load Current" graph.

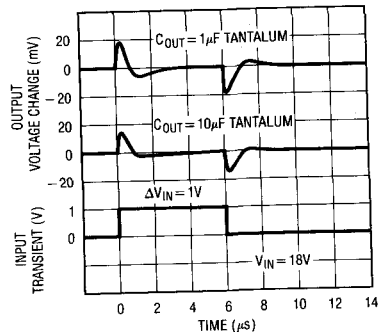
Note 7: Continuous shorts on the auxiliary output are not allowed unless adequate heat sinking is used to maintain junction temperature below 150°C.

Note 8: Guaranteed but not tested.

TYPICAL PERFORMANCE CHARACTERISTICS

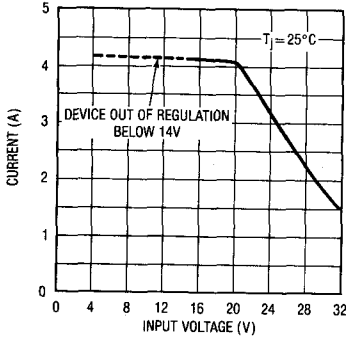


Line Transient Response, 12V Output

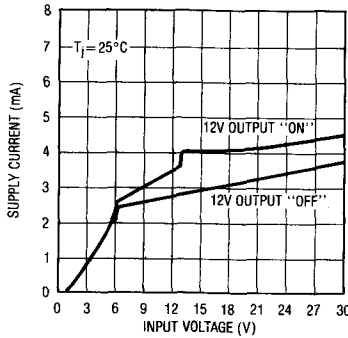


TYPICAL PERFORMANCE CHARACTERISTICS

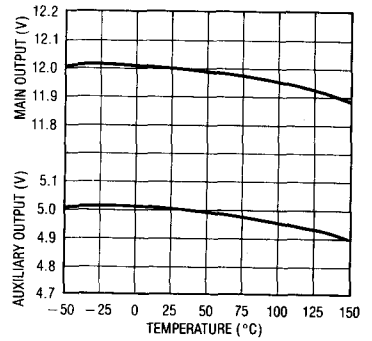
Maximum Available Load Current, 12V Output



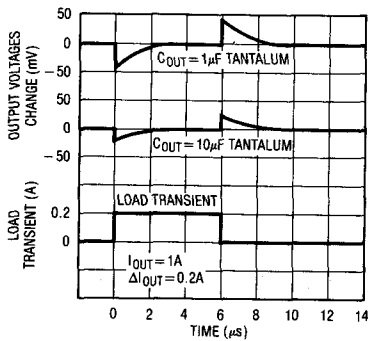
Quiescent Current



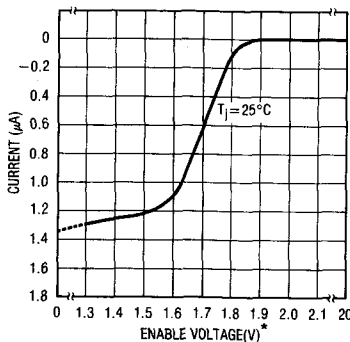
Output Voltage vs Temperature



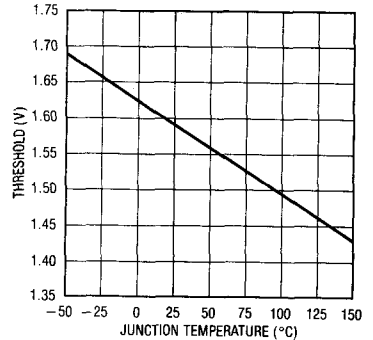
Load Transient Response, 12V Output



Enable Pin Characteristics

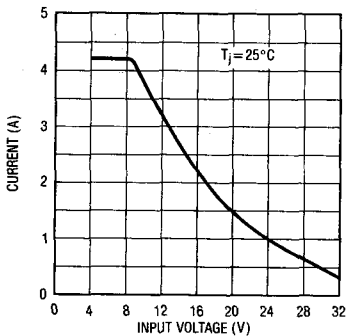


Enable Threshold

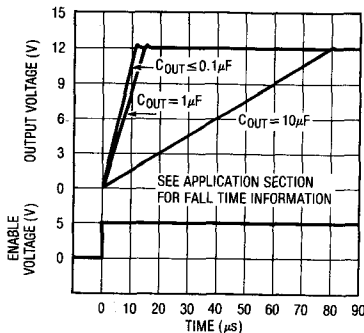


*NOTE SCALE CHANGE

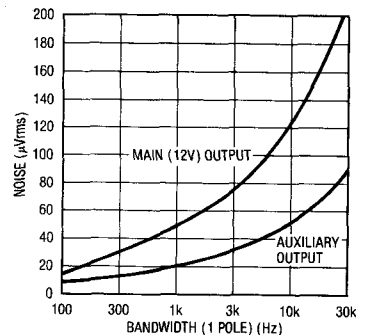
Short Circuit Current, 12V Output



Output Switching Characteristics



Output Voltage Noise



APPLICATIONS INFORMATION

General Information

The LT1036 is a dual output regulator. The main 12V output is capable of delivering up to 3A of load current and can be shut down with a logic signal. The auxiliary 5V output supplies a minimum of 75mA and is unaffected by the logic signal. The outputs are trimmed to $\pm 2\%$ initial tolerance and exhibit excellent line and load regulation.

The logic control feature makes the LT1036 ideal for many system applications where it is desirable to power-up a portion of the system for a period of time, and then power the system down during a standby operation. Applications such as multiple power supply sequencing, elimination of expensive AC and DC power switches, delayed start applications, switching 12V DC loads, and many others are now easily accomplished.

Timing functions, such as delayed power-up or power-down, can also be performed directly at the enable pin.

Because a logic low on the enable pin shuts down the main regulator, feedback from output to enable can be used to generate hysteresis or latching functions.

The low quiescent current drain of the LT1036 makes it useful in battery-powered or battery back-up applications. The enable pin can be used as a "low battery" detector or to shut down major portions of system power, allowing memory portions to continue to operate from the auxiliary output. At low output currents, the auxiliary output will regulate with input voltage typically as low as 6.2V, giving maximum battery life.

Good design practice with all regulators is to bypass the input and output terminals. A $2\mu\text{F}$ solid tantalum at the input and at both outputs is suggested. For the applications which follow, the bypass capacitors are still recommended, but for simplicity are not shown on the diagram. It is also recommended that for maximum noise immunity the voltage enable pin be tied high if it is unused. It can be tied directly to V_{IN} , as shown in Figure 1, or to the auxiliary output. If the enable pin is left open, it will float to a high logic level of approximately 1.6V and the main output regulator will be at 12V.

The enable pin is fully protected against input voltages up to 30V, even if the power input voltage is zero.

The basic shutdown control circuit uses a direct gate drive or an open collector driver and a pull-up resistor which are tied to V_{AUX} , as shown in Figure 2.

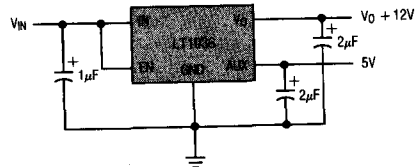


Figure 1

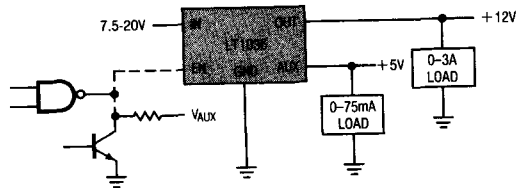


Figure 2

Driving the Enable Pin

The enable pin equivalent schematic is shown in Figure 3. Basically, enable pin current is zero above the threshold and about $1.5\mu\text{A}$ below the threshold, flowing out of the pin. Standard logic, such as TTL and CMOS, will interface directly to the enable pin, even if the logic output swing is higher than the input voltage (V_{IN}) to the regulator. 15V CMOS can be used to drive the enable pin, even if the regulator is not powered up, without loading the CMOS output.

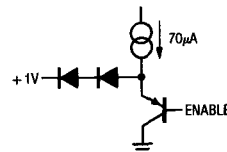


Figure 3

Timing functions, such as delayed power-up or power-down, can be implemented by driving the enable pin with an RC network. The current flowing out of the enable pin should not be used as the timing current in delayed power-up applications as it is temperature sensitive and varies somewhat from device to device. Instead, a resistor tied to the auxiliary output, the input, or to a logic signal

APPLICATIONS INFORMATION

should be used. The timing resistor chosen should provide at least 25 μ A of current to "swamp out" the effects of the internal current.

Main Output Current/Voltage Characteristics

Following a high to low transition at the enable pin, the main regulator output will begin to drop after a delay of approximately 0.4 μ s. With no capacitive load, the output will fall to zero in approximately 0.8 μ s ($R_L = 4\Omega$ to 100 Ω). With a capacitive load, fall time is limited by the RC product of the load and the output capacitance. For light loads ($R_L > 400\Omega$), the discharge time is controlled by an internal current pull-down of 15mA for output voltages down to 1.5V. Below 1.5V, the pull-down current drops to \approx 4mA. The DC output voltage in the shutdown mode is approximately 0.12V due to an internal current path in the regulator. (See Figure 4)

The user should note that the output in the low state can only sink about 3mA. If current is forced into the output, the output voltage will rise to 1V at 5mA and about 1.5V at 10mA. With no output capacitor, the rise time of the main output is about 12 μ s. With an output capacitor, rise time is limited by the short circuit current of the LT1036 and the load capacitance. A 10 μ F output capacitor slows the output rise time to approximately 80 μ s.

Output Current

The main output current limits at about 4A for input voltages below 20V. Internal foldback, or "power limiting", circuitry detects the input-output voltage differential and reduces current limit for input to output voltages exceeding 8V. With 25V input, for instance, short circuit current is reduced to \approx 0.9A.

An additional feature of the LT1036 is that the auxiliary supply does not incorporate, nor is it affected by, thermal shutdown. Any fault condition of the main regulator will not affect the auxiliary output voltage.

The following applications circuits will serve to indicate the versatility of the LT1036.

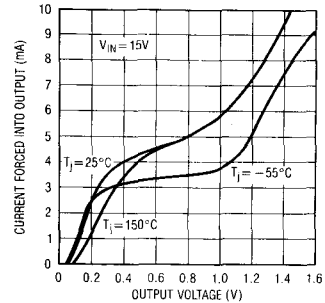
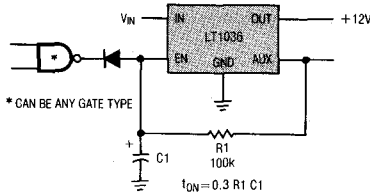


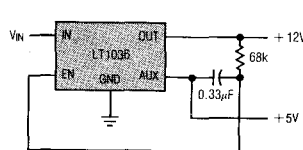
Figure 4

TYPICAL APPLICATIONS

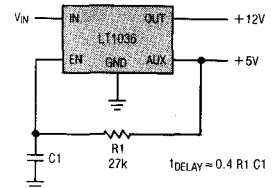
Fast Turn-Off, Delayed Turn-On



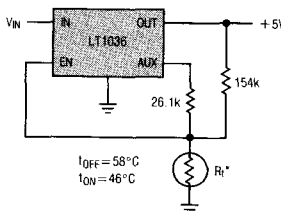
Latch-Off with Output Short



Delayed Power-Up

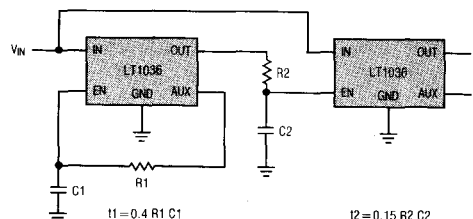


Thermal Cutoff at High Ambient Temperature



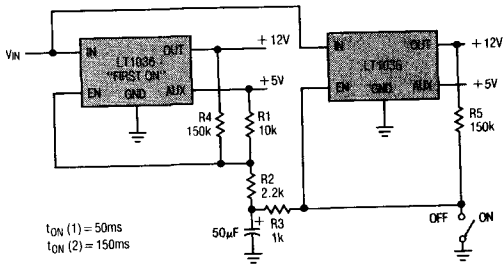
*YELLOW SPRINGS #44008, 30k Ω @ 25°C

Power Supply Turn-On Sequencing

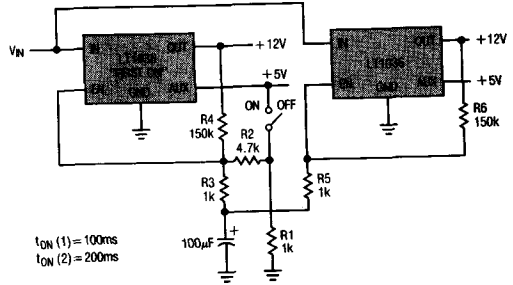


TYPICAL APPLICATIONS

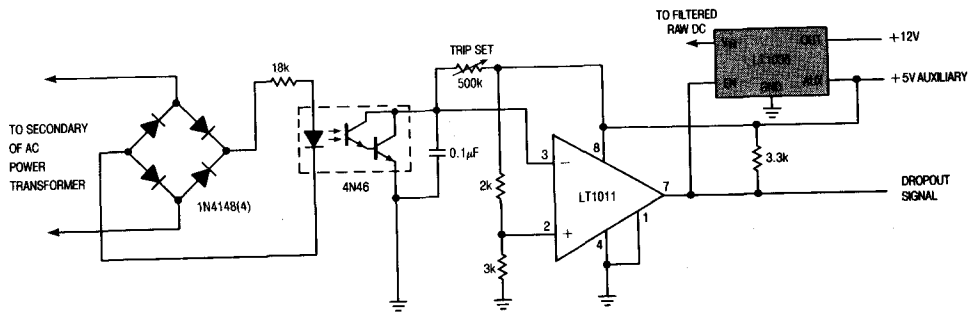
First-On, Last-Off Sequencing



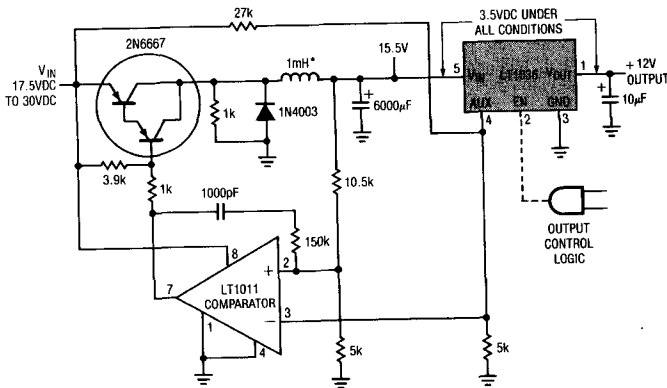
First-On, First-Off Sequencing



Line Dropout Detector

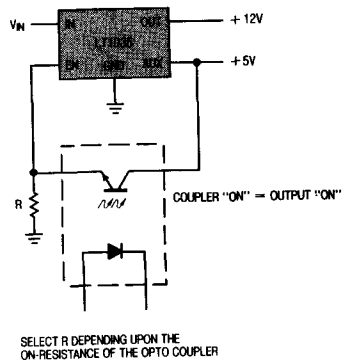


Low Dissipation Regulator



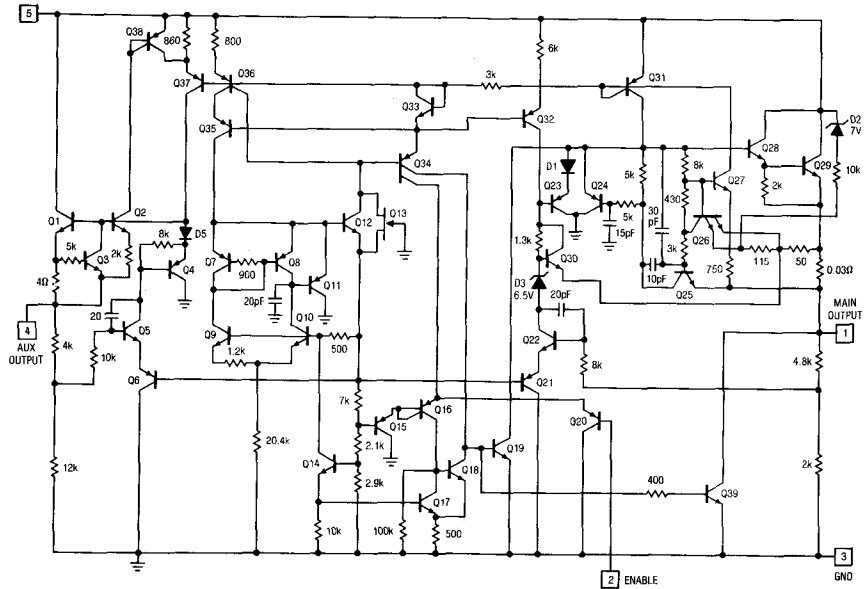
*DALE TD-5
 THIS CIRCUIT IS DESIGNED TO REDUCE POWER DISSIPATION
 IN THE LT1036 OVER A 90VAC-140VAC INPUT RANGE.

Opto-Coupled Output Control



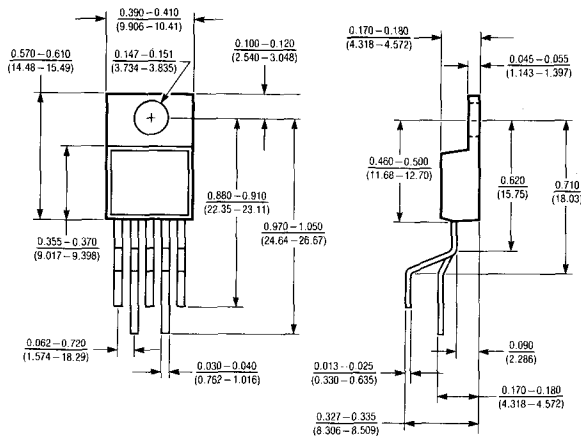
LT1036M/LT1036C

SCHEMATIC DIAGRAM



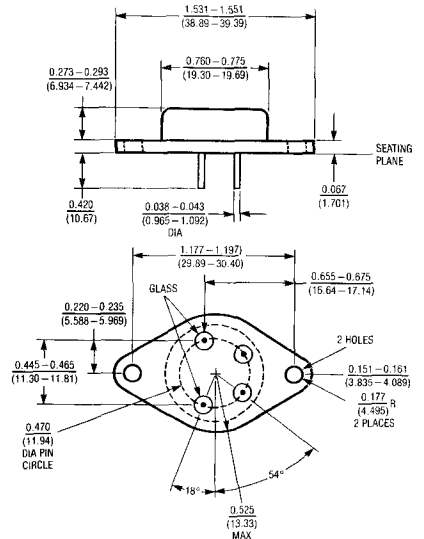
PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

TO-220 Package (5 Lead)



	T_{jMAX}	θ_{jC}
LT1036C	125°C	3°C/W

4-Pin Metal Package Similar to JEDEC TO-3



	T_{jMAX}	θ_{jC}
LT1036M	150°C	2.5°C/W
LT1036C	125°C	2.5°C/W

FEATURES

- *Guaranteed* 0.8% Initial Tolerance
- *Guaranteed* 0.4% Load Regulation
- *Guaranteed* 10 Amp Output Current
- 100% Thermal Limit Burn-in
- 24 Amp Transient Output Current
- Standard Adjustable Pinout
- Operates to 35V

APPLICATIONS

- System Power Supplies
- High Power Linear Regulator
- Battery Chargers
- Power Driver
- Constant Current Regulator

DESCRIPTION

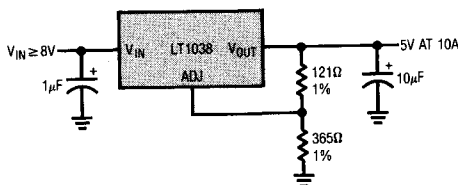
The LT1038 is a three terminal regulator which is capable of providing in excess of 10 amps output current over 1.2V to 32V range. The device is packaged in a standard TO-3 power package, and is plug-in compatible with industry standard adjustable regulators, such as the LM117 and LM138. Also, the LT1038 is a functional replacement for the LM396.

In addition to excellent load and line regulations, the LT1038 is fully protected by current limiting, safe area protection and thermal shutdown. New current limiting circuitry allows transient load currents up to 24 amps to be supplied for 500 μ s without causing the regulator to current limit and drop out of regulation during the transient.

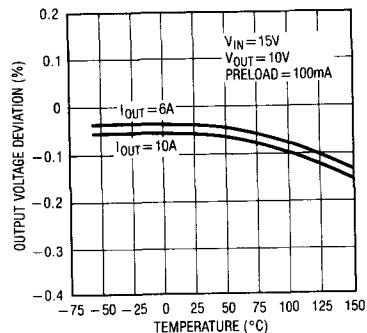
On-chip trimming of initial reference voltage to $\pm 0.8\%$ combined with 0.4% load regulation minimize errors in all high current applications. Further, the LT1038 is manufactured with standard bipolar processing and has Linear Technology's high reliability.

4

5V, 10 Amp Regulator



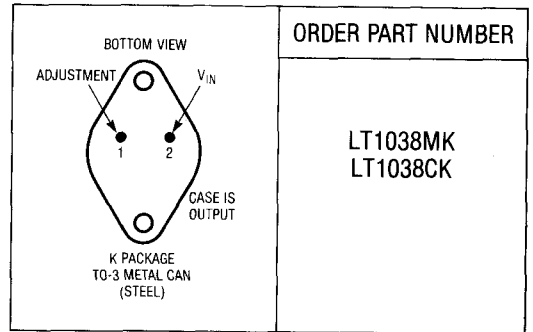
Load Regulation



ABSOLUTE MAXIMUM RATINGS

Power Dissipation Internally Limited
 Input to Output Voltage Differential 35V
 Operating Junction Temperature Range
 LT1038M
 Control Circuitry -55°C to 150°C
 Power Transistor -55°C to 200°C
 LT1038C
 Control Circuitry 0°C to 125°C
 Power Transistor 0°C to 175°C
 Storage Temperature -65°C to 150°C
 Lead Temperature (Soldering, 10 sec.) 300°C

PACKAGE/ORDER INFORMATION



PRECONDITIONING 100% THERMAL LIMIT BURN-IN

ELECTRICAL CHARACTERISTICS (See Note 1)

SYMBOL	PARAMETER	CONDITIONS	LT1038M			LT1038C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V _{REF}	Reference Voltage	I _{OUT} = 20mA, T _J = 25°C	1.24	1.25	1.26	1.23	1.25	1.275	V
		3V ≤ (V _{IN} - V _{OUT}) ≤ 35V 20mA ≤ I _{OUT} ≤ 10A, P ≤ 75W	●	1.22	1.25	1.285	1.22	1.25	1.285
$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	Line Regulation	3V ≤ (V _{IN} - V _{OUT}) ≤ 35V, I _{OUT} = 20mA (See Note 2) T _A = 25°C	●						
				0.005	0.01		0.005	0.02	%/V
				0.02	0.03		0.02	0.03	%/V
$\frac{\Delta V_{OUT}}{\Delta I_{OUT}}$	Load Regulation	20mA ≤ I _{OUT} ≤ 10A (See Note 2) T _A = 25°C							
		3V ≤ (V _{IN} - V _{OUT}) ≤ 35V 3V ≤ (V _{IN} - V _{OUT}) ≤ 35V	●		0.1	0.4		0.1	0.6
				0.3	0.8		0.3	1	%
	Thermal Regulation	T _A = 25°C, 20ms Pulse		0.002	0.005		0.002	0.01	%/W
	Ripple Rejection	V _{OUT} = 10V, f = 120Hz C _{ADJ} = 0	●	60			60		dB
		C _{ADJ} = 10μF	●	60	75		60	75	dB
I _{ADJ}	Adjust Pin Current		●	50	100		50	100	μA
ΔI _{ADJ}	Adjust Pin Current Change	20mA ≤ I _{OUT} ≤ 10A 3V ≤ (V _{IN} - V _{OUT}) ≤ 35V	●				0.2	3	μA
	Minimum Load Current	(V _{IN} - V _{OUT}) = 35V	●	7	20		7	20	mA
		(V _{IN} - V _{OUT}) ≤ 20V	●		10			10	mA
I _{SC}	Current Limit	(V _{IN} - V _{OUT}) ≤ 10V DC	●	10	14		10	14	A
		Transient (0.5ms)	●	14	22		14	22	A
		(V _{IN} - V _{OUT}) = 30V, T _J = 25°C	●	1	2		1	2	A
$\frac{\Delta V_{OUT}}{\Delta Temp}$	Temperature Stability		●	1	2		1		%

ELECTRICAL CHARACTERISTICS (See Note 1)

SYMBOL	PARAMETER	CONDITIONS	LT1038M			LT1038C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
$\frac{\Delta V_{OUT}}{\Delta Time}$	Long Term Stability	$T_A = 125^\circ\text{C}$, 1000 Hours		0.3	1		0.3	1	%
e_n	RMS Output Noise (% of V_{OUT})	$T_A = 25^\circ\text{C}$, $10\text{Hz} \leq f \leq 10\text{kHz}$		0.001			0.001		%
Θ_{JC}	Thermal Resistance Junction to Case	Power Transistor Control Circuitry			1 0.5			1 0.5	$^\circ\text{C}/\text{W}$ $^\circ\text{C}/\text{W}$

The ● denotes the specifications which apply over the full operating temperature range.

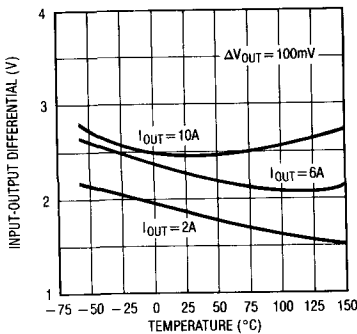
Note 1: Unless otherwise specified, these specifications apply: $V_{IN} - V_{OUT} = 5\text{V}$ and $I_{OUT} = 5\text{A}$. These specifications are applicable for power dissipations up to 75W. At input-output voltage differentials greater than 10V, achievable output current and power dissipation decrease due to protection circuitry.

Note 2: See thermal regulation specifications for changes in output voltage due to heating effects. Load and line regulation are measured at a constant junction temperature by low duty cycle pulse testing.

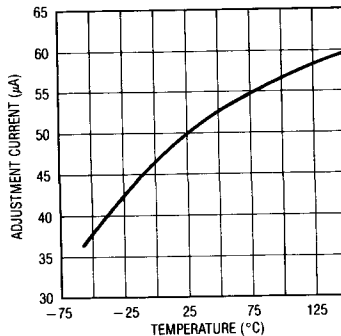
TYPICAL PERFORMANCE CHARACTERISTICS

4

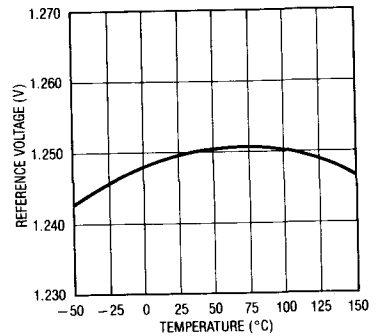
Dropout Voltage



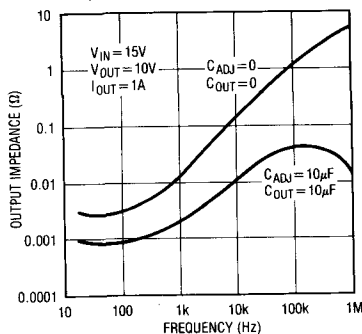
Adjustment Current



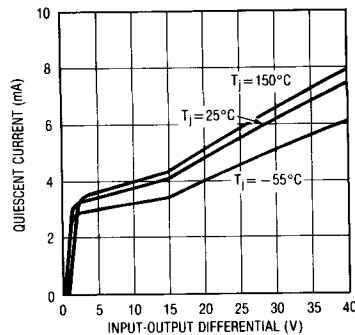
Temperature Stability



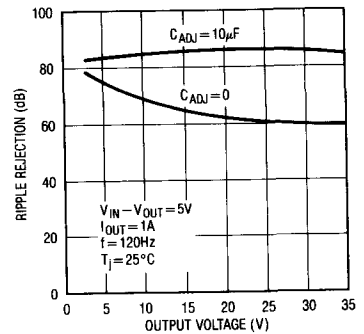
Output Impedance



Minimum Operating Current

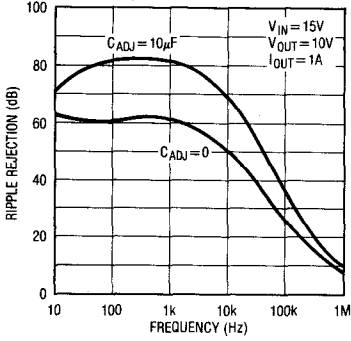


Ripple Rejection

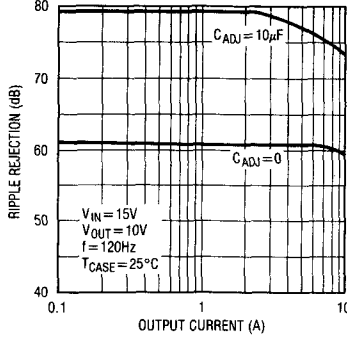


TYPICAL PERFORMANCE CHARACTERISTICS

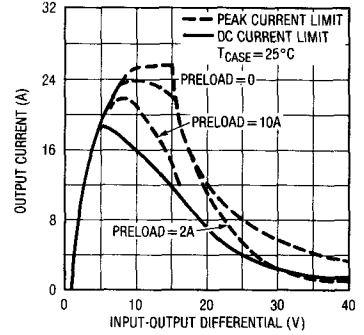
Ripple Rejection



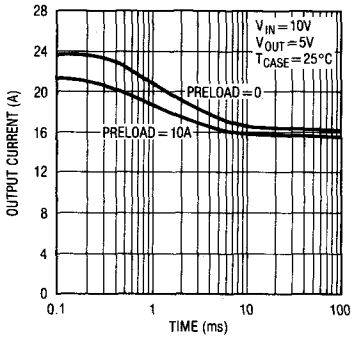
Ripple Rejection



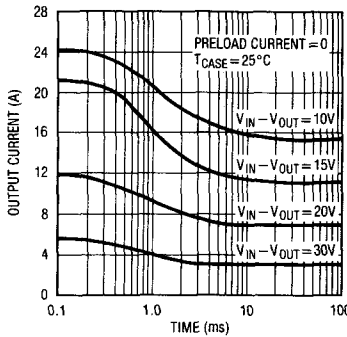
Current Limit



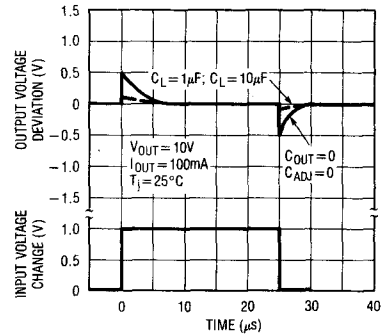
Current Limit



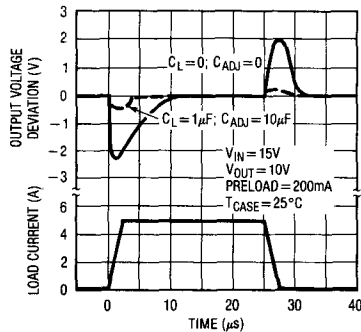
Current Limit



Line Transient Response



Load Transient Response



APPLICATIONS INFORMATION

General

The LT1038 develops a 1.25V reference voltage between the output and the adjustment terminal (see Figure 1). By placing a resistor, R1, between these two terminals, a constant current is caused to flow through R1 and down through R2 to set the overall output voltage. Normally this current is the specified minimum load current of 10 or 20mA. Because I_{ADJ} is very small and constant when compared with the current through R1, it represents a small error and can usually be ignored.

Bypass Capacitors

Input bypassing using a 1 μ F tantalum or 25 μ F electrolytic is recommended when the input filter capacitors are more than 5 inches from the device. Improved ripple rejection (80dB) can be accomplished by adding a 10 μ F capacitor from the adjust pin to ground. Increasing the size of the capacitor to 20 μ F will help ripple rejection at low output voltage since the reactance of this capacitor should be small compared to the voltage setting resistor, R2. For improved AC transient response and to prevent the possibil-

ity of oscillation due to unknown reactive load, a 1 μ F capacitor is also recommended at the output. Because of their low impedance at high frequencies, the best type of capacitor to use is solid tantalum.

Protection Diodes

The LT1038 does not require a protection diode from the adjustment terminal to the output (see Figure 2). Improved internal circuitry eliminates the need for this diode when the adjustment pin is bypassed with a capacitor to improve ripple rejection.

If a very large output capacitor is used, such as a 100 μ F shown in Figure 2, the regulator could be damaged or destroyed if the input is accidentally shorted to ground or crowbarred, due to the output capacitor discharging into the output terminal of the regulator. To prevent this, a diode, D1 as shown, is recommended to safely discharge the capacitor.

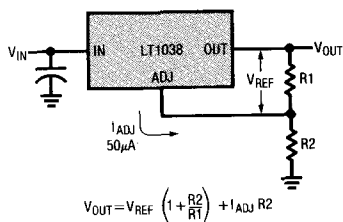


Figure 1. Basic Adjustable Regulator

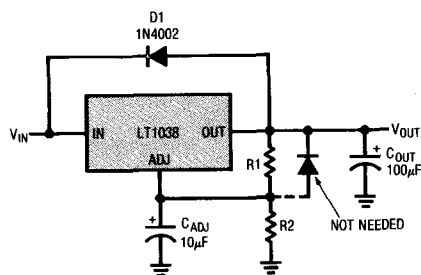


Figure 2

APPLICATIONS INFORMATION

Load Regulation

Because the LT1038 is a three-terminal device, it is not possible to provide true remote load sensing. Load regulation will be limited by the resistance of the wire connecting the regulator to the load. The data sheet specification for load regulation is measured at the bottom of the package. Negative side sensing can be a true Kelvin connection if the bottom of resistor R2 is returned to the negative side of the load. Although it may not be immediately obvious, best load regulation is obtained when the top of the resistor divider, R1, is connected *directly* to the case, *not to the load*. This is illustrated in Figure 3. If

R1 were connected to the load, the effective resistance between the regulator and the load would be

$$R_p \times \left(\frac{R_2 + R_1}{R_1} \right), R_p = \text{Parasitic Line Resistance.}$$

Connected as shown, R_p is not multiplied by the divider ratio. R_p is about 0.004Ω per foot using 16 gauge wire. This translates to 4mV/ft at 1A load current, so it is important to keep the lead between the regulator and the load as short as possible, and use large wire or PC board traces.

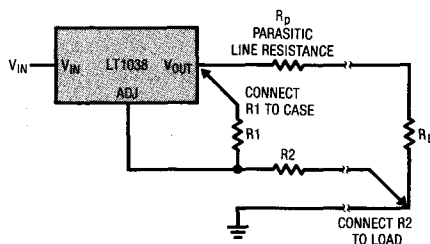
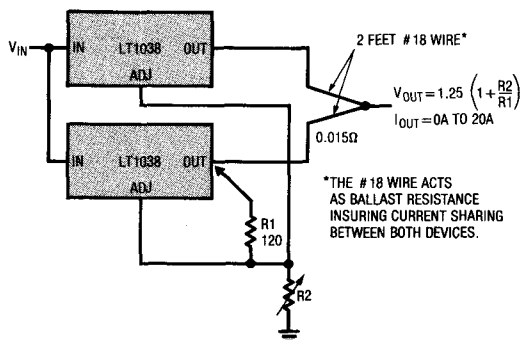


Figure 3. Connections for Best Load Regulation

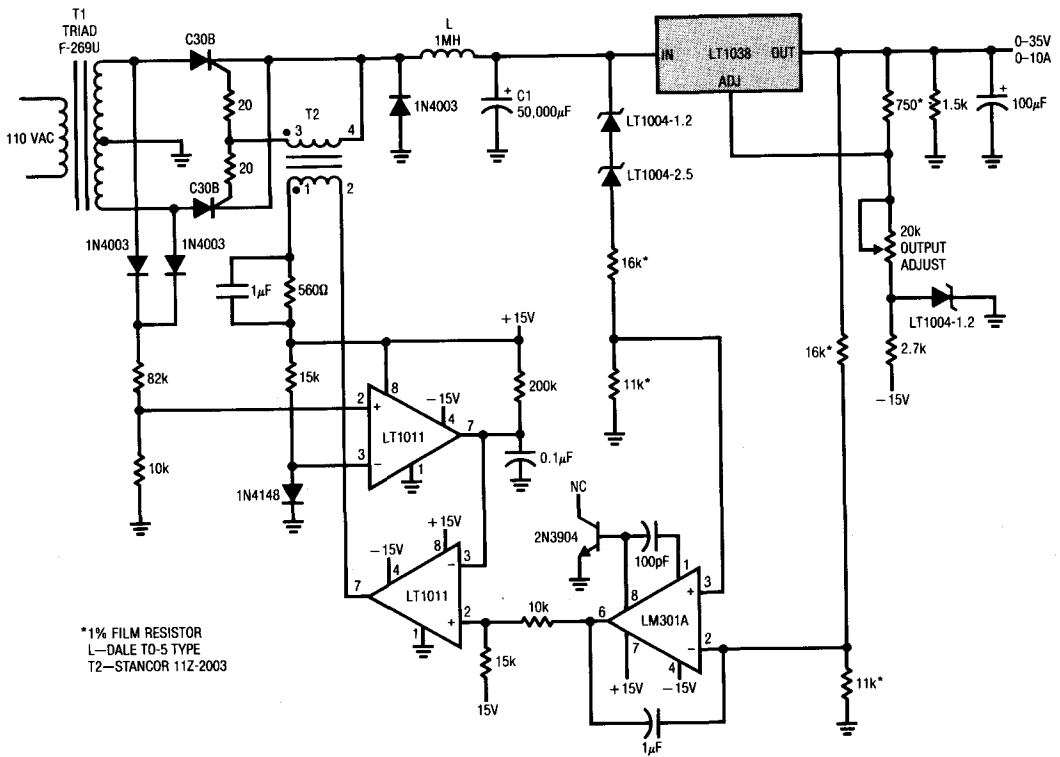
TYPICAL APPLICATIONS

Paralleling Regulators



TYPICAL APPLICATIONS

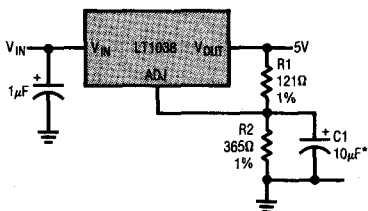
10 Amp Variable Regulator*



GENERAL PURPOSE REGULATOR WITH SCR PREREGULATOR TO LOWER POWER DISSIPATION. ABOUT 4V DIFFERENTIAL IS MAINTAINED ACROSS THE LT1038 INDEPENDENT OF OUTPUT VOLTAGE AND LOAD CURRENT.

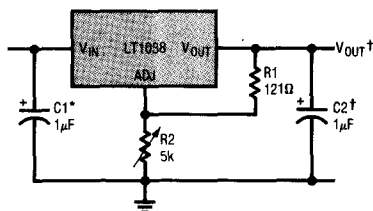
TYPICAL APPLICATIONS

Improving Ripple Rejection



*C1 IMPROVES RIPPLE REJECTION. X_C SHOULD BE SMALL COMPARED TO R2.

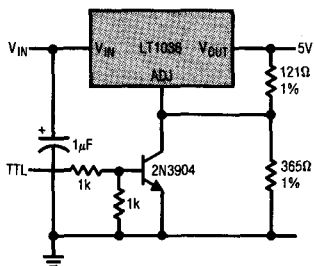
1.2V-25V Adjustable Regulator



*NEEDED IF DEVICE IS FAR FROM FILTER CAPACITORS
†OPTIONAL—IMPROVES TRANSIENT RESPONSE

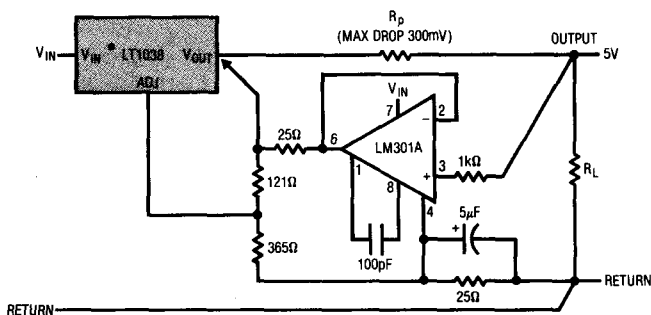
$$\dagger\dagger V_{OUT} = 1.25V \left(1 + \frac{R2}{R1} \right)$$

5V Regulator with Shutdown



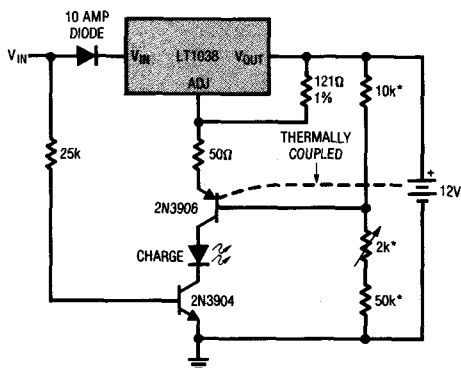
TYPICAL APPLICATIONS

Remote Sensing



4

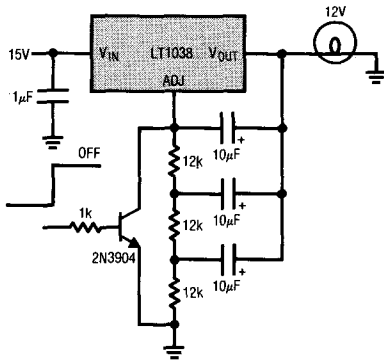
Temperature Compensated Lead Acid Battery Charger



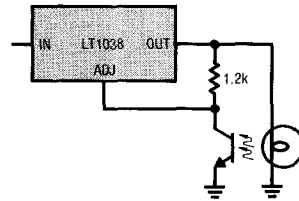
*LOAD ON BATTERY ≈ 200μA WHEN NOT CHARGING

TYPICAL APPLICATIONS

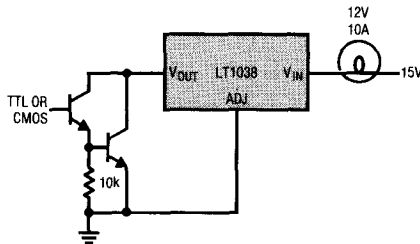
Lamp Flasher



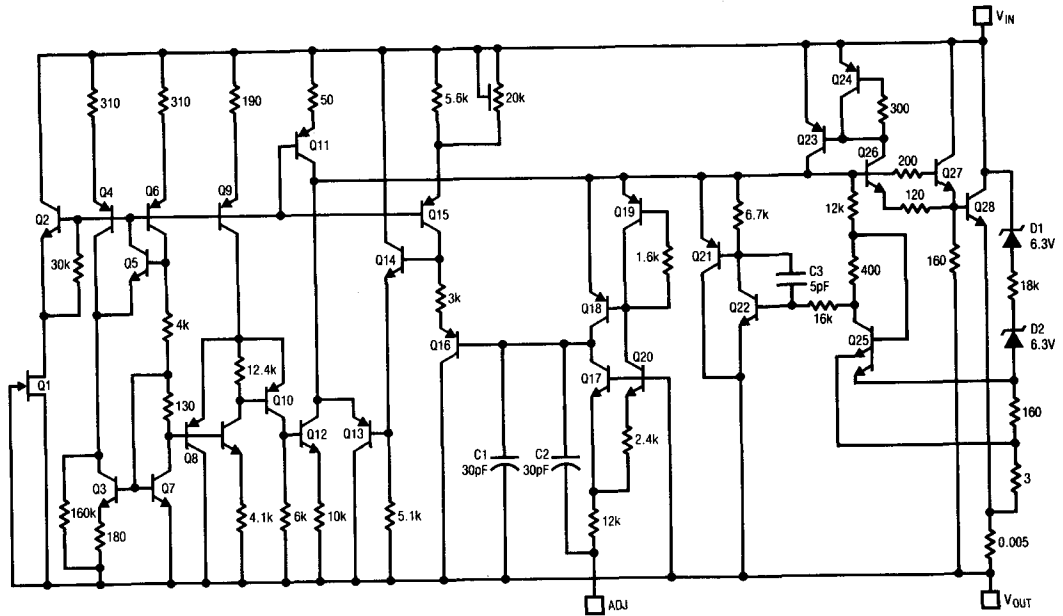
Automatic Light Control



Protected High Current Lamp Driver



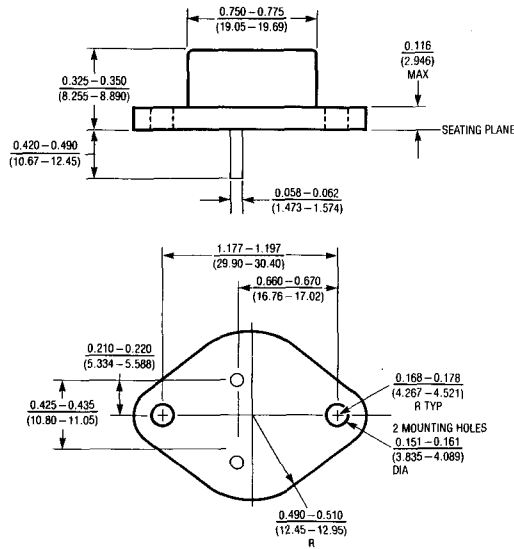
SCHEMATIC DIAGRAM



4

PACKAGE DESCRIPTION

K Package TO-3 Steel Metal Can



FEATURES

- Three Terminal Adjustable
- Output Current of 3A, 5A or 7.5A
- Operates Down to 1V Dropout
- Guaranteed Dropout Voltage at Multiple Current Levels
- 0.015% Line Regulation
- 0.01% Load Regulation
- 100% Thermal Limit Burn-In
- Fixed Versions Available

APPLICATIONS

- High Efficiency Linear Regulators
- Post Regulators for Switching Supplies
- Constant Current Regulators
- Battery Chargers

DESCRIPTION

The LT1083 series of positive adjustable regulators are designed to provide 7.5A, 5A and 3A with higher efficiency than currently available devices. All internal circuitry is designed to operate down to 1V input to output differential and the dropout voltage is fully specified as a function of load current. Dropout is guaranteed at a maximum of 1.5V at maximum output current, decreasing at lower load currents. On-chip trimming adjusts the reference voltage to 1%. Current limit is also trimmed, minimizing the stress on both the regulator and power source circuitry under overload conditions.

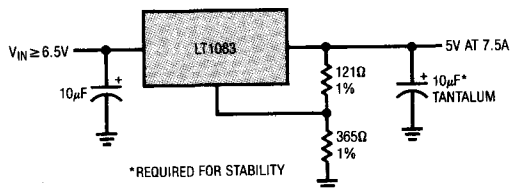
The LT1083 series devices are pin compatible with other three terminal regulators. A 10 μ F output capacitor is required on these devices; however, this is usually included in most regulator designs.

Unlike PNP regulators, where up to 10% of the output current is wasted as quiescent current, the LT1083 quiescent current flows into the load, increasing efficiency.

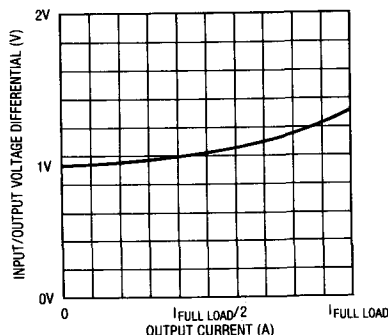
DEVICE	OUTPUT CURRENT
LT1083	7.5 Amps
LT1084	5.0 Amps
LT1085	3.0 Amps

*For a 1.5A low dropout regulator see the LT1086 data sheet.

5V, 7.5A Regulator



Dropout Voltage vs
 Output Current



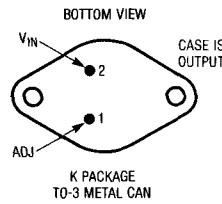
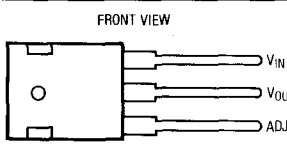
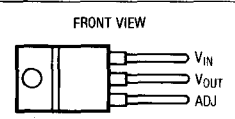
ABSOLUTE MAXIMUM RATINGS

Power Dissipation Internally Limited
 Input to Output Voltage Differential
 "M" Grades 35V
 "C" Grades 30V
 Operating Junction Temperature Range
 "M" Grades
 Control Section -55°C to 150°C
 Power Transistor -55°C to 200°C
 "C" Grades
 Control Section 0°C to 125°C
 Power Transistor 0°C to 150°C
 Storage Temperature -65°C to 150°C
 Lead Temperature (Soldering, 10 sec) 300°C

PRECONDITIONING

100% Thermal Limit Burn-In

PACKAGE/ORDER INFORMATION

 <p>BOTTOM VIEW V_{IN} CASE IS OUTPUT ADJ K PACKAGE TO-3 METAL CAN</p>	ORDER PART NUMBER	
	LT1083MK	LT1084CK
 <p>FRONT VIEW V_{IN} V_{OUT} ADJ P PACKAGE TO-3P PLASTIC</p>	LT1083CP	LT1084CP
	 <p>FRONT VIEW V_{IN} V_{OUT} ADJ T PACKAGE TO-220 PLASTIC</p>	LT1084CT

ELECTRICAL CHARACTERISTICS (See Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Reference Voltage	I _{OUT} = 10mA, T _J = 25°C, (V _{IN} - V _{OUT}) = 3V (K Package Only) 10mA ≤ I _{OUT} ≤ I _{FULL LOAD} 1.5V ≤ (V _{IN} - V _{OUT}) ≤ 25V (Notes 3, 5)	1.238	1.250	1.262	V
Line Regulation	I _{LOAD} = 10mA, 1.5V ≤ (V _{IN} - V _{OUT}) ≤ 15V, T _J = 25°C	●	0.015	0.2	%
	M Grade	●	0.035	0.2	%
	15V ≤ (V _{IN} - V _{OUT}) ≤ 35V	●	0.05	0.5	%
	C Grade	●	0.05	0.5	%
15V ≤ (V _{IN} - V _{OUT}) ≤ 30V (Notes 1, 2)	●	0.05	0.5	%	
Load Regulation	(V _{IN} - V _{OUT}) = 3V 10mA ≤ I _{OUT} ≤ I _{FULL LOAD} T _J = 25°C (Notes 1, 2, 3, 5)	●	0.1	0.3	%
	●	0.2	0.4	%	
Dropout Voltage	ΔV _{REF} = 1%, I _{OUT} = I _{FULL LOAD} , (Notes 4, 5)	●	1.3	1.5	V
Current Limit	(V _{IN} - V _{OUT}) = 5V	●	8.0	9.5	A
LT1084	(V _{IN} - V _{OUT}) = 5V	●	5.5	6.5	A
LT1085	(V _{IN} - V _{OUT}) = 5V	●	3.2	4	A

ELECTRICAL CHARACTERISTICS (See Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Minimum Load Current	$(V_{IN} - V_{OUT}) = 25V$	●	5	10	mA
Thermal Regulation LT1083 LT1084 LT1085	$T_A = 25^\circ C$, 30ms pulse		0.002 0.003 0.004	0.01 0.015 0.02	%/W %/W %/W
Ripple Rejection	$f = 120Hz$ $C_{ADJ} = 25\mu F$, $C_{OUT} = 25\mu F$ Tantalum $I_{OUT} = I_{FULL\ LOAD}$, $(V_{IN} - V_{OUT}) = 3V$ (Note 5)	●	60	75	dB
Adjust Pin Current	$T_J = 25^\circ C$	●	55	120	μA μA
Adjust Pin Current Change	$10mA \leq I_{OUT} \leq I_{FULL\ LOAD}$ $1.5V \leq (V_{IN} - V_{OUT}) \leq 25V$ (Note 5)	●	0.2	5	μA
Temperature Stability		●	0.5		%
Long Term Stability	$T_A = 125^\circ C$, 1000 Hrs.		0.3	1	%
RMS Output Noise (% of V_{OUT})	$T_A = 25^\circ C$ $10Hz \leq f \leq 10kHz$		0.003		%
Thermal Resistance Junction to Case LT1083	K Package: Control Circuitry/Power Transistor			0.6/1.6	$^\circ C/W$
LT1084	P Package: Control Circuitry/Power Transistor			0.5/1.6	$^\circ C/W$
	K Package: Control Circuitry/Power Transistor			0.75/2.3	$^\circ C/W$
	P Package: Control Circuitry/Power Transistor			0.65/2.3	$^\circ C/W$
	T Package: Control Circuitry/Power Transistor			0.65/2.7	$^\circ C/W$
LT1085	K Package: Control Circuitry/Power Transistor			0.9/3.0	$^\circ C/W$
	T Package: Control Circuitry/Power Transistor			0.7/3.0	$^\circ C/W$

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: See thermal regulation specifications for changes in output voltage due to heating effects. Load and line regulation are measured at a constant junction temperature by low duty cycle pulse testing.

Note 2: Line and load regulation are guaranteed up to the maximum power dissipation (60W for the LT1083, 45W for the LT1084 (K, P), 30W for the LT1084 (T) and 30W for the LT1085). Power dissipation is determined by the input/output differential and the output current. Guaranteed maximum power dissipation will not be available over the full input/output voltage range.

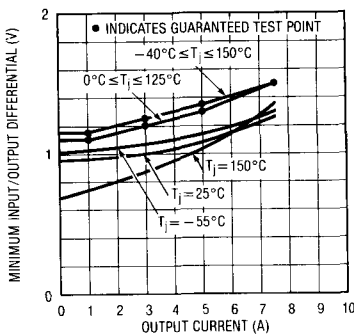
Note 3: $I_{FULL\ LOAD}$ is defined in the current limit curves. The $I_{FULL\ LOAD}$ curve is defined as the minimum value of current limit as a function of input to output voltage. Note that the 60W power dissipation for the LT1083 (45W for the LT1084 (K, P), 30W for the LT1084 (T), 30W for the LT1085) is only achievable over a limited range of input to output voltage.

Note 4: Dropout voltage is specified over the full output current range of the device. Test points and limits are shown on the Dropout Voltage curve.

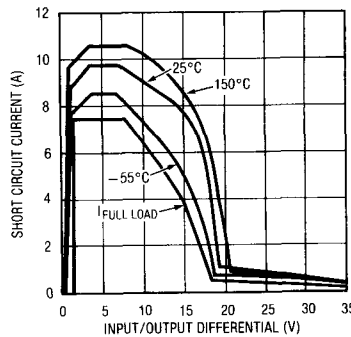
Note 5: For LT1083 $I_{FULL\ LOAD}$ is 5A for $-55^\circ C \leq T_J < -40^\circ C$ and 7.5A for $T_J \geq -40^\circ C$.

TYPICAL PERFORMANCE CHARACTERISTICS

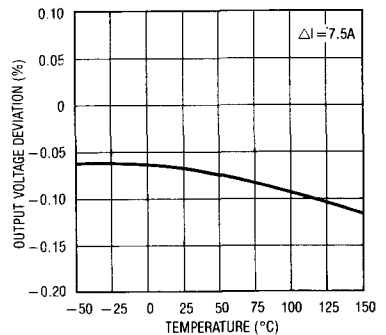
LT1083 Dropout Voltage



LT1083 Short Circuit Current

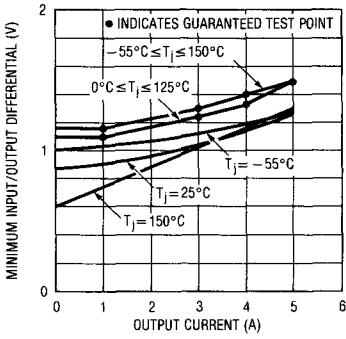


LT1083 Load Regulation

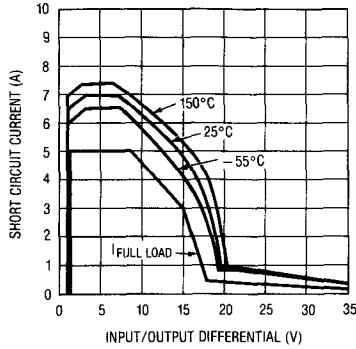


TYPICAL PERFORMANCE CHARACTERISTICS

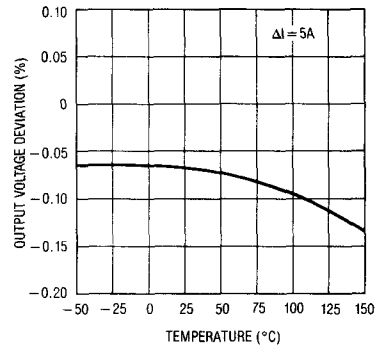
LT1084 Dropout Voltage



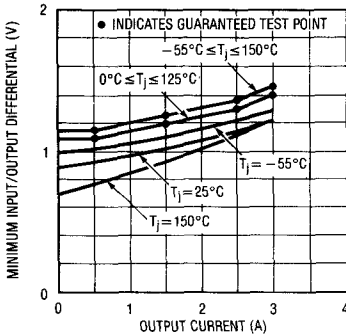
LT1084 Short Circuit Current



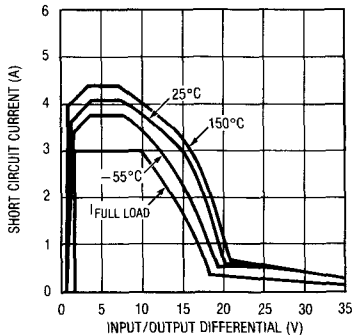
LT1084 Load Regulation



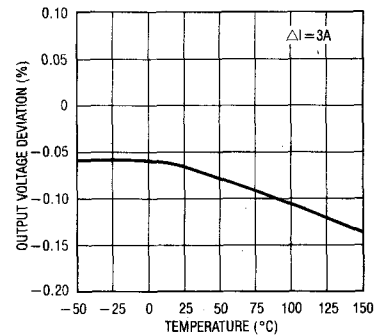
LT1085 Dropout Voltage



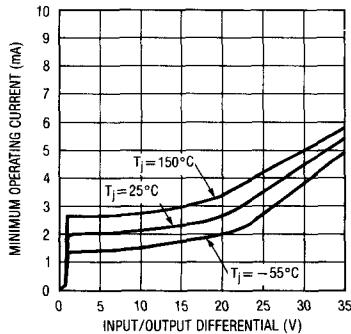
LT1085 Short Circuit Current



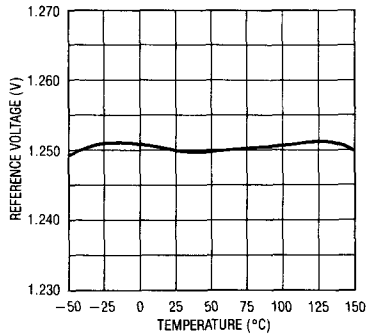
LT1085 Load Regulation



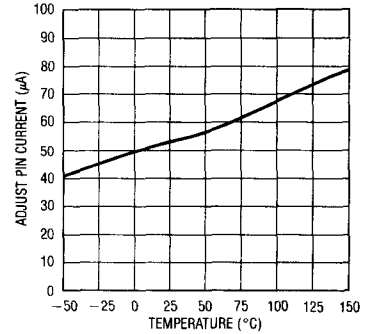
Minimum Operating Current



Temperature Stability

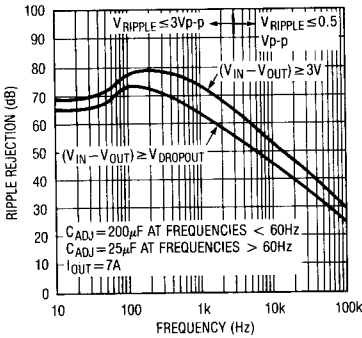


Adjust Pin Current

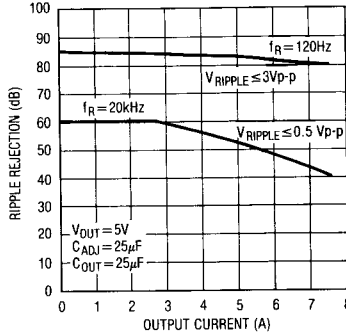


TYPICAL PERFORMANCE CHARACTERISTICS

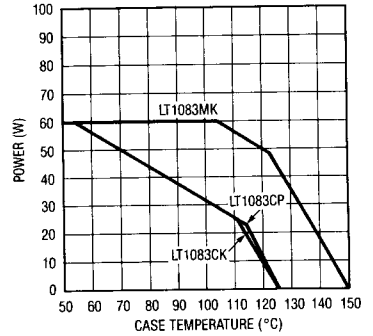
LT1083 Ripple Rejection



LT1083 Ripple Rejection vs Current

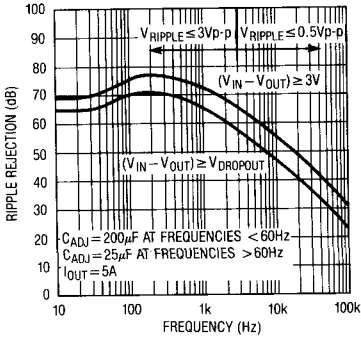


LT1083 Maximum Power Dissipation*

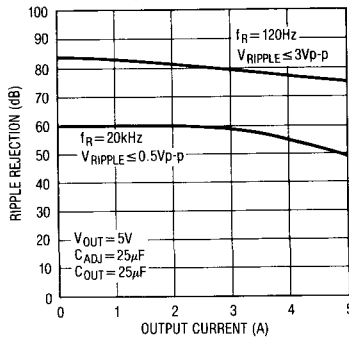


* AS LIMITED BY MAXIMUM JUNCTION TEMPERATURE

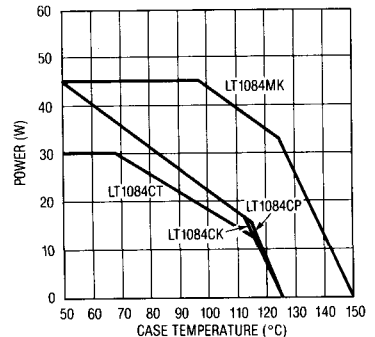
LT1084 Ripple Rejection



LT1084 Ripple Rejection vs Current



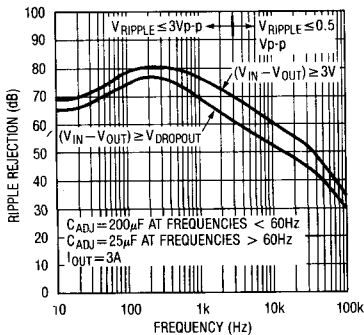
LT1084 Maximum Power Dissipation*



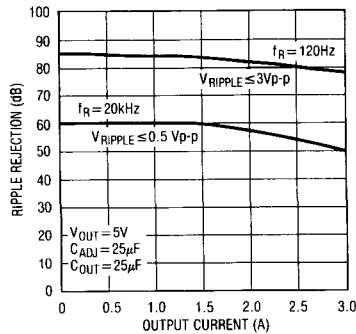
* AS LIMITED BY MAXIMUM JUNCTION TEMPERATURE

4

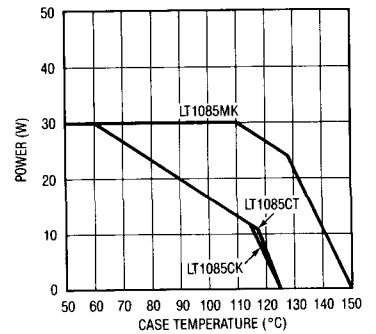
LT1085 Ripple Rejection



LT1085 Ripple Rejection vs Current

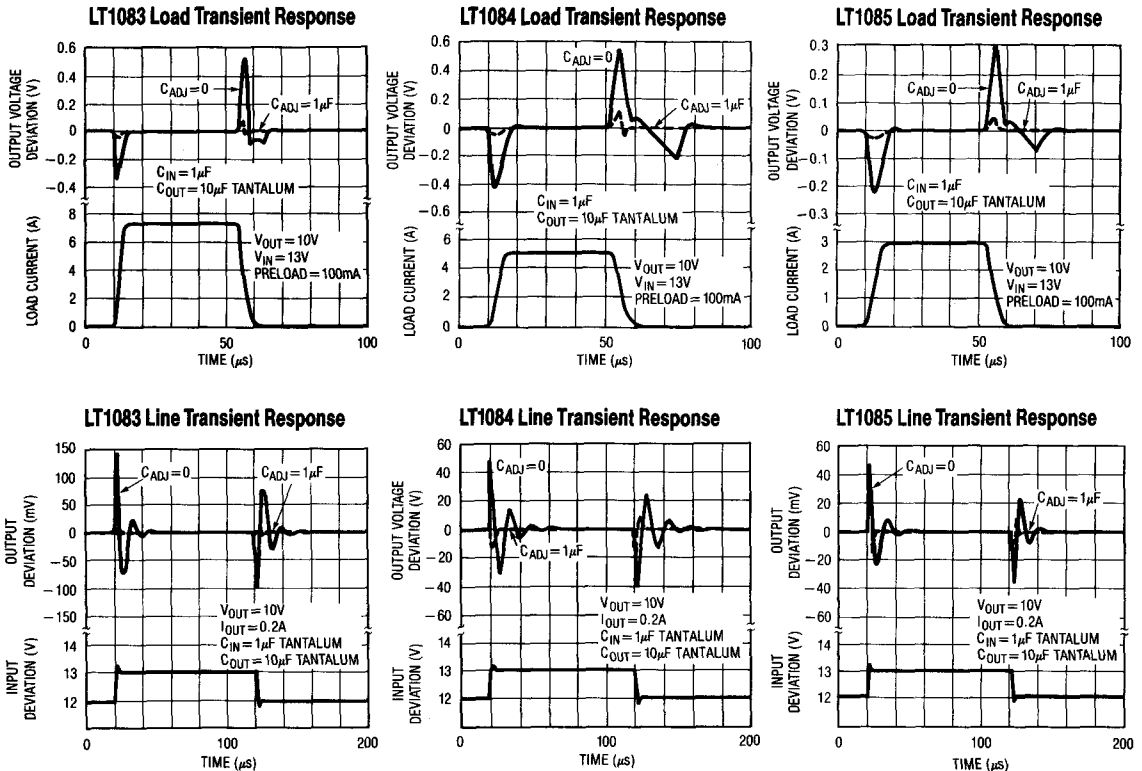


LT1085 Maximum Power Dissipation*



* AS LIMITED BY MAXIMUM JUNCTION TEMPERATURE

TYPICAL PERFORMANCE CHARACTERISTICS



APPLICATION HINTS

The LT1083 family of three terminal adjustable regulators is easy to use and has all the protection features that are expected in high performance voltage regulators. They are short circuit protected, have safe area protection as well as thermal shutdown to turn off the regulator should the temperature exceed about 165°C.

These regulators are pin compatible with older three terminal adjustable devices, offer lower dropout voltage and more precise reference tolerance. Further, the reference stability with temperature is improved over older types of regulators. The only circuit difference between using the LT1083 family and older regulators is that they require an output capacitor for stability.

Stability

The circuit design used in the LT1083 family requires the use of an output capacitor as part of the device frequency compensation. For all operating conditions, the addition of 150μF aluminum electrolytic or a 22μF solid tantalum on the output will ensure stability. Normally, capacitors much smaller than this can be used with the LT1083. Many different types of capacitors with widely varying characteristics are available. These capacitors differ in capacitor tolerance (sometimes ranging up to ±100%), equivalent series resistance, and capacitance temperature coefficient. The 150μF or 22μF values given will ensure stability.

APPLICATION HINTS

When the adjustment terminal is bypassed to improve the ripple rejection, the requirement for an output capacitor increases. The values of 22 μ F tantalum or 150 μ F aluminum cover all cases of bypassing the adjustment terminal. Without bypassing the adjustment terminal, smaller capacitors can be used with equally good results and the table below shows approximately what size capacitors are needed to ensure stability.

Recommended Capacitor Values

Input	Output	Adjustment
10 μ F	10 μ F Tantalum, 50 μ F Aluminum	None
10 μ F	22 μ F Tantalum, 150 μ F Aluminum	20 μ F

Normally, capacitor values on the order of 100 μ F are used in the output of many regulators to ensure good transient response with heavy load current changes. Output capacitance can be increased without limit and larger values of output capacitor further improve stability and transient response of the LT1083 regulators.

Another possible stability problem that can occur in monolithic IC regulators is current limit oscillations. These can occur because, in current limit, the safe area protection exhibits a negative impedance. The safe area protection decreases the current limit as the input-to-output voltage increases. That is the equivalent of having a negative resistance since increasing voltage causes current to decrease. Negative resistance during current limit is not unique to the LT1083 series and has been present on all power IC regulators. The value of the negative resistance is a function of how fast the current limit is folded back as input-to-output voltage increases. This negative resistance can react with capacitors or inductors on the input to cause oscillation during current limiting. Depending on the value of series resistance, the overall circuitry may end up unstable. Since this is a system problem, it is not necessarily easy to solve; however it does not cause any problems with the IC regulator and can usually be ignored.

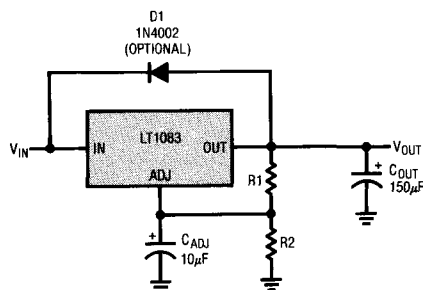
Protection Diodes

In normal operation, the LT1083 family does not need any protection diodes. Older adjustable regulators required

protection diodes between the adjustment pin and the output and from the output to the input to prevent overstressing the die. The internal current paths on the LT1083 adjustment pin are limited by internal resistors. Therefore, even with capacitors on the adjustment pin, no protection diode is needed to ensure device safety under short circuit conditions.

Diodes between input and output are usually not needed. The internal diode between the input and the output pins of the LT1083 family can handle microsecond surge currents of 50A to 100A. Even with large output capacitances, it is very difficult to get those values of surge currents in normal operations. Only with high value of output capacitors, such as 1000 μ F to 5000 μ F and with the input pin instantaneously shorted to ground, can damage occur. A crowbar circuit at the input of the LT1083 can generate those kinds of currents, and a diode from output to input is then recommended. Normal power supply cycling or even plugging and unplugging in the system will not generate current large enough to do any damage.

The adjustment pin can be driven on a transient basis ± 25 V, with respect to the output without any device degradation. Of course, as with any IC regulator, exceeding the maximum input to output voltage differential causes the internal transistors to break down and none of the protection circuitry is functional.



Overload Recovery

Like any of the IC power regulators, the LT1083 has safe area protection. The safe area protection decreases the current limit as input-to-output voltage increases and

APPLICATION HINTS

keeps the power transistor inside a safe operating region for all values of input-to-output voltage. The LT1083 protection is designed to provide some output current at all values of input-to-output voltage up to the device breakdown.

When power is first turned on, as the input voltage rises, the output follows the input, allowing the regulator to start up into very heavy loads. During the start-up, as the input voltage is rising, the input-to-output voltage differential remains small, allowing the regulator to supply large output currents. With high input voltage, a problem can occur wherein removal of an output short will not allow the output voltage to recover. Older regulators, such as the 7800 series, also exhibited this phenomenon, so it is not unique to the LT1083.

The problem occurs with a heavy output load when the input voltage is high and the output voltage is low, such as immediately after a removal of a short. The load line for such a load may intersect the output current curve at two points. If this happens, there are two stable output operating points for the regulator. With this double intersection, the power supply may need to be cycled down to zero and brought up again to make the output recover.

Ripple Rejection

The typical curves for ripple rejection reflect values for a bypassed adjustment pin. This curve will be true for all values of output voltage. For proper bypassing, and ripple rejection approaching the values shown, the impedance of the adjust pin capacitor, at the ripple frequency should equal the value of R1, (normally 100Ω-120Ω). The size of the required adjust pin capacitor is a function of the input ripple frequency. At 120Hz the adjust pin capacitor should be 13μF if R1 = 100Ω. At 10kHz only 0.16μF is needed.

For circuits without an adjust pin bypass capacitor, the ripple rejection will be a function of output voltage. The output ripple will increase directly as a ratio of the output voltage to the reference voltage (V_{OUT}/V_{REF}). For example, with the output voltage equal to 5V, and no adjust pin capacitor, the output ripple will be higher by the ratio of 5V/1.25V or 4 times larger. Ripple rejection will be degraded by 12dB from the value shown on the typical curve.

Output Voltage

The LT1083 develops a 1.25V reference voltage between the output and the adjust terminal (see Figure 1). By placing a resistor, R1, between these two terminals, a constant current is caused to flow through R1 and down through R2 to set the overall output voltage. Normally this current is the specified minimum load current of 10mA. Because I_{ADJ} is very small and constant when compared with the current through R1, it represents a small error and can usually be ignored.

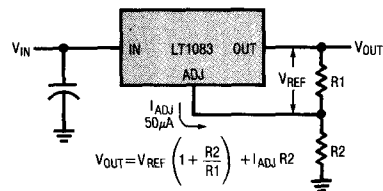


Figure 1. Basic Adjustable Regulator

Load Regulation

Because the LT1083 is a three-terminal device, it is not possible to provide true remote load sensing. Load regulation will be limited by the resistance of the wire connecting the regulator to the load. The data sheet specification for load regulation is measured at the bottom of the package. Negative side sensing is a true Kelvin connection, with the bottom of the output divider returned to the negative side of the load. Although it may not be immediately obvious, best load regulation is obtained when the top of the resistor divider, (R1), is connected *directly* to the case *not to the load*. This is illustrated in Figure 2. If R1 were connected to the load, the effective resistance between the regulator and the load would be

$$R_p \times \left(\frac{R_2 + R_1}{R_1} \right), R_p = \text{Parasitic Line Resistance.}$$

Connected as shown, R_p is not multiplied by the divider ratio. R_p is about 0.004Ω per foot using 16 gauge wire. This translates to 4mV/ft at 1A load current, so it is important to keep the positive lead between regulator and load as short as possible, and use large wire or PC board traces.

APPLICATION HINTS

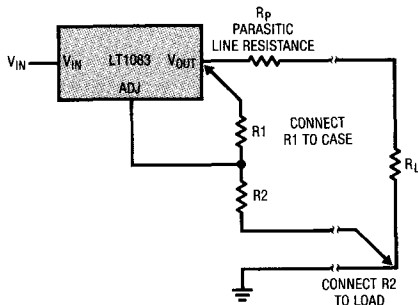


Figure 2. Connections for Best Load Regulation

Thermal Considerations

The LT1083 series of regulators have internal power and thermal limiting circuitry designed to protect the device under overload conditions. For continuous normal load conditions however, maximum junction temperature ratings must not be exceeded. It is important to give careful consideration to all sources of thermal resistance from junction to ambient. This includes junction to case, case to heat sink interface, and heat sink resistance itself. New thermal resistance specifications have been developed to more accurately reflect device temperature and ensure safe operating temperatures. The data section for these new regulators provides a separate thermal resistance and maximum junction temperature for both the *Control Section* and the *Power Transistor*. Previous regulators, with a single junction to case thermal resistance specification, used an average of the two values provided here and therefore could allow excessive junction temperatures under certain conditions of ambient temperature and heat sink resistance. To avoid this possibility, calculations should be made for both sections to ensure that both thermal limits are met.

Junction-to-case thermal resistance is specified from the IC junction to the bottom of the case directly below the die. This is the lowest resistance path for heat flow. Proper mounting is required to ensure the best possible thermal flow from this area of the package to the heat sink. Thermal compound at the case-to-heat-sink interface is strongly recommended. If the case of the device must be electrically isolated, a thermally conductive spacer can be used, as long as its added contribution to thermal resistance is considered. Note that the case of all devices in this series is electrically connected to the output.

For example, using a LT1083CK (TO-3, Commercial) and assuming:

$$V_{IN} \text{ (max continuous)} = 9V, V_{OUT} = 5V, I_{OUT} = 6A,$$

$$T_{AMBIENT} = 75^{\circ}C, \theta_{HEAT-SINK} = 1^{\circ}C/W,$$

$$\theta_{CASE-TO-HEAT-SINK} = 0.2^{\circ}C/W \text{ for K package with thermal compound.}$$

4

Power dissipation under these conditions is equal to:

$$P_D = (V_{IN} - V_{OUT}) (I_{OUT}) = 24W$$

Junction temperature will be equal to:

$$T_j = T_{AMBIENT} + P_D (\theta_{HEAT-SINK} + \theta_{CASE-TO-HEAT-SINK} + \theta_{jc})$$

For the Control Section:

$$T_j = 75^{\circ}C + 24W (1^{\circ}C/W + 0.2^{\circ}C/W + 0.6^{\circ}C/W) = 118^{\circ}C$$

$$118^{\circ}C < 125^{\circ}C = T_{jmax} \text{ (Control Section Commercial Range)}$$

For the Power Transistor:

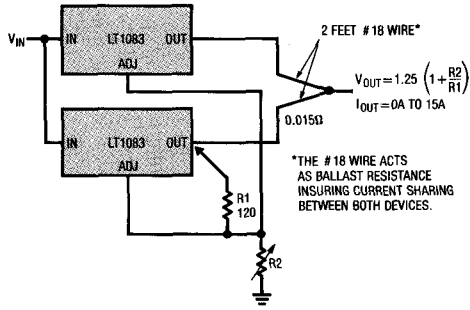
$$T_j = 75^{\circ}C + 24W (1^{\circ}C/W + 0.2^{\circ}C/W + 1.6^{\circ}C/W) = 142^{\circ}C$$

$$142^{\circ}C < 150^{\circ}C = T_{jmax} \text{ (Power Transistor Commercial Range)}$$

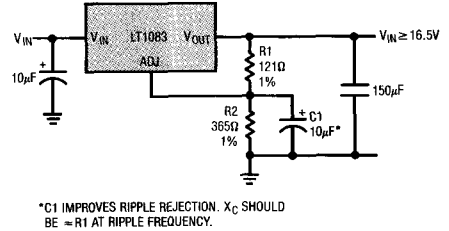
In both cases the junction temperature is below the maximum rating for the respective sections, ensuring reliable operation.

TYPICAL APPLICATIONS

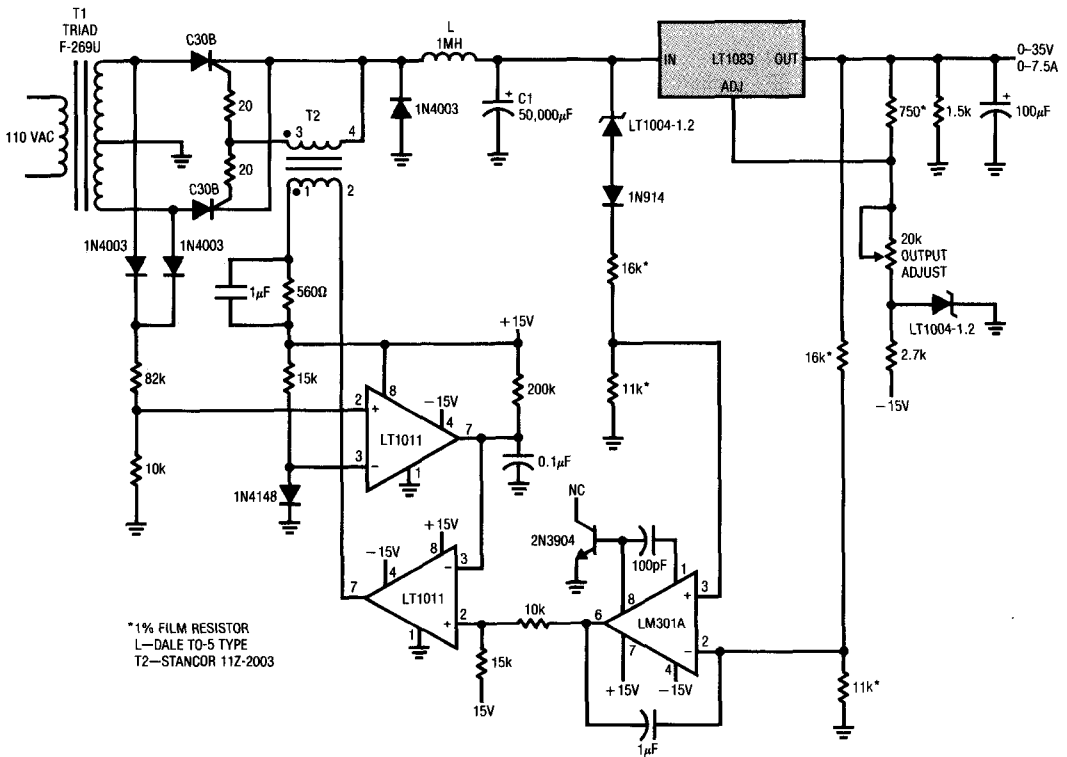
Paralleling Regulators



Improving Ripple Rejection



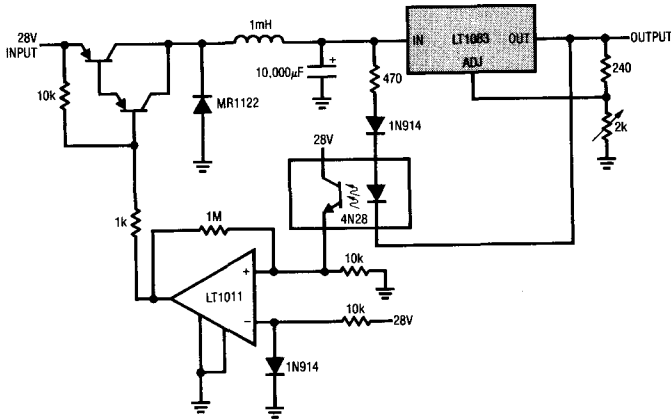
7.5A Variable Regulator



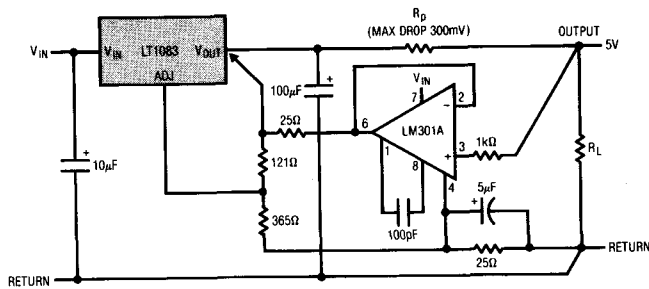
GENERAL PURPOSE REGULATOR WITH SCR PREREGULATOR TO LOWER POWER DISSIPATION. ABOUT 1.7V DIFFERENTIAL IS MAINTAINED ACROSS THE LT1083 INDEPENDENT OF OUTPUT VOLTAGE AND LOAD CURRENT.

TYPICAL APPLICATIONS

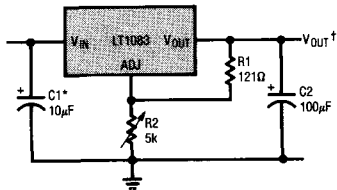
High Efficiency Regulator



Remote Sensing



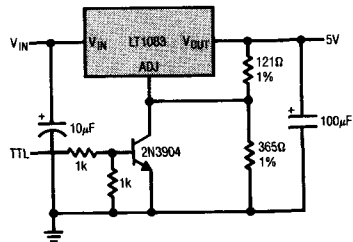
1.2V-15V Adjustable Regulator



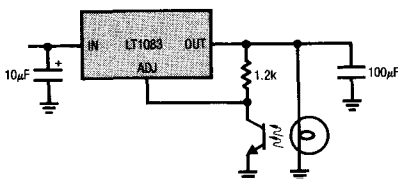
*NEEDED IF DEVICE IS FAR FROM FILTER CAPACITORS

$$V_{OUT} = 1.25V \left(1 + \frac{R_2}{R_1} \right)$$

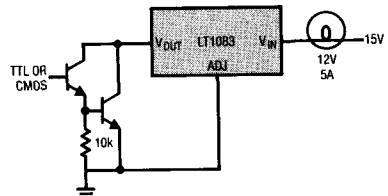
5V Regulator with Shutdown



Automatic Light Control

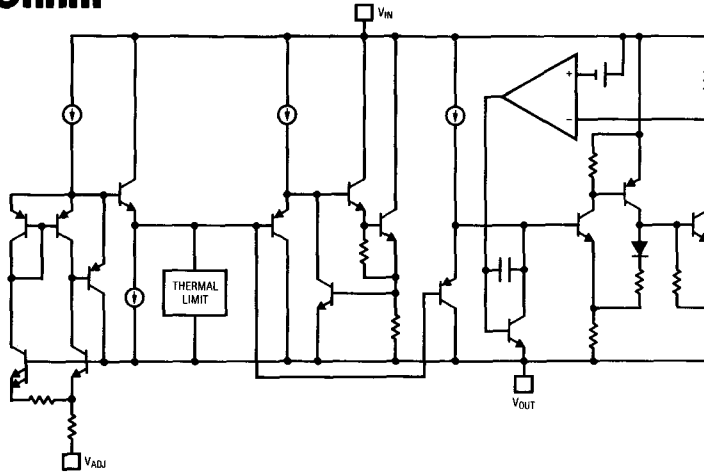


Protected High Current Lamp Driver



LT1083/LT1084/LT1085

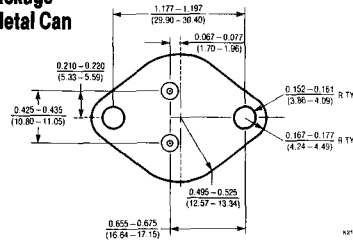
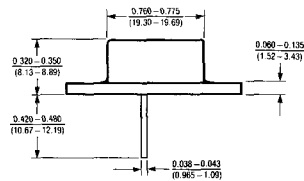
BLOCK DIAGRAM



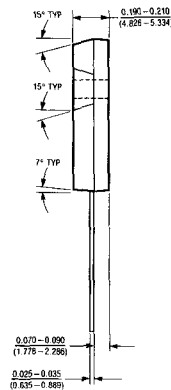
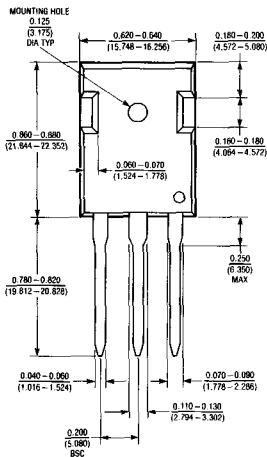
PACKAGE DESCRIPTIONS

Dimensions in inches (millimeters) unless otherwise noted.

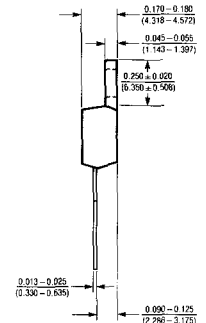
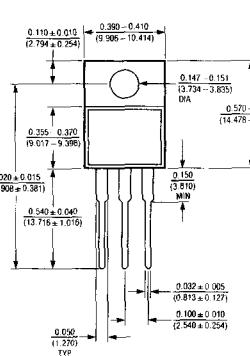
K Package TO-3 Metal Can



P Package TO-3P Plastic



T Package TO-220 Plastic



3A, 5A, 7.5A Low Dropout Positive Fixed Regulators

FEATURES

- Three Terminal Fixed 5V and 12V
- Output Current of 3A, 5A or 7.5A
- Operates Down to 1V Dropout
- Guaranteed Dropout Voltage at Multiple Current Levels
- 0.015% Line Regulation
- 0.1% Load Regulation
- 100% Thermal Limit Burn-In
- Adjustable Versions Available

APPLICATIONS

- High Efficiency Linear Regulators
- Post Regulators for Switching Supplies
- Constant Current Regulators
- Battery Chargers

DEVICE	OUTPUT CURRENT*
LT1083	7.5 Amps
LT1084	5.0 Amps
LT1085	3.0 Amps

*For a 1.5A low dropout regulator see the LT1083 data sheet.

DESCRIPTION

The LT1083 series of positive fixed regulators are designed to provide 3A, 5A and 7.5A with higher efficiency than currently available devices. All internal circuitry is designed to operate down to 1V input to output differential and the dropout voltage is fully specified as a function of load current. Dropout is guaranteed at a maximum of 1.5V at maximum output current, decreasing at lower load currents. On-chip trimming adjusts the output voltage to 1%. Current limit is also trimmed, minimizing the stress on both the regulator and power source circuitry under overload conditions.

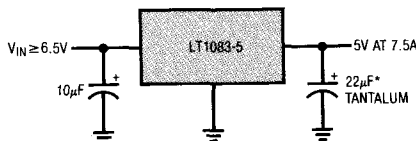
The LT1083 series devices are pin compatible with older 3 terminal regulators. A 10 μ F output capacitor is required on all new devices; however, this is usually included in most regulator packages.

Unlike LDO regulators, where up to 10% of the output current is wasted as quiescent current, the LT1083 quiescent current flows into the load, increasing efficiency.

REFER TO TABLE OF CONTENTS FOR REVISED DATA LOCATION

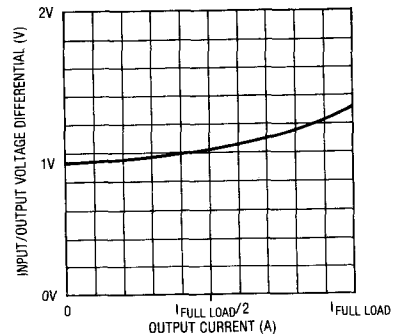
4

3A, 5A, 7.5A Regulator



*REQUIRED FOR STABILITY

Dropout Voltage vs Output Current

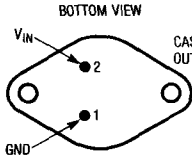
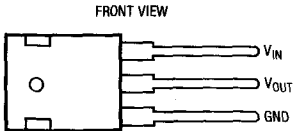
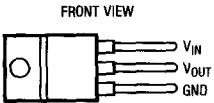


ABSOLUTE MAXIMUM RATINGS

Power Dissipation Internally Limited
 Input Voltage (Note 1) 30V
 Operating Input Voltage
 5V Devices 20V
 12V Devices 25V
 Operating Junction Temperature Range
 "M" Grades
 Control Section -55°C to 150°C
 Power Transistor -55°C to 200°C
 "C" Grades
 Control Section 0°C to 125°C
 Power Transistor 0°C to 150°C
 Storage Temperature -65°C to 150°C
 Lead Temperature (Soldering, 10 sec) 300°C

Note 1: Although the devices maximum operating voltage is limited, (20V for a 5V device, and 25V for a 12V device) the devices are guaranteed to withstand transient input voltages up to 30V. For input voltages greater than the maximum operating input voltage some degradation of specifications will occur. For input/output voltage differentials greater than 15V, a minimum external load of 5mA is required to maintain regulation.

PACKAGE/ORDER INFORMATION

	ORDER PART NUMBER		
 <p>BOTTOM VIEW VIN → 2 CASE IS OUTPUT GND → 1 K PACKAGE 2-LEAD TO-3 METAL CAN</p>	LT1083MK-5 LT1083MK-12 LT1083CK-5 LT1083CK-12 LT1084MK-5 LT1084MK-12 LT1084CK-5 LT1084CK-12 LT1085MK-5 LT1085MK-12 LT1085CK-5 LT1085CK-12		
	 <p>FRONT VIEW VIN VOUT GND P PACKAGE 3-LEAD TO-3 PLASTIC</p>	LT1083CP-5 LT1083CP-12 LT1084CP-5 LT1084CP-12	
		 <p>FRONT VIEW VIN VOUT GND T PACKAGE 3-LEAD TO-220 PLASTIC</p>	LT1084CT-5 LT1084CT-12 LT1085CT-5 LT1085CT-12

PRECONDITIONING

100% Thermal Limit Burn-In

ELECTRICAL CHARACTERISTICS

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS		
Output Voltage LT1083/4/5-5	$I_{OUT} = 0mA, T_J = 25°C, V_{IN} = 8V$ (K Package Only)	●	4.950	5.000	5.050	V	
			$0 \leq I_{OUT} \leq I_{FULL\ LOAD}, 6.5V \leq V_{IN} \leq 20V$ (Notes 3, 5)	4.900	5.000	5.100	V
	LT1083/4/5-12	$I_{OUT} = 0mA, T_J = 25°C, V_{IN} = 15V$ (K Package Only)	●	11.880	12.000	12.120	V
				$0 \leq I_{OUT} \leq I_{FULL\ LOAD}, 13.5V \leq V_{IN} \leq 25V$ (Notes 3, 5)	11.760	12.000	12.240
Line Regulation LT1083/4/5-5	$I_{OUT} = 0mA, T_J = 25°C, 6.5V \leq V_{IN} \leq 20V$ (Notes 1, 2)	●		0.5	10	mV	
				1.0	10	mV	
	LT1083/4/5-12	$I_{OUT} = 0mA, T_J = 25°C, 13.5V \leq V_{IN} \leq 25V$ (Notes 1, 2)	●		1.0	25	mV
					2.0	25	mV

ELECTRICAL CHARACTERISTICS

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Load Regulation LT1083/4/5-5	$V_{IN} = 8V, 0 \leq I_{OUT} \leq I_{FULL\ LOAD}$ $T_j = 25^\circ C$ (Notes 1, 2, 3, 5)	●	5	20	mV
			10	35	mV
LT1083/4/5-12	$V_{IN} = 15V, 0 \leq I_{OUT} \leq I_{FULL\ LOAD}$ $T_j = 25^\circ C$ (Notes 1, 2, 3, 5)	●	12	36	mV
			24	72	mV
Dropout Voltage ($V_{IN} - V_{OUT}$) LT1083/4/5-5	$\Delta V_{OUT} = 50mV, I_{OUT} = I_{FULL\ LOAD}$ (Notes 4, 5)	●	1.3	1.5	V
			1.3	1.5	V
LT1083/4/5-12	$\Delta V_{OUT} = 120mV, I_{OUT} = I_{FULL\ LOAD}$ (Notes 4, 5)	●	1.3	1.5	V
			1.3	1.5	V
Current Limit LT1083-5 LT1083-12 LT1084-5 LT1084-12 LT1085-5 LT1085-12	$V_{IN} = 10V$ $V_{IN} = 17V$ $V_{IN} = 10V$ $V_{IN} = 17V$ $V_{IN} = 10V$ $V_{IN} = 17V$	●	8.0	9.5	A
			8.0	9.5	A
			5.5	6.5	A
			5.5	6.5	A
			3.2	4.0	A
			3.2	4.0	A
Quiescent Current LT1083/4/5-5 LT1083/4/5-12	$V_{IN} \leq 20V$ $V_{IN} \leq 25V$	●	5.0	10.0	mA
			5.0	10.0	mA
Thermal Regulation LT1083-5/12 LT1084-5/12 LT1085-5/12	$T_A = 25^\circ C, 30ms$ pulse	●	0.002	0.01	%/W
			0.003	0.015	%/W
			0.004	0.02	%/W
Ripple Rejection LT1083/4/5-5 LT1083/4/5-12	$f = 120Hz, C_{OUT} = 25\mu F$ Tantalum $I_{OUT} = I_{FULL\ LOAD}$ $V_{IN} = 8V$ (Note 5) $V_{IN} = 15V$ (Note 5)	●	60	68	dB
			54	60	dB
			54	60	dB
Temperature Stability		●	0.5		%
Long Term Stability	$T_A = 125^\circ C, 1000$ Hrs.		0.03	1.0	%
RMS Output Noise (% of V_{OUT})	$T_A = 25^\circ C$ $10Hz = \leq f \leq 10kHz$		0.003		%
Thermal Resistance Junction to Case LT1083 LT1084 LT1085	K Package: Control Circuitry/Power Transistor P Package: Control Circuitry/Power Transistor K Package: Control Circuitry/Power Transistor P Package: Control Circuitry/Power Transistor T Package: Control Circuitry/Power Transistor K Package: Control Circuitry/Power Transistor T Package: Control Circuitry/Power Transistor	●		0.6/1.6	$^\circ C/W$
				0.5/1.6	$^\circ C/W$
				0.75/2.3	$^\circ C/W$
				0.65/2.3	$^\circ C/W$
				0.65/2.7	$^\circ C/W$
				0.9/3.0	$^\circ C/W$
	0.7/3.0	$^\circ C/W$			

4

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: See thermal regulation specifications for changes in output voltage due to heating effects. Load and line regulation are measured at a constant junction temperature by low duty cycle pulse testing.

Note 2: Line and load regulation are guaranteed up to the maximum power dissipation (60W for the LT1083, 45W for the LT1084 (K, P), 30W for the LT1084 (T) and 30W for the LT1085). Power dissipation is determined by the input/output differential and the output current. Guaranteed maximum power dissipation will not be available over the full input/output voltage range.

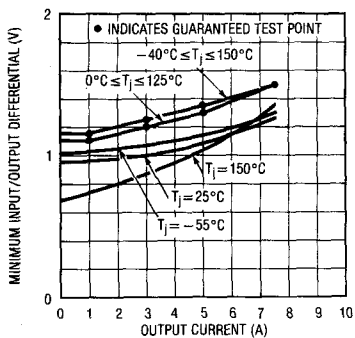
Note 3: $I_{FULL\ LOAD}$ is defined in the current limit curves. The $I_{FULL\ LOAD}$ curve is defined as the minimum value of current limit as a function of input to output voltage. Note that the 60W power dissipation for the LT1083 (45W for the LT1084 (K, P), 30W for the LT1084 (T), 30W for the LT1085) is only achievable over a limited range of input to output voltage.

Note 4: Dropout voltage is specified over the full output current range of the device. Test points and limits are shown on the Dropout Voltage curve.

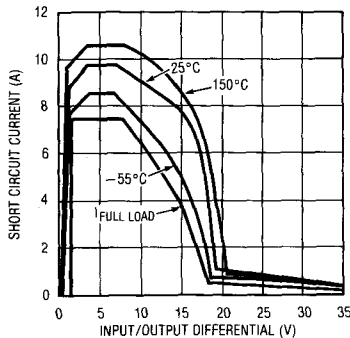
Note 5: For LT1083 $I_{FULL\ LOAD}$ is 5A for $-55^\circ C \leq T_j < -40^\circ C$ and 7.5A for $T_j \geq -40^\circ C$.

TYPICAL PERFORMANCE CHARACTERISTICS

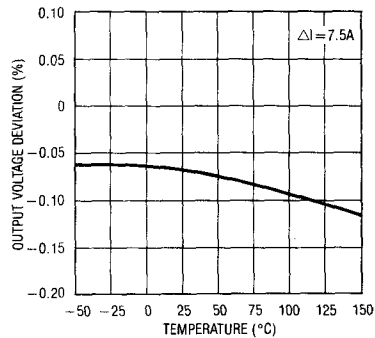
LT1083 Dropout Voltage



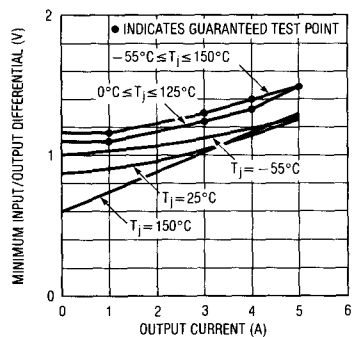
LT1083 Short Circuit Current



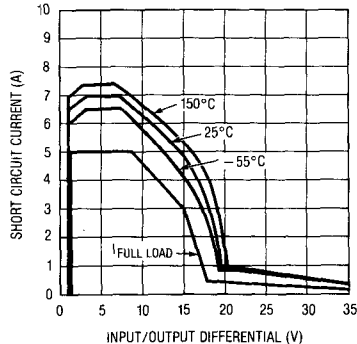
LT1083 Load Regulation



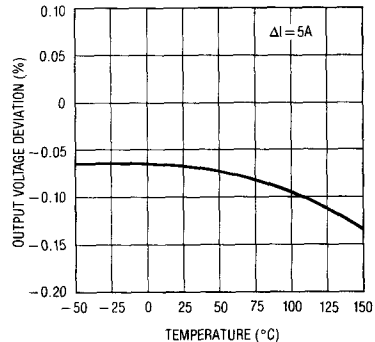
LT1084 Dropout Voltage



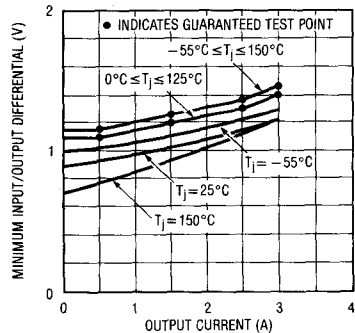
LT1084 Short Circuit Current



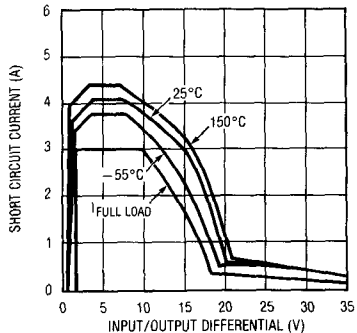
LT1084 Load Regulation



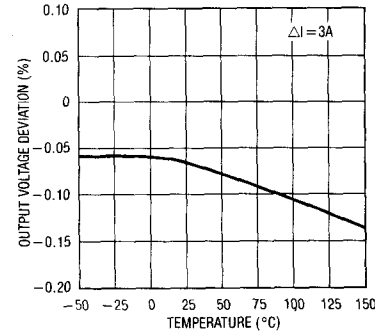
LT1085 Dropout Voltage



LT1085 Short Circuit Current

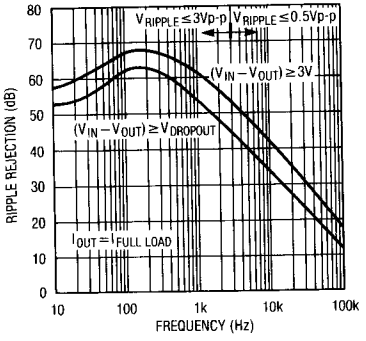


LT1085 Load Regulation

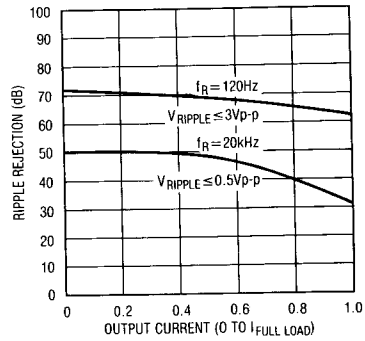


TYPICAL PERFORMANCE CHARACTERISTICS

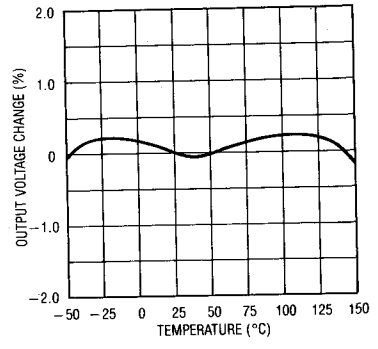
LT1083/4/5-5 Ripple Rejection



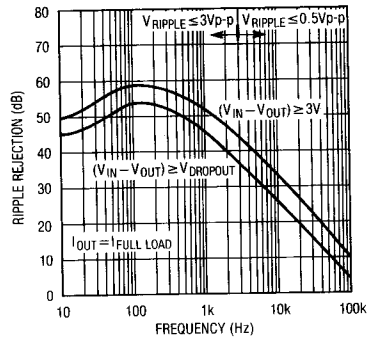
LT1083/4/5-5 Ripple Rejection vs Current



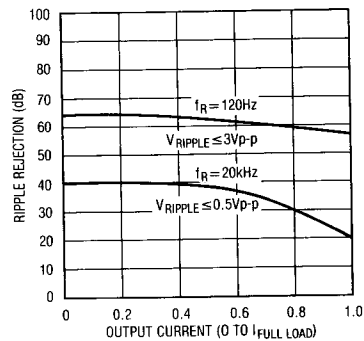
Temperature Stability



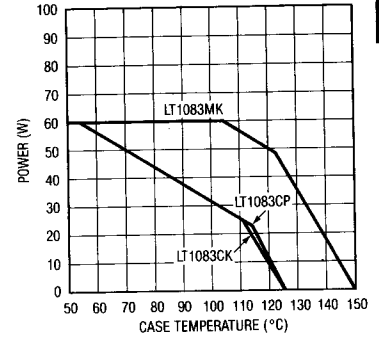
LT1083/4/5-12 Ripple Rejection



LT1083/4/5-12 Ripple Rejection vs Current



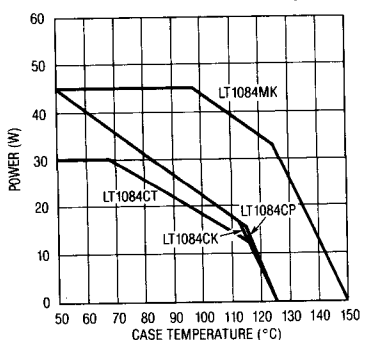
LT1083 Maximum Power Dissipation*



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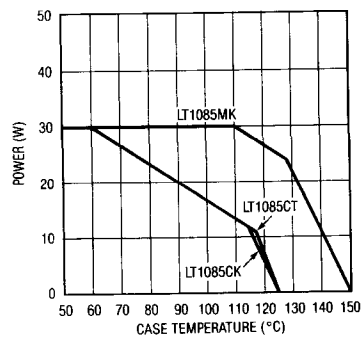
* AS LIMITED BY MAXIMUM JUNCTION TEMPERATURE

LT1084 Maximum Power Dissipation*



* AS LIMITED BY MAXIMUM JUNCTION TEMPERATURE

LT1085 Maximum Power Dissipation*



* AS LIMITED BY MAXIMUM JUNCTION TEMPERATURE

APPLICATION HINTS

The LT1083 family of three terminal regulators is easy to use and has all the protection features that are expected in high performance voltage regulators. They are short circuit protected, have safe area protection as well as thermal shutdown to turn off the regulator should the temperature exceed about 165°C.

These regulators offer lower dropout voltage and more precise reference tolerance. Further, the reference stability with temperature is improved over older types of regulators. The only circuit difference between using the LT1083 family and older regulators is that they require an output capacitor for stability.

Stability

The circuit design used in the LT1083 family requires the use of an output capacitor as part of the device frequency compensation. For all operating conditions, the addition of 150 μ F aluminum electrolytic or a 22 μ F solid tantalum on the output will ensure stability. Normally, capacitors much smaller than this can be used with the LT1083. Many different types of capacitors with widely varying characteristics are available. These capacitors differ in capacitor tolerance (sometimes ranging up to $\pm 100\%$), equivalent series resistance, and capacitance temperature coefficient. The 150 μ F or 22 μ F values given will ensure stability.

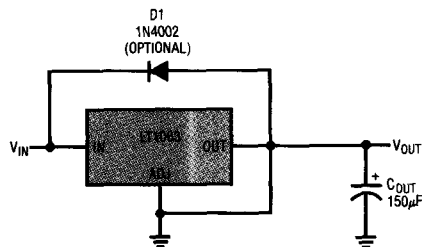
Normally, capacitor values on the order of 100 μ F are used in the output of many regulators to ensure good transient response with heavy load current changes. Output capacitance can be increased without limit and larger values of output capacitor further improve stability and transient response of the LT1083 regulators.

Another possible stability problem that can occur in monolithic IC regulators is current limit oscillations. These can occur because, in current limit, the safe area protection exhibits a negative impedance. The safe area protection decreases the current limit as the input-to-output voltage increases. That is the equivalent of having a negative resistance since increasing voltage causes current to decrease. Negative resistance during current limit is not unique to the LT1083 series and has been present on all power IC regulators. The value of the negative resistance is a function of how fast the current limit is

folded back as input-to-output voltage increases. This negative resistance can react with capacitors or inductors on the input to cause oscillation during current limiting. Depending on the value of series resistance, the overall circuitry may end up unstable. Since this is a system problem, it is not necessarily easy to solve; however it does not cause any problems with the IC regulator and can usually be ignored.

Protection Diodes

In normal operation, the LT1083 family does not need any protection diodes. The internal diode between the input and the output pins of the LT1083 family can handle microsecond surge currents of 50A to 100A. Even with large output capacitances, it is very difficult to get those values of surge currents in normal operation. Only with high value output capacitors, such as 1000 μ F to 5000 μ F and with the input pin instantaneously shorted to ground, can damage occur. A crowbar circuit at the input of the LT1083 can generate those kinds of currents, and a diode from output to input is then recommended. Normal power supply cycling or even plugging and unplugging in the system will not generate currents large enough to do any damage.



Overload Recovery

Like any of the IC power regulators, the LT1083 has safe area protection. The safe area protection decreases the current limit as input-to-output voltage increases and keeps the power transistor inside a safe operating region for all values of input-to-output voltage. The LT1083 protection is designed to provide some output current at all values of input-to-output voltage up to the device breakdown.

APPLICATION HINTS

When power is first turned on, as the input voltage rises, the output follows the input, allowing the regulator to start up into very heavy loads. During the start-up, as the input voltage is rising, the input-to-output voltage differential remains small, allowing the regulator to supply large output currents. With high input voltage, a problem can occur wherein removal of an output short will not allow the output voltage to recover. Older regulators, such as the 7800 series, also exhibited this phenomenon, so it is not unique to the LT1083.

The problem occurs with a heavy output load when the input voltage is high and the output voltage is low, such as immediately after a removal of a short. The load line for such a load may intersect the output current curve at two points. If this happens, there are two stable output operating points for the regulator. With this double intersection, the power supply may need to be cycled down to zero and brought up again to make the output recover.

Ripple Rejection

In applications that require improved ripple rejection, the LT1083 series adjustable regulators should be used. With LT1083 series adjustable regulators, the addition of a bypass capacitor from the adjust pin to ground will reduce output ripple by the ratio of $V_{OUT}/1.25V$. See LT1083 series adjustable regulator data sheet.

Load Regulation

Because the LT1083 is a three-terminal device, it is not possible to provide true remote load sensing. Load regulation will be limited by the resistance of the wire connecting the regulator to the load. The data sheet specification for load regulation is measured at the bottom of the package. Negative side sensing is a true Kelvin connection, with the ground pin of the device returned to the negative side of the load.

Thermal Considerations

The LT1083 series of regulators have internal power and thermal limiting circuitry designed to protect the device under overload conditions. For continuous normal load conditions however, maximum junction temperature ratings must not be exceeded. It is important to give careful consideration to all sources of thermal resistance from junction to ambient. This includes junction to case, case to heat sink interface, and heat sink resistance itself. New thermal resistance specifications have been developed to more accurately reflect device temperature and ensure safe operating temperatures. The data section for these new regulators provides a separate thermal resistance and maximum junction temperature for both the *Control Section* and the *Power Transistor*. Previous regulators, with a single junction to case thermal resistance specification, used an average of the two values provided here and therefore could allow excessive junction temperatures under certain conditions of ambient temperature and heat sink resistance. To avoid this possibility, calculations should be made for both sections to ensure that both thermal limits are met.

Junction-to-case thermal resistance is specified from the IC junction to the bottom of the case directly below the die. This is the lowest resistance path for heat flow. Proper mounting is required to ensure the best possible thermal flow from this area of the package to the heat sink. Thermal compound at the case-to-heat-sink interface is strongly recommended. If the case of the device must be electrically isolated, a thermally conductive spacer can be used, as long as its added contribution to thermal resistance is considered. Note that the case of all devices in this series is electrically connected to the output.

APPLICATION HINTS

For example, using a LT1083-5CK (TO-3, Commercial) and assuming:

V_{IN} (max continuous) = 9V, V_{OUT} = 5V, I_{OUT} = 6A,
 $T_{AMBIENT}$ = 75°C, $\theta_{HEAT\ SINK}$ = 1°C/W,
 $\theta_{CASE\ TO\ HEAT\ SINK}$ = 0.2°C/W for K package with thermal compound.

Power dissipation under these conditions is equal to:

$$P_D = (V_{IN} - V_{OUT}) (I_{OUT}) = 24W$$

Junction temperature will be equal to:

$$T_j = T_{AMBIENT} + P_D (\theta_{HEAT\ SINK} + \theta_{CASE\ TO\ HEAT\ SINK} + \theta_{jc})$$

For the Control Section:

$$T_j = 75^\circ C + 24W (1^\circ C/W + 0.2^\circ C/W + 0.6^\circ C/W) = 118^\circ C$$

$$118^\circ C < 125^\circ C = T_{jmax} \text{ (Control Section Commercial Range)}$$

For the Power Transistor:

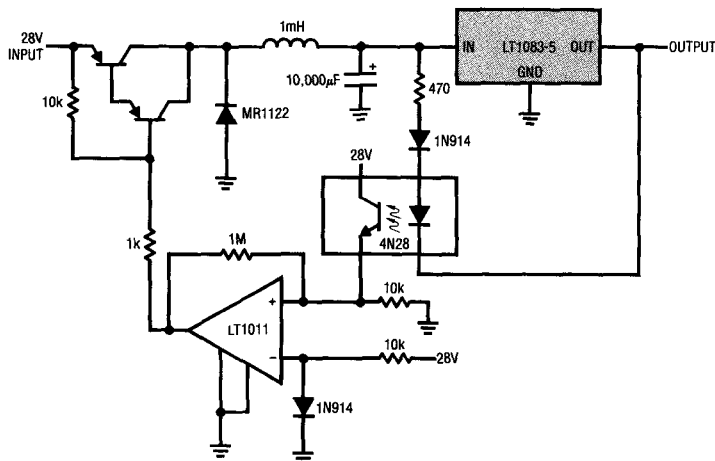
$$T_j = 75^\circ C + 24W (1^\circ C/W + 0.2^\circ C/W + 1.6^\circ C/W) = 142^\circ C$$

$$142^\circ C < 150^\circ C = T_{jmax} \text{ (Power Transistor Commercial Range)}$$

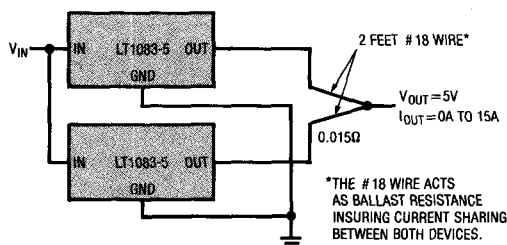
In both cases the junction temperature is below the maximum rating for the respective sections, ensuring reliable operation.

TYPICAL APPLICATIONS

High Efficiency Regulator

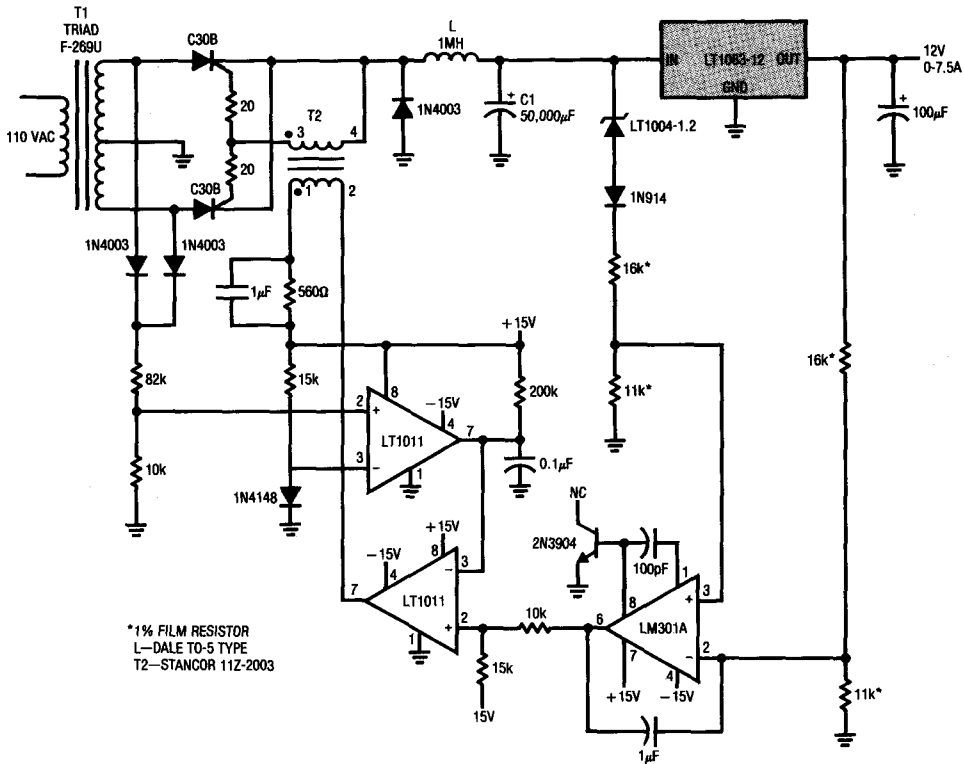


Paralleling Regulators



TYPICAL APPLICATIONS

7.5A Regulator

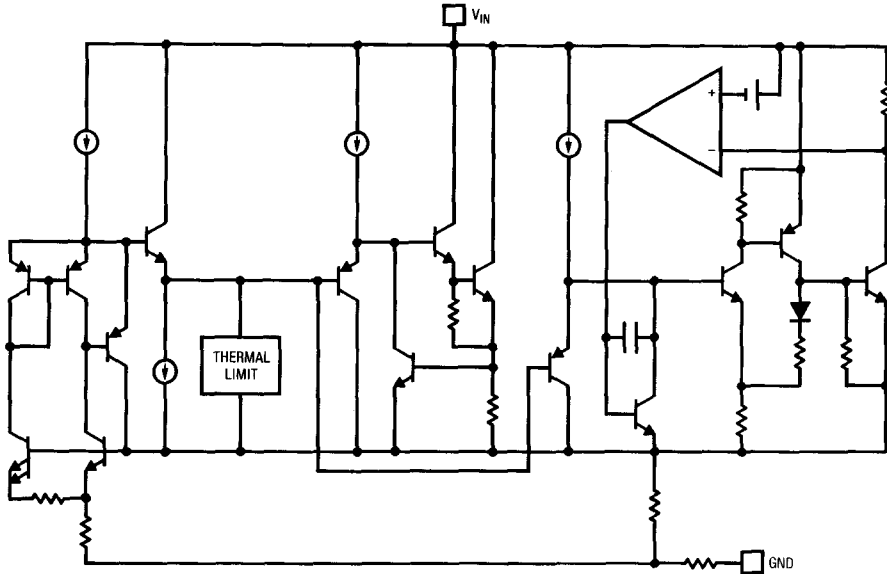


*1% FILM RESISTOR
 L—DALE TO-5 TYPE
 T2—STANCOR 11Z-2003

REGULATOR WITH SCR PREREGULATOR TO LOWER POWER DISSIPATION. ABOUT 1.7V DIFFERENTIAL IS MAINTAINED ACROSS THE LT1083 INDEPENDENT OF LOAD CURRENT.

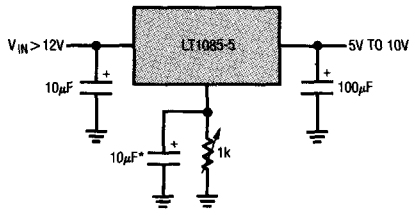
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BLOCK DIAGRAM



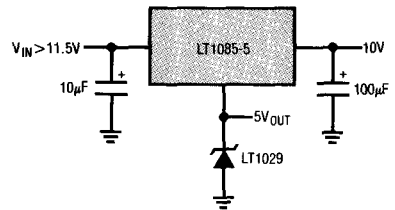
TYPICAL APPLICATIONS

Adjusting Output Voltage



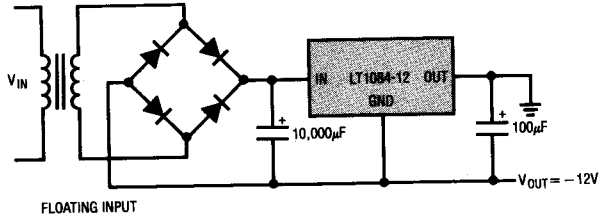
*OPTIONAL IMPROVES RIPPLE REJECTION

Regulator with Reference

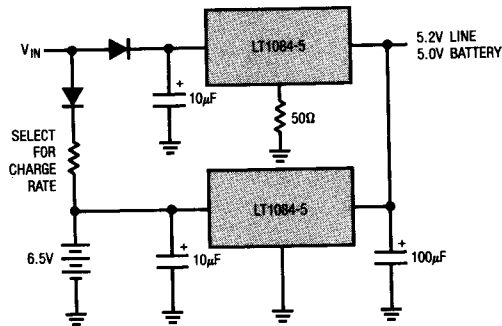


TYPICAL APPLICATIONS

Low Dropout Negative Supply

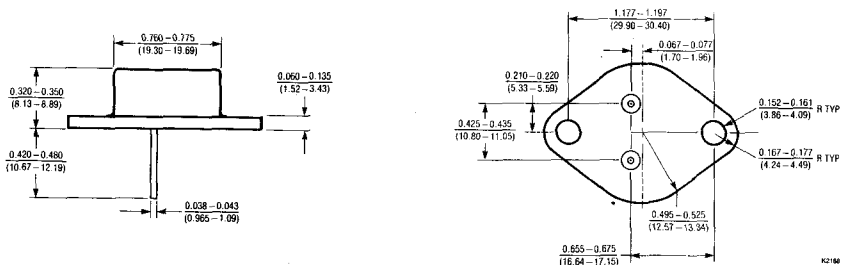


Battery Backed Up Regulated Supply

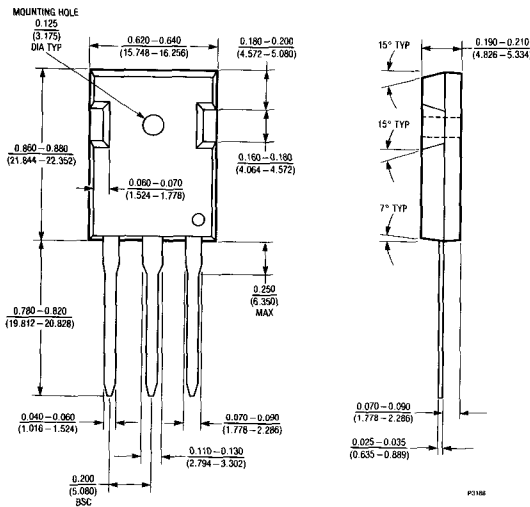


PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

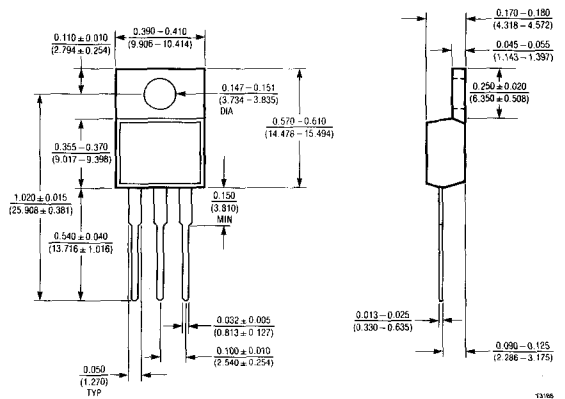
**K Package
 TO-3 Metal Can**



**P Package
 TO-3P Plastic**



**T Package
 TO-220 Plastic**



1.5A Low Dropout Positive Regulators Adjustable and Fixed 5V, 12V

FEATURES

- Three Terminal Adjustable or Fixed 5V, 12V
- Output Current of 1.5A, (0.5A for LT1086H)
- Operates Down to 1V Dropout
- Guaranteed Dropout Voltage at Multiple Current Levels
- 0.015% Line Regulation
- 0.1% Load Regulation
- 100% Thermal Limit Burn-In

APPLICATIONS

- High Efficiency Linear Regulators
- Post Regulators for Switching Supplies
- Constant Current Regulators
- Battery Chargers

DESCRIPTION

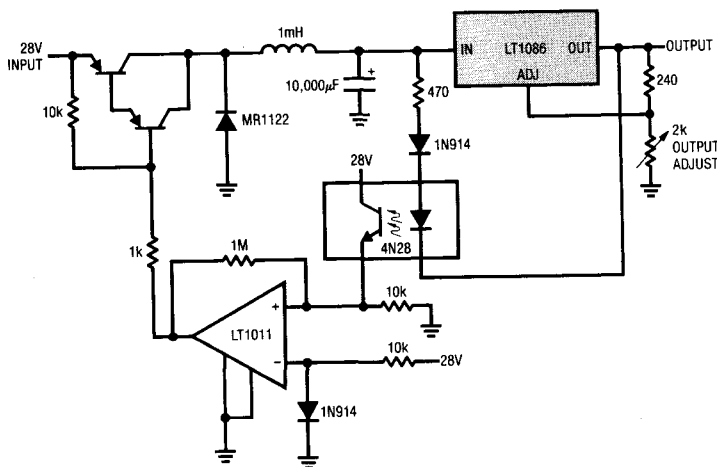
The LT1086 is designed to provide 1.5A with higher efficiency than currently available devices. All internal circuitry is designed to operate down to 1V input to output differential and the dropout voltage is fully specified as a function of load current. Dropout is guaranteed at a maximum of 1.5V at maximum output current, decreasing at lower load currents. On-chip trimming adjusts the reference/output voltage to 1%. Current limit is also trimmed, minimizing the stress on both the regulator and power source circuitry under overload conditions.

The LT1086 is not compatible with older 3 terminal adjustable regulators. A 10 μ F output capacitor is required on the new devices; however, this is usually included in most regulator designs.

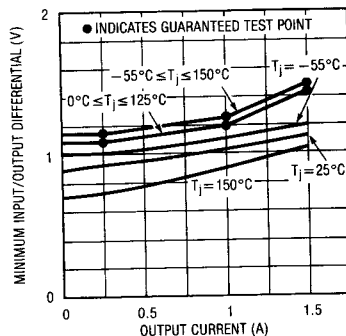
Unlike PNP regulators, where up to 10% of the output current is wasted as quiescent current, the LT1086 quiescent current flows into the load, increasing efficiency.

REFER TO TABLE OF CONTENTS
FOR REVISED DATA LOCATION

High Efficiency Regulator



LT1086 Dropout Voltage



ABSOLUTE MAXIMUM RATINGS

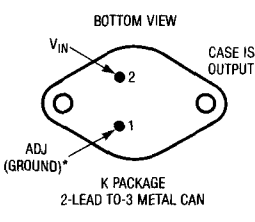
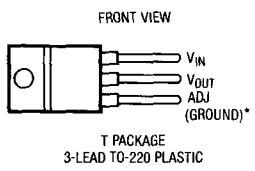
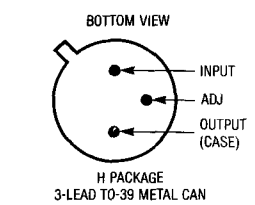
Power Dissipation	Internally Limited
Input Voltage*	30V
Operating Input Voltage	
Adj. Devices	25V
-5V Devices	20V
-12V Devices	25V
Operating Junction Temperature Range	
“M” Grades	
Control Section	-55°C to 150°C
Power Transistor	-55°C to 200°C
“C” Grades	
Control Section	0°C to 125°C
Power Transistor	0°C to 150°C
Storage Temperature	-65°C to 150°C
Lead Temperature (Soldering, 10 sec)	300°C

*Although the devices maximum operating voltage is limited, (20V for a -5V device, and 25V for adjustable and -12 devices) the devices are guaranteed to withstand transient input voltages up to 30V. For input voltages greater than the maximum operating input voltage some degradation of specifications will occur. For -5 and -12 devices operating at input/output voltage differentials greater than 15V, a minimum external load of 5mA is required to maintain regulation.

PRECONDITIONING

100% Thermal Limit Burn-In

PACKAGE/ORDER INFORMATION

 <p>BOTTOM VIEW VIN ADJ (GROUND)* CASE IS OUTPUT K PACKAGE 2-LEAD TO-3 METAL CAN</p>	ORDER PART NUMBER	
	LT1086MK	LT1086CK
 <p>FRONT VIEW VIN VOUT ADJ (GROUND)* T PACKAGE 3-LEAD TO-220 PLASTIC</p>	LT1086CT	
	LT1086-5CT	LT1086-12CT
 <p>BOTTOM VIEW INPUT ADJ OUTPUT (CASE) H PACKAGE 3-LEAD TO-39 METAL CAN</p>	LT1086CH	
	LT1086MH	

*FOR FIXED VERSIONS

ELECTRICAL CHARACTERISTICS (See Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Reference Voltage LT1086, LT1086H	$I_{OUT} = 10\text{mA}$, $T_J = 25^\circ\text{C}$, $(V_{IN} - V_{OUT}) = 3\text{V}$ (K Package Only) $10\text{mA} \leq I_{OUT} \leq 1.5\text{A}$, (0.5A for LT1086H) $1.5\text{V} \leq (V_{IN} - V_{OUT}) \leq 15\text{V}$	1.238	1.250	1.262	V
		1.225	1.250	1.270	V
Output Voltage LT1086-5	$I_{OUT} = 0\text{mA}$, $T_J = 25^\circ\text{C}$ $V_{IN} = 8\text{V}$ (K Package Only) $0 \leq I_{OUT} \leq 1.5\text{A}$, $6.5\text{V} \leq V_{IN} \leq 20\text{V}$	4.950	5.000	5.050	V
		4.900	5.000	5.100	V
LT1086-12	$I_{OUT} = 0\text{mA}$, $T_J = 25^\circ\text{C}$ $V_{IN} = 15\text{V}$ (K Package Only) $0\text{V} \leq I_{OUT} \leq 1.5\text{A}$, $13.5\text{V} \leq V_{IN} \leq 25\text{V}$	11.880	12.000	12.120	V
		11.760	12.000	12.240	V
Line Regulation LT1086, LT1086H	$I_{LOAD} = 10\text{mA}$, $1.5\text{V} \leq (V_{IN} - V_{OUT}) \leq 15\text{V}$, $T_J = 25^\circ\text{C}$	0.015	0.2	%	
		0.035	0.2	%	
	$I_{OUT} = 0\text{mA}$, $T_J = 25^\circ\text{C}$, $6.5\text{V} \leq V_{IN} \leq 20\text{V}$	0.5	10	mV	
		1.0	10	mV	
		1.0	25	mV	
2.0	25	mV			

ELECTRICAL CHARACTERISTICS (See Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	
Load Regulation LT1086, LT1086H	$(V_{IN} - V_{OUT}) = 3V$, $10mA \leq I_{OUT} \leq 1.5A$, (0.5A for LT1086H) $T_J = 25^\circ C$ (Notes 1, 2)	●	0.1	0.3	%	
			0.2	0.4	%	
			5	20	mV	
LT1086-5	$V_{IN} = 8V$, $0 \leq I_{OUT} \leq 1.5A$, $T_J = 25^\circ C$ (Notes 1, 2)	●	10	35	mV	
LT1086-12	$V_{IN} = 15V$, $0 \leq I_{OUT} \leq 1.5A$, $T_J = 25^\circ C$ (Notes 1, 2)	●	12	36	mV	
			24	72	mV	
Dropout Voltage ($V_{IN} - V_{OUT}$) LT1086 LT1086H LT1086-5 LT1086-12	$\Delta V_{REF} = 1\%$, $I_{OUT} = 1.5A$ (Note 3) $\Delta V_{REF} = 1\%$, $I_{OUT} = 0.5A$ (Note 3) $\Delta V_{OUT} = 50mV$, $I_{OUT} = 1.5A$ (Note 3) $\Delta V_{OUT} = 120mV$, $I_{OUT} = 1.5A$ (Note 3)	● ● ● ●	1.3	1.5	V	
			0.95	1.25	V	
			1.3	1.5	V	
			1.3	1.5	V	
Current Limit LT1086, LT1086-5, LT1086-12 LT1086H	$(V_{IN} - V_{OUT}) = 5V$ $(V_{IN} - V_{OUT}) = 25V$ $(V_{IN} - V_{OUT}) = 5V$ $(V_{IN} - V_{OUT}) = 2.5V$	● ● ● ●	1.5	1.6	2.5	A
			0.075	0.15		A
			0.5	0.7	1.2	A
			0.03	0.075		A
Minimum Load Current LT1086, LT1086H	$(V_{IN} - V_{OUT}) = 25V$ (Note 4)	●	5	10	mA	
Quiescent Current LT1086-5 LT1086-12	$V_{IN} \leq 20V$ $V_{IN} \leq 25V$	● ●	5	10	mA	
			5	10	mA	
Thermal Regulation	$T_A = 25^\circ C$, 30ms Pulse		0.008	0.04	%/W	
Ripple Rejection LT1086, LT1086H LT1086-5 LT1086-12	$f = 120Hz$, $C_{OUT} = 25\mu F$ Tantalum $I_{OUT} = 1.5A$, ($I_{OUT} = 0.5A$ for LT1086H) $C_{ADJ} = 25\mu F$, $(V_{IN} - V_{OUT}) = 3V$ $V_{IN} = 8V$ $V_{IN} = 15V$	● ● ● ●	60	75	dB	
			60	68	dB	
			54	60	dB	
Adjust Pin Current LT1086, LT1086H	$T_J = 25^\circ C$	●	55		μA	
				120	μA	
Adjust Pin Current Change LT1086, LT1086H	$10mA \leq I_{OUT} \leq 1.5A$, (0.5A for LT1086H) $1.5V \leq (V_{IN} - V_{OUT}) \leq 15V$	● ●	0.2	5	μA	
			0.5		%	
Temperature Stability			0.3	1	%	
Long Term Stability	$T_A = 125^\circ C$, 1000 Hrs.				%	
RMS Output Noise (% of V_{OUT})	$T_A = 25^\circ C$ $10Hz \leq f \leq 10kHz$		0.003		%	
Thermal Resistance Junction to Case	K Package: Control Circuitry/Power Transistor T Package: Control Circuitry/Power Transistor H Package: Control Circuitry/Power Transistor			1.7/4.0	$^\circ C/W$	
				1.5/4.0	$^\circ C/W$	
				15/20	$^\circ C/W$	

4

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: See thermal regulation specifications for changes in output voltage due to heating effects. Load and line regulation are measured at a constant junction temperature by low duty cycle pulse testing. Load regulation is measured at the output lead $\approx 1/8"$ from the package.

Note 2: Line and load regulation are guaranteed up to the maximum power dissipation of 15W for the LT1086, LT1086-5 and LT1086-12, and 3W for the LT1086H. Power dissipation is determined by the input/output differential

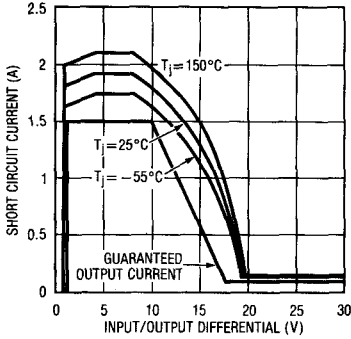
and the output current. Guaranteed maximum power dissipation will not be available over the full input/output voltage range. See Short Circuit Current Curve for available output current.

Note 3: Dropout voltage is specified over the full output current range of the device. Test points and limits are shown on the Dropout Voltage curve.

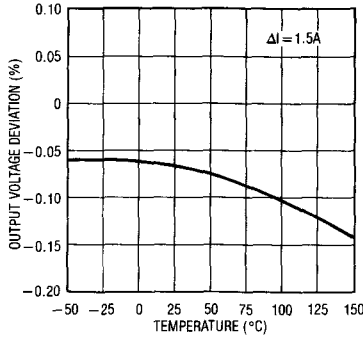
Note 4: Minimum load current is defined as the minimum output current required to maintain regulation. At 25V input/output differential the device is guaranteed to regulate if the output current is greater than 10mA.

TYPICAL PERFORMANCE CHARACTERISTICS

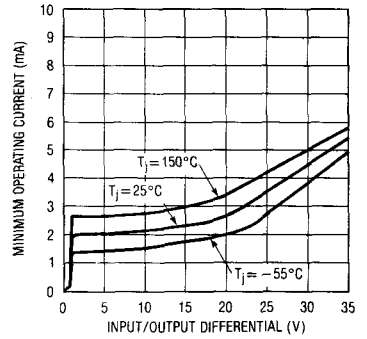
LT1086 Short Circuit Current



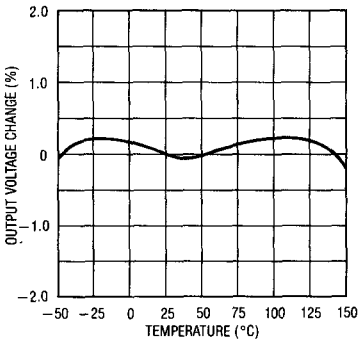
LT1086 Load Regulation



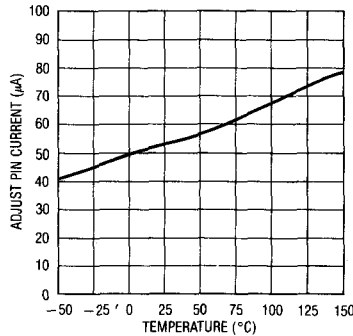
Minimum Operating Current (Adjustable Device)



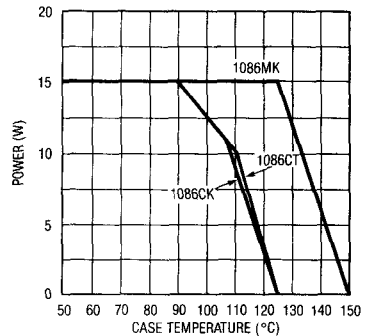
Temperature Stability



Adjust Pin Current

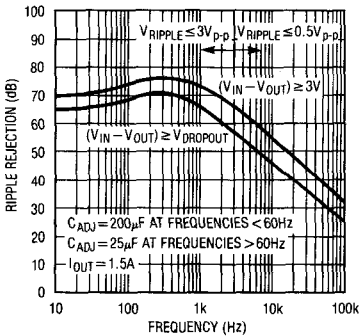


LT1086 Maximum Power Dissipation*

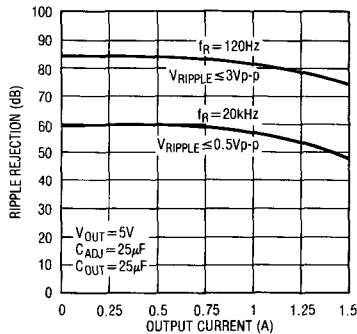


*AS LIMITED BY MAXIMUM JUNCTION TEMPERATURE

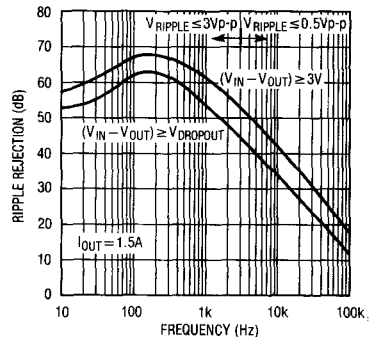
LT1086 Ripple Rejection



LT1086 Ripple Rejection vs Current

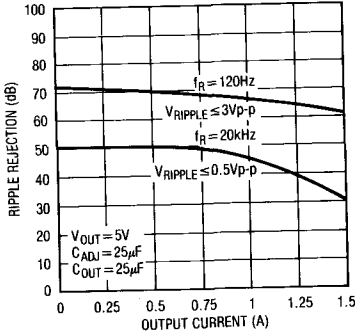


LT1086-5 Ripple Rejection

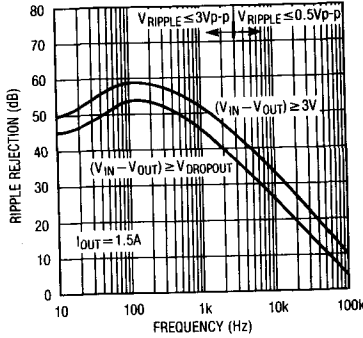


TYPICAL PERFORMANCE CHARACTERISTICS

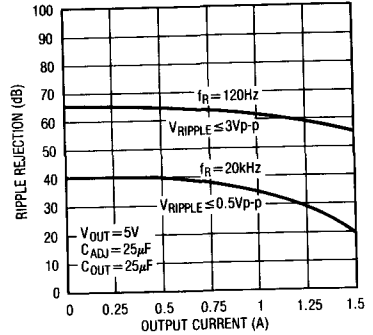
LT1086-5 Ripple Rejection vs Current



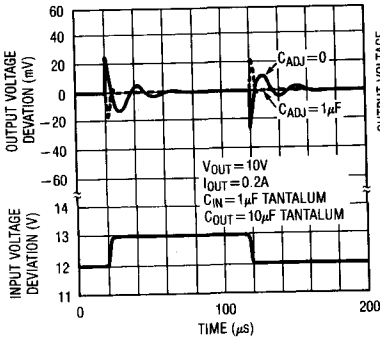
LT1086-12 Ripple Rejection



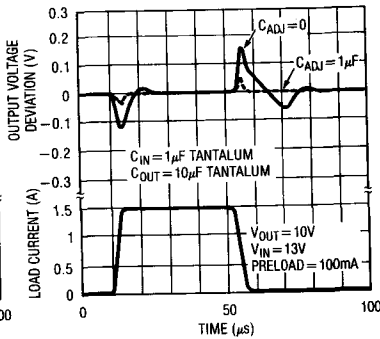
LT1086-12 Ripple Rejection vs Current



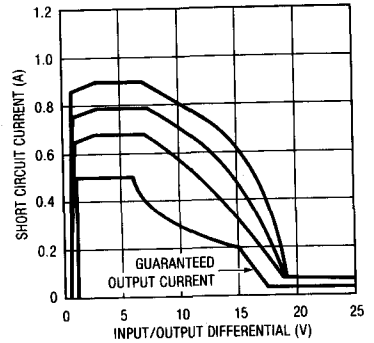
LT1086 Line Transient Response



LT1086 Load Transient Response

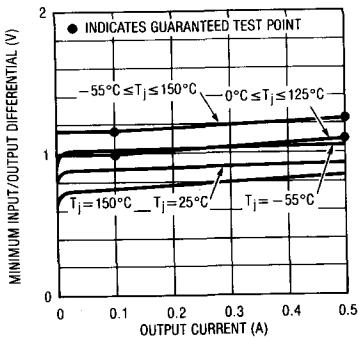


LT1086H Short Circuit Current

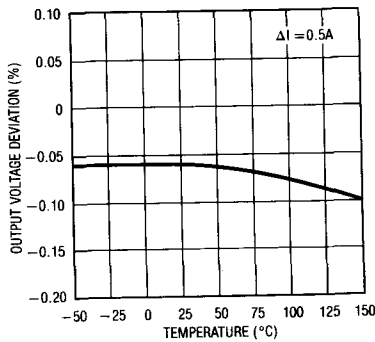


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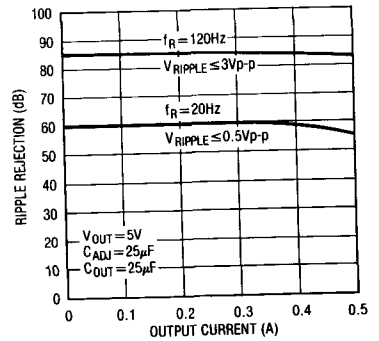
LT1086H Dropout Voltage



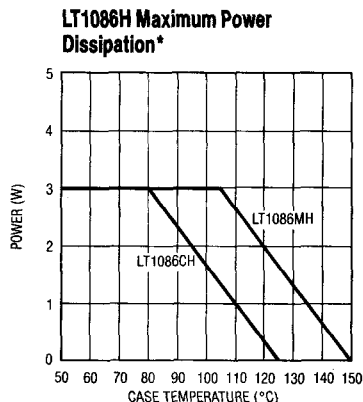
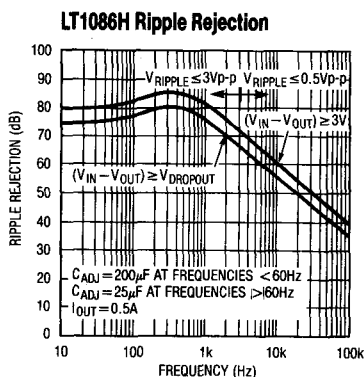
LT1086H Load Regulation



LT1086H Ripple Rejection vs Current



TYPICAL PERFORMANCE CHARACTERISTICS



*AS LIMITED BY MAXIMUM JUNCTION TEMPERATURE

APPLICATION HINTS

The LT1086 family of three terminal regulators is easy to use and has all the protection features that are expected in high performance voltage regulators. They are short circuit protected, have safe area protection as well as thermal shutdown to turn off the regulator should the temperature exceed about $165^{\circ}C$ at the sense point.

These regulators are pin compatible with older three terminal adjustable devices, offer lower dropout voltage and more precise reference tolerance. Further, the reference stability with temperature is improved over older types of regulators. The only circuit difference between using the LT1086 family and older regulators is that they require an output capacitor for stability.

Stability

The circuit design used in the LT1086 family requires the use of an output capacitor as part of the device frequency compensation. For all operating conditions, the addition of $150\mu F$ aluminum electrolytic or a $22\mu F$ solid tantalum on the output will ensure stability. Normally, capacitors much smaller than this can be used with the LT1086. Many different types of capacitors with widely varying characteristics are available. These capacitors differ in capacitor tolerance (sometimes ranging up to $\pm 100\%$), equivalent series resistance, and capacitance temperature coefficient. The $150\mu F$ or $22\mu F$ values given will ensure stability.

When using the LT1086 the adjustment terminal can be bypassed to improve ripple rejection. When the adjustment terminal is bypassed the requirement for an output capacitor increases. The values of $22\mu F$ tantalum or $150\mu F$ aluminum cover all cases of bypassing the adjustment terminal. For fixed voltage devices or adjustable devices without an adjust pin bypass capacitor, smaller output capacitors can be used with equally good results and the table below shows approximately what size capacitors are needed to ensure stability.

Recommended Capacitor Values

Input	Output	Adjustment
$10\mu F$	$10\mu F$ Tantalum, $50\mu F$ Aluminum	None
$10\mu F$	$22\mu F$ Tantalum, $150\mu F$ Aluminum	$20\mu F$

Normally, capacitor values on the order of $100\mu F$ are used in the output of many regulators to ensure good transient response with heavy load current changes. Output capacitance can be increased without limit and larger values of output capacitor further improve stability and transient response of the LT1086 regulators.

Another possible stability problem that can occur in monolithic IC regulators is current limit oscillations. These can occur because, in current limit, the safe area

APPLICATION HINTS

protection exhibits a negative impedance. The safe area protection decreases the current limit as the input-to-output voltage increases. That is the equivalent of having a negative resistance since increasing voltage causes current to decrease. Negative resistance during current limit is not unique to the LT1086 series and has been present on all power IC regulators. The value of the negative resistance is a function of how fast the current limit is folded back as input-to-output voltage increases. This negative resistance can react with capacitors or inductors on the input to cause oscillation during current limiting. Depending on the value of series resistance, the overall circuitry may end up unstable. Since this is a system problem, it is not necessarily easy to solve; however it does not cause any problems with the IC regulator and can usually be ignored.

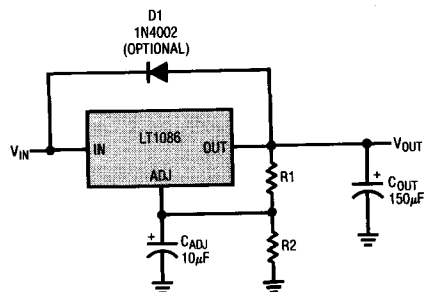
Protection Diodes

In normal operation, the LT1086 family does not need any protection diodes. Older adjustable regulators required protection diodes between the adjustment pin and the output and from the output to the input to prevent overstressing the die. The internal current paths on the LT1086 adjustment pin are limited by internal resistors. Therefore, even with capacitors on the adjustment pin, no protection diode is needed to ensure device safety under short circuit conditions.

Diodes between input and output are usually not needed. The internal diode between the input and the output pins of the LT1086 family can handle microsecond surge currents of 10A to 20A. Even with large output capacitances, it is very difficult to get those values of surge currents in normal operations. Only with high value of output capacitors, such as 1000 μ F to 5000 μ F and with the input pin instantaneously shorted to ground, can damage occur. A crowbar circuit at the input of the LT1086 can generate those kinds of currents, and a diode from output to input is then recommended. Normal power supply cycling or even plugging and unplugging in the system will not generate current large enough to do any damage.

The adjustment pin can be driven on a transient basis ± 25 V, with respect to the output without any device

degradation. Of course, as with any IC regulator, exceeding the maximum input to output voltage differential causes the internal transistors to break down and none of the protection circuitry is functional.



Overload Recovery

Like any of the IC power regulators, the LT1086 has safe area protection. The safe area protection decreases the current limit as input-to-output voltage increases and keeps the power transistor inside a safe operating region for all values of input-to-output voltage. The LT1086 protection is designed to provide some output current at all values of input-to-output voltage up to the device breakdown.

When power is first turned on, as the input voltage rises, the output follows the input, allowing the regulator to start up into very heavy loads. During the start-up, as the input voltage is rising, the input-to-output voltage differential remains small, allowing the regulator to supply large output currents. With high input voltage, a problem can occur wherein removal of an output short will not allow the output voltage to recover. Older regulators, such as the 7800 series, also exhibited this phenomenon, so it is not unique to the LT1086.

The problem occurs with a heavy output load when the input voltage is high and the output voltage is low, such as immediately after a removal of a short. The load line for such a load may intersect the output current curve at two points. If this happens, there are two stable output operating points for the regulator. With this double intersection, the power supply may need to be cycled down to zero and brought up again to make the output recover.

APPLICATION HINTS

Ripple Rejection

For the LT1086 the typical curves for ripple rejection reflect values for a bypassed adjustment pin. This curve will be true for all values of output voltage. For proper bypassing, and ripple rejection approaching the values shown, the impedance of the adjust pin capacitor, at the ripple frequency should equal the value of R1, (normally 100Ω–120Ω). The size of the required adjust pin capacitor is a function of the input ripple frequency. At 120Hz the adjust pin capacitor should be 13μF if R1 = 100Ω. At 10kHz only 0.16μF is needed.

For circuits without an adjust pin bypass capacitor, the ripple rejection will be a function of output voltage. The output ripple will increase directly as a ratio of the output voltage to the reference voltage (V_{OUT}/V_{REF}). For example, with the output voltage equal to 5V, and no adjust pin capacitor, the output ripple will be higher by the ratio of 5V/1.25V or 4 times larger. Ripple rejection will be degraded by 12dB from the value shown on the LT1086 curve. Typical curves are provided for -5 and -12 devices since the adjust pin is not available.

Output Voltage

The LT1086 develops a 1.25V reference voltage between the output and the adjust terminal (see Figure 1). By placing a resistor, R1, between these two terminals, a constant current is caused to flow through R1 and down through R2 to set the overall output voltage. Normally this current is chosen to be the specified minimum load current of 10mA. Because I_{ADJ} is very small and constant when compared with the current through R1, it represents a small error and can usually be ignored. For fixed voltage devices R1 and R2 are included in the device.

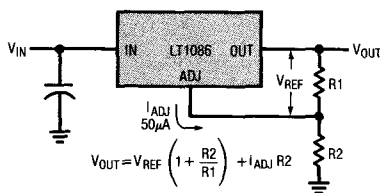


Figure 1. Basic Adjustable Regulator

Load Regulation

Because the LT1086 is a three-terminal device, it is not possible to provide true remote load sensing. Load regulation will be limited by the resistance of the wire connecting the regulator to the load. The data sheet specification for load regulation is measured at the bottom of the package. Negative side sensing is a true Kelvin connection, with the bottom of the output divider returned to the negative side of the load. Although it may not be immediately obvious, best load regulation is obtained when the top of the resistor divider, (R1), is connected *directly* to the case *not to the load*. This is illustrated in Figure 2. If R1 were connected to the load, the effective resistance between the regulator and the load would be

$$R_p \times \frac{R_2 + R_1}{R_1}, R_p = \text{Parasitic Line Resistance.}$$

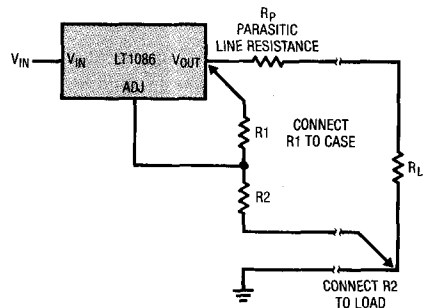


Figure 2. Connections for Best Load Regulation

Connected as shown, R_p is not multiplied by the divider ratio. R_p is about 0.004Ω per foot using 16 gauge wire. This translates to 4mV/ft at 1A load current, so it is important to keep the positive lead between regulator and load as short as possible, and use large wire or PC board traces.

Note that the resistance of the package leads for the H package ≈ 0.06Ω/in. While it is usually not possible to connect the load directly to the package, it is possible to connect larger wire or PC traces close to the case to avoid voltage drops that will degrade load regulation.

For fixed voltage devices the top of R1 is internally Kelvin connected, and the ground pin can be used for negative side sensing.

APPLICATION HINTS

Thermal Considerations

The LT1086 series of regulators have internal power and thermal limiting circuitry designed to protect the device under overload conditions. For continuous normal load conditions however, maximum junction temperature ratings must not be exceeded. It is important to give careful consideration to all sources of thermal resistance from junction to ambient. This includes junction to case, case to heat sink interface, and heat sink resistance itself. New thermal resistance specifications have been developed to more accurately reflect device temperature and ensure safe operating temperatures. The data section for these new regulators provides a separate thermal resistance and maximum junction temperature for both the *Control Section* and the *Power Transistor*. Previous regulators, with a single junction to case thermal resistance specification, used an average of the two values provided here and therefore could allow excessive junction temperatures under certain conditions of ambient temperature and heat sink resistance. To avoid this possibility, calculations should be made for both sections to ensure that both thermal limits are met.

For example, using a LT1086CK (TO-3, Commercial) and assuming:

$$\begin{aligned} V_{IN} \text{ (max continuous)} &= 9V, V_{OUT} = 5V, I_{OUT} = 1A, \\ T_{AMBIENT} &= 75^\circ\text{C}, \theta_{HEAT\ SINK} = 3^\circ\text{C/W}, \\ \theta_{CASE\ TO\ HEAT\ SINK} &= 0.2^\circ\text{C/W for K package with} \\ &\text{thermal compound.} \end{aligned}$$

Power dissipation under these conditions is equal to:

$$P_D = (V_{IN} - V_{OUT})(I_{OUT}) = 4W$$

Junction temperature will be equal to:

$$T_j = T_{AMBIENT} + P_D (\theta_{HEAT\ SINK} + \theta_{CASE\ TO\ HEAT\ SINK} + \theta_{jc})$$

For the Control Section:

$$\begin{aligned} T_j &= 75^\circ\text{C} + 4W (3^\circ\text{C/W} + 0.2^\circ\text{C/W} + 1.7^\circ\text{C/W}) = 95^\circ\text{C} \\ 95^\circ\text{C} < 125^\circ\text{C} &= T_{jmax} \text{ (Control Section} \\ &\text{Commercial Range)} \end{aligned}$$

For the Power Transistor:

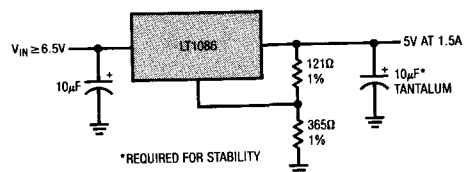
$$\begin{aligned} T_j &= 75^\circ\text{C} + 4W (3^\circ\text{C/W} + 0.2^\circ\text{C/W} + 4^\circ\text{C/W}) = 103.8^\circ\text{C} \\ 103.8^\circ\text{C} < 150^\circ\text{C} &= T_{jmax} \text{ (Power Transistor} \\ &\text{Commercial Range)} \end{aligned}$$

In both cases the junction temperature is below the maximum rating for the respective sections, ensuring reliable operation.

Junction to case thermal resistance for the K and T packages is specified from the I.C. junction to the bottom of the case directly below the die. This is the lowest resistance path for heat flow. While this is also the lowest resistance path for the H package, most available heat sinks for this package are of the clip-on type that attach to the cap of the package. The datasheet specification for thermal resistance for the H package is therefore written to reflect this. In all cases proper mounting is required to ensure the best possible heat flow from the die to the heat sink. Thermal compound at the case-to-heat sink interface is strongly recommended. In the case of the H package, mounting the device so that heat can flow out the bottom of the case will significantly lower thermal resistance (\approx a factor of 2). If the case of the device must be electrically isolated, a thermally conductive spacer can be used, as long as its added contribution to thermal resistance is considered. Note that the case of all devices in this series is electrically connected to the output.

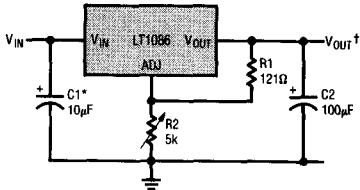
4

5V, 1.5A Regulator



TYPICAL APPLICATIONS

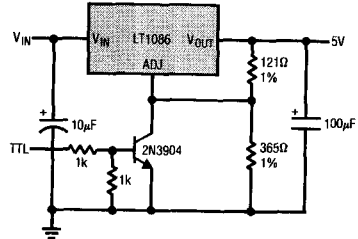
1.2V-15V Adjustable Regulator



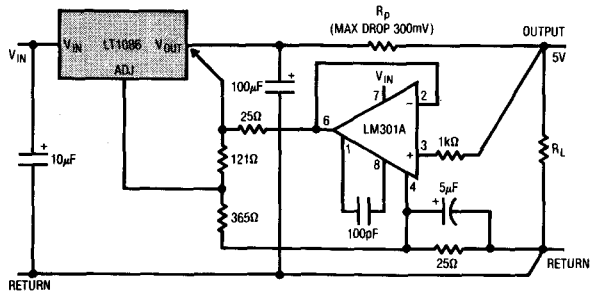
*NEEDED IF DEVICE IS FAR FROM FILTER CAPACITORS

$$V_{OUT} = 1.25V \left(1 + \frac{R2}{R1}\right)$$

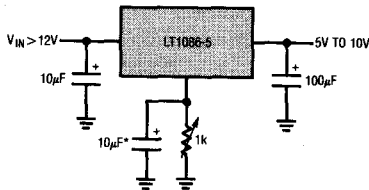
5V Regulator with Shutdown



Remote Sensing

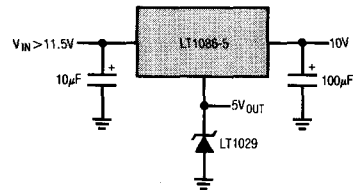


Adjusting Output Voltage of Fixed Regulators

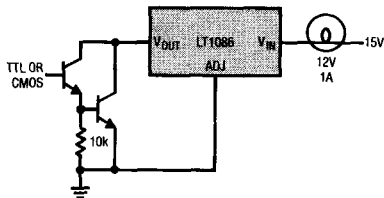


*OPTIONAL IMPROVES RIPPLE REJECTION

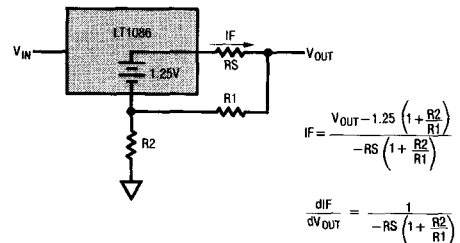
Regulator with Reference



Protected High Current Lamp Driver

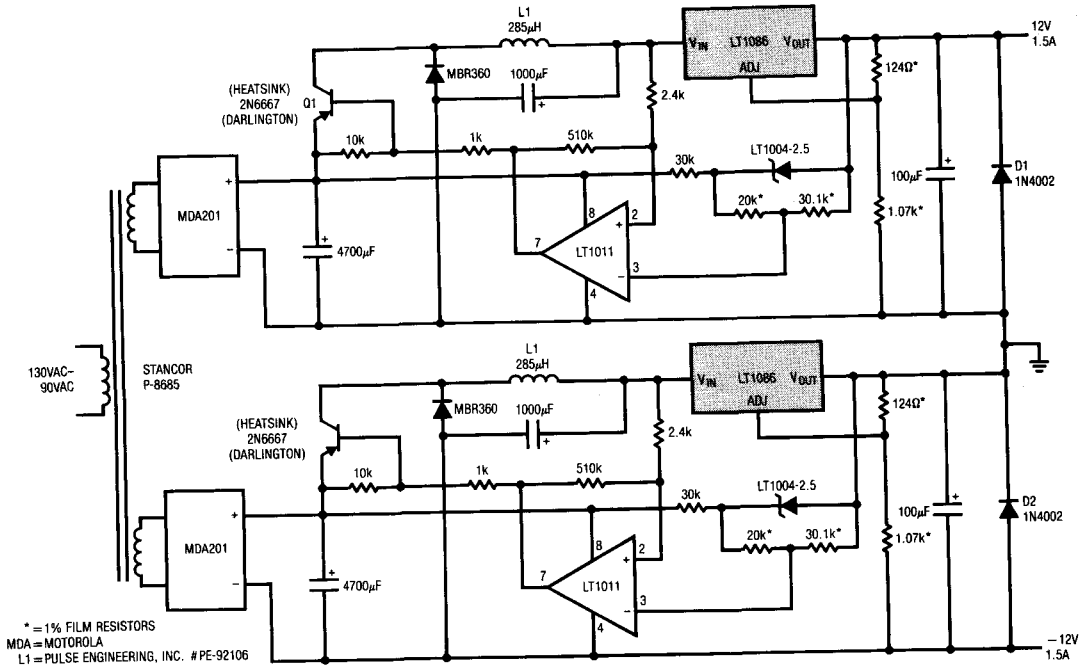


Battery Charger



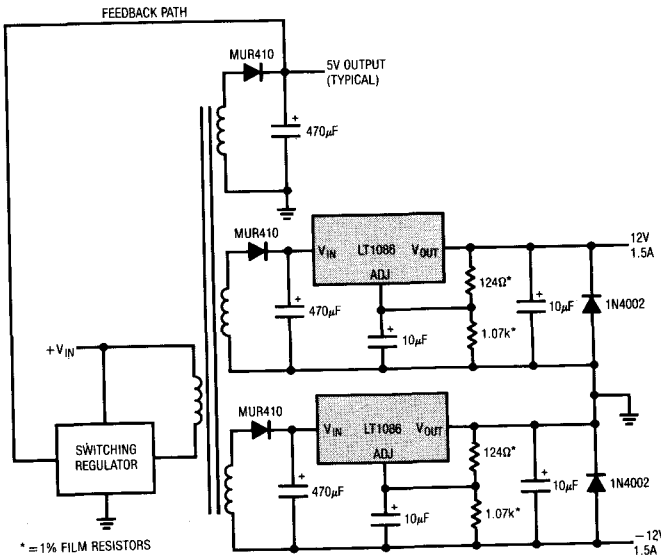
TYPICAL APPLICATIONS

High Efficiency Dual Linear Supply

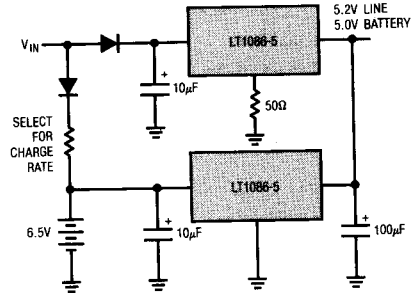


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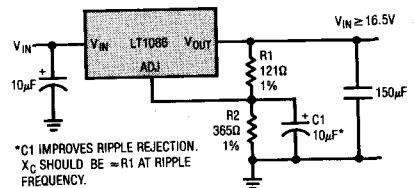
High Efficiency Dual Supply



Battery Backed Up Regulated Supply



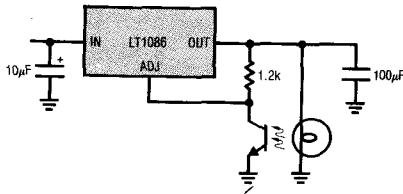
Improving Ripple Rejection



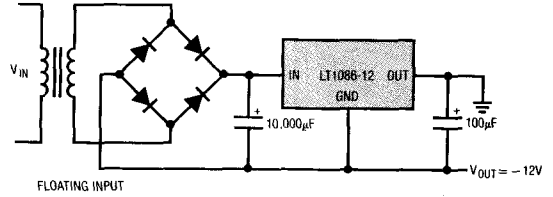
LT1086/LT1086-5
LT1086-12/LT1086H

TYPICAL APPLICATIONS

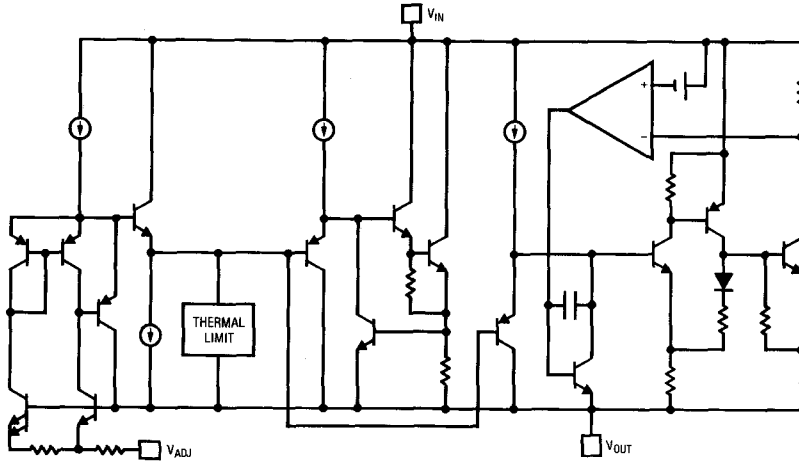
Automatic Light Control



Low Dropout Negative Supply

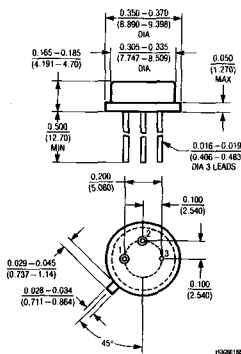


BLOCK DIAGRAM

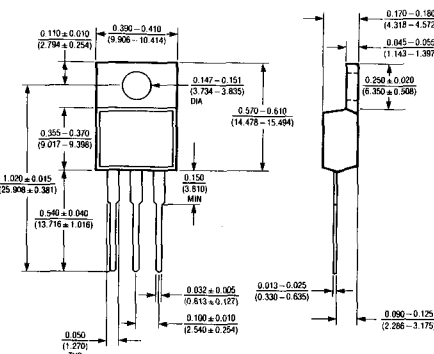


PACKAGE DESCRIPTIONS Dimensions in inches (millimeters) unless otherwise noted.

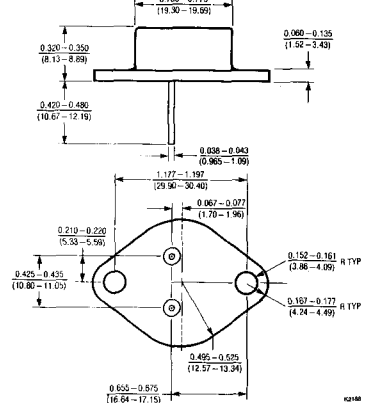
H Package
3-Lead TO-39 Metal Can



T Package
3-Lead TO-220 Plastic



K Package
2-Lead TO-3 Metal Can



FEATURES

- 8-Lead MiniDIP
- 40 μ A Supply Current
- 125mA Output Current
- 2.5V Reference Voltage
- Reference Output Sources 2mA and Sinks 2mA
- Open Collector
- Comparator Sinks 10mA
- Logic Shutdown
- 0.2V Dropout Voltage
- Thermal Limiting

APPLICATIONS

- Battery Systems
- Battery Backup System
- Portable Terminals
- Portable Instruments
- Memory Keep Alive

DESCRIPTION

The LT1120 is a combination micropower positive regulator and free collector comparator on a single monolithic chip. With only 40 μ A supply current, the LT1120 can supply over 125mA of output current. Input voltage range is from 4.5V to 36V and dropout voltage is 0.6V at 125mA. Dropout voltage decreases with lower load currents. Also included on the chip is a class B output 2.5V reference that can either source or sink current. A shutdown pin allows logic shutdown of the output.

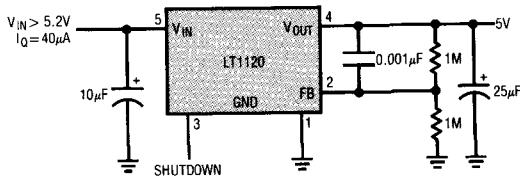
The comparator can be used as a comparator for system or battery monitoring. For example, the comparator can be used to warn of low system voltage. Frequency compensation of the comparator for amplifier applications can be obtained by adding external output capacitance.

The 2.5V reference will source or sink current. This allows it to be used as a supply splitter or auxiliary output.

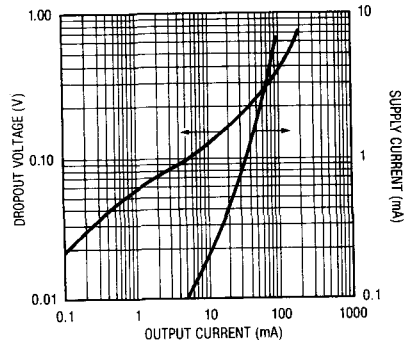
 REFER TO TABLE OF CONTENTS
 FOR REVISED DATA LOCATION

4

5V Regulator



Dropout Voltage and Supply Current



ABSOLUTE MAXIMUM RATINGS

Input Voltage 36V
 NPN Collector Voltage 36V
 Output Short Circuit Duration Indefinite
 Power Dissipation Internally Limited

Operating Temperature Range
 LT1120C 0°C to 100°C
 Storage Temperature Range
 LT1120C -65°C to 150°C

PACKAGE/ORDER INFORMATION

<p>J PACKAGE 8-LEAD CERAMIC MINIDIP</p> <p>N PACKAGE 8-LEAD PLASTIC MINIDIP</p>	ORDER PART NUMBER	<p>H PACKAGE 8-LEAD TO-5 METAL CAN</p>	ORDER PART NUMBER
	LT1120CJ8 LT1120CN8		LT1120CH

ELECTRICAL CHARACTERISTICS $T_J = 25^\circ\text{C}$

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Reference					
Reference Voltage	$4.5\text{V} \leq V_{IN} \leq 36\text{V}$	2.46	2.50	2.54	V
Line Regulation	$4.5\text{V} \leq V_{IN} \leq 36\text{V}$		0.01	0.015	%/V
Load Regulation	$-2.0\text{mA} \leq I_{REF} \leq 2\text{mA}, V_{IN} = 12\text{V}$		0.3	0.6	%
Output Source Current	$V_{IN} = 5\text{V}$	2	4		mA
Output Sink Current	$V_{IN} = 5\text{V}$	2	4		mA
Temperature Stability			1		%
Regulator					
Supply Current	$V_{IN} = 6\text{V}, I_{OUT} \leq 100\mu\text{A}$ $V_{IN} = 36\text{V}, I_{OUT} \leq 100\mu\text{A}$ $V_{IN} = 12\text{V}, I_{OUT} = 125\text{mA}$		45 75 11	80 100 20	μA μA mA
Output Current	$(V_{IN} - V_{OUT}) \geq 1\text{V}, V_{IN} \geq 6\text{V}$	125			mA
Load Regulation	$(V_{IN} - V_{OUT}) \geq 1\text{V}, V_{IN} \geq 6\text{V}$		0.2	0.5	%
Line Regulation	$6\text{V} \leq V_{IN} \leq 36\text{V}$		0.01	0.015	%/V
Dropout Voltage	$I_{OUT} = 100\mu\text{A}$ $I_{OUT} = 125\text{mA}$		0.02 0.4	0.05 0.65	V V
Feedback Sense Voltage	$V_{IN} = 12\text{V}$	2.44	2.5	2.56	V
Shutdown Pin Voltage	$V_{OUT} \leq 0.5\text{V}$	Normal		0.4	V
		Shutdown	2.2	1.4	
Shutdown Pin Current	$V_{IN} = 1.4\text{V}$		25		μA

ELECTRICAL CHARACTERISTICS $T_J = 25^\circ\text{C}$

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Regulator					
Feedback Bias Current			15	40	nA
Minimum Load Current	$V_{IN} = 36\text{V}$		1	5	μA
Short Circuit Current	$V_{IN} = 36\text{V}$		250	360	mA
Comparator					
Offset Voltage	$0\text{V} \leq V_{CM} \leq 35\text{V}, V_{IN} = 36\text{V}$		3	7	mV
Bias Current	$0\text{V} \leq V_{CM} \leq 35\text{V}, V_{IN} = 36\text{V}$ (Note 1)		15	40	nA
Offset Current	$0\text{V} \leq V_{CM} \leq 35\text{V}, V_{IN} = 36\text{V}$		4	15	nA
Gain	$\Delta V_{OUT} = 29\text{V}, R_L = 20\text{k}$	2000	10000		V/V
Common Mode Rejection	$0\text{V} \leq V_{CM} \leq 35\text{V}, V_{IN} = 36\text{V}$	80	94		dB
Power Supply Rejection	$4.5\text{V} \leq V_S \leq 36\text{V}$	80	96		dB
Output Sink Current	$V_{IN} = 4.5\text{V}$	10	18		mA
Saturation Voltage	$I_{OUT} = 1\text{mA}$		0.4	0.6	V
Input Voltage Range		0		$V_{IN} - 1$	V
Response Time			5		μs
Leakage Current				2	μA

4

ELECTRICAL CHARACTERISTICS

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Reference					
Reference Voltage	$4.5\text{V} \leq V_{IN} \leq 36\text{V}$	● 2.40	2.50	2.55	V
Line Regulation	$4.5\text{V} \leq V_{IN} \leq 36\text{V}$	●	0.01	0.02	%/V
Load Regulation	$-2.0\text{mA} \leq I_{REF} \leq 2\text{mA}, V_{IN} = 12\text{V}$	●	0.4	0.8	%
Output Source Current	$V_{IN} = 5\text{V}$	● 2			mA
Output Sink Current	$V_{IN} = 5\text{V}$	● 2			mA
Regulator					
Supply Current	$V_{IN} = 6\text{V}, I_{OUT} \leq 100\mu\text{A}$ $V_{IN} = 36\text{V}, I_{OUT} \leq 100\mu\text{A}$ $V_{IN} = 12\text{V}, I_{OUT} = 125\text{mA}$	●	65 85 11	95 100 20	μA μA mA
Output Current	$(V_{IN} - V_{OUT}) \geq 1\text{V}, V_{IN} \geq 6\text{V}$	● 125			mA
Load Regulation	$(V_{IN} - V_{OUT}) \geq 1\text{V}, V_{IN} \geq 6\text{V}$	●		1	%
Line Regulation	$6\text{V} \leq V_{IN} \leq 36\text{V}$	●		0.02	%/V
Dropout Voltage	$I_{OUT} = 100\mu\text{A}$ $I_{OUT} = 125\text{mA}$	●		0.06 0.85	V V
Feedback Sense Voltage	$V_{IN} = 12\text{V}$	● 2.38	2.5	2.57	V
Feedback Bias Current		●		50	nA
Minimum Load Current	$V_{IN} = 36\text{V}$	●		50	μA
Short Circuit Current	$V_{IN} = 36\text{V}$	●	240	360	mA

ELECTRICAL CHARACTERISTICS

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Comparator					
Offset Voltage		●		10	mV
Bias Current	$V_{IN} = 36V$ (Note 1)	●	15	60	nA
Gain	$\Delta V_{OUT} = 29V$, $R_L = 20k$	●	1000		V/V
Output Sink Current	$V_{IN} = 4.5V$	●	5	10	mA
Leakage Current	$V_{IN} = 36V$	●		8	μA

The ● denotes the specifications which apply over full operating temperature range.

Note 1: For $0V \leq V_{CM} \leq 0.1V$ and $T_A > 85^\circ C$ I bias max is 100nA.

PIN FUNCTIONS

Pin 1—Ground.

Pin 2—Feedback. This is the feedback point of the regulator. When operating, it is nominally at 2.5V. Optimum source resistance is 200k to 500k. The feedback pin should not be driven below ground or more positive than 5V.

Pin 3—Shutdown. A logic 1 shuts off main regulator. Caution: noise or leakage into the shutdown pin can affect output voltage.

Pin 4—Regulator Output. Main output, requires $10\mu F$ output capacitor. Can be shorted to V_{IN} or ground without damaging device.

Pin 5—Input Supply. Bypass with $10\mu F$ cap. Must always be more positive than ground.

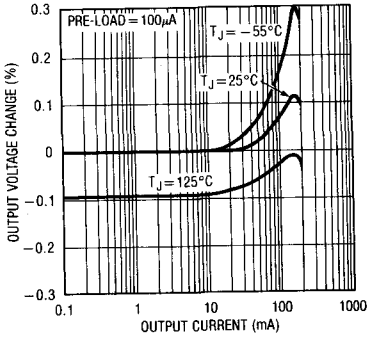
Pin 6—Reference. 2.5V can source or sink current. May be shorted to ground or up to 5V. Voltages in excess of 5V can damage the device.

Pin 7—Comparator Output. May be connected to any voltage from ground to 36V more positive than ground (operates above V_{IN}). Short circuit protected.

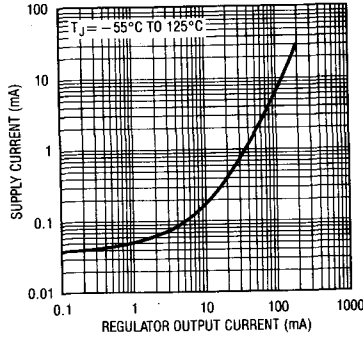
Pin 8—Comparator Input. Inverting comparator input.

TYPICAL PERFORMANCE CHARACTERISTICS

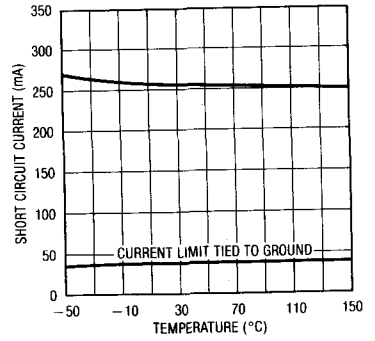
Regulator Load Regulation



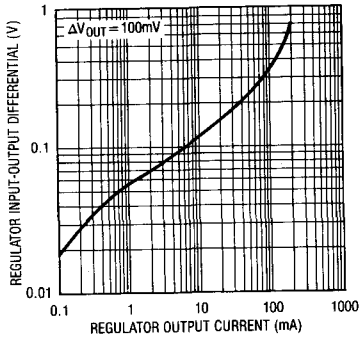
Supply Current



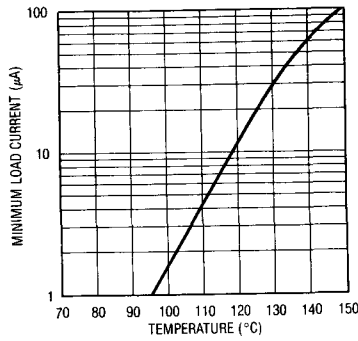
Regulator Short Circuit Current



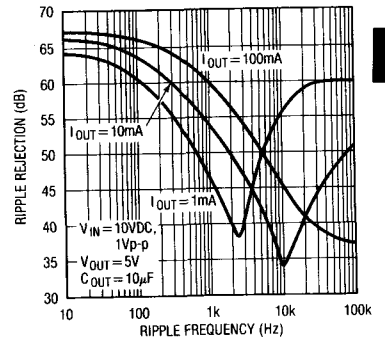
Dropout Voltage



Regulator Minimum Load Current

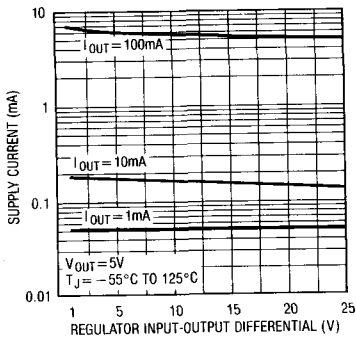


Regulator Ripple Rejection

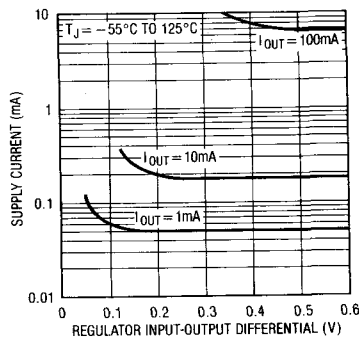


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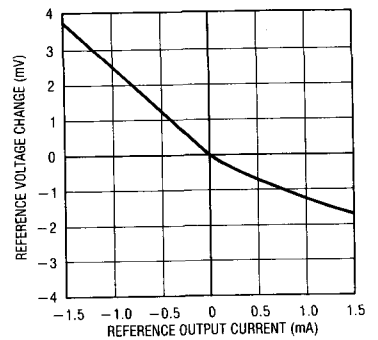
Supply Current



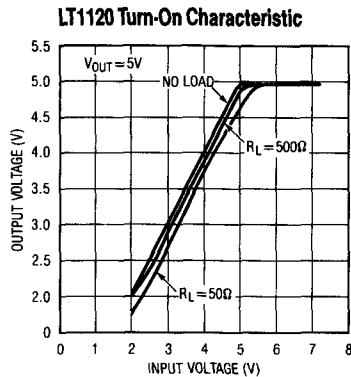
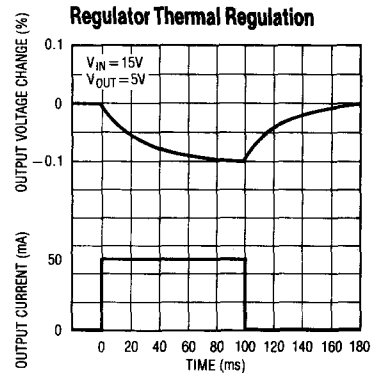
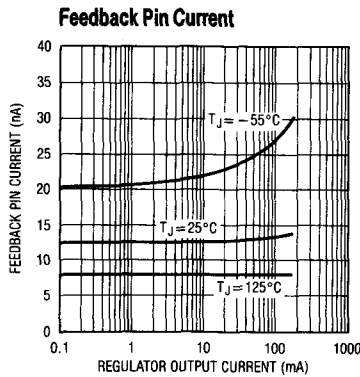
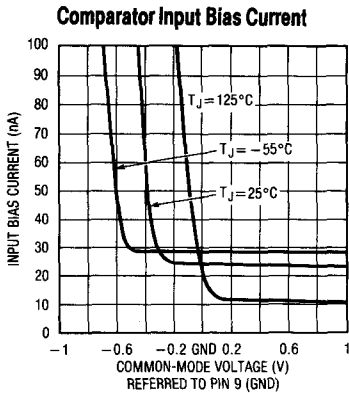
Supply Current at Dropout



Reference Regulation



TYPICAL PERFORMANCE CHARACTERISTICS



APPLICATION HINTS

The LT1120 is especially suited for micropower system applications. For example, the comparator section of the LT1020 may be used as a battery checker to provide an indication of low battery. Another type of system application for the LT1120 would be to generate the equivalent of split supplies off of a single power input. The regulator section provides regulated output voltage and the reference, which can both source and sink current is then an artificial system ground providing a split supply for the system.

For many applications the comparator can be frequency compensated to operate as an amplifier. Compensation values for various gains are given in the datasheet. The comparator gain is purposely low to make it easier to frequency compensate as an amplifier. The NPN output is capable of sinking 10mA and can drive loads connected to voltages in excess of the positive power supply. This is useful for driving switches or linear regulators off of a higher input voltage.

APPLICATION HINTS

Reference

Internal to the LT1120 is a 2.5V trimmed class B output reference. The reference was designed to be able to source or sink current so it could be used in supply splitting applications as well as a general purpose reference for external circuitry. The design of the reference allows it to source typically 4 or 5mA and sink 2mA. The available source and sink current decreases as temperature increases. It is sometimes desirable to decrease the AC output impedance by placing an output capacitor on them. The reference in the LT1120 becomes unstable with large capacitive loads placed directly on it. When using an output capacitor, about 20Ω should be used to isolate the capacitor from the reference pin. This 20Ω resistor can be placed directly in series with the capacitor or alternatively the reference line can have 20Ω placed in series with it and then a capacitor to ground. This is shown in Figure 1. Other than placing large capacitive loads on the reference, no other precautions are necessary and the reference is stable with nominal stray capacitances.

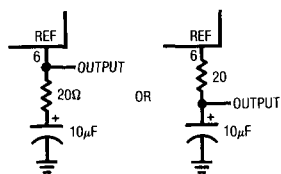


Figure 1. Bypassing Reference

Overload Protection

The main regulator in the LT1120 is current limited at approximately 250mA. The current limit is stable with both input voltage and temperature.

Like most other IC regulators, a minimum load is required on the output of the LT1120 to maintain regulation. For most standard regulators this is normally specified as 5mA. Of course, for a micropower regulator this would be a tremendously large current. The output current must be large enough to absorb all the leakage current of the pass transistor at the maximum operating temperature. It also affects the transient response; low output currents have long recovery times from load transients. At high operating temperatures the minimum load current increases and having too low of a load current may cause the output to go unregulated. Devices are tested for minimum load current at high temperature. The output voltage setting resistors to the feedback terminal can usually be used to provide the minimum load current.

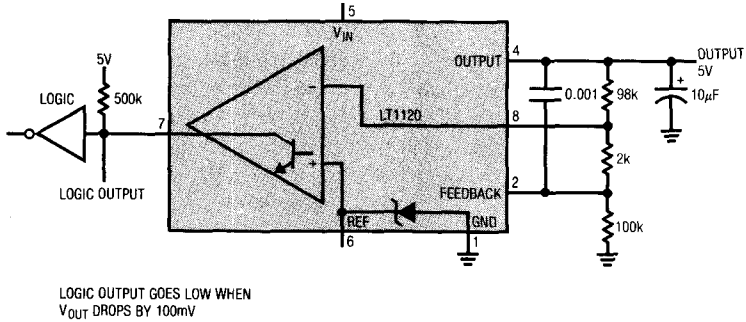
Frequency Compensation

The LT1120 is frequency compensated by a dominant pole on the output. An output capacitor of $10\mu\text{F}$ is usually large enough to provide good stability. **Increasing the output capacitor above $10\mu\text{F}$ further improves stability.** In order to ensure stability, a feedback capacitor is needed between the output pin and the feedback pin. This is because stray capacitance can form another pole with the large value of feedback resistors used with the LT1120. Also, a feedback capacitor minimizes noise pickup and improves ripple rejection.

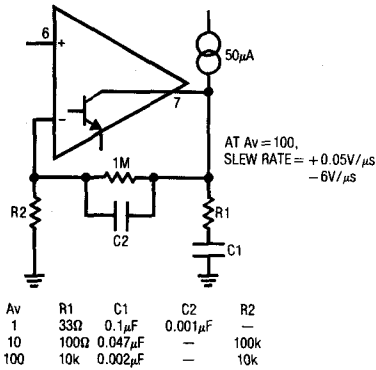
With the large dynamic operating range of the output current, 10000:1, frequency response changes widely. Low AC impedance capacitors are needed to insure stability. While solid tantalum are best, aluminum electrolytics can be used but larger capacitor values may be needed.

TYPICAL APPLICATIONS

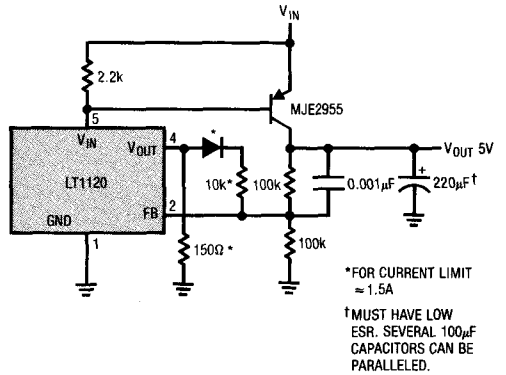
Regulator with Output Voltage Monitor



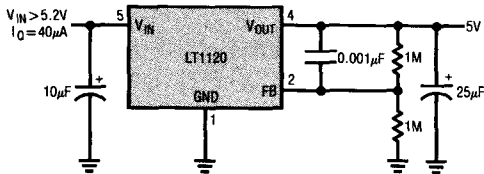
Compensating the Comparator as an Op Amp



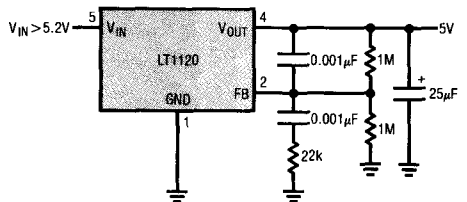
1 Amp Low Dropout Regulator



5V Regulator

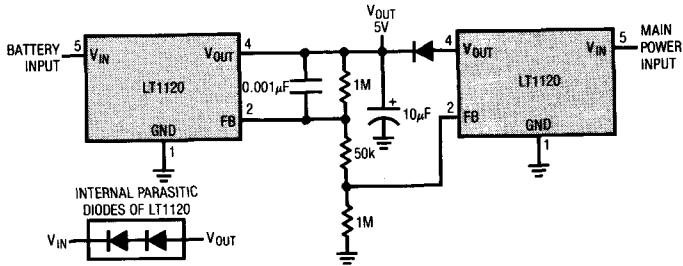


Regulator with Improved Transient Response

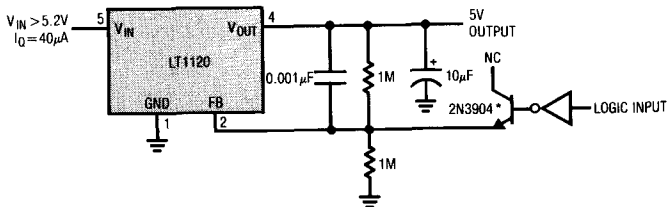


TYPICAL APPLICATIONS

Battery Backup Regulator

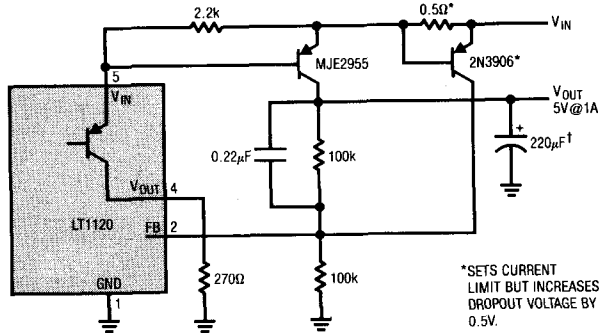


5V Regulator with Feedback Shutdown



*TRANSISTOR USED BECAUSE OF LOW LEAKAGE CHARACTERISTICS.
TO TURN OFF THE OUTPUT OF THE LT1120
FORCE FB (PIN 2) > 2.5V.

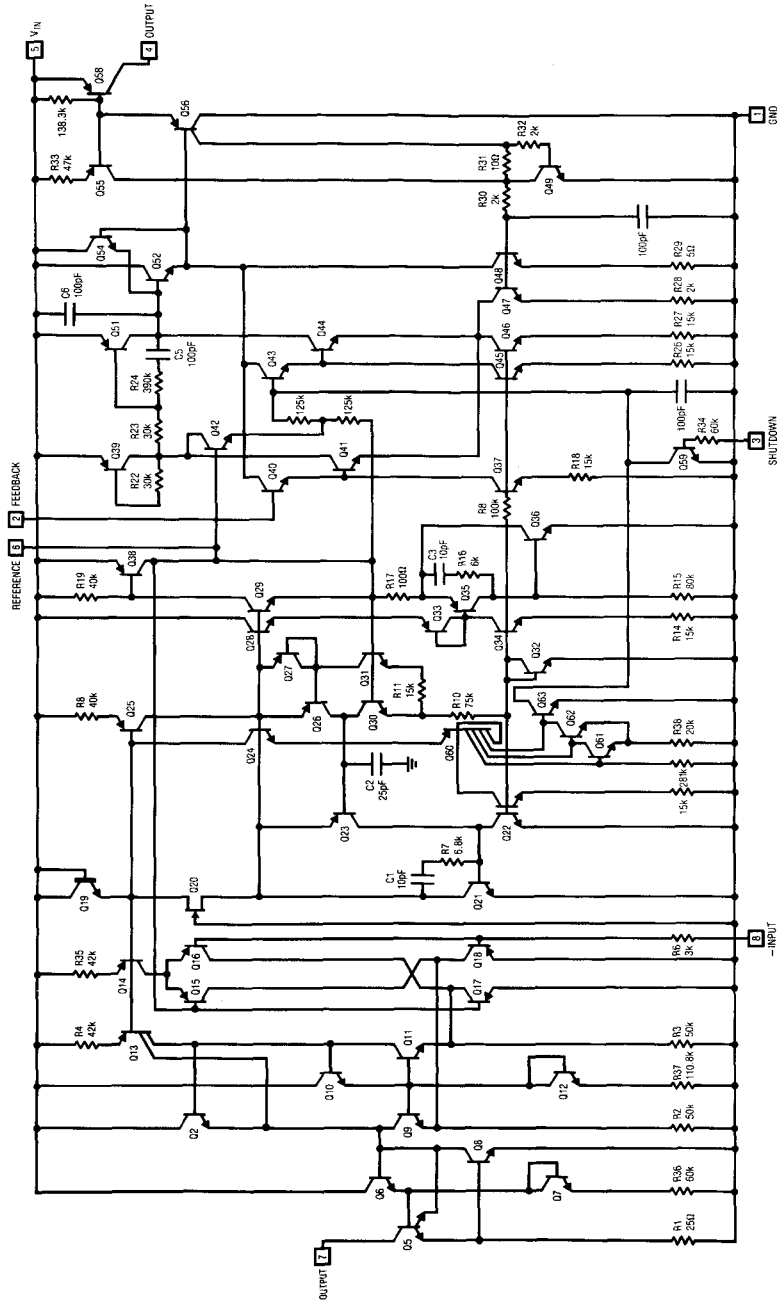
Current Limited 1 Amp Regulator



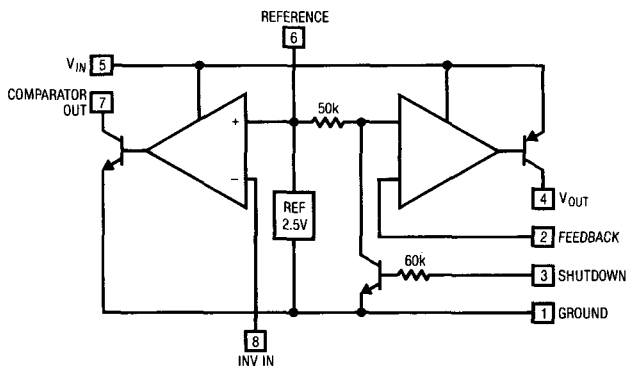
*SETS CURRENT
LIMIT BUT INCREASES
DROPOUT VOLTAGE BY
0.5V.

† MUST HAVE LOW
ESR. SEVERAL 100µF
CAPACITORS CAN BE
PARALLELED.

SCHEMATIC DIAGRAM



BLOCK DIAGRAM



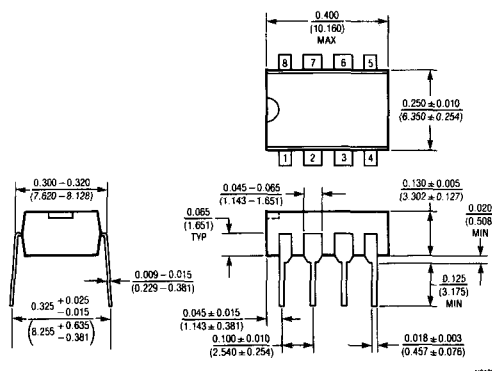
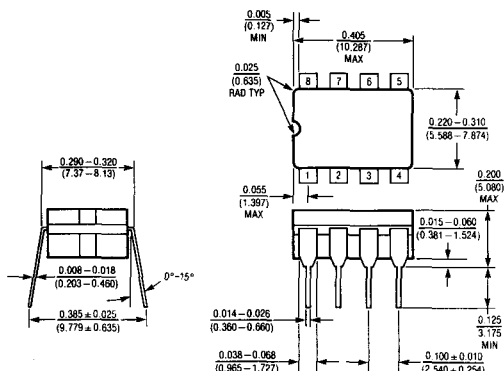
PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

4

J Package
8-Lead Ceramic MiniDIP

N Package
8-Lead Plastic MiniDIP

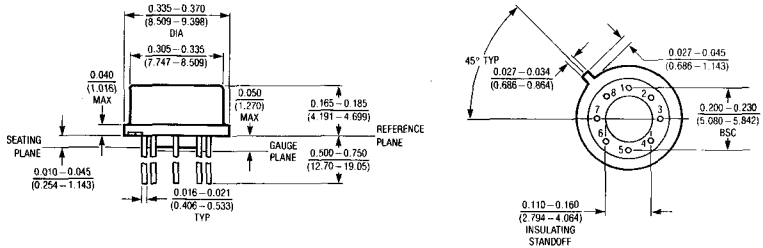


T_{JMAX}	θ_{JA}
150°C	100°C/W

T_{JMAX}	θ_{JA}
110°C	130°C/W

PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

H Package
8-Lead TO-5 Metal Can



NOTE: LEAD DIAMETER IS UNCONTROLLED BETWEEN THE REFERENCE PLANE AND SEATING PLANE.

48188

T_{JMAX}	θ_{JA}	θ_{JC}
150°C	150°C/W	45°C/W

FEATURES

- *Guaranteed* 1% Output Voltage Tolerance
- *Guaranteed* max. 0.01%/V Line Regulation
- *Guaranteed* max. 0.3% Load Regulation
- Min. 1.5A Output Current
- 100% Burn-in in Thermal Overload

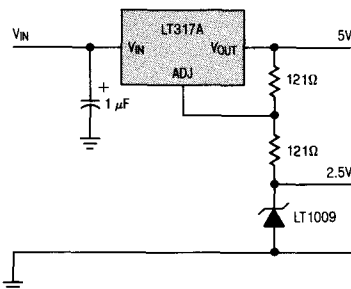
APPLICATIONS

- Wide Range Power Supplies
- Constant Current Supplies
- Voltage Programmable Supplies

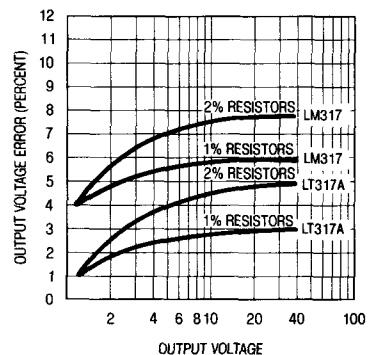
DESCRIPTION

The LT117A Series are 3-terminal positive adjustable voltage regulators which offer improved performance over earlier devices. A major feature of the LT117A is the output voltage tolerance is guaranteed at a maximum of $\pm 1\%$, allowing an overall power supply tolerance to be better than 3% using inexpensive 1% resistors. Line and load regulation performance has been improved as well. Additionally, the LT117A reference voltage is guaranteed not to exceed 2% when operating over the full load, line and power dissipation conditions. The LT117A adjustable regulators offer an improved solution for all positive voltage regulator requirements with load currents up to 1.5 amps.

Regulator with Reference



Output Voltage Error



LT117A/LT317A LM117/LM317

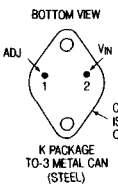
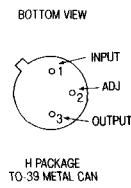
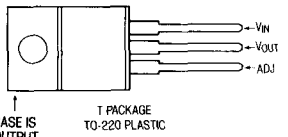
ABSOLUTE MAXIMUM RATINGS

Power Dissipation Internally Limited
 Input to Output Voltage Differential 40V
 Operating Junction Temperature Range
 LT117A/LM117 -55°C to 150°C
 LT317A/LM317 0°C to 125°C
 Storage Temperature Range
 LT117A/LM117 -65°C to 150°C
 LT317A/LM317 -65°C to 150°C
 Lead Temperature (Soldering, 10 sec.) 300°C

PRECONDITIONING:

100% THERMAL LIMIT BURN-IN

PACKAGE/ORDER INFORMATION

 <p>ORDER PART NO. LT117AK LT317AK LM117K LM317K</p>	 <p>ORDER PART NO. LT117AH LT317AH LM117H LM317H</p>
 <p>ORDER PART NO. LT317AT LM317T</p>	

ELECTRICAL CHARACTERISTICS (See Note 1) LT117A/LM117

SYMBOL	PARAMETER	CONDITIONS	LT117A			LM117			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V _{REF}	Reference Voltage	I _{OUT} = 10mA, T _J = 25°C	1.238	1.250	1.262				V
		3V ≤ (V _{IN} - V _{OUT}) ≤ 40V 10mA ≤ I _{OUT} ≤ I _{max} , P ≤ P _{max}	● 1.225	1.250	1.270	1.20	1.25	1.30	V
ΔV _{OUT} /ΔV _{IN}	Line Regulation	3V ≤ (V _{IN} - V _{OUT}) ≤ 40V, (See Note 2)		0.005	0.01	0.01	0.02	%/V	
		●	0.01	0.02	0.02	0.05	%/V		
ΔV _{OUT} /ΔI _{OUT}	Load Regulation	10mA ≤ I _{OUT} ≤ I _{max} , (See Note 2) V _{OUT} ≤ 5V V _{OUT} ≥ 5V		5	15	5	15	mV	
		●	0.1	0.3	0.1	0.3	%		
		V _{OUT} ≤ 5V V _{OUT} ≥ 5V	●	20	50	20	50	mV	
		●	0.3	1	0.3	1	%		
	Thermal Regulation	T _A = 25°C, 20msec Pulse		0.002	0.02	0.03	0.07	%/W	
	Ripple Rejection	V _{OUT} = 10V, f = 120Hz C _{ADJ} = 0	●	65		65		dB	
		C _{ADJ} = 10μF	●	66	80	66	80	dB	
I _{ADJ}	Adjust Pin Current		●	50	100	50	100	μA	
ΔI _{ADJ}	Adjust Pin Current Change	10mA ≤ I _{OUT} ≤ I _{max} 2.5V ≤ (V _{IN} - V _{OUT}) ≤ 40V	●	0.2	5	0.2	5	μA	
I _{min}	Minimum Load Current	(V _{IN} - V _{OUT}) = 40V	●	3.5	5	3.5	5	mA	
		Current Limit							
		(V _{IN} - V _{OUT}) ≤ 15V K Package H Package	●	1.5	2.2	1.5	2.2	A	
		●	0.5	0.8	0.5	0.8	A		
		(V _{IN} - V _{OUT}) = 40V, T _J = 25°C K Package H Package		0.3	0.5	0.3	0.4	A	
				0.15	0.2	0.15	0.2	A	
ΔV _{OUT} /ΔTemp	Temperature Stability	-55°C ≤ T _J ≤ +150°C		1	2	1		%	
ΔV _{OUT} /ΔTime	Long Term Stability	T _A = 125°C		0.3	1	0.3	1	%	
e _n	RMS Output Noise (% of V _{OUT})	T _A = 25°C, 10Hz ≤ f ≤ 10kHz		0.001		0.001		%	
θ _{Jc}	Thermal Resistance Junction to Case	H Package		12	15	12	15	°C/W	
		K Package		2.3	3	2.3	3	°C/W	

ELECTRICAL CHARACTERISTICS (See Note 1) LT317A/LM317

SYMBOL	PARAMETER	CONDITIONS	LT317A			LM317			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{REF}	Reference Voltage	$I_{OUT} = 10mA$, $T_I = 25^\circ C$	1.238	1.250	1.262				V
		$3V \leq (V_{IN} - V_O) \leq 40V$ $10mA \leq I_{OUT} \leq I_{MAX}$, $P \leq P_{MAX}$	● 1.225	1.250	1.270	1.20	1.25	1.30	V
$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	Line Regulation	$3V \leq (V_{IN} - V_{OUT}) \leq 40V$, (See Note 2)		0.005	0.01	0.01	0.04		%/V
			●	0.01	0.02	0.02	0.07		%/V
$\frac{\Delta V_{OUT}}{\Delta I_{OUT}}$	Load Regulation	$10mA \leq I_{OUT} \leq I_{MAX}$, (See Note 2) $V_O \leq 5V$ $V_O \geq 5V$		5	25	5	25		mV %
			●	0.1	0.5	0.1	0.5		
	Thermal Regulation	$T_A = 25^\circ C$, 20msec Pulse	●	0.002	0.02	0.04	0.07		%/W
			●						
	Ripple Rejection	$V_O = 10V$, $f = 120Hz$ $C_{ADJ} = 0$		65		65			dB
		$C_{ADJ} = 10\mu F$	●	66	80	66	80		dB
I_{ADJ}	Adjust Pin Current			50	100	50	100		μA
ΔI_{ADJ}	Adjust Pin Current Change	$10mA \leq I_{OUT} \leq I_{MAX}$ $2.5V \leq (V_{IN} - V_{OUT}) \leq 40V$	●	0.2	5	0.2	5		μA
I_{min}	Minimum Load Current	$(V_{IN} - V_{OUT}) = 40V$	●	3.5	10	3.5	10		mA
	Current Limit	$(V_{IN} - V_{OUT}) \leq 15V$ K and T Package H Package	●	1.5	2.2	1.5	2.2		A
			●	0.5	0.8	0.5	0.8		A
	Temperature Stability	$(V_{IN} - V_{OUT}) = 40V$, $T_I = 25^\circ C$ K and T Package H Package		0.15	0.4	0.15	0.4		A
				0.075	0.2	0.075	0.2		A
$\frac{\Delta V_{OUT}}{\Delta Temp}$	Long Term Stability	$0^\circ C \leq T_I \leq 125^\circ C$		1	2	1			%
$\frac{\Delta V_{OUT}}{\Delta Time}$	RMS Output Noise (% of V_{OUT})	$T_A = 125^\circ C$		0.3	1	0.3	1		%
e_n	Thermal Resistance Junction to Case	$T_A = 25^\circ C$, $10Hz \leq f \leq 10kHz$		0.001		0.001			%
θ_{JC}	Thermal Resistance Junction to Case	H Package		12	15	12	15		$^\circ C/W$
		K Package		2.3	3	2.3	3		$^\circ C/W$
		T Package		4	5	4			$^\circ C/W$

4

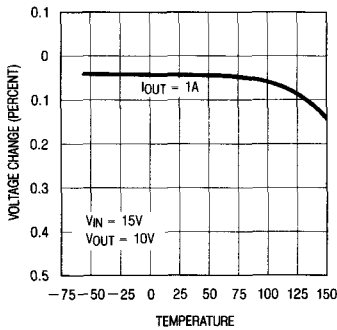
The ● denotes the specifications which apply over the full operating temperature range.

Note 1: Unless otherwise specified, these specifications apply for $V_{IN} - V_{OUT} = 5V$; and $I_{OUT} = 0.1A$ for the TO-39 and $I_{OUT} = 0.5A$ for the TO-3 and TO-220 packages. Although power dissipation is internally limited, these specifications are applicable for power dissipations of 2W for the TO-39, and 20W for the TO-3 and TO-220. I_{MAX} is 1.5A for the TO-3 and TO-220 packages and 0.5A for the TO-39.

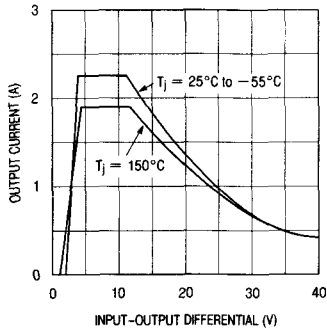
Note 2: Regulation is measured at constant junction temperature, using pulse testing with a low duty cycle. Changes in output voltage due to heating effects are covered under the specification for thermal regulation. Load regulation is measured on the output pin at a point $1/8"$ below the base of the K and H package and at the junction of the wide and narrow portion of the lead on the T package.

TYPICAL PERFORMANCE CHARACTERISTICS

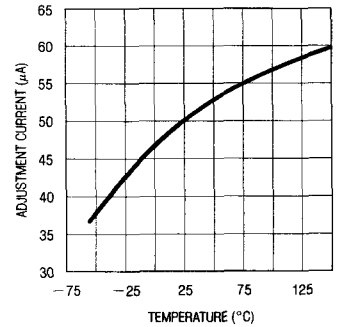
Load Regulation



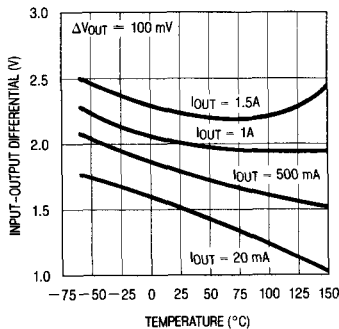
Current Limit (TO-3 and TO-220 Package)



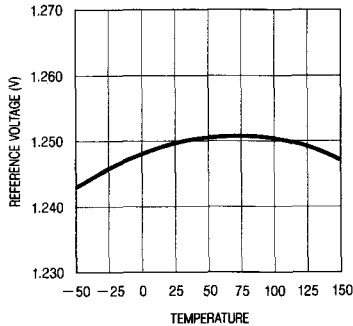
Adjustment Current



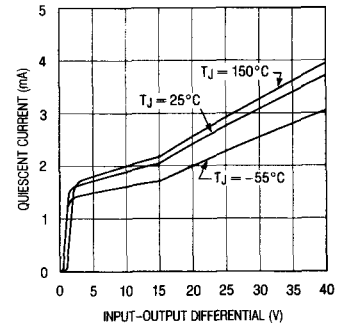
Dropout Voltage



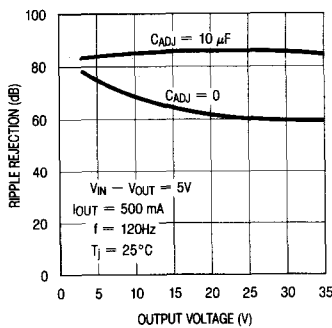
Temperature Stability



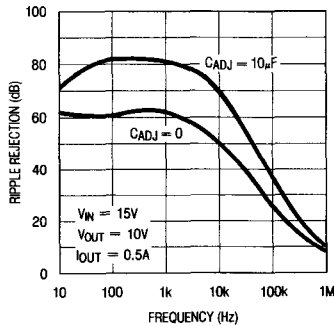
Minimum Operating Current



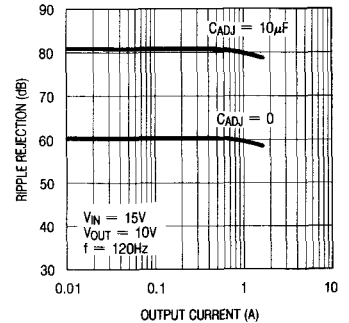
Ripple Rejection



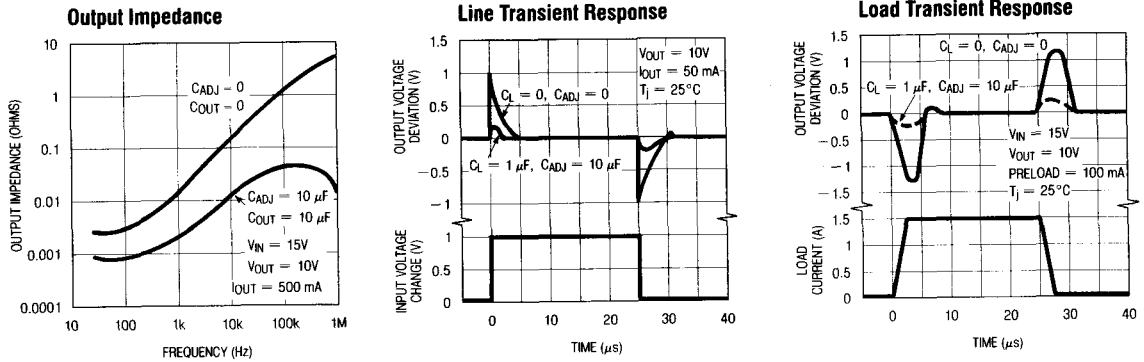
Ripple Rejection (dB)



Ripple Rejection



TYPICAL PERFORMANCE CHARACTERISTICS



APPLICATIONS INFORMATION

General: The LT117A develops a 1.25V reference voltage between the output and the adjustable terminal (see Figure 1). By placing a resistor, R1, between these two terminals, a constant current is caused to flow through R1 and down through R2 to set the overall output voltage. Normally this current is the specified minimum load current of 5mA or 10mA.

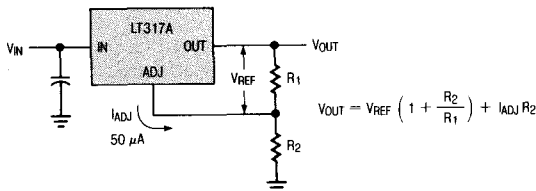


Figure 1

Because I_{ADJ} is very small and constant when compared with the current through R1, it represents a small error and can usually be ignored.

It is easily seen from the above equation, that even if the resistors were of exact value, the accuracy of the output is limited by the accuracy of V_{REF} . Earlier adjustable regulators had a reference tolerance of $\pm 4\%$. This tolerance is dangerously close to the $\pm 5\%$ supply tolerance required in many logic and analog systems. Further, many 1% resistors can drift $0.01\%/^\circ C$ adding another 1% to the output voltage tolerance.

For example, using 2% resistors and $\pm 4\%$ tolerance for V_{REF} , calculations will show that the expected range of a 5V regulator design would be $4.66V \leq V_{OUT} \leq 5.36V$ or approximately $\pm 7\%$. If the same example were used for a 15V regulator, the expected tolerance would be $\pm 8\%$. With these results most applications require some method of trimming, usually a trim pot. This solution is both expensive and not conducive to volume production.

One of the enhancements of Linear Technology's adjustable regulators over existing devices is tightened initial tolerance. This allows relatively inexpensive 1% or 2% film resistors to be used for R1 and R2 while setting output voltage within an acceptable tolerance range.

With a guaranteed 1% reference, a 5V power supply design, using $\pm 2\%$ resistors, would have a worst case manufacturing tolerance of $\pm 4\%$. If 1% resistors were used, the tolerance would drop to $\pm 2.5\%$. A plot of the worst case output voltage tolerance as a function of resistor tolerance is shown on the front page.

LT117A/LT317A LM117/LM317

For convenience, a table of standard 1% resistor values is shown below.

Table of ½% and 1% Standard Resistance Values

1.00	1.47	2.15	3.16	4.64	6.81
1.02	1.50	2.21	3.24	4.75	6.98
1.05	1.54	2.26	3.32	4.87	7.15
1.07	1.58	2.32	3.40	4.99	7.32
1.10	1.62	2.37	3.48	5.11	7.50
1.13	1.65	2.43	3.57	5.23	7.68
1.15	1.69	2.49	3.65	5.36	7.87
1.18	1.74	2.55	3.74	5.49	8.06
1.21	1.78	2.61	3.83	5.62	8.25
1.24	1.82	2.67	3.92	5.76	8.45
1.27	1.87	2.74	4.02	5.90	8.66
1.30	1.91	2.80	4.12	6.04	8.87
1.33	1.96	2.87	4.22	6.19	9.09
1.37	2.00	2.94	4.32	6.34	9.31
1.40	2.05	3.01	4.42	6.49	9.53
1.43	2.10	3.09	4.53	6.65	9.76

Standard Resistance Values are obtained from the Decade Table by multiplying by multiples of 10. As an example, 1.21 can represent 1.21Ω, 12.1Ω, 121Ω, 1.21KΩ etc.

Bypass Capacitors: Input bypassing using a 1μF tantalum or 25μF electrolytic is recommended when the input filter capacitors are more than 5 inches from the device. Improved ripple rejection (80 dB) can be accomplished by adding a 10μF capacitor from the adjust pin to ground. Increasing the size of the capacitor to 20μF will help ripple rejection at low output voltage since the reactance of this capacitor should be small compared to the voltage setting resistor, R2. For improved AC transient response and to prevent the possibility of oscillation due to unknown reactive load, a 1μF capacitor is also recommended at the output. Because of their low impedance at high frequencies, the best type of capacitor to use is solid tantalum.

Protection Diodes: The LT117A/317A do not require a protection diode from the adjustment terminal to the output (see Figure 2). Improved internal circuitry

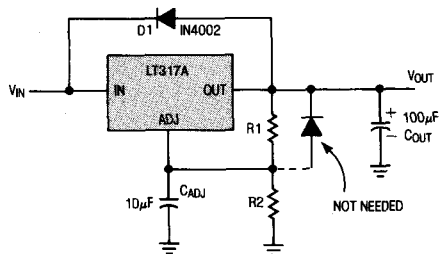


Figure 2

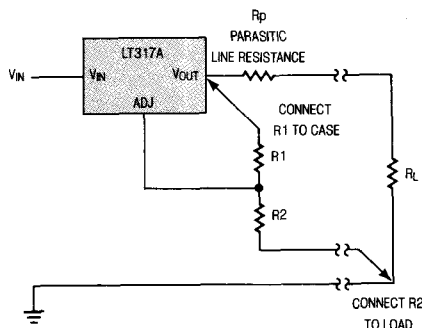
eliminates the need for this diode when the adjustment pin is bypassed with a capacitor to improve ripple rejection.

If a very large output capacitor is used, such as a 100μF shown in Figure 2, the regulator could be damaged or destroyed if the input is accidentally shorted to ground or crowbarred. This is due to the output capacitor discharging into the output terminal of the regulator. To prevent damage a diode D1 is recommended to safely discharge the capacitor.

Load Regulation: Because the LT117A is a three-terminal device, it is not possible to provide true remote load sensing. Load regulation will be limited by the resistance of the wire connecting the regulator to the load. For the data sheet specification, regulation is measured at the bottom of the package. Negative side sensing is a true Kelvin connection, with the bottom of the output divider returned to the negative side of the load. Although it may not be immediately obvious, best load regulation is obtained when the top of the divider is connected *directly* to the case *not to the load*. This is illustrated in Figure 3. If R1 were connected to the load, the effective resistance between the regulator and the load would be

$$R_p \times \left(\frac{R_2 + R_1}{R_1} \right), R_p = \text{Parasitic Line Resistance.}$$

Connected as shown, R_p is not multiplied by the divider ratio. R_p is about 0.004Ω per foot using 16 gauge wire. This translates to 4mV/ft at 1A load current, so it important to keep the positive lead between regulator and load as short as possible.

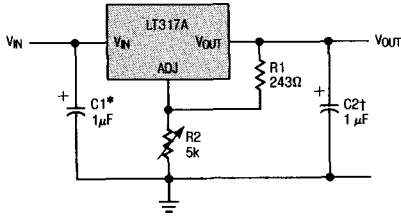


Connections for Best Load Regulation

Figure 3

TYPICAL APPLICATIONS

1.2V-25V Adjustable Regulator

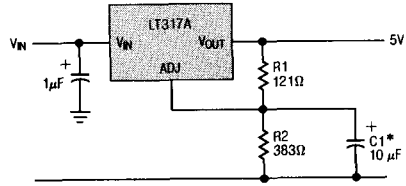


† Optional — improves transient response

* Needed if device is far from filter capacitors

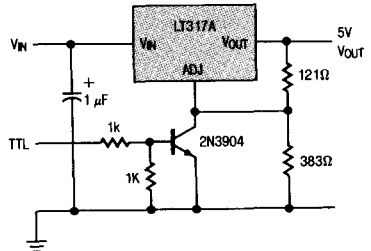
$$V_{OUT} = 1.25V \left(1 + \frac{R2}{R1} \right)$$

Improving Ripple Rejection

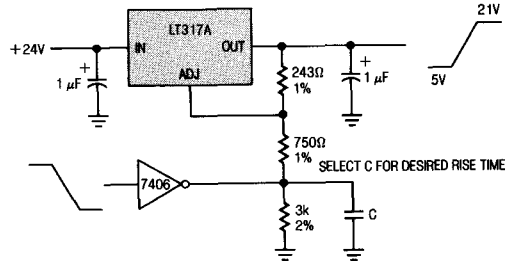


* C1 IMPROVES RIPPLE REJECTION
X_C SHOULD BE SMALL
COMPARED TO R2

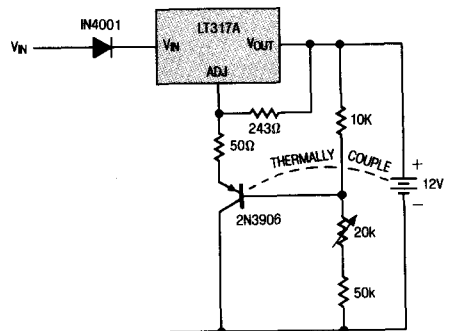
5V Regulator with Shut Down



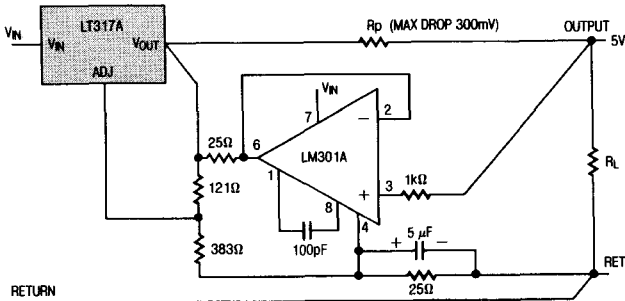
21V Programming Supply for UV PROM/EEROM



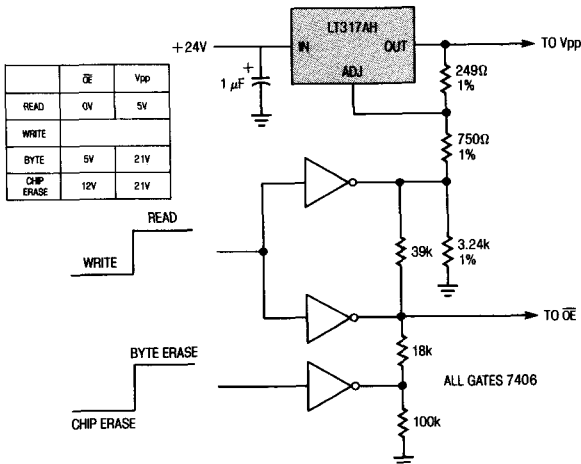
Temperature Compensated Lead Acid Battery Charger



Remote Sensing

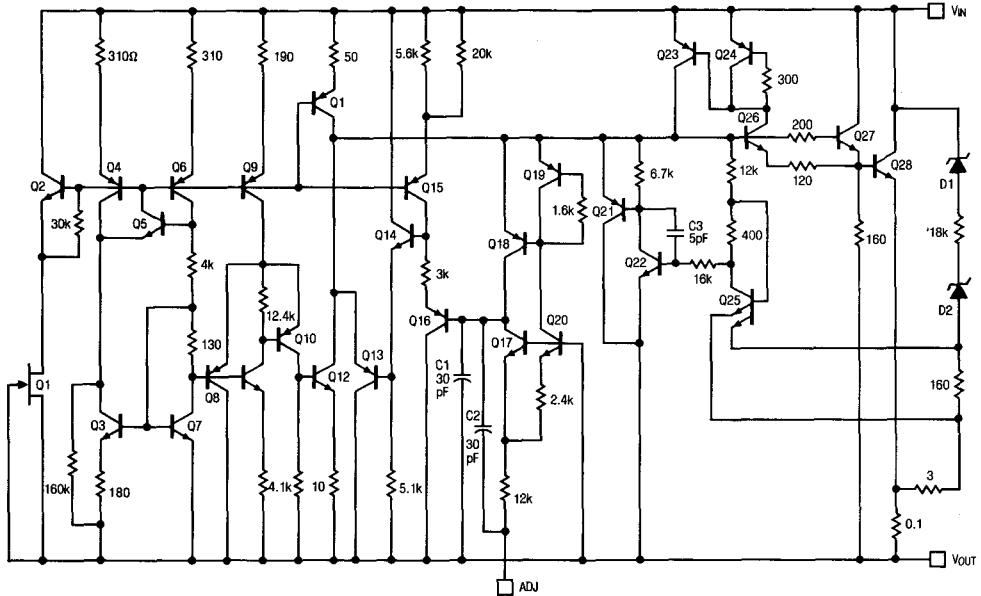


2816 EEPROM Supply Programmer for Read/Write Control



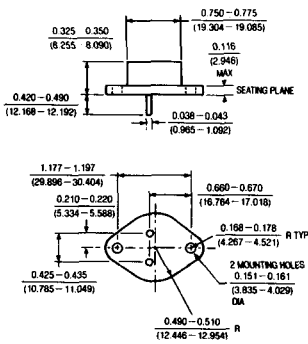
SCHEMATIC DIAGRAM

LT117A/LT317A

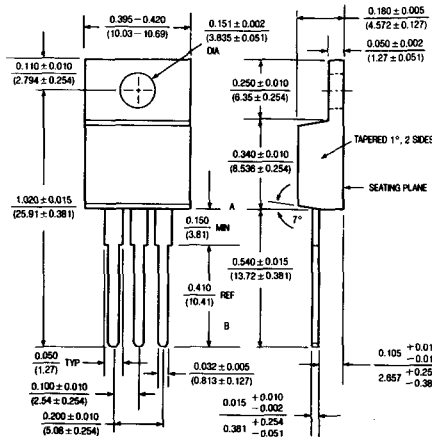


PACKAGE DESCRIPTION

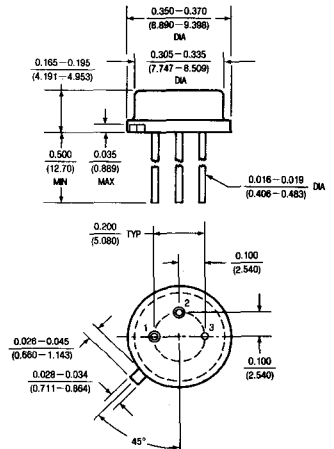
K Package TO-3 STEEL Metal Can



T Package TO-220 Plastic



H Package 3-Lead Metal Can



	T _j max.	θ _{ja}	θ _{jc}
117A 117	150°C	35°C/W	3°C/W
317A 317	125°C	35°C/W	3°C/W

	T _j max.	θ _{ja}	θ _{jc}
317A 317	125°C	50°C/W	5°C/W

	T _j max.	θ _{ja}	θ _{jc}
117A 117	150°C	150°C/W	15°C/W
317A 317	125°C	150°C/W	15°C/W

High Voltage Positive Adjustable Regulators

FEATURES

- 60V Operation
- *Guaranteed* 1% Output Voltage Tolerance
- *Guaranteed* max. 0.01%/V Line Regulation
- *Guaranteed* max. 0.3% Load Regulation
- Min. 1.5A Output Current
- 100% Burn-in in Thermal Overload

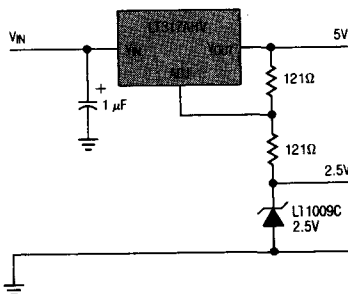
APPLICATIONS

- Wide Range Power Supplies
- Constant Current Supplies
- Voltage Programmable Supplies

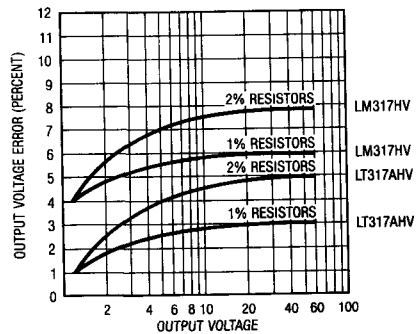
DESCRIPTION

The LT117AHV Series are 3-terminal positive adjustable voltage regulators which offer improved performance over earlier devices. A major feature of the LT117AHV is the output voltage tolerance is guaranteed at a maximum of $\pm 1\%$, allowing an overall power supply tolerance to be better than 3% using inexpensive 1% resistors. Line and load regulation performance has been improved as well. Additionally, the LT117AHV reference voltage is guaranteed not to exceed 2% when operating over the full load, line and power dissipation conditions. The LT117AHV adjustable regulators offer an improved solution for all positive voltage regulator requirements with load currents up to 1.5 amps. For performance curves and applications circuits see the LT117A series data sheet.

Regulator with Reference



Output Voltage Error

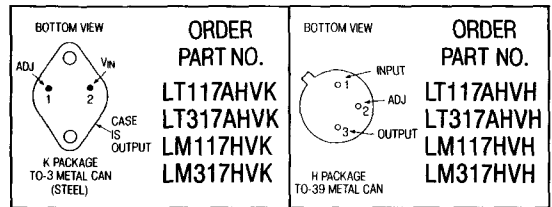


LT117AHV/LT317AHV LM117HV/LM317HV

ABSOLUTE MAXIMUM RATINGS

Power Dissipation	Internally Limited
Input to Output Voltage Differential	60V
Operating Junction Temperature Range	
LT117AHV/LM117HV	-55°C to 150°C
LT317AHV/LM317HV	0°C to 125°C
Storage Temperature Range	
LT117AHV/LM117HV	-65°C to 150°C
LT317AHV/LM317HV	-65°C to 150°C
Lead Temperature (Soldering, 10 sec.)	300°C

PACKAGE/ORDER INFORMATION



PRECONDITIONING:

100% THERMAL LIMIT BURN-IN

ELECTRICAL CHARACTERISTICS (See Note 1) LT117AHV/LM117HV

SYMBOL	PARAMETER	CONDITIONS	LT117AHV			LM117HV			UNITS	
			MIN	TYP	MAX	MIN	TYP	MAX		
V_{REF}	Reference Voltage	$I_{OUT} = 10mA$, $T_J = 25^\circ C$	1.238	1.250	1.262				V	
		$3V \leq (V_{IN} - V_{OUT}) \leq 60V$ $10mA \leq I_{OUT} \leq I_{max}$, $P \leq P_{max}$	●	1.225	1.250	1.270	1.20	1.25	1.30	V
$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	Line Regulation	$3V \leq (V_{IN} - V_{OUT}) \leq 60V$ (See Note 2)		0.005	0.01		0.01	0.02		%/V
			●	0.01	0.02		0.02	0.05		%/V
$\frac{\Delta V_{OUT}}{\Delta I_{OUT}}$	Load Regulation	$10mA \leq I_{OUT} \leq I_{max}$, (See Note 2) $V_{OUT} \leq 5V$ $V_{OUT} \geq 5V$		5	15		5	15		mV %
		$V_{OUT} \leq 5V$ $V_{OUT} \geq 5V$	●	20	50		20	50		mV %
			●	0.3	1		0.3	1		
	Thermal Regulation	$T_A = 25^\circ C$, 20msec Pulse		0.002	0.02		0.03	0.07		%/W
	Ripple Rejection	$V_{OUT} = 10V$, $f = 120Hz$ $C_{ADJ} = 0$	●	65			65			dB
		$C_{ADJ} = 10\mu F$	●	66	80		66	80		dB
I_{ADJ}	Adjust Pin Current		●	50	100		50	100		μA
ΔI_{ADJ}	Adjust Pin Current Change	$10mA \leq I_{OUT} \leq I_{max}$ $2.5V \leq (V_{IN} - V_{OUT}) \leq 60V$	●	0.2	5		0.2	5		μA
I_{min}	Minimum Load Current	$(V_{IN} - V_{OUT}) = 60V$	●	3.5	7		3.5	7		mA
	Current Limit	$(V_{IN} - V_{OUT}) \leq 15V$ K Package H Package	●	1.5	2.2		1.5	2.2		A A
		$(V_{IN} - V_{OUT}) = 60V$, $T_J = 25^\circ C$ K Package H Package		0.1			0.1			A A
				0.03			0.03			
$\frac{\Delta V_{OUT}}{\Delta Temp}$	Temperature Stability	$-55^\circ C \leq T_J \leq +150^\circ C$		1	2		1			%
$\frac{\Delta V_{OUT}}{\Delta Time}$	Long Term Stability	$T_A = 125^\circ C$		0.3	1		0.3	1		%
e_n	RMS Output Noise (% of V_{OUT})	$T_A = 25^\circ C$, $10Hz \leq f \leq 10kHz$		0.001			0.001			%
θ_{jc}	Thermal Resistance Junction to Case	H Package K Package		12	15		12	15		$^\circ C/W$ $^\circ C/W$
				2.3	3		2.3	3		

ELECTRICAL CHARACTERISTICS (See Note 1) LT317AHV/LM317HV

SYMBOL	PARAMETER	CONDITIONS	LT317AHV			LM317HV			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{REF}	Reference Voltage	$I_{OUT} = 10mA$, $T_J = 25^\circ C$	1.238	1.250	1.262				V
		$3V < (V_{IN} - V_O) < 60V$ $10mA \leq I_{OUT} \leq I_{MAX}$, $P < P_{MAX}$	● 1.225	1.250	1.270	1.20	1.25	1.30	V
$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	Line Regulation	$3V < (V_{IN} - V_{OUT}) < 60V$ (See Note 2)		0.005	0.01	0.01	0.04	%/V	
			●	0.01	0.02	0.02	0.07	%/V	
$\frac{\Delta V_{OUT}}{\Delta I_{OUT}}$	Load Regulation	$10mA \leq I_{OUT} \leq I_{MAX}$. (See Note 2) $V_O \leq 5V$ $V_O \geq 5V$		5	25	5	25	mV	
			●	0.1	0.5	0.1	0.5	%	
		$V_O \leq 5V$ $V_O \geq 5V$	●	20	50	20	70	mV	
			●	0.3	1	0.3	1.5	%	
	Thermal Regulation	$T_A = 25^\circ C$, 20msec Pulse		0.002	0.02	0.04	0.07	%/W	
	Ripple Rejection	$V_O = 10V$, $f = 120Hz$ $C_{ADJ} = 0$	●	65		65		dB	
		$C_{ADJ} = 10\mu F$	●	66	80	66	80	dB	
I_{ADJ}	Adjust Pin Current		●	50	100	50	100	μA	
ΔI_{ADJ}	Adjust Pin Current Change	$10mA \leq I_{OUT} \leq I_{MAX}$ $2.5V \leq (V_{IN} - V_{OUT}) \leq 60V$	●	0.2	5	0.2	5	μA	
I_{min}	Minimum Load Current	$(V_{IN} - V_{OUT}) = 60V$	●	3.5	12	3.5	12	mA	
	Current Limit	$(V_{IN} - V_{OUT}) \leq 15V$ K Package H Package	●	1.5	2.2	1.5	2.2	A	
			●	0.5	0.8	0.5	0.8	A	
		$(V_{IN} - V_{OUT}) = 60V$, $T_J = 25^\circ C$ K Package H Package		0.1		0.1		A	
				0.03		0.03		A	
$\frac{\Delta V_{OUT}}{\Delta Temp}$	Temperature Stability	$0^\circ C \leq T_J \leq 125^\circ C$		1	2	1		%	
$\frac{\Delta V_{OUT}}{\Delta Time}$	Long Term Stability	$T_A = 125^\circ C$		0.3	1	0.3	1	%	
e_n	RMS Output Noise (% of V_{OUT})	$T_A = 25^\circ C$, $10Hz \leq f \leq 10kHz$		0.001		0.001		%	
θ_{jc}	Thermal Resistance Junction to Case	H Package		12	15	12	15	$^\circ C/W$	
		K Package		2.3	3	2.3	3	$^\circ C/W$	

4

The ● denotes the specifications which apply over the full operating temperature range.

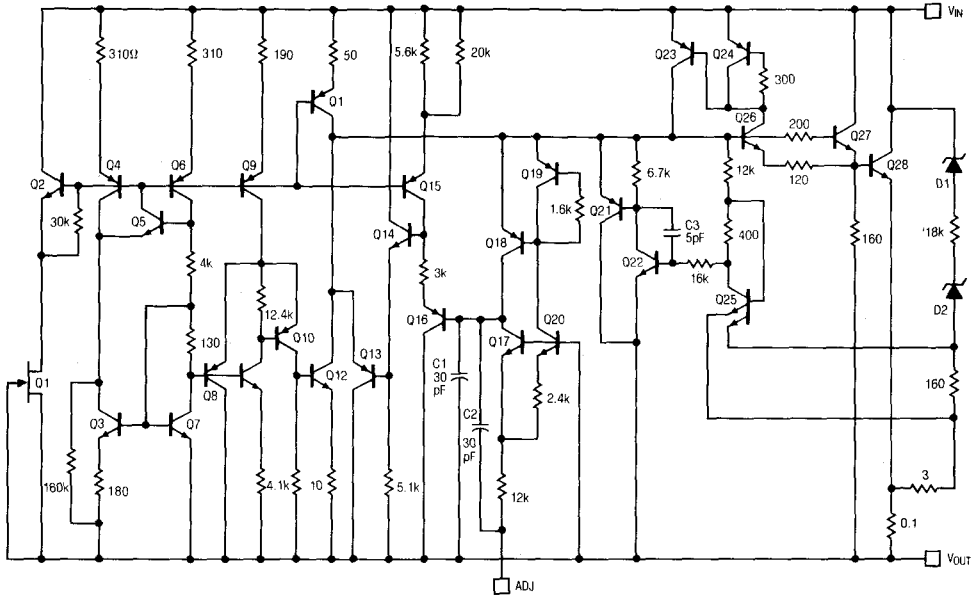
The shaded electrical specifications indicate those parameters which have been improved or guaranteed test limits provided for the first time.

Note 1: Unless otherwise specified, these specifications apply for $(V_{IN} - V_{OUT}) = 5V$; and $I_{OUT} = 0.1A$ for the TO-39 and $I_{OUT} = 0.5A$ for the TO-3 package. Although power dissipation is internally limited, these specifications are applicable for power dissipations of 2W for the TO-39, and 20W for the TO-3. I_{MAX} is 1.5A for the TO-3 package and 0.5A for the TO-39.

Note 2: Regulation is measured at constant junction temperature, using pulse testing with a low duty cycle. Changes in output voltage due to heating effects are covered under the specification for thermal regulation.

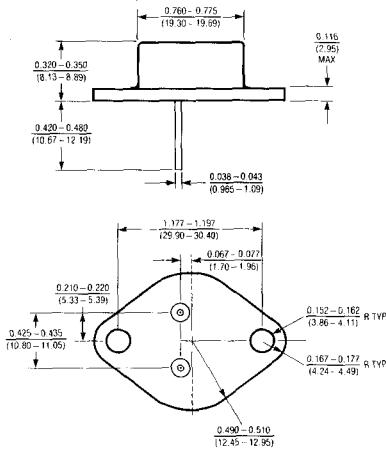
LT117AHV/LT317AHV
LM117HV/LM317HV

SCHEMATIC DIAGRAM



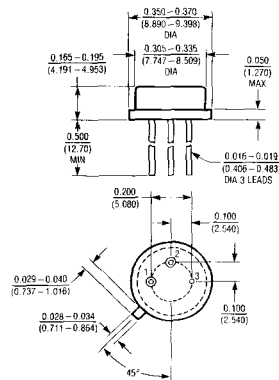
PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

K Package TO-3 STEEL Metal Can



	T _J max.	θ _{JA}	θ _{JC}
117AHV 117HV	150°C	35°C/W	3°C/W
317AHV 317HV	125°C	35°C/W	3°C/W

H Package 3-Lead Metal Can



	T _J max.	θ _{JA}	θ _{JC}
117AHV 117HV	150°C	150°C/W	15°C/W
317AHV 317HV	125°C	150°C/W	15°C/W

FEATURES

- *Guaranteed* 1% Initial Tolerance of Output Voltage
- 3 Amp Output Current
- 30 Watt
- Full Internal Overload Protection
- 100% Burn-in in Thermal Limit

APPLICATIONS

- Local 5V Regulators
- On Card Regulation
- Lab Supplies
- Instrumentation Supplies

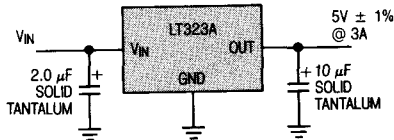
DESCRIPTION

The LT123A/LT323A is an improved version of the popular LM123/LM323 5 Volt, 3 Amp Regulator. These new devices offer maximum initial output voltage tolerance of 1% and maintain a maximum tolerance of 3% over worst case operating conditions. Line and load regulation are also improved by a factor of 2. These tightened specifications ease design and application problems since safety margins are improved. Also, error budgets in other parts of the system can be expanded, and output voltages at the end of long supply runs can be more accurately maintained.

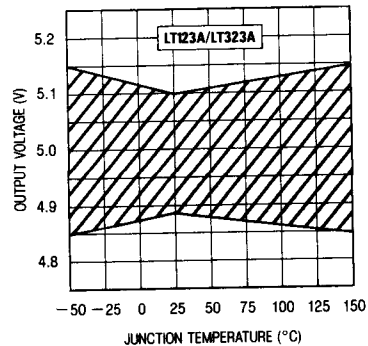
The LT123A/LT323A incorporates Linear Technology's advanced design, process and test techniques for improved quality and reliability over similar device types. Specifically, all devices are burned in by shorting the output, thereby forcing the regulator into its current limit and eventually, thermal limit. This ensures that all device protection features are functional. A graph of the worst case output voltage, taking into account temperature, load and line variations, and power dissipation is shown below. For higher output current requirements, see the LT1003, 5V, 5A regulator data sheet.

4

Precision 5 Volt Regulator



Worst Case Output Voltage

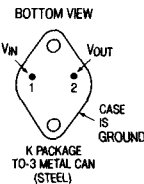
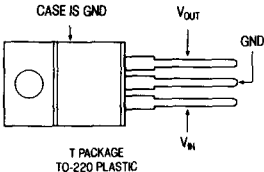


LT123A/LT323A LM123/LM323

ABSOLUTE MAXIMUM RATINGS

Input Voltage	20 Volts
Power Dissipation	Internally Limited
Operating Junction Temperature Range	
LT123A/LM123	-55°C to 150°C
LT323A/LM323	0°C to 125°C
Storage Temperature Range	
LT123A/LM123	-65°C to 150°C
LT323A/LM323	-65°C to 150°C
Lead Temperature (Soldering, 10 sec.)	300°C

PACKAGE/ORDER INFORMATION

 <p>BOTTOM VIEW</p> <p>V_{IN} V_{OUT}</p> <p>1 2</p> <p>CASE IS GROUND</p> <p>K PACKAGE TO-3 METAL CAN (STEEL)</p>	ORDER PART NO.
	LT123AK LT323AK LM123K LM323K
 <p>CASE IS GND</p> <p>V_{OUT} GND</p> <p>V_{IN}</p> <p>T PACKAGE TO-220 PLASTIC</p>	LT323AT LM323T

PRECONDITIONING:

Thermal limit burn-in for all devices.

ELECTRICAL CHARACTERISTICS (See Note 1)

SYMBOL	PARAMETER	CONDITIONS	LT123A			LM123			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V _{OUT}	Output Voltage	T _J = 25°C, V _{IN} = 7.5V, I _{OUT} = 0	4.95	5.0	5.05	4.7	5.0	5.3	V
		7.5V ≤ V _{IN} ≤ 15V, T _{MIN} ≤ T _J ≤ T _{MAX} , 0 ≤ I _{OUT} ≤ 3A, P ≤ 30W	● 4.85	5.0	5.15	4.6	5.0	5.4	V
$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	Line Regulation	T _J = 25°C, 7.5V ≤ V _{IN} ≤ 15V (See Note 1)		5	10		5	25	mV
$\frac{\Delta V_{OUT}}{\Delta I_{OUT}}$	Load Regulation	T _J = 25°C, V _{IN} = 7.5V, 0 ≤ I _{OUT} ≤ 3A (See Note 1)		25	50		25	100	mV
I _Q	Quiescent Current	7.5V ≤ V _{IN} ≤ 15V, 0 ≤ I _{OUT} ≤ 3A	●	12	20		12	20	mA
e _n	Output Noise Voltage	T _J = 25°C, 10Hz ≤ f ≤ 100kHz		40			40		μV _{rms}
I _{SC}	Short Circuit Current Limit	T _J = 25°C, V _{IN} = 15V, V _{IN} = 7.5V		3	4.5		3	4.5	A
				4	6		4	5	A
	Long Term Stability of Output Voltage	(See Note 3)			35			35	mV
θ _{JC}	Thermal Resistance Junction to Case	(See Note 3) K Package		1.8	2.5		1.8		°C/W

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: Load and line regulation are tested with pulsed low duty cycle techniques where pulse width ≤ 1msec and duty cycle ≤ 5%.

Note 2: T_{min} = -55°C for the LT123A/LM123 and 0°C for LT323A/LM323. T_{max} = 150°C for LT123A/LM123 and 125°C for LT323A/LM323.

Note 3: Guaranteed, but not tested.

ELECTRICAL CHARACTERISTICS (See Note 1)

SYMBOL	PARAMETER	CONDITIONS	LT323A			LM323			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OUT}	Output Voltage	$T_J = 25^\circ\text{C}, V_{IN} = 7.5\text{V}, I_{OUT} = 0$	4.95	5.0	5.05	4.8	5.0	5.2	V
		$7.5\text{V} \leq V_{IN} \leq 15\text{V}, T_{MIN} \leq T_J \leq T_{MAX}$ $0 \leq I_{OUT} \leq 3\text{A}, P \leq 30\text{W}$ (Note 2)	4.85	5.0	5.15	4.75	5.0	5.25	V
$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	Line Regulation	$T_J = 25^\circ\text{C}, 7.5\text{V} \leq V_{IN} \leq 15\text{V}$ (See Note 1)		5	10		5	25	mV
$\frac{\Delta V_{OUT}}{\Delta I_{OUT}}$	Load Regulation	$T_J = 25^\circ\text{C}, V_{IN} = 7.5\text{V}$ $0 \leq I_{OUT} \leq 3\text{A}$ (See Note 1)		25	50		25	100	mV
I_Q	Quiescent Current	$7.5\text{V} \leq V_{IN} \leq 15\text{V}, 0 \leq I_{OUT} \leq 3\text{A}$		12	20		12	20	mA
e_n	Output Noise Voltage	$T_J = 25^\circ\text{C}, 10\text{Hz} \leq f \leq 100\text{kHz}$		40			40		μV_{rms}
I_{SC}	Short Circuit Current Limit	$T_J = 25^\circ\text{C}, V_{IN} = 15\text{V}$		3	4.5		3	4.5	A
		$V_{IN} = 7.5\text{V}$ (See Note 4)		4	6		4	5	A
	Long Term Stability of Output Voltage	(See Note 3)			35			35	mV
θ_{JC}	Thermal Resistance Junction to Case	(See Note 3) K Package T Package		1.8 2.5	2.5 4.0		1.8 3.0		$^\circ\text{C}/\text{W}$ $^\circ\text{C}/\text{W}$

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: Load and line regulation are tested with pulsed low duty cycle techniques where pulse width $\leq 1\text{msec}$ and duty cycle $\leq 5\%$.

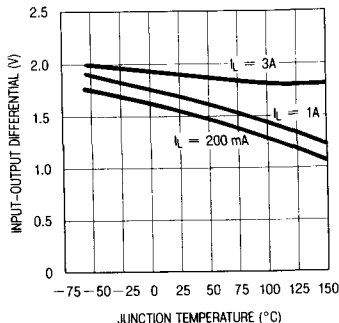
Note 2: $T_{min} = -55^\circ\text{C}$ for the LT123A/LM123 and 0°C for LT323A/LM323. $T_{max} = +150^\circ\text{C}$ for LT123A/LM123 and $+125^\circ\text{C}$ for LT323A/LM323.

Note 3: Guaranteed, but not tested.

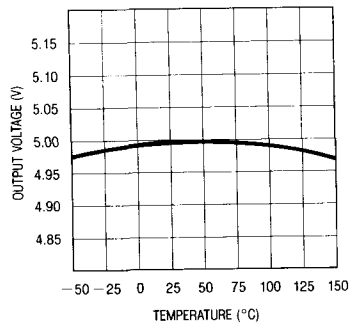
Note 4: I_{SC} at $V_{IN} = 7.5\text{V}$ is 6A max for LM323T.

TYPICAL PERFORMANCE CHARACTERISTICS

Dropout Voltage

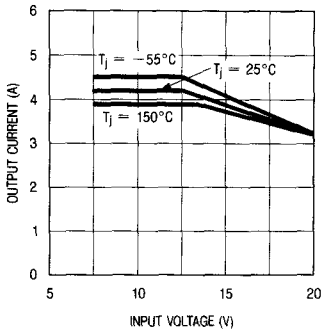


Output Voltage Temperature Drift

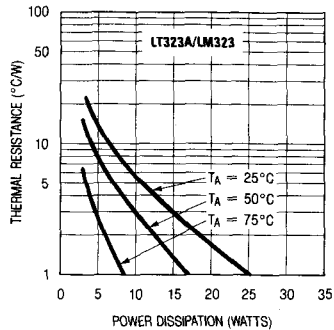


TYPICAL PERFORMANCE CHARACTERISTICS

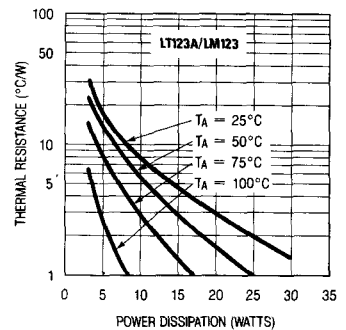
Peak Available Output Current



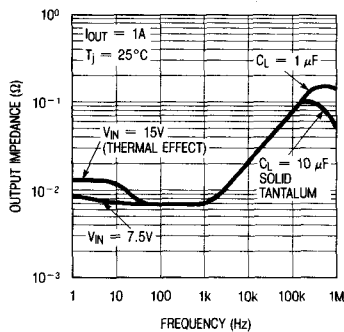
Suggested Heat Sink Thermal Resistance



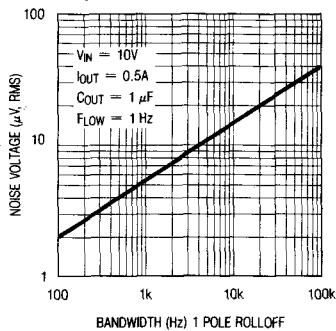
Suggested Heat Sink Thermal Resistance



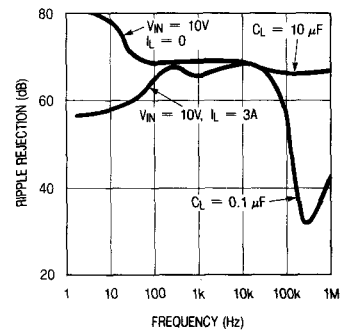
Output Impedance



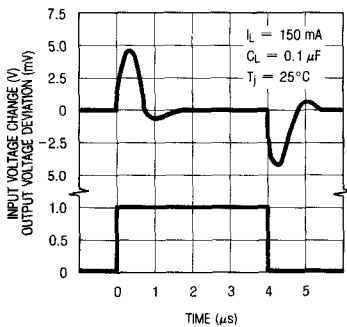
Output Noise Voltage



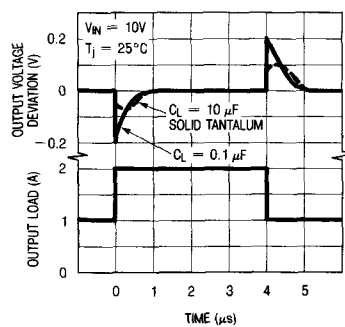
Ripple Rejection



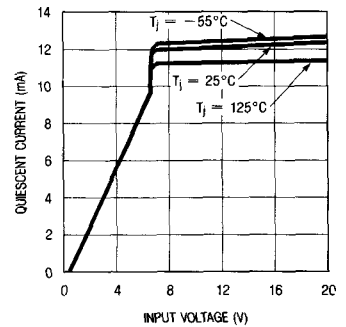
Line Transient Response



Load Transient Response



Quiescent Current

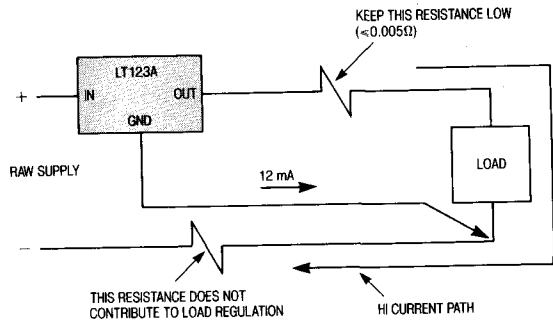


APPLICATIONS INFORMATION

Bypass Capacitors: The LT123A does not require an output capacitor for resistive loads. For almost all applications, however, a $1\mu\text{F}$ or larger solid tantalum capacitor should be used at the output within 2" of the regulator to improve the output impedance at high frequencies. For applications where very low high frequency impedance is required, a $10\mu\text{F}$ solid tantalum output capacitor is recommended. Total output capacitance either local or distributed may be increased without limit.

A $2\mu\text{F}$ or larger solid tantalum capacitor or a $25\mu\text{F}$ aluminum capacitor, must be used at the input if the regulator is more than 4" away from the large rectifier capacitor.

Avoiding Ground Loops: For best regulation, the ground pin of the LT123A should be tied directly to the load point as shown. This prevents excess drop in load voltage caused by load current flowing through the ground return lead. This is essentially a Kelvin connection for the low side of the regulator. A Kelvin connection cannot be made for the high output of regulator because only three pins are available on the package. Therefore, every attempt should be made to minimize the resistance between the output pin of the regulator and the load. #18 gauge hookup wire has a resistance of 0.006 ohms per foot. This translates to 0.36% change in load voltage at full load current. The LT123A is specified at 1% maximum load regulation, so one foot of wire represents a significant loss of regulation. If connectors are used, careful consideration must be given to contact resistance, especially if the connector is subjected to nasty ambients, vibration, or multiple insertions.



Raw Supply: Transformer, diode, and capacitor selection for the raw supply to the LT123A is very important because of the conflicting requirements for reliability, efficiency, and resistance to "brown-out" conditions. High secondary voltage on the transformer will cause unnecessarily high power dissipation in the regulator. Too low a secondary voltage will cause the regulator output to drop out of regulation with only a small reduction in AC mains voltage. The following formula gives a good starting point for transformer selection. This formula assumes a center tapped transformer, using two rectifier diodes.

where:

- $V_{\text{OUT}} = 5\text{V}$
- V_{DO} = Minimum input-output differential of the regulator
- V_{RECT} = Rectifier forward drop at $3I_{\text{OUT}}$
- V_{RIP} = $\frac{1}{2}$ p-p capacitor ripple voltage
- $$\approx \frac{(5.3 \times 10^{-3})(I_{\text{OUT}})}{2C}$$
- V_{NOM} = Rated line voltage for the transformer (RMS)
- V_{LOW} = Lowest expected line voltage (RMS)
- I_{OUT} = DC output current

*1.1 is a nominal load regulation factor for the transformer

APPLICATIONS INFORMATION

Example: $I_{OUT} = 2.5A$, $V_{OUT} = 5V$
Assume: $V_{DO} = 2.5V$, $V_{RECT} = 1.1V$, $C = 8,000\mu F$
 $V_{NOM} = 115V$, $V_{LOW} = 0.88V$

$$V_{RIP} = \frac{(5.3 \times 10^{-3})(2.5)}{2(8 \times 10^{-3})} = 0.83V$$

$$V_{RMS} = \left(\frac{5 + 2.5 + 1.1 + 0.83}{\sqrt{2}} \right) \left(\frac{115}{05} \right) (1.1)$$

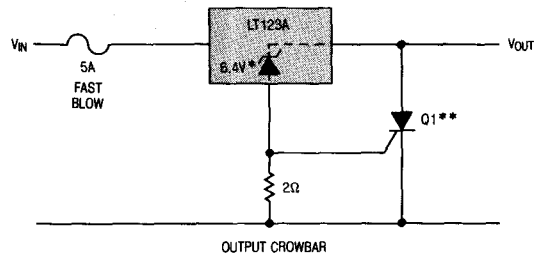
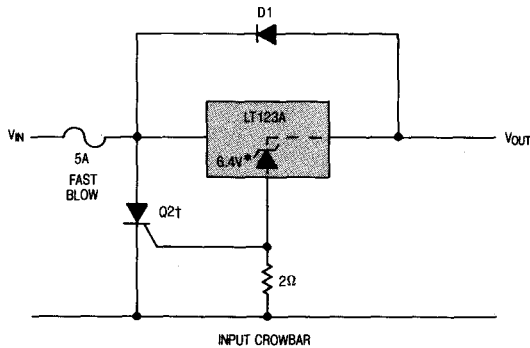
$$= 8.03 V_{RMS}$$

$$V_{RMS} = \left(\frac{V_{OUT} + V_{DO} + V_{RECT} + V_{RIP}}{\sqrt{2}} \right) \left(\frac{V_{NOM}}{V_{LOW}} \right) (1.1^*)$$

$$I_{RMS} = (I_{OUT}) (1.2)$$

The filter capacitor should be at *least* $2000\mu F$ per amp of load current to minimize capacitor heating and ripple voltage. The diodes should be rated at 5–6 amps even though their average current is only 1.5A at full rated load current. The reason for this is that although the *average* current is 1.5A, the RMS current is typically twice this value. In addition, the diode must withstand very high surge currents during power turn-on. This surge can be 10–20 times the DC rating of the supply, depending on capacitor size and wiring resistance and inductance.

TYPICAL APPLICATIONS



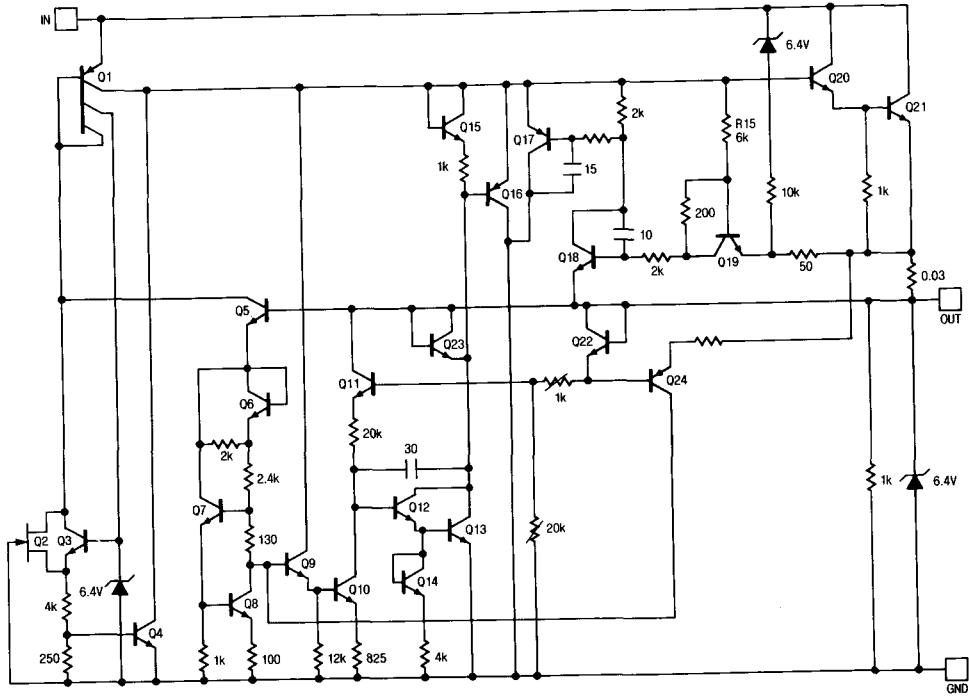
† Q2 AND D1 MUST WITHSTAND LARGE SURGE CURRENTS UNTIL THE 5A FUSE BLOWS. PEAK SURGE CURRENT IS LIMITED ONLY BY THE FUSE, WIRING, AND FILTER CAP RESISTANCE.

†† TRIP POINT IS APPROXIMATELY 7.3V.

* THE 6.4V ZENER IS INTERNAL TO THE LT123A.

** Q1 MUST BE ABLE TO WITHSTAND CONTINUOUS CURRENTS OF 5A IF ADDITIONAL SYSTEM SHUTDOWN IS NOT USED.

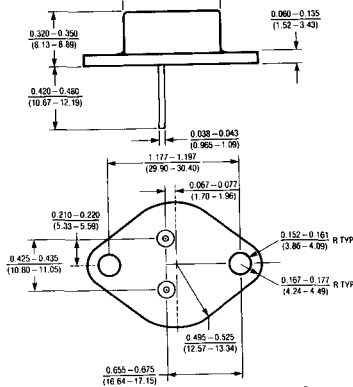
SCHEMATIC DIAGRAM



4

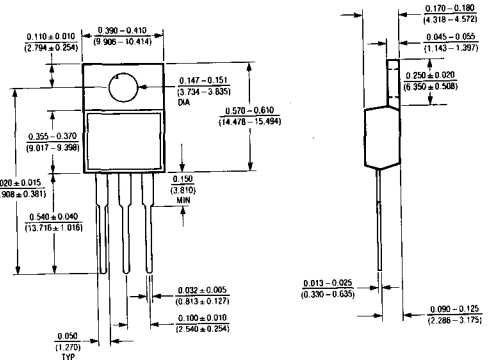
PACKAGE DESCRIPTION

K Package STEEL METAL CAN



	T _J max.	θ _{JA}	θ _{JC}
LT123AK LM123K	150°C	35°C/W	1.8°C/W
LT323AK LM323K	125°C	35°C/W	1.8°C/W

T Package TO-220



	T _J max.	θ _{JA}	θ _{JC}
LT323AT LM323T	125°C	50°C/W	2.5°C/W

NOTES

FEATURES

- *Guaranteed* 1% Initial Voltage Tolerance
- *Guaranteed* 0.01%/V Line Regulation
- *Guaranteed* 0.5% Load Regulation
- *Guaranteed* 0.02%/W Thermal Regulation
- 100% Burn-in in Thermal Limit

APPLICATIONS

- Adjustable Power Supplies
- System Power Supplies
- Precision Voltage/Current Regulators
- On-Card Regulators

DESCRIPTION

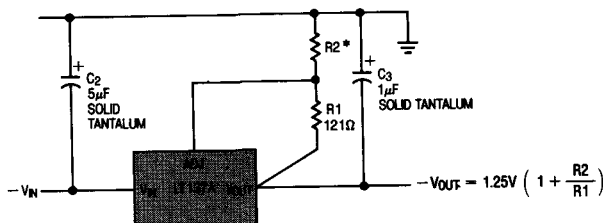
The LT137A/LT337A negative adjustable regulators will deliver up to 1.5Amps output current over an output voltage range of $-1.2V$ to $-37V$. Linear Technology has made significant improvements in these regulators compared to previous devices, such as better line and load regulation, and a maximum output voltage error of 1%.

Every effort has been made to make these devices easy to use and difficult to damage. Internal current and power limiting coupled with true thermal limiting prevents device damage due to overloads or shorts, even if the regulator is not fastened to a heat sink.

Maximum reliability is attained with Linear Technology's advanced processing techniques combined with a 100% burn-in in the thermal limit mode. This assures that all device protection circuits are working and eliminates field failures experienced with other regulators that receive only standard electrical testing.

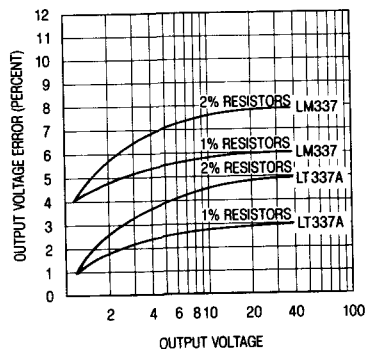
4

Negative Regulator



$$* R2 = R1 \left(\frac{|V_{OUT}|}{1.25V} - 1 \right)$$

Output Voltage Error



LT137A/LM137
LT337A/LM337

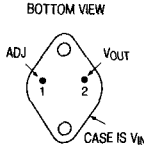
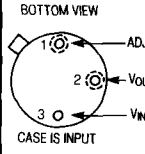
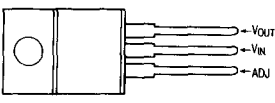
ABSOLUTE MAXIMUM RATINGS

Power Dissipation Internally Limited
 Input to Output Voltage Differential 40V
 Operating Junction Temperature Range
 LT137A/LM137 -55°C to 150°C
 LT337A/LM337 0°C to 125°C
 Storage Temperature Range
 LT137A/LM137 -65°C to 150°C
 LT337A/LM337 -65°C to 150°C
 Lead Temperature (Soldering, 10 sec.) 300°C

PRECONDITIONING

100% THERMAL LIMIT BURN-IN

PACKAGE/ORDER INFORMATION

BOTTOM VIEW  K PACKAGE	ORDER PART NO. LT137AK LM137K LT337AK LM337K	BOTTOM VIEW  H PACKAGE	ORDER PART NO. LT137AH LM137H LT337AH LM337H
FRONT VIEW  T PACKAGE	ORDER PART NO. LT337AT LM337T		

ELECTRICAL CHARACTERISTICS (See Note 1)

SYMBOL	PARAMETER	CONDITIONS	LT137A			LM137			UNITS	
			MIN	TYP	MAX	MIN	TYP	MAX		
V_{REF}	Reference Voltage	$ V_{IN} - V_{OUT} = 5V, I_{OUT} = 10mA, T_j = 25^\circ C$	-1.238	-1.250	-1.262	-1.225	-1.250	-1.275	V	
		$3V \leq V_{IN} - V_{OUT} \leq 40V$ $10mA \leq I_{OUT} \leq I_{MAX}, P \leq P_{MAX}$	● -1.220	-1.250	-1.280	-1.200	-1.250	-1.300	V	
$\frac{\Delta V_{OUT}}{\Delta I_{OUT}}$	Load Regulation	$10mA \leq I_{OUT} \leq I_{MAX}$, (See Note 2) $T_j = 25^\circ C, V_{OUT} \leq 5V$ $T_j = 25^\circ C, V_{OUT} \geq 5V$ $ V_{OUT} \leq 5V$ $ V_{OUT} \geq 5V$	●	5 0.1 10 0.2	25 0.5 50 1.0	15 0.3 20 0.3	25 0.5 50 1.0		mV % mV %	
$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	Line Regulation	$3V \leq V_{IN} - V_{OUT} \leq 40V$, (See Note 2) $T_j = 25^\circ C$	●	0.005 0.01	0.01 0.03	0.01 0.02	0.02 0.05		%/V %/V	
	Ripple Rejection	$V_{OUT} = -10V, f = 120Hz$ $C_{ADJ} = 0$ $C_{ADJ} = 10\mu F$	●	60 70	66 80	60 66	77		dB dB	
	Thermal Regulation	$T_j = 25^\circ C, 10msec$ Pulse	●	0.002	0.02	0.002	0.02		%/W	
I_{ADJ}	Adjust Pin Current		●	65	100	65	100		μA	
ΔI_{ADJ}	Adjust Pin Current Change	$10mA \leq I_{OUT} \leq I_{MAX}$ $3V \leq V_{IN}, V_{OUT} \leq 40V$	●	0.2 1.0	2 5	0.5 2	5 5		μA μA	
	Minimum Load Current	$ V_{IN} - V_{OUT} \leq 40V$ $ V_{IN} - V_{OUT} \leq 10V$	●	2.5 1.2	5.0 3.0	2.5 1.2	5.0 3.0		mA mA	
I_{SC}	Current Limit	$ V_{IN} - V_{OUT} \leq 15V$, K and T Package H Package $ V_{IN} - V_{OUT} = 40V$, K and T Package $T_j = 25^\circ C$ H Package	●	1.5 0.24 0.15	2.2 0.4 0.25	3.2 1.0 0.5	1.5 0.24 0.15	2.2 0.4 0.25		A A A
$\frac{\Delta V_{OUT}}{\Delta Temp}$	Temperature Stability of Output Voltage (Note 4)	$T_{MIN} \leq T \leq T_{MAX}$	●	0.6	1.5	0.6			%	
$\frac{\Delta V_{OUT}}{\Delta Time}$	Long Term Stability	$T_A = 125^\circ C, 1000$ Hours		0.3	1.0	0.3	1.0		%	
e_n	RMS Output Noise (% of V_{OUT})	$T_A = 25^\circ C, 10Hz \leq f \leq 10kHz$		0.003		0.003			%	
θ_{JC}	Thermal Resistance Junction to Case	H Package K Package		12 2.3	15 3.0	12 2.3	15 3.0		$^\circ C/W$ $^\circ C/W$	

ELECTRICAL CHARACTERISTICS (See Note 1)

SYMBOL	PARAMETER	CONDITIONS	LT337A			LM337			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V _{REF}	Reference Voltage	$ V_{IN} - V_{OUT} = 5V, I_{OUT} = 10mA,$ $T_J = 25^\circ C$	1.230	1.250	1.262	-1.213	-1.250	-1.287	V
		$3V \leq V_{IN} - V_{OUT} \leq 40V$ $10mA \leq I_{OUT} \leq I_{MAX}, P \leq P_{MAX}$	1.220	1.250	1.280	-1.200	-1.250	-1.300	V
$\frac{\Delta V_{OUT}}{\Delta I_{OUT}}$	Load Regulation	$10mA \leq I_{OUT} \leq I_{MAX}$, (See Note 2 & 3) $T_J = 25^\circ C, V_{OUT} \leq 5V$		5	25		15	50	mV
		$T_J = 25^\circ C, V_{OUT} \geq 5V$		0.1	0.5		0.3	1.0	%
		$ V_{OUT} \leq 5V$		10	50		20	70	mV
		$ V_{OUT} \geq 5V$		0.2	1.0		0.3	1.5	%
$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	Line Regulation	$3V \leq V_{IN} - V_{OUT} \leq 40V$, (See Note 2) $T_J = 25^\circ C$		0.005	0.01		0.01	0.04	%/V
				0.01	0.02		0.02	0.07	%/V
	Ripple Rejection	$V_{OUT} = -10V, f = 120Hz$ $C_{ADJ} = 0$ $C_{ADJ} = 10\mu F$		66	77		66	77	dB
	Thermal Regulation	$T_J = 25^\circ C, 10msec$ Pulse		0.002	0.02		0.003	0.04	%/W
I _{ADJ}	Adjust Pin Current			65	100		65	100	μA
ΔI_{ADJ}	Adjust Pin Current Change	$10mA \leq I_{OUT} \leq I_{MAX}$		0.5	5		0.5	5	μA
		$3V \leq V_{IN} - V_{OUT} \leq 40V$		1.0	5		2	5	μA
I _{sc}	Current Limit	$ V_{IN} - V_{OUT} \leq 40V$		2.5	5		2.5	10	mA
		$ V_{IN} - V_{OUT} \leq 10V$		1.0	3		1	6	mA
I _{sc}	Current Limit	$ V_{IN} - V_{OUT} \leq 15V,$ K and T Package		1.5	2.2		1.5	2.2	A
		H Package		0.5	0.8		0.5	0.8	A
		$ V_{IN} - V_{OUT} = 40V,$ K and T Package		0.15	0.5		0.15	0.4	A
		H Package		0.10	0.20		0.10	0.17	A
$\frac{\Delta V_{OUT}}{\Delta Temp}$	Temperature Stability of Output Voltage (Note 4)			0.6	1.5		0.6	1.5	%
$\frac{\Delta V_{OUT}}{\Delta Time}$	Long Term Stability	$T_A = 125^\circ C, 1000$ Hours		0.3	1.0		0.3	1.0	%
e _n	RMS Output Noise (% of V _{OUT})	$T_A = 25^\circ C, 10Hz \leq f \leq 10kHz$		0.003			0.003		%
θ_{JC}	Thermal Resistance Junction to Case	H Package		12	15		12	15	$^\circ C/W$
		K Package		2.3	3.0		2.3	3.0	$^\circ C/W$
		T Package		3	5		3	5	$^\circ C/W$

4

The ● denotes the specifications which apply over the full operating temperature range.

The shaded electrical specifications indicate those parameters which have been improved or guaranteed test limits provided for the first time.

Note 1: Unless otherwise indicated, these specifications apply: $|V_{IN} - V_{OUT}| = 5V$; and $I_{OUT} = 0.1A$ for the H package, $I_{OUT} = 0.5A$ for the K and T packages. Power dissipation is internally limited. However, these specifications apply for power dissipation up to 2W for the H package and 20W for the K and T packages. $I_{MAX} = 1.5A$ for the K and T packages, and 0.2A for the H package.

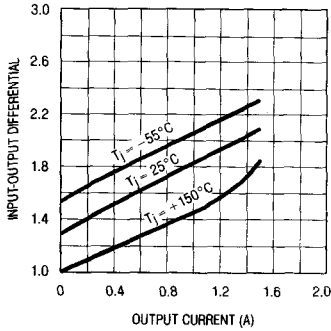
Note 2: Testing is done using a pulsed low duty cycle technique. See thermal regulation specifications for output changes due to heating effects. Load regulation is measured on the output pin at a point 1/8" below the base of the K and H package and at the junction of the wide and narrow portion of the lead on the T package.

Note 3: Load Regulation for the LT337AT is the same as for LM337T.

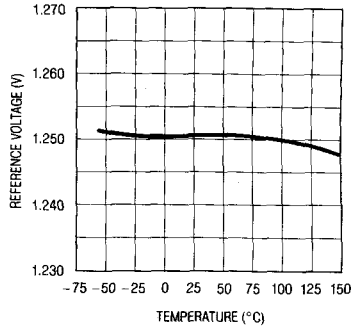
Note 4: Guaranteed on LT137A and LT337A, but not 100% tested in production.

TYPICAL PERFORMANCE CHARACTERISTICS

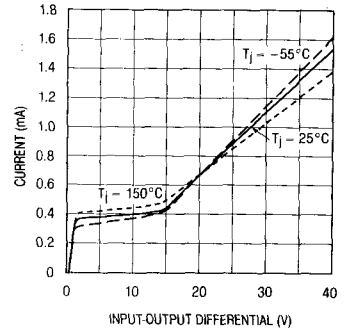
Dropout Voltage



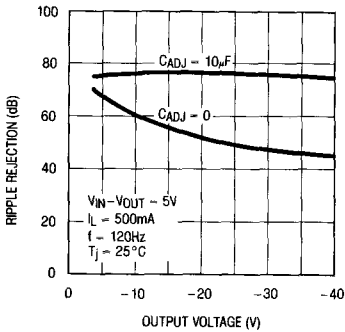
Temperature Stability



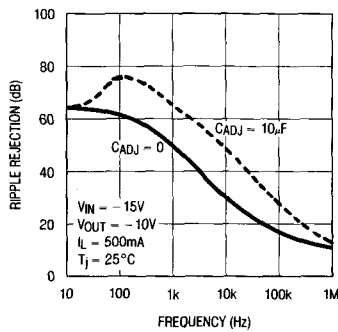
Minimum Load Current



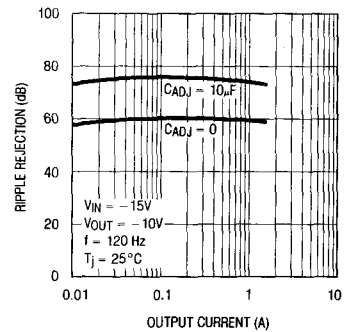
Ripple Rejection



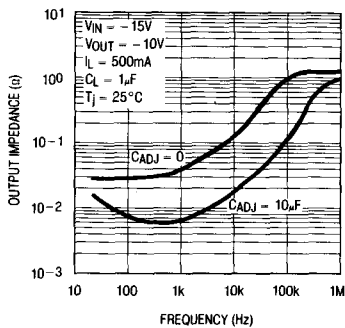
Ripple Rejection



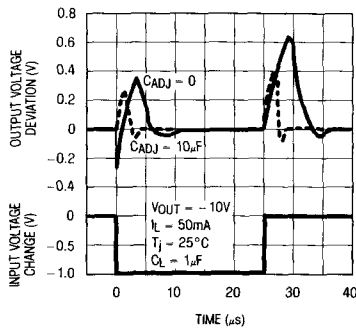
Ripple Rejection



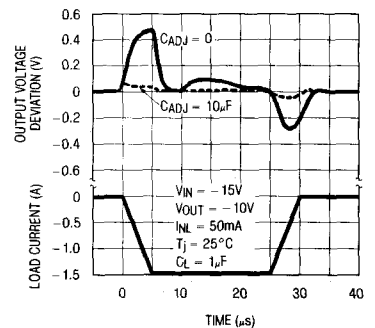
Output Impedance



Line Transient Response

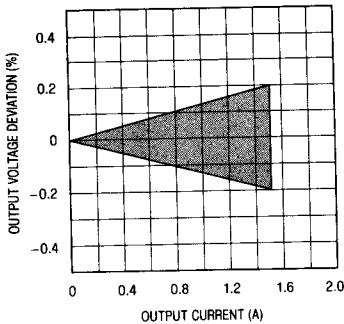


Load Transient Response



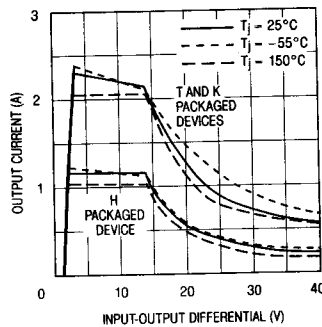
TYPICAL PERFORMANCE CHARACTERISTICS

Load Regulation*

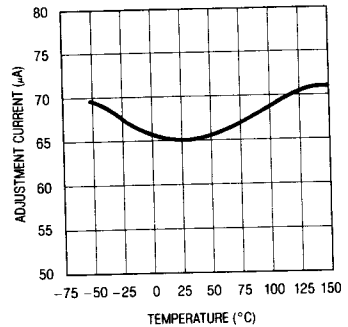


*The LT137A/337A has load regulation compensation which makes the typical unit read close to zero. This band represents the typical production spread.

Current Limit



Adjustment Current



APPLICATION INFORMATION

Output Voltage: The output voltage is determined by two external resistors, R_1 & R_2 (see Figure 1). The exact formula for the output voltage is:

$$V_{OUT} = V_{Ref} \left(1 + \frac{R_2}{R_1} \right) + I_{ADJ} (R_2)$$

Where: V_{Ref} = Reference Voltage, I_{ADJ} = Adjustment Pin Current. In most applications, the second term is small enough to be ignored, typically about 0.5% of V_{OUT} . In more critical applications, the exact formula should be used, with I_{ADJ} equal to $65\mu\text{A}$. Solving for R_2 yields:

$$R_2 = \frac{V_{OUT} - V_{Ref}}{\frac{V_{Ref}}{R_1} + I_{ADJ}}$$

Smaller values of R_1 and R_2 will reduce the influence of I_{ADJ} on the output voltage, but the no-load current drain on the regulator will be increased. Typical values for R_1 are between 100Ω and 300Ω , giving 12.5mA and 4.2mA no-load current respectively. There is an additional consideration in selecting R_1 , the minimum load current specification of the regulator. The operating current of the LT137A flows from input to output. If this current is not absorbed by the load, the output of the regulator will rise above the regulated value. The current drawn by R_1 and R_2 is normally high enough to

absorb the current, but care must be taken in no-load situations where R_1 and R_2 have high values. The maximum value for the operating current, which must be absorbed, is 5mA for the LT137A. If input-output voltage differential is less than 10V, the operating current that must be absorbed drops to 3mA.

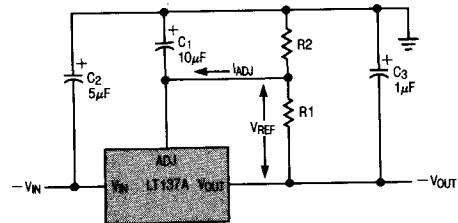


Figure 1

EXAMPLES:

- A precision 10V regulator to supply up to 1Amp load current.
 - Select $R_1 = 100\Omega$ to minimize effect of I_{ADJ}
 - Calculate $R_2 = \frac{V_{OUT} - V_{Ref}}{\frac{V_{Ref}}{R_1} - I_{ADJ}} = \frac{10V - 1.25V}{\frac{1.25V}{100\Omega} - 65\mu\text{A}} = 704\Omega$
- A 15V regulator to run off batteries and supply 50mA. $V_{IN\ MAX} = 25V$
 - To minimize battery drain, select R_1 as high as possible

$$R_1 = \frac{1.25V}{3mA} = 417\Omega, \text{ use } 404\Omega, 1\%$$

LT137A/LM137 LT337A/LM337

b. The high value for R_1 will exaggerate the error due to I_{ADJ} , so the exact formula to calculate R_2 should be used.

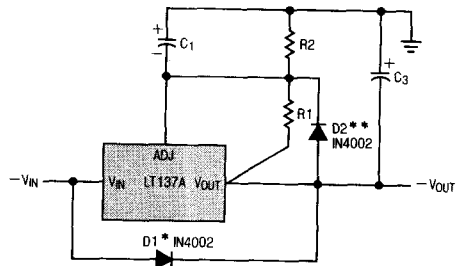
$$R_2 = \frac{V_{OUT} - V_{Ref}}{\frac{V_{Ref}}{R_1} - I_{ADJ}} = \frac{15V - 1.25V}{\frac{1.25V}{404\Omega} - 65 \times 10^{-6}} = 4539\Omega$$

Use $R_2 = 4530\Omega$

Capacitors and Protection Diodes: An output capacitor, C_3 , is required to provide proper frequency compensation of the regulator feedback loop. A $1\mu F$ or larger solid tantalum capacitor is generally sufficient for this purpose if the 1MHz impedance of the capacitor is 2Ω or less. High Q capacitors, such as Mylar, are not recommended because they tend to reduce the phase margin at light load currents. Aluminum electrolytic capacitors may also be used, but the minimum value should be $10\mu F$ to ensure a low impedance at 1MHz. The output capacitor should be located within a few inches of the regulator to keep lead impedance to a minimum. The following caution should be noted: if the output voltage is greater than 6V and an output capacitor greater than $20\mu F$ has been used, it is possible to damage the regulator if the input voltage becomes shorted, due to the output capacitor discharging into the regulator. This can be prevented by using diode D1 (see Figure 2) between the input and the output.

The input capacitor, C_2 , is only required if the regulator is more than 4 inches from the raw supply filter capacitor.

Bypassing the Adjustment Pin: The adjustment pin of the LT137A may be bypassed with a capacitor to ground, C_1 , to reduce output ripple, noise, and impedance. These parameters scale directly with output voltage if the adjustment pin is not bypassed. A bypass capacitor reduces ripple, noise, and impedance to that of a 1.25V regulator. In a 15V regulator for example, these parameters are improved by $15V/1.25V = 12$ to 1. This improvement holds only for those frequencies where the impedance of the bypass capacitor is less than R_1 . Ten microfarads is generally sufficient for 60Hz power line applications where the ripple frequency is 120Hz, since $X_C = 130\Omega$. The capacitor should have a voltage rating at least as high as the output voltage of the regulator. Values larger than $10\mu F$ may be used, but if the output is larger than 25V, a diode, D2, should be added between the output and adjustment pins (see Figure 2).



* D1 protects the regulator from input shorts to ground. It is required only when C_3 is larger than $20\mu F$ and V_{OUT} is larger than 6V.

** D2 protects the adjust pin of the regulator from output shorts if C_2 is larger than $10\mu F$ and V_{OUT} is larger than $-25V$.

Figure 2

Proper Connection of Divider Resistors: The LT137A has an excellent load regulation specification of 0.5% and is measured at a point $1/8"$ from the bottom of the package. To prevent degradation of load regulation, the resistors which set output voltage, R_1 and R_2 , must be connected as shown in Figure 3. Note that the positive side of the load has a true force and sense (Kelvin) connection, but the negative side of the load does not.

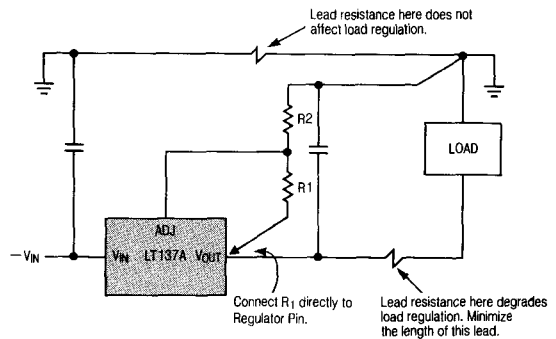


Figure 3

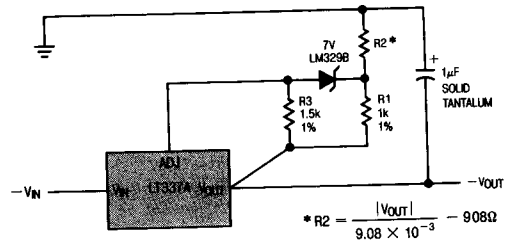
R_1 should be connected *directly* to the output lead of the regulator, as close as possible to the specified point $1/8"$ from the case. R_2 should be connected to the positive side of the load separately from the positive (ground) connection to the raw supply. With this arrangement, load regulation is degraded only by the resistance between the regulator output pin and the load. If R_1 is connected to the load, regulation will be degraded.

TYPICAL APPLICATIONS

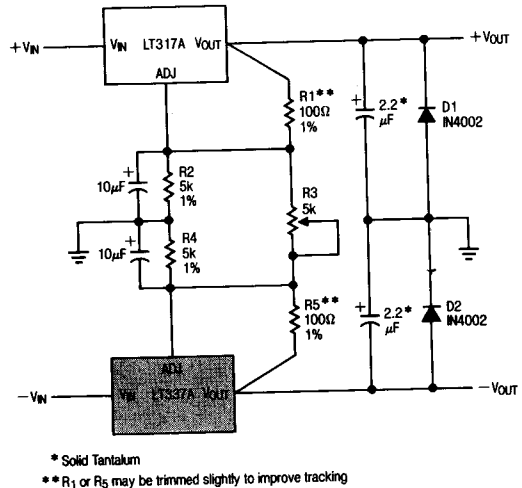
The output stability, load regulation, line regulation, thermal regulation, temperature drift, long term drift, and noise, can be improved by a factor of 6.6 over the standard regulator configuration. This assumes a zener whose drift and noise is considerably better than the regulator itself. The LM329B has 20PPM/°C maximum drift and about 10 times lower noise than the regulator.

In the application shown below, regulators #2 to "N" will track regulator #1 to within ±24mV initially, and to ±60mV over all load, line, and temperature conditions. If any regulator output is shorted to ground, all other outputs will drop to ≈ -2V. Load regulation of regulators 2 to "N" will be improved by $V_{OUT}/1.25V$ compared to a standard regulator, so regulator #1 should be the one which has the lowest load current.

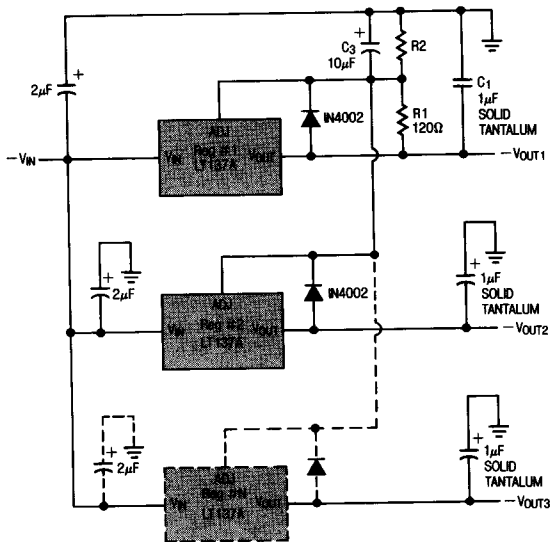
High Stability Regulator



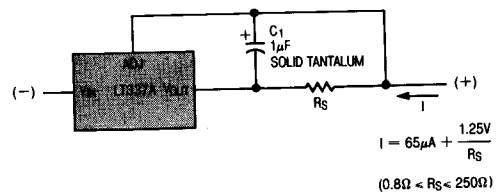
Dual Tracking Supply ± 1.25V to ± 20V



Multiple Tracking Regulators

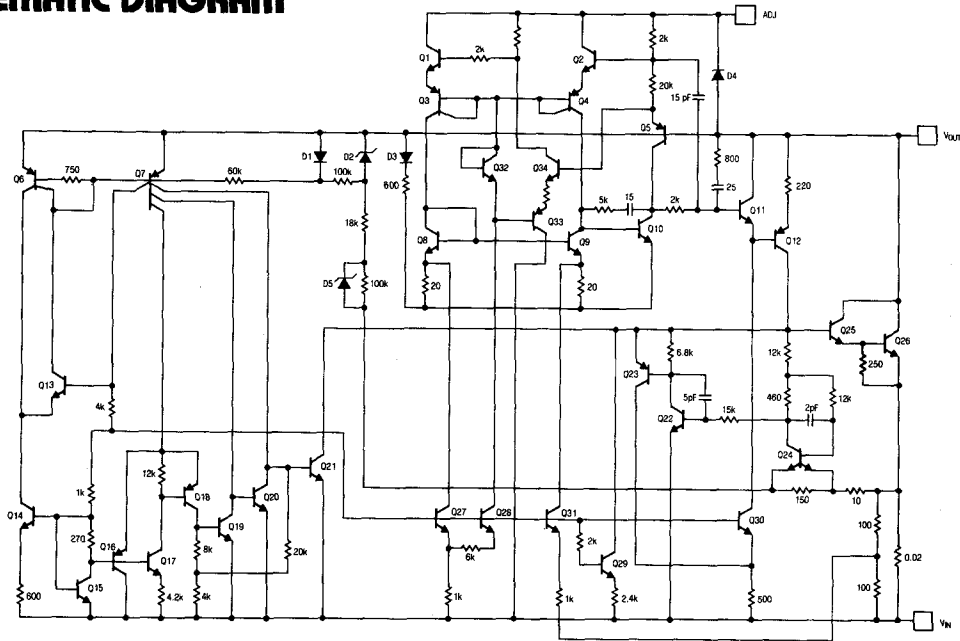


Current Regulator



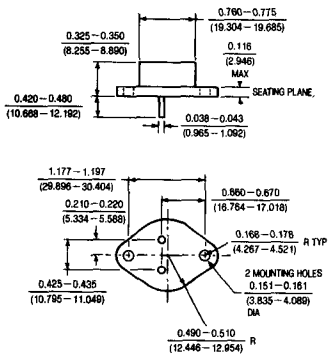
LT137A/LM137
LT337A/LM337

SCHEMATIC DIAGRAM



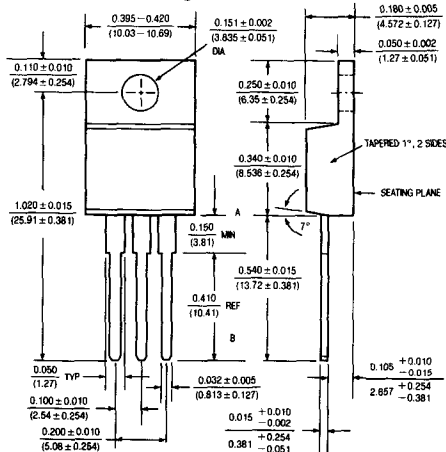
PACKAGE DESCRIPTION

K Package TO-3 STEEL Metal Can



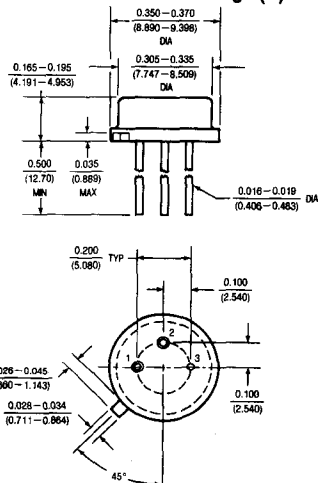
	T _J MAX	θ _{JC}
137A 137	150°C	3°C/W
337A 337	125°C	3°C/W

T Package TO-220 Plastic



	T _J MAX	θ _{JC}
337A 337	125°C	4°C/W
137A 137	150°C	4°C/W

3-Lead Metal Can Package (H)



	T _J MAX	θ _{JC}
137A 137	150°C	15°C/W
337A 337	125°C	15°C/W

FEATURES

- 50V Operation
- *Guaranteed* 1% Initial Voltage Tolerance
- *Guaranteed* 0.01%/V Line Regulation
- *Guaranteed* 0.5% Load Regulation
- *Guaranteed* 0.02%/W Thermal Regulation
- 100% Burn-in in Thermal Limit

APPLICATIONS

- Adjustable Power Supplies
- System Power Supplies
- Precision Voltage/Current Regulators
- On-Card Regulators

DESCRIPTION

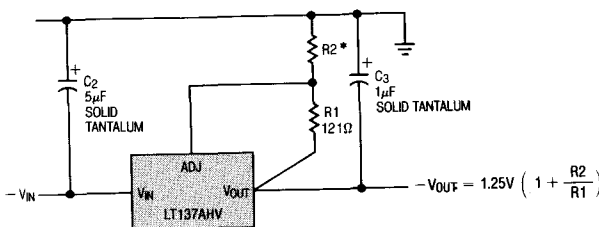
The LT137AHV/LM137HV negative high voltage adjustable regulators will deliver up to 1.5 Amps output current over an output voltage range of -1.2V to -47V. Linear Technology has made significant improvements in these regulators compared to previous devices, such as better line and load regulation, and a maximum output voltage error of 1% for the LT137AHV and LT337AHV.

Every effort has been made to make these devices easy to use and difficult to damage. Internal current and power limiting coupled with true thermal limiting prevents device damage due to overloads or shorts, even if the regulator is not fastened to a heat sink.

Maximum reliability is attained with Linear Technology's advanced processing techniques combined with a 100% burn-in in the thermal limit mode. This assures that all device protection circuits are working and eliminates field failures experienced with other regulators that receive only standard electrical testing. For performance curves and applications circuits see the LT137A series data sheet.

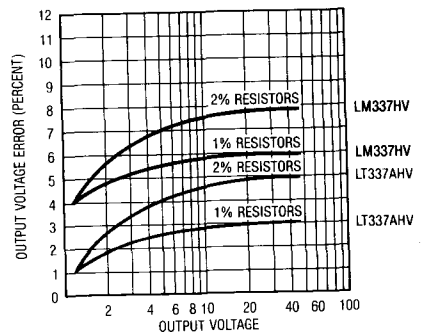
4

Negative Regulator



$$* R2 = R1 \left(\frac{|V_{OUT}|}{1.25V} - 1 \right)$$

Worst Case Output Voltage Error @ $T_J = 25^\circ C$

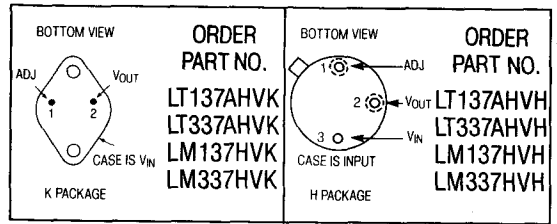


LT137AHV/LT337AHV LM137HV/LM337HV

ABSOLUTE MAXIMUM RATINGS

Power Dissipation	Internally Limited
Input to Output Voltage Differential	50V
Operating Junction Temperature Range	
LT137AHV/LM137HV	-55°C to 150°C
LT337AHV/LM337HV	0°C to 125°C
Storage Temperature Range	
LT137AHV/LM137HV	-65°C to 150°C
LT337AHV/LM337HV	-65°C to 150°C
Lead Temperature (Soldering, 10 sec.)	300°C

PACKAGE/ORDER INFORMATION



PRECONDITIONING

100% THERMAL LIMIT BURN-IN

ELECTRICAL CHARACTERISTICS (See Note 1)

SYMBOL	PARAMETER	CONDITIONS	LT137AHV			LM137HV			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{REF}	Reference Voltage	$ V_{IN} - V_{OUT} = 5V, I_{OUT} = 10mA, T_j = 25^\circ C$	-1.238	-1.250	-1.262	-1.225	-1.250	-1.275	V
		$3V \leq V_{IN} - V_{OUT} \leq 50V, 10mA \leq I_{OUT} \leq I_{MAX}, P \leq P_{MAX}$	-1.220	-1.250	-1.280	-1.200	-1.250	-1.300	V
$\frac{\Delta V_{OUT}}{\Delta I_{OUT}}$	Load Regulation	$10mA \leq I_{OUT} \leq I_{MAX}, (See Note 2), T_j = 25^\circ C, V_{OUT} \leq 5V$	5	25		15	25		mV
		$T_j = 25^\circ C, V_{OUT} \geq 5V$	0.1	0.5		0.3	0.5		%
		$ V_{OUT} \leq 5V$	10	50		20	50		mV
		$ V_{OUT} \geq 5V$	0.2	1.0		0.3	1.0		%
$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	Line Regulation	$3V \leq V_{IN} - V_{OUT} \leq 50V (See Note 2), T_j = 25^\circ C$	0.005	0.01		0.01	0.02		%/V
			0.01	0.03		0.02	0.05		%/V
	Ripple Rejection	$V_{OUT} = -10V, f = 120Hz, C_{ADJ} = 0, C_{ADJ} = 10\mu F$	70	60		60	60		dB
				80		66	77		dB
	Thermal Regulation	$T_j = 25^\circ C, T = 2ms \text{ to } 12ms$		0.002	0.02		0.002	0.02	%/W
I_{ADJ}	Adjust Pin Current		65	100		65	100		μA
ΔI_{ADJ}	Adjust Pin Current Change	$10mA \leq I_{OUT} \leq I_{MAX}, 2.5V \leq V_{IN} - V_{OUT} \leq 50V$	0.2	2		0.5	5		μA
			2	6		3	6		μA
	Minimum Load Current	$ V_{IN} - V_{OUT} \leq 50V, V_{IN} - V_{OUT} \leq 10V$	2.5	5.0		2.5	5.0		mA
			1.2	3.0		1.2	3.0		mA
I_{SC}	Current Limit	$ V_{IN} - V_{OUT} \leq 13V$							
		K Package	1.5	2.2	3.2	1.5	2.2	3.2	A
		H Package	0.5	0.8	1.6	0.5	0.8	1.6	A
		$ V_{IN} - V_{OUT} = 50V$							
		K Package	0.2	0.4	0.8	0.2	0.4	0.8	A
		H Package	0.1	0.17	0.5	0.1	0.17	0.5	A
$\frac{\Delta V_{OUT}}{\Delta Temp}$	Temperature Stability of Output Voltage (Note 3)	$T_{MIN} \leq T \leq T_{MAX}$	0.6	1.5		0.6			%
$\frac{\Delta V_{OUT}}{\Delta Time}$	Long Term Stability	$T_A = 125^\circ C, 1000 \text{ Hours}$	0.3	1.0		0.3	1.0		%
e_n	RMS Output Noise (% of V_{OUT})	$T_A = 25^\circ C, 10Hz \leq f \leq 10kHz$	0.003			0.003			%
θ_{JC}	Thermal Resistance Junction to Case	H Package	12	15		12	15		$^\circ C/W$
		K Package	2.3	3.0		2.3	3.0		$^\circ C/W$

ELECTRICAL CHARACTERISTICS (See Note 1)

SYMBOL	PARAMETER	CONDITIONS	LT337AHV			LM337HV			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{REF}	Reference Voltage	$ V_{IN} - V_{OUT} = 5V, I_{OUT} = 10mA, T_j = 25^\circ C$	-1.238	-1.250	-1.262	-1.213	-1.250	-1.287	V
		$3V \leq V_{IN} - V_{OUT} \leq 50V, 10mA \leq I_{OUT} \leq I_{MAX}, P \leq P_{MAX}$	●	-1.220	-1.250	-1.280	-1.200	-1.250	-1.300
$\frac{\Delta V_{OUT}}{\Delta I_{OUT}}$	Load Regulation	$10mA \leq I_{OUT} \leq I_{MAX}$ (See Note 2) $T_j = 25^\circ C, V_{OUT} \leq 5V$		5	25	15	50	mV	
		$T_j = 25^\circ C, V_{OUT} \geq 5V$		0.1	0.5	0.3	1.0	%	
		$ V_{OUT} \leq 5V$	●	10	50	20	70	mV	
		$ V_{OUT} \geq 5V$	●	0.2	1.0	0.3	1.5	%	
$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	Line Regulation	$3V \leq V_{IN} - V_{OUT} \leq 50V$ (See Note 2) $T_j = 25^\circ C$		0.005	0.04	0.01	0.04	%/V	
	Ripple Rejection	$V_{OUT} = -10V, f = 120Hz, C_{ADJ} = 0, C_{ADJ} = 10\mu F$	●	60	80	66	77	dB	
	Thermal Regulation	$T_j = 25^\circ C, T = 2ms$ to 12ms		0.002	0.04	0.003	0.04	%/W	
I_{ADJ}	Adjust Pin Current		●	65	100	65	100	μA	
ΔI_{ADJ}	Adjust Pin Current Change	$10mA \leq I_{OUT} \leq I_{MAX}$	●	0.2	2	2	5	μA	
		$2.5V \leq V_{IN} - V_{OUT} \leq 50V$	●	2	6	3	6	μA	
I_{SC}	Current Limit	$ V_{IN} - V_{OUT} \leq 40V$	●	2.5	5	2.5	10	mA	
		$ V_{IN} - V_{OUT} \leq 10V$	●	1.2	3	1	6	mA	
I_{SC}	Current Limit	$ V_{IN} - V_{OUT} \leq 13V$ K Package	●	1.5	2.2	3.5	1.5	2.2	3.5
		H Package	●	0.5	0.8	1.8	0.5	0.8	1.8
		$ V_{IN} - V_{OUT} = 50V$ K Package		0.1	0.4	0.8	0.1	0.4	0.8
		H Package		0.05	0.17	0.5	0.05	0.17	0.5
$\frac{\Delta V_{OUT}}{\Delta Temp}$	Temperature Stability of Output Voltage (Note 3)		●	0.6	1.5	0.6		%	
$\frac{\Delta V_{OUT}}{\Delta Time}$	Long Term Stability	$T_A = 125^\circ C, 1000$ Hours		0.3	1.0	0.3	1.0	%	
e_n	RMS Output Noise (% of V_{OUT})	$T_A = 25^\circ C, 10Hz \leq f \leq 10kHz$		0.003		0.003		%	
θ_{JC}	Thermal Resistance Junction to Case	H Package		12	15	12	15	$^\circ C/W$	
		K Package		2.3	3.0	2.3	3.0	$^\circ C/W$	

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The ● denotes the specifications which apply over the full operating temperature range.

The shaded electrical specifications indicate those parameters which have been improved or guaranteed test limits provided for the first time.

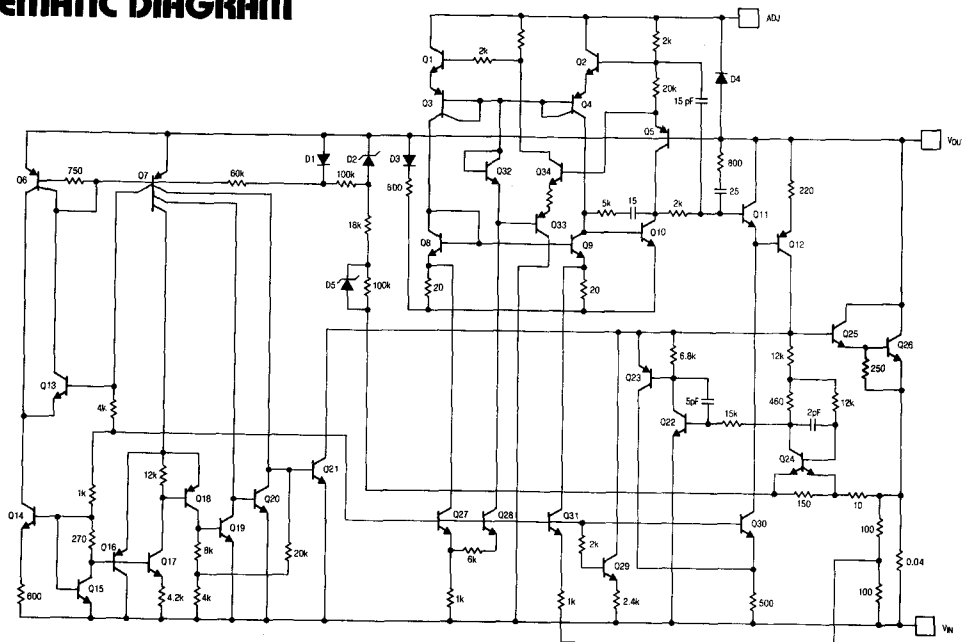
Note 1: Unless otherwise indicated, these specifications apply: $|V_{IN} - V_{OUT}| = 5V$; and $I_{OUT} = 0.1A$ for the H package, $I_{OUT} = 0.5A$ for the K package. Power dissipation is internally limited. However, these specifications apply for power dissipation up to 2W for the H package and 20W for the K package. $I_{MAX} = 1.5A$ for the K package, and 0.2A for the H package.

Note 2: Testing is done using a pulsed low duty cycle technique. See thermal regulation specifications for output changes due to heating effects. Load regulation is measured on the output pin at a point 1/8 inch below the base of the K and H package.

Note 3: Guaranteed on the LT137AHV and LT337AHV, but not 100% tested in production.

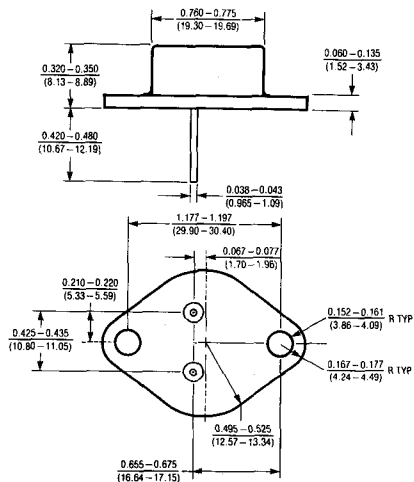
LT137AHV/LT337AHV LM137HV/LM337HV

SCHEMATIC DIAGRAM



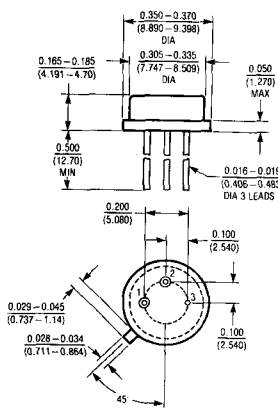
PACKAGE DESCRIPTION

K Package TO-3 STEEL Metal Can



	T _J MAX	θ _{JC}
137AHV 137HV	150°C	3°C/W
337AHV 337HV	125°C	3°C/W

H Package 3-Lead Metal Can



	T _J MAX	θ _{JC}
137AHV 137HV	150°C	15°C/W
337AHV 337HV	125°C	15°C/W

FEATURES

- *Guaranteed* 1% Initial Tolerance
- *Guaranteed* 0.3% Load Regulation
- *Guaranteed* 5 Amp Output Current
- 100% Thermal Limit Burn-in
- 12 Amp Transient Output Current

APPLICATIONS

- High Power Linear Regulator
- Battery Chargers
- Power Driver
- Constant Current Regulator

DESCRIPTION

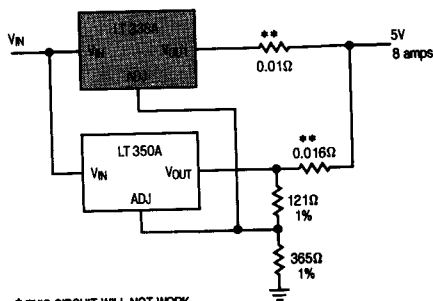
The LT138A series of adjustable regulators provide 5 amps output current over an output voltage range of 1.2 volts to 32 volts. The internal voltage reference is trimmed to less than 1%, enabling a very tight output voltage. In addition to excellent line and load regulation, with full overload protection, the LT138A incorporates new current limiting circuitry allowing large transient load currents to be handled for short periods. Transient load currents of up to 12 amps can be supplied without limiting, eliminating the need for a large output capacitor.

The LT138A is an improved version of the popular LM138 with improved circuit design and advanced process techniques to provide superior performance and reliability.

The graph below shows the significant improvement in output voltage tolerance achieved by using the LT138A or LT338A.

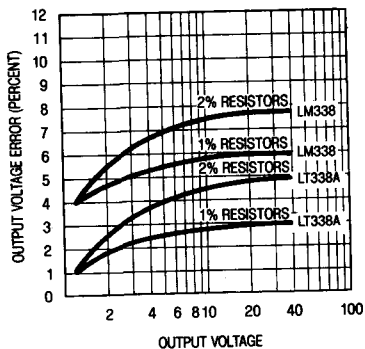
4

* Parallel Regulators for Higher Current



* THIS CIRCUIT WILL NOT WORK WITH LM VERSION DEVICES
 ** CURRENT SHARING RESISTORS DEGRADE REGULATION TO 1%

Output Voltage Error



LT138A/LT338A
LM138/LM338

ABSOLUTE MAXIMUM RATINGS

Power Dissipation Internally Limited
 Input to Output Voltage Differential 35V
 Operating Junction Temperature Range
 LT138A/LM138 -55°C to 150°C
 LT338A/LM338 0°C to 125°C
 Storage Temperature Range
 LT138A/LM138 -65°C to 150°C
 LT338A/LM338 -65°C to 150°C
 Lead Temperature (Soldering, 10 sec.) 300°C

PACKAGE/ORDER INFORMATION

BOTTOM VIEW
ADJUSTMENT
1 2
VIN
CASE IS OUTPUT
K PACKAGE
TO-3 METAL CAN
(STEEL)

ORDER PART NUMBER

LT138AK
LT338AK
LM138K
LM338K

PRECONDITIONING

100% THERMAL LIMIT BURN-IN

ELECTRICAL CHARACTERISTICS (See Note 1)

SYMBOL	PARAMETER	CONDITIONS	LT138A			LM138			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V _{REF}	Reference Voltage	I _{OUT} = 10mA T _J = 25°C	1.238	1.250	1.262				V
		3V ≤ (V _{IN} - V _{OUT}) ≤ 35V 10mA ≤ I _{OUT} ≤ 5A, P ≤ 50W	1.225	1.250	1.270	1.19	1.24	1.29	V
ΔV _{OUT} /ΔV _{IN}	Line Regulation	3V ≤ (V _{IN} - V _{OUT}) ≤ 35V, (See Note 2) T _A = 25°C		0.005	0.01		0.005	0.01	%/V
				0.02	0.04		0.02	0.04	%/V
ΔV _{OUT} /ΔI _{OUT}	Load Regulation	10mA ≤ I _{OUT} ≤ 5A, (See Note 2) T _A = 25°C V _{OUT} ≤ 5V V _{OUT} ≥ 5V		5	15		5	15	mV
				0.1	0.3		0.1	0.3	%
		V _{OUT} ≤ 5V V _{OUT} ≥ 5V		20	30		20	30	mV
	Thermal Regulation	T _A = 25°C, 20msec pulse		0.002	0.01		0.002	0.01	%/W
	Ripple Rejection	V _{OUT} = 10V, f = 120Hz C _{ADJ} = 0 C _{ADJ} = 10μF		60			60		dB
I _{ADJ}	Adjust Pin Current		60	75		60	75		dB
ΔI _{ADJ}	Adjust Pin Current Change	10mA ≤ I _{OUT} ≤ 5A, 3V ≤ (V _{IN} - V _{OUT}) ≤ 35V	60			60			μA
	Minimum Load Current	(V _{IN} - V _{OUT}) = 35V		45	100		45	100	μA
I _{SC}	Current Limit	(V _{IN} - V _{OUT}) ≤ 10V DC 0.5ms peak		0.2	5		0.2	5	μA
				3.5	5		3.5	5	mA
		(V _{IN} - V _{OUT}) = 30V, T _J = 25°C		5	8		5	8	A
			7	12		7	12	A	
				1			1		A
ΔV _{OUT} /ΔTemp	Temperature Stability			1	2		1		%
ΔV _{OUT} /ΔTime	Long Term Stability	T _A = 125°C, 1000 Hours		0.3	1		0.3	1	%
e _n	RMS Output Noise (% of V _{OUT})	T _A = 25°C, 10Hz ≤ f ≤ 10kHz		0.001			0.003		%
θ _{JC}	Thermal Resistance Junction to Case	K Package		1			1		°C/W

ELECTRICAL CHARACTERISTICS (See Note 1)

SYMBOL	PARAMETER	CONDITIONS	LT338A			LM338			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V _{REF}	Reference Voltage	$I_{OUT} = 10mA, T_A = 25^\circ C$	1.238	1.250	1.262				V
		$3V < (V_{IN} - V_{OUT}) < 35V$ $10mA < I_{OUT} < 5A, P < 50W$	● 1.225	1.250	1.270	1.19	1.24	1.29	V
$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	Line Regulation	$3V < (V_{IN} - V_{OUT}) < 35V$, (See Note 2) $T_A = 25^\circ C$		0.005 0.02	0.01 0.04		0.005 0.02	0.03 0.06	%/V %/V
		$10mA < I_{OUT} < 5A$, (See Note 2) $T_A = 25^\circ C$ $V_{OUT} < 5V$ $V_{OUT} > 5V$		5 0.1	15 0.3		5 0.1	25 0.5	mV %
$\frac{\Delta V_{OUT}}{\Delta I_{OUT}}$	Load Regulation	$V_{OUT} < 5V$ $V_{OUT} > 5V$	●	20 0.3	30 0.6		20 0.3	50 1	mV %
		Thermal Regulation	$T_A = 25^\circ C, 20msec$ Pulse		0.002	0.02		0.002	0.02
Ripple Rejection	Ripple Rejection	$V_{OUT} = 10V, f = 120Hz$ $C_{ADJ} = 0$ $C_{ADJ} = 10\mu F$	●	60	75		60	75	dB dB
			● 60			60			
I _{ADJ}	Adjust Pin Current		●	45	100		45	100	μA
ΔI_{ADJ}	Adjust Pin Current Change	$10mA < I_{OUT} < 5A$, $3V < (V_{IN} - V_{OUT}) < 35V$	●	0.2	5		0.2	5	μA
		Minimum Load Current		3.5	10		3.5	10	mA
I _{SC}	Current Limit	$(V_{IN} - V_{OUT}) < 10V$ DC 0.5ms peak	●	5	8		5	8	A A
			●	7	12		7	12	
		$(V_{IN} - V_{OUT}) = 30V, T_J = 25^\circ C$		1	2		1		A %
$\frac{\Delta V_{OUT}}{\Delta Temp}$	Temperature Stability		●	1	2		1		%
$\frac{\Delta V_{OUT}}{\Delta Time}$	Long Term Stability	$T_A = 125^\circ C, 1000$ Hours		0.3	1		0.3	1	%
e _n	RMS Output Noise (% of V _{OUT})	$T_A = 25^\circ C, 10Hz < f < 10kHz$		0.001			0.003		%
θ _{JC}	Thermal Resistance Junction to Case	K Package			1			1	°C/W

4

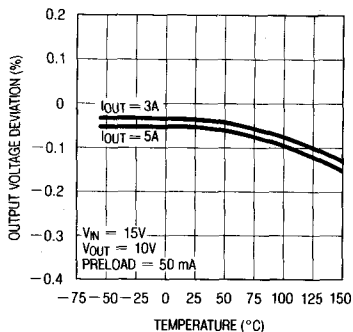
The ● denotes the specifications which apply over the full operating temperature range.

Note 1: Unless otherwise specified, these specifications apply: $V_{IN} - V_{OUT} = 5V$ and $I_{OUT} = 2.5A$. These specifications are applicable for power dissipations up to 50W.

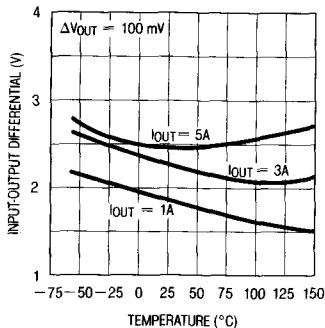
Note 2: See thermal regulation specifications for changes in output voltage due to heating effects. Load and line regulation are measured at a constant junction temperature by low duty cycle pulse testing.

TYPICAL PERFORMANCE CHARACTERISTICS

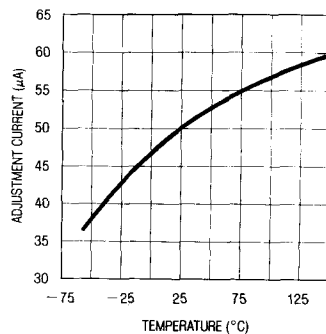
Load Regulation



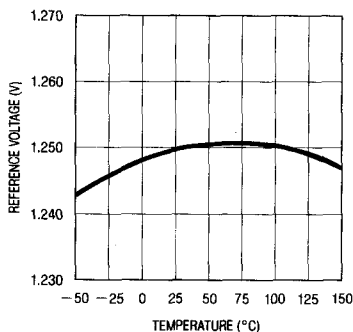
Dropout Voltage



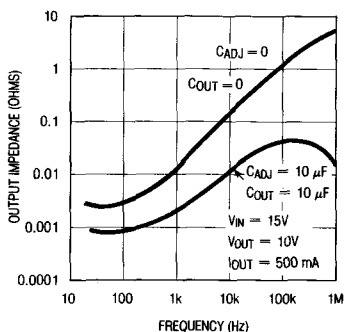
Adjustment Current



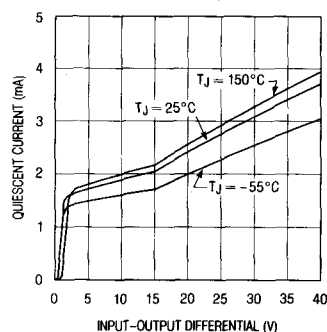
Temperature Stability



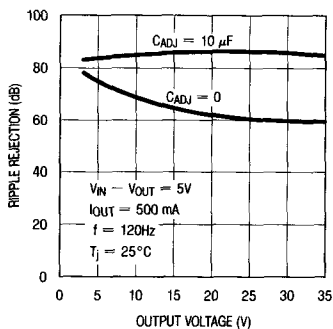
Output Impedance



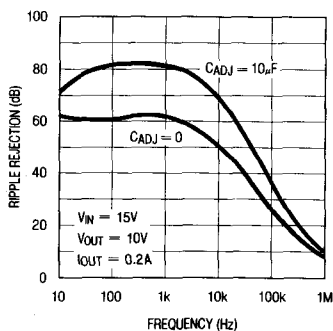
Minimum Operating Current



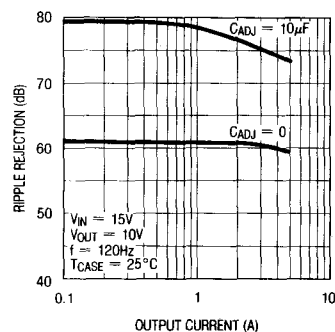
Ripple Rejection



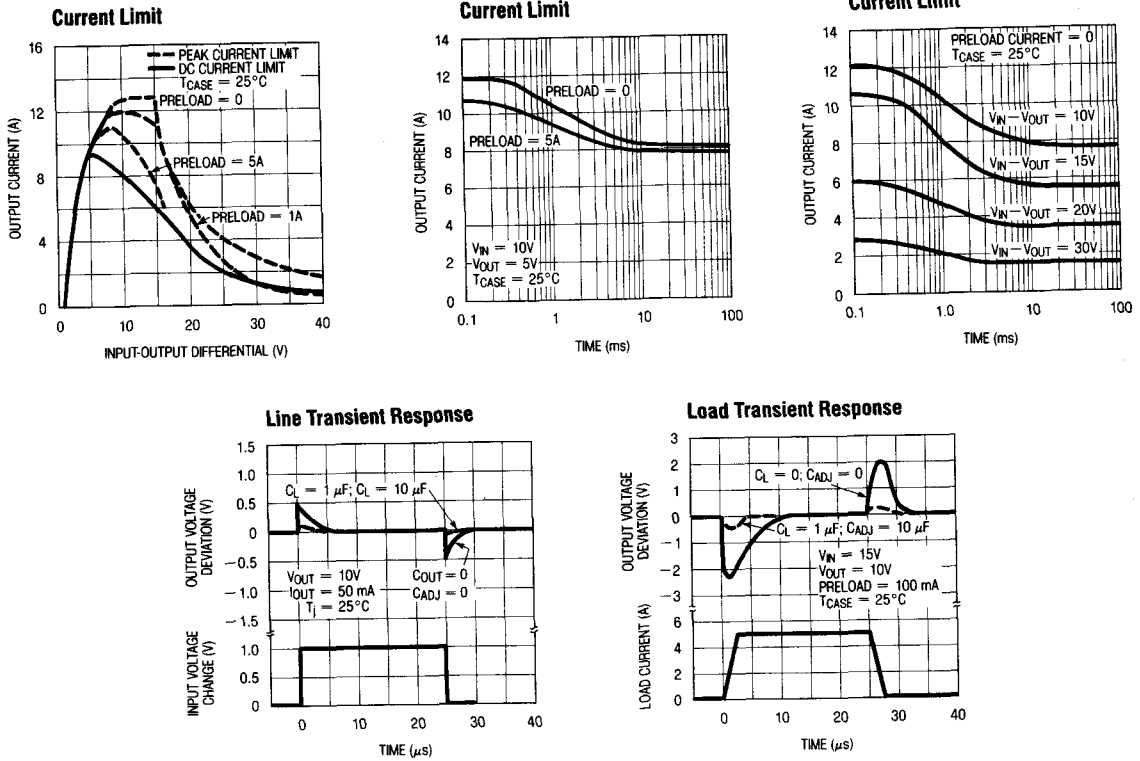
Ripple Rejection



Ripple Rejection



TYPICAL PERFORMANCE CHARACTERISTICS

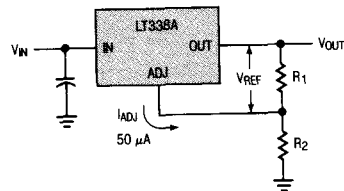


4

APPLICATIONS INFORMATION

General

The LT138A develops a 1.25V reference voltage between the output and the adjustable terminal (see Figure 1). By placing a resistor, R1, between these two terminals, a constant current is caused to flow through R1 and down through R2 to set the overall output voltage. Normally this current is the specified minimum load current of 5mA or 10mA. Because I_{ADJ} is very small and constant when compared with the current through R1, it represents a small error and can usually be ignored. It is easily seen from the output voltage equation, that even if the resistors were of exact value, the accuracy of the output is limited by the accuracy of V_{REF} . Earlier adjustable regulators had a reference tolerance of $\pm 4\%$ which is dangerously



$$V_{OUT} = V_{REF} \left(1 + \frac{R_2}{R_1} \right) + I_{ADJ} R_2$$

Basic Adjustable Regulator
Figure 1

close to the $\pm 5\%$ supply tolerance required in many logic and analog systems. Further, even 1% resistors can drift $0.01\%/^{\circ}C$, adding additional error to the output voltage tolerance.

LT138A/LT338A LM138/LM338

For example, using 2% resistors and $\pm 4\%$ tolerance for V_{REF} , calculations will show that the expected range of a 5V regulator design would be $4.66V \leq V_{OUT} \leq 5.36V$ or approximately $\pm 7\%$. If the same example were used for a 15V regulator, the expected tolerance would be $\pm 8\%$. With these results most applications required some method of trimming, usually a trim pot. This solution is both expensive and not conducive to volume production.

One of the enhancements of Linear Technology's adjustable regulators over existing devices is the tightened initial tolerance of V_{REF} . This allows relatively inexpensive 1% or 2% film resistors to be used for R1 and R2 to set the output voltage within an acceptable tolerance.

With a guaranteed 1% reference, a 5V power supply design, using $\pm 2\%$ resistors, would have a worst case manufacturing tolerance of $\pm 4\%$. If 1% resistors are used, the tolerance will drop to $\pm 2.5\%$. A plot of the worst case output voltage tolerance as a function of resistor tolerance is shown on the front page.

For convenience, a table of standard 1% resistor values is shown below.

Table of 1/2% and 1% Standard Resistance Values

1.00	1.47	2.15	3.16	4.64	6.81
1.02	1.50	2.21	3.24	4.75	6.98
1.05	1.54	2.26	3.32	4.87	7.15
1.07	1.58	2.32	3.40	4.99	7.32
1.10	1.62	2.37	3.48	5.11	7.50
1.13	1.65	2.43	3.57	5.23	7.68
1.15	1.69	2.49	3.65	5.36	7.87
1.18	1.74	2.55	3.74	5.49	8.06
1.21	1.78	2.61	3.83	5.62	8.25
1.24	1.82	2.67	3.92	5.76	8.45
1.27	1.87	2.74	4.02	5.90	8.66
1.30	1.91	2.80	4.12	6.04	8.87
1.33	1.96	2.87	4.22	6.19	9.09
1.37	2.00	2.94	4.32	6.34	9.31
1.40	2.05	3.01	4.42	6.49	9.53
1.43	2.10	3.09	4.53	6.65	9.76

Standard Resistance Values are obtained from the Decade Table by multiplying by multiples of 10. As an example, 1.21 can represent 1.21 Ω , 12.1 Ω , 121 Ω , 1.21K Ω etc.

Bypass Capacitors

Input bypassing using a $1\mu F$ tantalum or $25\mu F$ electrolytic is recommended when the input filter capacitors are more than 5 inches from the device. Improved ripple rejection (80 dB) can be accomplished by adding a

$10\mu F$ capacitor from the adjust pin to ground. Increasing the size of the capacitor to $20\mu F$ will help ripple rejection at low output voltage since the reactance of this capacitor should be small compared to the voltage setting resistor, R2. For improved AC transient response and to prevent the possibility of oscillation due to unknown reactive load, a $1\mu F$ capacitor is also recommended at the output. Because of their low impedance at high frequencies, the best type of capacitor to use is solid tantalum.

Protection Diodes

The LT138A/338A do not require a protection diode from the adjustment terminal to the output (see figure 2). Improved internal circuitry eliminates the need for this diode when the adjustment pin is bypassed with a capacitor to improve ripple rejection.

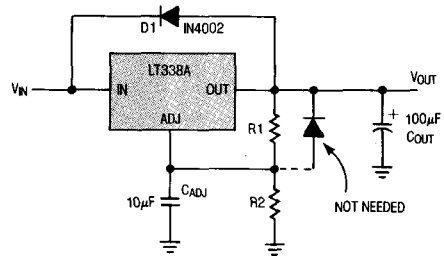


Figure 2

If a very large output capacitor is used, such as a $100\mu F$ shown in figure 2, the regulator could be damaged or destroyed if the input is accidentally shorted to ground or crowbarred, due to the output capacitor discharging into the output terminal of the regulator. To prevent this, a diode D1 as shown, is recommended to safely discharge the capacitor.

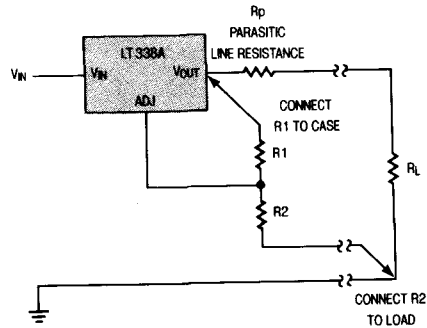
Load Regulation

Because the LT138A is a three-terminal device, it is not possible to provide true remote load sensing. Load regulation will be limited by the resistance of the wire connecting the regulator to the load. The data sheet specification for load regulation is measured at the bottom of the package. Negative side sensing is a true Kelvin connection, with the bottom of the output divider returned to the negative side of the load. Although it may not be immediately obvious, best load regulation is obtained when the top of the resistor divider, (R1), is connected *directly* to the case *not to the load*. This is illustrated in Figure 3. If R1 were connected to the

load, the effective resistance between the regulator and the load would be

$$R_p \times \left(\frac{R_2 + R_1}{R_1} \right), R_p = \text{Parasitic Line Resistance.}$$

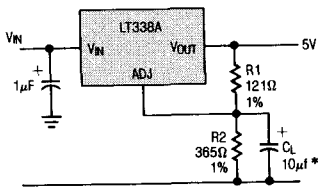
Connected as shown, R_p is not multiplied by the divider ratio. R_p is about 0.004Ω per foot using 16 gauge wire. This translates to 4mV/ft at 1A load current, so it is important to keep the positive lead between regulator and load as short as possible, and use large wire or PC board traces.



Connections For Best Load Regulation
Figure 3.

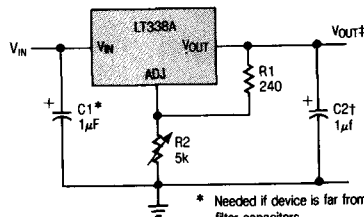
TYPICAL APPLICATIONS

Improving Ripple Rejection



* C_1 IMPROVES RIPPLE REJECTION X_C SHOULD BE SMALL COMPARED TO R_2

1.2V-25V Adjustable Regulator

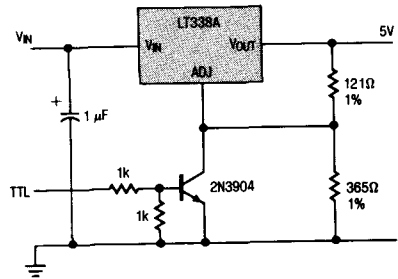


* Needed if device is far from filter capacitors

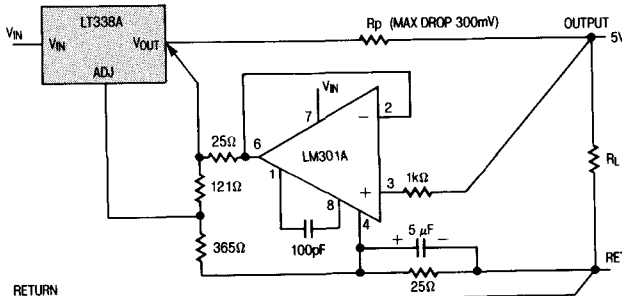
† Optional—improves transient response

$$\ddagger V_{OUT} = 1.25V \left(1 + \frac{R_2}{R_1} \right)$$

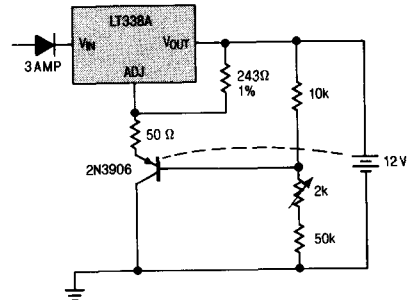
5V Regulator With Shut Down



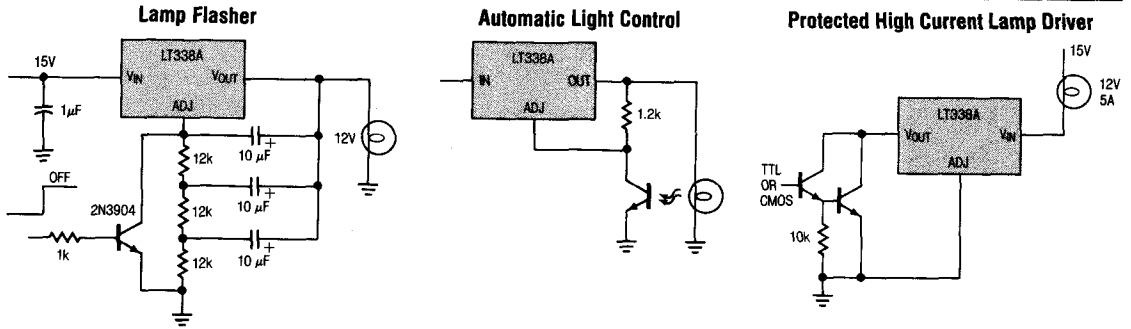
Remote Sensing



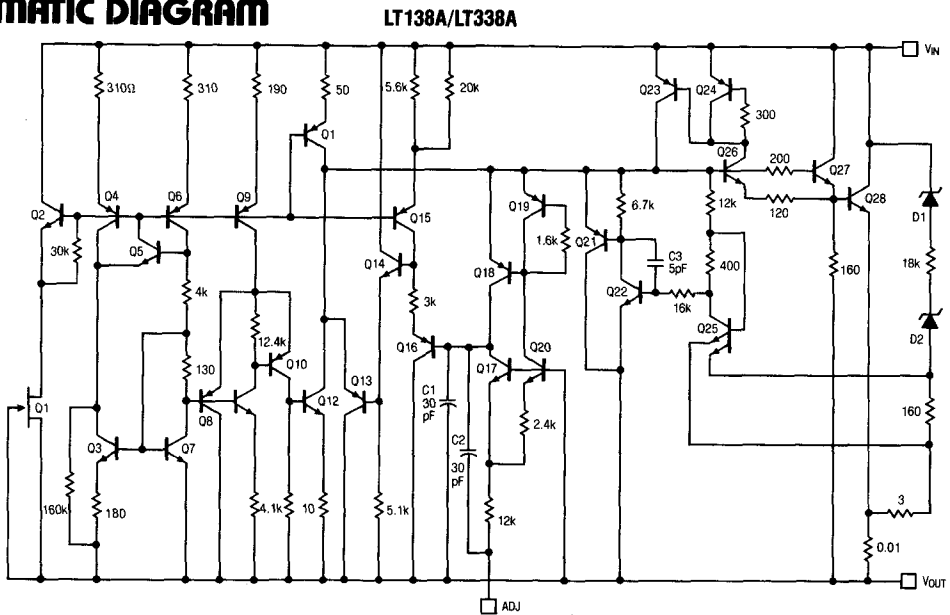
Temperature Compensated Lead Acid Battery Charger



LT138A/LT338A LM138/LM338



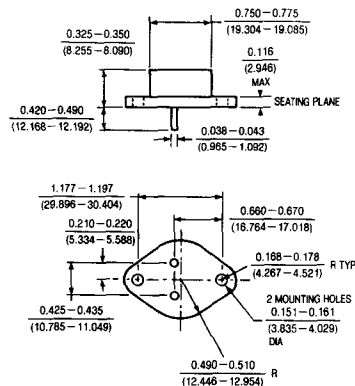
SCHEMATIC DIAGRAM



PACKAGE DESCRIPTION

**K Package To-3
Steel Metal Can**

	T _j max.	θ _{ja}	θ _{jc}
138A 138	150°C	35°C/W	1°C/W
338A 338	125°C	35°C/W	1°C/W



FEATURES

- *Guaranteed* 1% Initial Voltage Tolerance
- *Guaranteed* 3A Output Current
- *Guaranteed* 0.3% Load Regulation
- *Guaranteed* 0.01%/V Line Regulation
- 100% Thermal Limit Burn-in

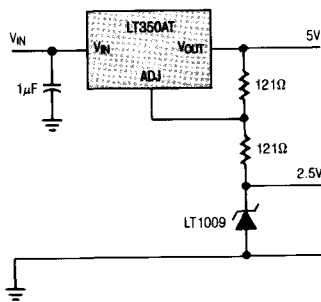
APPLICATIONS

- Improved Linear Regulators
- Adjustable Power Supplies
- Constant Current Regulation
- Battery Chargers

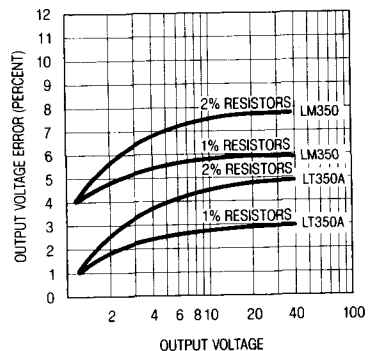
DESCRIPTION

The LT150A Series are 3-terminal positive adjustable voltage regulators which offer improved performance over earlier devices. A major feature of the LT150A/350A is the output voltage tolerance is guaranteed at a maximum of $\pm 1\%$, allowing an overall power supply tolerance to be better than 3% using inexpensive 1% resistors. Line and load regulation performance has been improved as well. Additionally, the LT150A/350A reference voltage is guaranteed not to exceed 2% when operating over the full load, line and power dissipation conditions. The LT150A/350A adjustable regulators offer an improved solution for all positive voltage regulator requirements with load currents up to 3 amps.

Regulator With Reference



Output Voltage Error



LT150A/LT350A LM150/LM350

ABSOLUTE MAXIMUM RATINGS

Power Dissipation Internally Limited
 Input to Output Voltage Differential 35V
 Operating Junction Temperature Range
 LT150A/LM150 -55°C to 150°C
 LT350A/LM350 0°C to 125°C
 Storage Temperature Range
 LT150A/LM150 -65°C to 150°C
 LT350A/LM350 -65°C to 150°C
 Lead Temperature (Soldering, 10 sec.) 300°C

PACKAGE/ORDER INFORMATION

<p>BOTTOM VIEW ADJUSTMENT 1 2 VIN CASE IS OUTPUT K PACKAGE TO-3 METAL CAN (STEEL)</p>	<p>ORDER PART NUMBER</p> <p>LT150AK LT350AK LM150K LM350K</p>
<p>VOUT VIN VOUT ADJ T PACKAGE TO-220 PLASTIC</p>	<p>LT350AT LM350T</p>

PRECONDITIONING:

100% THERMAL LIMIT BURN-IN

ELECTRICAL CHARACTERISTICS (See Note 1)

SYMBOL	PARAMETER	CONDITIONS	LT150A			LM150			UNITS	
			MIN	TYP	MAX	MIN	TYP	MAX		
V _{REF}	Reference Voltage	I _{OUT} = 10mA, T _J = 25°C	1.230	1.250	1.262				V	
		3V ≤ (V _{IN} - V _{OUT}) ≤ 35V 10mA ≤ I _{OUT} ≤ 3A, P ≤ 30W	1.225	1.250	1.270	1.20	1.25	1.30	V	
ΔV _{OUT} /ΔV _{IN}	Line Regulation	3V ≤ (V _{IN} - V _{OUT}) ≤ 35V, (See Note 2)		0.005	0.01		0.005	0.01	%/V	
					0.02	0.05		0.02	0.05	%/V
ΔV _{OUT} /ΔI _{OUT}	Load Regulation	10mA ≤ I _{OUT} ≤ 3A, (See Note 2) T _A = 25°C V _{OUT} ≤ 5V V _{OUT} ≥ 5V		5	15		5	15	mV	
					0.1	0.3		0.1	0.3	%
					15	50		20	50	mV
				0.3	1		0.3	1	%	
	Thermal Regulation	T _A = 25°C, 20msec Pulse		0.002	0.01		0.002	0.01	%/W	
	Ripple Rejection	V _{OUT} = 10V, f = 120Hz C _{ADJ} = 0 C _{ADJ} = 10μF		66	65	66	65	86	dB	
I _{ADJ}	Adjust Pin Current			50	100		50	100	μA	
ΔI _{ADJ}	Adjust Pin Current Change	10mA ≤ I _L ≤ 3A 3V ≤ (V _{IN} - V _{OUT}) ≤ 35V		0.2	5		0.2	5	μA	
	Minimum Load Current	(V _{IN} - V _{OUT}) = 35V		3.5	5		3.5	5	mA	
	Current Limit	(V _{IN} - V _{OUT}) ≤ 10V		3	4.5		3.0	4.5	A	
		(V _{IN} - V _{OUT}) = 30V		0.3	1		0.3	1	A	
ΔV _{OUT} /ΔTemp	Temperature Stability	-55°C ≤ T _J ≤ +150°C					1		%	
ΔV _{OUT} /ΔTime	Long Term Stability	T _A = 125°C		0.3	1		0.3	1	%	
e _n	RMS Output Noise (% of V _{OUT})	T _A = 25°C, 10Hz ≤ f ≤ 10kHz		0.001			0.001		%	
θ _{JC}	Thermal Resistance Junction to Case	K Package			1.5			1.5	°C/W	

ELECTRICAL CHARACTERISTICS (See Note 1)

SYMBOL	PARAMETER	CONDITIONS	LT350A			LM350			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{REF}	Reference Voltage	$I_{OUT} = 10mA, T_J = 25^\circ C$	1.238	1.250	1.262				V
		$3V \leq (V_{IN} - V_{OUT}) \leq 35V$ $10mA \leq I_{OUT} \leq 3A, P \leq 30W$	● 1.225	1.250	1.270	1.20	1.25	1.30	V
$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	Line Regulation	$3V \leq (V_{IN} - V_{OUT}) \leq 35V$, (See Note 2) $T_A = 25^\circ C$		0.005 0.02	0.01 0.05		0.005 0.02	0.03 0.07	%/V %/V
$\frac{\Delta V_{OUT}}{\Delta I_{OUT}}$	Load Regulation	$10mA \leq I_{OUT} \leq 3A$, (See Note 2) $T_A = 25^\circ C$ $V_{OUT} \leq 5V$ $V_{OUT} \geq 5V$		5 6.1	15 0.3		5 0.1	25 0.5	mV %
		$V_{OUT} \leq 5V$ $V_{OUT} \geq 5V$	● 15 ● 0.3	60 1		20 0.3	70 1.5	mV %	
	Thermal Regulation	$T_A = 25^\circ C$, 20msec Pulse		0.002	0.01		0.002	0.03	%/W
	Ripple Rejection	$V_{OUT} = 10V, f = 120Hz$ $C_{ADJ} = 0$ $C_{ADJ} = 10\mu F$	● 66	65 86		66	65 86		dB dB
I_{ADJ}	Adjust Pin Current		●	50	100		50	100	μA
ΔI_{ADJ}	Adjust Pin Current Change	$10mA \leq I_{OUT} \leq 3A$ $3V \leq (V_{IN} - V_{OUT}) \leq 35V$	●	0.2	5		0.2	5	μA
	Minimum Load Current	$(V_{IN} - V_{OUT}) \leq 35V$	●	3.5	10		3.5	10	mA
	Current Limit	$(V_{IN} - V_{OUT}) \leq 10V$	●	3	4.5		3	4.5	A
		$(V_{IN} - V_{OUT}) = 30V, T_J = 25^\circ C$	●	0.25	1		0.25	1	A
$\frac{\Delta V_{OUT}}{\Delta Temp}$	Temperature Stability		●	1	2		1		%
$\frac{\Delta V_{OUT}}{\Delta Time}$	Long Term Stability	$T_A = 125^\circ C$		0.3	1		0.3	1	%
e_n	RMS Output Noise (% of V_{OUT})	$T_A = 25^\circ C, 10Hz \leq f \leq 10kHz$		0.001			0.001		%
θ_{JC}	Thermal Resistance Junction to Case	K Package		1.2	1.5		1.2	1.5	$^\circ C/W$
		T Package		3	4		3	4	$^\circ C/W$

The ● denotes the specifications which apply over the full operating temperature range.

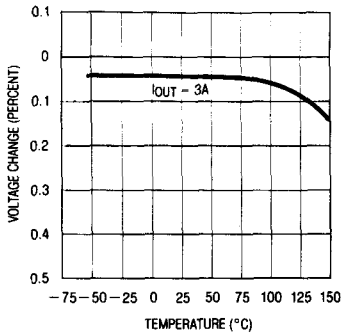
Note 1: Unless otherwise specified, these specifications apply for $V_{IN} - V_{OUT} = 5V$ and $I_{OUT} = 1.5A$. These specifications are applicable for power dissipations up to 30W for the K package and up to 25W for the T package. Power dissipation is guaranteed at these values up to 15 Volts input-output differential. Above 15 Volts input-output differential power dissipation is limited by device internal protection circuitry.

Note 2: Regulation is measured at a constant T_J . Changes in output due to heating must be taken into account separately. Pulse testing with low duty cycle is used.

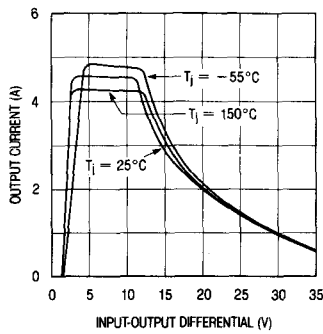
4

TYPICAL PERFORMANCE CHARACTERISTICS

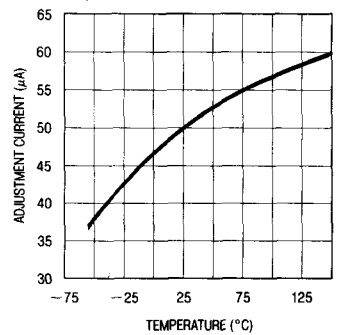
Load Regulation



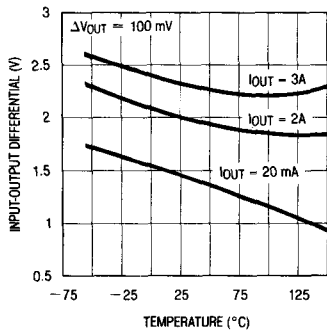
Current Limit



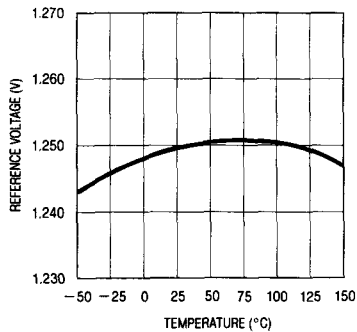
Adjustment Current



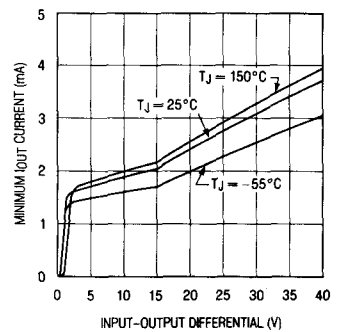
Dropout Voltage



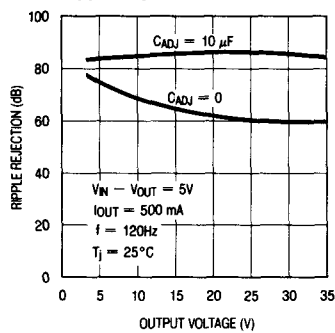
Temperature Stability



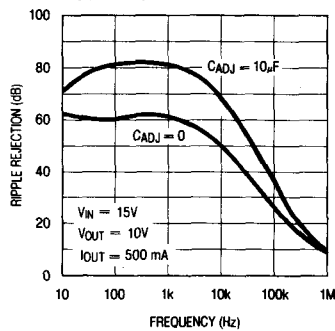
Minimum Operating Current



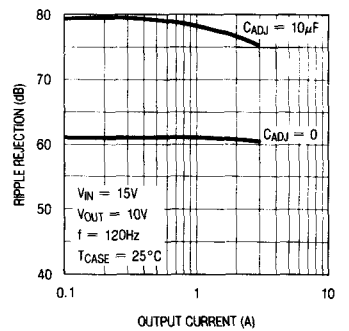
Ripple Rejection



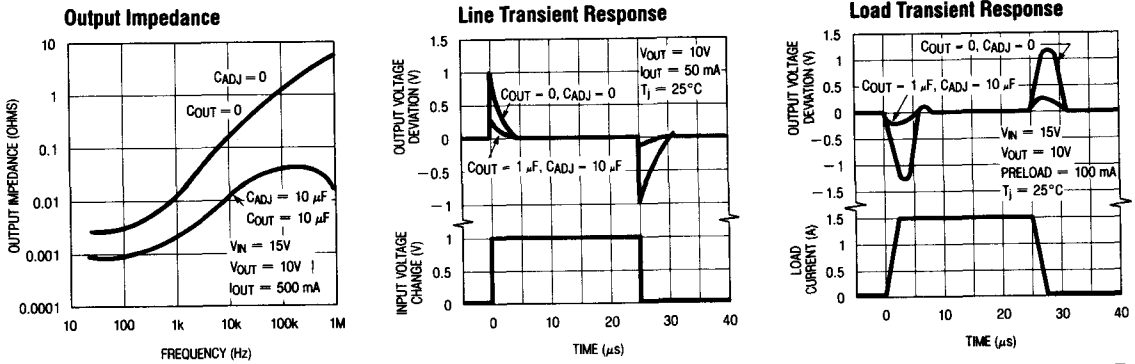
Ripple Rejection



Ripple Rejection



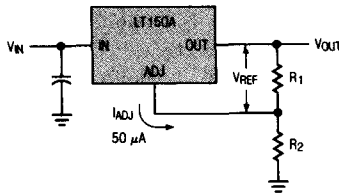
TYPICAL PERFORMANCE CHARACTERISTICS



APPLICATION INFORMATION

General

The LT150A develops a 1.25V reference voltage between the output and the adjustable terminal (see Figure 1). By placing a resistor, R₁, between these two terminals, a constant current is caused to flow through R₁ and down through R₂ to set the overall output voltage. Normally this current is the specified minimum load current of 5mA or 10mA.



$$V_{OUT} = V_{REF} \left(1 + \frac{R_2}{R_1} \right) + I_{ADJ} R_2$$

Basic Adjustable Regulator
Figure 1

Because I_{ADJ} is very small and constant when compared with the current through R₁, it represents a small error and can usually be ignored. It is easily seen from the above equation, that even if the resistors were of exact value, the accuracy of the output is limited by the accuracy of V_{REF}. Earlier adjustable regulators had a reference tolerance of ±4% which is

dangerously close to the ±5% supply tolerance required in many logic and analog systems. Further, even 1% resistors can drift 0.01%/°C, adding additional error to the output voltage tolerance.

For example, using 2% resistors and ±4% tolerance for V_{REF}, calculations will show that the expected range of a 5V regulator design would be 4.66V ≤ V_{OUT} ≤ 5.36V or approximately ±7%. If the same example were used for a 15V regulator, the expected tolerance would be ±8%. With these results most applications required some method of trimming, usually a trim pot. This solution is both expensive and not conducive to volume production.

One of the enhancements of Linear Technology's adjustable regulators over existing devices is the tightened initial tolerance of V_{REF}. This allows relatively inexpensive 1% or 2% film resistors to be used for R₁ and R₂ to set the output voltage within an acceptable tolerance.

With a guaranteed 1% reference, a 5V power supply design, using ±2% resistors, would have a worst case manufacturing tolerance of ±4%. If 1% resistors were used, the tolerance would drop to ±2.5%. A plot of the worst case output voltage tolerance as a function of resistor tolerance is shown on the front page.

LT150A/LT350A LM150/LM350

For convenience, a table of standard 1% resistor values is shown below.

Table of ½% and 1% Standard Resistance Values

1.00	1.47	2.15	3.16	4.64	6.81
1.02	1.50	2.21	3.24	4.75	6.98
1.05	1.54	2.26	3.32	4.87	7.15
1.07	1.58	2.32	3.40	4.99	7.32
1.10	1.62	2.37	3.48	5.11	7.50
1.13	1.65	2.43	3.57	5.23	7.68
1.15	1.69	2.49	3.65	5.36	7.87
1.18	1.74	2.55	3.74	5.49	8.06
1.21	1.78	2.61	3.83	5.62	8.25
1.24	1.82	2.67	3.92	5.76	8.45
1.27	1.87	2.74	4.02	5.90	8.66
1.30	1.91	2.80	4.12	6.04	8.87
1.33	1.96	2.87	4.22	6.19	9.09
1.37	2.00	2.94	4.32	6.34	9.31
1.40	2.05	3.01	4.42	6.49	9.53
1.43	2.10	3.09	4.53	6.65	9.76

Standard Resistance Values are obtained from the Decade Table by multiplying by multiples of 10. As an example, 1.21 can represent 1.21Ω, 12.1Ω, 121Ω, 1.21KΩ etc.

Bypass Capacitors

Input bypassing using a 1μF tantalum or 25μF electrolytic is recommended when the input filter capacitors are more than 5 inches from the device. Improved ripple rejection (80 dB) can be accomplished by adding a 10μF capacitor from the adjust pin to ground. Increasing the size of the capacitor to 20μF will help ripple rejection at low output voltage since the reactance of this capacitor should be small compared to the voltage setting resistor, R2. For improved AC transient response and to prevent the possibility of oscillation due to unknown reactive load, a 1μF capacitor is also recommended at the output. Because of their low impedance at high frequencies, the best type of capacitor to use is solid tantalum.

Protection Diodes

The LT150A/350A do not require a protection diode from the adjustment terminal to the output (see Figure 2). Improved internal circuitry eliminates the need for this diode when the adjustment pin is bypassed with a capacitor to improve ripple rejection.

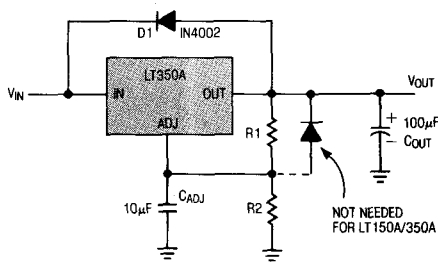


Figure 2

If a very large output capacitor is used, such as a 100μF shown in Figure 2, the regulator could be damaged or destroyed if the input is accidentally shorted to ground or crowbarred, due to the output capacitor discharging into the output terminal of the regulator. To prevent this, a diode D1 as shown, is recommended to safely discharge the capacitor.

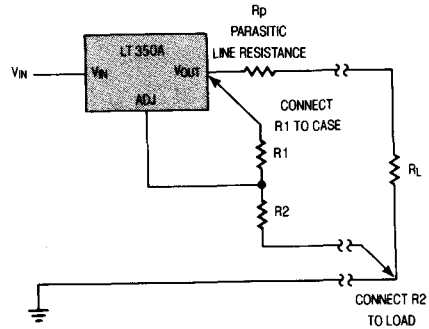
Load Regulation

Because the LT150A is a three-terminal device, it is not possible to provide true remote load sensing. Load regulation will be limited by the resistance of the wire connecting the regulator to the load. The data sheet specification for load regulation is measured at the bottom of the package. Negative side sensing is a true Kelvin connection, with the bottom of the output divider returned to the negative side of the load. Although it may not be immediately obvious, best load regulation is obtained when the top of the resistor divider (R1) is connected *directly* to the case *not to the load*. This is illustrated in Figure 3. If R1 were connected to the load, the effective resistance between the regulator and the load would be

$$R_p \times \left(\frac{R_2 + R_1}{R_1} \right), R_p = \text{Parasitic Line Resistance.}$$

Connected as shown, R_p is not multiplied by the divider ratio. R_p is about 0.004Ω per foot using 16 gauge wire. This translates to 4mV/ft at 1A load current, so it

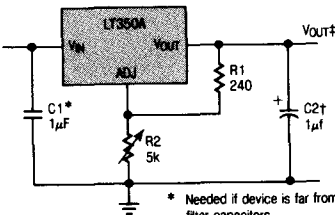
is important to keep the positive lead between regulator and load as short as possible, and use large wire or PC board traces.



Connections for Best Load Regulation
Figure 3

TYPICAL APPLICATIONS

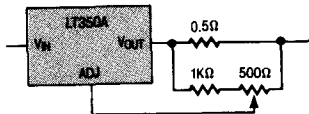
1.2V–25V Adjustable Regulator



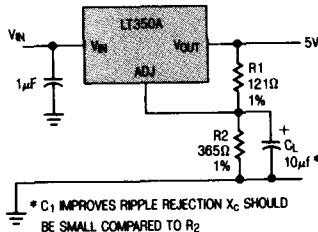
* Needed if device is far from filter capacitors

† Optional—improves transient response ‡ $V_{OUT} = 1.25V \left(1 + \frac{R_2}{R_1}\right)$

Adjustable Current Limiter

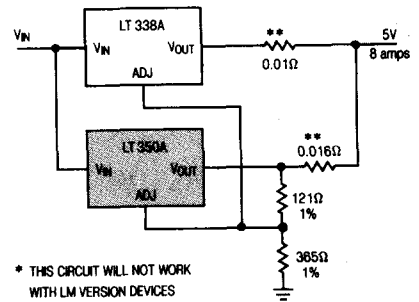


Improving Ripple Rejection



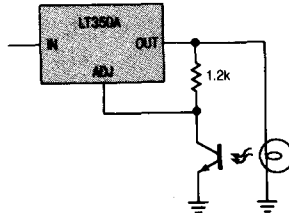
* C_L IMPROVES RIPPLE REJECTION X_C SHOULD BE SMALL COMPARED TO R_2

*Parallel Regulators for Higher Current

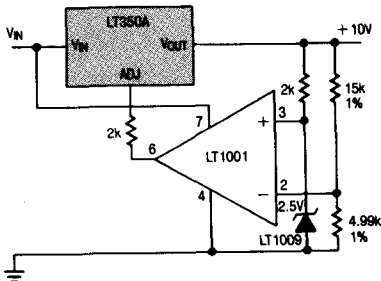


* THIS CIRCUIT WILL NOT WORK WITH LM VERSION DEVICES BECAUSE OF WIDER REFERENCE VOLTAGE LIMITS
** CURRENT SHARING RESISTORS DEGRADE REGULATION TO 1%

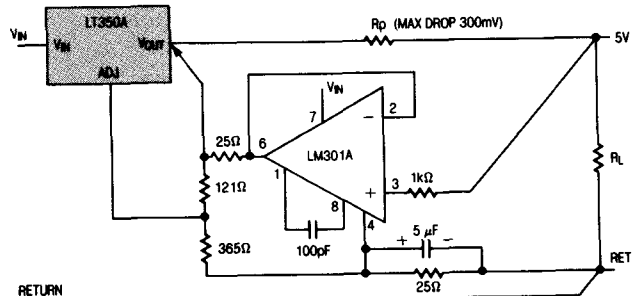
Automatic Light Control



Precision High Current Reference



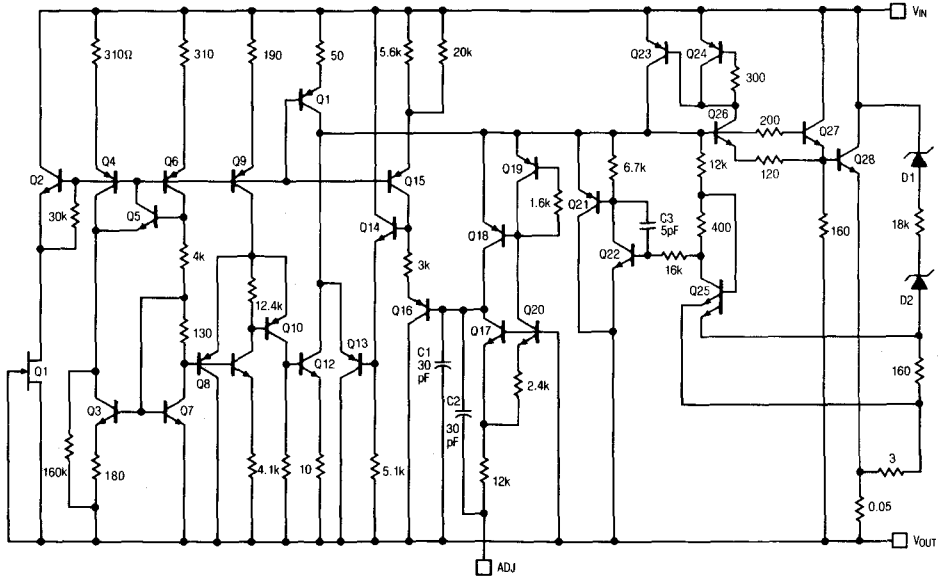
Remote Sensing



LT150A/LT350A LM150/LM350

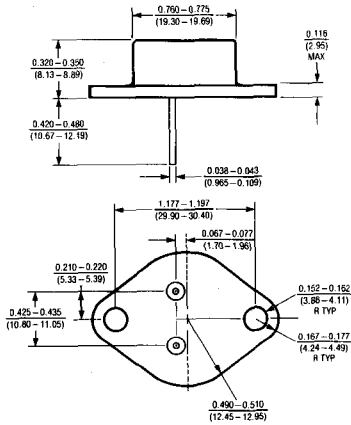
SCHEMATIC DIAGRAM

LT150A/LT350A



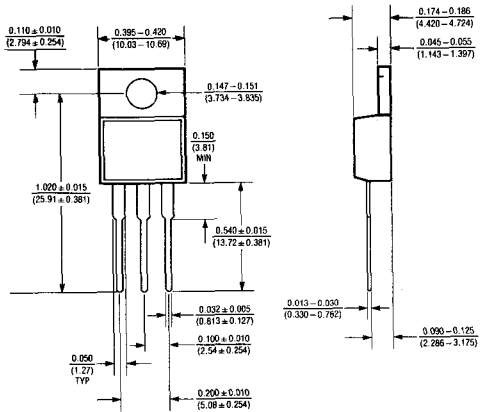
PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

K Package TO-3 STEEL Metal Can



	T _j max.	θ _{ja}	θ _{jc}
LT150A LM150	150°C	35°C/W	1.5°C/W
LT350A LM350	125°C	35°C/W	1.5°C/W

T Package TO-220 Plastic



	T _j max.	θ _{ja}	θ _{jc}
LT350A LM350	125°C	50°C/W	2.5°C/W

SECTION 5—SWITCHING REGULATORS/ VOLTAGE CONVERTERS

SECTION 5—SWITCHING REGULATORS AND VOLTAGE CONVERTERS

INDEX	5-2
PROPRIETARY PRODUCTS	
<i>LT1026, Voltage Converter</i>	5-3
<i>LTC1044/7660, Switched Capacitor Voltage Converter</i>	5-9
<i>LTC1044CS8, Switched Capacitor Voltage Converter</i>	5-21
<i>LT1054, Switched Capacitor Voltage Converter with Regulator</i>	5-23
<i>LT1054CS/LT1054IS, Switched Capacitor Voltage Converter with Regulator</i>	5-35
<i>LT1070, 5A High Efficiency Switching Regulator</i>	5-37
<i>LT1071, 2.5A High Efficiency Switching Regulator</i>	5-37
<i>LT1072, 1.25A High Efficiency Switching Regulator</i>	5-49
<i>LT1074, Switching Regulator</i>	13-21
<i>LT1170, 5A High Efficiency 100kHz Switching Regulator</i>	5-61
<i>LT1171, 2.5A High Efficiency 100kHz Switching Regulator</i>	5-61
<i>LT1172, 1.25A High Efficiency 100kHz Switching Regulator</i>	5-73
ENHANCED AND SECOND SOURCE PRODUCTS	
<i>SG1524/SG3524, Regulating Pulse Width Modulators</i>	5-85
<i>SG3524S, Regulating Pulse Width Modulator</i>	5-93
<i>LT1524/LT3524, Regulating Pulse Width Modulators</i>	5-85
<i>SG1525A/SG3525A, Regulating Pulse Width Modulators</i>	5-97
<i>LT1525A/LT3525A, Regulating Pulse Width Modulators</i>	5-97
<i>LT1526/LT3526, Regulating Pulse Width Modulators</i>	5-105
<i>SG1527A/SG3527A, Regulating Pulse Width Modulators</i>	5-97
<i>LT1527A/LT3527A, Regulating Pulse Width Modulators</i>	5-97
<i>LT1846/LT1847, Current Mode PWM Controller</i>	5-113
<i>LT3846/LT3847, Current Mode PWM Controller</i>	5-113

FEATURES

- Generates + and - from Single Input
- Up to $\pm 18V$ Output
- Only Needs Four $1\mu F$ Capacitors
- No Inductors
- 10mA Output Current Min
- Operates Down to 4V
- No Latch Up
- 8 Pin Minidip

APPLICATIONS

- Line Drivers
- Op Amp Supplies
- Battery Splitters
- RS232 Power

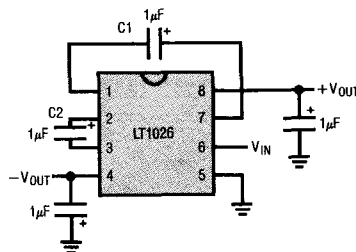
DESCRIPTION

The LT1026 is a switched capacitor voltage doubler and inverter on a single monolithic die. Capable of operating from 4V to 10V input, it provides $\pm 7V$ to $\pm 18V$ out. Output currents of over 10mA are available. Two charge pumps first double the input voltage then invert the doubled voltage. Manufactured in bipolar technology, the LT1026 is not susceptible to latch up and generates up to 36V.

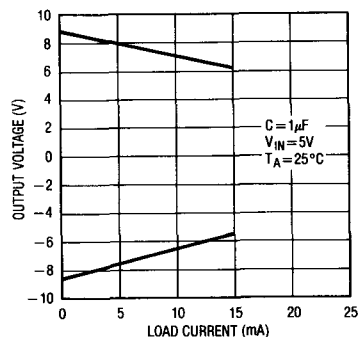
The LT1026 offers a convenient way of generating additional system voltages without using inductors. Powering interface circuits, op amps or data acquisition circuitry off logic supplies is simplified. Other Linear Technology voltage converters such as the low power LTC1044 CMOS and 100mA bipolar LT1054 are available.

TYPICAL APPLICATION

Voltage Doubler and Inverter



Output Voltage



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	10V
V+20V
V-	-20V
Short Circuit Duration	10 seconds
Operating Temperature Range	
LT1026M	-55°C to 125°C
LT1026C	0°C to 70°C
Lead Temperature (Soldering, 10 sec.)	300°C

PACKAGE/ORDER INFORMATION

<p>TOP VIEW</p> <p>J PACKAGE 8-LEAD CERAMIC DIP</p> <p>N PACKAGE 8-LEAD PLASTIC DIP</p> <p>TOP VIEW</p> <p>H PACKAGE 8-LEAD TO-5 METAL CAN</p>	ORDER PART NUMBER
	LT1026MJ LT1026CJ LT1026CN
	LT1026MH LT1026CH

ELECTRICAL CHARACTERISTICS

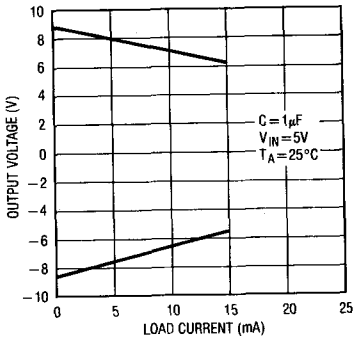
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	
Output Voltage	$V_{IN} = 4V$ (Note 1)	$I_L = 0$ Positive	● 6.5	7		V
		$I_L = 0$ Negative	● -6	-6.7		V
		$I_L = 10mA$ Positive	● 5.25	5.7		V
		$I_L = -10mA$ Negative	● -4.5	-5		V
	$V_{IN} = 5V$	$I_L = 15mA$ Positive	● 6.25	7		V
		$I_L = -15mA$ Negative	● -5.5	-6.2		V
	$V_{IN} = 10V$	$I_L = 0$ Positive	● 18	18.5		V
		$I_L = 0$ Negative	● -17.7	-18		V
		$I_L = 10mA$ Positive	● 16	17.6		V
		$I_L = -10mA$ Negative	● -15.3	-17		V
		$I_L = 15mA$ Positive	● 15.25	17		V
		$I_L = -15mA$ Negative	● -14.5	-16.5		V
$V_{IN} = 5V$	$I_L = 10mA, -10mA$ Positive	● 6.25	7.2		V	
	Negative	● -5.5	-6.5		V	
$V_{IN} = 10V$	$I_L = 10mA, -10mA$ Positive	● 15	16.8		V	
	Negative	● -14.25	-15.75		V	
Supply Current	$V_{IN} = 4V$ $I_L = 0$	●	7	12.5	mA	
	$V_{IN} = 10V$ $I_L = 0$	●	15	30	mA	

The ● denotes specifications which apply over 0°C to 70°C for commercial or -55°C to 125°C for military grade devices. Loads are applied to individual outputs unless otherwise marked.

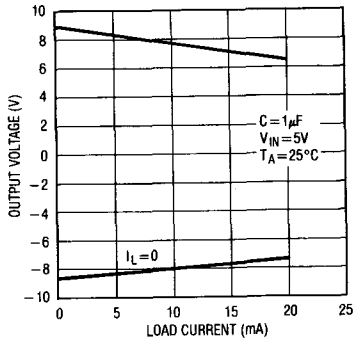
Note 1: V_{IN} Min = -4.5V for $T_A \leq 40^\circ C$

TYPICAL PERFORMANCE CHARACTERISTICS

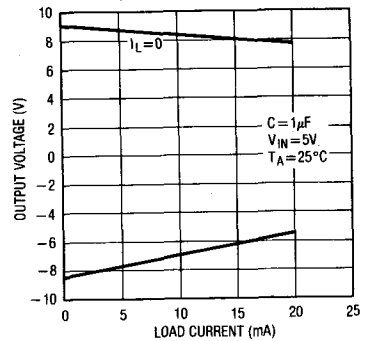
Load Regulation (Both Outputs Loaded)



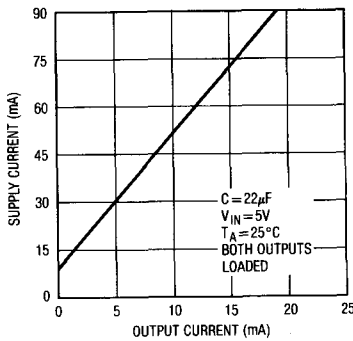
Load Regulation for Positive Loading



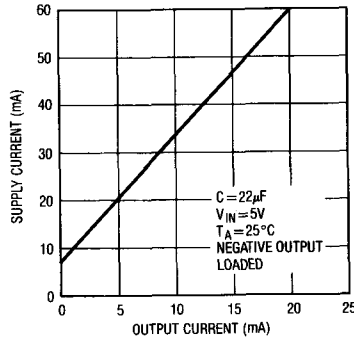
Load Regulation for Negative Loading



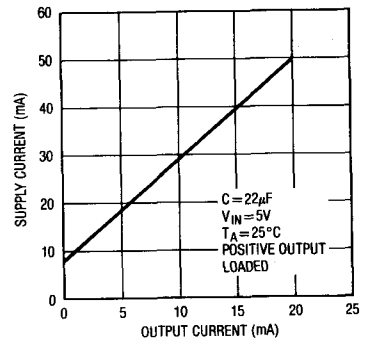
Supply Current



Supply Current

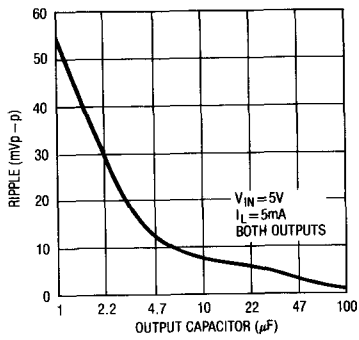


Supply Current

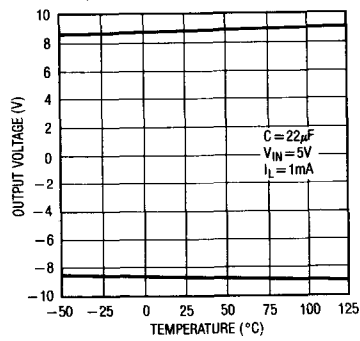


5

Ripple



Output Voltage vs Temperature



APPLICATION HINTS

The LT1026 is a non-regulating voltage converter which converts a single input voltage into both a positive and negative output at up to 15mA. A positive input voltage is first doubled and then the doubled voltage is inverted. The voltage output level is dependent on both the input voltage and the output loading. The total output current available depends on the individual loading of the outputs since loading on one output affects the load and the voltage of the other.

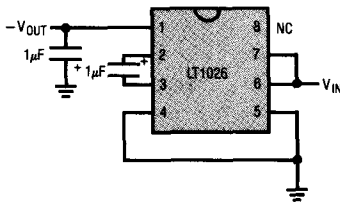
Only four external components are needed for operation. Two charge pump capacitors and two output storage capacitors. Nominal value for these capacitors is 1 μ F, but the LT1026 will operate (with reduced performance) down to 0.1 μ F. Higher value capacitors (22 μ F) will reduce ripple and slightly lower output impedance. For higher output currents the outputs of several converters may be paralleled with common output capacitors.

The substrate diodes are an inherent part of the IC, and must always be reversed biased to isolate the individual transistors. In the LT1026 the substrate is tied to the negative output. If the negative output is not used, such as when only the voltage doubler output is needed, the $-V_{OUT}$ must be tied to ground so the substrate diodes are properly biased. The substrate diodes must never become forward biased even during overload conditions. For example, pulling the $-V_{OUT}$ positive with respect to ground can forward bias the substrate diodes. Clamping the substrate to ground with an external diode would be needed to ensure proper operation and prevent the substrate from carrying any current.

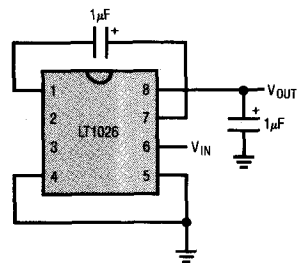
No overload protection is included on the LT1026. Neither output is damaged by momentary shorts, but during sustained shorts the resulting high current flow will overheat the IC.

TYPICAL APPLICATIONS

Positive to Negative Converter

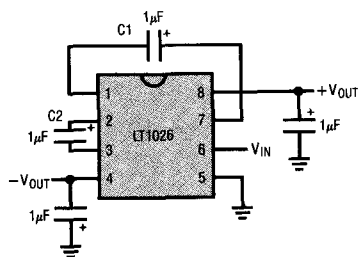


Voltage Doubler

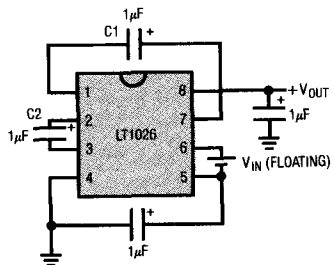


TYPICAL APPLICATIONS

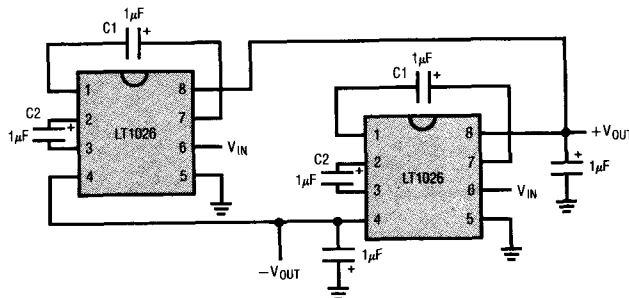
Standard Configuration Voltage Doubler and Inverter



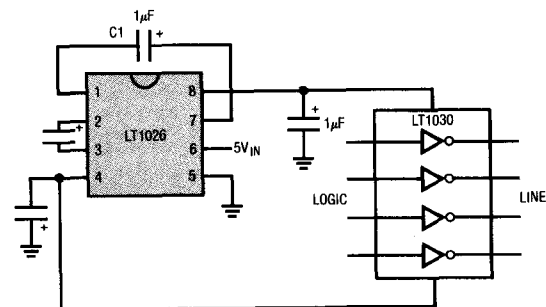
Voltage Quadrupler



Parallel Converters for Higher Output Current and Lower Output Impedance



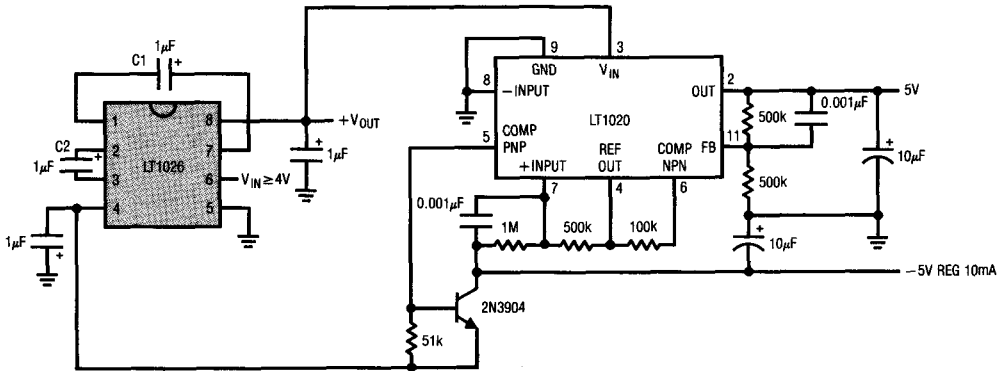
5V Powered RS232 Line Driver



5

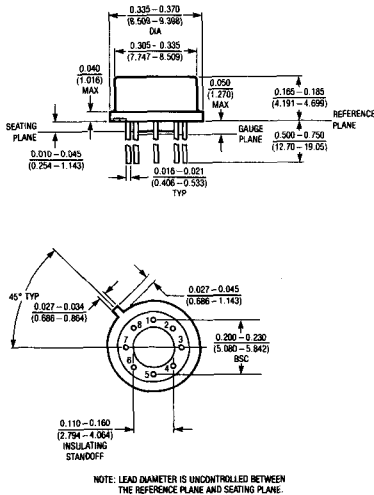
TYPICAL APPLICATIONS

Regulated Converter

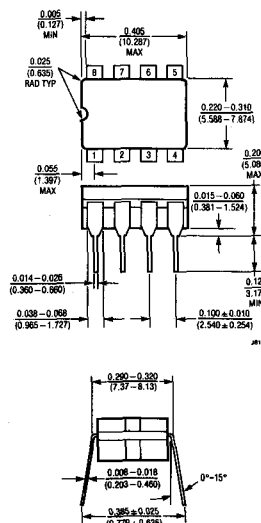


PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

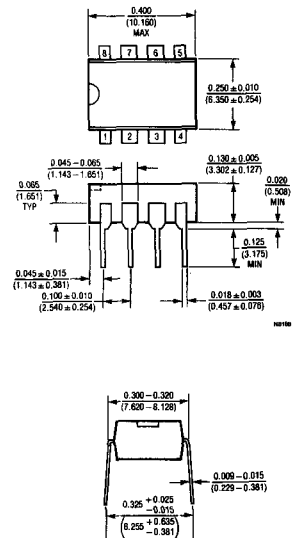
H Package
8-Lead TO-5 Metal Can



J Package
8-Lead Ceramic DIP



N Package
8-Lead Plastic DIP



Switched Capacitor Voltage Converter

FEATURES

- Plug-In Compatible with 7660 with These Additional Features:
 - *Guaranteed* Operation to 9V, with No External Diode, Over Full Temperature Range
 - Boost Pin (Pin 1) for Higher Switching Frequency
 - Lower Quiescent Power
 - Efficient Voltage Doubler
- 200 μ A *Max.* No Load Supply Current at 5V
- 97% *Min.* Open Circuit Voltage Conversion Efficiency
- 95% *Min.* Power Conversion Efficiency
- Wide Operating Supply Voltage Range, 1.5V to 9V
- Easy to Use
- Commercial Device *Guaranteed* Over -40°C to 85°C Temperature Range

APPLICATIONS

- Conversion of +5V to $\pm 5\text{V}$ Supplies
- Precise Voltage Division, $V_{\text{OUT}} = V_{\text{IN}} / 2 \pm 20\text{ppm}$
- Voltage Multiplication, $V_{\text{OUT}} = \pm nV_{\text{IN}}$
- Supply Splitter, $V_{\text{OUT}} = \pm V_{\text{S}} / 2$

DESCRIPTION

The LTC1044 is a monolithic CMOS switched capacitor voltage converter which is manufactured using Linear Technology's enhanced LTCMOS™ silicon gate process. The LTC1044 provides several voltage conversion functions: the input voltage can be inverted ($V_{\text{OUT}} = -V_{\text{IN}}$), doubled ($V_{\text{OUT}} = 2V_{\text{IN}}$), divided ($V_{\text{OUT}} = V_{\text{IN}} / 2$) or multiplied ($V_{\text{OUT}} = \pm nV_{\text{IN}}$).

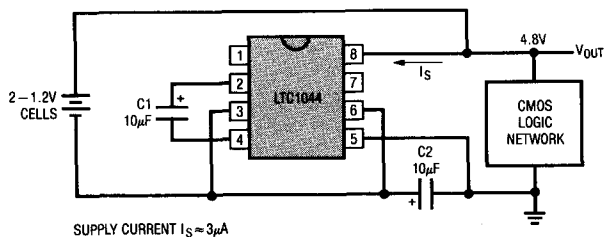
Designed to be pin-for-pin and functionally compatible with the popular 7660, the LTC1044 provides significant features and improvements over earlier 7660 designs. These improvements include: full 1.5V to 9V supply operation over the entire operating temperature range, without the need for external protection diodes; 2½ times lower quiescent current for greater power conversion efficiency; and a "boost" function which is available to raise the internal oscillator frequency to optimize performance in specific applications.

Although the LTC1044 provides significant design and performance advantages over the earlier 7660 device, it still maintains its compatibility with existing 7660 designs.

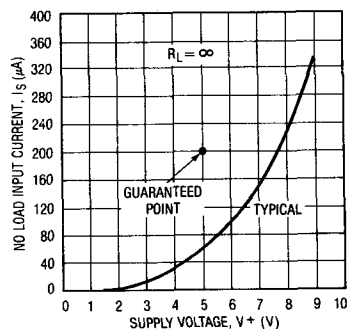
LTCMOS™ is a trademark of Linear Technology Corp.

5

Generating CMOS Logic Supply from 2 Mercury Batteries



Supply Current vs Supply
Voltage

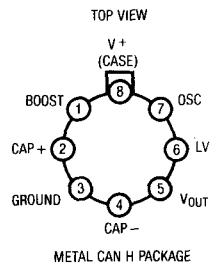
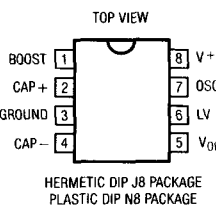


ABSOLUTE MAXIMUM RATINGS

(Notes 1 and 2)

Supply Voltage	9.5V
Input Voltage on Pins 1, 6 and 7	
(Note 2)	$-0.3V \leq V_{IN} \leq V^+ + 0.3V$
Current into Pin 6	20 μ A
Output Short Circuit Duration	
($V^+ \leq 5.5V$)	Continuous
Operating Temperature Range	
LTC1044C	$-40^\circ C \leq T_A \leq 85^\circ C$
LTC1044M	$-55^\circ C \leq T_A \leq 125^\circ C$
Storage Temperature Range	$-65^\circ C$ to $+150^\circ C$
Lead Temperature (Soldering, 10 sec.)	300 $^\circ C$

PACKAGE/ORDER INFORMATION

 <p>TOP VIEW</p> <p>METAL CAN H PACKAGE</p>	ORDER PART NUMBER
	LTC1044CH LTC1044MH
 <p>TOP VIEW</p> <p>HERMETIC DIP J8 PACKAGE PLASTIC DIP N8 PACKAGE</p>	LTC1044CJ8 LTC1044CN8 LTC1044MJ8

ELECTRICAL CHARACTERISTICS $V^+ = 5V$, $T_A = 25^\circ C$, Test Circuit Figure 1, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	LTC1044M			LTC1044C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
I_S	Supply Current	$R_L = \infty$, Pins 1 and 7 No Connection $R_L = \infty$, Pins 1 and 7 $V^+ = 3V$		60 20	200		60 20	200	μ A μ A
V^+_{L}	Minimum Supply Voltage	$R_L = 10k$	● 1.5			1.5			V
V^+_{H}	Maximum Supply Voltage	$R_L = 10k$ (Note 3)	●		9			9	V
R_{OUT}	Output Resistance	$I_L = 20mA$, $f_{OSC} = 5kHz$ $V^+ = 2V$, $I_L = 3mA$, $f_{OSC} = 1kHz$	●		100 150 400	●		100 130 325	Ω Ω Ω
f_{OSC}	Oscillator Frequency	$C_{OSC} = 1pF$ (Note 4) $V^+ = 5V$ $V^+ = 2V$	● ●	5 1		5 1			kHz kHz
P_{EFF}	Power Efficiency	$R_L = 5k\Omega$, $f_{OSC} = 5kHz$		95	98		95	98	%
V_{OUTEFF}	Voltage Conversion Efficiency	$R_L = \infty$		97	99.9		97	99.9	%
I_{OSC}	Oscillator Sink or Source Current	$V_{OSC} = 0V$ or V^+ Pin 1 = 0V Pin 1 = V^+	● ●		3 20		3 20		μ A μ A

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: Absolute Maximum Ratings are those values beyond which the life of the device may be impaired.

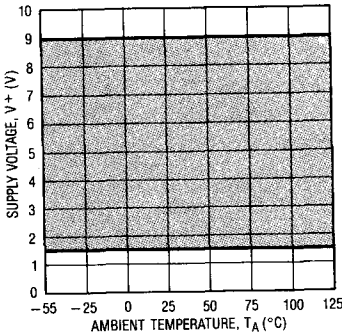
Note 2: Connecting any input terminal to voltages greater than V^+ or less than ground may cause destructive latch-up. It is recommended that no inputs from sources operating from external supplies be applied prior to power-up of the LTC1044.

Note 3: The LTC1044 is guaranteed to operate with alkaline, mercury or NiCad 9V batteries, even though the initial battery voltage may be slightly higher than 9.0V.

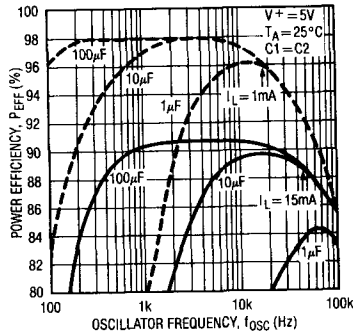
Note 4: f_{OSC} is tested with $C_{OSC} = 100pF$ to minimize the effects of test fixture capacitance loading. The 1pF frequency is correlated to this 100pF test point, and is intended to simulate the capacitance at pin 7 when the device is plugged into a test socket and no external capacitor is used.

TYPICAL PERFORMANCE CHARACTERISTICS (Using Test Circuit Shown in Figure 1)

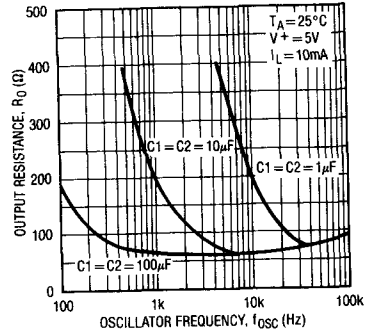
Operating Voltage Range vs Temperature



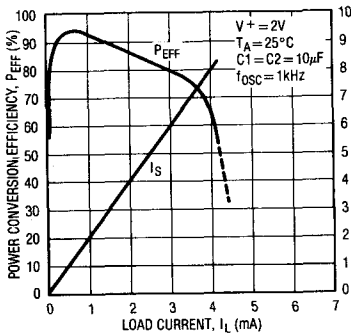
Power Efficiency vs Oscillator Frequency



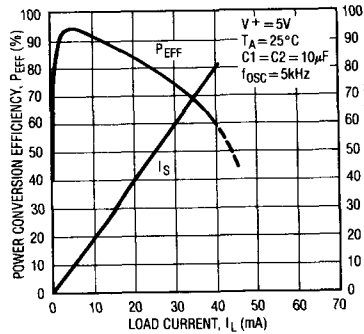
Output Resistance vs Oscillator Frequency



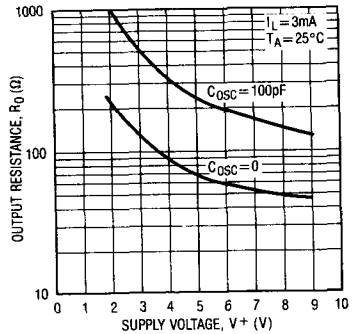
Power Conversion Efficiency vs Load Current for V+ = 2V



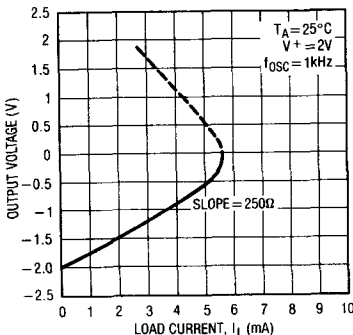
Power Conversion Efficiency vs Load Current for V+ = 5V



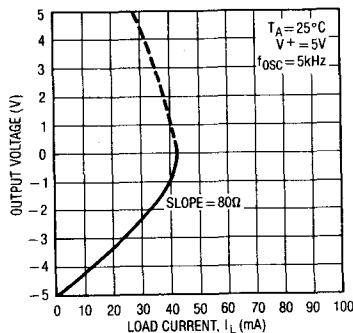
Output Resistance vs Supply Voltage



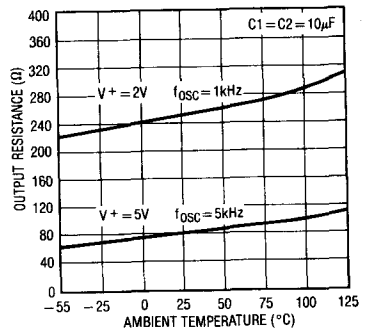
Output Voltage vs Load Current for V+ = 2V



Output Voltage vs Load Current for V+ = 5V



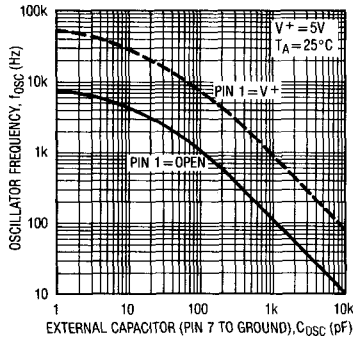
Output Resistance vs Temperature



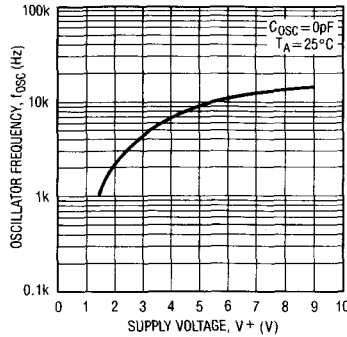
5

TYPICAL PERFORMANCE CHARACTERISTICS (Using Test Circuit Shown in Figure 1)

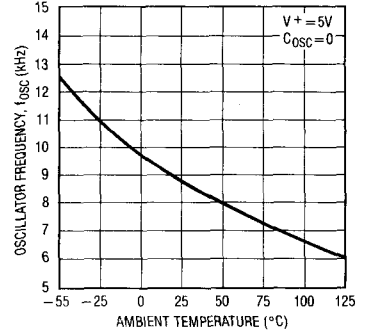
Oscillator Frequency as a Function of C_{OSC}



Oscillator Frequency vs Supply Voltage



Oscillator Frequency vs Temperature



TEST CIRCUIT

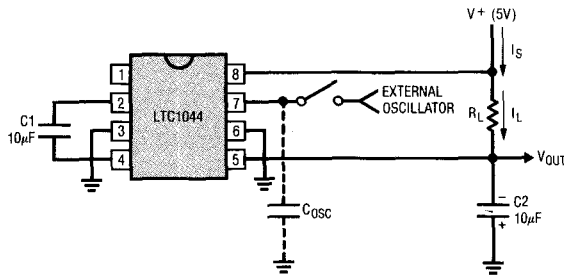


Figure 1

APPLICATIONS INFORMATION

Theory of Operation

To understand the theory of operation of the LTC1044, a review of a basic switched capacitor building block is helpful.

In Figure 2, when the switch is in the left position, capacitor C1 will charge to voltage V1. The total charge on C1 will be $q_1 = C1V_1$. The switch then moves to the right, discharging C1 to voltage V2. After this discharge time, the charge on C1 is $q_2 = C1V_2$. Note that charge has been transferred from the source, V1, to the output, V2. The amount of charge transferred is:

$$\Delta q = q_1 - q_2 = C1(V_1 - V_2).$$

If the switch is cycled f times per second, the charge transfer per unit time (i.e., current) is:

$$I = f \times \Delta q = f \times C1(V_1 - V_2).$$

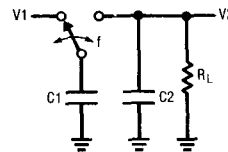


Figure 2. Switched Capacitor Building Block

APPLICATIONS INFORMATION

Rewriting in terms of voltage and impedance equivalence,

$$I = \frac{V1 - V2}{(1/fC1)} = \frac{V1 - V2}{R_{EQUIV}}$$

A new variable, R_{EQUIV} , has been defined such that $R_{EQUIV} = 1/fC1$. Thus, the equivalent circuit for the switched capacitor network is as shown in Figure 3.

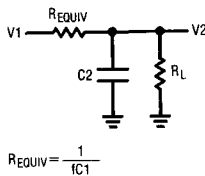


Figure 3. Switched Capacitor Equivalent Circuit

Examination of Figure 4 shows that the LTC1044 has the same switching action as the basic switched capacitor building block. With the addition of finite switch on-resistance and output voltage ripple, the simple theory, although not exact, provides an intuitive feel for how the device works.

For example, if you examine power conversion efficiency as a function of frequency (see typical curve), this simple theory will explain how the LTC1044 behaves. The loss, and hence the efficiency, is set by the output impedance. As frequency is decreased, the output impedance will eventually be dominated by the $1/fC1$ term and power efficiency will drop. The typical curves for power efficiency versus frequency show this effect for various capacitor values.

Note also that power efficiency decreases as frequency goes up. This is caused by internal switching losses which occur due to some finite charge being lost on each switching cycle. This charge loss per unit cycle, when multiplied by the switching frequency, becomes a current loss. At high frequency this loss becomes significant and the power efficiency starts to decrease.

LV (Pin 6)

The internal logic of the LTC1044 runs between V^+ and LV (pin 6). For V^+ greater than or equal to 3V, an internal switch shorts LV to GND (pin 3). For V^+ less than 3V, the LV pin should be tied to GND. For V^+ greater than or equal to 3V, the LV pin can be tied to GND or left floating.

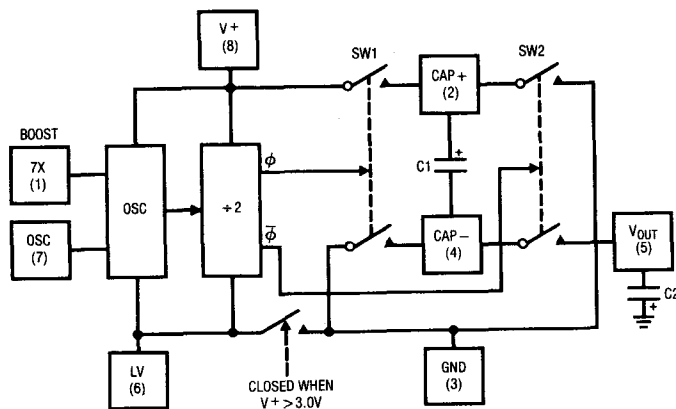


Figure 4. LTC1044 Switched Capacitor Voltage Converter Block Diagram

APPLICATIONS INFORMATION

OSC (Pin 7) and Boost (Pin 1)

The switching frequency can be raised, lowered or driven from an external source. Figure 5 shows a functional diagram of the oscillator circuit.

By connecting the boost pin (pin 1) to V^+ , the charge and discharge current is increased and, hence, the frequency is increased by approximately 7 times. Increasing the frequency will decrease output impedance and ripple for higher load currents.

Loading pin 7 with more capacitance will lower the frequency. Using the boost (pin 1) in conjunction with external capacitance on pin 7 allows user selection of the frequency over a wide range.

Driving the LTC1044 from an external frequency source can be easily achieved by driving pin 7 and leaving the boost pin open, as shown in Figure 6. The output current from pin 7 is small, typically $0.5\mu A$, so a logic gate is capable of driving this current. The choice of using a CMOS logic gate is best because it can operate over a wide supply voltage range (3V to 15V) and has enough voltage swing to drive the internal Schmitt trigger shown

in Figure 5. For 5V applications, a TTL logic gate can be used by simply adding an external pull-up resistor (see Figure 6).

External Diode (D_x)

Previous circuits of this type have required a diode between V_{OUT} (pin 5) and the external capacitor, C_2 , for voltages above 6.5V (5V for military temperature range). Because of improvements which have been made in the LTC1044 circuit design and Linear Technology's silicon gate CMOS process, this diode is no longer required. The LTC1044 will operate from 1.5V to 9V, without the protection diode, over all temperature ranges.

It should, however, be noted that the LTC1044 will operate without any problems in existing 7660 designs which use the protection diode, as long as the maximum operating voltage (V^+) of 9V is not exceeded.

Capacitor Selection

External capacitors C_1 and C_2 are not critical. Matching is not required, nor do they have to be high quality or tight tolerance. Aluminum or tantalum electrolytics are excellent choices, with cost and size being the only consideration.

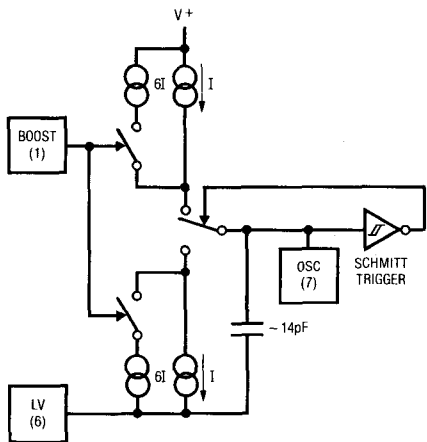


Figure 5. Oscillator

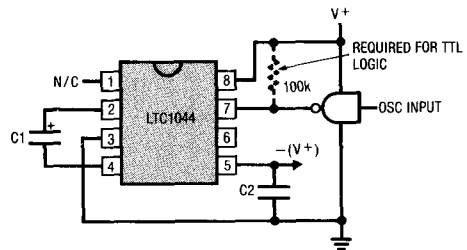


Figure 6. External Clocking

TYPICAL APPLICATIONS

Negative Voltage Converter

Figure 7 shows a typical connection which will provide a negative supply from an available positive supply. This circuit operates over full temperature and power supply ranges *without* the need of any external diodes. The LV pin (pin 6) is shown grounded, but for $V^+ \geq 3V$ it may be "floated", since LV is internally switched to ground (pin 3) for $V^+ \geq 3V$.

The output voltage (pin 5) characteristics of the circuit are those of a nearly ideal voltage source in series with an 80Ω resistor. The 80Ω output impedance is composed of two terms: 1) the equivalent switched capacitor resistance (see Theory of Operation) and 2) a term related to the on-resistance of the MOS switches.

At an oscillator frequency of 10kHz and $C1 = 10\mu F$, the first term is:

$$R_{EQUIV} = \frac{1}{(f_{OSC} / 2) \times C1} = \frac{1}{5 \times 10^3 \times 10 \times 10^{-6}} = 20\Omega.$$

Notice that the above equation for R_{EQUIV} is *not* a capacitive reactance equation ($X_C = 1/\omega C$) and does not contain a 2π term.

The exact expression for output impedance is extremely complex, but the dominant effect of the capacitor is clearly shown on the typical curves of output impedance and power efficiency versus frequency. For $C1 = C2 = 10\mu F$, the output impedance goes from 60Ω at $f_{OSC} = 10kHz$ to 200Ω at $f_{OSC} = 1kHz$. As the $1/fC$ term becomes large compared to the switch on-resistance term, the output resistance is determined by $1/fC$ only.

Voltage Doubling

Figure 8 shows two methods of voltage doubling. In Figure 8a doubling is achieved by simply rearranging the connection of the two external capacitors. When the input voltage is less than 3V, an external $1M\Omega$ resistor is required to ensure the oscillator will start. It is not required for higher input voltages.

In this application the ground input (pin 3) is taken above V^+ (pin 8) during turn-on, making it prone to latch-up. The latch-up is not destructive but simply prevents the circuit from doubling. Resistor R1 is added to eliminate the problem. In most cases 200Ω is sufficient. It may be necessary in a particular application to increase this value to guarantee start-up.

The voltage drop across R1 is: $V_{R1} = 2 \times I_{OUT} \times R1$. If this voltage exceeds two diode drops (1.4V for silicon, 0.8V for Schottky), the circuit in Figure 8a is recommended. This circuit will never have a start-up problem.

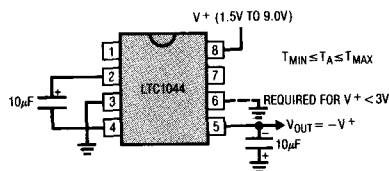
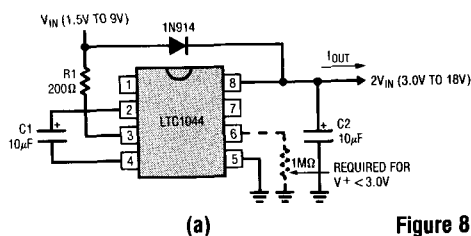
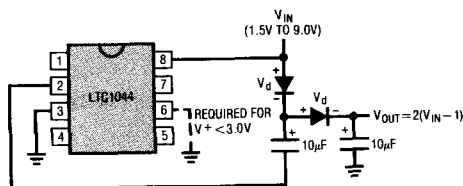


Figure 7. Negative Voltage Converter



(a)



(b)

Figure 8. Voltage Doubler

TYPICAL APPLICATIONS

Ultra Precision Voltage Divider

An ultra precision voltage divider is shown in Figure 9. To achieve the 0.0002% accuracy indicated, the load current should be kept below 100nA. However, with a slight loss in accuracy, the load current can be increased.

Battery Splitter

A common need in many systems is to obtain (+) and (-) supplies from a single battery or single power supply system. Where current requirements are small, the circuit shown in Figure 10 is a simple solution. It provides symmetrical \pm output voltages, both equal to one half the input voltage. The output voltages are both referenced to pin 3 (output common). If the input voltage between pin 8 and pin 5 is less than 6V, pin 6 should also be connected to pin 3, as shown by the dashed line.

Paralleling for Lower Output Resistance

Additional flexibility of the LTC1044 is shown in Figures 11, 12 and 13.

Figure 11 shows two LTC1044s connected in parallel to provide a lower effective output resistance. If, however, the output resistance is dominated by $1/fC_1$, increasing the capacitor size (C1) or increasing the frequency will be of more benefit than the paralleling circuit shown.

Figures 12 and 13 make use of "stacking" two LTC1044s to provide even higher voltages. In Figure 12, a negative voltage doubler or tripler can be achieved, depending upon how pin 8 of the second LTC1044 is connected, as shown schematically by the switch. Figure 13 indicates a similar circuit which can be used to obtain positive tripling, or even quadrupling (the doubler circuit appears in Figure 8a). In both of these circuits, the available output current will be dictated/decreased by the product of the individual power conversion efficiencies and the voltage step-up ratio.

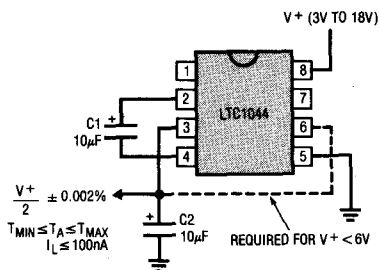


Figure 9. Ultra Precision Voltage Divider

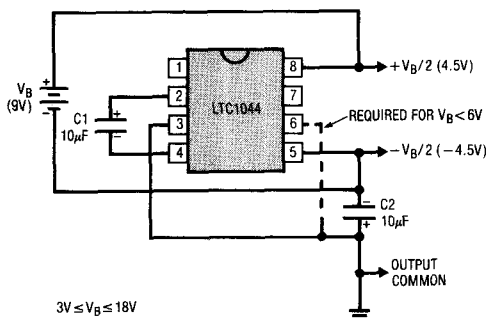
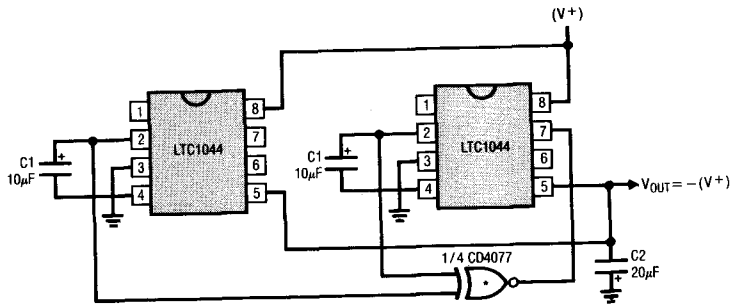


Figure 10. Battery Splitter

TYPICAL APPLICATIONS



*THE EXCLUSIVE NOR GATE SYNCHRONIZES BOTH LTC1044s TO MINIMIZE RIPPLE

Figure 11. Paralleling for Lower Output Resistance

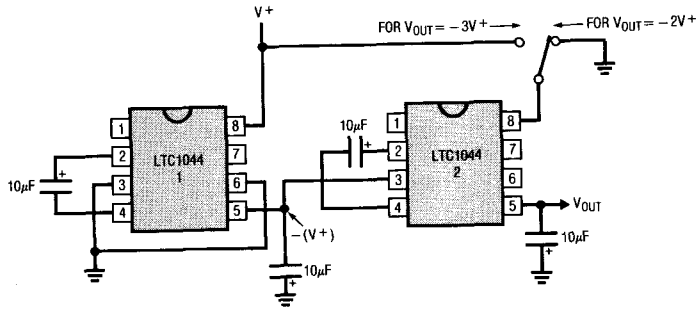
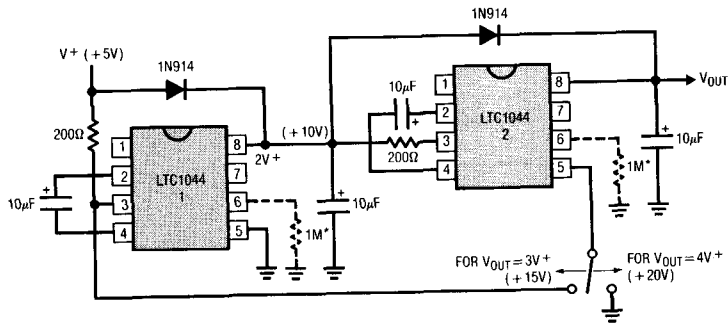


Figure 12. Stacking for Higher Voltage



*REQUIRED FOR V+ < 3.0V

Figure 13. Voltage Tripler / Quadrupler

TYPICAL APPLICATIONS

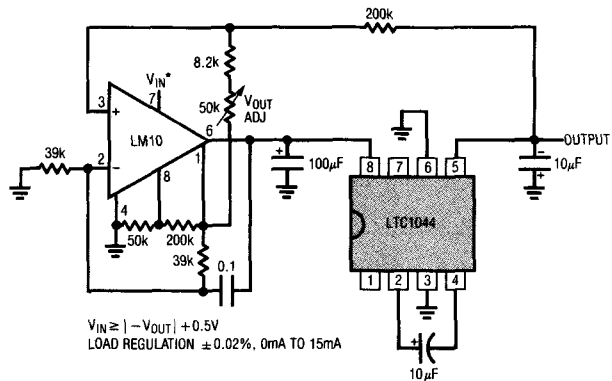


Figure 14. Low Output Impedance Voltage Converter

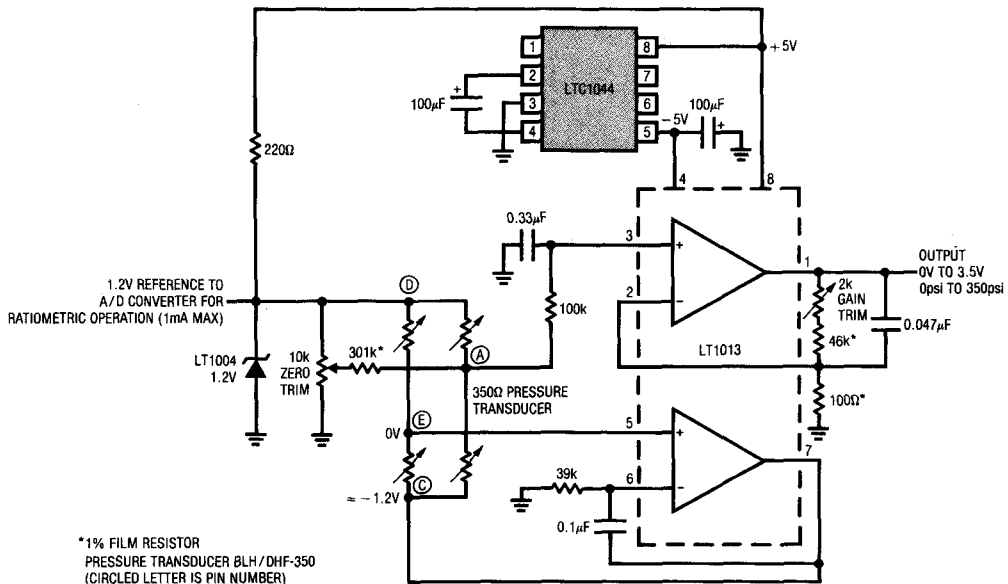


Figure 15. Single 5V Strain Gauge Bridge Signal Conditioner

TYPICAL APPLICATIONS

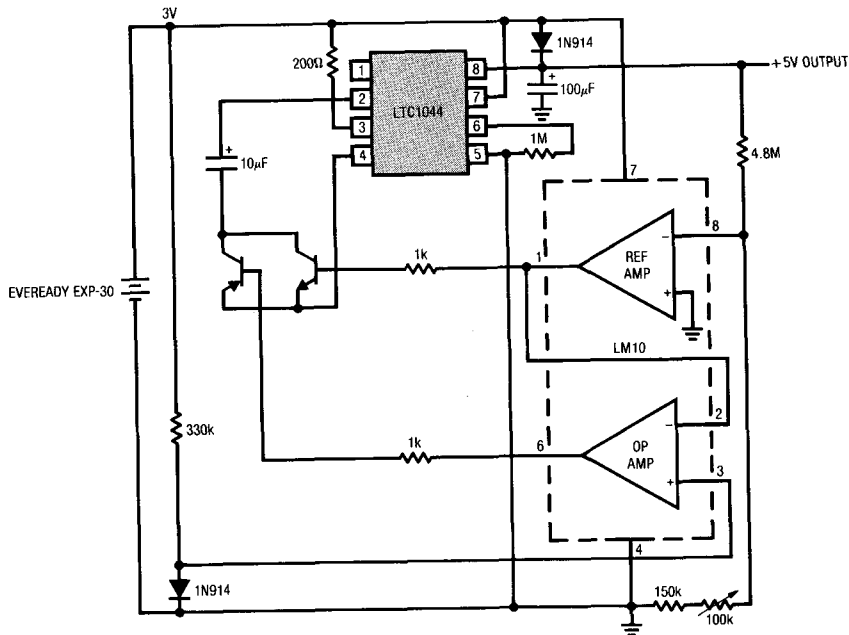


Figure 16. Regulated Output +3V to +5V Converter

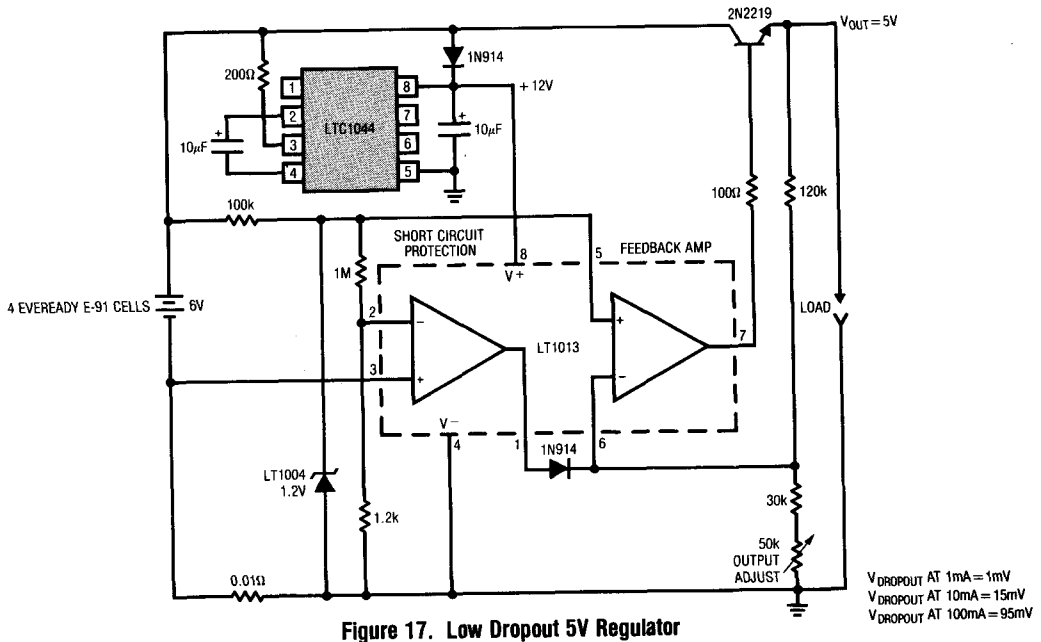
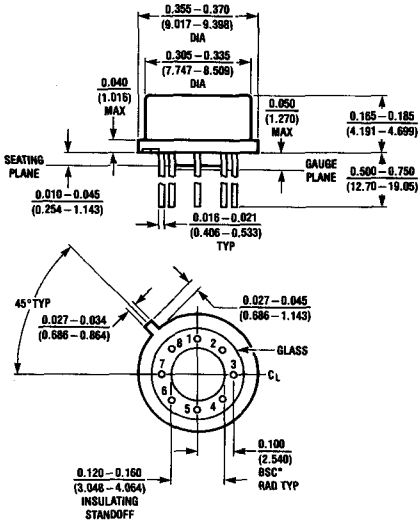


Figure 17. Low Dropout 5V Regulator

$V_{\text{DROPOUT AT 1mA}} = 1\text{mV}$
 $V_{\text{DROPOUT AT 10mA}} = 15\text{mV}$
 $V_{\text{DROPOUT AT 100mA}} = 95\text{mV}$

PACKAGE DESCRIPTION

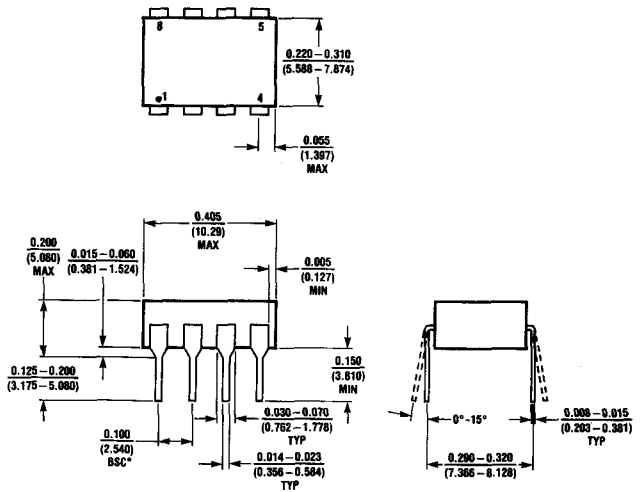
**H Package
Metal Can**



NOTE: DIMENSIONS IN INCHES (MILLIMETERS)

T_{jmax}	θ_{ja}	θ_{jc}
150°C	150°C/W	45°C/W

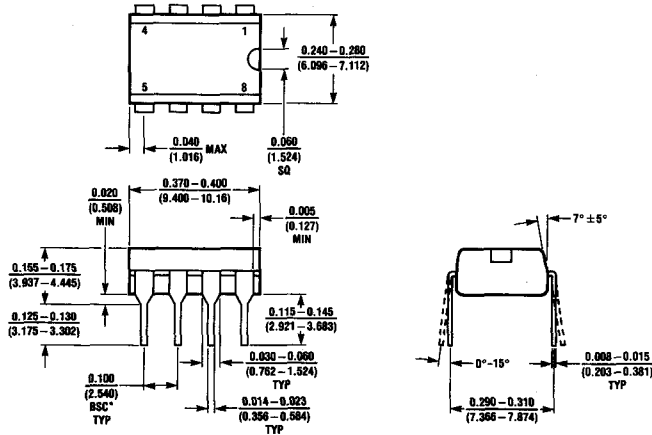
**J8 Package
8 Lead Hermetic DIP**



NOTE: DIMENSIONS IN INCHES (MILLIMETERS) UNLESS OTHERWISE NOTED
*LEADS WITHIN 0.007 OF TRUE POSITION (TP) AT GAUGE PLANE

T_{jmax}	θ_{ja}
150°C	100°C/W

**N8 Package
8 Lead Plastic**



NOTE: DIMENSIONS IN INCHES (MILLIMETERS) UNLESS OTHERWISE NOTED
*LEADS WITHIN 0.007 OF TRUE POSITION (TP) AT GAUGE PLANE

T_{jmax}	θ_{ja}
100°C	130°C/W

FEATURES

- Plug-In Compatible with 7660 with These Additional Features:
 - *Guaranteed* Operation to 9V, with No External Diode, Over Full Temperature Range
 - Boost Pin (Pin 1) for Higher Switching Frequency
 - Lower Quiescent Power
 - Efficient Voltage Doubler
- 200 μ A *Max.* No Load Supply Current at 5V
- 97% *Min.* Open Circuit Voltage Conversion Efficiency
- 95% *Min.* Power Conversion Efficiency
- Wide Operating Supply Voltage Range, 1.5V to 9V
- Easy to Use
- Commercial Device *Guaranteed* Over -40°C to 85°C Temperature Range

APPLICATIONS

- Conversion of +5V to $\pm 5\text{V}$ Supplies
- Precise Voltage Division, $V_{\text{OUT}} = V_{\text{IN}} / 2 \pm 20\text{ppm}$
- Voltage Multiplication, $V_{\text{OUT}} = \pm nV_{\text{IN}}$
- Supply Splitter, $V_{\text{OUT}} = \pm V_{\text{S}} / 2$

DESCRIPTION

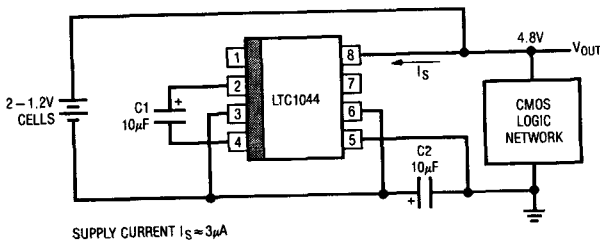
The LTC1044 is a monolithic CMOS switched capacitor voltage converter which is manufactured using Linear Technology's enhanced LTCMOS™ silicon gate process. The LTC1044 provides several voltage conversion functions: the input voltage can be inverted ($V_{\text{OUT}} = -V_{\text{IN}}$), doubled ($V_{\text{OUT}} = 2V_{\text{IN}}$), divided ($V_{\text{OUT}} = V_{\text{IN}} / 2$) or multiplied ($V_{\text{OUT}} = \pm nV_{\text{IN}}$).

Designed to be pin-for-pin and functionally compatible with the popular 7660, the LTC1044 provides significant features and improvements over earlier 7660 designs. These improvements include: full 1.5V to 9V supply operation over the entire operating temperature range, without the need for external protection diodes; 2½ times lower quiescent current for greater power conversion efficiency; and a "boost" function which is available to raise the internal oscillator frequency to optimize performance in specific applications.

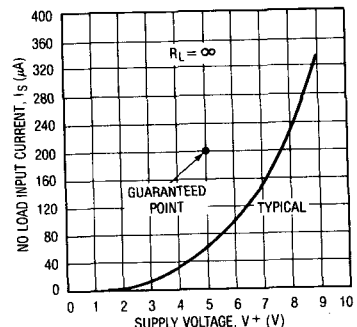
Although the LTC1044 provides significant design and performance advantages over the earlier 7660 device, it still maintains its compatibility with existing 7660 designs.

LTCMOS™ is a trademark of Linear Technology Corp.

Generating CMOS Logic Supply from 2 Mercury Batteries



Supply Current vs Supply Voltage



ABSOLUTE MAXIMUM RATINGS

(Notes 1 and 2)

Supply Voltage	9.5V
Input Voltage on Pins 1, 6 and 7 (Note 2)	$-0.3V \leq V_{IN} \leq V^+ + 0.3V$
Current into Pin 6	20 μ A
Output Short Circuit Duration ($V^+ \leq 5.5V$)	Continuous
Operating Temperature Range	$-40^\circ C \leq T_A \leq 85^\circ C$
Storage Temperature Range	$-65^\circ C$ to $+150^\circ C$
Lead Temperature (Soldering, 10 sec.)	300 $^\circ C$

PACKAGE/ORDER INFORMATION

<p>TOP VIEW</p> <p>BOOST 1 8 V+</p> <p>CAP+ 2 7 OSC</p> <p>GROUND 3 6 LV</p> <p>CAP- 4 5 VOUT</p> <p>S8 PACKAGE PLASTIC SO</p>	ORDER PART NUMBER
	LTC1044CS8
	PART MARKING
	1044

ELECTRICAL CHARACTERISTICS $V^+ = 5V$, $T_A = 25^\circ C$, unless otherwise specified.

See LTC1044/7660 data sheet for test circuit.

SYMBOL	PARAMETER	CONDITIONS	LTC1044CS8			UNITS
			MIN	TYP	MAX	
I_S	Supply Current	$R_L = \infty$, Pins 1 and 7 No Connection $R_L = \infty$, Pins 1 and 7 $V = 3V$		60 20	200	μA μA
V^+_{L}	Minimum Supply Voltage	$R_L = 10k$	●	1.5		V
V^+_{H}	Maximum Supply Voltage	$R_L = 10k$ (Note 3)	●		9	V
R_{OUT}	Output Resistance	$I_L = 200mA$, $f_{OSC} = 5kHz$	●		100 130 325	Ω Ω Ω
f_{OSC}	Oscillator Frequency	$C_{QSC} = 1pF$ (Note 4) $V^+ = 5V$ $V^+ = 2V$	● ●	5 1		kHz kHz
P_{EFF}	Power Efficiency	$R_L = 5k\Omega$, $f_{OSC} = 5kHz$		95	98	%
V_{OUTEFF}	Voltage Conversion Efficiency	$R_L = \infty$		97	99.9	%
I_{OSC}	Oscillator Sink or Source Current	$V_{OSC} = 0V$ or V^+ Pin 1 = 0V Pin 1 = V^+	● ●		3 20	μA μA

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: Absolute Maximum Ratings are those values beyond which the life of the device may be impaired.

Note 2: Connecting any input terminal to voltages greater than V^+ or less than ground may cause destructive latch-up. It is recommended that no inputs from sources operating from external supplies be applied prior to power-up of the LTC1044.

Note 3: The LTC1044 is guaranteed to operate with alkaline, mercury or NiCad 9V batteries, even though the initial battery voltage may be slightly higher than 9.0V.

Note 4: f_{OSC} is tested with $C_{QSC} = 100pF$ to minimize the effects of test fixture capacitance loading. The 1pF frequency is correlated to this 100pF test point, and is intended to simulate the capacitance at pin 7 when the device is plugged into a test socket and no external capacitor is used.

Switched Capacitor Voltage Converter with Regulator

FEATURES

- 100mA Output Current
- Low Loss—1.1V at 100mA
- Operating Range 3.5V to 15V
- Reference and Error Amplifier for Regulation
- External Shutdown
- External Oscillator Sync
- Can be Paralleled
- Pin Compatible with the LTC1044/7660

APPLICATIONS

- Voltage Inverter
- Negative Voltage Doubler
- Voltage Regulator
- Positive Voltage Doubler

DESCRIPTION

The LT1054 is a monolithic, bipolar, switched capacitor voltage converter and regulator. The LT1054 provides higher output current than previously available converters with significantly lower voltage losses. An adaptive switch drive scheme optimizes efficiency over a wide range of output currents. Total voltage loss at 100mA output current is typically 1.1V. This holds true over the full supply voltage range of 3.5V to 15V. Quiescent current is typically 2.5 mA.

The LT1054 also provides regulation, a feature not previously available in switched capacitor voltage converters. By adding an external feedback divider, a regulated output can be obtained. This output will be regulated against changes in both input voltage and output current. The LT1054 can also be shut down by grounding the feedback pin. Supply current in shutdown is less than 100 μ A.

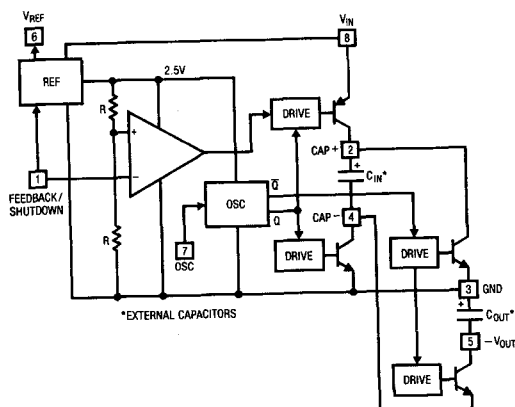
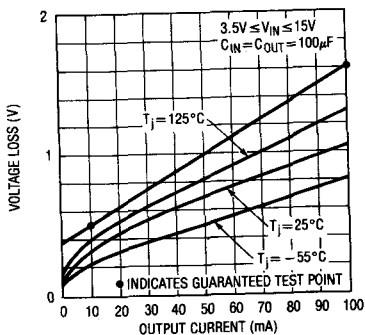
The internal oscillator of the LT1054 runs at a nominal frequency of 25kHz. The oscillator pin can be used to adjust the switching frequency, or to externally synchronize the LT1054.

The LT1054 is pin compatible with previous converters such as the LTC1044/7660.

REFER TO TABLE OF CONTENTS FOR REVISED DATA LOCATION

5

BLOCK DIAGRAM


Voltage Loss


ABSOLUTE MAXIMUM RATINGS

Supply Voltage (Note 1)	16V
Input Voltage (Pin 1)	$0V \leq V_{PIN1} \leq V^+$
Input Voltage (Pin 7)	$0V \leq V_{PIN7} \leq V_{REF}$
Operating Temperature Range	
LT1054C	0°C to 70°C
LT1054M	-55°C to 125°C
Junction Temperature (Note 2)	
LT1054C	125°C
LT1054M	150°C
Storage Temperature Range	-55°C to 150°C
Lead Temperature (Soldering, 10 sec.)	300°C

PACKAGE/ORDER INFORMATION

	ORDER PART NUMBER LT1054MJ LT1054CJ LT1054CN
	LT1054MH LT1054CH ALSO AVAILABLE IN SO PACKAGE

ELECTRICAL CHARACTERISTICS

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	
Supply Current	$I_{LOAD} = 0mA$ $V_{IN} = 3.5V$ $V_{IN} = 15V$	●	2.5 3.0	3.5 4.5	mA mA	
Supply Voltage Range		●	3.5	15	V	
Voltage Loss ($V_{IN} - V_{OUT} $)	$C_{IN} = C_{OUT} = 100\mu F$ Tantalum (Note 3) $I_{OUT} = 10mA$ $I_{OUT} = 100mA$	●	0.35 1.10	0.55 1.60	V V	
Output Resistance	$\Delta I_{OUT} = 10mA$ to 100mA (Note 4)	●	10	15	Ω	
Oscillator Frequency	$3.5V \leq V_{IN} \leq 15V$	●	15	25	35	kHz
Reference Voltage	$I_{REF} = 60\mu A$ $T_j = 25^\circ C$	●	2.35 2.25	2.50 2.75	V V	
Regulated Voltage	$V_{IN} = 7V$, $T_j = 25^\circ C$, $R_L = 500\Omega$ (Note 5)		-4.70	-5.00	-5.20	V
Line Regulation	$7V \leq V_{IN} \leq 12V$, $R_L = 500\Omega$ (Note 5)	●	5	25	mV	
Load Regulation	$V_{IN} = 7V$ $100\Omega \leq R_L \leq 500\Omega$ (Note 5)	●	10	50	mV	
Maximum Switch Current			300		mA	
Supply Current in Shutdown	$V_{PIN1} = 0V$	●	100	150	μA	

The ● denotes specifications which apply over the full operating temperature range. For C grade parts these specifications also apply up to a junction temperature of 100°C.

Note 1: The absolute maximum supply voltage rating of 16V is for unregulated circuits. For regulation mode circuits with $V_{OUT} \leq 15V$ at Pin 5, this rating may be increased to 20V.

Note 2: The devices are guaranteed by design to be functional up to the absolute maximum junction temperature.

Note 3: For voltage loss tests, the device is connected as a voltage

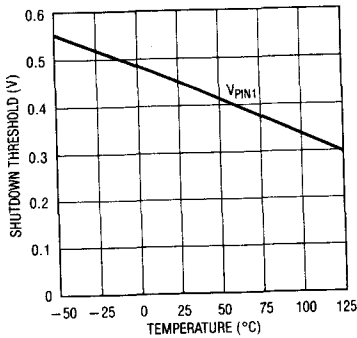
inverter, with Pins 1, 6, and 7 unconnected. The voltage losses may be higher in other configurations.

Note 4: Output resistance is defined as the slope of the curve, (ΔV_{OUT} vs ΔI_{OUT}), for output currents of 10 to 100 mA. This represents the linear portion of the curve. The incremental slope of the curve will be higher at currents < 10mA due to the characteristics of the switch transistors.

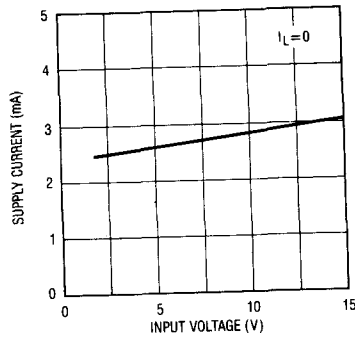
Note 5: All regulation specifications are for a device connected as a positive to negative converter/regulator with $R1 = 20k$, $R2 = 102.5k$, $C1 = 0.002\mu F$, $C_{IN} = 10\mu F$ tantalum, $C_{OUT} = 100\mu F$ tantalum.

TYPICAL PERFORMANCE CHARACTERISTICS

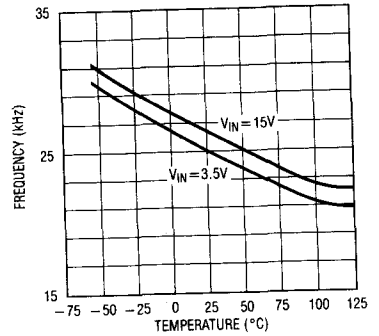
Shutdown Threshold



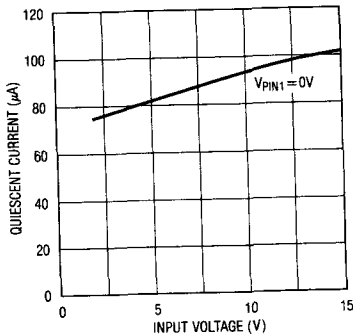
Supply Current



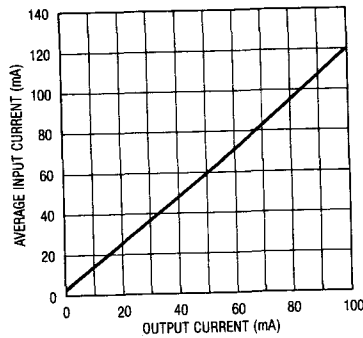
Oscillator Frequency



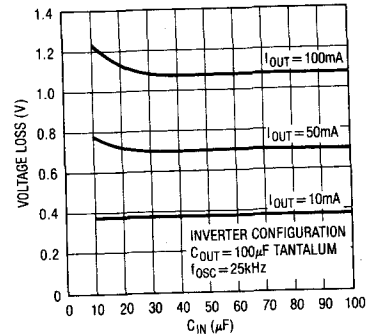
Supply Current in Shutdown



Average Input Current

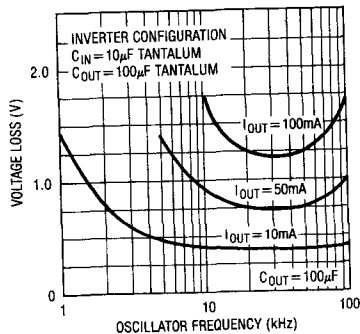


Output Voltage Loss

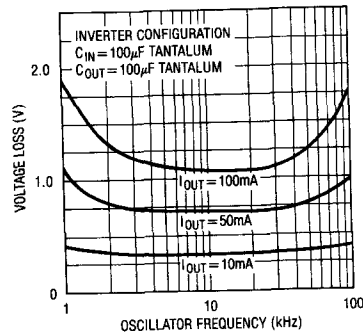


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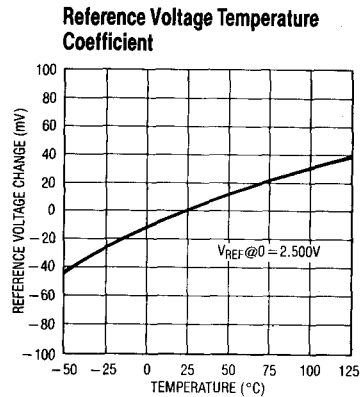
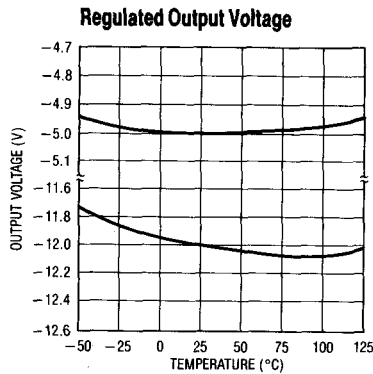
Output Voltage Loss



Output Voltage Loss



TYPICAL PERFORMANCE CHARACTERISTICS



APPLICATIONS INFORMATION

Theory of Operation

To understand the theory of operation of the LT1054, a review of a basic switched capacitor building block is helpful.

In Figure 1, when the switch is in the left position, capacitor C1 will charge to voltage V1. The total charge on C1 will be $q_1 = C_1V_1$. The switch then moves to the right, discharging C1 to voltage V2. After this discharge time, the charge on C1 is $q_2 = C_1V_2$. Note that charge has been transferred from the source, V1, to the output, V2. The amount of charge transferred is:

$$\Delta q = q_1 - q_2 = C_1(V_1 - V_2).$$

If the switch is cycled f times per second, the charge transfer per unit time (i.e., current) is:

$$I = f \times \Delta q = f \times C_1(V_1 - V_2).$$

To obtain an equivalent resistance for the switched-capacitor network we can rewrite this equation in terms of voltage and impedance equivalence:

$$I = \frac{V_1 - V_2}{(1/fC_1)} = \frac{V_1 - V_2}{R_{EQUIV}}$$

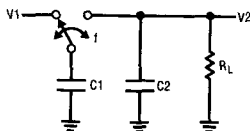


Figure 1. Switched Capacitor Building Block

A new variable, R_{EQUIV} , is defined such that $R_{EQUIV} = 1/fC_1$. Thus, the equivalent circuit for the switched capacitor network is as shown in Figure 2. The LT1054 has the same switching action as the basic switched capacitor building block. Even though this simplification doesn't include finite switch on-resistance and output voltage ripple, it provides an intuitive feel for how the device works.

These simplified circuits explain voltage loss as a function of frequency (see typical curve). As frequency is decreased, the output impedance will eventually be dominated by the $1/fC_1$ term and voltage losses will rise.

Note that losses also rise as frequency increases. This is caused by internal switching losses which occur due to some finite charge being lost on each switching cycle. This charge loss per-unit-cycle, when multiplied by the switching frequency, becomes a current loss. At high frequency this loss becomes significant and voltage losses again rise.

The oscillator of the LT1054 is designed to run in the frequency band where voltage losses are at a minimum.

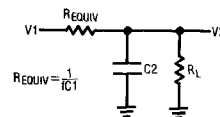


Figure 2. Switched Capacitor Equivalent Circuit

APPLICATIONS INFORMATION

Pin Functions

V⁺ (Pin 8): Input supply pin. The LT1054 alternately charges C_{IN} to the input voltage when C_{IN} is switched in parallel with the input supply, and then transfers charge to C_{OUT} when C_{IN} is switched in parallel with C_{OUT}. Switching occurs at the oscillator frequency. During the time that C_{IN} is charging, the peak supply current will be approximately equal to 2.2 times the output current. During the time that C_{IN} is delivering charge to C_{OUT} the supply current drops to approximately 0.2 times the output current. An input supply bypass capacitor will supply part of the peak input current drawn by the LT1054, and average out the current drawn from the supply. A minimum input supply bypass capacitor of 2μF, preferably tantalum or some other low ESR type is recommended. A larger capacitor may be desirable in some cases, for example when the actual input supply is connected to the LT1054 through long leads, or when the pulse currents drawn by the LT1054 might affect other circuitry through supply coupling.

V_{OUT} (Pin 5): In addition to being the output pin, the pin is also tied to the substrate of the device. **Special care must be taken in LT1054 circuits to avoid pulling this pin positive with respect to any of the other pins.** Pulling Pin 5 positive with respect to Pin 3 (GND) will forward bias the substrate diode which will prevent the device from starting. This condition can occur when the output load driven by the LT1054 is referred to its positive supply, (or to some other positive voltage). Note that most op amps present just such a load, since their supply currents flow from their V⁺ terminals to their V⁻ terminals. To prevent start-up problems with this type of load, an external transistor must be added as shown in Figure 3. This will prevent V_{OUT}

(Pin 5) from being pulled above the ground pin (Pin 3) during start-up. Any small, general purpose transistor such as 2N2222 or 2N2219 can be used. R_X should be chosen to provide enough base drive to the external transistor so that it is saturated under nominal output voltage and maximum output current conditions. In some cases an N-channel enhancement mode MOSFet can be used in place of the transistor.

$$R_X \leq \frac{(|V_{OUT}|) \beta}{I_{OUT}}$$

V_{REF} (Pin 6): Reference output pin. This pin provides a 2.5V reference point for use in LT1054 based regulator circuits. The temperature coefficient of the reference voltage has been adjusted so that the temperature coefficient of the regulated output voltage is close to zero. This requires the reference output to have a positive temperature coefficient as can be seen in the typical performance curves. This non-zero drift is necessary to offset a drift term inherent in the internal reference divider and comparator network tied to the feedback pin. The overall result of these drift terms is a regulated output which has a slight positive temperature coefficient at output voltages below 5V and a slight negative TC at output voltages above 5V. Reference output current should be limited, for regulator feedback networks, to approximately 60μA. The reference pin will draw ≈100μA when shorted to ground, and will not affect the internal reference/regulator, so that this pin can also be used as a pull-up for LT1054 circuits that require synchronization.

CAP⁺/CAP⁻ (Pin 2/Pin 4): Pin 2, the positive side of the input capacitor (C_{IN}) is alternately driven between V⁺ and ground. When driven to V⁺, Pin 2 sources current from V⁺. When driven to ground, Pin 2 sinks current to ground. Pin 4, the negative side of the input capacitor is driven alternately between ground and V_{OUT}. When driven to ground, Pin 4 sinks current to ground. When driven to V_{OUT}, Pin 4 sources current from C_{OUT}. In all cases current flow in the switches is unidirectional, as should be expected using bipolar switches.

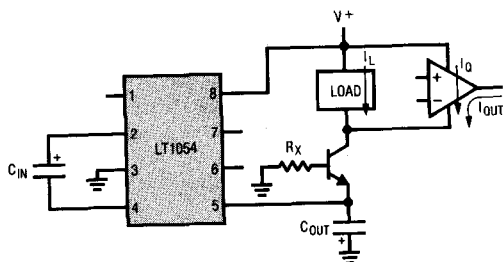


Figure 3

APPLICATIONS INFORMATION

OSC (Pin 7): Oscillator pin. This pin can be used to raise or lower the oscillator frequency, or to synchronize the device to an external clock. Internally, Pin 7 is connected to the oscillator timing capacitor ($C_1 \approx 150\text{pF}$) which is alternately charged and discharged by current sources of $\pm 7\mu\text{A}$, so that the duty cycle is $\approx 50\%$. The LT1054 oscillator is designed to run in the frequency band where switching losses are minimized. However, the frequency can be raised, lowered or synchronized to an external system clock if necessary.

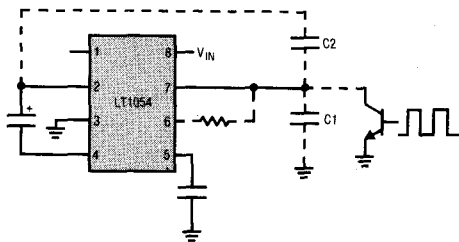


Figure 4

The frequency can be lowered by adding an external capacitor (C_1 Figure 4) from Pin 7 to ground. This will increase the charge and discharge times, which lowers the oscillator frequency. The frequency can be increased by adding an external capacitor (C_2 Figure 4, in the range of 5pF – 20pF) from Pin 2 to Pin 7. This capacitor will couple charge into C_1 at the switch transitions, which will shorten the charge and discharge time, raising the oscillator frequency. Synchronization can be accomplished by adding an external resistive pull-up from Pin 7 to the reference pin (Pin 6). A $20\text{k}\Omega$ pull-up is recommended. An open collector gate or an NPN transistor can then be used to drive the oscillator pin at the external clock frequency as shown in Figure 4. Pulling up Pin 7 to an external voltage is **not recommended**. For circuits that require both frequency synchronization and regulation, an external reference can be used as the reference point for the top of the R_1/R_2 divider allowing Pin 6 to be used as a pull-up point for Pin 7.

Feedback/Shutdown (Pin 1): This pin has two functions. Pulling Pin 1 below the shutdown threshold ($\approx 0.45\text{V}$) puts the device into shutdown. In shutdown, the reference/regulator is turned off and switching stops. The switches are set such that both C_{IN} and C_{OUT} are discharged through the output load. Quiescent current in shutdown drops to approximately $100\mu\text{A}$ (see typical curves). Any open-collector gate can be used to put the LT1054 into shutdown. For normal (unregulated) operation the device will start back up when the external gate is shut off. In LT1054 circuits that use the regulation feature, the external resistor divider can provide enough pull-down to keep the device in shutdown until the output capacitor (C_{OUT}) has fully discharged. For most applications where the LT1054 would be run intermittently, this does not present a problem because the discharge time of the output capacitor will be short compared to the off time of the device. In applications where the device has to start-up before the output capacitor (C_{OUT}) has fully discharged, a restart pulse must be applied to Pin 1 of the LT1054. Using the circuit of Figure 5, the restart signal can be either a pulse ($t_p > 100\mu\text{s}$) or a logic high. Diode coupling the restart signal into Pin 1 will allow the output voltage to come up and regulate without overshoot. The resistor divider R_3/R_4 in Figure 5 should be chosen to provide a signal level at Pin 1 of 0.7V – 1.1V .

Pin 1 is also the inverting input of the LT1054's error amplifier, and as such can be used to obtain a regulated output voltage.

Regulation

The error amplifier of the LT1054 services the drive to the PNP switch to control the voltage across the input capacitor (C_{IN}), which in turn will determine the output voltage. Using the reference and error amplifier of the LT1054, an external resistive divider is all that is needed to set the regulated output voltage. Figure 5 shows the basic regulator configuration and the formula for calculating the appropriate resistor values. R_2 should be chosen to be $20\text{k}\Omega$ or greater because the reference output current is limited

APPLICATIONS INFORMATION

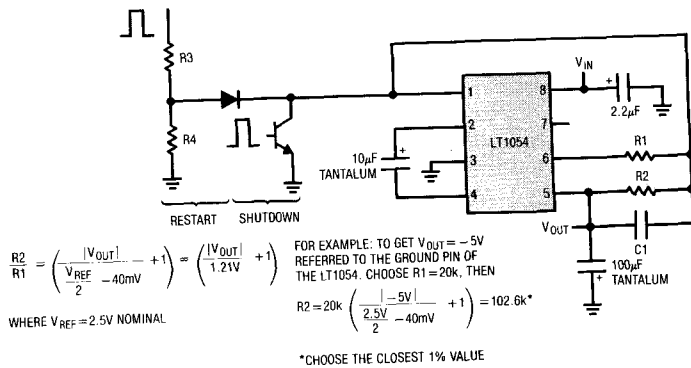


Figure 5

to $\approx 100\mu A$. R1 should be chosen to be in the range of 100k to 300k. Frequency compensation is accomplished by adjusting the ratio of C_{IN}/C_{OUT} . For best results, this ratio should be $\approx 1/10$. C1, required for good load regulation at light load currents, should be $0.002\mu F$ for all output voltages.

It can be seen from the circuit block diagram that the maximum regulated output voltage is limited by the supply voltage. For the basic configuration, $|V_{OUT}|$ referred to the ground pin of the LT1054 must be less than the total of the supply voltage minus the voltage loss due to the switches. The voltage loss versus output current due to the switches can be found in the typical performance curves. Other configurations such as the negative doubler can provide higher output voltages at reduced output currents (see typical applications).

Capacitor Selection

While the exact values of C_{IN} and C_{OUT} are non-critical, good quality, low ESR capacitors such as solid tantalum are necessary to minimize voltage losses at high currents. For C_{IN} the effect of the ESR of the capacitor will be multiplied by four, due to the fact that switch currents are approximately two times higher than output current, and losses will occur on both the charge and discharge cycle. This means that using a capacitor with 1Ω of ESR for C_{IN} will have the same effect as increasing the output

impedance of the LT1054 by 4Ω . This represents a significant increase in the voltage losses. For C_{OUT} the affect of ESR is less dramatic. C_{OUT} is alternately charged and discharged at a current approximately equal to the output current, and the ESR of the capacitor will cause a step function to occur, in the output ripple, at the switch transitions. This step function will degrade the output regulation for changes in output load current, and should be avoided. Realizing that large value tantalum capacitors can be expensive, a technique that can be used is to parallel a smaller tantalum capacitor with a large aluminum electrolytic capacitor to gain both low ESR and reasonable cost. Where physical size is a concern some of the newer chip type surface mount tantalum capacitors can be used. These capacitors are normally rated at working voltages in the 10V-20V range and exhibit very low E.S.R., (in the range of 0.1Ω).

Output Ripple

The peak-to-peak output ripple is determined by the value of the output capacitor and the output current. Peak-to-peak output ripple may be approximated by the formula:

$$dV = \frac{I_{OUT}}{2fC_{OUT}}$$

where $dV = p-p$ ripple
 $f =$ oscillator frequency

APPLICATIONS INFORMATION

For output capacitors with significant ESR, a second term must be added to account for the voltage step at the switch transitions. This step is, approximately equal to:

$$(2I_{OUT})(ESR \text{ of } C_{OUT})$$

Power Dissipation

The power dissipation of any LT1054 circuit must be limited such that the junction temperature of the device does not exceed the maximum junction temperature ratings. The total power dissipation must be calculated from two components, the power loss due to voltage drops in the switches, and the power loss due to drive current losses. The total power dissipated by the LT1054 can be calculated from:

$$P \approx (V_{IN} - |V_{OUT}|)(I_{OUT}) + (V_{IN})(I_{OUT})(0.2)$$

where both V_{IN} and V_{OUT} are referred to the ground pin (Pin 3) of the LT1054. For LT1054 regulator circuits, the power dissipation will be equivalent to that of a linear regulator. Due to the limited power handling capability of the LT1054 packages, the user will have to limit output current requirements or take steps to dissipate some power external to the LT1054 for large input/output differentials. This can be accomplished by placing a resistor in series with C_{IN} as shown in Figure 6. A portion of the input voltage will then be dropped across this resistor, without affecting the output regulation. Because switch current is approximately 2.2 times the output current, and the resistor will cause a voltage drop when C_{IN} is both charging and discharging, the resistor should be chosen as:

$$R_X = V_X / (4.4 I_{OUT})$$

where

$$V_X \approx V_{IN} - [(LT1054 \text{ voltage loss})(1.3) + |V_{OUT}|]$$

and I_{OUT} = maximum required output current. The factor of 1.3 will allow some operating margin for the LT1054.

For example: assume a +12V to -5V converter at 100mA output current. First calculate the power dissipation without an external resistor:

$$P = (12V - |-5V|)(100mA) + (12V)(100mA)(0.2)$$

$$P = 700mW + 240mW = 940mW$$

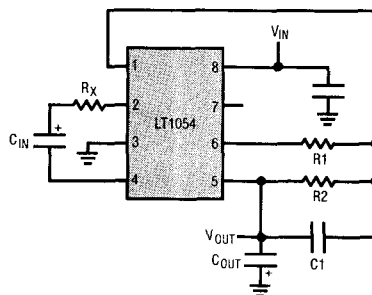


Figure 6

At θ_{JA} of 130°C/W for a commercial plastic device this would cause a junction temperature rise of 122°C, so that the device would exceed the maximum junction temperature at an ambient temperature of 25°C. Now calculate the power dissipation with an external-resistor (R_X). First find how much voltage can be dropped across R_X . The maximum voltage loss of the LT1054 in the standard regulator configuration at 100mA output current is 1.6V, so

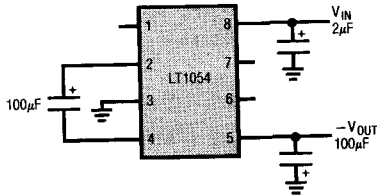
$$V_X = 12V - [(1.6V)(1.3) + |-5V|] = 4.9V \text{ and}$$

$$R_X = 4.9V / (4.4)(100mA) = 11\Omega.$$

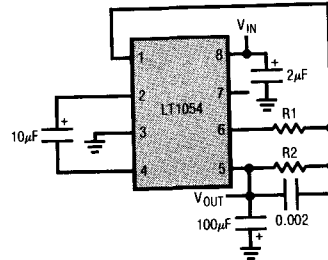
This resistor will reduce the power dissipated by the LT1054 by $(4.9V)(100mA) = 490mW$. The total power dissipated by the LT1054 would then be $\approx (940mW - 490mW) = 450mW$. The junction temperature rise would now be only 58°C. Although commercial devices are guaranteed to be functional up to a junction temperature of 125°C, the specifications are only guaranteed up to a junction temperature of 100°C, so ideally you should limit the junction temperature to 100°C. For the above example this would mean limiting the ambient temperature to 42°C. Other steps can be taken, however, to allow higher ambient temperatures. The thermal resistance numbers for the LT1054 packages represent worst-case numbers with no heat-sinking and still air. Small clip-on type heat sinks can be used to lower the thermal resistance of the LT1054 package. In some systems there may be some available airflow which will help to lower the thermal resistance. Wide PC board traces from the LT1054 leads can also help to remove heat from the device. This is especially true for plastic packages.

TYPICAL APPLICATIONS

Basic Voltage Inverter

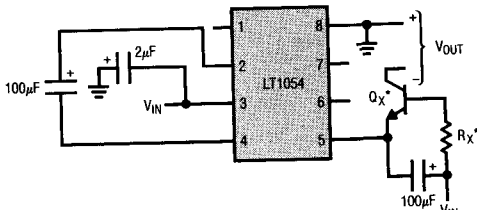


Basic Voltage Inverter/Regulator



$$\frac{R2}{R1} = \left(\frac{|V_{OUT}|}{V_{REF} - 40mV} + 1 \right) = \left(\frac{|V_{OUT}|}{1.21V} + 1 \right) \quad \text{[REFER TO FIGURE 5]}$$

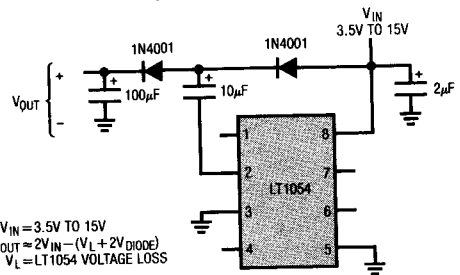
Negative Voltage Doubler



$V_{IN} = -3.5V \text{ TO } -15V$
 $V_{OUT} = 2V_{IN} + (\text{LT1054 VOLTAGE LOSS}) + (Q_X \text{ SATURATION VOLTAGE})$

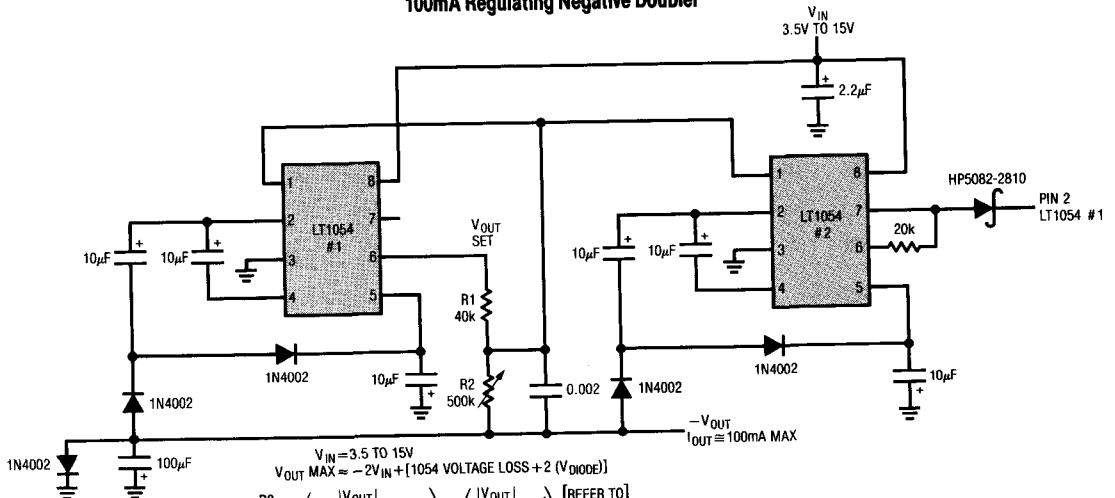
*SEE FIGURE 3

Positive Doubler



$V_{IN} = 3.5V \text{ TO } 15V$
 $V_{OUT} \approx 2V_{IN} - (V_L + 2V_{DIODE})$
 $V_L = \text{LT1054 VOLTAGE LOSS}$

100mA Regulating Negative Doubler



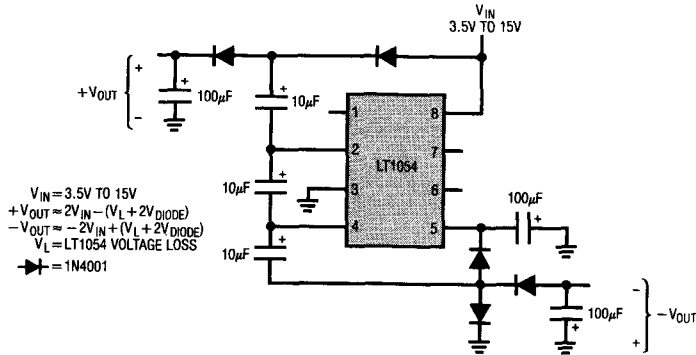
$V_{IN} = 3.5 \text{ TO } 15V$
 $V_{OUT \text{ MAX}} \approx -2V_{IN} + [1054 \text{ VOLTAGE LOSS} + 2(V_{DIODE})]$

$$\frac{R2}{R1} = \left(\frac{|V_{OUT}|}{V_{REF} - 40mV} + 1 \right) = \left(\frac{|V_{OUT}|}{1.21V} + 1 \right) \quad \text{[REFER TO FIGURE 5]}$$

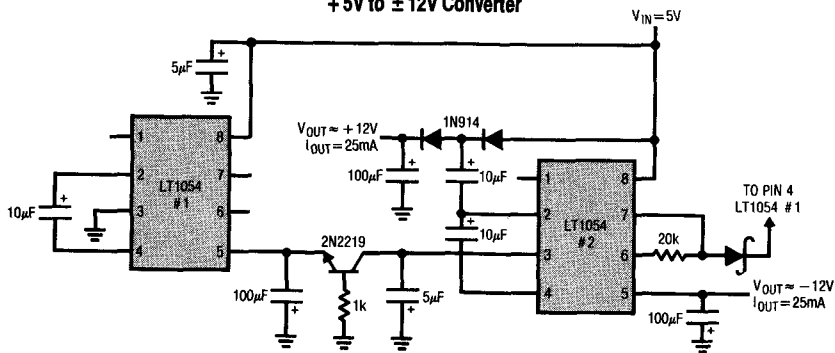
5

TYPICAL APPLICATIONS

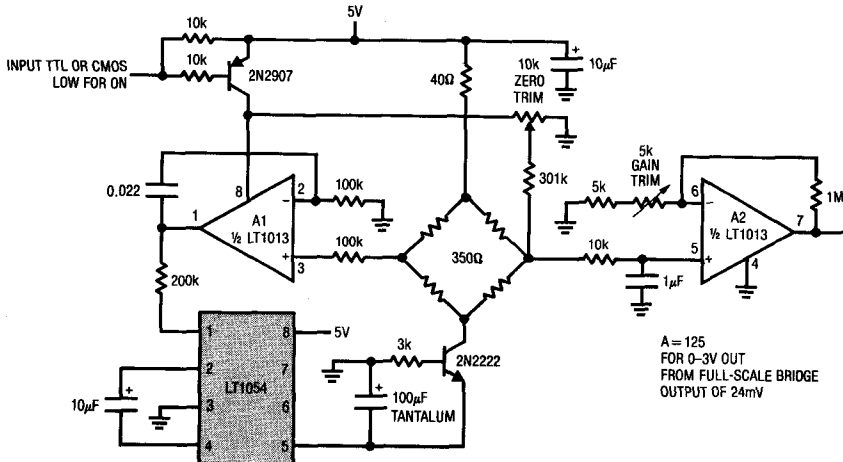
Dual Output Voltage Doubler



+5V to ±12V Converter

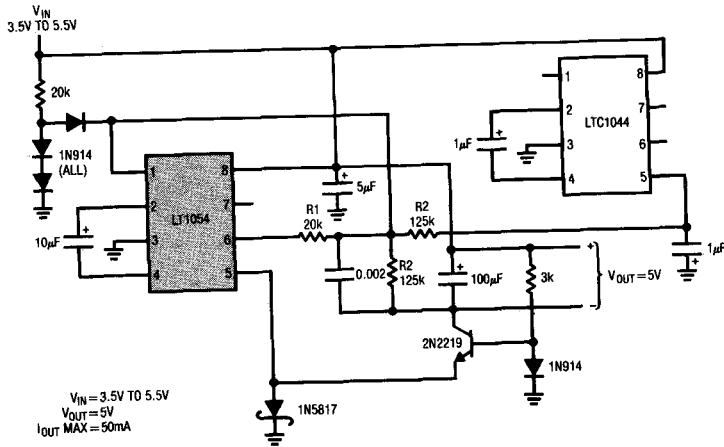


Strain Gage Bridge Signal Conditioner

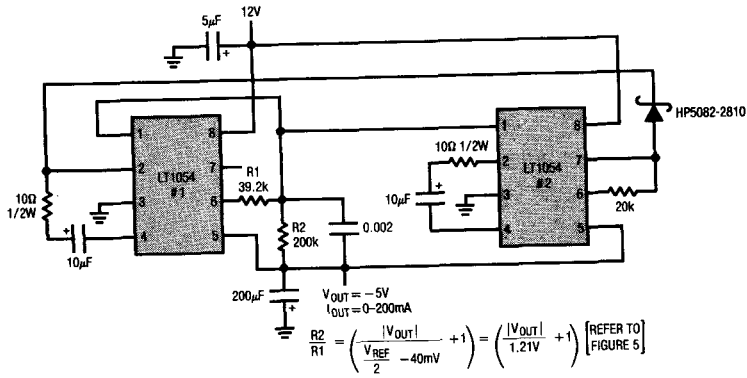


TYPICAL APPLICATIONS

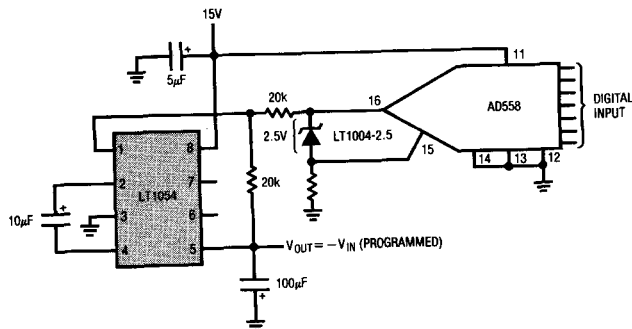
3.5V to 5V Regulator



Regulating 200mA +12V to -5V Converter

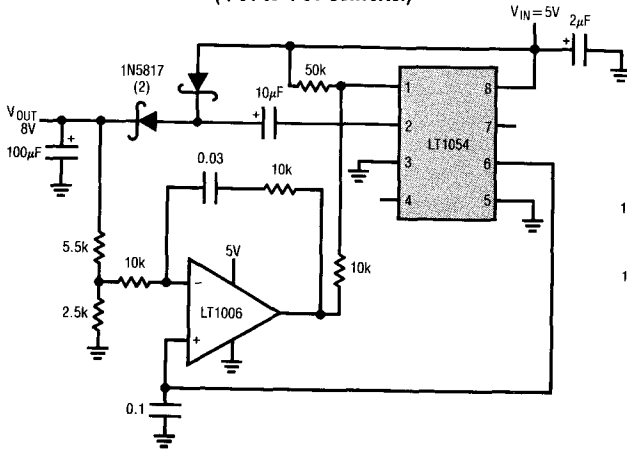


Digitally Programmable Negative Supply

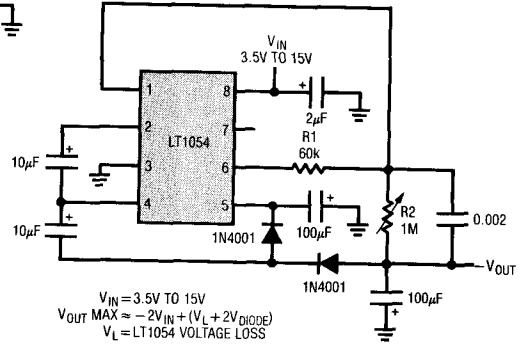


TYPICAL APPLICATIONS

Positive Doubler with Regulation (+5V to +8V Converter)



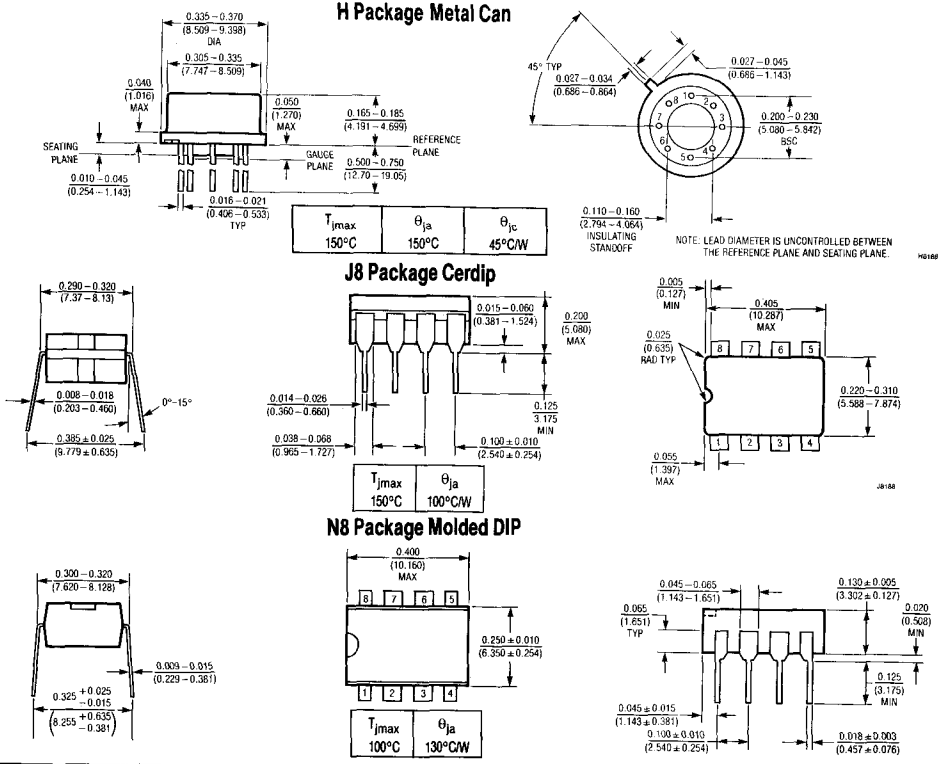
Negative Doubler with Regulator



$V_{IN} = 3.5V \text{ TO } 15V$
 $V_{OUT \text{ MAX}} \approx -2V_{IN} + (V_L + 2V_{D(10DE)})$
 $V_L = \text{LT1054 VOLTAGE LOSS}$

$$\frac{R_2}{R_1} = \left(\frac{|V_{OUT}|}{V_{REF} - 40\text{mV}} + 1 \right) = \left(\frac{|V_{OUT}|}{1.21V} + 1 \right)$$
 [REFER TO FIGURE 10]

PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.



Switched Capacitor Voltage Converter with Regulator

FEATURES

- 100mA Output Current
- Low Loss—1.1V at 100mA
- Operating Range 3.5V to 15V
- Reference and Error Amplifier for Regulation
- External Shutdown
- External Oscillator Sync
- Can be Paralleled

DESCRIPTION

The LT1054 is a monolithic, bipolar, switched capacitor voltage converter and regulator. The LT1054 provides higher output current than previously available converters with significantly lower voltage losses. An adaptive switch drive scheme optimizes efficiency over a wide range of output currents. Total voltage loss at 100mA output current is typically 1.1V. This holds true over the full supply voltage range of 3.5V to 15V. Quiescent current is typically 2.5 mA.

APPLICATIONS

- Voltage Inverter
- Negative Voltage Doubler
- Voltage Regulator
- Positive Voltage Doubler

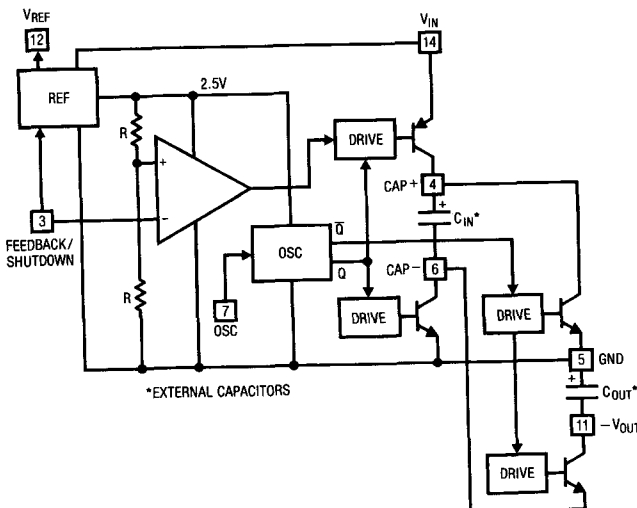
The LT1054 also provides regulation, a feature not previously available in switched capacitor voltage converters. By adding an external resistive divider, a regulated output can be obtained. This output will be regulated against changes in both input voltage and output current. The LT1054 can also be shut down by grounding the feedback pin. Supply current in shut down is less than 100 μ A.

The internal oscillator of the LT1054 runs at a nominal frequency of 25kHz. The oscillator pin can be used to adjust the switching frequency, or to externally synchronize the LT1054.

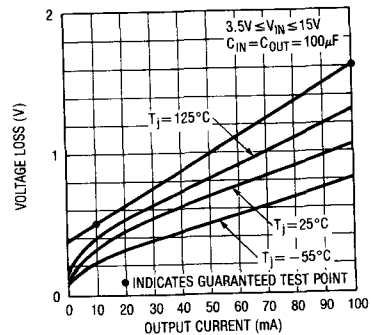
REFER TO TABLE OF CONTENTS FOR REVISED DATA LOCATION

5

BLOCK DIAGRAM



Voltage Loss



LT1054CS/LT1054IS

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (Note 1)	16V
Input Voltage (Pin 3)	$0V \leq V_{PIN3} \leq V^+$
Input Voltage (Pin 13)	$0V \leq V_{PIN13} \leq V_{REF}$
Operating Temperature Range	
LT1054C	0°C to 70°C
LT1054I	-40°C to 85°C
Junction Temperature (Note 2)	125°C
Storage Temperature Range	-65°C to 150°C
Lead Temperature (Soldering, 10 sec.)	300°C

PACKAGE/ORDER INFORMATION

<p>TOP VIEW</p> <p>S PACKAGE 16 LEAD PLASTIC SOL</p>	ORDER PART NUMBER
	LT1054CS LT1054IS
	PART MARKING
	LT1054CS LT1054IS

ELECTRICAL CHARACTERISTICS

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	
Supply Current	$I_{LOAD} = 0mA$ $V_{IN} = 3.5V$ $V_{IN} = 15V$	●	2.5 3.0	3.5 4.5	mA mA	
Supply Voltage Range		●	3.5	15	V	
Voltage Loss ($V_{IN} - V_{OUT} $)	$C_{IN} = C_{OUT} = 100\mu F$ Tantalum (Note 3) $I_{OUT} = 10mA$ $I_{OUT} = 100mA$	●	0.35 1.10	0.55 1.60	V V	
Output Resistance	$\Delta I_{OUT} = 10mA$ to 100mA (Note 4)	●	10	15	Ω	
Oscillator Frequency	$3.5V \leq V_{IN} \leq 15V$	●	15	25	35	kHz
Reference Voltage	$I_{REF} = 60\mu A$ $T_j = 25^\circ C$	●	2.35 2.25	2.50	2.65 2.75	V V
Regulated Voltage	$V_{IN} = 7V$, $T_j = 25^\circ C$ (Note 5)		-4.70	-5.00	-5.20	V
Line Regulation	$7V \leq V_{IN} \leq 12V$ (Note 5)	●	5	25	mV	
Load Regulation	$V_{IN} = 7V$ $100\Omega \leq R_L \leq 500\Omega$ (Note 5)	●	10	50	mV	
Maximum Switch Current			300		mA	
Supply Current In Shutdown	$V_{PIN3} = 0V$	●	100	150	μA	

The ● denotes specifications which apply over the full operating temperature range. For C grade parts these specifications also apply up to a junction temperature of 100°C.

Note 1: The absolute maximum supply voltage rating of 16V is for unregulated circuits. For regulation mode circuits with $V_{OUT} \leq 15V$ at Pin 11, this rating may be increased to 20V.

Note 2: The devices are guaranteed by design to be functional up to the absolute maximum junction temperature.

Note 3: For voltage loss tests, the device is connected as a voltage inverter, with Pins 3, 12, and 13 unconnected. The voltage losses may be higher in other configurations.

Note 4: Output resistance is defined as the slope of the curve, (ΔV_{OUT} vs ΔI_{OUT}), for output currents of 10 to 100 mA. This represents the linear portion of the curve. The incremental slope of the curve will be higher at currents < 10mA due to the characteristics of the switch transistors.

Note 5: All regulation specifications are for a device connected as a positive to negative converter/regulator with $R1 = 20k$, $R2 = 102.5k$, $C1 = 0.05\mu F$, $C_{IN} = 10\mu F$ tantalum, $C_{OUT} = 100\mu F$ tantalum.

FEATURES

- Wide Input Voltage Range 3V–60V
- Low Quiescent Current—6mA
- Internal 5A Switch (2.5A for LT1071)
- Very Few External Parts Required
- Self-Protected Against Overloads
- Operates in Nearly All Switching Topologies
- Shutdown Mode Draws Only 50 μ A Supply Current
- Flyback-Regulated Mode has Fully Floating Outputs
- Comes in Standard 5-Pin Packages
- Can be Externally Synchronized (Consult Factory)

APPLICATIONS

- Logic Supply 5V @ 10A
- 5V Logic to \pm 15V Op Amp Supply
- Offline Converter up to 200W
- Battery Upconverter
- Power Inverter (+ to -) or (- to +)
- Fully Floating Multiple Outputs
- For Lower Current Applications see LT1072

USER NOTE:

This data sheet is only intended to provide specifications, graphs, and a general functional description of the LT1070/LT1071. Application circuits are included to show the capability of the LT1070/LT1071. A complete design manual (AN-19) should be obtained to assist in developing new designs. This manual contains a comprehensive discussion of both the LT1070 and the external components used with it, as well as complete formulas for calculating the values of these components. The manual can also be used for the LT1071 by factoring in the lower switch current rating. A second application note, AN-25, which details off-line applications is available.

DESCRIPTION

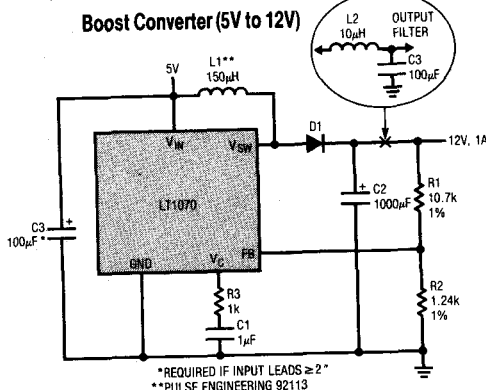
The LT1070 and LT1071 are monolithic high power switching regulators. They can be operated in all standard switching configurations including buck, boost, flyback, forward, inverting and "Cuk". A high current, high efficiency switch is included on the die along with all oscillator, control, and protection circuitry. Integration of all functions allows the LT1070/LT1071 to be built in a standard 5-pin TO-3 or TO-220 power package. This makes it extremely easy to use and provides "bust proof" operation similar to that obtained with 3-pin linear regulators.

The LT1070/LT1071 operates with supply voltages from 3V to 60V, and draws only 6mA quiescent current. It can deliver load power up to 100 watts with no external power devices. By utilizing current-mode switching techniques, it provides excellent AC and DC load and line regulation.

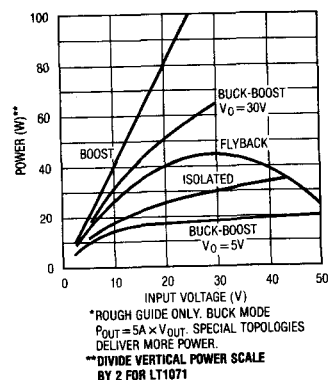
The LT1070/LT1071 has many unique features not found even on the vastly more difficult to use low power control chips presently available. It uses adaptive anti-sat switch drive to allow very wide ranging load currents with no loss in efficiency. An externally activated shutdown mode reduces total supply current to 50 μ A typical for standby operation. Totally isolated and regulated outputs can be generated by using the optional "flyback regulation mode" built into the LT1070/LT1071, without the need for opto-couplers or extra transformer windings.

5

TYPICAL APPLICATION



Maximum Output Power*



ABSOLUTE MAXIMUM RATINGS

Supply Voltage
 LT1070/71HV (See Note 1) 60V
 LT1070/71 (See Note 1) 40V

Switch Output Voltage
 LT1070/71HV 75V
 LT1070/71 65V

Feedback Pin Voltage (Transient, 1ms) ± 15V

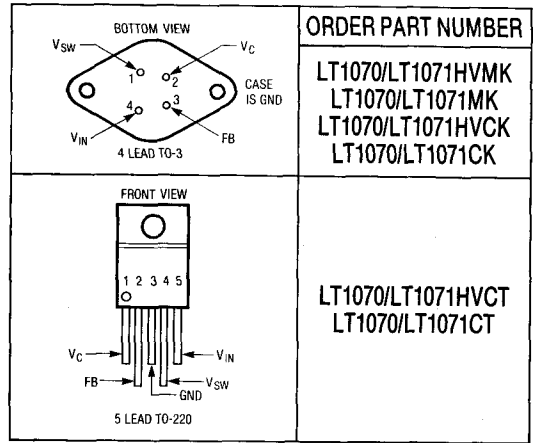
Operating Junction Temperature Range
 LT1070/71HVM, LT1070/71M -55°C to +150°C
 LT1070/71HVC, LT1070/71C (Oper.) 0°C to +100°C
 LT1070/71HVC, LT1070/71C (Sh. Ckt.)... 0°C to +125°C

Storage Temperature Range -65°C to +150°C

Lead Temperature (Soldering, 10sec) 300°C

Note 1: Minimum switch "on" time for the LT1070/LT1071 in current limit is ≈ 1.0μsec. This limits the maximum input voltage during short circuit conditions, in the buck and inverting modes only, to ≈ 35V. Normal (unshorted) conditions are not affected. Mask changes are being implemented which will reduce minimum "on" time to ≤ 1μsec, increasing maximum short circuit input voltage above 40V. If the present LT1070/LT1071 (contact factory for package date code) is being operated in the buck or inverting mode at high input voltages and short circuit conditions are expected, a resistor must be placed in series with the inductor, as follows:

PACKAGE/ORDER INFORMATION



The value of the resistor is given by:

$$R = \frac{t \cdot f \cdot V_{IN} - V_f}{I_{LIMIT}} - R_L$$

t = Minimum "on" time of LT1070/LT1071 in current limit, ≈ 1μs

f = Operating frequency (40kHz)

V_f = Forward voltage of external catch diode at I_{LIMIT}

I_{LIMIT} = Current limit of LT1070 (≈ 8A), LT1071 (≈ 4A)

R_L = Internal series resistance of inductor

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, V_{IN} = 15V, V_C = 0.5V, V_{FB} = V_{REF}, output pin open.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V _{REF}	Reference Voltage	Measured at Feedback Pin	1.224 1.214	1.244 1.244	1.264 1.274	V
I _B	Feedback Input Current	V _{FB} = V _{REF}		350	750 1100	nA
g _m	Error Amplifier Transconductance	ΔI _C = ± 25μA	3000 2400	4400	6000 7000	μmho
	Error Amplifier Source or Sink Current	V _C = 1.5V	150 120	200	350 400	μA μA
	Error Amplifier Clamp Voltage	Hi Clamp, V _{FB} = 1V Lo Clamp, V _{FB} = 1.5V	1.8 0.25	0.38	2.3 0.52	V V
	Reference Voltage Line Regulation	3V ≤ V _{IN} ≤ V _{MAX}			0.03	%/V
A _v	Error Amplifier Voltage Gain	0.7V ≤ V _C ≤ 1.4V	500	800	2000	V/V
	Minimum Input Voltage			2.6	3.0	V
I _Q	Supply Current	3V ≤ V _{IN} ≤ V _{MAX} , V _C = 0.6V		6	9	mA
	Control Pin Threshold	Duty Cycle = 0	0.8 0.6	0.9	1.08 1.25	V
	Normal/Flyback Threshold on Feedback Pin		0.4	0.45	0.54	V
V _{FB}	Flyback Reference Voltage	I _{FB} = 50μA	15 14	16.3	17.6 18	V

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, $V_{IN} = 15V$, $V_C = 0.5V$, $V_{FB} = V_{REF}$, output pin open.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	
V_{FB}	Change in Flyback Reference Voltage	$0.05 \leq I_{FB} \leq 1mA$	4.5	6.8	8.5	V	
	Flyback Reference Voltage Line Regulation	$I_{FB} = 50\mu A$ $3V \leq V_{IN} \leq V_{MAX}$		0.01	0.03	%/V	
	Flyback Amplifier Transconductance (gm)	$\Delta I_C = \pm 10\mu A$	150	300	500	μmho	
BV	Output Switch Breakdown Voltage	$V_C = 1.5V$ Source	●	15	32	70	μA
		$I_{FB} = 50\mu A$ Sink	●	25	40	70	μA
V_{SAT}	Output Switch (Note 1) "On" Resistance	LT1070	●		0.15	0.24	Ω
		LT1071	●		0.3	0.5	Ω
I_{LIM}	Switch Current Limit (LT1070)	Duty Cycle $\leq 50\%$ $T_j \geq 25^\circ C$	●	5		10	A
		Duty Cycle $\leq 50\%$ $T_j < 25^\circ C$	●	5		11	A
I_{LIM}	Switch Current Limit (LT1071)	Duty Cycle = 80% (Note 2)	●	4		10	A
		Duty Cycle $\leq 50\%$ $T_j \geq 25^\circ C$	●	2.5		5	A
		Duty Cycle $\leq 50\%$ $T_j < 25^\circ C$	●	2.5		5.5	A
$\frac{\Delta I_{IN}}{\Delta I_{SW}}$	Supply Current Increase During Switch On-Time				25	35	mA/A
f	Switching Frequency		●	35	40	45	kHz
DC (max)	Maximum Switch Duty Cycle			90	92	97	%
	Flyback Sense Delay Time				1.5		μs
	Shutdown Mode Supply Current	$3V \leq V_{IN} \leq V_{MAX}$ $V_C = 0.05V$			100	250	μA
	Shutdown Mode Threshold Voltage	$3V \leq V_{IN} \leq V_{MAX}$	●	100	150	250	mV
				50	300		mV

The ● denotes the specifications which apply over the full operating temperature range.

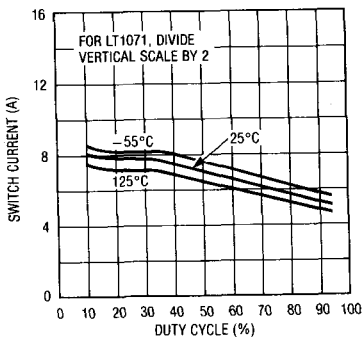
Note 1: Measured with V_C in hi clamp, $V_{FB} = 0.8V$, $I_{SW} = 4A$ for LT1070 and $2A$ for LT1071.

Note 2: For duty cycles (DC) between 50% and 80%, minimum guaranteed switch current is given by $I_{LIM} = 3.33(2 - DC)$ for the LT1070 and $I_{LIM} = 1.67(2 - DC)$ for the LT1071.

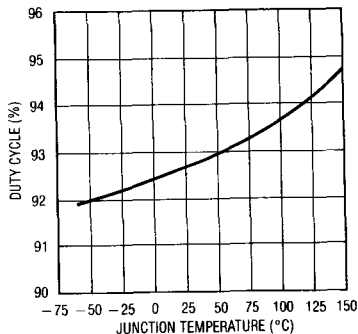
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TYPICAL PERFORMANCE CHARACTERISTICS

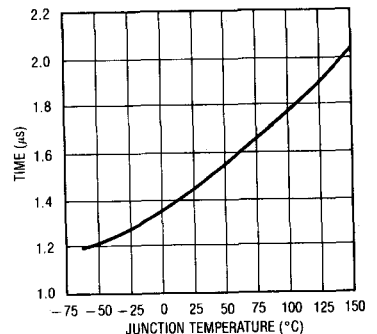
Switch Current Limit vs Duty Cycle



Maximum Duty Cycle

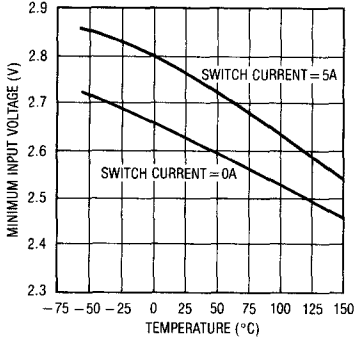


Flyback Blanking Time

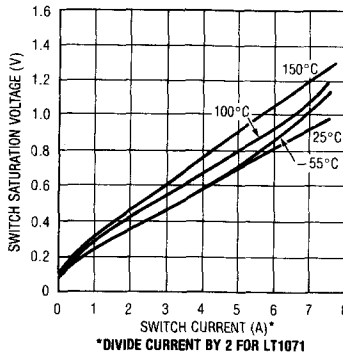


TYPICAL PERFORMANCE CHARACTERISTICS

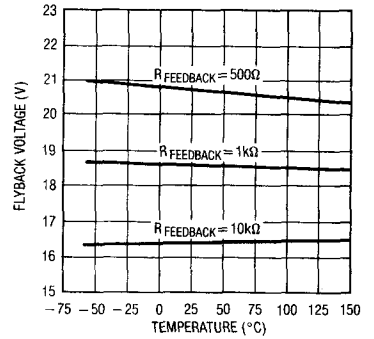
Minimum Input Voltage



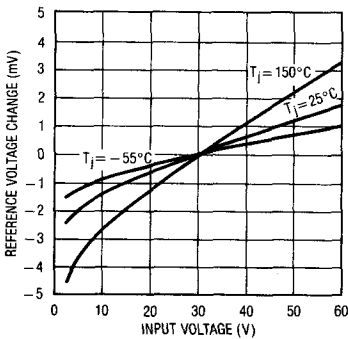
Switch Saturation Voltage



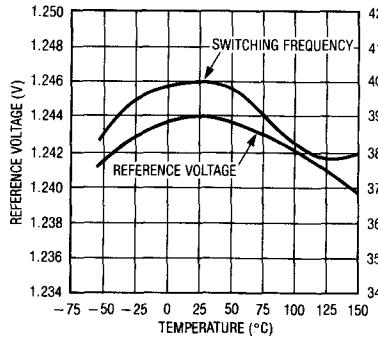
Isolated Mode Flyback Reference Voltage



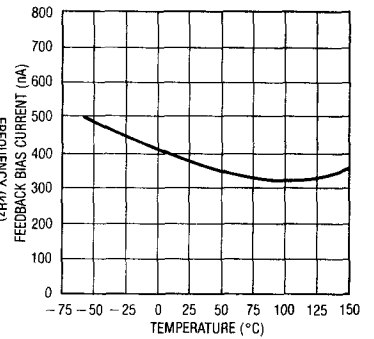
Line Regulation



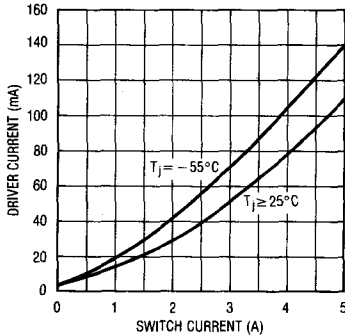
Reference Voltage vs Temperature



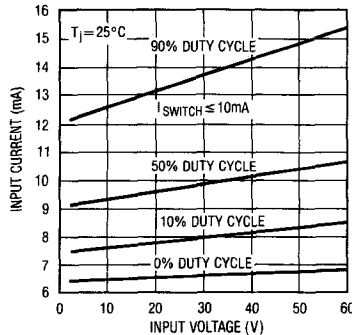
Feedback Bias Current vs Temperature



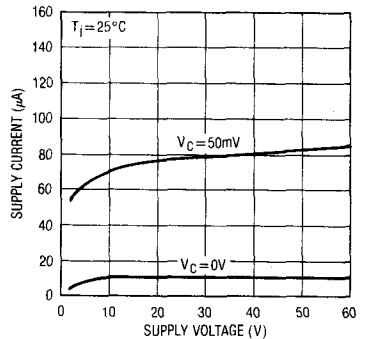
Driver Current* vs Switch Current



Supply Current vs Input Voltage*



Supply Current vs Supply Voltage (Shutdown Mode)

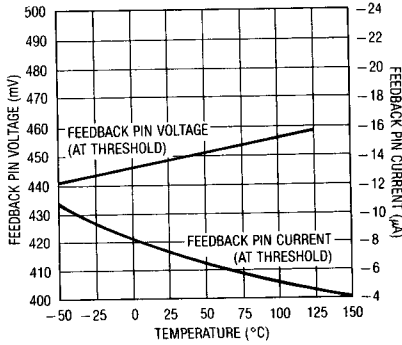


*AVERAGE LT1070 POWER SUPPLY CURRENT IS FOUND BY MULTIPLYING DRIVER CURRENT BY DUTY CYCLE, THEN ADDING QUIESCENT CURRENT.

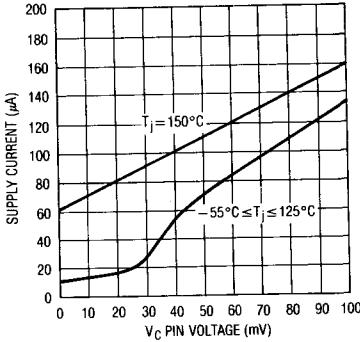
*UNDER VERY LOW OUTPUT CURRENT CONDITIONS, DUTY CYCLE FOR MOST CIRCUITS WILL APPROACH 10% OR LESS.

TYPICAL PERFORMANCE CHARACTERISTICS

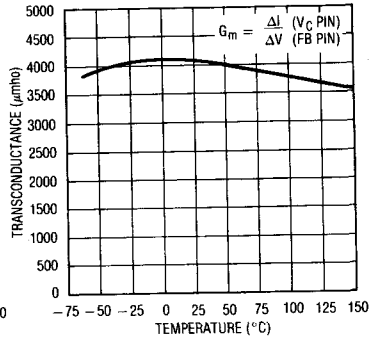
Normal/Flyback Mode Threshold on Feedback Pin



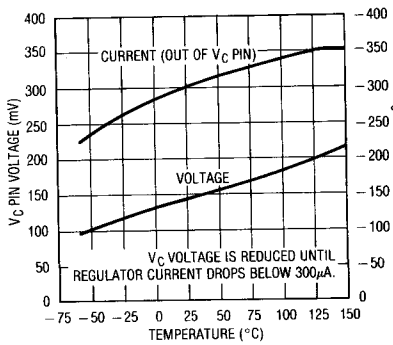
Shutdown Mode Supply Current



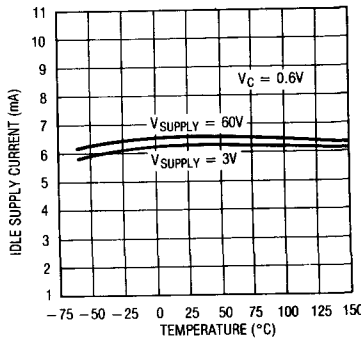
Error Amplifier Transconductance



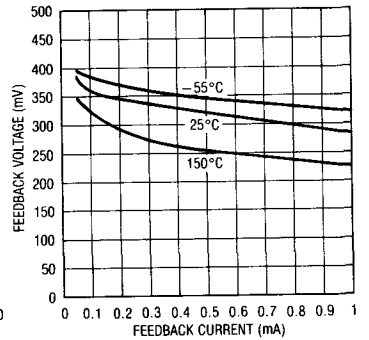
Shutdown Thresholds



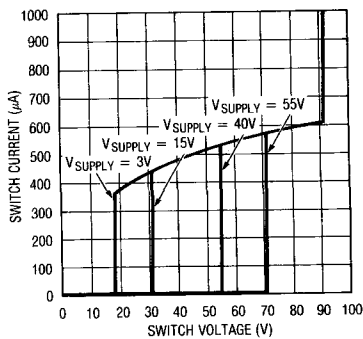
Idle Supply Current vs Temperature



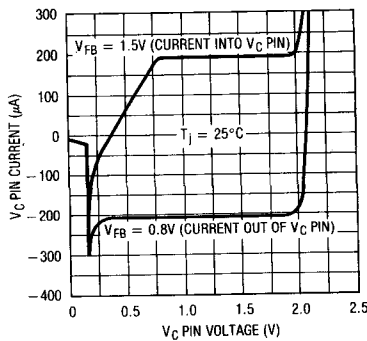
Feedback Pin Clamp Voltage



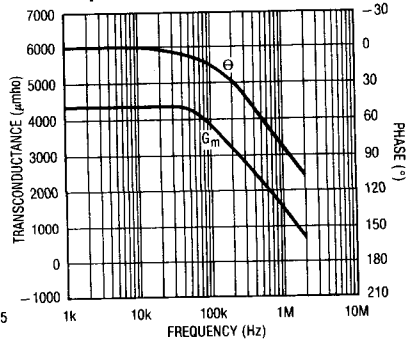
Switch "Off" Characteristics



Vc Pin Characteristics

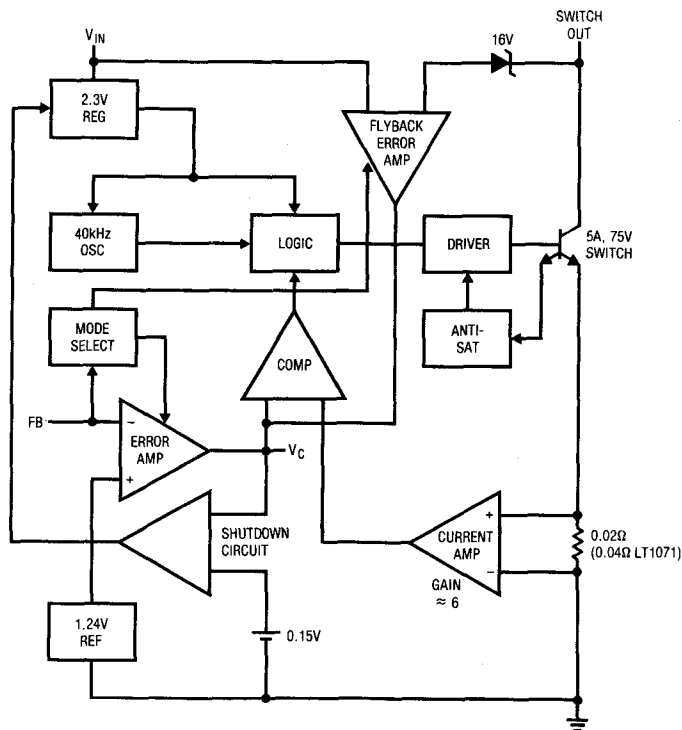


Transconductance of Error Amplifier



5

BLOCK DIAGRAM



LT1070/LT1071 OPERATION

The LT1070/LT1071 is a current mode switcher. This means that switch duty cycle is directly controlled by switch current rather than by output voltage. Referring to the block diagram, the switch is turned "on" at the start of each oscillator cycle. It is turned "off" when switch current reaches a predetermined level. Control of output voltage is obtained by using the output of a voltage sensing error amplifier to set current trip level. This technique has several advantages. First, it has immediate response to input voltage variations, unlike ordinary switchers which have notoriously poor line transient response. Second, it reduces the 90° phase shift at midfrequencies in the energy storage inductor. This greatly simplifies closed loop frequency compensation under widely varying input voltage or output load conditions. Finally, it allows simple pulse-by-pulse current limiting to provide maximum switch protection under output overload or short condi-

tions. A low-dropout internal regulator provides a 2.3V supply for all internal circuitry on the LT1070/LT1071. This low-dropout design allows input voltage to vary from 3V to 60V with virtually no change in device performance. A 40kHz oscillator is the basic clock for all internal timing. It turns "on" the output switch via the logic and driver circuitry. Special adaptive anti-sat circuitry detects onset of saturation in the power switch and adjusts driver current instantaneously to limit switch saturation. This minimizes driver dissipation and provides very rapid turn-off of the switch.

A 1.2V bandgap reference biases the positive input of the error amplifier. The negative input is brought out for output voltage sensing. This feedback pin has a second function; when pulled low with an external resistor, it programs the LT1070/LT1071 to disconnect the main error amplifier output

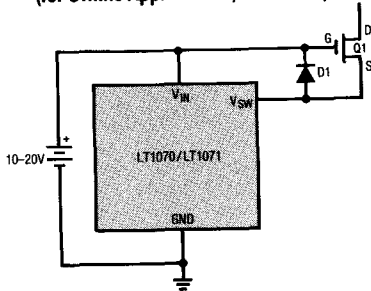
LT1070/LT1071 OPERATION

and connects the output of the flyback amplifier to the comparator input. The LT1070/LT1071 will then regulate the value of the flyback pulse with respect to the supply voltage. This flyback pulse is directly proportional to output voltage in the traditional transformer coupled flyback topology regulator. By regulating the amplitude of the flyback pulse, the output voltage can be regulated with no direct connection between input and output. The output is fully floating up to the breakdown voltage of the transformer windings. Multiple floating outputs are easily obtained with additional windings. A special delay network inside the LT1070/LT1071 ignores the leakage inductance spike at the leading edge of the flyback pulse to improve output regulation.

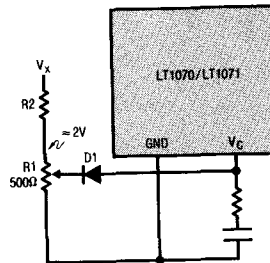
The error signal developed at the comparator input is brought out externally. This pin (V_C) has four different functions. It is used for frequency compensation, current limit adjustment, soft starting, and total regulator shutdown. During normal regulator operation this pin sits at a voltage between 0.9V (low output current) and 2.0V (high output current). The error amplifiers are current output (gm) types, so this voltage can be externally clamped for adjusting current limit. Likewise, a capacitor coupled external clamp will provide soft start. Switch duty cycle goes to zero if the V_C pin is pulled to ground through a diode, placing the LT1070/LT1071 in an idle mode. Pulling the V_C pin below 0.15V causes total regulator shutdown, with only 50 μ A supply current for shutdown circuitry biasing. See AN-19 for full application details.

TYPICAL APPLICATIONS (Note that maximum output currents are divided by 2 for LT1071.)

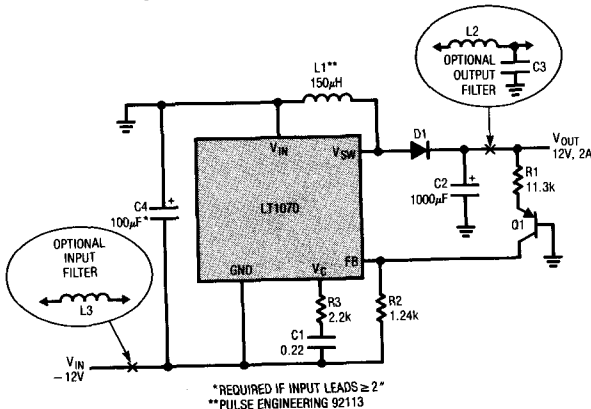
Driving High Voltage FET
(for Offline Applications, See AN-25)



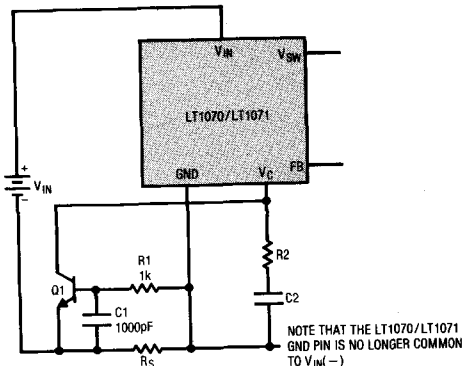
External Current Limit



Negative to Positive Buck-Boost Converter

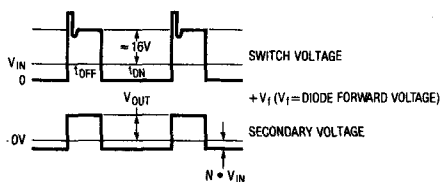
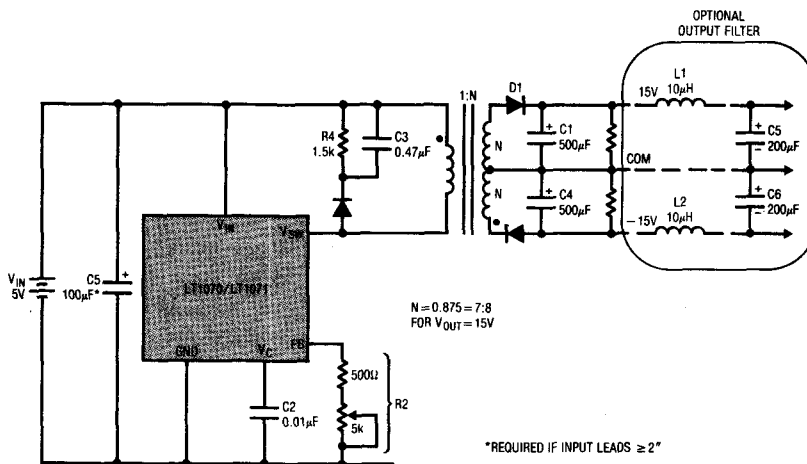


External Current Limit

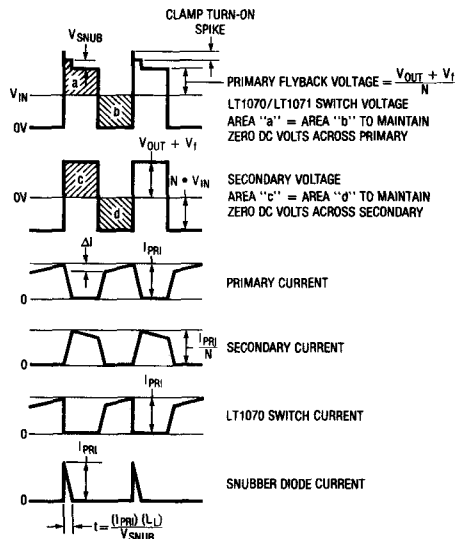
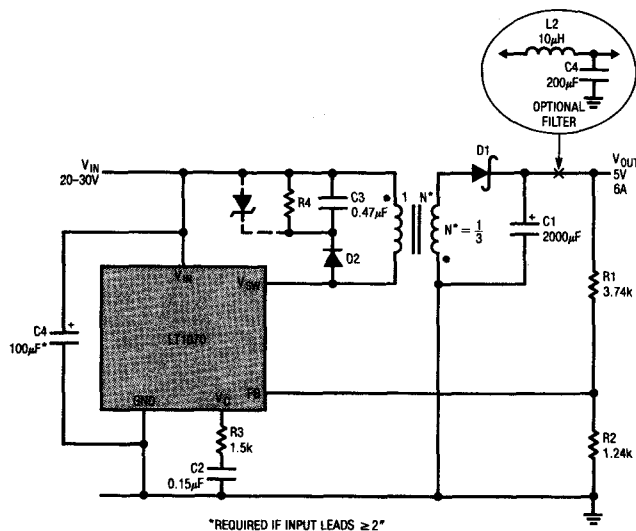


TYPICAL APPLICATIONS

Totally Isolated Converter

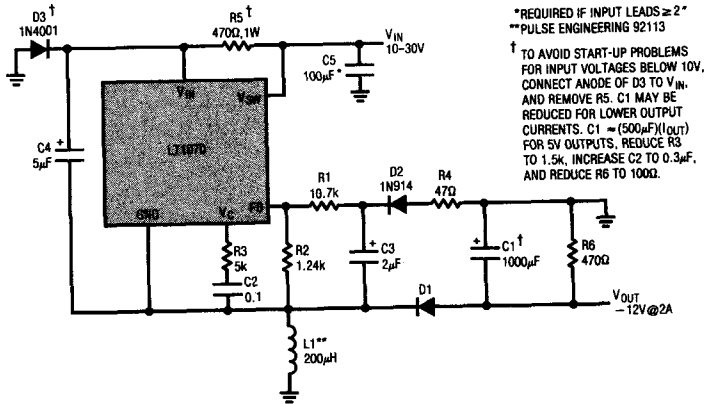


Flyback Converter

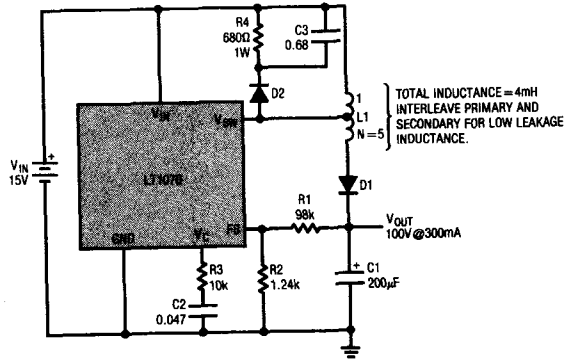


TYPICAL APPLICATIONS

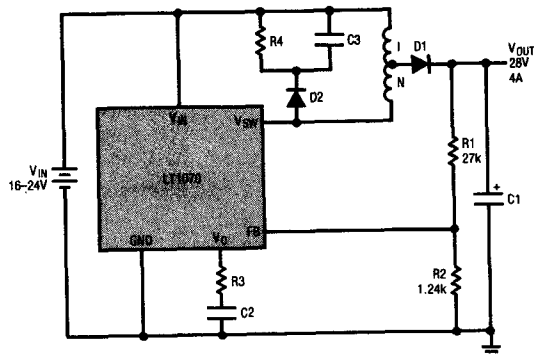
Positive to Negative Buck-Boost Converter



Voltage Boosted Boost Converter

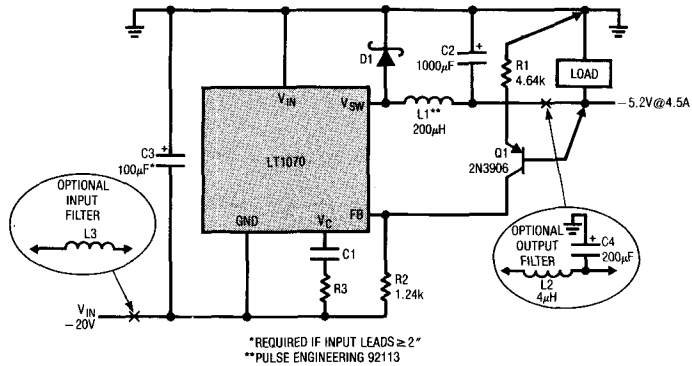


Current Boosted Boost Converter

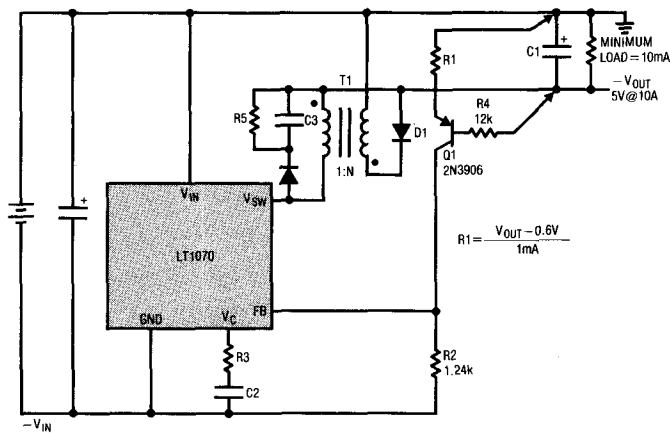


TYPICAL APPLICATIONS

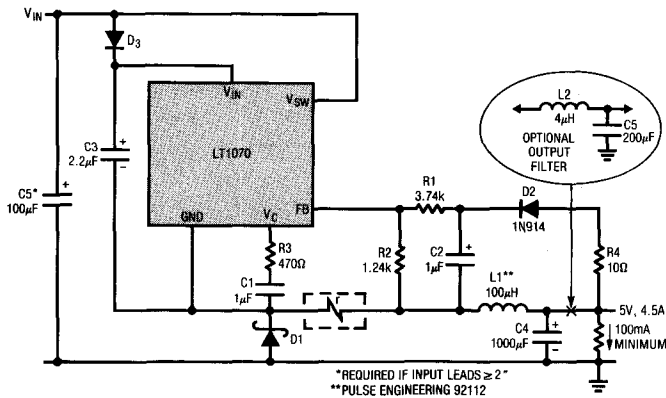
Negative Buck Converter



Negative Current Boosted Buck Converter

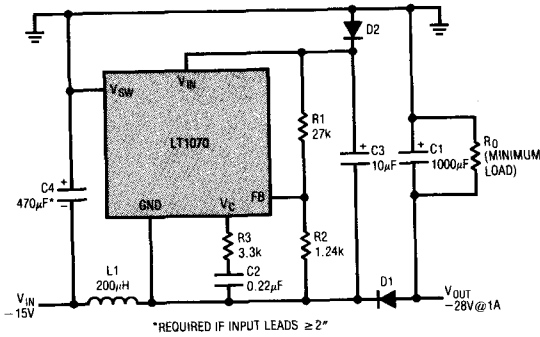


Positive Buck Converter

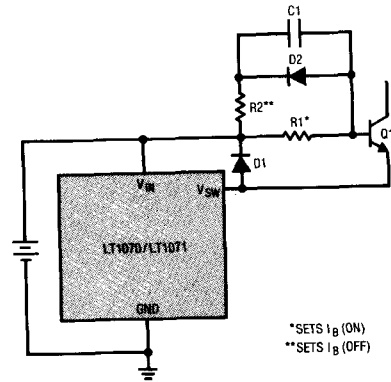


TYPICAL APPLICATIONS

Negative Boost Regulator

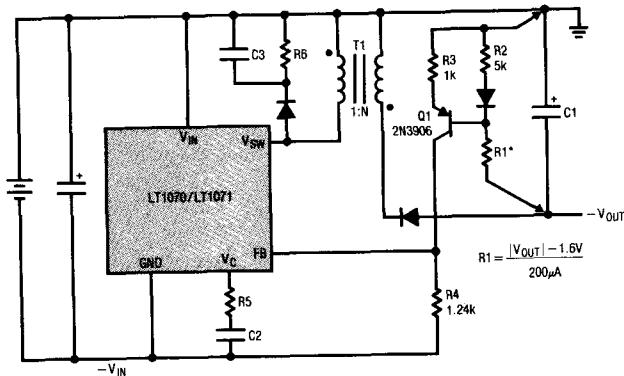


Driving High Voltage NPN



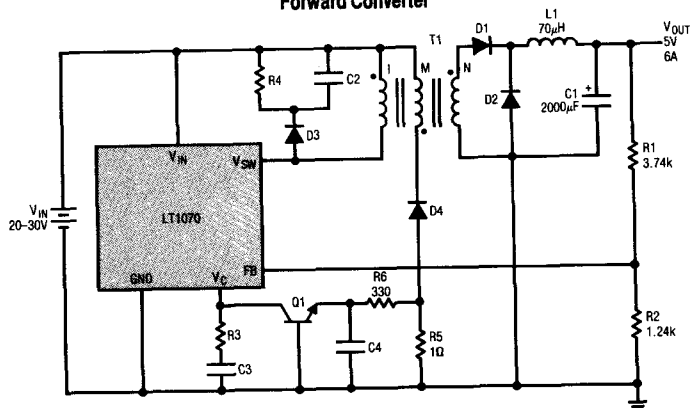
*SETS I_B (ON)
 **SETS I_B (OFF)

Negative Input-Negative Output Flyback Converter



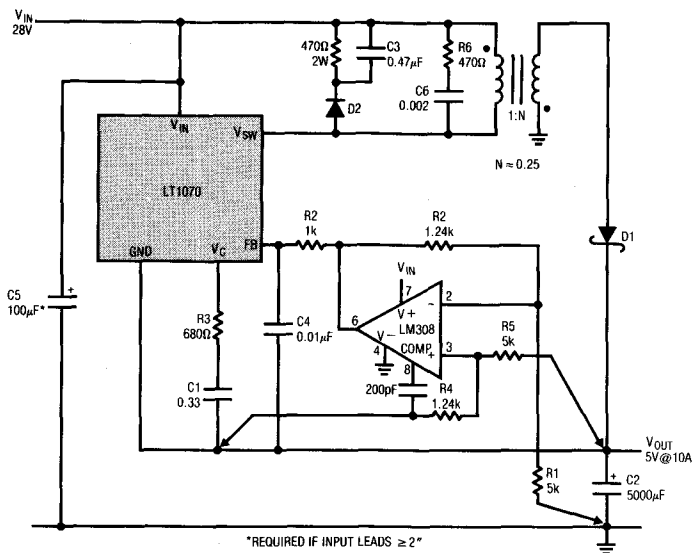
5

Forward Converter



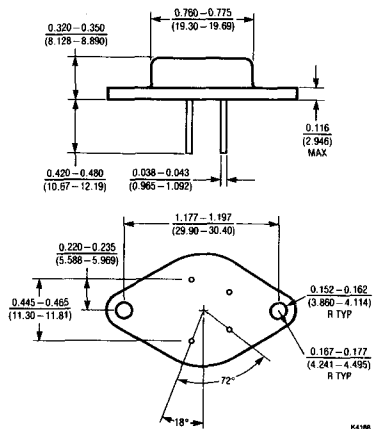
TYPICAL APPLICATIONS

Positive Current Boosted Buck Converter

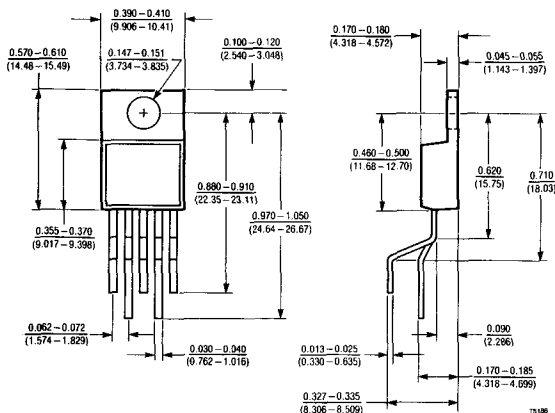


PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

TO-3 Type Metal Can (Steel) K Package



TO-220 Type Plastic T Package



	T_{JMAX}	θ_{JC}	θ_{JA}
LT1070MK, LT1070HVMK	150°C	2°C/W	35°C/W
LT1070CK, LT1070HVCK	100°C	2°C/W	35°C/W
LT1071MK, LT1071HVMK	150°C	4°C/W	35°C/W
LT1071CK, LT1071HVCK	100°C	4°C/W	35°C/W

	T_{JMAX}	θ_{JC}	θ_{JA}
LT1070CT, LT1070HVCT	100°C	2°C/W	75°C/W
LT1071CT, LT1071HVCT	100°C	4°C/W	75°C/W

1.25A High Efficiency Switching Regulator

FEATURES

- Available in MiniDIP, TO-220, and TO-3 Packages
- Wide Input Voltage Range 3V-60V
- Low Quiescent Current—6mA
- Internal 1.25A Switch
- Very Few External Parts Required
- Self-Protected Against Overloads
- Operates in Nearly All Switching Topologies
- Shutdown Mode Draws Only 50 μ A Supply Current
- Flyback-Regulated Mode has Fully Floating Outputs
- Can be Externally Synchronized

APPLICATIONS

- Logic Supply 5V @ 2.5A
- 5V Logic to \pm 15V Op Amp Supply
- Offline Converter up to 50W
- Battery Upconverter
- Power Inverter (+ to -) or (- to +)
- Fully Floating Multiple Outputs
- Driver for High Current Supplies

USER NOTE:

This data sheet is only intended for reference. Specifications, graphs, and a general functional description of the LT1072. Application circuits are included to show the capability of the LT1072. A complete design manual (AN-19) should be obtained to assist in developing new designs. This manual contains a comprehensive discussion of both the LT1070 and the external components used with it, as well as complete formulas for calculating the values of these components. The manual can also be used for the LT1072 by factoring in the lower switch current rating.

DESCRIPTION

The LT1072 is a monolithic high power switching regulator. It can be operated in all standard switching configurations including buck, boost, flyback, forward, inverting and "Cuk". A high current, high efficiency switch is included on the die along with all oscillator, control, and protection circuitry. Integration of all functions allows the LT1072 to be built in a standard 5-pin TO-3 or TO-220 power package as well as the 8-pin miniDIP. This makes it extremely easy to use and provides "bust proof" operation similar to that obtained with 3-pin linear regulators.

The LT1072 operates with \pm 50V voltages from 3V to 60V, and draws only 6mA quiescent current. It can deliver load power up to 20 watts with no external power devices. By utilizing current mode switching techniques, it provides excellent average load and line regulation.

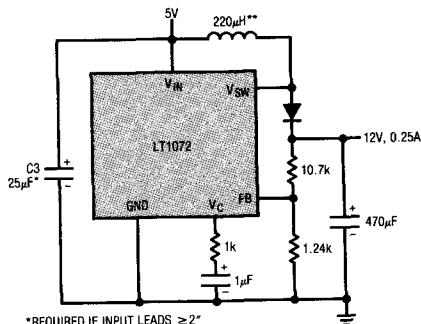
The LT1072 has many unique features not found even on other switching regulators. It is much more difficult to use low power control chips presently available. It uses adaptive anti-sat switch drive to allow very wide ranging load currents with no loss in efficiency. An externally activated shutdown mode reduces total supply current to 50 μ A typical for standby operation. Totally isolated and regulated outputs can be generated by using the optional "flyback regulation mode" built into the LT1072, without the need for opto-couplers or extra transformer windings.

REFER TO TABLE OF CONTENTS FOR REVISED DATA LOCATION

5

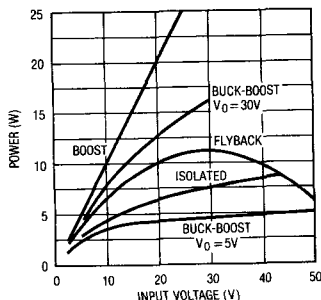
TYPICAL APPLICATION

Boost Converter (5V to 12V)



*REQUIRED IF INPUT LEADS $\geq 2^{\circ}$
 **PULSE ENGINEERING 52626

Maximum Output Power*



*ROUGH GUIDE ONLY. BUCK MODE $P_{OUT} = 1A \times V_{OUT}$.
 MINIDIP OUTPUT POWER MAY BE LIMITED BY PACKAGE TEMPERATURE RISE AT HIGH INPUT VOLTAGES OR HIGH DUTY CYCLES.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	
LT1072HV (See Note 1)	60V
LT1072 (See Note 1)	40V
Switch Output Voltage	
LT1072HV	75V
LT1072	65V
Feedback Pin Voltage (Transient, 1ms)	± 15V
Operating Junction Temperature Range	
LT1072HVM, LT1072M	-55°C to +150°C
LT1072HVC, LT1072C (Oper.)	0°C to +100°C
LT1072HVC, LT1072C (Sh. Ckt.)	0°C to +125°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 10sec)	300°C

Note 1: Minimum switch "on" time for the LT1072 in current limit is ≈ 0.7µsec. This limits the maximum input voltage during short circuit conditions, in the buck and inverting modes only, to ≈ 40V. Normal (unshorted) conditions are not affected. If the LT1072 is being operated in the buck or inverting mode at high input voltages and short circuit conditions are expected, a resistor must be placed in series with the inductor, as follows:

The value of the resistor is given by:

$$R = \frac{(t)(f)(V_{IN}) - V_f}{I_{(LIMIT)}} - R_L$$

PACKAGE/ORDER INFORMATION

	ORDER PART NUMBER
	LT1072HVMK LT1072MK LT1072HVCK LT1072CK
	LT1072HVCT LT1072CT
	LT1072MJ8 LT1072CJ8 LT1072CN8

t = Minimum "on" time of LT1072 in current limit, ≈ 0.7µs

f = Operating frequency (40kHz)

V_f = Forward voltage of external catch diode at I_(LIMIT)

I_(LIMIT) = Current limit of LT1072 (2A)

R_L = Internal series resistance of inductor

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, V_{IN} = 15V, V_C = 0.5V, V_{FB} = V_{REF}, output pin open.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V _{REF}	Reference Voltage	Measured at Feedback Pin V _C = 0.8V	1.224	1.244	1.264	V
I _B	Feedback Input Current	V _{FB} = V _{REF}		350	750	nA
g _m	Error Amplifier Transconductance	ΔI _C = ± 25µA	3000	4400	6000	µmho
	Error Amplifier Source or Sink Current	V _C = 1.5V	150	200	350	µA
	Error Amplifier Clamp Voltage	Hi Clamp, V _{FB} = 1V Lo Clamp, V _{FB} = 1.5V	1.8	0.25	2.3	V
	Reference Voltage Line Regulation	3V ≤ V _{IN} ≤ V _{MAX} V _C = 0.8V			0.03	%/V
A _V	Error Amplifier Voltage Gain	0.9V ≤ V _C ≤ 1.4V	500	800	2000	V/V
	Minimum Input Voltage			2.6	3.0	V
I _Q	Supply Current	3V ≤ V _{IN} ≤ V _{MAX} , V _C = 0.6V		6	9	mA
	Control Pin Threshold	Duty Cycle = 0	0.8	0.9	1.08	V
	Normal/Flyback Threshold on Feedback Pin		0.6	0.9	1.25	V
			0.4	0.45	0.54	V

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, $V_{IN} = 15V$, $V_C = 0.5V$, $V_{FB} = V_{REF}$, output pin open.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{FB}	Flyback Reference Voltage	$I_{FB} = 50\mu A$	15 14	16.3	17.6 18	V
	Change in Flyback Reference Voltage	$0.05 \leq I_{FB} \leq 1mA$	4.5	6.8	8.5	V
	Flyback Reference Voltage Line Regulation	$I_{FB} = 50\mu A$ $3V \leq V_{IN} \leq V_{MAX}$		0.01	0.03	%/V
	Flyback Amplifier Transconductance (gm)	$\Delta I_C = \pm 10\mu A$	150	300	500	μmho
	Flyback Amplifier Source and Sink Current	$V_C = 0.6V$ Source $I_{FB} = 50\mu A$ Sink	15 25	32 40	70 70	μA μA
BV	Output Switch Breakdown Voltage	$3V \leq V_{IN} \leq V_{MAX}$ LT1072	65	90		V
		$I_{SW} = 5mA$ LT1072HV	75	90		V
V_{SAT}	Output Switch (Note 1) "On" Resistance	$I_{SW} = 1.25A$		0.6	1	Ω
	Control Voltage to Switch Current Transconductance			2		A/V
I_{LIM}	Switch Current Limit	Duty Cycle $\leq 50\%$ $T_j \geq 25^\circ C$	1.25		3	A
		Duty Cycle $\leq 50\%$ $T_j < 25^\circ C$	1.25		3.5	A
		Duty Cycle = 80% (Note 2)	1		2.5	A
$\frac{\Delta I_{IN}}{\Delta I_{SW}}$	Supply Current Increase During Switch On-Time			25	35	mA/A
f	Switching Frequency		35 33	40	45 47	kHz
DC (max)	Maximum Switch Duty Cycle		90	92	97	%
	Flyback Sense Delay Time			1.5		μs
	Shutdown Mode Supply Current	$3V \leq V_{IN} \leq V_{MAX}$ $V_C = 0.05V$		100	250	μA
	Shutdown Mode Threshold Voltage	$3V \leq V_{IN} \leq V_{MAX}$	100 50	150	250 300	mV mV

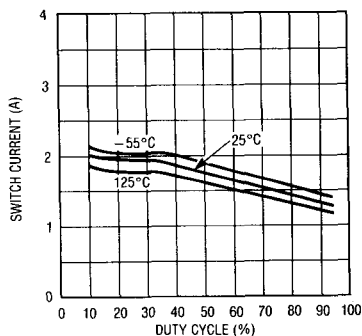
The ● denotes the specifications which apply over the full operating temperature range.

Note 1: Measured with V_C in hi clamp, $V_{FB} = 0.8V$.

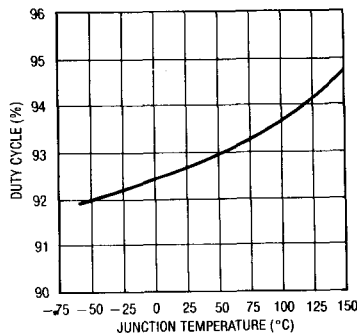
Note 2: For duty cycles (DC) between 50% and 80%, minimum guaranteed switch current is given by $I_{LIM} = 0.833(2 - DC)$.

TYPICAL PERFORMANCE CHARACTERISTICS

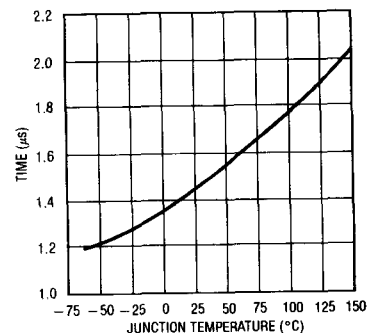
Switch Current Limit vs Duty Cycle



Maximum Duty Cycle

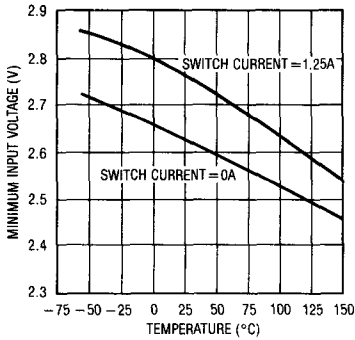


Flyback Blanking Time

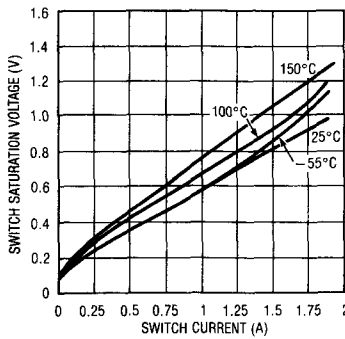


TYPICAL PERFORMANCE CHARACTERISTICS

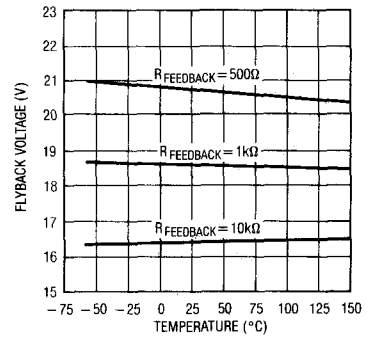
Minimum Input Voltage



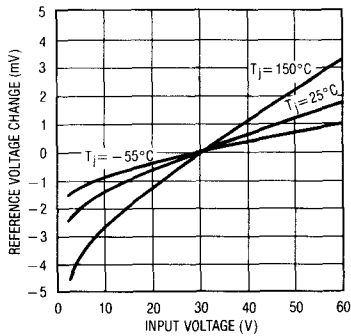
Switch Saturation Voltage



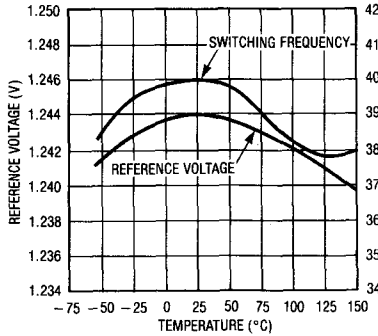
Isolated Mode Flyback Reference Voltage



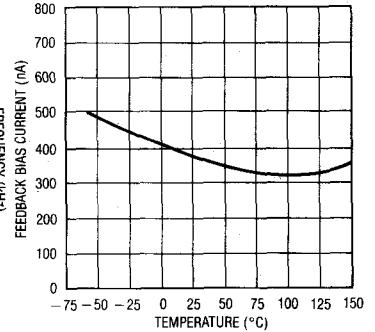
Line Regulation



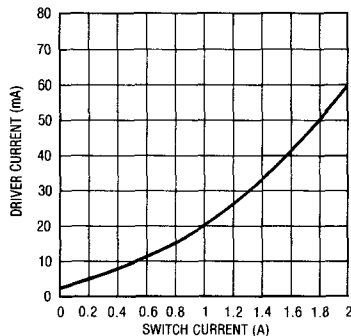
Reference Voltage and Switching Frequency vs Temperature



Feedback Bias Current vs Temperature

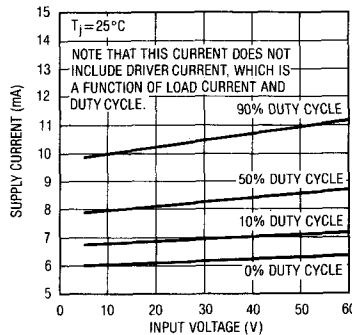


Driver Current* vs Switch Current



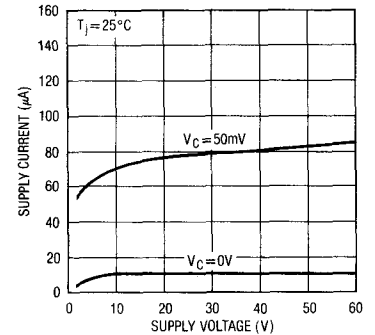
*AVERAGE LT1072 POWER SUPPLY CURRENT IS FOUND BY MULTIPLYING DRIVER CURRENT BY DUTY CYCLE, THEN ADDING QUIESCENT CURRENT.

Supply Current vs Input Voltage*



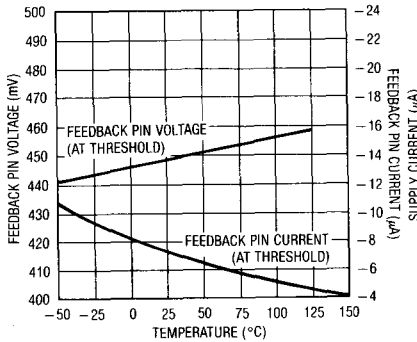
*UNDER VERY LOW OUTPUT CURRENT CONDITIONS, DUTY CYCLE FOR MOST CIRCUITS WILL APPROACH 10% OR LESS.

Supply Current vs Supply Voltage (Shutdown Mode)

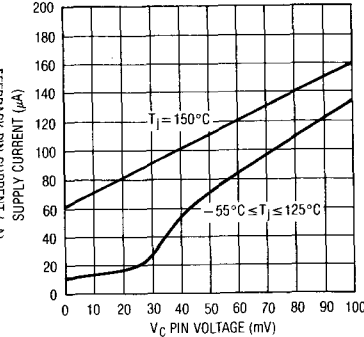


TYPICAL PERFORMANCE CHARACTERISTICS

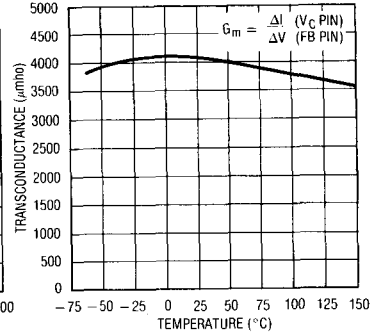
Normal/Flyback Mode Threshold on Feedback Pin



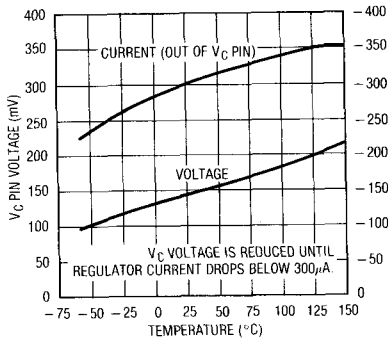
Shutdown Mode Supply Current



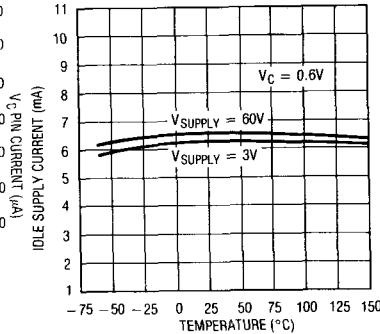
Error Amplifier Transconductance



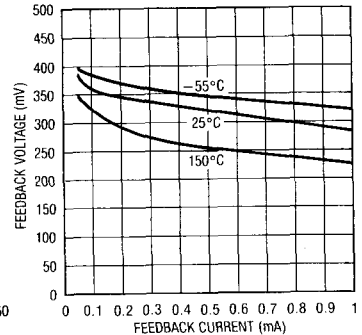
Shutdown Thresholds



Idle Supply Current vs Temperature

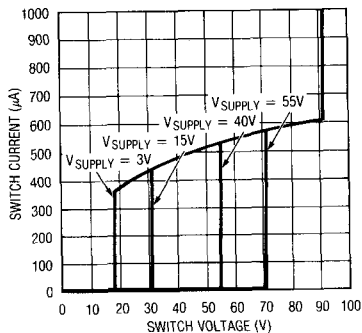


Feedback Pin Clamp Voltage

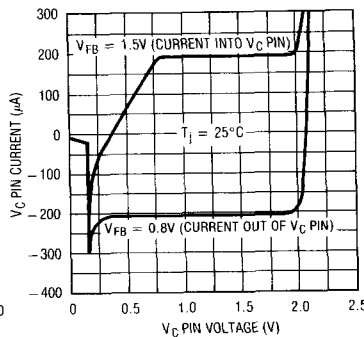


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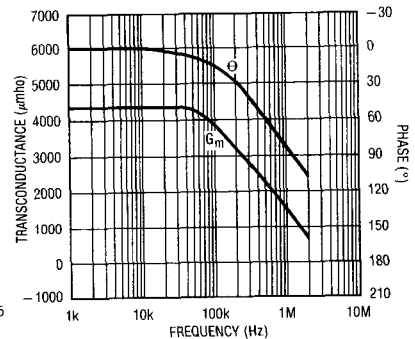
Switch "Off" Characteristics



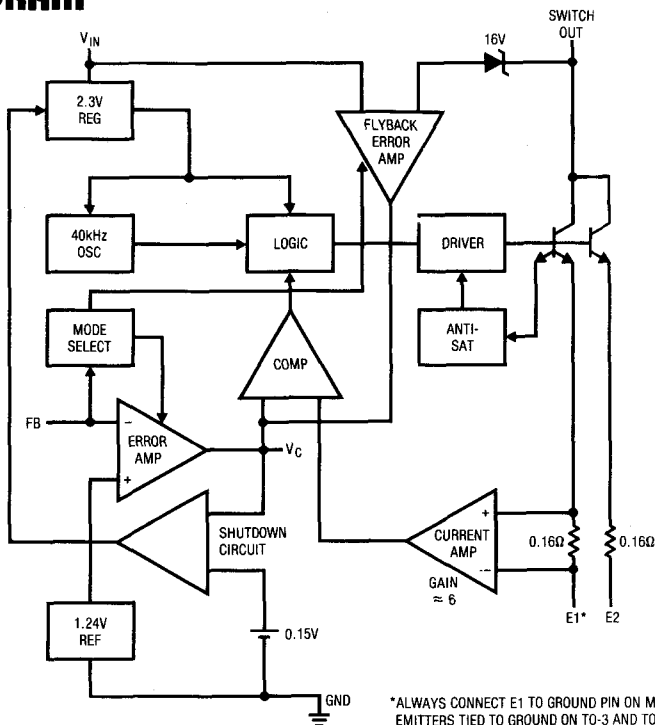
Vc Pin Characteristics



Transconductance of Error Amplifier



BLOCK DIAGRAM



LT1072 OPERATION

The LT1072 is a current mode switcher. This means that switch duty cycle is directly controlled by switch current rather than by output voltage. Referring to the block diagram, the switch is turned "on" at the start of each oscillator cycle. It is turned "off" when switch current reaches a predetermined level. Control of output voltage is obtained by using the output of a voltage sensing error amplifier to set current trip level. This technique has several advantages. First, it has immediate response to input voltage variations, unlike ordinary switchers which have notoriously poor line transient response. Second, it reduces the 90° phase shift at midfrequencies in the energy storage inductor. This greatly simplifies closed loop frequency compensation under widely varying input voltage or output load conditions. Finally, it allows simple pulse-by-pulse current limiting to provide maximum switch protection under output overload or short conditions. A low-dropout internal regulator provides a 2.3V supply for all internal cir-

cuitry on the LT1072. This low-dropout design allows input voltage to vary from 3V to 60V with virtually no change in device performance. A 40kHz oscillator is the basic clock for all internal timing. It turns "on" the output switch via the logic and driver circuitry. Special adaptive antisat circuitry detects onset of saturation in the power switch and adjusts driver current instantaneously to limit switch saturation. This minimizes driver dissipation and provides very rapid turn-off of the switch.

A 1.2V bandgap reference biases the positive input of the error amplifier. The negative input is brought out for output voltage sensing. This feedback pin has a second function; when pulled low with an external resistor, it programs the LT1072 to disconnect the main error amplifier output and connects the output of the flyback amplifier to the comparator input. The LT1072 will then regulate the value of the flyback pulse with respect to the supply voltage. This flyback pulse is

LT1072 OPERATION

directly proportional to output voltage in the traditional transformer coupled flyback topology regulator. By regulating the amplitude of the flyback pulse, the output voltage can be regulated with no direct connection between input and output. The output is fully floating up to the breakdown voltage of the transformer windings. Multiple floating outputs are easily obtained with additional windings. A special delay network inside the LT1072 ignores the leakage inductance spike at the leading edge of the flyback pulse to improve output regulation.

The error signal developed at the comparator input is brought out externally. This pin (V_C) has four different functions. It is used for frequency compensation, current limit adjustment, soft starting, and total regulator shutdown. During normal regulator operation this pin sits at a voltage between 0.9V (low output current) and 2.0V (high output current). The error amplifiers are current output (gm) types, so this voltage can be externally clamped for adjusting current limit. Likewise, a capacitor coupled external clamp will provide soft start. Switch duty cycle goes to zero if the V_C pin is pulled to ground through a diode, placing the LT1072 in an idle mode. Pulling the V_C pin below 0.15V causes total regulator shutdown, with only 50 μ A supply current for shutdown circuitry biasing. See AN-19 for full application details.

Extra Pins on the MiniDIP Package

The miniDIP LT1072 has the emitters of the power transistor brought out separately from the ground pin. This eliminates errors due to ground pin voltage drops and allows the user to reduce switch current limit 2:1 by leaving the second emitter (E2) disconnected. The first emitter (E1) should always be connected to the ground pin. Note that switch "on" resistance doubles when E2 is left open, so efficiency will suffer somewhat when switch currents exceed 100mA. Also, note that chip dissipation will actually *increase* with E2 open during normal load operation, even though dissipation in current limit mode will *decrease*. See "Thermal Considerations."

Thermal Considerations When Using the MiniDIP Package

The low supply current and high switch efficiency of the LT1072 allow it to be used without a heat sink in most applications when the TO-220 or TO-3 package is selected.

These packages are rated at 50°C/W and 35°C/W respectively. The miniDIPs, however, are rated at 100°C/W in ceramic (J) and 130°C/W in plastic (N).

Care should be taken for miniDIP applications to ensure that the worst case input voltage and load current conditions do not cause excessive die temperatures. The following formulas can be used as a rough guide to calculate LT1072 power dissipation. For more details, the reader is referred to Application Note 19 (AN-19), "Efficiency Calculations" section.

Average supply current (including driver current) is:

$$I_{IN} \approx 6\text{mA} + I_{SW}(0.004 + \text{DC}/40)$$

I_{SW} = switch current

DC = switch duty cycle

Switch power dissipation is given by:

$$P_{SW} = (I_{SW})^2 \cdot R_{SW} \cdot \text{DC}$$

R_{SW} = LT1072 switch "on" resistance (1 Ω maximum)

Total power dissipation is the sum of supply current times input voltage plus switch power:

$$P_{TOT} = (I_{IN})(V_{IN}) + P_{SW}$$

In a typical example, using a boost converter to generate +12V@0.12A from a +5V input, duty cycle is approximately 60%, and switch current is about 0.65A, yielding:

$$I_{IN} = 6\text{mA} + 0.65(0.004 + \text{DC}/40) = 18\text{mA}$$

$$P_{SW} = (0.65)^2 \cdot 1\Omega \cdot (0.6) = 0.25\text{W}$$

$$P_{TOT} = (5\text{V})(0.018\text{A}) + 0.25 = 0.34\text{W}$$

Temperature rise in a plastic miniDIP would be 130°C/W times 0.34W, or approximately 44°C. The maximum ambient temperature would be limited to 100°C (commercial temperature limit) minus 44°C, or 56°C.

In most applications, full load current is used to calculate die temperature. However, if overload conditions must also be accounted for, four approaches are possible. First, if loss of regulated output is acceptable under overload conditions, the internal *thermal limit* of the LT1072 will protect the die in most applications by shutting off switch

LT1072 OPERATION

current. *Thermal limit is not a tested parameter*, however, and should be considered only for non-critical applications with temporary overloads. A second approach is to use the larger TO-220 (T) or TO-3 (K) package which, even without a heat sink, may limit die temperatures to safe levels under overload conditions. In critical situations, heat sinking of these packages is required; especially if overload conditions must be tolerated for extended periods of time.

The third approach for lower current applications is to leave the second switch emitter (miniDIP only) open. This increases switch "on" resistance by 2:1, but reduces switch current limit by 2:1 also, resulting in a net 2:1 reduction in I^2R switch dissipation under current limit conditions.

The fourth approach is to clamp the V_C pin to a voltage less than its internal clamp level of 2V. The LT1070 switch current limit is zero at approximately 1V on the V_C pin and 2A at 2V on the V_C pin. Peak switch current can be externally clamped between these two levels with a diode. See AN-19 for details.

LT1072 Synchronizing

The LT1072 can be externally synchronized in the frequency range of 48kHz to 70kHz. This is accomplished as

shown in the accompanying figures. Synchronizing occurs when the V_C pin is pulled to ground with an external transistor. To avoid disturbing the DC characteristics of the internal error amplifier, the width of the synchronizing pulse should be under $1\mu s$. C2 sets the pulse width at $\approx 0.35\mu s$. The effect of a synchronizing pulse on the LT1072 amplifier offset can be calculated from:

$$\Delta V_{OS} = \frac{\left(\frac{KT}{q}\right) (t_s) (f_s) \left(I_C + \frac{V_C}{R_3}\right)}{I_C}$$

$$\frac{KT}{q} = 26mV @ 25^\circ C$$

t_s = pulse width

f_s = pulse frequency

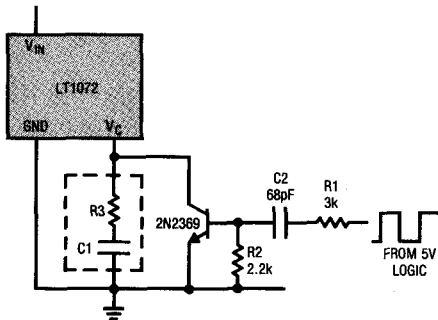
I_C = LT1072 V_C source current ($\approx 200\mu A$)

V_C = LT1072 operating V_C voltage (1V-2V)

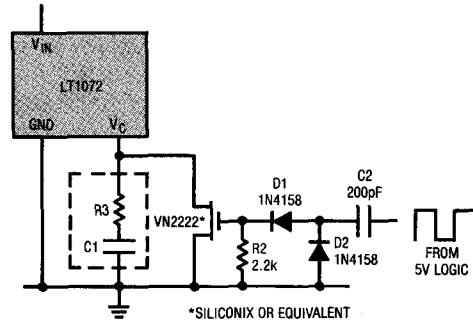
R_3 = resistor used to set mid-frequency "zero" in LT1072 frequency compensation network.

With $t_s = 0.35\mu s$, $f_s = 50kHz$, $V_C = 1.5V$, and $R_3 = 2K\Omega$, offset voltage shift is $\approx 2.2mV$. This is not particularly bothersome, but note that high offsets could result if R_3 were reduced to a much lower value. Also, the synchronizing transistor must sink higher currents with low values of R_3 , so larger drives may have to be used. The transistor must be capable of pulling the V_C pin to within 200mV of ground to ensure synchronizing.

Synchronizing with Bipolar Transistor

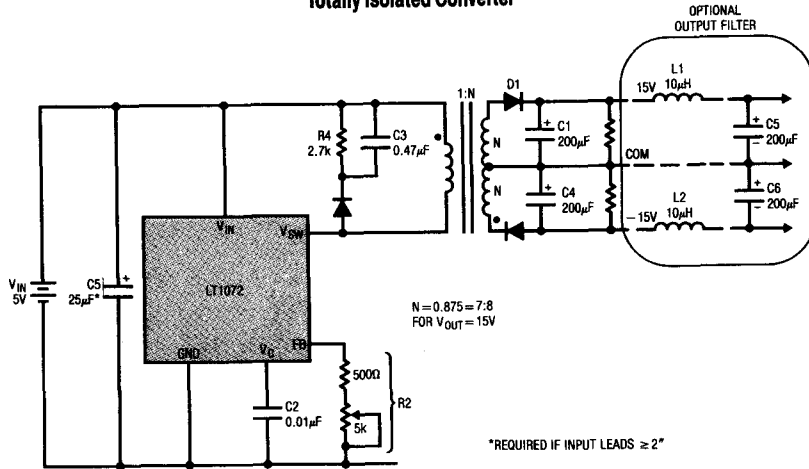


Synchronizing with MOS Transistor

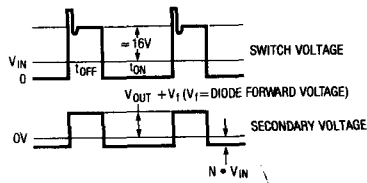


TYPICAL APPLICATIONS

Totally Isolated Converter

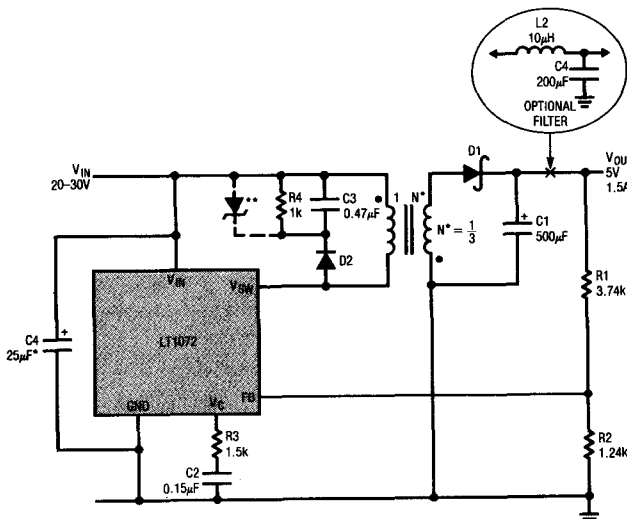


*REQUIRED IF INPUT LEADS $\geq 2^\circ$

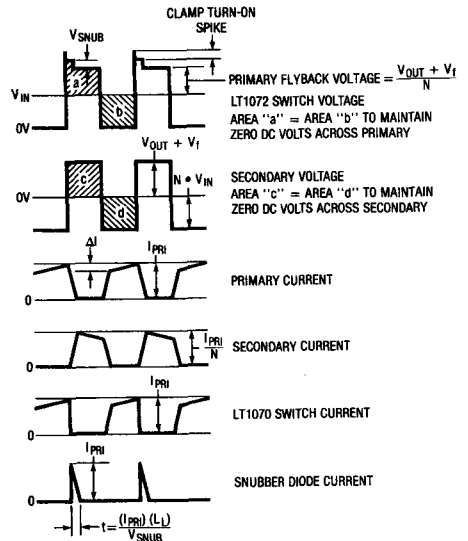


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Flyback Converter

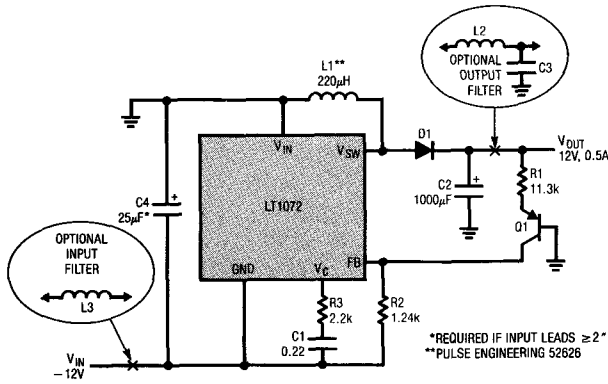


*REQUIRED IF INPUT LEADS $\geq 2^\circ$
 **OPTIONAL TO REPLACE R4 & C3

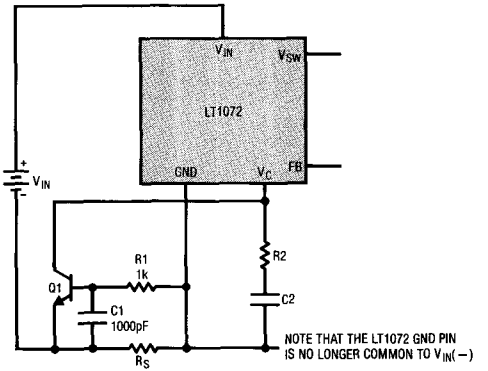


TYPICAL APPLICATIONS

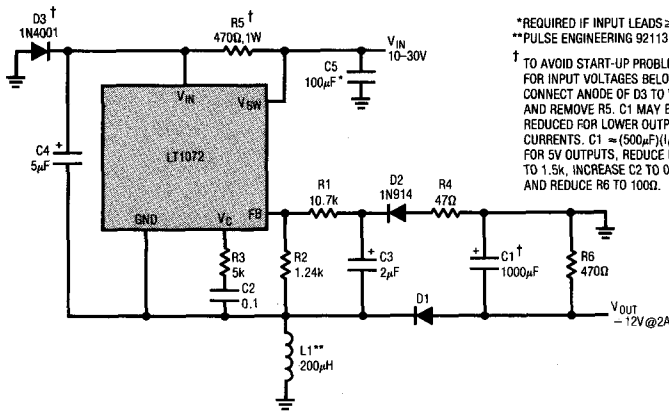
Negative to Positive Buck-Boost Converter



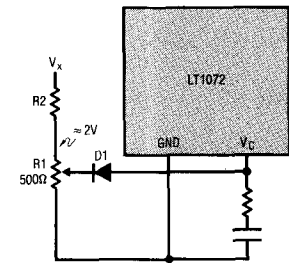
External Current Limit



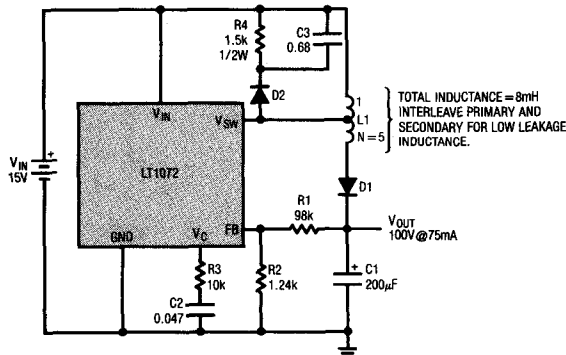
Positive to Negative Buck-Boost Converter



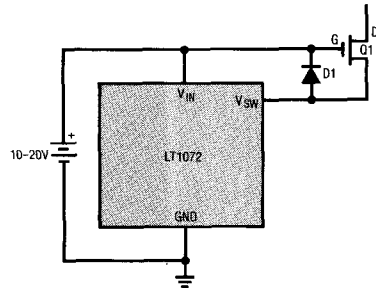
External Current Limit



Voltage Boosted Boost Converter

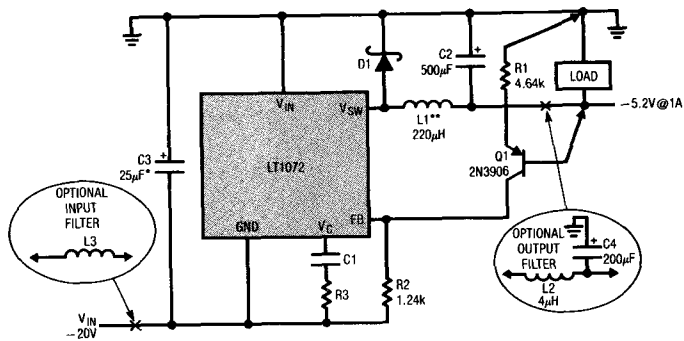


Driving High Voltage FET
 (for Offline Applications, See AN-25)



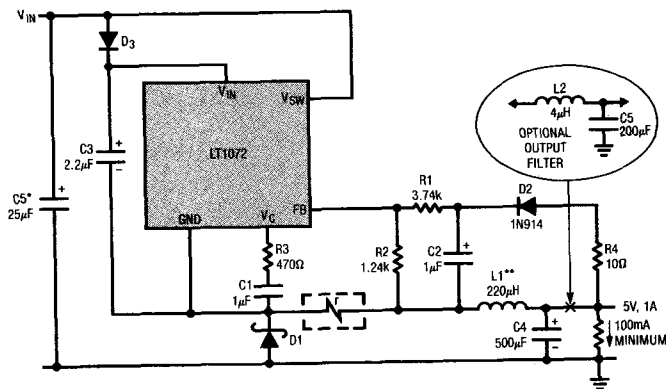
TYPICAL APPLICATIONS

Negative Buck Converter



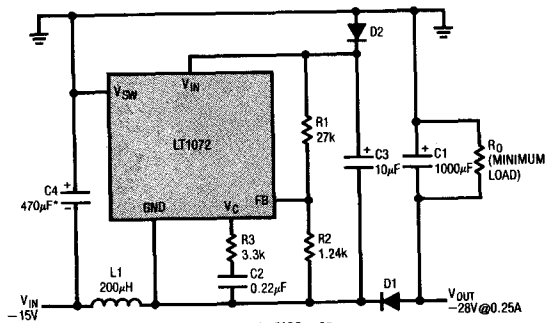
*REQUIRED IF INPUT LEADS $\geq 2^\circ$
 **PULSE ENGINEERING 52626

Positive Buck Converter



*REQUIRED IF INPUT LEADS $\geq 2^\circ$
 **PULSE ENGINEERING 52626

Negative Boost Regulator

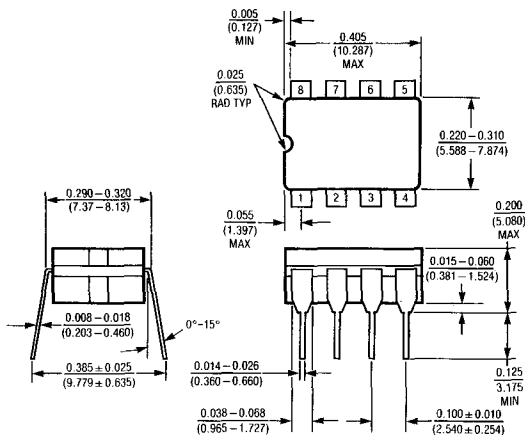


*REQUIRED IF INPUT LEADS $\geq 2^\circ$

5

PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

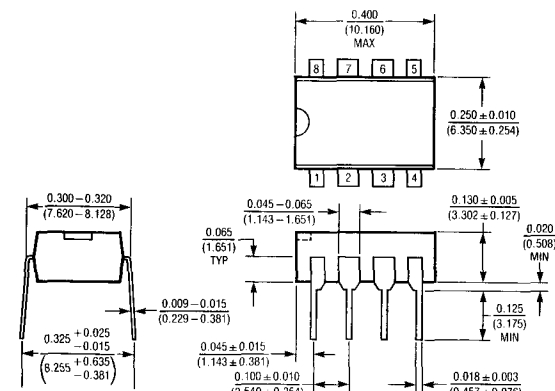
J Package
8 Lead Hermetic DIP



T_{jMAX}	θ_{jA}
150°C	100°C/W

Based on continuous operation.

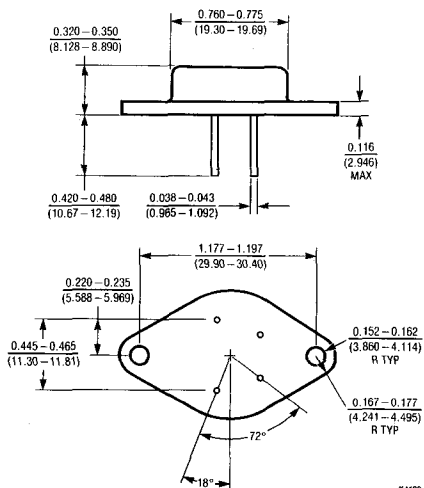
N Package
8 Lead Molded DIP



T_{jMAX}	θ_{jA}
100°C*	130°C/W

Based on continuous operation.
* T_{jMAX} = 125°C for intermittent fault conditions.

TO-3 Type Metal Can (Steel) K Package

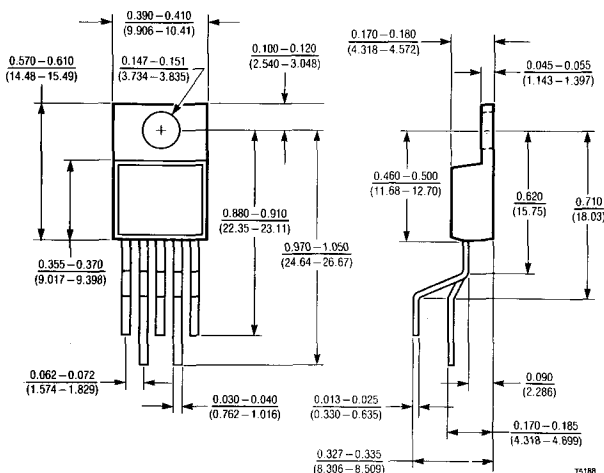


	T_{jMAX}	θ_{jC}	θ_{jA}
LT1072MK, LT1072HVMK	150°C	8°C/W	35°C/W
LT1072CK, LT1072HVCK	100°C*	8°C/W	35°C/W

Based on continuous operation.

* T_{jMAX} = 125°C for intermittent fault conditions.

TO-220 Type Plastic T Package



LT1072CT, LT1072HVCT	T_{jMAX}	θ_{jC}	θ_{jA}
	100°C*	6°C/W	75°C/W

Based on continuous operation.

* T_{jMAX} = 125°C for intermittent fault conditions.

5A and 2.5A High Efficiency 100kHz Switching Regulators

FEATURES

- Wide Input Voltage Range 3V–40V
- Low Quiescent Current—6mA
- Internal 5A Switch (2.5A for LT1171)
- Very Few External Parts Required
- Self-Protected Against Overloads
- Operates in Nearly All Switching Topologies
- Shutdown Mode Draws Only 50 μ A Supply Current
- Flyback-Regulated Mode has Fully Floating Outputs
- Comes in Standard 5-Pin Packages
- Can be Externally Synchronized

APPLICATIONS

- Logic Supply 5V @ 10A
- 5V Logic to \pm 15V Op Amp Supply
- Offline Converter up to 200W
- Battery Upconverter
- Power Inverter (+ to -) or (- to +)
- Fully Floating Multiple Outputs
- For Lower Current Applications see LT1170

USER NOTE:

This data sheet is only intended to provide specifications, graphs, and a general functional description of the LT1170/LT1171. Application circuits are included to show the capability of the LT1170/LT1171. A complete design manual (AN-19) should be obtained to assist in developing new designs. This manual contains a comprehensive discussion of both the LT1170 and the external components used with it, as well as complete formulas for calculating the values of these components. The manual can also be used for the LT1170 and LT1171 by factoring in the higher frequency. A second application note, AN-25, which details off-line applications is available.

DESCRIPTION

The LT1170 and LT1171 are monolithic high power switching regulators. They can be operated in all standard switching configurations including buck, boost, flyback, forward, inverting and "Cuk". A high current, high efficiency switch is included on the die along with all oscillator, control, and protection circuitry. Integration of all functions allows the LT1170/LT1171 to be built in a standard 5-pin TO-3 or TO-220 power package. This makes them extremely easy to use and provides "bust proof" operation similar to that obtained with 3-pin linear regulators.

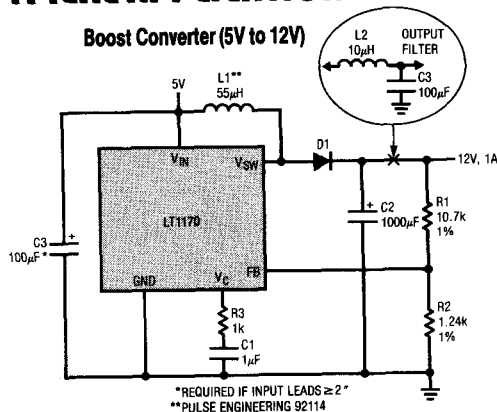
The LT1170/LT1171 operate on supply voltages from 3V to 40V, and draw only 6mA quiescent current. It can deliver load currents up to 100 watts without external power devices. By utilizing current mode switching techniques, it provides excellent transient and DC load and line regulation.

The LT1170/LT1171 has many unique features not found even on the vastly more difficult to use low power control chips presently available. It uses adaptive anti-sat switch drive to allow very wide ranging load currents with no loss in efficiency. An externally activated shutdown mode reduces total supply current to 50 μ A typical for standby operation.

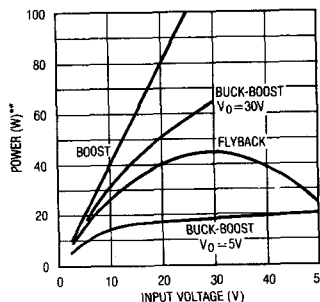
REFER TO TABLE OF CONTENTS FOR REVISED DATA LOCATION

5

TYPICAL APPLICATION



Maximum Output Power*



*ROUGH GUIDE ONLY. BUCK MODE $P_{OUT} = 5A \times V_{OUT}$. SPECIAL TOPOLOGIES DELIVER MORE POWER.
**DIVIDE VERTICAL POWER SCALE BY TWO FOR LT1171

ABSOLUTE MAXIMUM RATINGS

Supply Voltage
 LT1170/71 (See Note 1) 40V
 Switch Output Voltage
 LT1170/71 65V
 Feedback Pin Voltage (Transient, 1ms) ± 15V
 Operating Junction Temperature Range
 LT1170/71M - 55°C to + 150°C
 LT1170/71C (Oper.) 0°C to + 100°C
 LT1170/71C (Sh. Ckt.) 0°C to + 125°C
 Storage Temperature Range - 65°C to + 150°C
 Lead Temperature (Soldering, 10 sec) 300°C

Note 1: Minimum effective switch "on" time for the LT1170/71 (in current limit only) is ≈ 0.6μs. This limits the maximum safe input voltage during an output shorted condition. Buck mode and inverting mode input voltage is limited to:

$$V_{IN} (\text{max, output shorted}) = 15V + \frac{R \cdot I_L + V_f}{t \cdot f}$$

buck and inverting mode

R = Inductor DC Resistance

I_L = 10A for LT1170 and 5A for LT1171

V_f = Output Catch Diode Forward Voltage at I_L

t = 0.6μs, f = 100kHz Switching Frequency

PACKAGE/ORDER INFORMATION

<p>BOTTOM VIEW V_{SW} 1 2 V_C V_{IN} 4 3 FB CASE IS GND K PACKAGE 4-LEAD TO-3 METAL CAN</p>	<p>ORDER PART NUMBER</p> <p>LT1170/LT1171MK LT1170/LT1171CK</p>
	<p>LT1170/LT1171CT</p>
<p>FRONT VIEW 5 V_{IN} 4 V_{SW} 3 GND 2 FB 1 V_C T PACKAGE 5-LEAD TO-220</p>	

Maximum input voltage can be increased by increasing R or V_f.

Transformer designs will tolerate much higher input voltages because leakage inductance limits rate of rise of current in the switch. These designs must be evaluated individually to assure that current limit is well controlled up to maximum input voltage.

Boost mode designs are never protected against output shorts because the external catch diode and inductor connect input to output.

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, V_{IN} = 15V, V_C = 0.5V, V_{FB} = V_{REF}, output pin open.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V _{REF}	Reference Voltage	Measured at Feedback Pin V _C = 0.8V	1.224 1.214	1.244 1.244	1.264 1.274	V
I _B	Feedback Input Current	V _{FB} = V _{REF}		350	750 1100	nA
g _m	Error Amplifier Transconductance	ΔI _C = ± 25μA	3000 2400	4400	6000 7000	μmho
	Error Amplifier Source or Sink Current	V _C = 1.5V	150 120	200	350 400	μA μA
	Error Amplifier Clamp Voltage	Hi Clamp, V _{FB} = 1V Lo Clamp, V _{FB} = 1.5V	1.8 0.25	0.38	2.3 0.52	V V
	Reference Voltage Line Regulation	3V ≤ V _{IN} ≤ V _{MAX} V _C = 0.8V			0.03	%/V
A _v	Error Amplifier Voltage Gain	0.9V ≤ V _C ≤ 1.4V	500	800	2000	V/V
	Minimum Input Voltage			2.6	3.0	V
I _Q	Supply Current	3V ≤ V _{IN} ≤ V _{MAX} , V _C = 0.6V		6	9	mA
	Control Pin Threshold	Duty Cycle = 0	0.8 0.6	0.9	1.08 1.25	V

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, $V_{IN} = 15V$, $V_C = 0.5V$, $V_{FB} = V_{REF}$, output pin open.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	
BV	Output Switch Breakdown Voltage	$3V \leq V_{IN} \leq V_{MAX}$ $I_{SW} = 5mA$	65	90		V	
V_{SAT}	Output Switch (Note 1) "On" Resistance	LT1170		0.15	0.24	Ω	
		LT1171		0.3	0.5	Ω	
	Control Voltage to Switch Current Transconductance	LT1170		8		A/V	
		LT1171		4		A/V	
I_{LIM}	Switch Current Limit (LT1170)	Duty Cycle = 50% $T_J \geq 25^\circ C$	●	5	10	A	
		Duty Cycle = 50% $T_J < 25^\circ C$	●	5	11	A	
		Duty Cycle = 80% (Note 2)	●	4	10	A	
I_{LIM}	Switch Current Limit (LT1171)	Duty Cycle = 50% $T_J \geq 25^\circ C$	●	2.5	5	A	
		Duty Cycle = 50% $T_J < 25^\circ C$	●	2.5	5.5	A	
		Duty Cycle = 80% (Note 2)	●	2	5	A	
$\frac{\Delta I_{IN}}{\Delta I_{SW}}$	Supply Current Increase During Switch On-Time			25	35	mA/A	
f	Switching Frequency		●	88	100	112	kHz
				85		115	kHz
DC (max)	Maximum Switch Duty Cycle			80	90	95	%
					100	250	μA
	Shutdown Mode Supply Current	$3V \leq V_{IN} \leq V_{MAX}$ $V_C = 0.05V$				μA	
	Shutdown Mode Threshold Voltage	$3V \leq V_{IN} \leq V_{MAX}$	●	100	150	250	mV
				50	300	300	mV

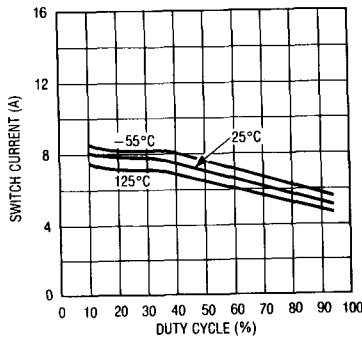
The ● denotes the specifications which apply over the full operating temperature range.
 Note 1: Measured with V_C in hi clamp, $V_{FB} = 0.8V$, $I_{SW} = 4A$ for LT1170 and 2A for LT1171.

Note 2: For duty cycles (DC) between 50% and 80%, minimum guaranteed switch current is given by $I_{LIM} = 3.33(2 - DC)$ for the LT1170 and $I_{LIM} = 1.67(2 - DC)$ for the LT1171.

5

TYPICAL PERFORMANCE CHARACTERISTICS

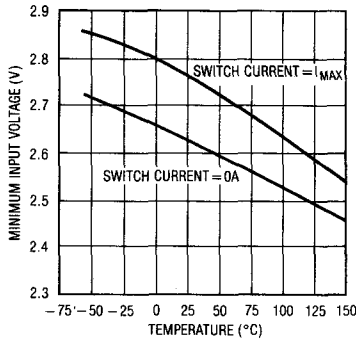
Switch Current Limit vs Duty Cycle*



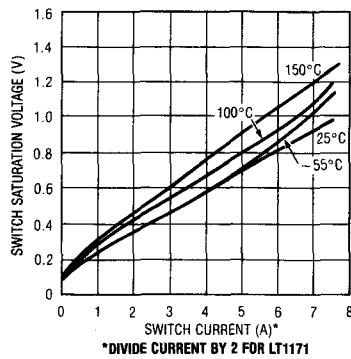
*DIVIDE VERTICAL SCALE BY TWO FOR LT1171

TYPICAL PERFORMANCE CHARACTERISTICS

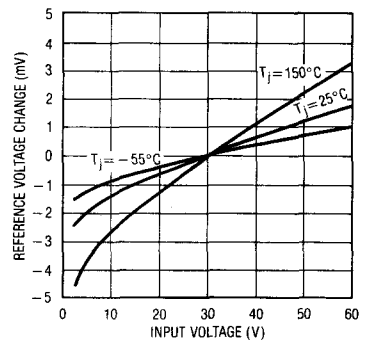
Minimum Input Voltage



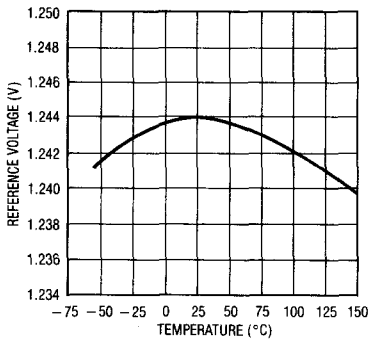
Switch Saturation Voltage



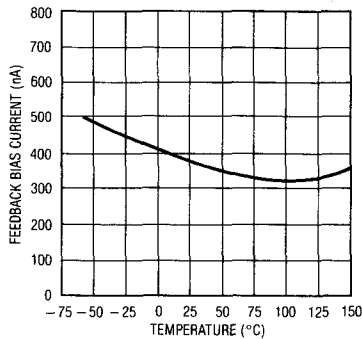
Line Regulation



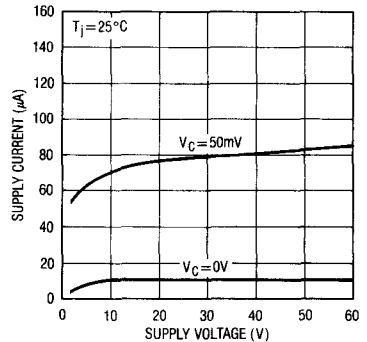
Reference Voltage vs Temperature



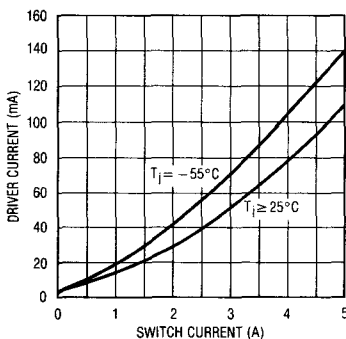
Feedback Bias Current vs Temperature



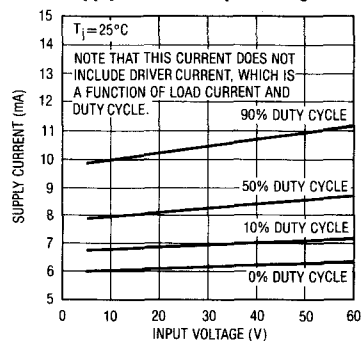
Supply Current vs Supply Voltage (Shutdown Mode)



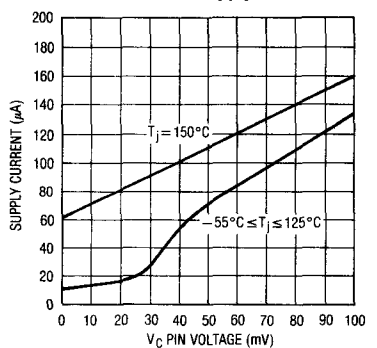
Driver Current* vs Switch Current



Supply Current vs Input Voltage*



Shutdown Mode Supply Current

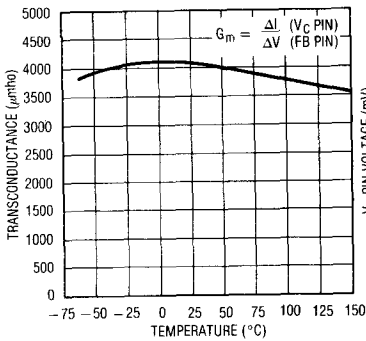


*AVERAGE LT1170 POWER SUPPLY CURRENT IS FOUND BY MULTIPLYING DRIVER CURRENT BY DUTY CYCLE, THEN ADDING QUIESCENT CURRENT.

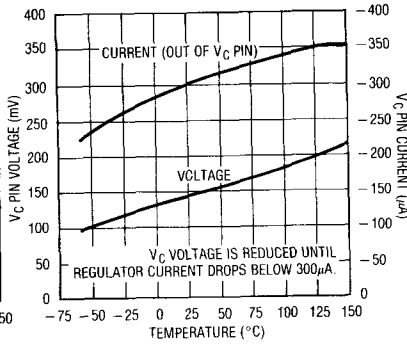
*UNDER VERY LOW OUTPUT CURRENT CONDITIONS, DUTY CYCLE FOR MOST CIRCUITS WILL APPROACH 10% OR LESS.

TYPICAL PERFORMANCE CHARACTERISTICS

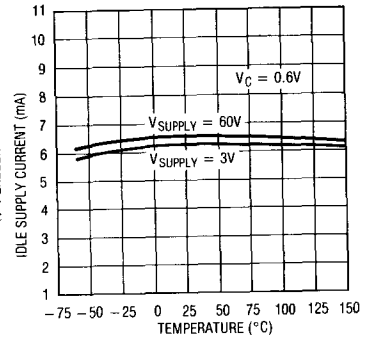
Error Amplifier Transconductance



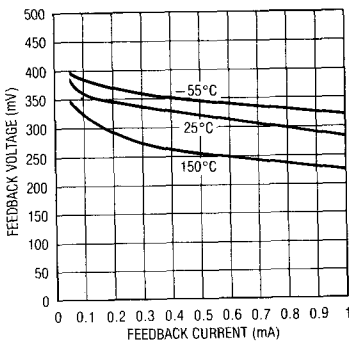
Shutdown Thresholds



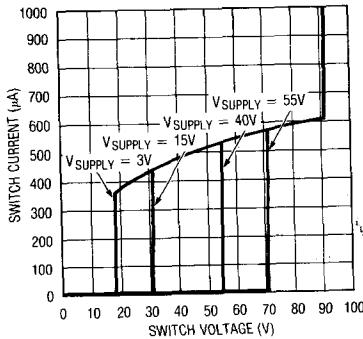
Idle Supply Current vs Temperature



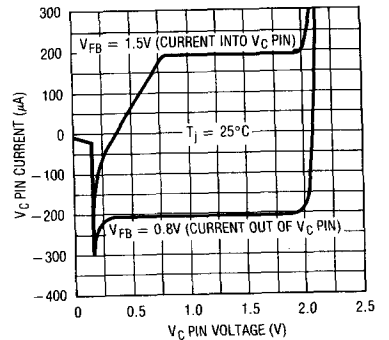
Feedback Pin Clamp Voltage



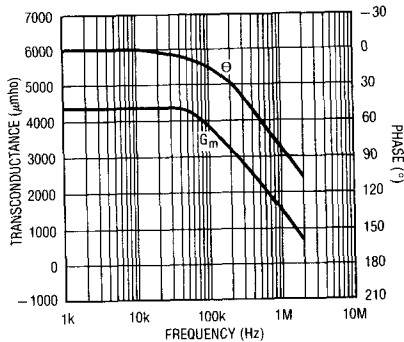
Switch "Off" Characteristics



Vc Pin Characteristics

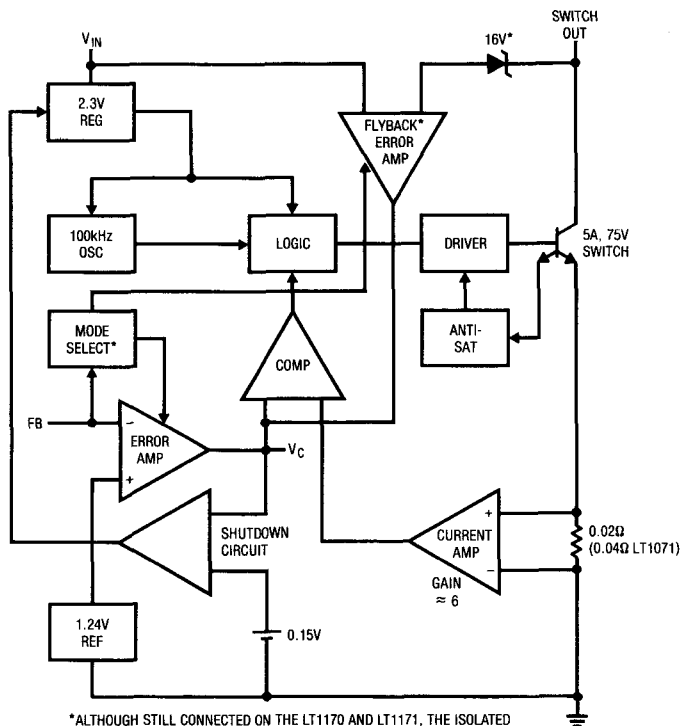


Transconductance of Error Amplifier



5

BLOCK DIAGRAM*



*ALTHOUGH STILL CONNECTED ON THE LT1170 AND LT1171, THE ISOLATED FLYBACK CIRCUITRY IS NOT SPECIFIED FOR 100kHz OPERATION.

LT1170/LT1171 OPERATION

The LT1170/LT1171 is a current mode switcher. This means that switch duty cycle is directly controlled by switch current rather than by output voltage. Referring to the block diagram, the switch is turned "on" at the start of each oscillator cycle. It is turned "off" when switch current reaches a predetermined level. Control of output voltage is obtained by using the output of a voltage sensing error amplifier to set current trip level. This technique has several advantages. First, it has immediate response to input voltage variations, unlike ordinary switchers which have notoriously poor line transient response. Second, it reduces the 90° phase shift at midfrequencies in the energy storage inductor. This greatly simplifies closed loop frequency compensation under widely varying input voltage or output load conditions. Finally, it allows simple pulse-by-pulse current limiting to provide maximum switch protection under output overload or short condi-

tions. A low-dropout internal regulator provides a 2.3V supply for all internal circuitry on the LT1170/LT1171. This low-dropout design allows input voltage to vary from 3V to 60V with virtually no change in device performance. A 100kHz oscillator is the basic clock for all internal timing. It turns "on" the output switch via the logic and driver circuitry. Special adaptive anti-sat circuitry detects onset of saturation in the power switch and adjusts driver current instantaneously to limit switch saturation. This minimizes driver dissipation and provides very rapid turn-off of the switch.

A 1.2V bandgap reference biases the positive input of the error amplifier. The negative input is brought out for output voltage sensing. This feedback pin has a second function; when pulled low with an external resistor, it programs the LT1170/LT1171 to disconnect the main error amplifier output

LT1170/LT1171 OPERATION

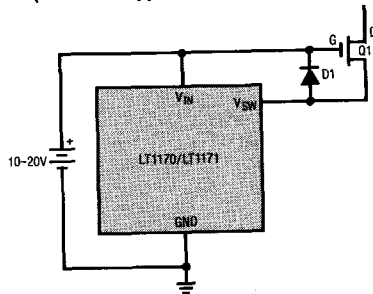
and connects the output of the flyback amplifier to the comparator input. The LT1170/LT1171 will then regulate the value of the flyback pulse with respect to the supply voltage*. This flyback pulse is directly proportional to output voltage in the traditional transformer coupled flyback topology regulator. By regulating the amplitude of the flyback pulse, the output voltage can be regulated with no direct connection between input and output. The output is fully floating up to the breakdown voltage of the transformer windings. Multiple floating outputs are easily obtained with additional windings. A special delay network inside the LT1170/LT1171 ignores the leakage inductance spike at the leading edge of the flyback pulse to improve output regulation.

*See note under block diagram.

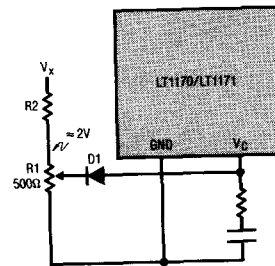
The error signal developed at the comparator input is brought out externally. This pin (V_C) has four different functions. It is used for frequency compensation, current limit adjustment, soft starting, and total regulator shutdown. During normal regulator operation this pin sits at a voltage between 0.9V (low output current) and 2.0V (high output current). The error amplifiers are current output (gm) types, so this voltage can be externally clamped for adjusting current limit. Likewise, a capacitor coupled external clamp will provide soft start. Switch duty cycle goes to zero if the V_C pin is pulled to ground through a diode, placing the LT1170/LT1171 in an idle mode. Pulling the V_C pin below 0.15V causes total regulator shutdown, with only 50 μ A supply current for shutdown circuitry biasing. See AN-19 for full application details.

TYPICAL APPLICATIONS (Note that maximum output currents are divided by 2 for LT1171.)

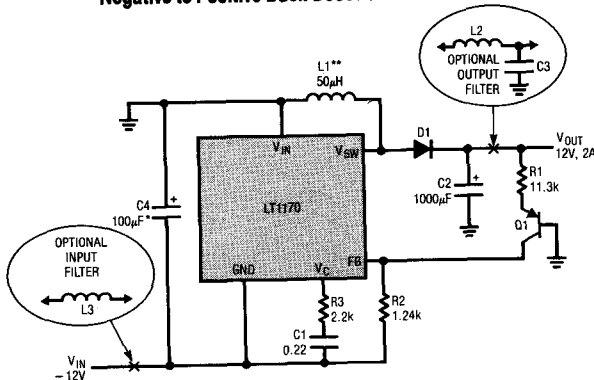
Driving High Voltage FET
(for Offline Applications, See AN-25)



External Current Limit

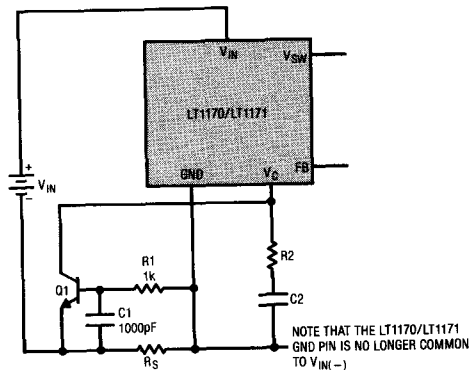


Negative to Positive Buck-Boost Converter



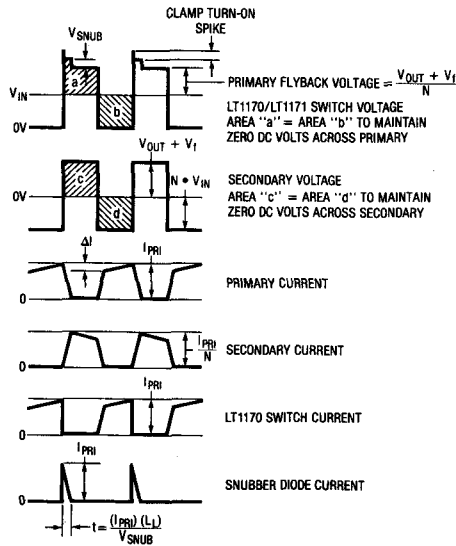
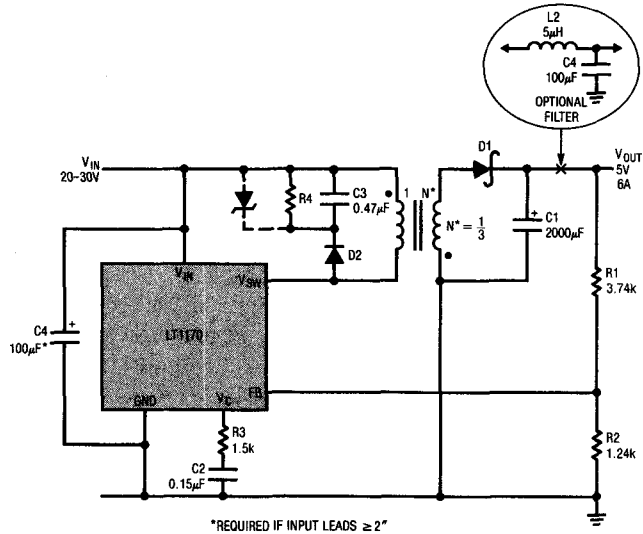
*REQUIRED IF INPUT LEADS $\geq 2^\circ$
**PULSE ENGINEERING 92114

External Current Limit



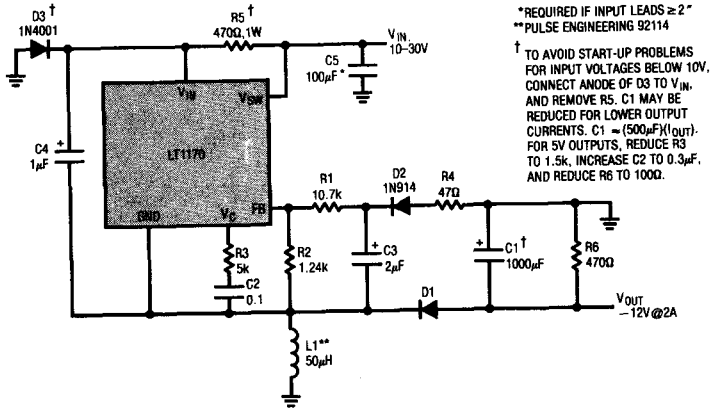
TYPICAL APPLICATIONS

Flyback Converter

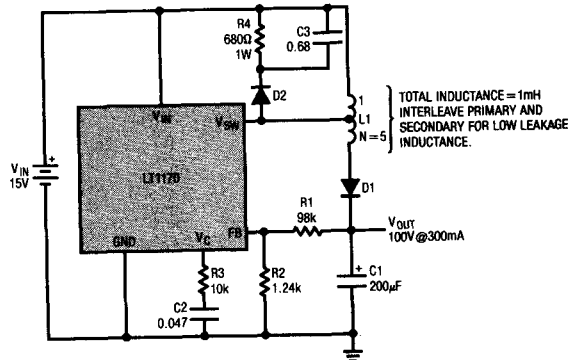


TYPICAL APPLICATIONS

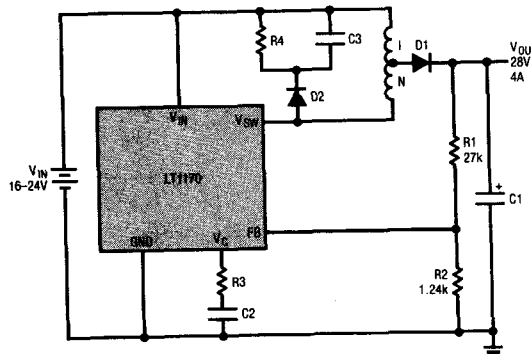
Positive to Negative Buck-Boost Converter



Voltage Boosted Boost Converter

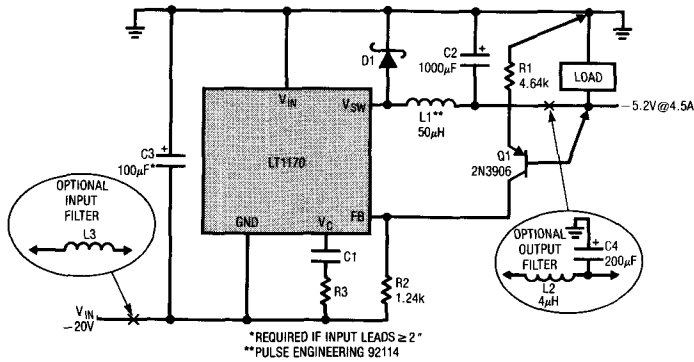


Current Boosted Boost Converter

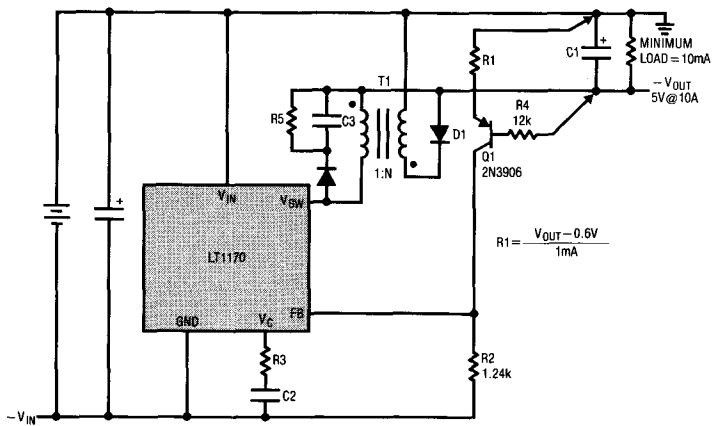


TYPICAL APPLICATIONS

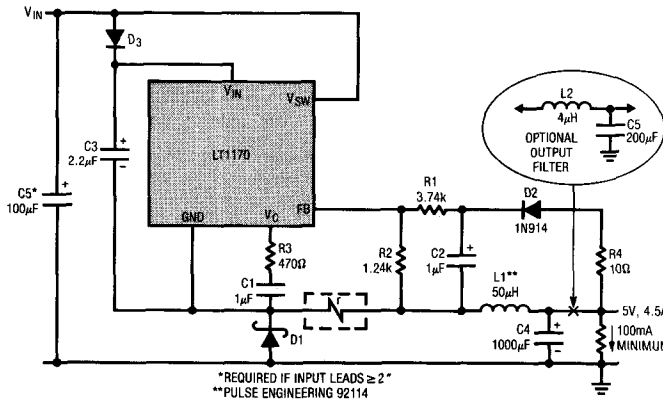
Negative Buck Converter



Negative Current Boosted Buck Converter

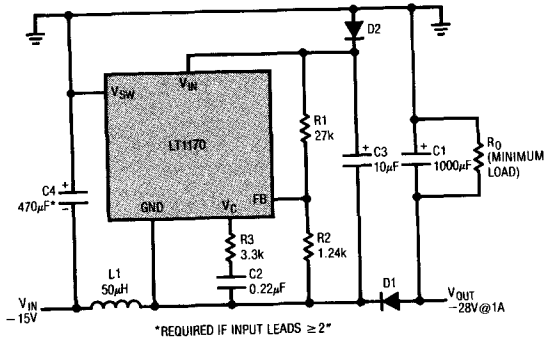


Positive Buck Converter

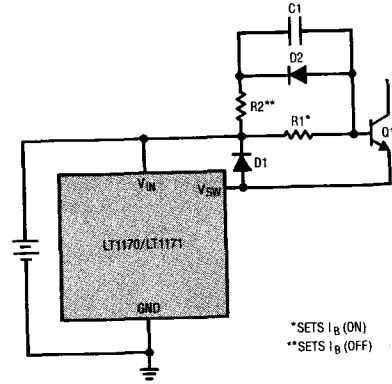


TYPICAL APPLICATIONS

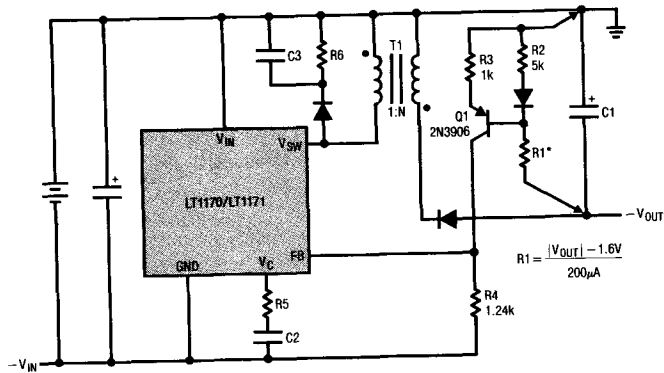
Negative Boost Regulator



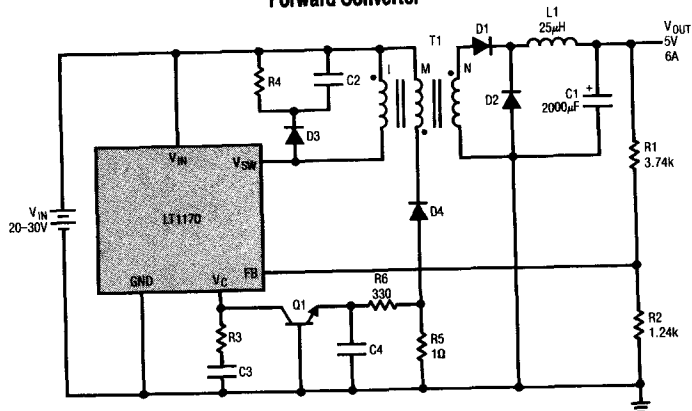
Driving High Voltage NPN



Negative Input-Negative Output Flyback Converter



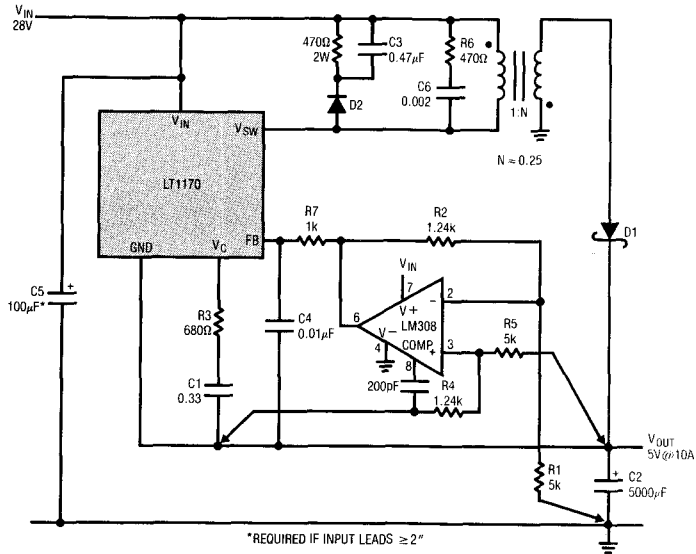
Forward Converter



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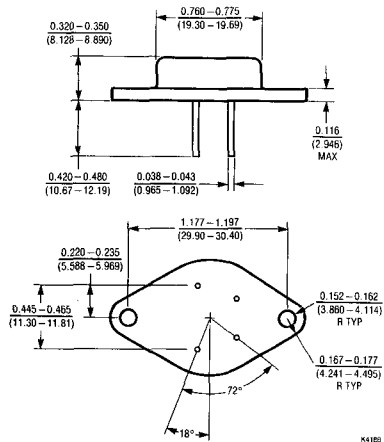
TYPICAL APPLICATIONS

Positive Current Boosted Buck Converter

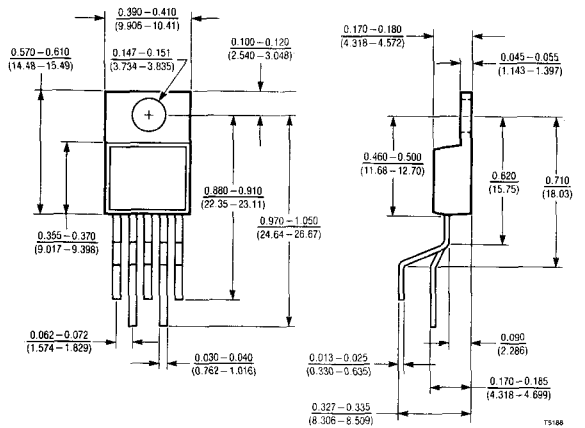


PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

TO-3 Type Metal Can (Steel) K Package



TO-220 Type Plastic T Package



	T _{JMAX}	θ _{JC}	θ _{JA}
LT1170MK	150°C	2°C/W	35°C/W
LT1170CK	100°C	2°C/W	35°C/W
LT1171MK	150°C	4°C/W	35°C/W
LT1171CK	100°C	4°C/W	35°C/W

	T _{JMAX}	θ _{JC}	θ _{JA}
LT1170CT	100°C	2°C/W	75°C/W
LT1171CT	100°C	4°C/W	75°C/W

1.25A High Efficiency 100kHz Switching Regulator

FEATURES

- Available in MiniDIP, TO-220, and TO-3 Packages
- Wide Input Voltage Range 3V–60V
- Low Quiescent Current—6mA
- Internal 1.25A Switch
- Very Few External Parts Required
- Self-Protected Against Overloads
- Operates in Nearly All Switching Topologies
- Shutdown Mode Draws Only 50 μ A Supply Current
- Comes in Standard 5-Pin Packages
- Can be Externally Synchronized

APPLICATIONS

- Logic Supply 5V @ 2.5A
- 5V Logic to \pm 15V Op Amp Supply
- Offline Converter up to 50W
- Battery Upconverter
- Power Inverter (+ to -) or (- to +)
- Fully Floating Multiple Outputs
- Driver for High Current Supplies

USER NOTE:

This data sheet is only intended to provide specifications, graphs, and a general functional description of the LT1172. Application circuits are included to show the capability of the LT1172. A complete design manual (AN-19) should be obtained to assist in developing new designs. This manual contains a comprehensive discussion of both the LT1070 and the external components used with it, as well as complete formulas for calculating the values of these components. The manual can also be used for the LT1172 by factoring in the lower switch current rating, and higher frequency.

DESCRIPTION

The LT1172 is a monolithic high power switching regulator. It can be operated in all standard switching configurations including buck, boost, flyback, forward, inverting and "Cuk". A high current, high efficiency switch is included on the die along with all oscillator, control, and protection circuitry. Integration of all functions allows the LT1172 to be built in a standard 5-pin TO-3 or TO-220 power package as well as the 8-pin miniDIP. This makes it extremely easy to use and provides "bust proof" operation similar to that obtained with 3-pin linear regulators.

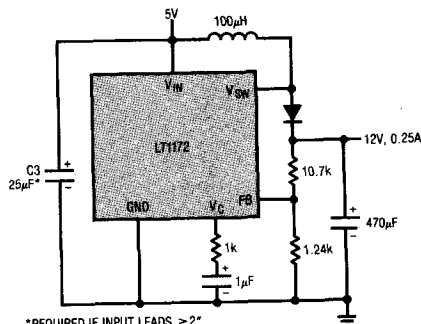
The LT1172 operates with supply voltages from 3V to 60V, and draws only 6mA quiescent current. It can deliver load power up to 20 watts with no external power devices. By utilizing current-mode switching techniques, it provides excellent AC and DC load and line regulation.

The LT1172 has many unique features not found even on the vastly more difficult to use low power control chips presently available. It uses adaptive anti-sat switch drive to allow very wide ranging load currents with no loss in efficiency. An externally activated shutdown mode reduces total supply current to 50 μ A typical for standby operation.

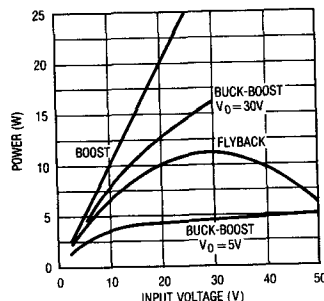
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TYPICAL APPLICATION

Boost Converter (5V to 12V)



Maximum Output Power*



*ROUGH GUIDE ONLY. BUCK MODE $P_{OUT} = 1A \times V_{OUT}$.
 MINIDIP OUTPUT POWER MAY BE LIMITED BY PACKAGE TEMPERATURE RISE AT HIGH INPUT VOLTAGES OR HIGH DUTY CYCLES.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	
LT1172HV (See Note 1)	60V
LT1172 (See Note 1)	40V
Switch Output Voltage	
LT1172HV	75V
LT1172	65V
Feedback Pin Voltage (Transient, 1ms)	± 15V
Operating Junction Temperature Range	
LT1172HVM, LT1172M	-55°C to +150°C
LT1172HVC, LT1172C (Oper.)	0°C to +100°C
LT1172HVC, LT1172C (Sh. Ckt.)	0°C to +125°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 10sec)	300°C

Note 1: Minimum switch "on" time for the LT1172 in current limit is ≈ 0.6μsec. This limits the maximum input voltage during short circuit conditions, in the buck and inverting modes only, to ≈ 25V. Normal (unshorted) conditions are not affected. If the LT1172 is being operated in the buck or inverting mode at high input voltages and short circuit conditions are expected, a resistor must be placed in series with the inductor, as follows:

The value of the resistor is given by:

$$R = \frac{(t) (f) (V_{IN}) - V_f}{I_{(LIMIT)}} - R_L$$

PACKAGE/ORDER INFORMATION

<p>BOTTOM VIEW K PACKAGE 4 LEAD TO-3 METAL CAN</p>	ORDER PART NUMBER
	LT1172HVMK LT1172MK LT1172HVCK LT1172CK
<p>FRONT VIEW T PACKAGE 5 LEAD TO-220</p>	LT1172HVCT LT1172CT
	LT1172MJ8 LT1172CJ8 LT1172CN8
<p>TOP VIEW J PACKAGE 8 LEAD CERAMIC DIP N PACKAGE 8 LEAD PLASTIC DIP</p>	

t = Minimum "on" time of LT1172 in current limit, ≈ 0.6μs

f = Operating frequency (100kHz)

V_f = Forward voltage of external catch diode at I_(LIMIT)

I_(LIMIT) = Current limit of LT1172 (2A)

R_L = Internal series resistance of inductor

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, V_{IN} = 15V, V_C = 0.5V, V_{FB} = V_{REF}, output pin open.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V _{REF}	Reference Voltage	Measured at Feedback Pin V _C = 0.8V	1.224	1.244	1.264	V
I _B	Feedback Input Current	V _{FB} = V _{REF}	●	350	750	nA
g _m	Error Amplifier Transconductance	ΔI _C = ± 25μA	●	3000	4400	μmho
	Error Amplifier Source or Sink Current	V _C = 1.5V	●	150	200	350 μA
	Error Amplifier Clamp Voltage	Hi Clamp, V _{FB} = 1V Lo Clamp, V _{FB} = 1.5V	1.8	0.25	2.3	V
	Reference Voltage Line Regulation	3V ≤ V _{IN} ≤ V _{MAX} V _C = 0.8V	●		0.03	%/V
A _v	Error Amplifier Voltage Gain	0.9V ≤ V _C ≤ 1.4V	500	800	2000	V/V
	Minimum Input Voltage	●		2.6	3.0	V
I _Q	Supply Current	3V ≤ V _{IN} ≤ V _{MAX} , V _C = 0.6V		6	9	mA
	Control Pin Threshold	Duty Cycle = 0	●	0.8	0.9	1.08 V
			0.6		1.25	

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, $V_{IN} = 15V$, $V_C = 0.5V$, $V_{FB} = V_{REF}$, output pin open.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
BV	Output Switch Breakdown Voltage	$3V \leq V_{IN} \leq V_{MAX}$ $I_{SW} = 5mA$	●	65	90		V
			●	75	90		V
V_{SAT}	Output Switch (Note 1) "On" Resistance		●		0.6	1	Ω
	Control Voltage to Switch Current Transconductance				2		A/V
I_{LIM}	Switch Current Limit	Duty Cycle = 50% Duty Cycle = 50% Duty Cycle = 80% (Note 2)	●	1.25		3	A
			●	1.25		3.5	A
			●	1		2.5	A
$\frac{\Delta I_{IN}}{\Delta I_{SW}}$	Supply Current Increase During Switch On-Time			25	35		mA/A
f	Switching Frequency		●	88	100	112	kHz
				85		115	kHz
DC (max)	Maximum Switch Duty Cycle			80	90	95	%
	Shutdown Mode Supply Current	$3V \leq V_{IN} \leq V_{MAX}$ $V_C = 0.05V$			100	250	μA
	Shutdown Mode Threshold Voltage	$3V \leq V_{IN} \leq V_{MAX}$	●	100	150	250	mV
				50		300	mV

The ● denotes the specifications which apply over the full operating temperature range.

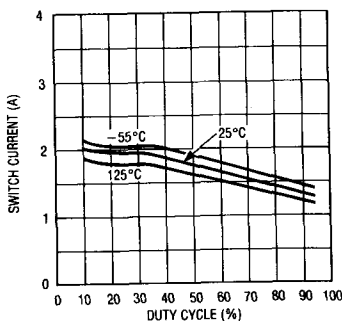
Note 1: Measured with V_C in hi clamp, $V_{FB} = 0.8V$.

Note 2: For duty cycles (DC) between 50% and 80%, minimum guaranteed switch current is given by $I_{LIM} = 0.833(2 - DC)$.

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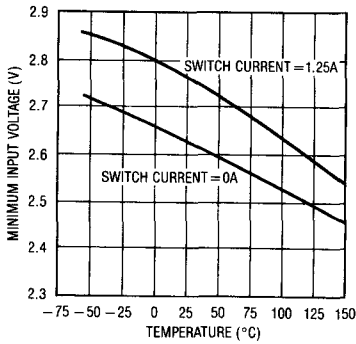
TYPICAL PERFORMANCE CHARACTERISTICS

Switch Current Limit vs Duty Cycle

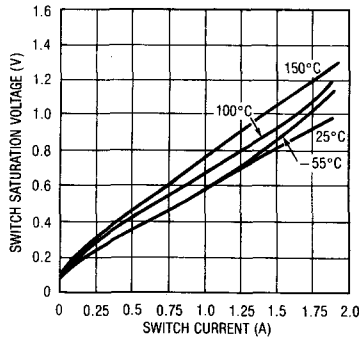


TYPICAL PERFORMANCE CHARACTERISTICS

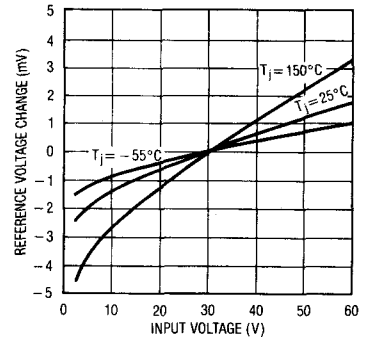
Minimum Input Voltage



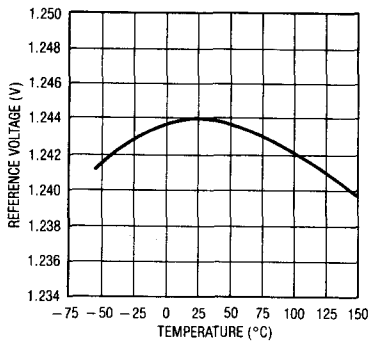
Switch Saturation Voltage



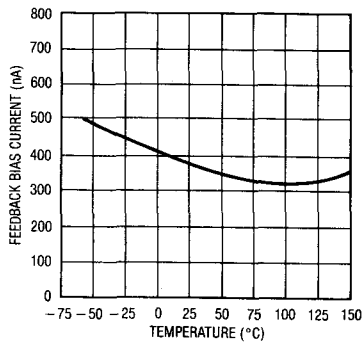
Line Regulation



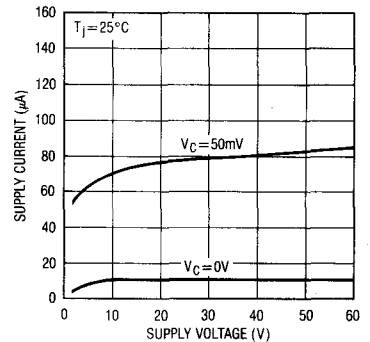
Reference Voltage vs Temperature



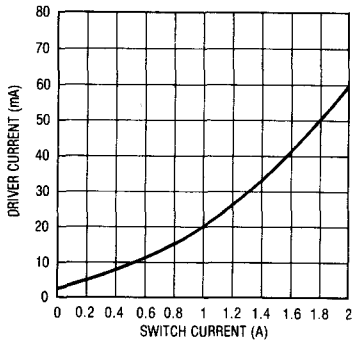
Feedback Bias Current vs Temperature



Supply Current vs Supply Voltage (Shutdown Mode)

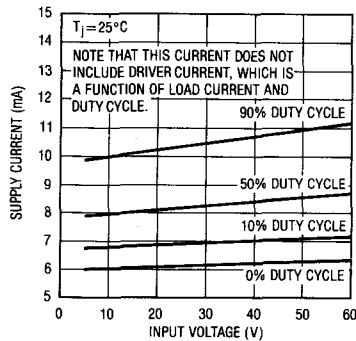


Driver Current* vs Switch Current



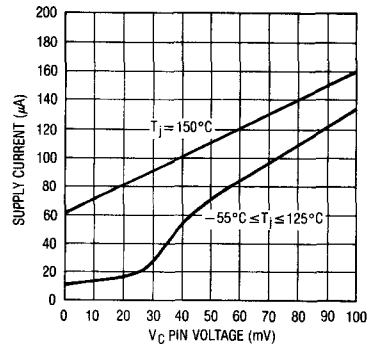
*AVERAGE LT1172 POWER SUPPLY CURRENT IS FOUND BY MULTIPLYING DRIVER CURRENT BY DUTY CYCLE, THEN ADDING QUIESCENT CURRENT.

Supply Current vs Input Voltage*



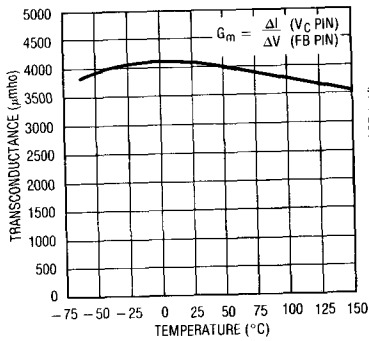
*UNDER VERY LOW OUTPUT CURRENT CONDITIONS, DUTY CYCLE FOR MOST CIRCUITS WILL APPROACH 10% OR LESS.

Shutdown Mode Supply Current

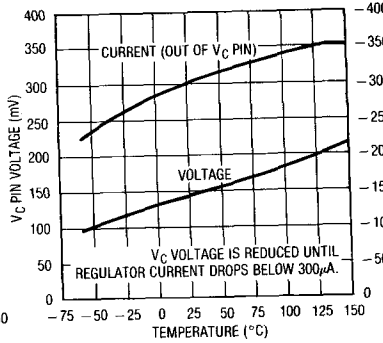


TYPICAL PERFORMANCE CHARACTERISTICS

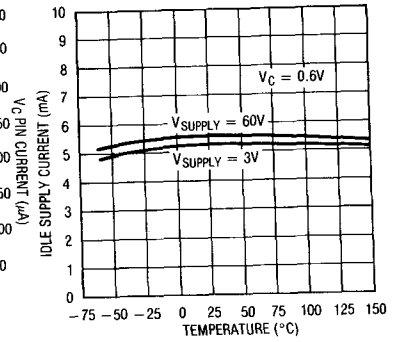
Error Amplifier Transconductance



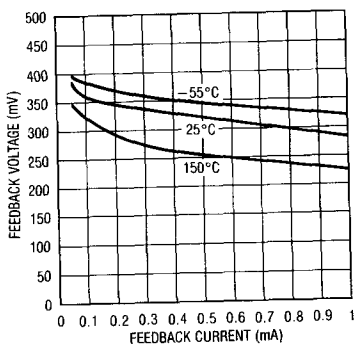
Shutdown Thresholds



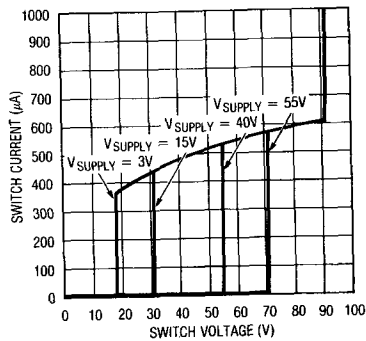
Idle Supply Current vs Temperature



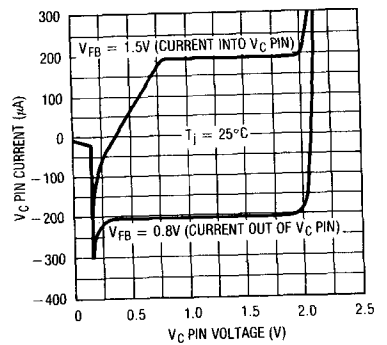
Feedback Pin Clamp Voltage



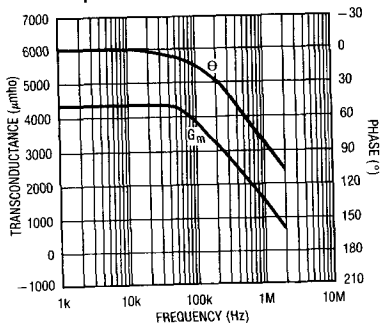
Switch "Off" Characteristics



Vc Pin Characteristics

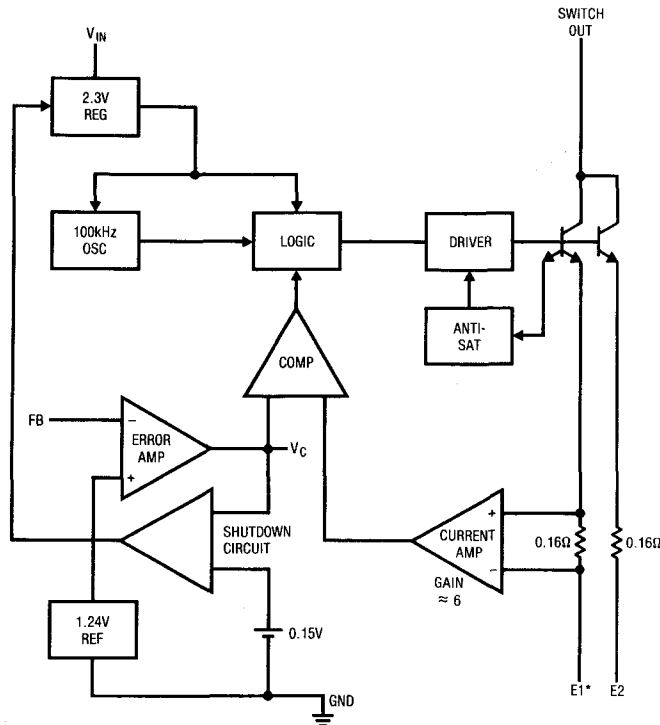


Transconductance of Error Amplifier



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BLOCK DIAGRAM



*ALWAYS CONNECT E1 TO GROUND PIN ON MINIDIP PACKAGE.
E1 AND E2 INTERNALLY TIED TO GROUND ON TO-3 AND TO-220 PACKAGES.

LT1172 OPERATION

The LT1172 is a current mode switcher. This means that switch duty cycle is directly controlled by switch current rather than by output voltage. Referring to the block diagram, the switch is turned "on" at the start of each oscillator cycle. It is turned "off" when switch current reaches a predetermined level. Control of output voltage is obtained by using the output of a voltage sensing error amplifier to set current trip level. This technique has several advantages. First, it has immediate response to input voltage variations, unlike ordinary switchers which have notoriously poor line transient response. Second, it reduces the 90° phase shift at midfrequencies in the energy storage inductor. This greatly simplifies closed loop frequency compensation under widely varying input voltage or output

load conditions. Finally, it allows simple pulse-by-pulse current limiting to provide maximum switch protection under overload or short conditions. A low-dropout internal regulator provides a 2.3V supply for all internal circuitry on the LT1172. This low-dropout design allows input voltage to vary from 3V to 60V with virtually no change in device performance. A 100kHz oscillator is the basic clock for all internal timing. It turns "on" the output switch via the logic and driver circuitry. Special adaptive antisat circuitry detects onset of saturation in the power switch and adjusts driver current instantaneously to limit switch saturation. This minimizes driver dissipation and provides very rapid turn-off of the switch.

LT1172 OPERATION

A 1.2V bandgap reference biases the positive input of the error amplifier. The negative input is brought out for output voltage sensing.

The error signal developed at the comparator input is brought out externally. This pin (V_C) has four different functions. It is used for frequency compensation, current limit adjustment, soft starting, and total regulator shutdown. During normal regulator operation this pin sits at a voltage between 0.9V (low output current) and 2.0V (high output current). The error amplifiers are current output (gm) types, so this voltage can be externally clamped for adjusting current limit. Likewise, a capacitor coupled external clamp will provide soft start. Switch duty cycle goes to zero if the V_C pin is pulled to ground through a diode, placing the LT1172 in an idle mode. Pulling the V_C pin below 0.15V causes total regulator shutdown, with only 50 μ A supply current for shutdown circuitry biasing. See AN-19 for full application details.

Extra Pins on the MiniDIP Package

The miniDIP LT1172 has the emitters of the power transistor brought out separately from the ground pin. This eliminates errors due to ground pin voltage drops and allows the user to reduce switch current limit 2:1 by leaving the second emitter (E2) disconnected. The first emitter (E1) should always be connected to the ground pin. Note that switch "on" resistance doubles when E2 is left open, so efficiency will suffer somewhat when switch currents exceed 100mA. Also, note that chip dissipation will actually *increase* with E2 open during normal load operation, even though dissipation in current limit mode will *decrease*. See "Thermal Considerations."

Thermal Considerations When Using the MiniDIP Package

The low supply current and high switch efficiency of the LT1172 allow it to be used without a heat sink in most applications when the TO-220 or TO-3 package is selected. These packages are rated at 50°C/W and 35°C/W respectively. The miniDIPs, however, are rated at 100°C/W in ceramic (J) and 130°C/W in plastic (N).

Care should be taken for miniDIP applications to ensure that the worst case input voltage and load current conditions do not cause excessive die temperatures. The following formulas can be used as a rough guide to calculate LT1172 power dissipation. For more details, the reader is referred to Application Note 19 (AN-19), "Efficiency Calculations" section.

Average supply current (including driver current) is:

$$I_{IN} \approx 6\text{mA} + I_{SW}(0.004 + \text{DC}/40)$$

I_{SW} = switch current
DC = switch duty cycle

Switch power dissipation is given by:

$$P_{SW} = (I_{SW})^2 \cdot R_{SW} \cdot \text{DC}$$

R_{SW} = LT1172 switch "on" resistance (1 Ω maximum)

Total power dissipation is the sum of supply current times input voltage plus switch power:

$$P_{TOT} = (I_{IN})(V_{IN}) + P_{SW}$$

In a typical example, using a boost convertor to generate +12V@0.12A from a +5V input, duty cycle is approximately 60%, and switch current is about 0.65A, yielding:

$$I_{IN} = 6\text{mA} + 0.65(0.004 + \text{DC}/40) = 18\text{mA}$$

$$P_{SW} = (0.65)^2 \cdot 1\Omega \cdot (0.6) = 0.25\text{W}$$

$$P_{TOT} = (5\text{V})(0.018\text{A}) + 0.25 = 0.34\text{W}$$

Temperature rise in a plastic miniDIP would be 130°C/W times 0.34W, or approximately 44°C. The maximum ambient temperature would be limited to 100°C (commercial temperature limit) minus 44°C, or 56°C.

In most applications, full load current is used to calculate die temperature. However, if overload conditions must also be accounted for, four approaches are possible. First, if loss of regulated output is acceptable under overload conditions, the internal *thermal limit* of the LT1172 will protect the die in most applications by shutting off switch current. *Thermal limit is not a tested parameter*, however,

LT1172 OPERATION

and should be considered only for non-critical applications with temporary overloads. A second approach is to use the larger TO-220 (T) or TO-3 (K) package which, even without a heat sink, may limit die temperatures to safe levels under overload conditions. In critical situations, heat sinking of these packages is required; especially if overload conditions must be tolerated for extended periods of time.

The third approach for lower current applications is to leave the second switch emitter (miniDIP only) open. This increases switch "on" resistance by 2:1, but reduces switch current limit by 2:1 also, resulting in a net 2:1 reduction in I^2R switch dissipation under current limit conditions.

The fourth approach is to clamp the V_C pin to a voltage less than its internal clamp level of 2V. The LT1172 switch current limit is zero at approximately 1V on the V_C pin and 2A at 2V on the V_C pin. Peak switch current can be externally clamped between these two levels with a diode. See AN-19 for details.

LT1172 Synchronizing

The LT1172 can be externally synchronized in the frequency range of 120kHz to 160kHz. This is accomplished as shown in the accompanying figures. Synchronizing occurs when the V_C pin is pulled to ground with an

external transistor. To avoid disturbing the DC characteristics of the internal error amplifier, the width of the synchronizing pulse should be under $0.3\mu s$. C_2 sets the pulse width at $\approx 0.2\mu s$. The effect of a synchronizing pulse on the LT1172 amplifier offset can be calculated from:

$$\Delta V_{OS} = \frac{\left(\frac{KT}{q}\right) (t_s) (f_s) \left(I_C + \frac{V_C}{R_3}\right)}{I_C}$$

$$\frac{KT}{q} = 26mV @ 25^\circ C$$

t_s = pulse width

f_s = pulse frequency

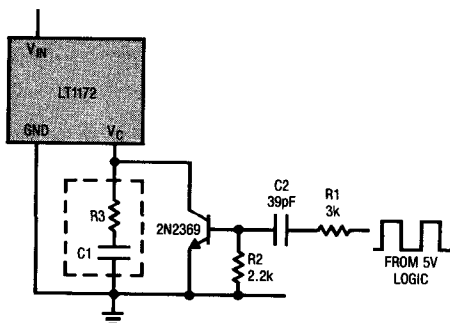
I_C = LT1172 V_C source current ($\approx 200\mu A$)

V_C = LT1172 operating V_C voltage (1V-2V)

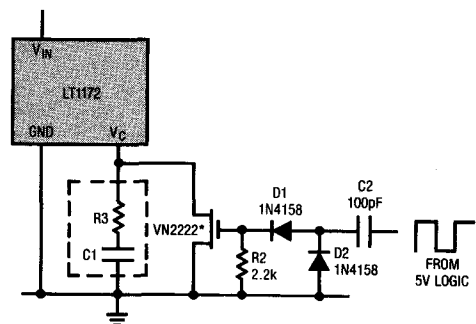
R_3 = resistor used to set mid-frequency "zero" in LT1172 frequency compensation network.

With $t_s = 0.2\mu s$, $f_s = 150kHz$, $V_C = 1.5V$, and $R_3 = 2K\Omega$, offset voltage shift is $\approx 3.8mV$. This is not particularly bothersome, but note that high offsets could result if R_3 were reduced to a much lower value. Also, the synchronizing transistor must sink higher currents with low values of R_3 , so larger drives may have to be used. The transistor must be capable of pulling the V_C pin to within 200mV of ground to ensure synchronizing.

Synchronizing with Bipolar Transistor



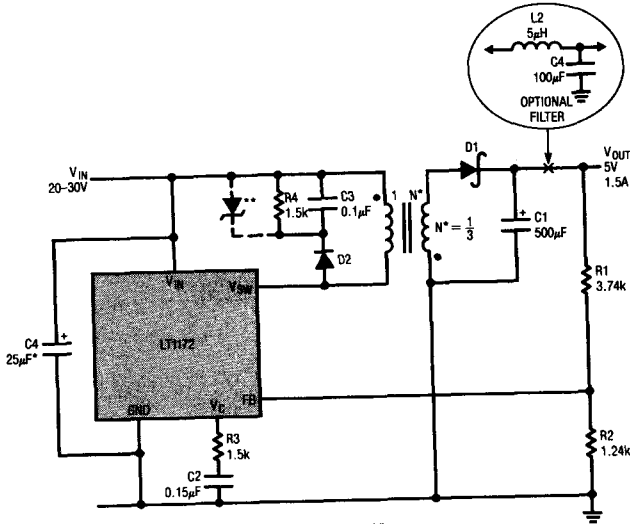
Synchronizing with MOS Transistor



*SILICONIX OR EQUIVALENT

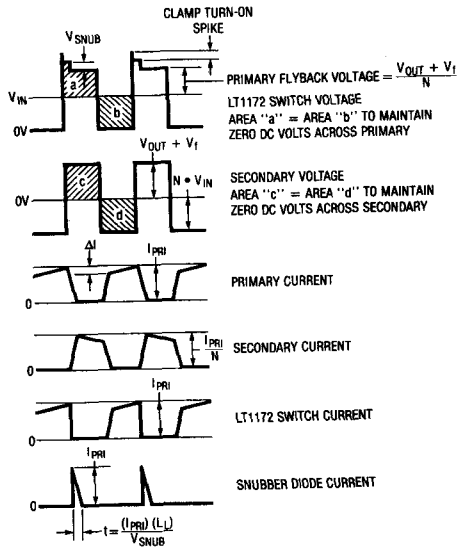
TYPICAL APPLICATIONS

Flyback Converter



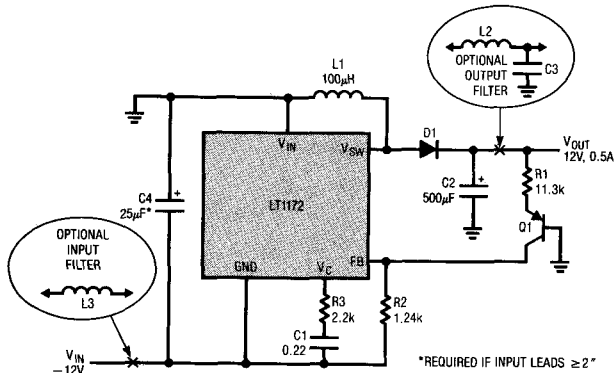
*REQUIRED IF INPUT LEADS $\geq 2"$
 **OPTIONAL TO REPLACE R4 & C3

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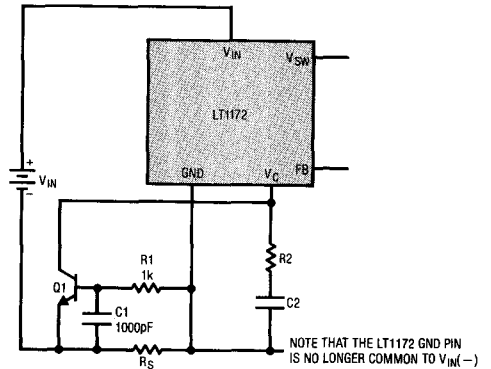


TYPICAL APPLICATIONS

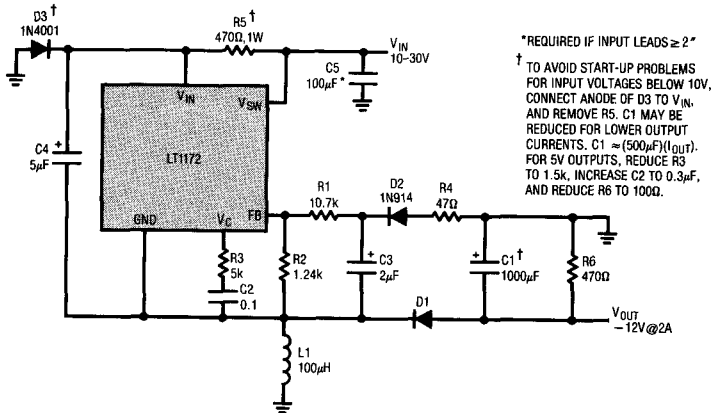
Negative to Positive Buck-Boost Converter



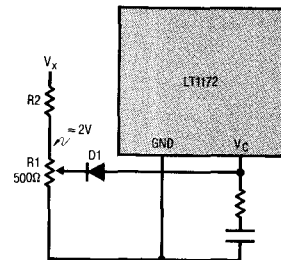
External Current Limit



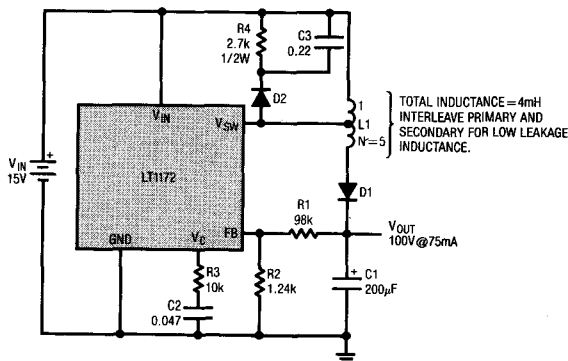
Positive to Negative Buck-Boost Converter



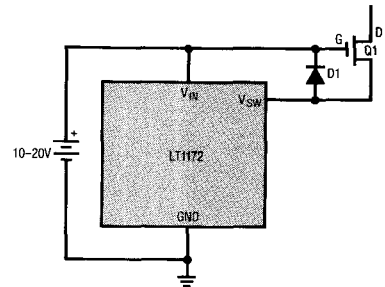
External Current Limit



Voltage Boosted Boost Converter

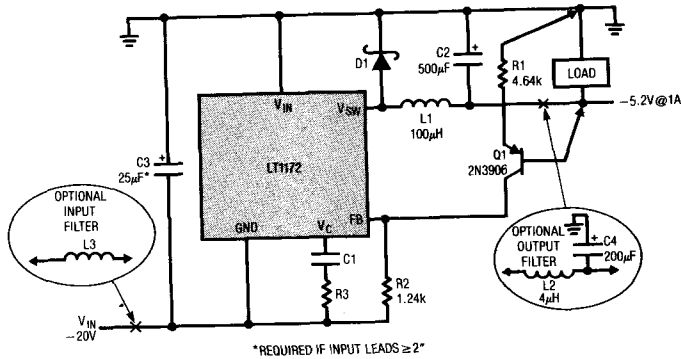


**Driving High Voltage FET
(for Offline Applications, See AN-25)**

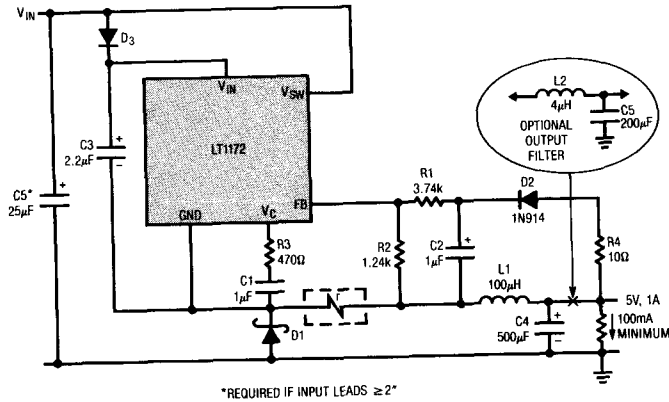


TYPICAL APPLICATIONS

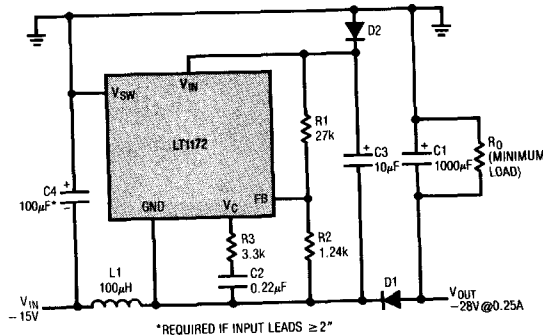
Negative Buck Converter



Positive Buck Converter

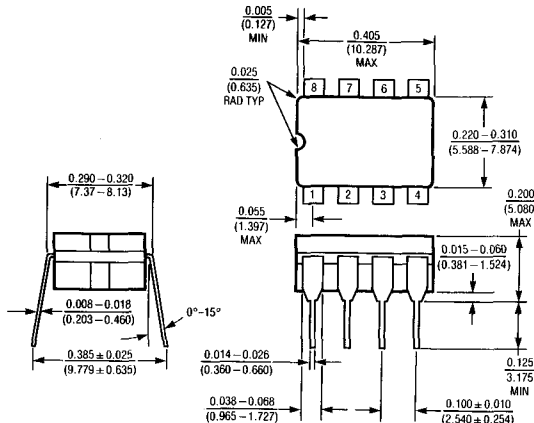


Negative Boost Regulator



PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

J Package
8-Lead Ceramic DIP

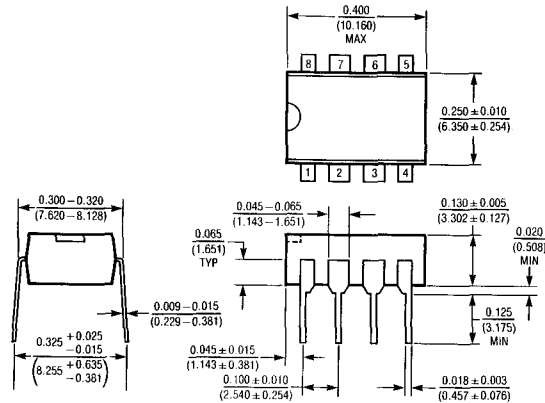


J8168

T_{JMAX}	θ_{JA}
150°C	100°C/W

Based on continuous operation.

N Package
8-Lead Plastic DIP



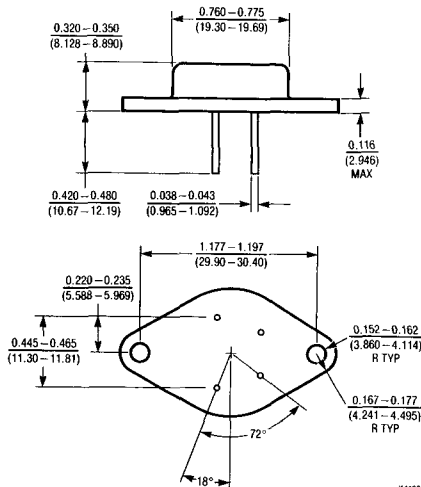
N8168

T_{JMAX}	θ_{JA}
100°C*	130°C/W

Based on continuous operation.

* T_{JMAX} = 125°C for intermittent fault conditions.

K Package
4-Lead TO-3 Metal Can



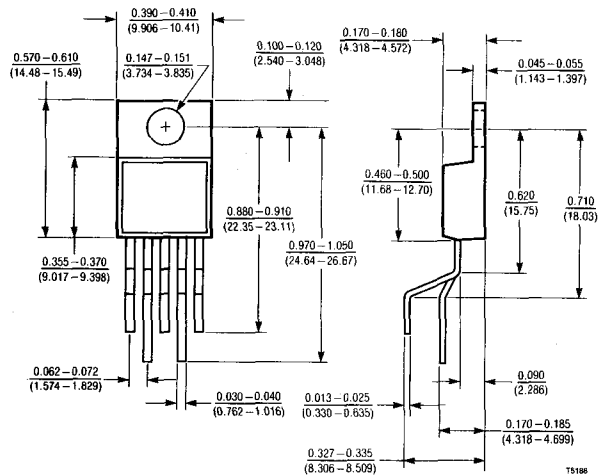
K4168

	T_{JMAX}	θ_{JC}	θ_{JA}
LT1172MK, LT1172HVMK	150°C	8°C/W	35°C/W
LT1172CK, LT1172HVCK	100°C*	8°C/W	35°C/W

Based on continuous operation.

* T_{JMAX} = 125°C for intermittent fault conditions.

T Package
5-Lead TO-220



T5168

	T_{JMAX}	θ_{JC}	θ_{JA}
LT1172CT, LT1172HVCT	100°C*	8°C/W	75°C/W

Based on continuous operation.

* T_{JMAX} = 125°C for intermittent fault conditions.

FEATURES

- *Guaranteed* $\pm 2\%$ Reference Tolerance
- *Guaranteed* $\pm 6\%$ Oscillator Tolerance
- *Guaranteed* 10mV/1000 Hrs Long Term Stability
- Interchangeable with all SG1524 or LM1524 Devices
- Operates Above 100kHz

APPLICATIONS

- Switching Power Supplies
- Motor Speed Control
- Off-Line Power Converters

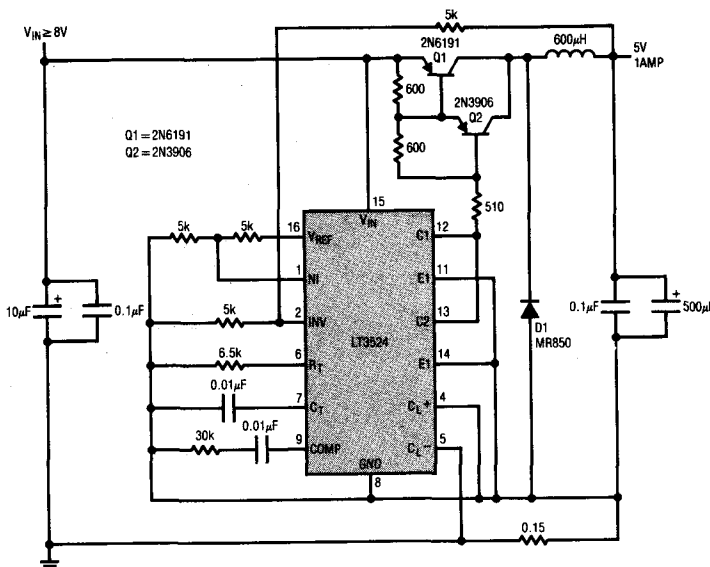
DESCRIPTION

The LT1524 PWM switching regulator control circuit contains all the essential circuitry to implement single-ended or push-pull switching regulators. Included on the circuit are oscillator, voltage reference, a pulse width modulator, error amplifier, overload protection circuitry and output drivers.

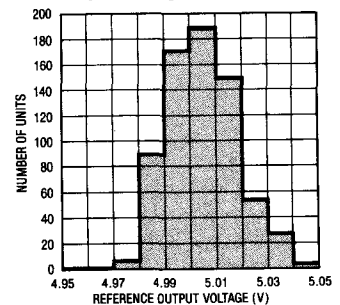
Although pin-for-pin and functionally compatible with industry standard 1524 and 3524 devices, Linear Technology has incorporated several improvements in the design of the LT1524. A subsurface zener reference has been used to provide excellent stability with time and the reference is trimmed at the wafer level to provide an initial accuracy of 2%. Additionally, the oscillator is trimmed to provide a maximum tolerance of 6%.

Linear Technology Corporation's advanced processing, design and passivation techniques make the LT1524 and LT3524 a superior and more reliable choice over previous devices.

5V, 1 Amp Regulator



Distribution of Reference Output Voltage

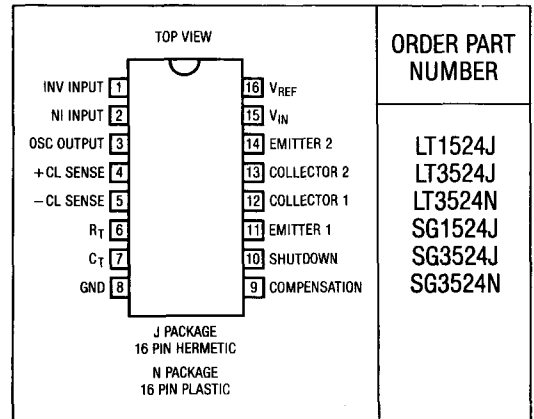


LT1524/LT3524 SG1524/SG3524

ABSOLUTE MAXIMUM RATINGS

Input Voltage	40V
Reference Output Current	50mA
Output Current (Each Output)	100mA
Oscillator Charging Current (Pin 6 or 7)	5mA
Internal Power Dissipation (Note 1)	1W
Operating Temperature Range	
LT1524/SG1524	-55°C to +125°C
LT3524/SG3524	0°C to +70°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°C

PACKAGE/ORDER INFORMATION



ELECTRICAL CHARACTERISTICS (Note 2)

PARAMETER	CONDITIONS	LT1524			SG1524			UNITS	
		MIN	TYP	MAX	MIN	TYP	MAX		
Reference Section:									
Output Voltage		●	4.9	5.0	5.1	4.8	5.0	5.2	V
Line Regulation	$V_{IN} = 8V$ to 40V	●		2	10		10	20	mV
Load Regulation	$I_L = 0mA$ to 20mA	●		10	20		20	50	mV
Ripple Rejection	$f = 120Hz$			80			66		dB
Short Circuit Current Limit	$V_{REF} = 0$			100			100		mA
Temperature Stability		●		0.3	1		0.3	1	%
Long Term Stability				2	10		20		mV/khr
Oscillator Section:									
Maximum Frequency	$C_T = 0.001\mu F$, $R_T = 2k\Omega$	●		300			300		kHz
Initial Accuracy	R_T and C_T Constant			3	6		5		%
Voltage Stability	$V_{IN} = 8V$ to 40V				1			1	%
Temperature Stability	Note 3	●		2			2		%
Output Amplitude	Pin 3			3.5			3.5		V
Output Pulse Width	$C_T = 0.01\mu F$, $T_A = 25^\circ C$			0.5			0.5		μs
Error Amplifier Section:									
Input Offset Voltage	$V_{CM} = 2.5V$	●		0.5	5		0.5	5	mV
Input Bias Current	$V_{CM} = 2.5V$	●		0.5	2		2	10	μA
Open Loop Voltage Gain		●		72	80		72	80	dB
Common-Mode Voltage		●		1.8	3.4		1.8	3.4	V
Common-Mode Rejection Ratio				70	86		70		dB
Small Signal Bandwidth	$A_V = 0dB$			3			3		MHz
Output Voltage				0.5	3.8		0.5	3.8	V

ELECTRICAL CHARACTERISTICS

PARAMETER	CONDITIONS	LT1524			SG1524			UNITS	
		MIN	TYP	MAX	MIN	TYP	MAX		
Comparator Section:									
Minimum Duty Cycle		●		0		0		%	
Maximum Duty Cycle		●	45	49		45	49	%	
Input Threshold	Zero Duty Cycle	●		1		1		V	
Input Threshold	Max Duty Cycle	●		3.5		3.5		V	
Input Bias Current		●	0.2	2		1		μA	
Current Limiting Section:									
Sense Voltage	Pin 9 = 2V with Error Amplifier Set for Max Out		190	200	210	190	200	210	mV
Sense Voltage T.C.		●		0.2		0.2		mV/°C	
Common-Mode Voltage		●	-0.7		1	-0.7		1	V
Output Section: (Each Output)									
Collector-Emitter Voltage		●	40			40			V
Collector Leakage Current	$V_{CE} = 40V$	●		0.1	50		0.1	50	μA
Saturation Voltage	$I_C = 50mA$	●		1	2		1	2	V
Emitter Output Voltage	$V_{IN} = 20V$	●	17	18		17	18		V
Rise Time	$R_C = 2k\Omega$			0.2			0.2		μS
Fall Time	$R_C = 2k\Omega$			0.1			0.1		μS
Total Standby Current:	$V_{IN} = 40V$ (Note 4)	●		8	10		8	10	mA

ELECTRICAL CHARACTERISTICS (Note 2)

PARAMETER	CONDITIONS	LT3524			SG3524			UNITS	
		MIN	TYP	MAX	MIN	TYP	MAX		
Reference Section:									
Output Voltage		●	4.9	5.0	5.1	4.6	5.0	5.4	V
Line Regulation	$V_{IN} = 8V$ to 40V	●		3	10		10	30	mV
Load Regulation	$I_L = 0mA$ to 20mA	●		10	20		20	50	mV
Ripple Rejection	$f = 120Hz$			80			66		dB
Short Circuit Current Limit	$V_{REF} = 0$			100			100		mA
Temperature Stability		●		0.3	1		0.3	1	%
Long Term Stability				2	10		20		mV/chr
Oscillator Section:									
Maximum Frequency	$C_T = 0.001\mu F$, $R_T = 2k\Omega$	●		300			300		kHz
Initial Accuracy	R_T and C_T Constant			3	6		5		%
Voltage Stability	$V_{IN} = 8V$ to 40V				1			1	%
Temperature Stability	Note 3	●		2			2		%
Output Amplitude	Pin 3				3.5			3.5	V
Output Pulse Width	$C_T = 0.01\mu F$, $T_A = 25^\circ C$				0.5			0.5	μS
Error Amplifier Section:									
Input Offset Voltage	$V_{CM} = 2.5V$	●		1	5		2	10	mV
Input Bias Current	$V_{CM} = 2.5V$	●		0.5	2		2	10	μA
Open Loop Voltage Gain		●	72	80			60	80	dB
Common-Mode Voltage				1.8	3.4		1.8	3.4	V
Common-Mode Rejection Ratio			70	86			70		dB
Small Signal Bandwidth	$A_V = 0dB$			3			3		MHz
Output Voltage			0.5		3.8		0.5	3.8	V

ELECTRICAL CHARACTERISTICS

PARAMETER	CONDITIONS	LT3524			SG3524			UNITS	
		MIN	TYP	MAX	MIN	TYP	MAX		
Comparator Section:									
Minimum Duty Cycle		●	0			0			%
Maximum Duty Cycle		●	45	49		45	49		%
Input Threshold	Zero Duty Cycle	●	1			1			V
Input Threshold	Max Duty Cycle	●	3.5			3.5			V
Input Bias Current		●	1	2		1			μA
Current Limiting Section:									
Sense Voltage	Pin 9 = 2V with Error Amplifier Set for Max Out		190	200	210	180	200	220	mV
Sense Voltage T.C.		●	0.2			0.2			mV/°C
Common-Mode Voltage		●	-1		1	-1		1	V
Output Section: (Each Output)									
Collector-Emitter Voltage		●	40			40			V
Collector Leakage Current	$V_{CE} = 40V$	●	0.1			50	0.1	50	μA
Saturation Voltage	$I_C = 50mA$	●	1			2	1	2	V
Emitter Output Voltage	$V_{IN} = 20V$	●	17	18		17	18		V
Rise Time	$R_C = 2k\Omega$		0.2			0.2			μs
Fall Time	$R_C = 2k\Omega$		0.1			0.1			μs
Total Standby Current:	$V_{IN} = 40V$ (Note 4)	●	8			10	8	10	mA

The ● denotes specifications that apply over the full operating temperature range.

The shaded electrical specifications indicate those parameters which have been improved or guaranteed test limits provided for the first time.

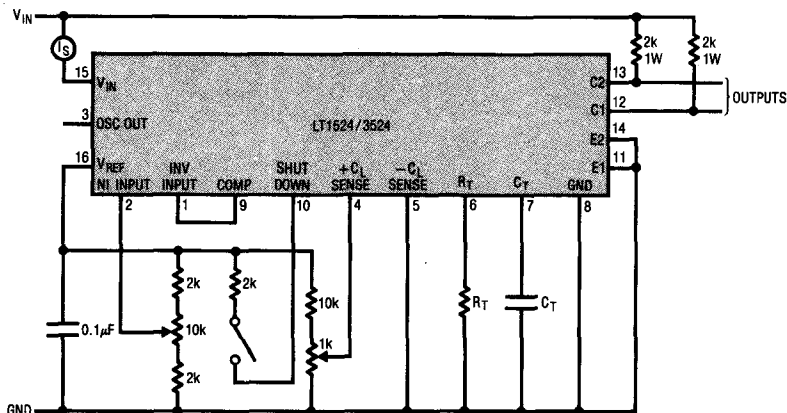
Note 1: For operating at elevated temperatures, the device in the J package must be derated at 100°C/W to a maximum junction temperature of 150°C, while the device in the N package is derated at 150°C/W to a maximum junction temperature of 115°C.

Note 2: These specifications apply for $V_{IN} = 20V$, $f = 20kHz$, $T_A = 25^\circ C$ unless otherwise noted.

Note 3: Although many manufacturers specify a maximum specification of 2%, Linear Technology's experience is that this specification is not being presently met by other manufacturers. Linear Technology's basic design, although improved, is essentially identical to other manufacturers' devices. Linear Technology is, however, unwilling to place a maximum specification on its data sheet which cannot be met or guaranteed.

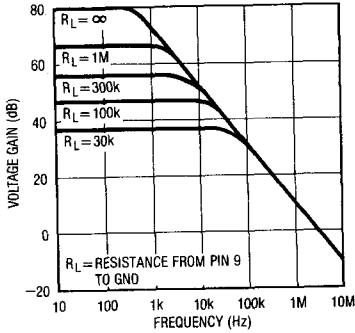
Note 4: Standby current does not include the oscillator charging current, error and current limit dividers, and the outputs are open circuit.

TEST CIRCUIT

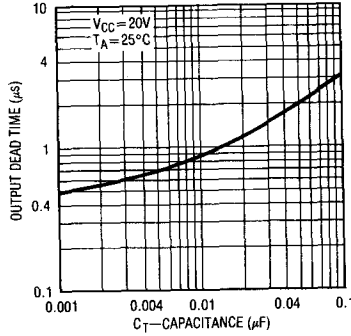


TYPICAL PERFORMANCE CHARACTERISTICS

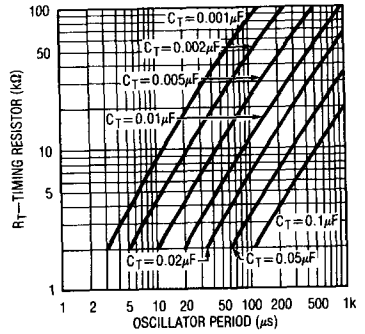
Error Amplifier Gain



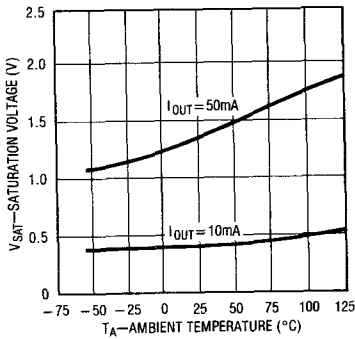
Output Dead Time



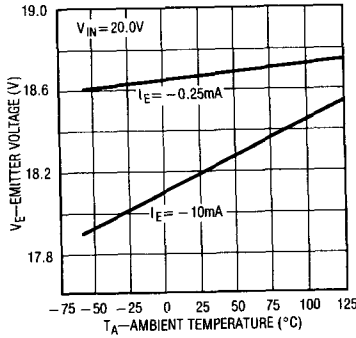
Oscillator Period



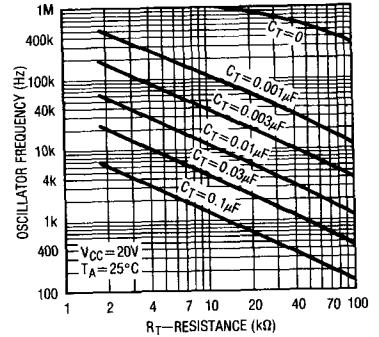
Output Transistor Saturation Voltage



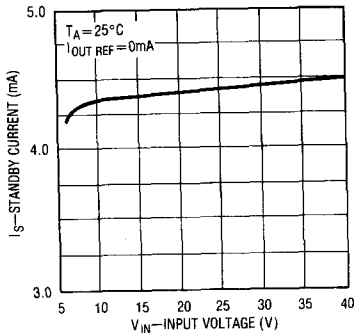
Output Transistor Emitter Voltage



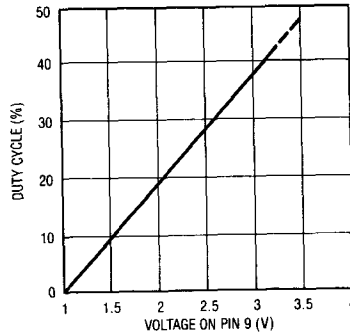
Oscillator Frequency vs Timing Resistance



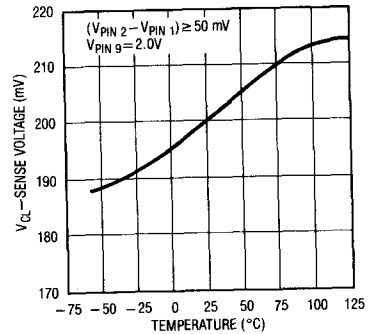
Standby Current



Duty Cycle



Current Limit Sense Voltage ($V_{PIN 4} - V_{PIN 5}$)



APPLICATIONS INFORMATION

FUNCTIONAL DESCRIPTION AND PIN FUNCTIONS

Voltage Regulator

The internal 5V regulator (input pin 15, output pin 16) supplies a regulated 5V to all internal circuitry, as well as up to 50mA for external circuitry. For operation below 8V input, pins 15 and 16 may be tied together and 5V to 6V externally applied.

Oscillator

The internal oscillator circuitry sets the frequency of operation for the switching regulator. The oscillator waveform is a ramp from about 1V to 3.5V (pin 7). Frequency is set by a timing resistor from pin 6 to ground and a capacitor from pin 7 to ground. The oscillator period is approximately RC for the recommended range of 1.8k to 100k for R and 0.001 μ F to 0.1 μ F for C .

The fall time of the ramp sets the blanking or dead time where both outputs are off in push-pull regulators. This is controlled by the value of the capacitor alone.

Output Transistors

The two output transistors have both the emitters (pins 11 and 14) and the collectors available (pins 12 and 13). Internal current limiting for both of these transistors is about 100mA. The two transistors are driven 180° out of phase by the flip-flop. For single-ended operation they should be connected in parallel.

Error Amplifier

The differential input (pins 1 and 2) single-ended output (pin 9) transconductance amplifier provides about 80dB of gain, as well as providing a point for loop frequency compensation or electronic shutdown.

DC gain of the loop can be controlled by resistive loading, while AC compensation is usually accomplished with a series R-C connected from pin 9 to ground. The output impedance at pin 9 is about 5M Ω and current is about 200 μ A, so external op-amps or voltage sources can easily drive the comparator input. Normally, the 5V reference is divided down to generate a voltage within the common-mode range of the error amplifier.

Synchronous Operation

When an external clock is desired, a clock pulse of approximately 3V can be applied directly to the oscillator output, pin 3. The impedance to ground at this point is approximately 2k Ω . In this configuration, $R_T C_T$ must be selected for a clock period slightly greater than that of the external clock.

If two or more LT1524 regulators are to be operated synchronously, all oscillator output terminals should be tied together. The oscillator programmed for the minimum clock period will be the master from which all the other LT1524s operate. In this application, the $C_T R_T$ values of the slaved regulators must be set for a period approximately 10% longer than that of the master regulator. In addition, C_T (master) = 2 C_T (slave) to ensure that the master output pulse, which occurs first, has a wider pulse width and will subsequently reset the slave regulators.

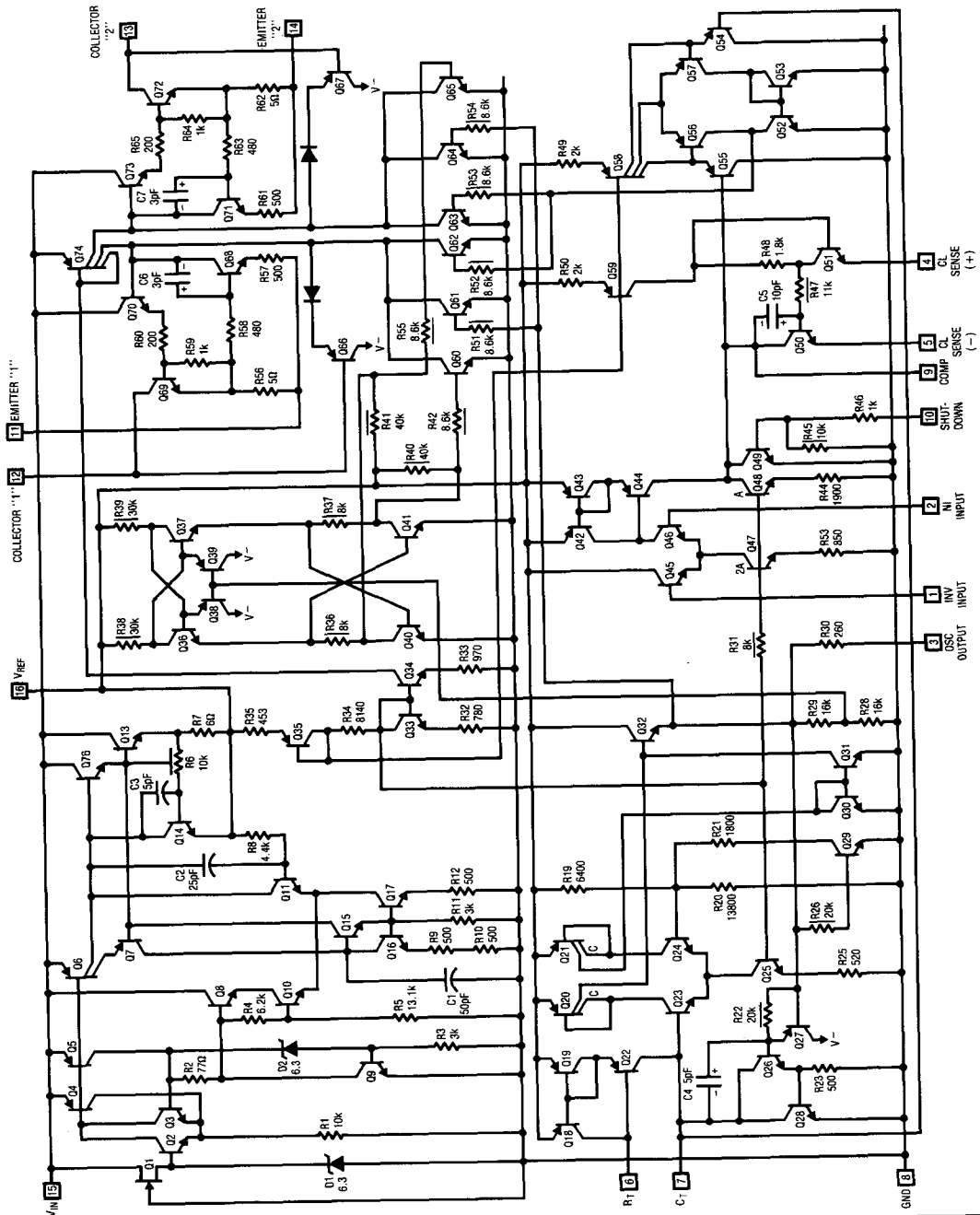
Shutdown

A logic high at pin 10 will shut down the regulator and cause both output transistors to turn off.

Current Limit

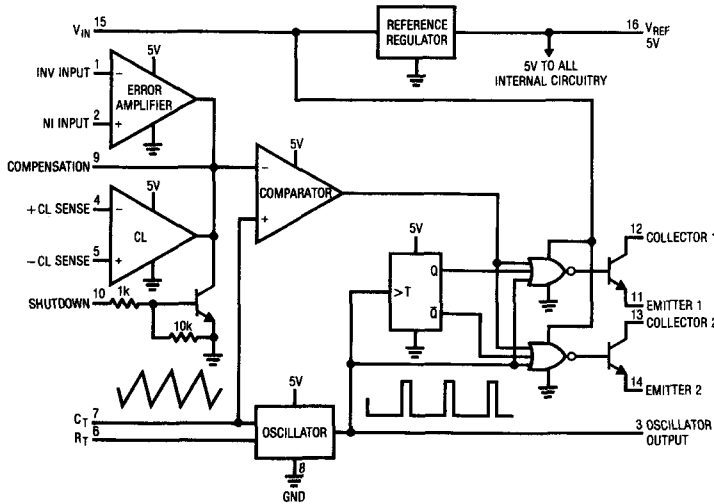
Current limiting is activated when the voltage between pins 4 and 5 exceeds 200mV. The output of the current limit amplifier internally sums with the error amplifier to shorten the output pulse width. The gain of the current limit circuitry is relatively low, so current control in limit is typically about 5%. Two areas of caution should be observed with current limiting. First, the response time of the current limit is set by the loop roll-off on pin 9. Fast current limiting requires external circuitry. Second, the common-mode range of the current limit amplifier is limited. Even fast spikes outside this range can disrupt operation.

SCHEMATIC DIAGRAM



LT1524/LT3524 SG1524/SG3524

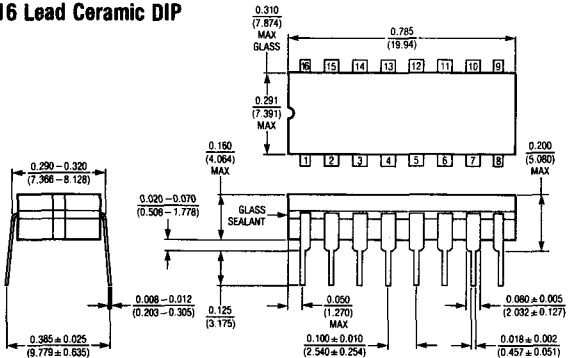
BLOCK DIAGRAM



PACKAGE DESCRIPTION

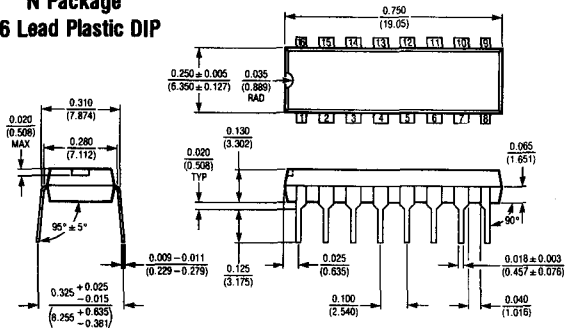
J Package 16 Lead Ceramic DIP

	T _J MAX	θ _{JA}	θ _{JC}
LT1524J SG1524J	150°C	100°C/W	30°C/W
LT3524J SG3524J	150°C	100°C/W	30°C/W



N Package 16 Lead Plastic DIP

	T _J MAX	θ _{JA}	θ _{JC}
LT3524N SG3524N	115°C	140°C/W	-50°C/W



FEATURES

- $\pm 5\%$ Typ. Oscillator Tolerance
- 20mV/1000 Hrs Typ. Long Term Stability
- Interchangeable with all SG3524 or LM3524 Devices
- Operates Above 100kHz

APPLICATIONS

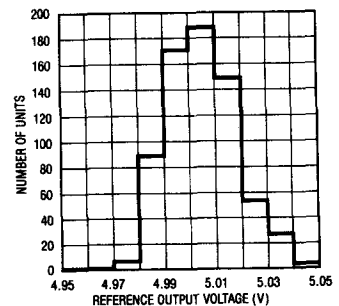
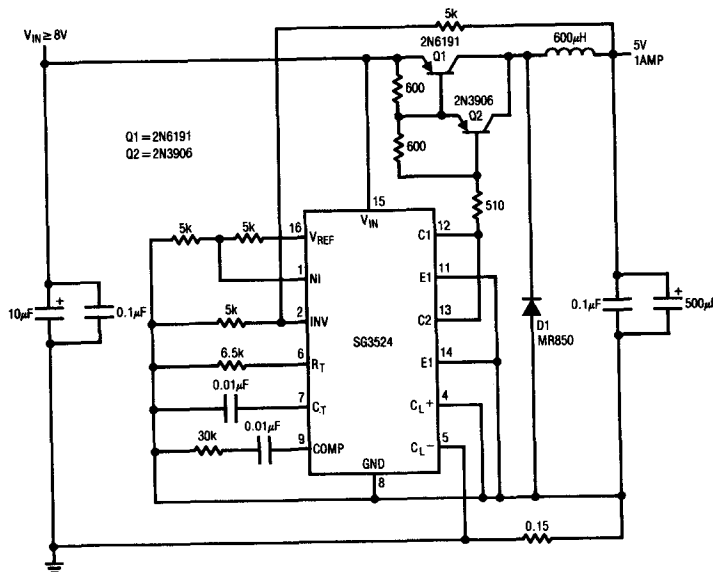
- Switching Power Supplies
- Motor Speed Control
- Off-Line Power Converters

DESCRIPTION

The SG3524 PWM switching regulator control circuit contains all the essential circuitry to implement single-ended or push-pull switching regulators. Included on the circuit are oscillator, voltage reference, a pulse width modulator, error amplifier, overload protection circuitry and output drivers.

Although pin-for-pin and functionally compatible with industry standard 3524 devices, Linear Technology has incorporated several improvements in the design of the 3524. A subsurface zener reference has been used to provide excellent stability with time and the reference is trimmed at the wafer level.

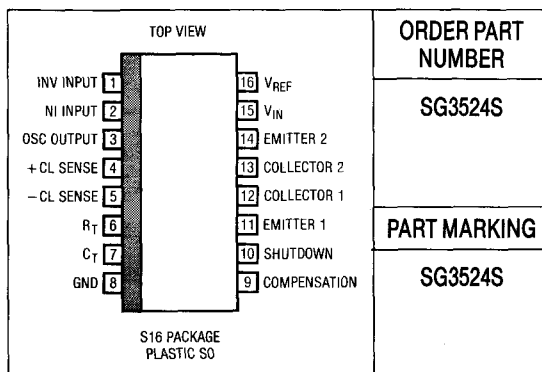
Linear Technology Corporation's advanced processing, design and passivation techniques make the SG3524 a superior and more reliable choice over previous devices.

5V, 1 Amp Regulator
Distribution of Reference Output Voltage


ABSOLUTE MAXIMUM RATINGS

Input Voltage	40V
Reference Output Current	50mA
Output Current (Each Output)	100mA
Oscillator Charging Current (Pin 6 or 7)	5mA
Internal Power Dissipation (Note 1)	1W
Operating Temperature Range	0°C to 70°C
Storage Temperature Range	- 65°C to 150°C
Lead Temperature (Soldering, 10 sec.)	300°C

PACKAGE/ORDER INFORMATION



ELECTRICAL CHARACTERISTICS (Note 2)

PARAMETER	CONDITIONS	SG3524			UNITS
		MIN	TYP	MAX	
Reference Section:					
Output Voltage		4.6	5.0	5.4	V
Line Regulation	$V_{IN} = 8V \text{ to } 40V$		10	30	mV
Load Regulation	$I_L = 0mA \text{ to } 20mA$		20	50	mV
Ripple Rejection	$f = 120Hz$		66		dB
Short Circuit Current Limit	$V_{REF} = 0$		100		mA
Temperature Stability			0.3	1	%
Long Term Stability			20		mV/√khr
Oscillator Section:					
Maximum Frequency	$C_T = 0.001\mu F, R_T = 2k\Omega$		300		kHz
Initial Accuracy	R_T and C_T Constant		5		%
Voltage Stability	$V_{IN} = 8V \text{ to } 40V$			1	%
Temperature Stability	Note 3		2		%
Output Amplitude	Pin 3		3.5		V
Output Pulse Width	$C_T = 0.01\mu F, T_A = 25^\circ C$		0.5		μs
Error Amplifier Section:					
Input Offset Voltage	$V_{CM} = 2.5V$		2	10	mV
Input Bias Current	$V_{CM} = 2.5V$		2	10	μA
Open Loop Voltage Gain		60	80		dB
Common-Mode Voltage		1.8		3.4	V
Common-Mode Rejection Ratio			70		dB
Small Signal Bandwidth	$A_V = 0dB$		3		MHz
Output Voltage		0.5		3.8	V
Comparator Section:					
Duty Cycle	% Each Output On	0		45	%
Input Threshold	Zero Duty Cycle		1		V
Input Threshold	Max Duty Cycle		3.5		V
Input Bias Current			1		μA

ELECTRICAL CHARACTERISTICS (Note 2)

PARAMETER	CONDITIONS	SG3524			UNITS
		MIN	TYP	MAX	
Current Limiting Section:					
Sense Voltage	Pin 9 = 2V with Error Amplifier Set for Max Out	180	200	220	mV
Sense Voltage T.C.			0.2		mV/°C
Common-Mode Voltage		-1		1	V
Output Section: (Each Output)					
Collector-Emitter Voltage		40			V
Collector Leakage Current	$V_{CE} = 40V$		0.1	50	μA
Saturation Voltage	$I_C = 50mA$		1	2	V
Emitter Output Voltage	$V_{IN} = 20V$	17	18		V
Rise Time	$R_C = 2k\Omega$		0.2		μs
Fall Time	$R_C = 2k\Omega$		0.1		μs
Total Standby Current:	$V_{IN} = 40V$ (Note 4)		8	10	mA

The ● denotes specifications that apply over the full operating temperature range.

Note 1: For operating at elevated temperatures, the device in the SO package must be derated at 100°C/W to a maximum junction temperature of 115°C.

Note 2: These specifications apply for $V_{IN} = 20V$, $f = 20kHz$, $T_A = 25^\circ C$ unless otherwise noted.

Note 3: Although many manufacturers specify a maximum specification of 2%, Linear Technology's experience is that this specification is not being presently met by other manufacturers. Linear Technology's basic design, although improved, is essentially identical to other manufacturer's devices. Linear Technology is, however, unwilling to place a maximum specification on its data sheet which cannot be met or guaranteed.

Note 4: Standby current does not include the oscillator charging current, error and current limit dividers, and the outputs are open circuit.

NOTES

Regulating Pulse Width Modulators

FEATURES

- Undervoltage Lockout with Hysteresis
- *Guaranteed* 1% 5.1V Reference
- *Guaranteed* 10mV/1000 Hr Long Term Stability
- Latching PWM
- 8V to 35V Operation
- 100Hz to 400kHz Oscillator
- 400mA Source and Sink Current

APPLICATIONS

- Switching Power Supplies
- Motor Speed Control
- Power Converters

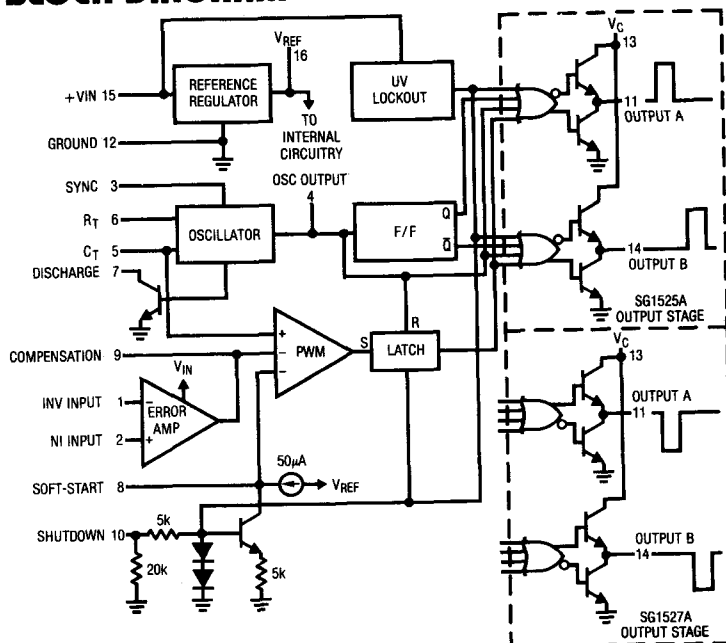
DESCRIPTION

The LT1525A and LT1527A are improved general purpose switching regulator control circuits. Included on the chip are a trimmed 1% voltage subsurface zener reference, oscillator, comparator and high current class B totem pole output drivers. Included in the design of the LT1525A are easy synchronization to an external clock, soft-start and adjustable deadtime control. A shutdown pin allows instantaneous shutdown.

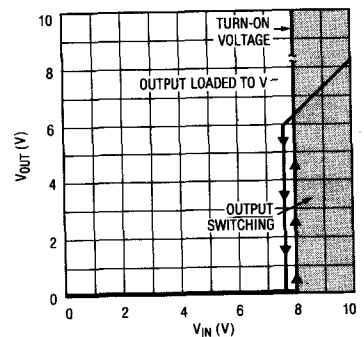
The LT1525A and LT1527A differ only in their output logic phasing. The LT1525A has a low output during the "off" state, while the LT1527A has a high output during the "off" state. Both devices have undervoltage lockout with about 0.5V hysteresis, giving reliable operation even with slowly varying supplies.

The combination of improved features and advanced processing for high reliability make Linear Technology's switching regulators a supreme choice.

BLOCK DIAGRAM



LT1525A Start-Up



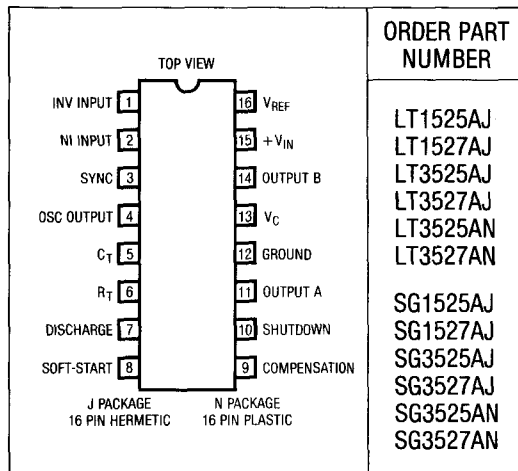
LT/SG1525A, LT/SG3525A
 LT/SG1527A, LT/SG3527A

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage (+V _{IN})	+40V
Logic Inputs	-0.3V to +5.5V
Analog Inputs	-0.3V to +V _{IN}
Output Current, Source or Sink	500mA
Reference Output Current	50mA
Oscillator Charging Current	5mA
Power Dissipation at T _A = +25°C (Note 2)	1000mW
Thermal Resistance: Junction to Ambient	100°C/W
Power Dissipation at T _C = +25°C (Note 3)	2000mW
Thermal Resistance: Junction to Case	60°C/W
Operating Temperature Range	
1525A, 1527A	-55°C to 150°C
3525A, 3527A	0°C to 70°C
Storage Temperature Range	-65°C to 150°C
Lead Temperature (Soldering, 10 sec.)	+300°C

PACKAGE/ORDER INFORMATION



ORDER PART NUMBER

LT1525AJ
LT1527AJ
LT3525AJ
LT3527AJ
LT3525AN
LT3527AN
SG1525AJ
SG1527AJ
SG3525AJ
SG3527AJ
SG3525AN
SG3527AN

RECOMMENDED OPERATING CONDITIONS

(Note 4)

Input Voltage (+V _{IN})	+8V to +35V	Reference Load Current	0mA to 20mA
Collector Supply Voltage (V _C)	+4.5V to +35V	Oscillator Frequency Range	100Hz to 400kHz
Sink / Source Load Current (Steady State)	0mA to 100mA	Oscillator Timing Resistor	2kΩ to 150kΩ
Sink / Source Load Current (Peak)	0mA to 400mA	Oscillator Timing Capacitor	0.001μF to 0.1μF
		Deadtime Resistor Range	0Ω to 500Ω

ELECTRICAL CHARACTERISTICS V_{IN} = +20V unless otherwise noted

PARAMETER	CONDITIONS	LT1525A LT1527A			SG1525A SG1527A			UNITS	
		MIN	TYP	MAX	MIN	TYP	MAX		
REFERENCE SECTION									
Output Voltage	T _J = 25°C	5.05	5.10	5.15	5.05	5.10	5.15	V	
Line Regulation	V _{IN} = 8V to 35V	●	5	10	10	20		mV	
Load Regulation	I _L = 0mA to 20mA	●	20	50	20	50		mV	
Temperature Stability		●	20	50	20	50		mV	
Total Output Variation	Line, Load, and Temperature	●	5.0	5.1	5.2	5.0	5.1	5.2	V
Short Circuit Current	V _{REF} = 0, T _J = 25°C		80	100	80	100		mA	
Output Noise Voltage	10Hz ≤ f ≤ 10kHz, T _J = 25°C		40	200	40	200		μVrms	
Long Term Stability	T _J = 125°C		1	10	20	50		mV/√Khr	

ELECTRICAL CHARACTERISTICS

PARAMETER	CONDITIONS	LT1525A LT1527A			SG1525A SG1527A			UNITS	
		MIN	TYP	MAX	MIN	TYP	MAX		
OSCILLATOR SECTION (Note 6)									
Initial Accuracy	$T_j = 25^\circ\text{C}$ (Note 6)		2	6		2	6	%	
Voltage Stability	$V_{IN} = 8\text{V to }35\text{V}$	●	0.5	1		0.3	1	%	
Temperature Stability		●	3	6		3	6	%	
Minimum Frequency	$R_f = 150\text{k}\Omega$, $C_f = 0.1\mu\text{F}$	●		100			100	Hz	
Maximum Frequency	$R_f = 2\text{k}\Omega$, $C_f = 1\text{nF}$	●	400			400		kHz	
Current Mirror	$I_{RT} = 2\text{mA}$	●	1.7	2.0	2.2	1.7	2.0	2.2	mA
Clock Amplitude		●	3.0	3.5		3.0	3.5	V	
Clock Width	$T_j = 25^\circ\text{C}$		0.3	0.5	1	0.3	0.5	1	μs
Sync Threshold		●	1.2	2.0	2.8	1.2	2.0	2.8	V
Sync Input Current	Sync Voltage = 3.5V	●		1.0	2.5		1.0	2.5	mA
ERROR AMPLIFIER SECTION ($V_{CM} = 5.1\text{V}$)									
Input Offset Voltage		●		0.5	5		0.5	5	mV
Input Bias Current		●		0.2	3		1	10	μA
Input Offset Current		●			0.5			1	μA
DC Open Loop Gain	$R_L \geq 10\text{M}\Omega$	●	70	80		60	75	dB	
Gain Bandwidth Product	$A_V = 0\text{dB}$, $T_j = 25^\circ\text{C}$ (Note 5)		1	2		1	2	MHz	
Output Low Level		●		0.2	0.5		0.2	0.5	V
Output High Level		●	3.8	5.6		3.8	5.6	V	
Common Mode Rejection	$V_{CM} = 1.5\text{V to }5.2\text{V}$	●	75	90		60	75	dB	
Supply Voltage Rejection	$V_{IN} = 8\text{V to }35\text{V}$	●	75	90		50	60	dB	
PWM COMPARATOR									
Minimum Duty Cycle		●			0			0	%
Maximum Duty Cycle		●	45	49		45	49	%	
Input Threshold	Zero Duty Cycle (Note 6)	●	0.6	0.9		0.6	0.9	V	
Input Threshold	Max Duty Cycle (Note 6)	●		3.3	3.6		3.3	3.6	V
Input Bias Current		●		0.05	1.0		0.05	1.0	μA
SOFT-START SECTION									
Soft-Start Current	$V_{SHUTDOWN} = 0\text{V}$	●	25	50	80	25	50	80	μA
Soft-Start Voltage	$V_{SHUTDOWN} = 2\text{V}$	●		0.4	0.6		0.4	0.6	V
Shutdown Input Current	$V_{SHUTDOWN} = 2.5\text{V}$	●		0.4	1.0		0.4	1.0	mA
OUTPUT DRIVERS (Each Output) ($V_C = 20\text{V}$)									
Undervoltage Lockout Hysteresis			0.2	0.6	1	0.2	0.6	1	V
Output Low Level	$I_{SINK} = 20\text{mA}$	●		0.2	0.4		0.2	0.4	V
	$I_{SINK} = 100\text{mA}$	●		1.0	2.0		1.0	2.0	V
Output High Level	$I_{SOURCE} = 20\text{mA}$	●	18	19		18	19	V	
	$I_{SOURCE} = 100\text{mA}$	●	17	18		17	18	V	
Undervoltage Lockout	V_{COMP} and $V_{SS} = \text{High}$	●	6	7	8	6	7	8	V
Collector Leakage	$V_C = 35\text{V}$ (Note 7)	●			200			200	μA
Rise Time	$C_L = 1\text{nF}$, $T_j = 25^\circ\text{C}$ (Note 5)			100	600		100	600	ns
Fall Time	$C_L = 1\text{nF}$, $T_j = 25^\circ\text{C}$ (Note 5)			50	300		50	300	ns
Shutdown Delay	$V_{SD} = 3\text{V}$, $C_S = 0$, $T_j = 25^\circ\text{C}$ (Note 5)			0.2	0.5		0.2	0.5	μs
TOTAL STANDBY CURRENT									
Supply Current	$V_{IN} = 35\text{V}$	●		14	20		14	20	mA

ELECTRICAL CHARACTERISTICS

PARAMETER	CONDITIONS	LT3525A LT3527A			SG3525A SG3527A			UNITS	
		MIN	TYP	MAX	MIN	TYP	MAX		
REFERENCE SECTION									
Output Voltage	$T_J = 25^\circ\text{C}$	5.05	5.10	5.15	5.00	5.10	5.20	V	
Line Regulation	$V_{IN} = 8\text{V to }35\text{V}$	●	5	10	10	20		mV	
Load Regulation	$I_L = 0\text{mA to }20\text{mA}$	●	20	50	20	50		mV	
Temperature Stability		●	20	50	20	50		mV	
Total Output Variation	Line, Load, and Temperature	●	4.95	5.1	5.25	4.95	5.25	V	
Short Circuit Current	$V_{REF} = 0, T_J = 25^\circ\text{C}$		80	100	80	100		mA	
Output Noise Voltage	$10\text{Hz} \leq f \leq 10\text{kHz}, T_J = 25^\circ\text{C}$		40	100	40	200		μVrms	
Long Term Stability	$T_J = 125^\circ\text{C}$		1	10	20	50		mV/khr	
OSCILLATOR SECTION (Note 6)									
Initial Accuracy	$T_J = 25^\circ\text{C}$ (Note 6)		2	6	2	6		%	
Voltage Stability	$V_{IN} = 8\text{V to }35\text{V}$	●	0.5	2	1	2		%	
Temperature Stability		●	3	6	3	6		%	
Minimum Frequency	$R_T = 150\text{k}\Omega, C_T = 0.1\mu\text{F}$	●		100		100		Hz	
Maximum Frequency	$R_T = 2\text{k}\Omega, C_T = 1\text{nF}$	●	400		400			kHz	
Current Mirror	$I_{RT} = 2\text{mA}$	●	1.7	2.0	2.2	1.7	2.0	2.2	mA
Clock Amplitude		●	3.0	3.5	3.0	3.5		V	
Clock Width	$T_J = 25^\circ\text{C}$		0.3	0.5	1.0	0.3	0.5	1.0	μs
Sync Threshold		●	1.2	2.0	2.8	1.2	2.0	2.8	V
Sync Input Current	Sync Voltage = 3.5V	●	1.0	2.5	1.0	2.5		mA	
ERROR AMPLIFIER SECTION ($V_{CM} = 5.1\text{V}$)									
Input Offset Voltage		●	2	5	2	10		mV	
Input Bias Current		●	1	3	1	10		μA	
Input Offset Current		●		0.5		1		μA	
DC Open Loop Gain	$R_L \geq 10\text{M}\Omega$	●	70	80	60	75		dB	
Gain Bandwidth Product	$A_V = 0\text{dB}, T_J = 25^\circ\text{C}$ (Note 5)		1	2	1	2		MHz	
Output Low Level		●	0.2	0.5	0.2	0.5		V	
Output High Level		●	3.8	5.6	3.8	5.6		V	
Common Mode Rejection	$V_{CM} = 1.5\text{V to }5.2\text{V}$	●	75	90	60	75		dB	
Supply Voltage Rejection	$V_{IN} = 8\text{V to }35\text{V}$	●	75	90	50	60		dB	
PWM COMPARATOR									
Minimum Duty Cycle		●		0		0		%	
Maximum Duty Cycle		●	45	49	45	49		%	
Input Threshold	Zero Duty Cycle (Note 6)	●	0.6	0.9	0.6	0.9		V	
Input Threshold	Max Duty Cycle (Note 6)	●	3.3	3.6	3.3	3.6		V	
Input Bias Current		●	0.05	1.0	0.05	1.0		μA	
SOFT-START SECTION									
Soft-Start Current	$V_{SHUTDOWN} = 0\text{V}$	●	25	50	80	25	50	80	μA
Soft-Start Voltage	$V_{SHUTDOWN} = 2\text{V}$	●		0.4	0.6	0.4	0.6		V
Shutdown Input Current	$V_{SHUTDOWN} = 2.5\text{V}$	●		0.4	1.0	0.4	1.0		mA

ELECTRICAL CHARACTERISTICS

PARAMETER	CONDITIONS	LT3525A LT3527A			SG3525A SG3527A			UNITS	
		MIN	TYP	MAX	MIN	TYP	MAX		
OUTPUT DRIVERS (Each Output) ($V_C = 20V$)									
Undervoltage Lockout Hysteresis			0.2	0.6		0.2	0.6	V	
Output Low Level	$I_{SINK} = 20mA$	●		0.2	0.4		0.2	0.4	V
	$I_{SINK} = 100mA$	●		1.0	2.0		1.0	2.0	V
Output High Level	$I_{SOURCE} = 20mA$	●	18	19		18	19	V	
	$I_{SOURCE} = 100mA$	●	17	18		17	18	V	
Undervoltage Lockout	V_{COMP} and $V_{SS} = High$	●	6	7	8	6	7	8	V
Collector Leakage	$V_C = 35V$ (Note 7)	●			200		200	μA	
Rise Time	$C_L = 1nF$, $T_J = 25^\circ C$ (Note 5)			100	600		100	600	ns
Fall Time	$C_L = 1nF$, $T_J = 25^\circ C$ (Note 5)			50	300		50	300	ns
Shutdown Delay	$V_{SD} = 3V$, $C_S = 0$, $T_J = 25^\circ C$ (Note 5)			0.2	0.5		0.2	0.5	μS
TOTAL STANDBY CURRENT									
Supply Current	$V_{IN} = 35V$	●		14	20		14	20	mA

The ● denotes the specifications which apply of the full operating temperature range.

Note 1: Values beyond which damage may occur.

Note 2: Derate at 10mW/°C for ambient temperatures above +50°C.

Note 3: Derate at 16mW/°C for case temperatures above +25°C.

Note 4: Range over which the device is functional and parameter limits are guaranteed.

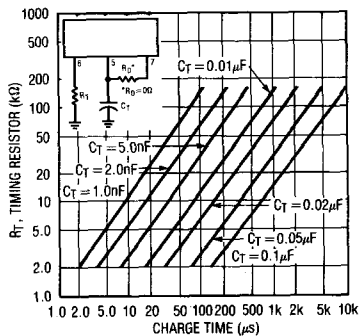
Note 5: These parameters, although guaranteed over the recommended operating conditions, are not 100% tested in production.

Note 6: Tested at $f_{OSC} = 40kHz$ ($R_T = 3.6k\Omega$, $C_T = 0.01\mu F$, $R_D = 0\Omega$).

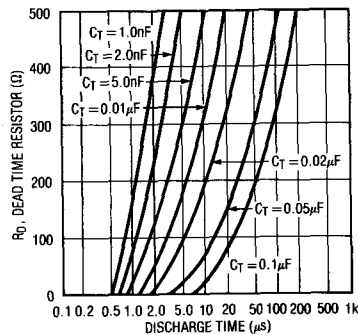
Note 7: Applies to 1525A/3525A only, due to polarity of output pulses.

TYPICAL PERFORMANCE CHARACTERISTICS

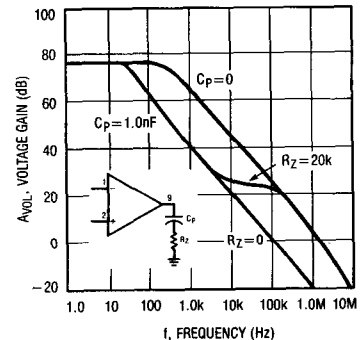
Oscillator Charge Time vs R_T



Oscillator Discharge Time

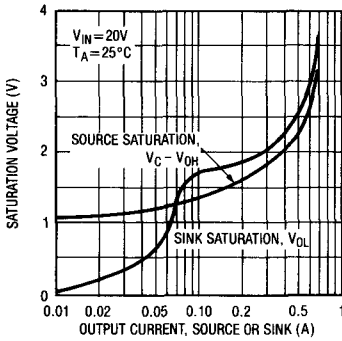


Error Amplifier Open Loop Frequency Response

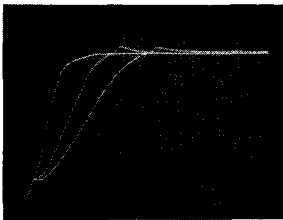
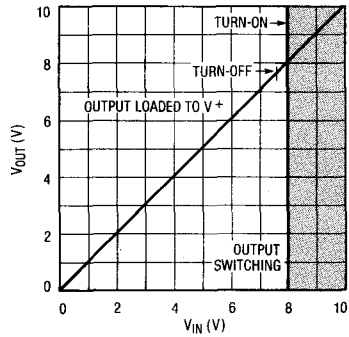


TYPICAL PERFORMANCE CHARACTERISTICS

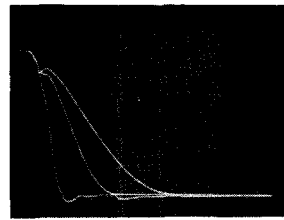
1525A Output Saturation Characteristics



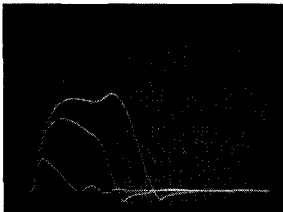
LT1527A Start-Up



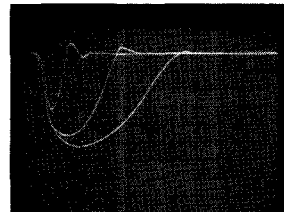
1525A/1527A
 $C_L = 1\text{kpF}$,
 $= 5\text{kpF}$,
 $= 10\text{kpF}$
 $V = 2.5V/\text{DIV}$
 $H = 100\text{ns}/\text{DIV}$



1525A/1527A
 $C_L = 1\text{kpF}$,
 $= 5\text{kpF}$,
 $= 10\text{kpF}$
 $V = 2.5V/\text{DIV}$
 $H = 100\text{ns}/\text{DIV}$



OUTPUT CURRENT
 $100\text{mA}/\text{DIV}$
 $100\text{ns}/\text{DIV}$



OUTPUT CURRENT
 $100\text{mA}/\text{DIV}$
 $100\text{ns}/\text{DIV}$

APPLICATIONS INFORMATION

Shutdown Options

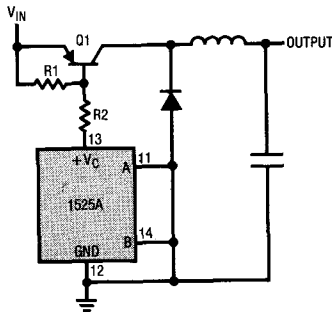
1. An external open collector comparator or transistor can be used to pull down the compensation pin (9). This will set the PWM latch and turn off both outputs. Pulse-by-pulse protection can be accomplished if the shutdown signal is momentary, since the PWM latch will be reset with each clock pulse.
2. Shutdown can also be accomplished by pulling down on the soft-start pin (8). When using this approach, shutdown will not affect the amplifier compensation network; however, if a soft-start capacitor is used, it must be discharged, possibly slowing shutdown response.

APPLICATIONS INFORMATION

- Applying a positive-going signal to the shutdown pin (10) will provide the most rapid shutdown of the outputs if a soft-start capacitor is not used at pin 8. An external soft-start capacitor at pin 8 will slow shutdown response due to the discharge time of the soft-start capacitor. Discharge current is approximately twice the charging current.
- The shutdown terminal can be used to set the PWM latch on a pulse-by-pulse basis if there is no external capacitance on pin 8. Soft-start characteristics may still be achieved by applying an external capacitor, blocking diode and charging resistor to the compensation pin (9).

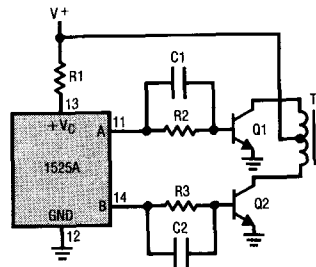
TYPICAL APPLICATIONS

Single Ended Supply



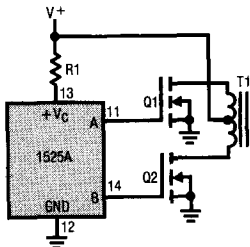
FOR SINGLE ENDED SUPPLIES, THE DRIVER OUTPUTS ARE GROUNDED. THE +V_C TERMINAL IS SWITCHED TO GROUND BY THE TÖTEM-POLE SOURCE TRANSISTORS ON EVERY OSCILLATOR CYCLE.

Bipolar Push-Pull Supply



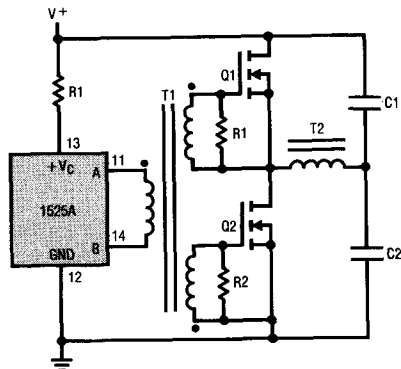
IN CONVENTIONAL PUSH-PULL BIPOLAR DESIGNS, FORWARD BASE DRIVE IS CONTROLLED BY R1-R3. RAPID TURN-OFF TIMES FOR THE POWER DEVICES ARE ACHIEVED WITH SPEED-UP CAPACITORS C1 AND C2.

Power FETs Push-Pull Supply



THE LOW SOURCE IMPEDANCE OF THE OUTPUT DRIVERS PROVIDES RAPID CHARGING OF POWER FET INPUT CAPACITANCE, WHILE MINIMIZING EXTERNAL COMPONENTS.

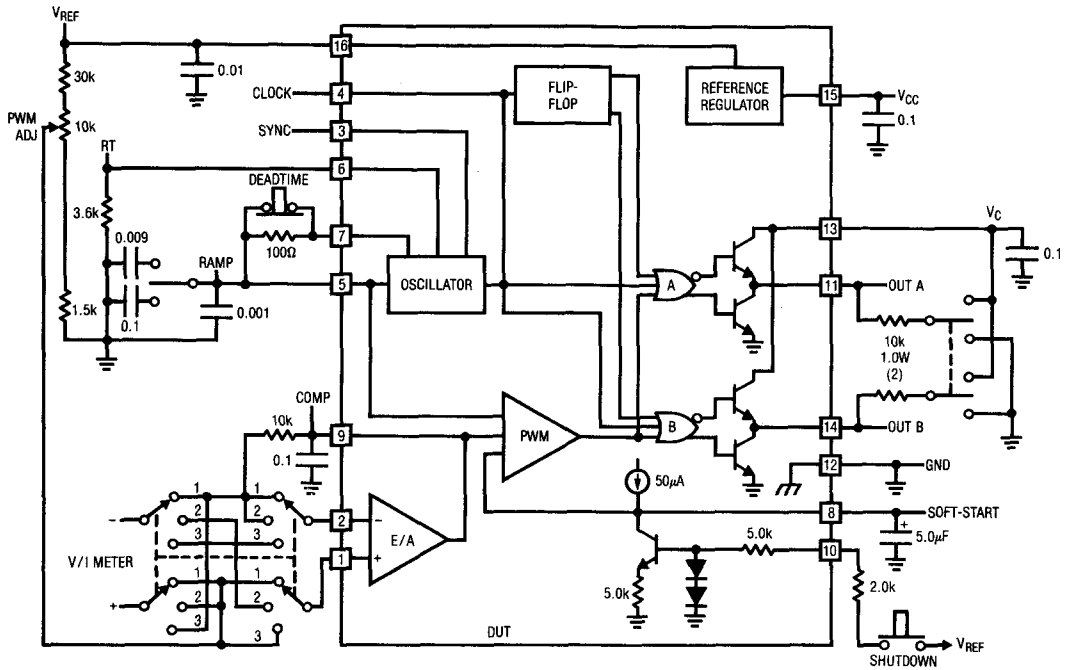
Driving Transformers Directly



LOW POWER TRANSFORMERS CAN BE DRIVEN DIRECTLY BY THE 1525A. AUTOMATIC RESET OCCURS DURING DEADTIME. WHEN BOTH ENDS OF THE PRIMARY WINDING ARE SWITCHED TO GROUND.

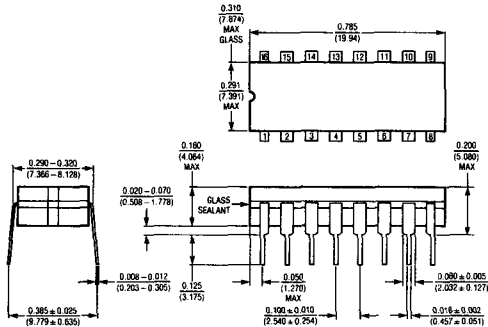
LT/SG1525A, LT/SG3525A
 LT/SG1527A, LT/SG3527A

TEST CIRCUIT



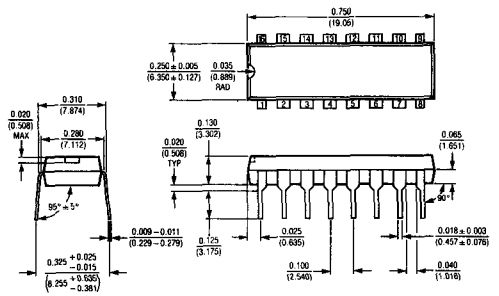
PACKAGE DESCRIPTION

16 Pin Cavity DIP (J)



	T _{jmax}	Θ _{JA}	Θ _{JC}
LT/SG1525AJ	150°C	100°C/W	60°C/W
LT/SG1527AJ	150°C	100°C/W	60°C/W
LT/SG3525AJ	150°C	100°C/W	60°C/W
LT/SG3527AJ	150°C	100°C/W	60°C/W

16 Pin Molded DIP (N)



	T _{jmax}	Θ _{JA}	Θ _{JC}
LT/SG3525AN	105°C	100°C/W	60°C/W
LT/SG3527AN	105°C	100°C/W	60°C/W

FEATURES

- 8V to 35V Operation
- *Guaranteed* $\pm 1\%$ 5V Reference
- *Guaranteed* 10mV/1000 Hrs. Long Term Stability
- *Guaranteed* $\pm 3\%$ Oscillator Temperature Stability
- Undervoltage Lockout
- 100mA Source/Sink Outputs

APPLICATIONS

- Switching Power Supplies
- Motor Speed Control
- Power Converters

DESCRIPTION

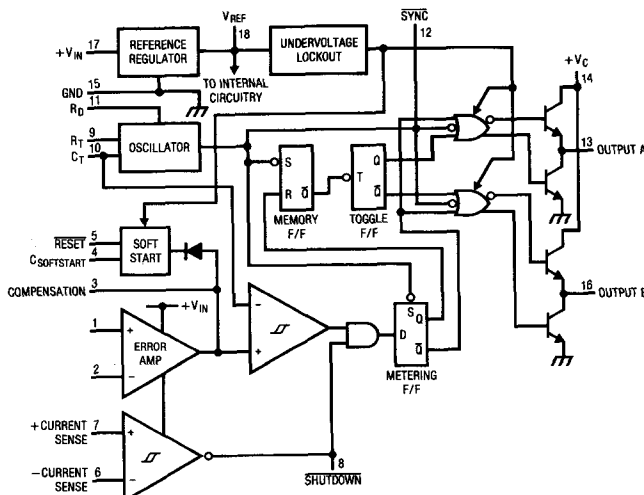
The LT1526 is an improved general purpose switching regulator control circuit. Included on the chip are a 1% voltage reference, oscillator, error amplifier, pulse width modulator and low impedance output drivers. Also included are protective features such as a current limit comparator, undervoltage lockout, soft-start circuitry, and adjustable deadtime. This versatile device can be used to implement single-ended or push-pull switching regulators of either polarity, both transformerless and transformer-coupled.

Although pin-for-pin and functionally compatible with industry standard 1526 and 3526 devices, Linear Technology has incorporated several improvements in the design of the LT1526. A subsurface zener has been used to provide excellent reference voltage stability and the reference offers improved line regulation and load regulation. The current limit comparator sense voltage initial accuracy and temperature stability have been greatly improved.

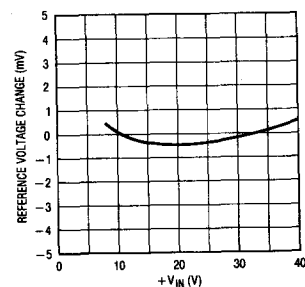
The combination of improved features and advanced linear processing for high reliability make Linear Technology's switching regulators a superior choice.

5

BLOCK DIAGRAM



Reference Line Regulation

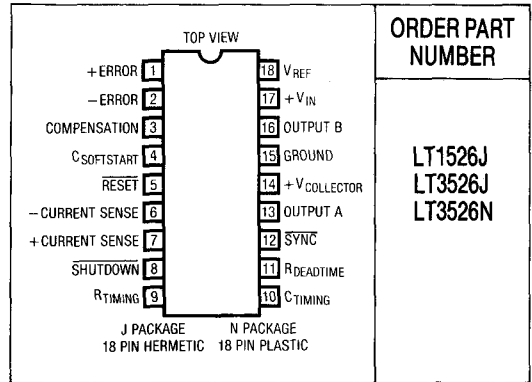


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Input Voltage (+ V _{IN})	+ 40V
Collector Supply Voltage (+ V _C)	+ 40V
Logic Inputs	- 0.3V to + 5.5V
Analog Inputs	- 0.3V to + V _{IN}
Source/Sink Load Current (each output)	200mA
Reference Load Current	50mA
Logic Sink Current	15mA
Operating Junction Temperature Range	
LT1526	- 55°C to + 150°C
LT3526	0°C to + 125°C
Storage Temperature Range	- 65°C to + 150°C
Lead Temperature (Soldering, 10sec)	+ 300°C

PACKAGE/ORDER INFORMATION



RECOMMENDED OPERATING CONDITIONS (Note 2)

Input Voltage	+ 8V to + 35V	Oscillator Frequency Range	1Hz to 400kHz
Collector Supply Voltage	+ 4.5V to + 35V	Oscillator Timing Resistor	2kΩ to 150kΩ
Sink/Source Load Current (each output)	0mA to 100mA	Oscillator Timing Capacitor	1nF to 20μF
Reference Load Current	- 5mA to 20mA	Available Deadtime Range at 40kHz	3% to 50%

ELECTRICAL CHARACTERISTICS

(+ V_{IN} = 15V, and over operating junction temperature, unless otherwise specified.)

PARAMETER	CONDITIONS	LT1526			LT3526			UNITS	
		MIN	TYP	MAX	MIN	TYP	MAX		
REFERENCE SECTION (Note 3)									
Output Voltage	T _J = + 25°C	4.95	5.00	5.05	4.90	5.00	5.10	V	
Line Regulation	+ V _{IN} = 8V to 35V	●	2	10	2	15		mV	
Load Regulation	I _L = - 5mA to + 20mA	●	5	10	5	20		mV	
Temperature Stability		●	15	50	15	50		mV	
Total Output Voltage Range	Over Recommended Operating Conditions	●	4.90	5.00	5.10	4.85	5.00	5.15	V
Short Circuit Current	V _{REF} = 0V	●	25	50	100	25	50	100	mA
Long Term Stability	T _J = 125°C		2	10	2	10		mV/√khr	
UNDERVOLTAGE LOCKOUT									
RESET Output Voltage	V _{REF} = 3.8V	●	0.2	0.4	0.2	0.4		V	
RESET Output Voltage	V _{REF} = 4.8V	●	2.4	4.8	2.4	4.8		V	
OSCILLATOR SECTION (Note 4)									
Initial Accuracy	T _J = + 25°C		± 3	± 8	± 3	± 8		%	
Voltage Stability	+ V _{IN} = 8V to 35V	●	0.5	1	0.5	1		%	
Temperature Stability		●	1	3	1	3		%	

ELECTRICAL CHARACTERISTICS

(+ V_{IN} = 15V, and over operating junction temperature, unless otherwise specified.)

PARAMETER	CONDITIONS	LT1526			LT3526			UNITS	
		MIN	TYP	MAX	MIN	TYP	MAX		
OSCILLATOR SECTION (Note 4)									
Minimum Frequency	R _T = 150kΩ, C _T = 20μF	●		1		1		Hz	
Maximum Frequency	R _T = 2kΩ, C _T = 1.0nF	●	400			400		kHz	
Sawtooth Peak Voltage	+ V _{IN} = 35V	●	3.0	3.5		3.0	3.5	V	
Sawtooth Valley Voltage	+ V _{IN} = 8V	●	0.5	1.0		0.5	1.0	V	
ERROR AMPLIFIER SECTION (Note 5)									
Input Offset Voltage	R _S ≤ 2kΩ	●	2	5		2	10	mV	
Input Bias Current		●	-350	-1000		-350	-2000	nA	
Input Offset Current		●	35	100		35	200	nA	
DC Open Loop Gain	R _L ≥ 10MΩ	●	64	72		60	72	dB	
High Output Voltage	V _{pin1} - V _{pin2} ≥ 150mV, I _{source} = 100μA	●	3.6	4.2		3.6	4.2	V	
Low Output Voltage	V _{pin2} - V _{pin1} ≥ 150mV, I _{sink} = 100μA	●		0.2	0.4		0.2	0.4	V
Common-Mode Rejection	R _S ≤ 2kΩ	●	70	94		70	94	dB	
Supply Voltage Rejection	+ V _{IN} = 12V to 18V	●	66	80		66	80	dB	
PWM COMPARATOR (Note 4)									
Minimum Duty Cycle	V _{compensation} = +0.4V	●		0			0	%	
Maximum Duty Cycle	V _{compensation} = +3.6V	●	45	49		45	49	%	
DIGITAL PORTS (SYNC, SHUTDOWN, and RESET)									
HIGH Output Voltage	I _{source} = 40μA	●	2.4	4.0		2.4	4.0	V	
LOW Output Voltage	I _{sink} = 3.6mA	●		0.2	0.4		0.2	0.4	V
HIGH Input Current	V _{IH} = +2.4V	●		-125	-200		-125	-200	μA
LOW Input Current	V _{IL} = +0.4V	●		-225	-360		-225	-360	μA
CURRENT LIMIT COMPARATOR (Note 6)									
Sense Voltage	R _S ≤ 50Ω	●	90	100	110	80	100	120	mV
Input Bias Current		●		-3	-10		-3	-10	μA
SOFT-START SECTION									
Error Clamp Voltage	RESET = +0.4V	●		0.1	0.4		0.1	0.4	V
C _S Charging Current	RESET = +2.4V	●	50	100	150	50	100	150	μA
OUTPUT DRIVERS (Each Output) (Note 7)									
HIGH Output Voltage	I _{source} = 20mA	●	12.5	13.5		12.5	13.5	V	
	I _{source} = 100mA	●	12	13		12	13	V	
LOW Output Voltage	I _{sink} = 20mA	●		0.2	0.3		0.2	0.3	V
	I _{sink} = 100mA	●		1.2	2.0		1.2	2.0	V
Collector Leakage	V _C = 40V	●		50	150		50	150	μA
Rise Time	C _L = 1000pF	●		0.3	0.6		0.3	0.6	μs
Fall Time	C _L = 1000pF	●		0.1	0.2		0.1	0.2	μs
POWER CONSUMPTION (Note 8)									
Standby Current	SHUTDOWN = +0.4V	●		18	30		18	30	mA

The ● denotes specifications that apply over the full operating temperature range.

The shaded electrical specifications indicate those parameters which have been improved or guaranteed test limits provided for the first time.

Note 1: Values beyond which damage may occur.

Note 2: Range over which the device is functional and parameter limits are guaranteed.

Note 3: I_L = 0mA.

Note 4: f_{OSC} = 40kHz (R_T = 4.12kΩ ± 1%, C_T = 0.01μF ± 1%, R_D = 0Ω).

Note 5: V_{CM} = 0V to +5.2V.

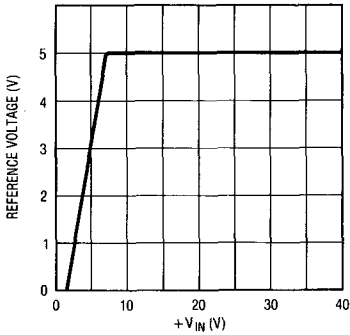
Note 6: V_{CM} = 0 to V_{IN} - 3V. The current limit sense voltage for the LT1526 is 80mV ≤ V_{SENSE} ≤ 120mV for temperatures less than 0°C or greater than 125°C.

Note 7: V_C = +15V.

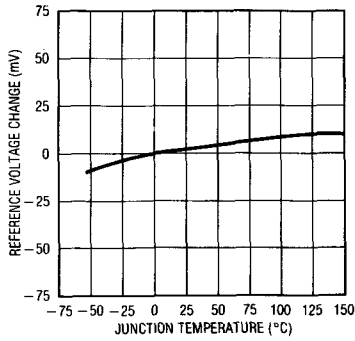
Note 8: + V_{IN} = +35V, R_T = 4.12kΩ.

TYPICAL PERFORMANCE CHARACTERISTICS

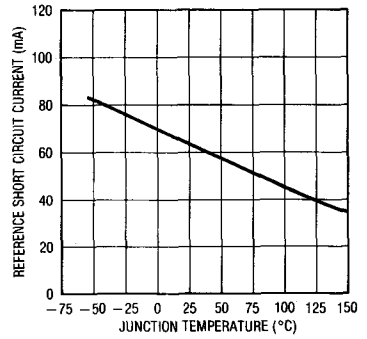
Reference Voltage vs Supply Voltage



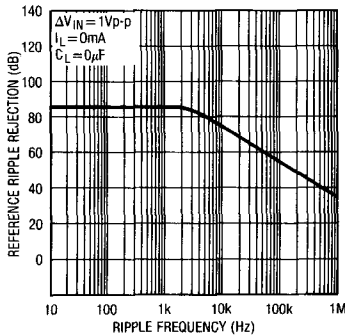
Reference Temperature Stability



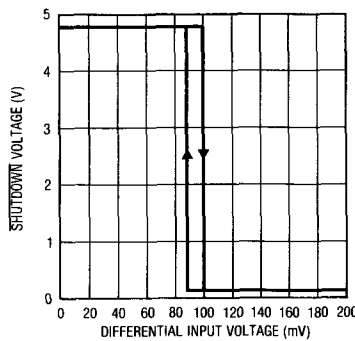
Reference Short Circuit Current



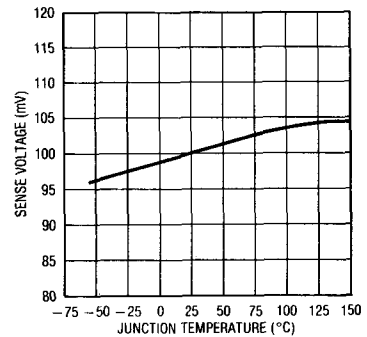
Reference Ripple Rejection



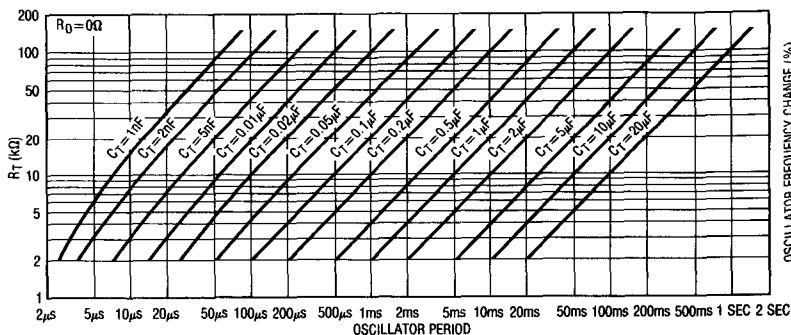
Current Limit Comparator Transfer Function



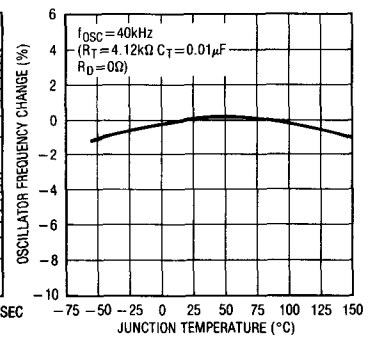
Current Limit Comparator Sense Voltage



Oscillator Period vs RT and CT

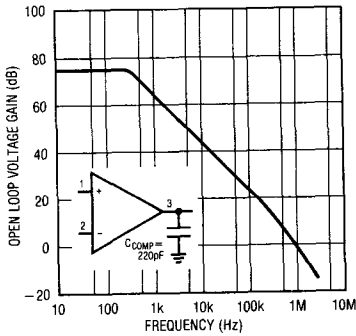


Oscillator Frequency Temperature Stability

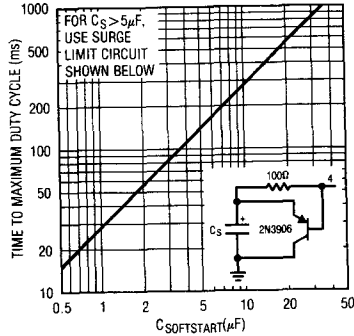


TYPICAL PERFORMANCE CHARACTERISTICS

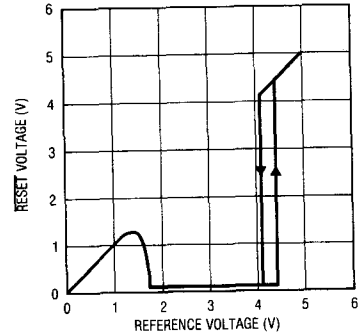
Error Amplifier Open Loop Gain vs Frequency



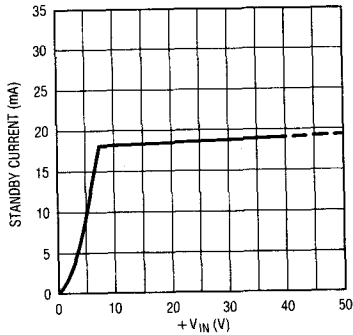
Soft-start Time Constant vs C_S



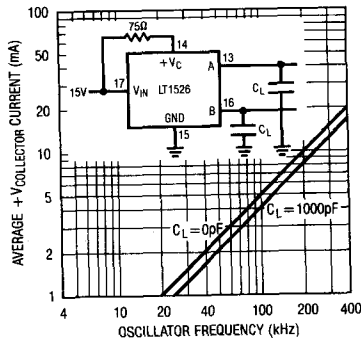
Undervoltage Lockout Characteristic



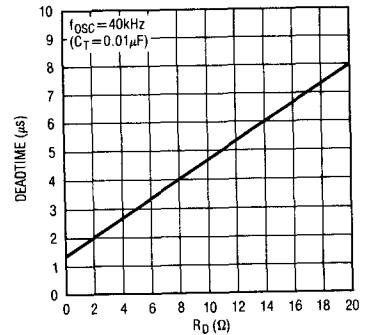
Standby Current vs Supply Voltage



+V_{COLLECTOR} Current (Note 9)

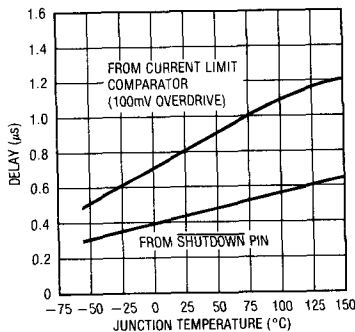


Output Driver Deadtime vs R_D

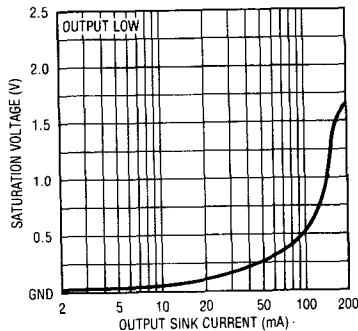


NOTE 9: TRANSIENT CURRENTS OCCUR WITHIN THE OUTPUT STAGES DURING SWITCHING, INDEPENDENT OF LOADING. THE GRAPH SHOWS THE AVERAGE (DC) VALUE OF THE TRANSIENT CURRENTS.

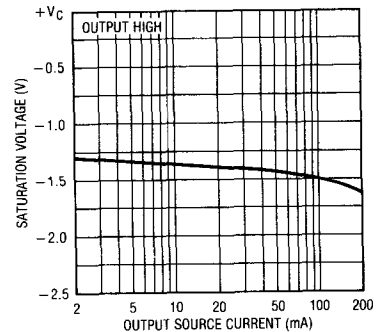
Output Driver Shutdown Delay



Output Driver Saturation Voltage vs I_{SINK}



Output Driver Saturation Voltage vs I_{SOURCE}



5

APPLICATIONS INFORMATION

FUNCTIONAL DESCRIPTION AND PIN FUNCTION

Voltage Reference

The reference regulator (pin 18) supplies a regulated 5.0V to all internal circuitry, as well as up to 20mA for external circuitry. It is fully active at supply voltages (pin 17) of 8V and greater.

The LT1526 can operate from a 5V supply by connecting $+V_{IN}$ to V_{REF} (pin 18 to pin 17) and maintaining the supply between 4.8V and 5.2V.

Undervoltage Lockout

The undervoltage lockout circuitry protects both the switching regulator and the power devices it controls from inadequate supply voltage, which can result in unstable control circuitry. If $+V_{IN}$ is too low, the circuit turns off the output drivers, holds \overline{RESET} (pin 5) low and the soft-start capacitor in a discharged state.

Soft-Start

The soft-start circuitry protects the power devices from high surge currents during power supply turn-on by limiting the available PWM duty cycle.

When $+V_{IN}$ reaches a sufficient voltage to allow \overline{RESET} to go high, a 100 μ A current source charges the external C_S capacitor (pin 4) linearly to 5V. The ERROR AMPLIFIER output is clamped to 600mV above the C_S voltage, and the available duty cycle of the PWM increases linearly. Maximum duty cycle is available when the C_S voltage reaches about 3V.

Digital Control Ports

The three digital control ports are bidirectional. Each port can drive TTL and 5V CMOS logic directly. They can also be driven by open-collector TTL, open-drain CMOS, and open-collector voltage comparators.

Driving \overline{SYNC} (pin 12) low causes a discharge cycle in the oscillator. Driving $\overline{SHUTDOWN}$ (pin 8) low causes the outputs to turn off. Driving \overline{RESET} (pin 5) low causes the outputs to turn off and discharges the C_S capacitor.

Oscillator

The internal oscillator circuitry sets the frequency of operation for the switching regulator. Frequency is set by R_T (pin 9), C_T (pin 10), and R_D (pin 11). With $R_D = 0\Omega$, the values for R_T and C_T may be chosen from the oscillator period graph. If the desired deadtime is increased, the value of R_T may need to be decreased to maintain the desired frequency.

The frequency at either output is half that of the oscillator, and the frequency at $+V_C$ (pin 14) is equal to the oscillator.

Synchronous Operation

Two or more switching regulators may be synchronized by setting the master to the desired frequency and sharing the oscillator signals with the slave units. Slave C_T pins are tied to the master C_T pin, and slave \overline{SYNC} pins are tied to the master \overline{SYNC} pin. Slave R_T and R_D pins are left open.

External logic synchronization can be used by setting the oscillator period to be 10% longer than the external clock period, and connecting the external clock to the \overline{SYNC} pin. A periodic low of about 0.5 μ s wide will lock the oscillator to the external frequency.

Error Amplifier

The differential input (pins 1 and 2), single-ended output (pin 3) transconductance amplifier provides about 70dB of gain. The output has an impedance of 2M Ω , and since all voltage gain occurs at the output, the gain characteristics can be controlled with shunt reactance to ground.

Output Drivers

The totem-pole output drivers can source and sink 100mA continuously and 200mA peak. The outputs are driven 180° out of phase by the flip-flop. Loads can be driven either from the outputs or the $+V_C$ pin. Since large transient currents occur within the output stages during switching, a resistor is recommended in series with $+V_C$ (pin 14) to limit the peak current. The resistor value should be $+V_C/200\text{mA}$.

APPLICATIONS INFORMATION

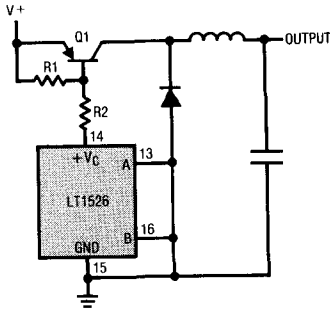
Current Limit

The current limit comparator turns off the outputs when the input voltage (pin 7 to pin 6) exceeds 100mV. Hysteresis

is built into the trip point, of about 10mV, to prevent oscillations.

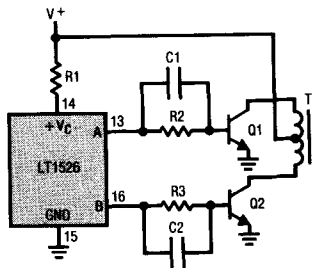
TYPICAL APPLICATIONS

Single Ended Supply



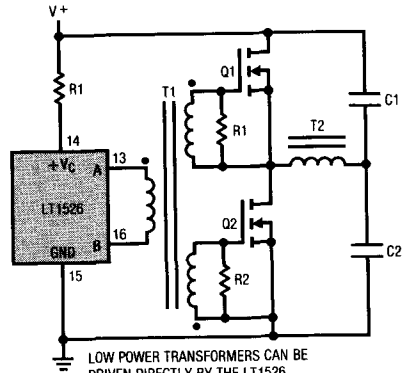
FOR SINGLE ENDED SUPPLIES, THE DRIVER OUTPUTS ARE GROUNDED. THE +V_C TERMINAL IS SWITCHED TO GROUND BY THE TOTEM POLE SOURCE TRANSISTORS ON EVERY OSCILLATOR CYCLE.

Bipolar Push-Pull Supply



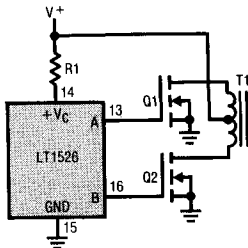
IN CONVENTIONAL BIPOLAR PUSH-PULL DESIGNS, FORWARD BASE DRIVE IS CONTROLLED BY R1-R3. RAPID TURN-OFF TIMES FOR THE POWER DEVICES ARE ACHIEVED WITH SPEED-UP CAPACITORS C1 AND C2.

Driving Transformers Directly



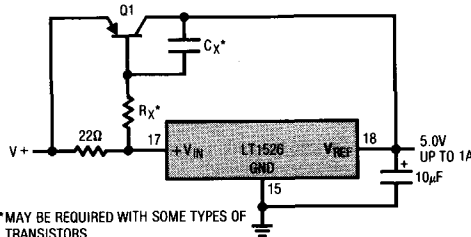
LOW POWER TRANSFORMERS CAN BE DRIVEN DIRECTLY BY THE LT1526. AUTOMATIC RESET OCCURS DURING DEAD-TIME, WHEN BOTH ENDS OF THE PRIMARY WINDING ARE SWITCHED TO GROUND.

Power FETs Push-Pull Supply



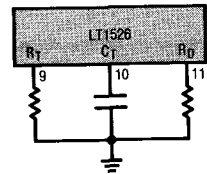
THE LOW SOURCE IMPEDANCE OF THE OUTPUT DRIVERS PROVIDES RAPID CHARGING OF POWER FET INPUT CAPACITANCE, WHILE MINIMIZING EXTERNAL COMPONENTS.

Extending Reference Output Current

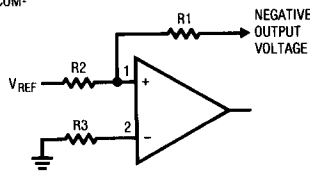


*MAY BE REQUIRED WITH SOME TYPES OF TRANSISTORS.

Oscillator Connections

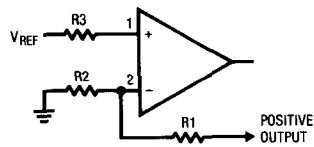


Error Amplifier Connections



$$V_{OUT} = V_{REF} \left(\frac{R1}{R2} \right)$$

$$R3 = \left(\frac{R1R2}{R1 + R2} \right)$$

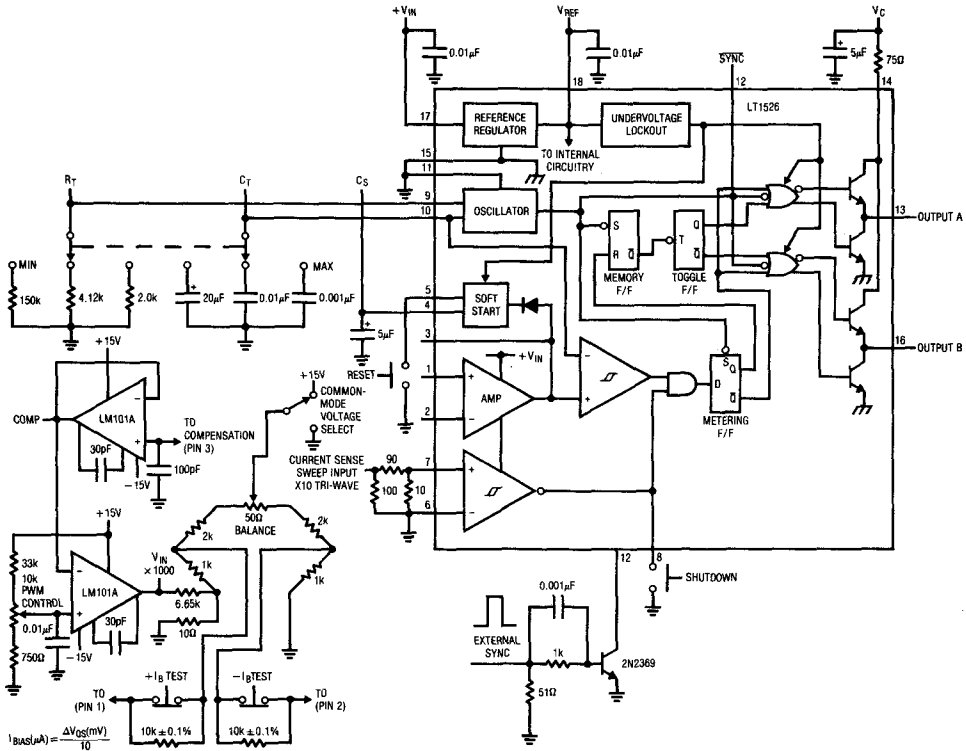


$$V_{OUT} = V_{REF} \left(\frac{R1 + R2}{R2} \right)$$

$$R3 = \left(\frac{R1R2}{R1 + R2} \right)$$

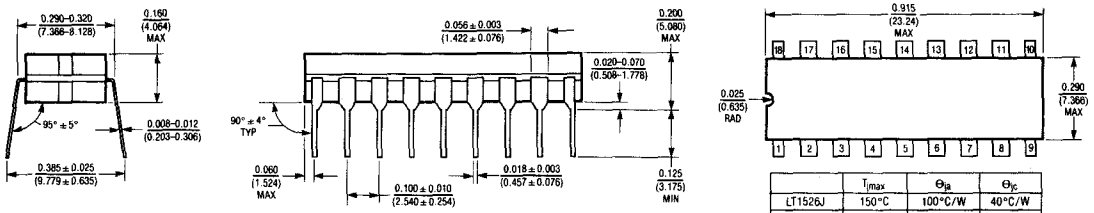
TYPICAL APPLICATIONS

LT1526 Lab Test Fixture

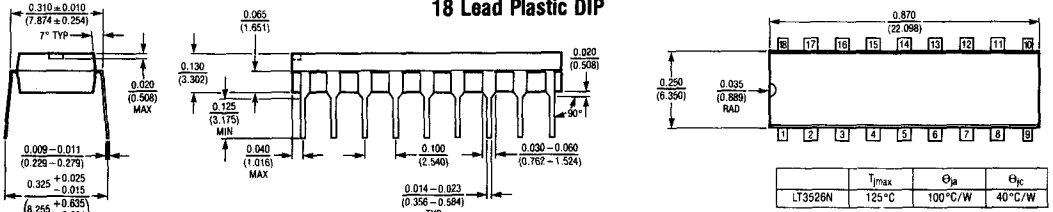


PACKAGE DESCRIPTION

J Package
18 Lead Ceramic DIP



N Package
18 Lead Plastic DIP



Current Mode PWM Controller

FEATURES

- Automatic Feed-Forward Compensation
- Programmable Pulse-by-Pulse Current Limiting
- $\pm 1\%$ Bandgap Reference
- Undervoltage Lockout
- External Shutdown
- Dual 200mA Totem Pole Outputs
- Double Pulse Suppression
- Soft-Start Capability
- Direct Replacement for UC1846, UC1847

APPLICATIONS

- Switching Power Supplies
- Motor Speed Control
- Power Converters

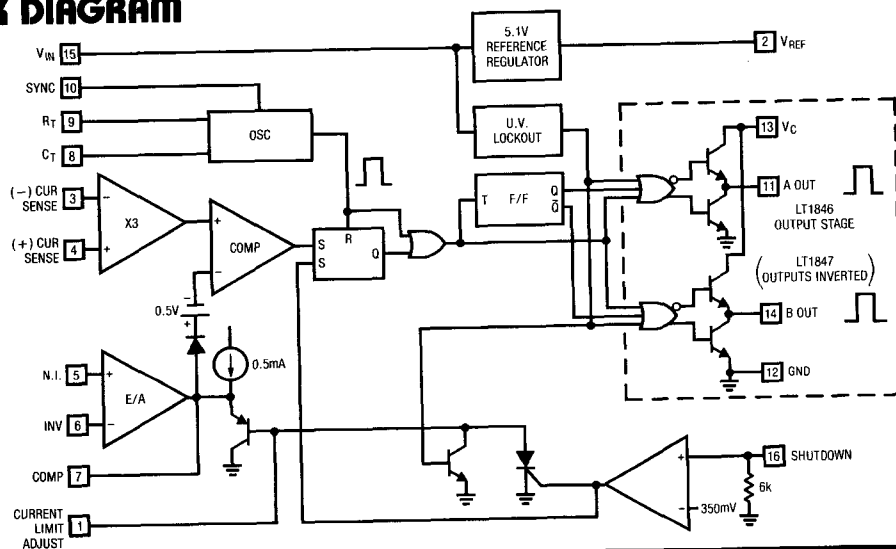
DESCRIPTION

The LT1846 family of control ICs contains all necessary circuitry to implement fixed frequency, fixed output voltage, current mode control schemes. Current mode control loops are easy to design and compensate, and provide superior transient line regulation, inherent pulse-by-pulse current limiting, and automatic symmetry correction for push-pull converters. In addition, the LT1846 has built-in undervoltage lockout with hysteresis to prevent oscillations near the threshold, soft-start capability, and can be shut down instantaneously by an external logic level. Internal logic prevents double-pulsing and output overlap.

The oscillator circuitry of the LT1846 allows the user to adjust output deadtime as well as frequency and also provides a bidirectional sync pin to allow paralleling power modules.

Both the internal error amplifier and current sense amplifiers operate over a wide common-mode range to allow design flexibility. The dual outputs provide active pull up/pull down, ideal for driving bipolar or FET switches. The internal reference regulator provides excellent stability for changes in line, load, and temperature. The LT1846 outputs are low in the off state while the LT1847 outputs are high in the off state.

BLOCK DIAGRAM



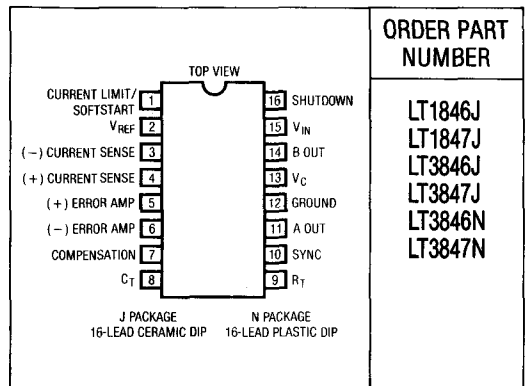
LT1846/1847, LT3846/3847

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage (Pin 15)	+ 40V
Collector Supply Voltage (Pin 13)	+ 40V
Output Current, Source or Sink (Pins 11, 14)	500mA
Analog Inputs (Pins 3, 4, 5, 6, 16)	- 0.3V to + V_{IN}
Reference Output Current (Pin 2)	- 30mA
Sync Output Current (Pin 10)	- 5mA
Error Amplifier Output Current (Pin 7)	- 5mA
Soft Start Sink Current (Pin 1)	50mA
Oscillator Charging Current (Pin 9)	5mA
Operating Temperature Range	
LT1846/1847	- 55°C to + 125°C
LT3846/3847	0°C to 70°C
Power Dissipation at $T_A = 25^\circ\text{C}$ (Note 2)	1000mW
Power Dissipation at $T_C = 25^\circ\text{C}$ (Note 3)	2000mW
Thermal Resistance, Junction to Ambient	100°C/W
Thermal Resistance, Junction to Case	60°C/W
Storage Temperature Range	- 65°C to + 150°C
Lead Temperature (Soldering, 10sec)	+ 300°C

PACKAGE/ORDER INFORMATION



ELECTRICAL CHARACTERISTICS (Note 4)

PARAMETER	CONDITIONS	LT1846/LT1847			LT3846/LT3847			UNITS	
		MIN	TYP	MAX	MIN	TYP	MAX		
Reference Voltage									
Output Voltage	$T_j = 25^\circ\text{C}, I_O = 1\text{mA}$	5.05	5.10	5.15	5.00	5.10	5.20	V	
Line Regulation	$V_{IN} = 8\text{V to } 40\text{V}$	●	5	20	5	20		mV	
Load Regulation	$I_L = 1\text{mA to } 10\text{mA}$	●	3	15	3	15		mV	
Temperature Stability	Over Operating Range, (Note 5)	●	0.4		0.4			mV/°C	
Total Output Variation	Line, Load, and Temperature (Note 5)	●	5.00	5.20	4.95	5.25		V	
Output Noise Voltage	$10\text{Hz} \leq f \leq 10\text{kHz}, T_j = 25^\circ\text{C}$ (Note 5)		100		100			μV	
Long Term Stability	$T_j = 125^\circ\text{C}, 1000\text{Hrs.}$, (Note 5)		5		5			mV	
Short Circuit Output Current	$V_{REF} = 0\text{V}$	●	- 10	- 45	- 10	- 45		mA	
Oscillator Section									
Initial Accuracy	$T_j = 25^\circ\text{C}$		39	43	47	39	43	47	kHz
Voltage Accuracy	$V_{IN} = 8\text{V to } 40\text{V}$	●	- 1	± 2		- 1	± 2		%
Temperature Stability	Over Operating Range (Note 5)	●	- 1		- 1				%
Sync Output High Level		●	3.9	4.35	3.9	4.35		V	
Sync Output Low Level		●	2.3	2.5	2.3	2.5		V	
Sync Input High Level	Pin 8 = 0V	●	3.9	3.0	3.9	3.0		V	
Sync Input Low Level	Pin 8 = 0V	●	3.0	2.5	3.0	2.5		V	
Sync Input Current	Sync Voltage = 5.25V, Pin 8 = 0V	●	0.7	1.5	0.7	1.5		mA	
Error Amp Section									
Input Offset Voltage		●	0.5	5	0.5	10		mV	
Input Bias Current		●	- 0.6	- 1	- 0.6	- 2		μA	
Input Offset Current		●	40	250	40	250		nA	
Common-Mode Range	$V_{IN} = 8\text{V to } 40\text{V}$	●	0	$V_{IN} - 2\text{V}$	0	$V_{IN} - 2\text{V}$		V	

ELECTRICAL CHARACTERISTICS (Note 4)

PARAMETER	CONDITIONS	LT1846/LT1847			LT3846/LT3847			UNITS	
		MIN	TYP	MAX	MIN	TYP	MAX		
Error Amp Section (Cont.)									
Open Loop Voltage Gain	$\Delta V_O = 1.2V$ to $3V$	●	80	105		80	105	dB	
Unity Gain Bandwidth		●	0.7	1.0		0.7	1.0	MHz	
CMRR	$V_{CM} = 0V$ to $38V$, $V_{IN} = 40V$	●	75	100		75	100	dB	
PSRR	$V_{IN} = 8V$ to $40V$	●	80	105		80	105	dB	
Output Sink Current	$V_{ID} = -15mV$ to $-5V$, $V_{Pin7} = 1.2V$	●	2	6		2	6	mA	
Output Source Current	$V_{ID} = 15mV$ to $5V$, $V_{Pin7} = 2.5V$	●	-0.4	-0.5		-0.4	-0.5	mA	
High Level Output Voltage	R_L (Pin 7) = $15k\Omega$	●	4.3	4.6		4.3	4.6	V	
Low Level Output Voltage	R_L (Pin 7) = $15k\Omega$	●		0.7	1		0.7	1	V
Current Sense Amplifier Section									
Amplifier Gain	$V_{Pin3} = 0V$, Pin 1 Open (Notes 6 & 7)	●	2.5	2.8	3	2.5	2.8	3	V/V
Maximum Differential Input Signal ($V_{Pin4} - V_{Pin3}$)	Pin 1 Open (Note 6) R_L (Pin 7) = $15k\Omega$	●	1.1	1.2		1.1	1.2		V
Input Offset Voltage	$V_{Pin1} = 0.5V$ Pin 7 Open (Note 6)	●		5	25		5	25	mV
CMRR	$V_{CM} = 1V$ to $12V$	●	60	83		60	83	dB	
PSRR	$V_{IN} = 8V$ to $40V$	●	60	84		60	84	dB	
Input Bias Current	$V_{Pin1} = 0.5V$, Pin 7 Open (Note 6)	●		-2.5	-10		-2.5	-10	μA
Input Offset Current	$V_{Pin1} = 0.5V$, Pin 7 Open (Note 6)	●		0.08	1		0.08	1	μA
Input Common-Mode Range		●	0		$V_{IN} - 3$	0		$V_{IN} - 3$	V
Delay to Outputs	$T_j = 25^\circ C$, (Note 5)			200	500		200	500	ns
Current Limit Adjust Section									
Current Limit Offset	$V_{Pin3} = 0V$ $V_{Pin4} = 0V$, Pin 7 Open (Note 6)	●	0.45	0.5	0.55	0.45	0.5	0.55	V
Input Bias Current	$V_{Pin5} = V_{REF}$, $V_{Pin6} = 0V$	●		-10	-30		-10	-30	μA
Shutdown Terminal Section									
Threshold Voltage		●	250	350	400	250	350	400	mV
Input Voltage Range		●	0		V_{IN}	0		V_{IN}	V
Minimum Latching Current (I_{Pin1})	(Note 8)	●	3.0	1.5		3.0	1.5		mA
Maximum Non-Latching (I_{Pin1})	(Note 9)	●		1.5	0.8		1.5	0.8	mA
Delay to Outputs	(Note 5), $T_j = 25^\circ C$			300	600		300	600	ns
Output Section									
Collector-Emitter Voltage		●	40			40			V
Collector Leakage Current	$V_C = 40V$ (Note 10)	●			200			200	μA
Output Low Level	$I_{SINK} = 20mA$	●		0.1	0.4		0.1	0.4	V
	$I_{SINK} = 100mA$	●		0.4	2.1		0.4	2.1	V
Output High Level	$I_{SOURCE} = 20mA$	●	13	13.5		13	13.5		V
	$I_{SOURCE} = 100mA$	●	12	13.5		12	13.5		V
Rise Time	(Note 5), $C_L = 1nF$, $T_j = 25^\circ C$			50	300		50	300	ns
Fall Time	(Note 5), $C_L = 1nF$, $T_j = 25^\circ C$			50	300		50	300	ns
Undervoltage Lockout Section									
Start-Up Threshold		●		7.7	8.0		7.7	8.0	V
Threshold Hysteresis		●		0.75			0.75		V
Total Standby Current									
Supply Current	(Note 11)	●		17	21		17	21	mA

LT1846/1847, LT3846/3847

The ● denotes the specifications that apply over the full operating temperature range.

Note 1: All voltages are with respect to Ground, pin 12. Currents are positive into, negative out of the specified terminal.

Note 2: Derate at 10mW/°C for T_A above 50°C.

Note 3: Derate at 16mW/°C for T_C above 25°C.

Note 4: Unless otherwise stated $V_{IN} = 15V$, $R_T = 10k$, $C_T = 4.7nF$.

Note 5: These parameters, although guaranteed over the recommended operating conditions are not 100% tested in production.

Note 6: Parameter measured at trip point of latch with $V_{Pin5} = V_{REF}$, $V_{Pin6} = 0V$.

Note 7: Amplifier gain defined as

$$G = \frac{\Delta V_{Pin7}}{\Delta V_{Pin4}}; \Delta V_{Pin4} = 0V \text{ to } 1.0V$$

Note 8: Current into pin 1 guaranteed to latch circuit in shutdown state.

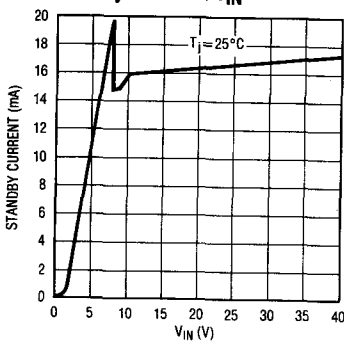
Note 9: Current into pin 1 guaranteed not to latch circuit in shutdown state.

Note 10: Applies to LT1846/3846 only due to polarity of outputs.

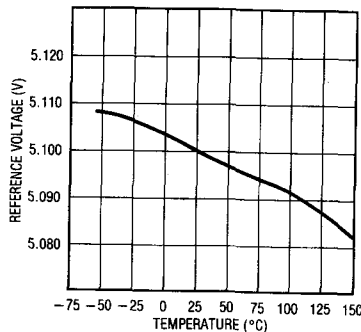
Note 11: Standby current does not include oscillator charging current, error and current limit dividers, and the outputs are open circuit.

TYPICAL PERFORMANCE CHARACTERISTICS

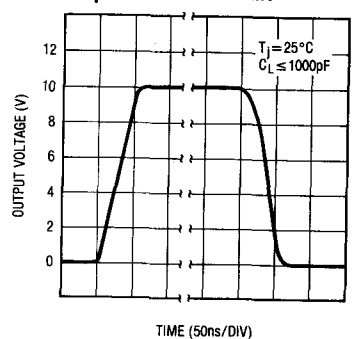
Standby Current vs V_{IN}



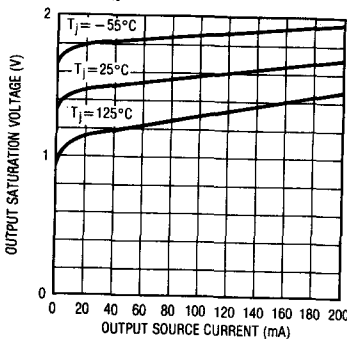
Reference Voltage vs Temperature



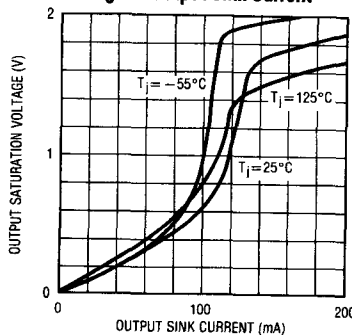
Output Rise and Fall Time



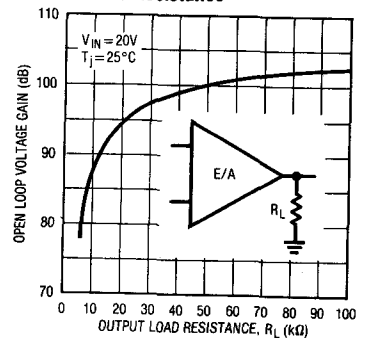
Output High Level Saturation Voltage vs Output Source Current



Output Low Level Saturation Voltage vs Output Sink Current

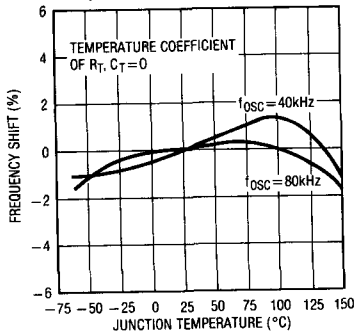


Error Amp Open-Loop DC Gain vs Load Resistance

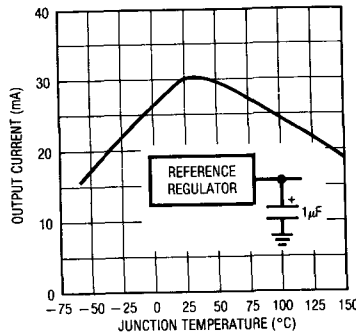


TYPICAL PERFORMANCE CHARACTERISTICS

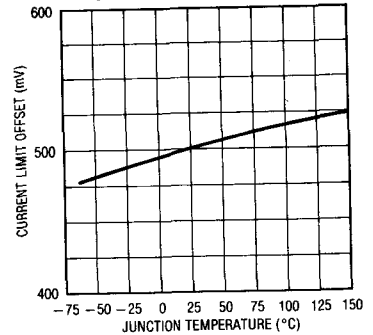
Oscillator Frequency vs Temperature



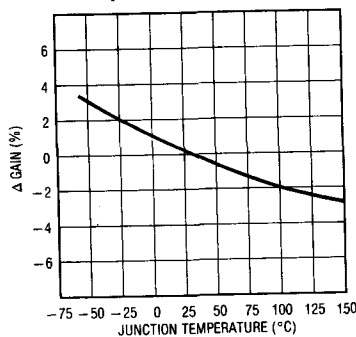
Reference Current Limit



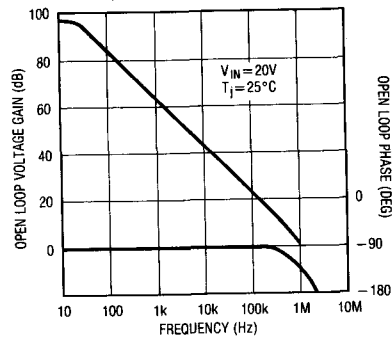
Current Limit Offset vs Temperature



Current Sense Amplifier Gain vs Temperature



Error Amplifier Gain and Phase vs Frequency



APPLICATIONS INFORMATION

Current Mode Control

Current mode controllers directly control peak inductor current with the error signal rather than controlling the duty cycle of the PWM as conventional controllers do. There are several inherent advantages in this type of control.

Current mode controllers are easier to frequency compensate. Peak inductor current is forced to follow the error signal and can change only if the error signal changes. This forces the inductor to act like a constant current source at mid frequencies and the order of the system can be reduced by one, eliminating 90° of phase shift.

Peak current on a pulse-by-pulse basis can be limited by simply limiting the positive swing of the error amplifier.

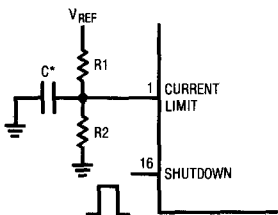
Transient line regulation is greatly improved. A change in the line voltage causes a change in the slope of the inductor current. This means that the time it takes for the inductor current to reach the peak control value automatically changes, and requires very little change in the output of the error amp. Since transient response is limited by the integrator response of the error amplifier, excellent line transient response is obtained if the error amplifier output does not have to change.

APPLICATIONS INFORMATION

With current mode control, some amount of slope compensation is required to prevent oscillations for duty cycles greater than 50%. Slope compensation can also be used to decrease noise sensitivity for low values of inductor current ripple, and to prevent subharmonic oscillations in the inductor current.

Shutdown/Soft Start

A logic high at pin 16 will initiate a shutdown cycle. During a shutdown cycle, both outputs are held off and pins 1 and 7 are pulled low. If pin 1 current ($I_{P1} = V_{REF}/R_1$) is less than the latch threshold current, typically 1.5mA (see Electrical Characteristics), the device will restart at the end of the shutdown pulse. If pin 1 current is greater than the latch threshold current, the device will latch off until power is recycled.

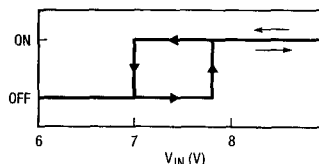


Soft start is accomplished by the addition of a capacitor from pin 1 to ground. This forces the peak value of the switch current to come up slowly. Pin 16 can be left floating if the shutdown function is not used.

Undervoltage Lockout

The purpose of the undervoltage lockout is to prevent the device from switching until the internal circuitry is operating properly. Built-in hysteresis prevents the circuit from oscillating at the threshold point. Pin 1 (current limit adjust) and pin 7 (comp) are held low during undervoltage lockout, and outputs are low (LT1846) or high (LT1847).

Output Switches



Oscillator Section

The frequency of the oscillator is set by an external resistor (R_T) from pin 9 to ground, and an external capacitor (C_T) from pin 8 to ground. C_T is charged by a constant current $I_{RT} = V_{P9} / R_T$ ($\approx 3.6V/R_T$), and is discharged by a constant current $8mA - I_{RT}$. Upper and lower trip levels are determined by the internal circuitry, such that the oscillator frequency is approximated by the formula

$$f_T \approx \frac{2.2}{R_T(\Omega)C_T(F)}$$

In addition, output deadtime, which is equal to the capacitor discharge time, is a function of the size of C_T and can be calculated according to the formula:

$$T_d \approx 220C_T \left(\frac{8mA}{8mA - \frac{3.6V}{R_T}} \right)$$

For large values of R_T (small I_{RT}): $T_d \approx 220C_T$.

Note that these formulas are approximations based on a 1.75V swing at the C_T pin, and a discharge current of 8mA. Variations in the value of the discharge current will obviously cause the deadtime to vary. For very short deadtimes, fixed internal delays of approximately 100ns must also be added to the calculated value. Capacitor values less than 1000pF or deadtimes of less than 300ns are not recommended. This is due to the fact that at extreme cold temperatures the oscillator deadtime may become shorter than the time required to reset the current sense latch.

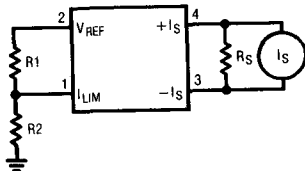
APPLICATIONS INFORMATION

Current Limit

Peak switch current on a pulse-by-pulse basis is a function of the voltage level set at pin 1 and the current sense resistor R_S , and can be determined by the formula:

$$I_S = \frac{R_2 V_{REF} - 0.5V}{R_1 + R_2} \quad G = I/A \text{ GAIN} = 2.75 \text{ TYP}$$

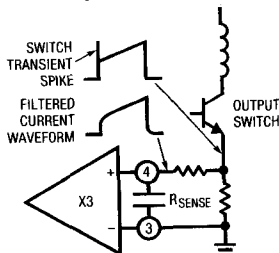
$$G \cdot R_S$$



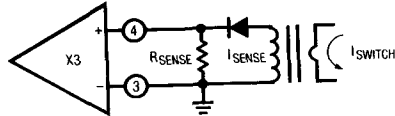
Current Sensing

The current sense amplifier is a differential amplifier with a gain of 3 and a common-mode range of 0 to $V_{IN} - 3V$. Maximum differential input signal is 1.2V. Several sensing schemes are possible. Direct resistive sensing is the simplest, but power losses in the resistor may not be acceptable. The use of a current sense transformer will increase efficiency for higher current levels, but will increase circuit complexity. In configurations where switch current is sensed, a small RC may be necessary to keep switch turn on transients from tripping the current sense latch. Without this filter, erratic operation will result especially at lower values of output current. Minimum on-time of the output switch during a short circuit is equal to the delay from the current sense amplifier to the output, typically 200ns. This delay will be longer if a filter for switch transients is added. For best noise immunity, the signal at the current sense amplifier inputs should be as large as possible.

Resistive Sensing of Switch Current with RC Filter



Transformer Sensing Gives Isolation and Improved Efficiency



Error Amplifier

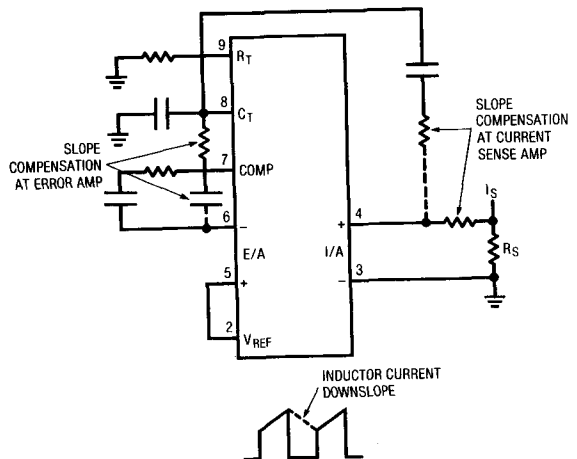
The error amplifier of the LT1846 can operate over a common-mode range of 0 to $V_{IN} - 2V$. The output stage consists of an NPN Darlington pull-down and a 0.5mA current source pull-up. See Typical Performance Characteristics for gain and phase characteristics.

Reference Regulator

The reference regulator provides a fixed 5.1V for internal circuitry as well as up to 20mA of output current for external circuitry such as the current limit divider. A small bypass capacitor (0.1-1.0 μ F) from the reference pin (pin 2) to the ground pin (pin 12) is recommended. This capacitor should be located as close as possible to the device.

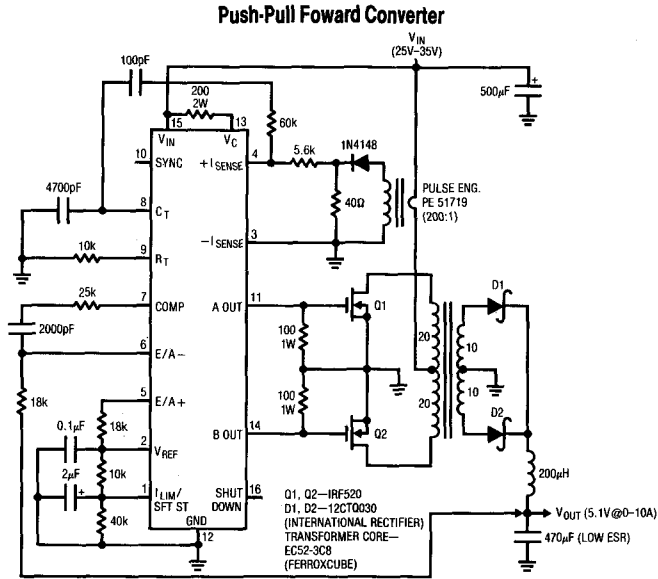
Slope Compensation

Slope compensation can be accomplished by summing a triangle wave derived from the oscillator waveform, with the inductor current waveform at the current sense amplifier input or the summing node of the error amplifier as shown below. Slope compensation should be greater than 1/2 of the downslope of the inductor current waveform.



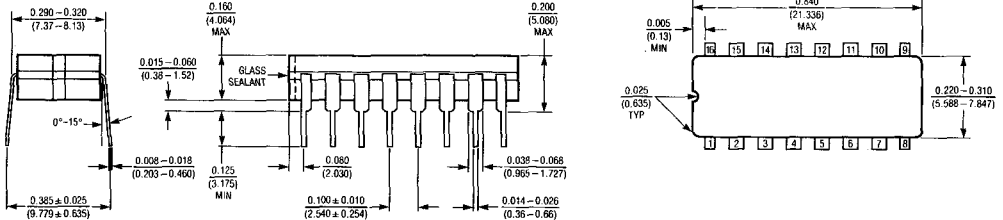
LT1846/1847, LT3846/3847

TYPICAL APPLICATIONS CIRCUIT



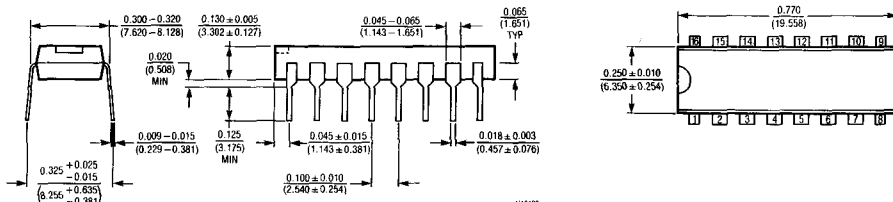
PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

J Package 16-Lead Ceramic DIP



	T_{jmax}	θ_{JA}	θ_{JC}
LT1846	150°C	100°C/W	60°C/W
LT1847			
LT3846	105°C	100°C/W	60°C/W
LT3847			

N Package 16-Lead Plastic DIP



SECTION 6—COMPARATORS

6

SECTION 6—COMPARATORS

INDEX	6-2
SELECTION GUIDE	6-3
PROPRIETARY PRODUCTS	
<i>LT685, High Speed Comparator</i>	6-5
<i>LT1011, Voltage Comparator</i>	6-9
<i>LT1015, High Speed Dual Line Receiver</i>	13-6
<i>LT1016, Ultra Fast Precision Comparator</i>	6-25
<i>LT1016CS8, Ultra Fast Precision Comparator</i>	6-41
<i>LT1017, Micropower Dual Comparator</i>	6-45
<i>LT1018, Micropower Dual Comparator</i>	6-45
<i>LT1017CS/LT1018CS, Micropower Dual Comparator</i>	6-53
<i>LTC1040, Dual Micropower Comparator</i>	6-57
<i>LTC1041, BANG-BANG Controller</i>	6-69
<i>LTC1042, Window Comparator</i>	6-77
ENHANCED AND SECOND SOURCE PRODUCTS	
<i>LM111/LM311, Voltage Comparator</i>	6-85
<i>LT111A/LT311A, Improved LM111</i>	6-85
<i>LM119/LM319, Dual Comparator</i>	6-93
<i>LT119A/LT319A, Improved LM119</i>	6-93

MILITARY

PART NUMBER	RESPONSE TIME MAX (ns)	V _{OS} MAX (mV)	I _B MAX (nA)	DRIVE CAPABILITY (mA)	GAIN MIN (V/mV)	I _{SUPPLY} POSITIVE (mA)	I _{SUPPLY} NEGATIVE (mA)	PACKAGES AVAILABLE	IMPORTANT FEATURES
LT1011AM	250	0.5	25	50	200	4.0	2.5	H, J8	Low V _{OS} , Low I _B , High Output Drive, 12 Bit Acc.
LT1011M	250	1.5	50	50	200	4.0	2.5	H, J8	
LT1016M	12	± 2.5	10000	10	2	35	5	H, J8	Ultra High Speed, TTL Outputs, True Output Latch, Stable in Active Region, Pin/Pin Replacement for AM686.
LT1017M	—	1	15	30	1000	0.060	—	H, J8	LT1017 Has Lowest Supply Current, LT1018 is Faster. Both are Dual Comparators with Same Pin-Out as 193 Types.
LT1018M	—	1	75	35	1000	0.250	—	H, J8	
LT111A	250	1.0	100	50	200	4.0	2.5	H, J8	Low V _{OS} , High Gain
LM111	—	3.0	100	50	40	6.0	5.0	H, J8	General Purpose
LT119A	80 (typ)	1.0	500	25	20	11.5	4.5	H, J	Dual, Low V _{OS} , Hi CMRR
LM119	80 (typ)	4.0	500	25	10	11.5	4.5	H, J	Dual, General Purpose
LTC1040M	100µs	0.5	3	*	†	300nA**	1nA	J	CMOS Sampling Comparator
LTC1041M	100µs	0.5	0.3	10	—	3	—	J8, N8	CMOS Bang-Bang Controller
LTC1042M	100µs	1.0	3	*	†	300nA**	1nA	J8	CMOS Window Comparator
LT685M	6.5	± 2.0	10000	††	1.6 typ	22	—	H, J	Ultra High Speed, ECL Outputs, Output Latch, External Hysteresis Control

COMMERCIAL

PART NUMBER	RESPONSE TIME MAX (ns)	V _{OS} MAX (mV)	I _B MAX (nA)	DRIVE CAPABILITY (mA)	GAIN MIN (V/mV)	I _{SUPPLY} POSITIVE (mA)	I _{SUPPLY} NEGATIVE (mA)	PACKAGES AVAILABLE	IMPORTANT FEATURES
LT1011AC	250	0.5	25	50	200	4.0	2.5	H, J8, N8	Low V _{OS} , Low I _B , High Output Drive, 12 Bit Acc.
LT1011C	250	1.5	50	50	200	4.0	2.5	H, J8, N8	
LT1016C	12	± 2.5	10000	10	2	35	5	H, J8, S8	Ultra High Speed, TTL Outputs, True Output Latch, Stable in Active Region, Pin/Pin Replacement for AM686.
LT1017C	—	1	15	30	1000	0.060	—	H, S	LT1017 Has Lowest Supply Current, LT1018 is Faster. Both are Dual Comparators with Same Pin-Out as 193 Types.
LT1018C	—	1	75	35	1000	0.250	—	H, S	
LT311A	250	1.0	100	50	200	4.0	2.5	H, J8	Low V _{OS} , High Gain
LM311	—	7.5	250	50	40	7.5	5.0	H, J8	General Purpose
LT319A	80 (typ)	1.0	500	25	20	12.5	5.0	H, J, N	Dual, Low V _{OS} , Hi CMRR
LM319	80 (typ)	8.0	1000	25	8	12.5	5.0	H, J, N	Dual, General Purpose
LTC1040C	100µs	0.5	3	*	†	300nA**	1nA	J, N, S	CMOS Sampling Comparator
LTC1041C	100µs	0.5	0.3	10	—	3	—	J8, N8	CMOS Bang-Bang Controller
LTC1042C	100µs	1.0	3	*	†	300nA**	1nA	J, N8	CMOS Window Comparator
LT685C	6.5	± 2.0	10000	††	1.6 typ	22	26	H, J, N	Ultra High Speed, ECL Outputs, Output Latch, External Hysteresis Control

* 1 Std. TTL Load.

** Supply Current Depends on Clock Rate.

 † Gain errors are included in V_{OS} spec.

†† Can drive terminated 500 transmission lines.

REFER TO TABLE OF CONTENTS FOR REVISED DATA LOCATION

NOTES

FEATURES

- Ultra Fast (5.5ns typ)
- Complementary ECL Output
- 50Ω Line Driving Capability
- Low Offset Voltage
- Output Latch Capability
- External Hysteresis Control
- Pin Compatible with Am685

APPLICATIONS

- High Speed A to D Converters
- High Speed Sampling Circuits
- Oscillators

DESCRIPTION

The LT685 is an ultra-fast comparator with differential inputs and complementary outputs fully compatible with ECL logic levels. The output current capability is adequate for driving transmission lines terminated in 50Ω. The low input offset and high resolution make this comparator ideally suited for analog-to-digital signal processing applications.

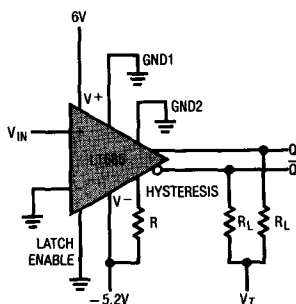
A latch function is provided to allow the comparator to be used in a sample-hold mode. When the latch enable input is ECL high, the comparator functions normally. When the latch enable is driven low, the comparator outputs are locked in their existing logical states. If the latch function is not used, the latch enable must be connected to ground or ECL high.

The device is pin-compatible with the Am685. Hysteresis has been added to improve switching time with slow input signals as well as to minimize oscillation. A single resistor between the hysteresis pin and V⁻ adds input hysteresis voltage as more current is drawn. If hysteresis is not required, the pin can be left unconnected.

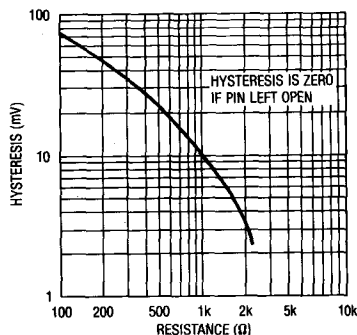
6

TYPICAL APPLICATION

Comparator with Hysteresis



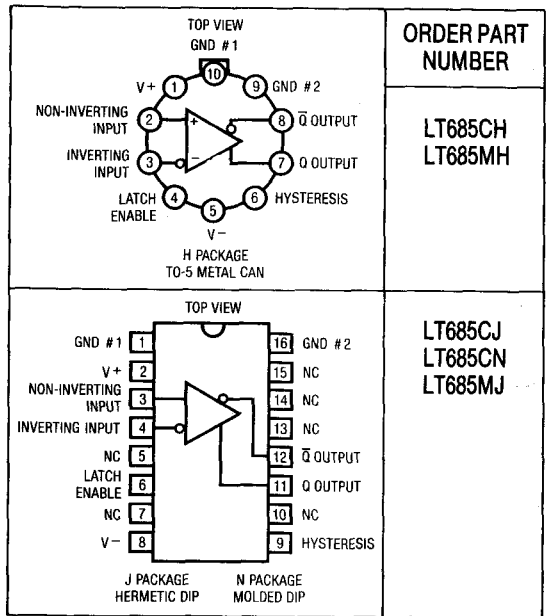
Hysteresis



ABSOLUTE MAXIMUM RATINGS

Positive Supply Voltage	7V
Negative Supply Voltage	-7V
Input Voltage	±4V
Differential Input Voltage	±6V
Latch Pin Voltage	2V to V-
Hysteresis Pin Voltage.....	0V to V-
Output Current.....	30mA
Power Dissipation (Note 1)	500mW
Operating Temperature	
LT685C.....	-30°C ≤ T _A ≤ 85°C
LT685M	-55°C ≤ T _A ≤ 125°C

PACKAGE/ORDER INFORMATION



ORDER PART NUMBER

LT685CH
LT685MH

LT685CJ
LT685CN
LT685MJ

ELECTRICAL CHARACTERISTICS

V₊ = 6.0V, V₋ = -5.2V, V_T = -2.0V, R_L = 50Ω, R = ∞ over the operating temperature ranges, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	LT685C			LT685M			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V _{OS}	Input Offset Voltage	T _A = 25°C	1.0	±2.0	±2.5	1.0	±2.0	±3.0	mV
dV _{OS} /dT	Input Offset Voltage Drift	(Note 2)		±10			±10		μV/°C
I _{OS}	Input Offset Current	T _A = 25°C	0.3	±1.0	±1.3	0.3	±1.0	±1.6	μA
I _B	Input Bias Current	T _A = 25°C	5	10	13	5	10	16	μA
R _{IN}	Input Resistance	T _A = 25°C (Note 2)	6.0			6.0			kΩ
C _{IN}	Input Capacitance	T _A = 25°C (Note 2)		3.0			3.0		pF
V _{CM}	Input Voltage Range			±3.3			±3.3		V
CMRR	Common-Mode Rejection		80			80			dB
SVRR	Supply Voltage Rejection		70			70			dB
V _{OH}	Output High Voltage	T _A = 25°C T _A = T _{MIN} T _A = T _{MAX}	-0.960 -1.060 -0.890	-0.810 -0.890 -0.700		-0.960 -1.100 -0.850	-0.810 -0.920 -0.620		V
V _{OL}	Output Low Voltage	T _A = 25°C T _A = T _{MIN} T _A = T _{MAX}	-1.850 -1.890 -1.825	-1.650 -1.675 -1.625		-1.850 -1.910 -1.810	-1.650 -1.690 -1.575		V
I ₊	Positive Supply Current			22			22		mA
I ₋	Negative Supply Current			26			26		mA
P _{DISS}	Power Dissipation			300			300		mW

SWITCHING CHARACTERISTICS ($V_{IN} = 100mV$ step, 5mV overdrive)

SYMBOL	PARAMETER	CONDITIONS	LT685C			LT685M			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PD}	Propagation Delay (Note 3)	$T_A = 25^\circ C$	4.5	5.5	6.5	4.5	5.5	6.5	ns
		$T_A = T_{MAX}$	5.0		9.5	5.5		12	ns
		$T_A = T_{MIN}$	4.0		6.5	3.5		6.5	ns
$t_{PD(E)}$	Latch Enable to Output Delay (Note 2)	$T_A = 25^\circ C$	4.5	5.5	6.5	4.5	5.5	6.5	ns
		$T_A = T_{MAX}$	5.0		9.5	5.5		12	ns
		$T_A = T_{MIN}$	4.0		6.5	3.5		6.5	ns
t_S	Minimum Set-Up Time (Note 2)	$T_{MIN} \leq T_A \leq 25^\circ C$			3.0			3.0	ns
		$T_A = T_{MAX}$			4.0			6.0	ns
									1.0
t_H	Minimum Hold Time (Note 2)	$T_{MIN} \leq T_A \leq T_{MAX}$			1.0			1.0	ns
$t_{PW(E)}$	Minimum Latch Enable Pulse Width (Note 2)	$T_{MIN} \leq T_A \leq 25^\circ C$			3.0			3.0	ns
		$T_A = T_{MAX}$			4.0			5.0	ns

Note 1: For the metal can package, derate at 6.8mW/°C for operation at ambient temperatures above +100°C; for the hermetic dual-in-line package, derate at 9mW/°C for operation at ambient temperatures above +105°C.

Note 2: Guaranteed by design, but not tested.

Note 3: Sample tested at 25°C only.

Definitions:

t_{PD} : The propagation delay measured from the time the input signal crosses the input offset voltage to the 50% point of the output transition.

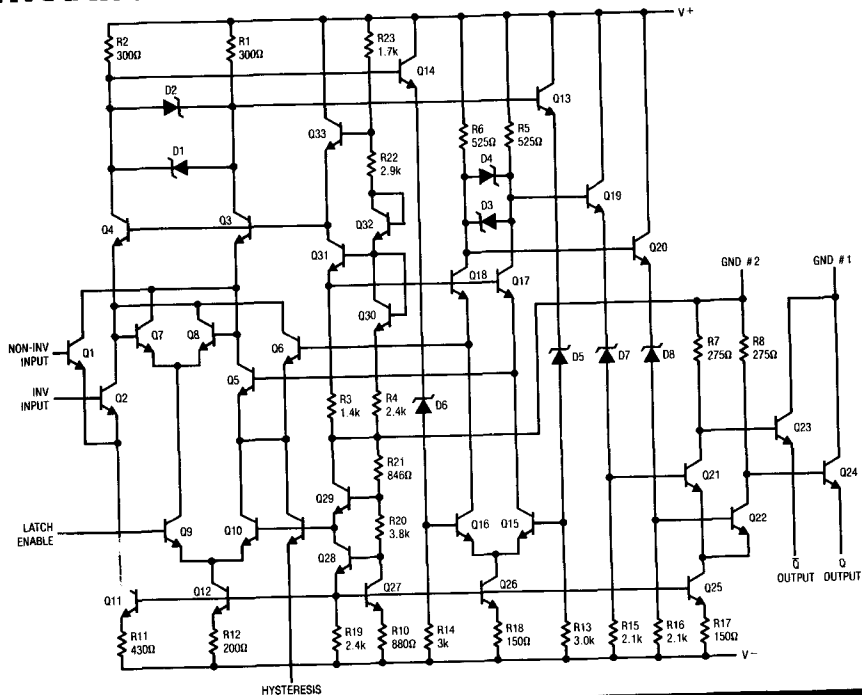
$t_{PD(E)}$: The propagation delay measured from the 50% point of the latch enable signal positive transition to the 50% point of the output transition.

t_S : The minimum time before the negative transition of the latch enable signal that an input signal change must be present in order to be acquired and held at the outputs.

t_H : The minimum time after the negative transition of the latch enable signal that the input signal must remain unchanged in order to be acquired and held at the outputs.

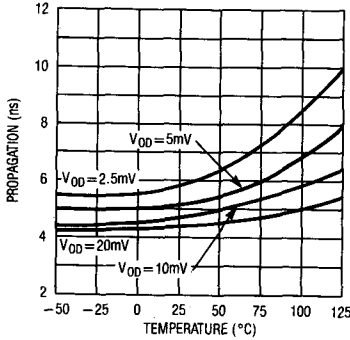
$t_{PW(E)}$: The minimum time that the latch enable signal must be HIGH in order to acquire and hold an input signal change.

SCHEMATIC DIAGRAM

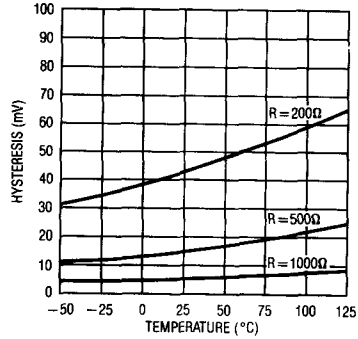


TYPICAL PERFORMANCE CHARACTERISTICS

Propagation Delays as a Function of Temperature

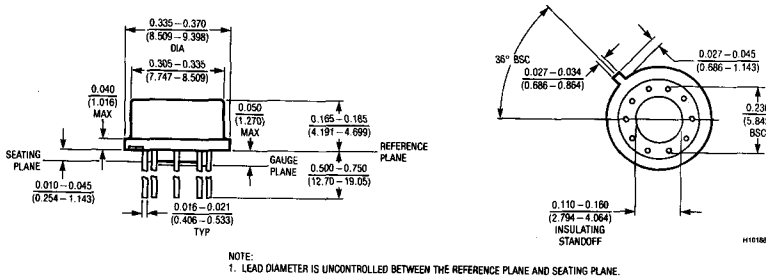


Hysteresis as a Function of Temperature

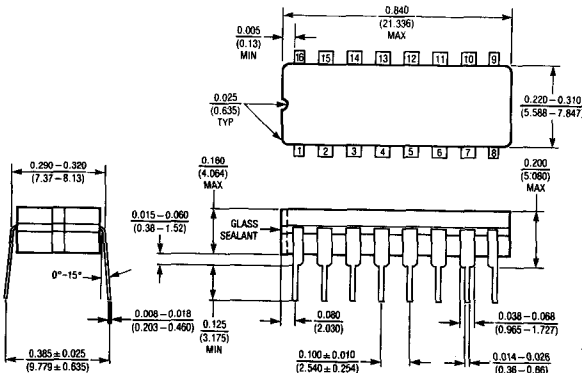


PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

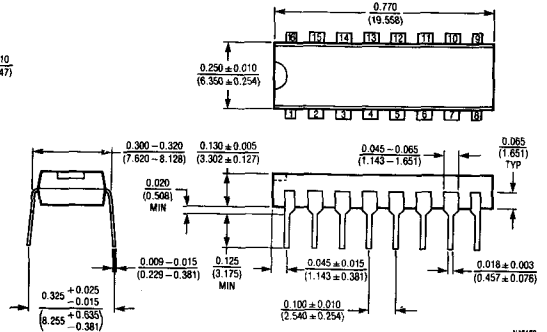
H Package
10 Lead TO-5 Metal Can



J Package
16 Lead Cerdip



N Package
16 Lead Molded DIP



FEATURES

- Pin-Compatible with LM111 Series Devices
- *Guaranteed Max.* 0.5mV Input Offset Voltage
- *Guaranteed Max.* 25nA Input Bias Current
- *Guaranteed Max.* 3nA Input Offset Current
- *Guaranteed Max.* 250ns Response Time
- *Guaranteed Min.* 200,000 Voltage Gain
- 50mA Output Current Source or Sink
- $\pm 30V$ Differential Input Voltage
- Fully Specified for Single +5V Operation

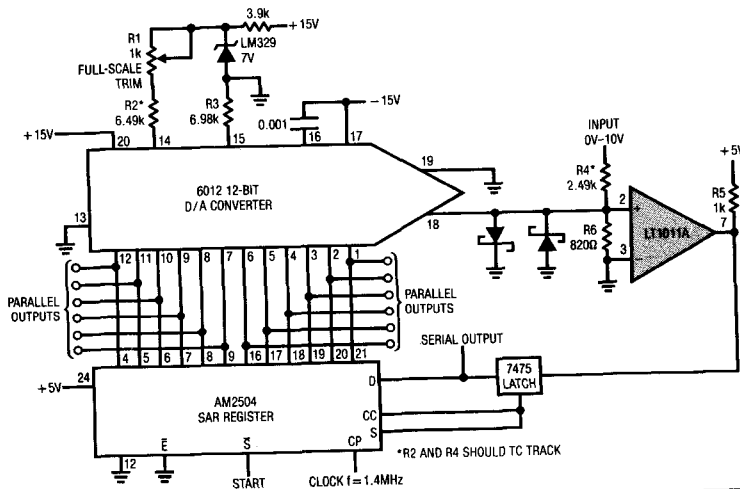
APPLICATIONS

- SAR A to D Converters
- Voltage to Frequency Converters
- Precision R/C Oscillator
- Peak Detector
- Motor Speed Control
- Pulse Generator
- Relay/Lamp Driver

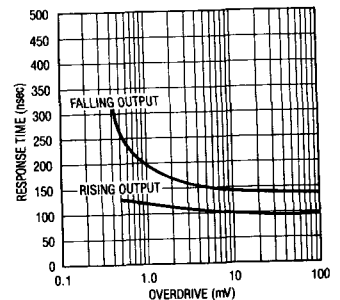
DESCRIPTION

The LT1011 is a general purpose comparator with significantly better input characteristics than the LM111. Although pin-compatible with the LM111, it offers four times lower bias current, six times lower offset voltage, and five times higher voltage gain. Offset voltage drift—a previously unspecified parameter—is guaranteed at $15\mu V/^\circ C$. Additionally, the supply current is lower by a factor of two with no loss in speed. The LT1011 is several times faster than the LM111 when subjected to large overdrive conditions. It is also fully specified for DC parameters and response time when operating on a single +5V supply. These parametric improvements allow the LT1011 to be used in high accuracy (≥ 12 -bit) systems without trimming. In a 12-bit A to D application, for instance, using a 2mA DAC, the offset error introduced by the LT1011 is less than 1/2 LSB. The LT1011 retains all the versatile features of the LM111, including single 3V to $\pm 18V$ supply operation, and a floating transistor output with 50mA source/sink capability. It can drive loads referenced to ground, negative supply or positive supply, and is specified up to 50V between V^- and the collector output. A differential input voltage up to the full supply voltage is allowed, even with $\pm 18V$ supplies, enabling the inputs to be clamped to the supplies with simple diode clamps.

10 μ s 12-Bit A-D Converter



Response Time vs Overdrive



ABSOLUTE MAXIMUM RATINGS

Supply Voltage (pin 8 to pin 4)	36V
Output to Negative Supply (pin 7 to pin 4)	
LT1011AM, LT1011M	50V
LT1011AC, LT1011C	40V
Ground to Negative Supply (pin 1 to pin 4)	30V
Differential Input Voltage	±36V
Voltage at Strobe Pin (pin 6 to pin 8)	5V
Input Voltage (Note 1)	Equal to Supplies
Output Short Circuit Duration	10 sec.
Operating Temperature Range (Note 2)	
LT1011AM/LT1011M	-55°C to 125°C
LT1011AC/LT1011C	0°C to 70°C
Storage Temperature Range	-65°C to 150°C
Lead Temperature (Soldering, 10 sec.)	300°C

PACKAGE/ORDER INFORMATION

<p>TOP VIEW H PACKAGE TO-5 METAL CAN</p>	ORDER PART NUMBER
	LT1011AMH LT1011MH LT1011ACH LT1011CH
<p>TOP VIEW J8 PACKAGE 8 PIN CERDIP</p>	LT1011AMJ8 LT1011MJ8 LT1011ACJ8 LT1011CJ8 LT1011ACN8 LT1011CN8

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V, V_{CM} = 0V, R_S = 0, T_J = 25^\circ C, V_I = -15V,$ output at pin 7 unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1011AM/LT1011AC		LT1011M/LT1011C		UNITS
			MIN	TYP MAX	MIN	TYP MAX	
V_{OS}	Input Offset Voltage	Note 3	●	0.3 0.5	0.6 1.5	3.0	mV
V_{OS}	*Input Offset Voltage	$R_S \leq 50k\Omega$ (Note 4)	●	0.75 1.5	2.0 3.0		mV
I_{OS}	*Input Offset Current	Note 4	●	0.2 3 5	0.2 4 6		nA
I_b	Input Bias Current	Note 3		15 25	20 50		nA
I_b	*Input Bias Current	Note 4	●	20 35 50	25 65 80		nA
$\frac{\Delta V_{OS}}{\Delta T}$	Input Offset Voltage Drift (Note 5)	$T_{MIN} \leq T \leq T_{MAX}$	●	4 15	4 25		$\mu V/^\circ C$
A_{VOL}	*Large Signal Voltage Gain	$R_L = 1k\Omega$ to +15V, -10V $\leq V_{OUT} \leq$ 14.5V $R_L = 500\Omega$ to +5V, 0.5V $\leq V_{OUT} \leq$ 4.5V		200 500	200 500		V/mV
CMRR	Common-Mode Rejection Ratio			94 115	90 115		dB
	*Input Voltage Range (Note 8)	$V_S = \pm 15V$ $V_S = \text{Single } +5V$	●	-14.5 13	-14.5 13		V
			●	0.5 3.0	0.5 3.0		V
T_d	*Response Time	Note 6		150 250	150 250		ns
V_{OL}	*Output Saturation Voltage	$V_{IN} = 5mV, I_{SINK} = 8mA$ $V_I = 0, I_{SINK} = 50mA$	●	0.25 0.4	0.25 0.4		V
			●	0.7 1.5	0.7 1.5		V
	*Output Leakage Current	$V_{IN} = 5mV, V_I = -15V$ $V_{OUT} = 35V$ (25V for LT1011C)	●	0.2 10 500	0.2 10 500		nA
	*Positive Supply Current			3.2 4.0	3.2 4.0		mA
	*Negative Supply Current			1.7 2.5	1.7 2.5		mA
	*Strobe Current	Minimum to Ensure Output Transistor is Off		500	500		μA
	Input Capacitance			6	6		pF

* indicates parameters which are guaranteed for all supply voltages, including a single 5V supply. See Note 4.

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: Inputs may be clamped to supplies with diodes so that maximum input voltage actually exceeds supply voltage by one diode drop. See Input Protection in applications section.

Note 2: $T_j \text{ max} = 150^\circ\text{C}$ for the LT1011AM/LT1011M and 95°C for the LT1011AC/LT1011C.

Note 3: Output is sinking 1.5mA with $V_{\text{OUT}} = 0\text{V}$.

Note 4: These specifications apply for all supply voltages from a single +5V to $\pm 15\text{V}$, the entire input voltage range, and for both high and low output states. The high state is $I_{\text{SINK}} \geq 100\mu\text{A}$, $V_{\text{OUT}} \geq (V^+ - 1\text{V})$ and the low state is $I_{\text{SINK}} \leq 8\text{mA}$, $V_{\text{OUT}} \leq 0.8\text{V}$. Therefore, this specification defines a worst-case error band that includes effects due to common-mode signals, voltage gain, and output load.

Note 5: Drift is calculated by dividing the offset voltage difference measured at min and max temperatures by the temperature difference.

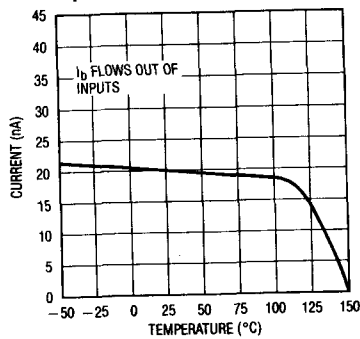
Note 6: Response time is measured with a 100mV step and 5mV overdrive. The output load is a 500Ω resistor tied to +5V. Time measurement is taken when the output crosses 1.4V.

Note 7: Do not short the strobe pin to ground. It should be current driven at 3mA to 5mA for the shortest strobe time. Currents as low as 500μA will strobe the LT111A if speed is not important. External leakage on the strobe pin in excess of 0.2μA when the strobe is "off" can cause offset voltage shifts.

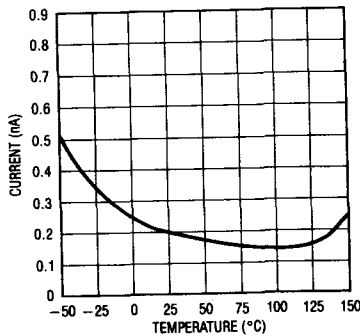
Note 8: See graph, Input Offset Voltage vs Common-Mode Voltage.

TYPICAL PERFORMANCE CHARACTERISTICS

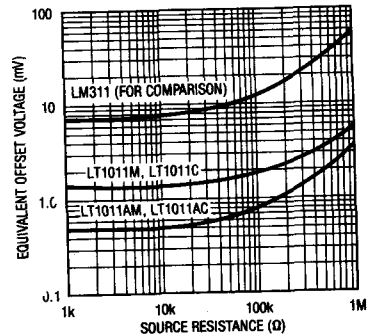
Input Bias Current



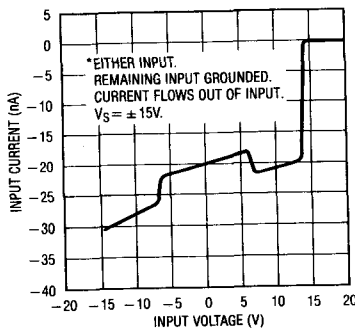
Input Offset Current



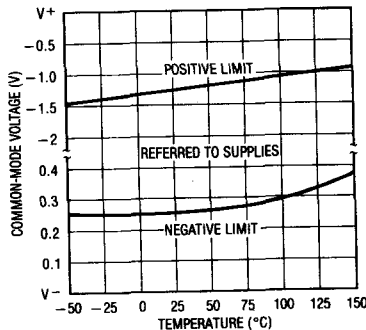
Worst-Case Offset Error



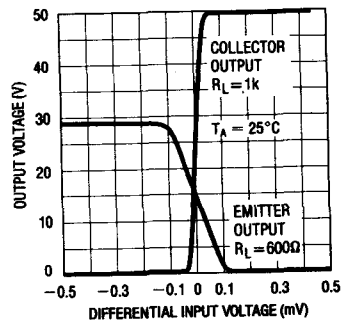
Input Characteristics*



Common-Mode Limits

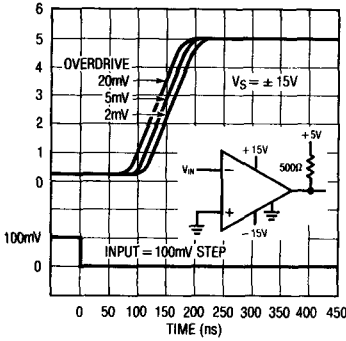


Transfer Function (Gain)

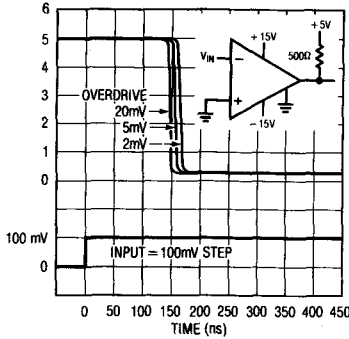


TYPICAL PERFORMANCE CHARACTERISTICS

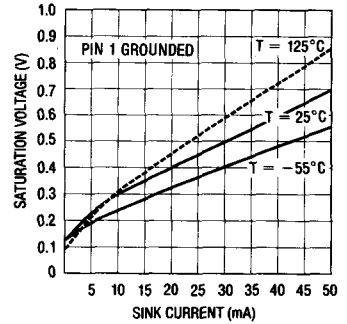
Response Time—
Collector Output



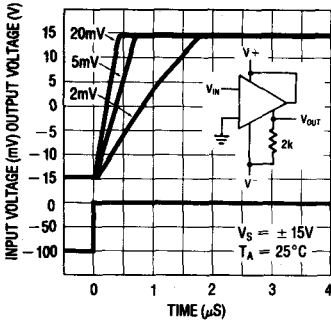
Response Time—
Collector Output



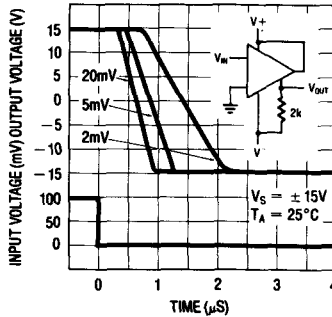
Collector Output Saturation
Voltage



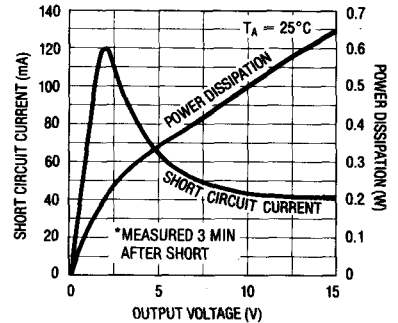
Response Time Using GND Pin
as Output



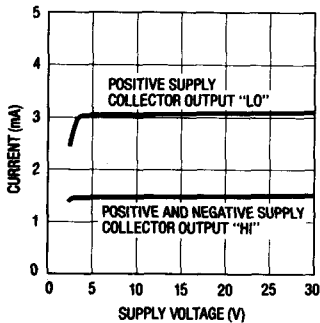
Response Time Using GND Pin
as Output



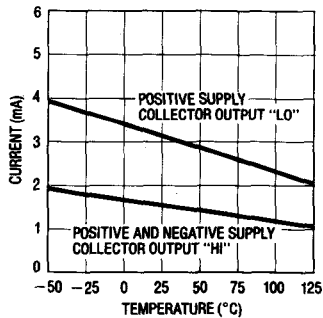
Output Limiting
Characteristics*



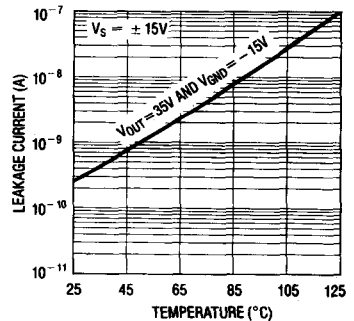
Supply Current vs Supply
Voltage



Supply Current vs Temperature

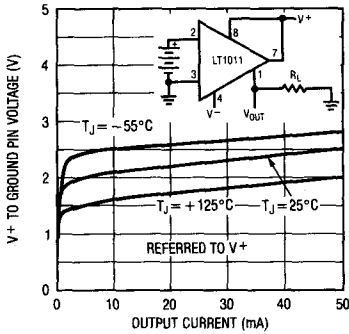


Output Leakage Current

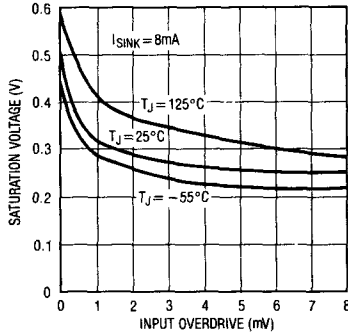


TYPICAL PERFORMANCE CHARACTERISTICS

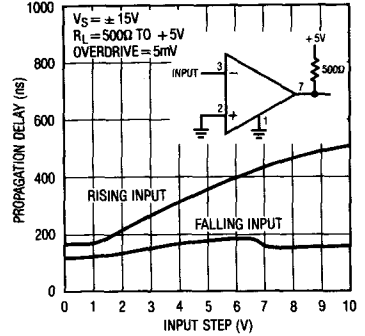
**Output Saturation—
Ground Output**



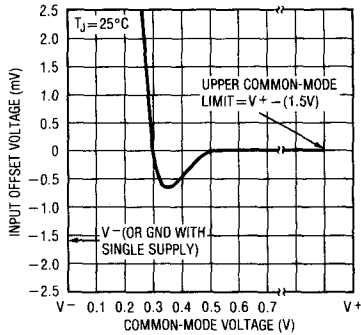
Output Saturation Voltage



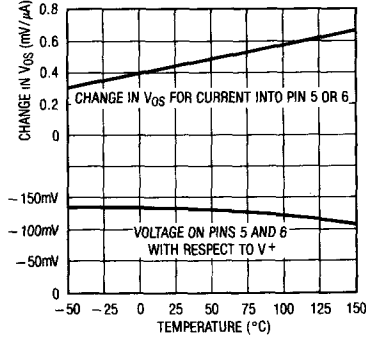
Response Time vs Input Step Size



**Input Offset Voltage vs Common-
Mode Voltage**



Offset Pin Characteristics



6

APPLICATIONS INFORMATION

Preventing Oscillation Problems

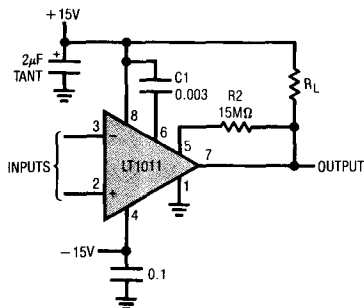
Oscillation problems in comparators are nearly always caused by stray capacitance between the output and inputs or between the output and other sensitive pins on the comparator. This is especially true with high gain-bandwidth comparators like the LT1011, which are designed for fast switching with millivolt input signal levels. The gain-bandwidth product of the LT1011 is over 10GHz. Oscillation problems tend to occur at frequencies around 5MHz, where the LT1011 has a gain of ≈ 2000 . This implies that attenuation of output signals must be at least 2000:1 at 5MHz as measured at the inputs. If the source impedance is $1k\Omega$, the effective stray capacitance between output and input must have a reactance of more than (2000) ($1k\Omega$) = $2M\Omega$, or less than $0.02pF$. The actual interlead capacitance between input and output pins on the LT1011 is less than $0.002pF$ when cut to printed circuit mount length. Additional stray capacitance due to printed circuit traces must be minimized by routing the output trace directly away from input lines and, if possible, running ground traces next to input traces to provide shielding. Additional steps to ensure oscillation-free operation are:

1. Bypass the strobe/balance pins with a $0.01\mu F$ capacitor connected from pin 5 to pin 6. This eliminates stray capacitive feedback from the output to the balance pins, which are nearly as sensitive as the inputs.
2. Bypass the negative supply (pin 4) with a $0.1\mu F$ ceramic capacitor close to the comparator. $0.1\mu F$ can also be used for the positive supply (pin 8) if the pull-up load is tied to a separate supply. When the pull-up load is tied directly to pin 8, use a $2\mu F$ solid tantalum bypass capacitor.
3. Bypass any slow moving or DC input with a capacitor ($\geq 0.01\mu F$) close to the comparator to reduce high frequency source impedance.
4. Keep resistive source impedance as low as possible. If a resistor is added in series with one input to balance source impedances for DC accuracy, bypass it with a capacitor. The low input bias current of the

LT1011 usually eliminates any need for source resistance balancing. A $5k\Omega$ imbalance, for instance, will create only $0.25mV$ DC offset.

5. Use hysteresis. This consists of shifting the input offset voltage of the comparator when the output changes state. Hysteresis forces the comparator to move quickly through its linear region, eliminating oscillations by "overdriving" the comparator under all input conditions. Hysteresis may be either AC or DC. AC techniques do not shift the apparent offset voltage of the comparator, but require a *minimum* input signal slew rate to be effective. DC hysteresis works for all input slew rates, but creates a shift in offset voltage dependent on the previous condition of the input signal. The circuit shown below is an excellent compromise between AC and DC hysteresis.

Comparator with Hysteresis

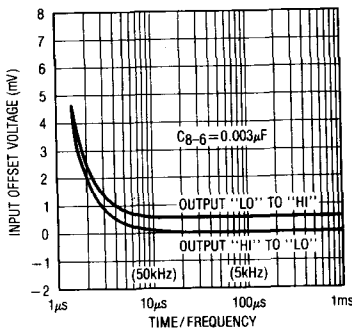


This circuit is especially useful for general purpose comparator applications because it does not force any signals directly back onto the input signal source. Instead, it takes advantage of the unique properties of the balance pins to provide extremely fast, clean output switching even with low frequency input signals in the millivolt range. The $0.003\mu F$ capacitor from pin 6 to pin 8 generates AC hysteresis because the voltage on the balance pins shifts slightly, depending on the state of the output. Both pins move about $4mV$. If one pin (6) is bypassed, AC hysteresis is created. It is only a few millivolts referred to the inputs, but is sufficient to switch the output at nearly the maximum speed of which the comparator is capable. To prevent

APPLICATIONS INFORMATION

problems from low values of input slew rate, a slight amount of DC hysteresis is also used. The sensitivity of the balance pins to current is about 0.5mV input referred offset for each microampere of balance pin current. The 15mΩ resistor tied from output to pin 5 generates 0.5mV DC hysteresis. The combination of AC and DC hysteresis creates clean oscillation-free switching with very small input errors. The curve below plots input referred error versus switching frequency for the circuit as shown.

Input Offset Voltage vs Time to Last Transition



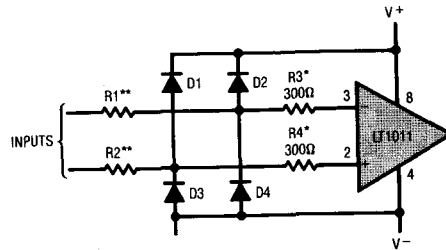
Note that at low frequencies, the error is simply the DC hysteresis, while at high frequencies, an additional error is created by the AC hysteresis. The high frequency error can be reduced by reducing C_H , but lower values may not provide clean switching with very low slew rate input signals.

Input Protection

The inputs to the LT1011 are particularly suited to general purpose comparator applications because large differential and/or common-mode voltages can be tolerated without damage to the comparator. Either or both inputs can be raised 40V above the negative supply, independent of the positive supply voltage. Internal forward biased diodes will conduct when the inputs are taken below the

negative supply. In this condition, input current must be limited to 1mA. If very large (fault) input voltages must be accommodated, series resistors and clamp diodes should be used (see drawing below).

Limiting Fault Input Currents



- D1-D4 1N4148
- *MAY BE ELIMINATED FOR
- $I_{FAULT} \approx 1mA$
- **SELECT ACCORDING TO ALLOWABLE FAULT CURRENT AND POWER DISSIPATION

The input resistors should limit fault current to a reasonable value (0.1mA to 20mA). Power dissipation in the resistors must be considered for continuous faults, especially when the LT1011 supplies are off. And one final caution: lightly loaded supplies may be forced to higher voltages by large fault currents flowing through D1-D4.

R3 and R4 limit input current to the LT1011 to less than 1mA when the input signals are held below V^- . They may be eliminated if R1 and R2 are large enough to limit fault current to less than 1mA.

Input Slew Rate Limitations

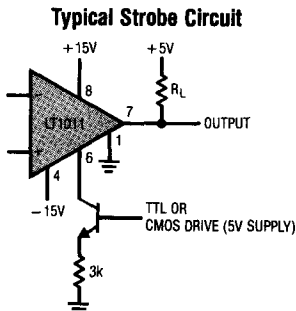
The response time of a comparator is typically measured with a 100mV step and a 5mV-10mV overdrive. Unfortunately, this does not simulate many real-world situations where the step size is typically much larger and overdrive can be significantly less. In the case of the LT1011, step size is important because the slew rate of internal nodes will limit response time for input step sizes larger than 1V. At 5V step size, for instance, response time increases from 150ns to 360ns. See the curve labeled Response Time vs Input Step Size for more detail.

APPLICATIONS INFORMATION

If response time is critical and large input signals are expected, clamp diodes across the inputs are recommended. The slew rate limitation can also affect performance when differential input voltage is low, but both inputs must slew quickly. Maximum suggested common-mode slew rate is $10V/\mu s$.

Strobing

The LT1011 can be strobed by pulling current out of the strobe pin. The output transistor is forced to an "off" state, giving a "hi" output at the collector (pin 7). Currents as low as $250\mu A$ will cause strobing, but at low strobe currents strobe delay will be 200ns–300ns. If strobe current is increased to 3mA, strobe delay drops to about 60ns. The voltage at the strobe pin is about 150mV below V^+ at zero strobe current and about 2V below V^+ for 3mA strobe current. *Do not ground the strobe pin. It must be current driven.* The drawing below shows a typical strobe circuit.



Note that there is no bypass capacitor between pins 5 and 6. This maximizes strobe speed, but leaves the comparator more sensitive to oscillation problems for slow, low level inputs. A 1pF capacitor between the output and pin 5 will greatly reduce oscillation problems without reducing strobe speed.

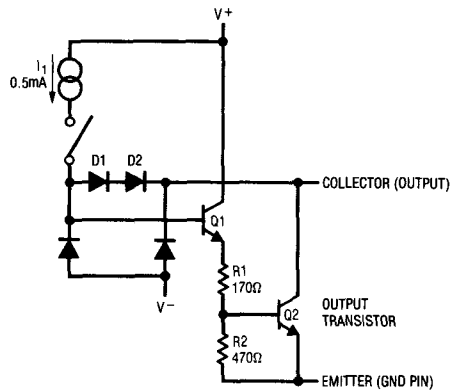
DC hysteresis can also be added by placing a resistor from output to pin 5. See step number 5 under "Preventing Oscillation Problems".

The pin (6) used for strobing is also one of the offset adjust pins. Current flow into or out of pin 6 must be kept very low ($<0.2\mu A$) when not strobing to prevent input offset voltage shifts.

Output Transistor

The LT1011 output transistor is truly floating in the sense that no current flows into or out of either the collector or emitter when the transistor is in the "off" state. The equivalent circuit is shown in the drawing below.

Output Transistor Circuitry



In the "off" state, I_1 is switched off and both Q1 and Q2 turn off. The collector of Q2 can be now held at any voltage above V^- without conducting current, including voltages above the positive supply level. Maximum voltage above V^- is 50V for the LT1011 and 40V for the LT1011C. The emitter can be held at any voltage between V^+ and V^- as long as it is negative with respect to the collector.

In the "on" state, I_1 is connected, turning on Q1 and Q2. Diodes D1 and D2 prevent deep saturation of Q2 to improve speed and also limit the drive current of Q1. The R_1/R_2 divider sets the saturation voltage of Q2 and provides turn-off drive. Either the collector or emitter pin can be held at a voltage between V^+ and V^- . This allows the remaining pin to drive the load. In typical applications, the emitter is connected to V^- or ground and the collector drives a load tied to V^+ or a separate positive supply.

APPLICATIONS INFORMATION

When the emitter is used as the output, the collector is typically tied to V^+ and the load is connected to ground or V^- . Note that the emitter output is phase reversed with respect to the collector output so that the "+" and "-" input designations must be reversed. When the collector is tied to V^+ , the voltage at the emitter in the "on" state is about 2V below V^+ (see curves).

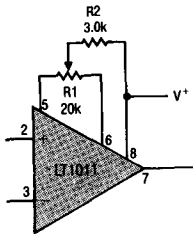
Input Signal Range

The common-mode input voltage range of the LT1011 is about 300mV above the negative supply and 1.5V below

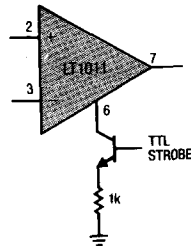
the positive supply, independent of the actual supply voltages (see curve in typical performance characteristics). This is the voltage range over which the output will respond correctly when the common-mode voltage is applied to one input and a higher or lower signal is applied to the remaining input. *If one input is inside the common-mode range and one is outside, the output will be correct. If the inputs are outside the common-mode range in opposite directions, the output will still be correct. If both inputs are outside the common-mode range in the same direction, the output will not respond to the differential input; it will remain unconditionally high (collector output).*

TYPICAL APPLICATIONS

Offset Balancing

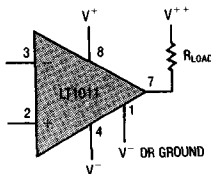


Strobing



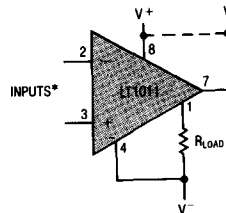
NOTE: DO NOT GROUND STROBE PIN.

Driving Load Referenced to Positive Supply



V^{++} CAN BE GREATER OR LESS THAN V^+

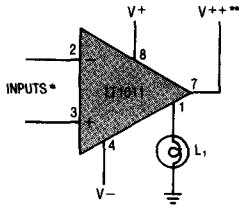
Driving Load Referenced to Negative Supply



* INPUT POLARITY IS REVERSED WHEN USING PIN 1 AS OUTPUT

TYPICAL APPLICATIONS

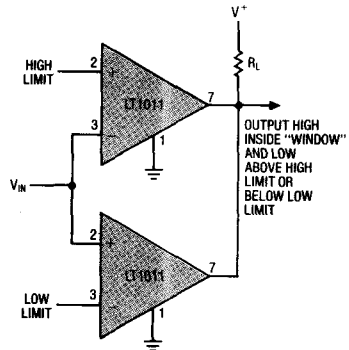
Driving Ground Referred Load



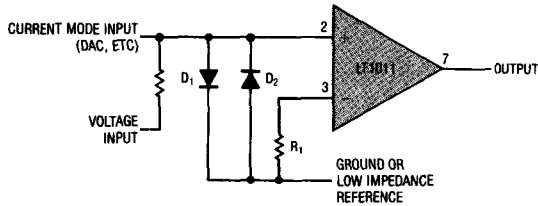
* INPUT POLARITY IS REVERSED WHEN USING PIN 1 AS OUTPUT

**V++ MAY BE ANY VOLTAGE ABOVE V-. PIN 1 SWINGS TO WITHIN ≈ 2V OF V++.

Window Detector

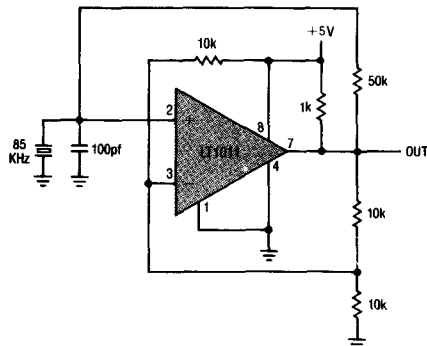


Using Clamp Diodes to Improve Frequency Response*



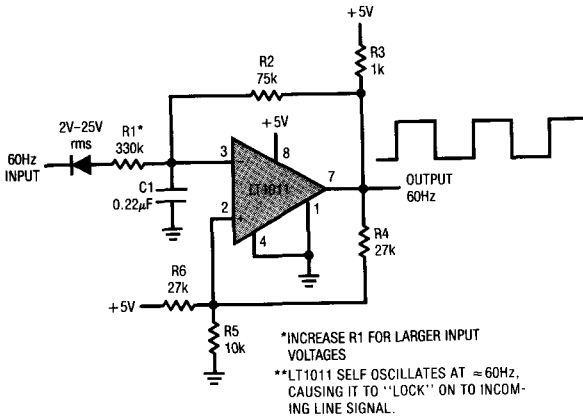
*SEE CURVE, "RESPONSE TIME VS INPUT STEP SIZE"

Crystal Oscillator



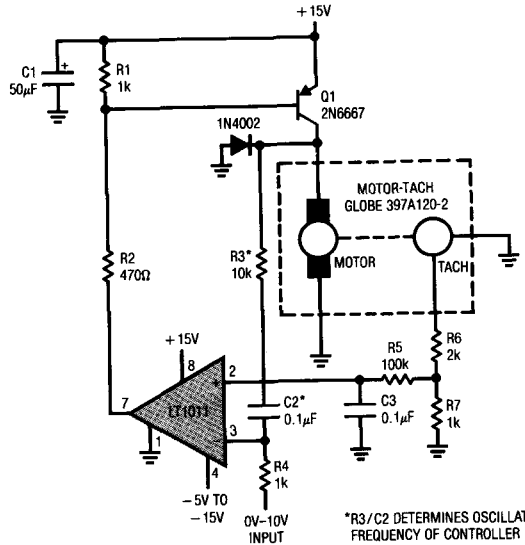
TYPICAL APPLICATIONS

Noise Immune 60Hz Line Sync**



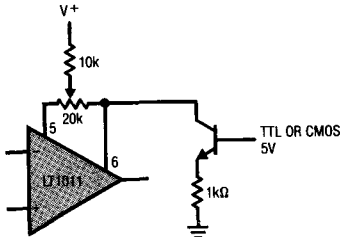
*INCREASE R1 FOR LARGER INPUT VOLTAGES
 **LT1011 SELF OSCILLATES AT $\approx 60\text{Hz}$, CAUSING IT TO "LOCK" ON TO INCOMING LINE SIGNAL.

High Efficiency Motor Speed Controller**

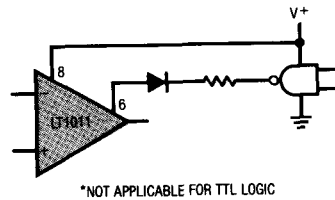


*R3/C2 DETERMINES OSCILLATION FREQUENCY OF CONTROLLER
 **Q1 OPERATES IN SWITCH MODE

Combining Offset Adjust and Strobe

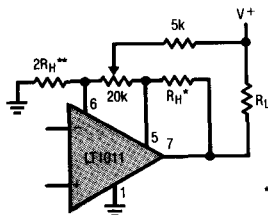


Direct Strobe Drive when CMOS* Logic Uses Same V+ Supply as LT1011



*NOT APPLICABLE FOR TTL LOGIC

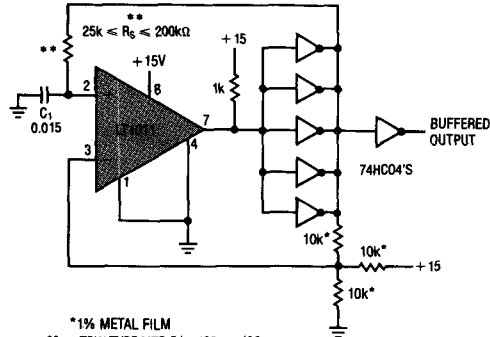
Combining Offset Adjustment and Hysteresis



*HYSTERESIS IS $\approx 0.45\text{mV}/\mu\text{A}$ OF CURRENT CHANGE IN R_H
 **THIS RESISTOR CAUSES HYSTERESIS TO BE CENTERED AROUND V_{OS}

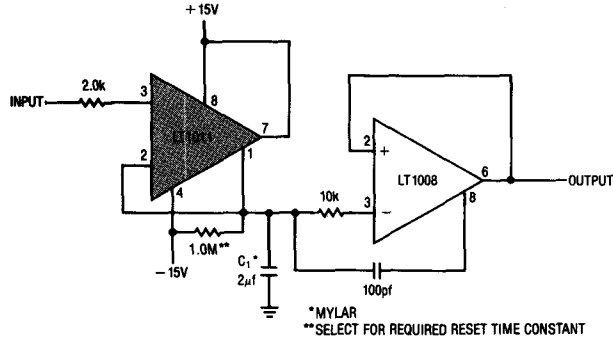
TYPICAL APPLICATIONS

Low Drift R/C Oscillator†



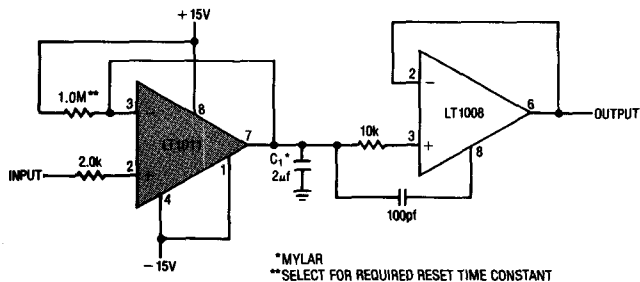
*1% METAL FILM
 ** = TRW TYPE MTR-5/+ 120ppm/°C.
 C₁ = .015 = POLYSTYRENE -120ppm/°C ± 30ppm WESCO TYPE 32-P
 NOTE: COMPARATOR CONTRIBUTES ≤ 10ppm/°C DRIFT FOR FREQUENCIES BELOW 10kHz.
 †LOW DRIFT AND ACCURATE FREQUENCY ARE OBTAINED BECAUSE THIS CONFIGURATION REJECTS EFFECTS DUE TO INPUT OFFSET VOLTAGE AND BIAS CURRENT OF THE COMPARATOR.

Positive Peak Detector



*MYLAR
 **SELECT FOR REQUIRED RESET TIME CONSTANT

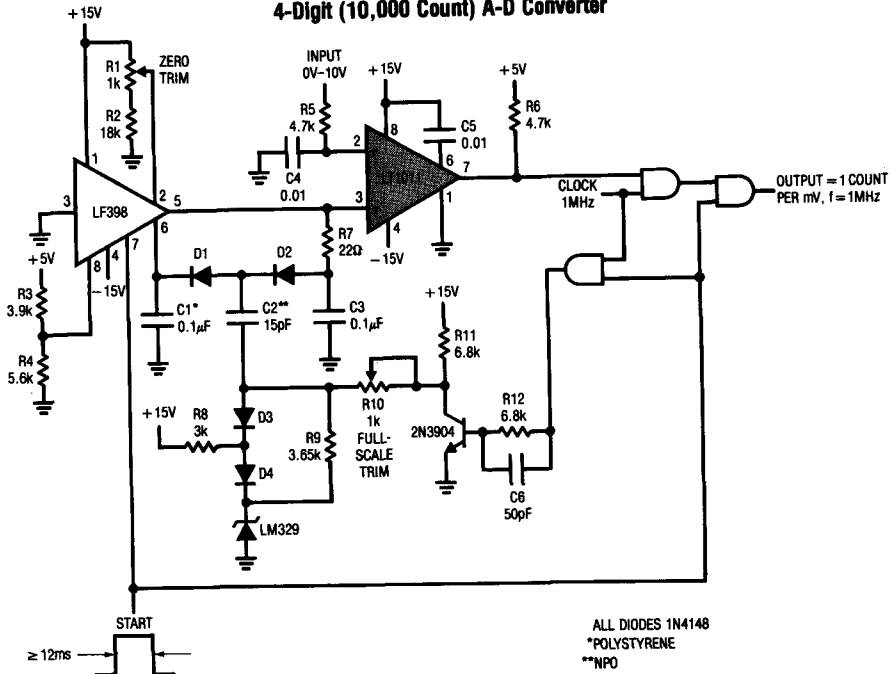
Negative Peak Detector



*MYLAR
 **SELECT FOR REQUIRED RESET TIME CONSTANT

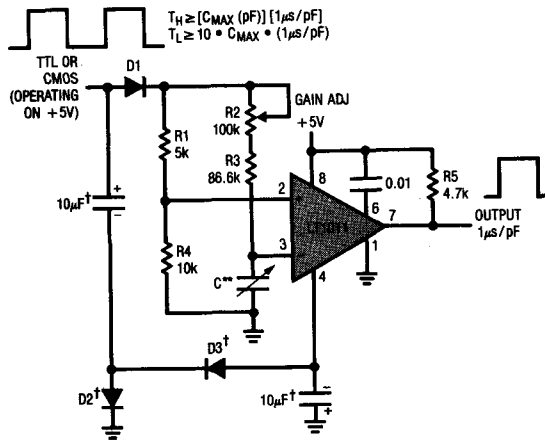
TYPICAL APPLICATIONS

4-Digit (10,000 Count) A-D Converter



6

Capacitance to Pulse Width Converter



$$*PW = (R2 + R3) (C) \left(\frac{R1 + R4}{R1} \right), \text{ INPUT CAPACITANCE OF}$$

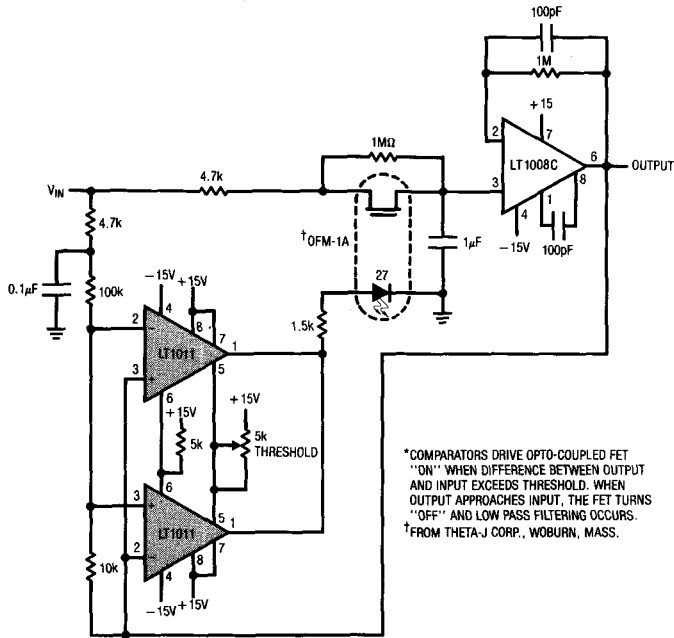
LT1011 IS $\approx 6pF$. THIS IS AN OFFSET TERM.

† THESE COMPONENTS MAY BE ELIMINATED IF NEGATIVE SUPPLY IS AVAILABLE (-1V TO -15V).

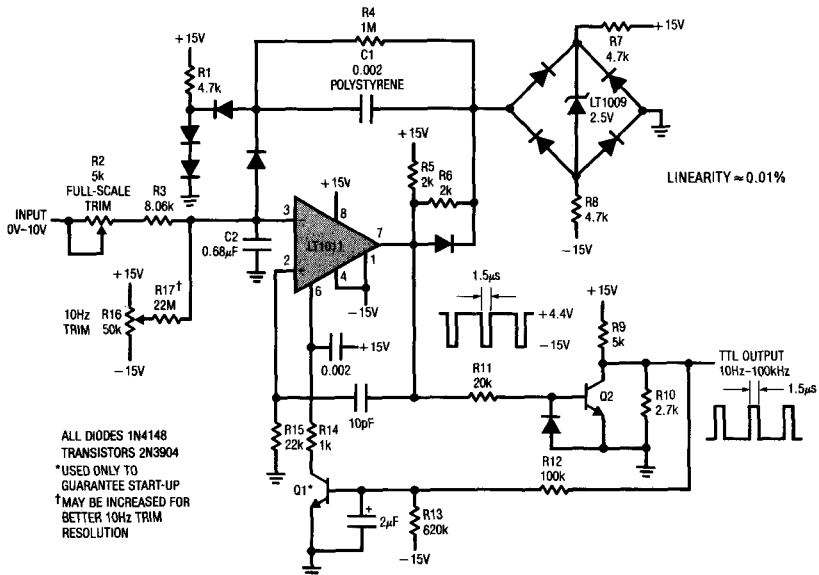
** TYPICAL 2 SECTIONS OF 365pF VARIABLE CAPACITOR WHEN USED AS SHAFT ANGLE INDICATION.

TYPICAL APPLICATIONS

Fast Settling* Filter

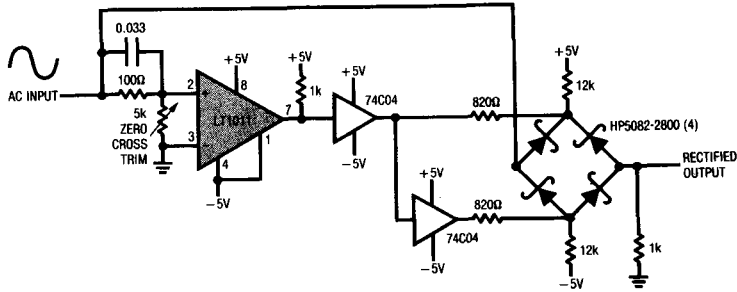


10Hz to 100kHz Voltage to Frequency Converter

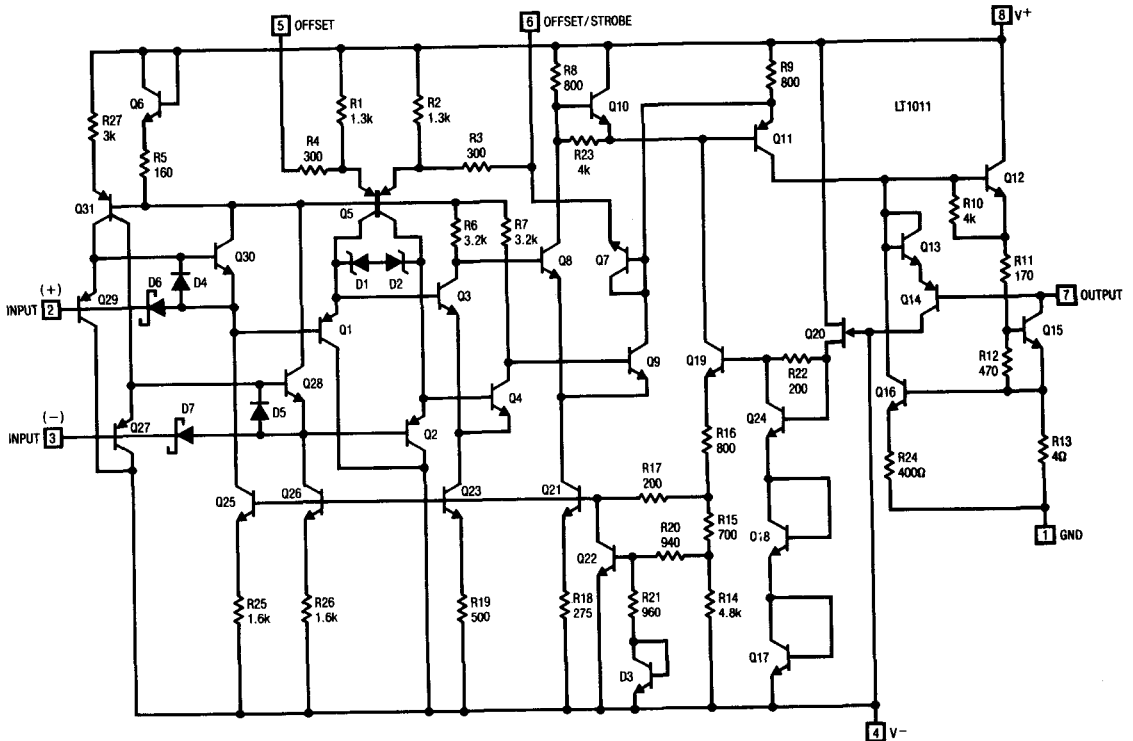


TYPICAL APPLICATIONS

100kHz Precision Rectifier



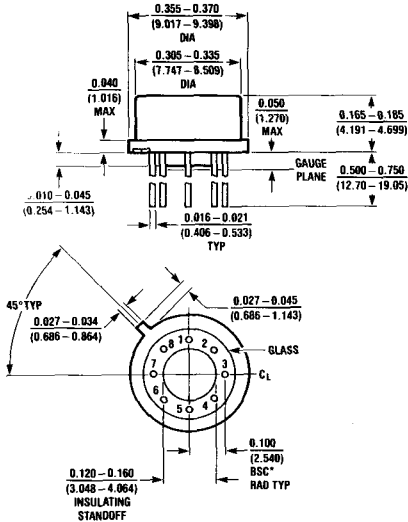
SCHEMATIC DIAGRAM



6

PACKAGE DESCRIPTION

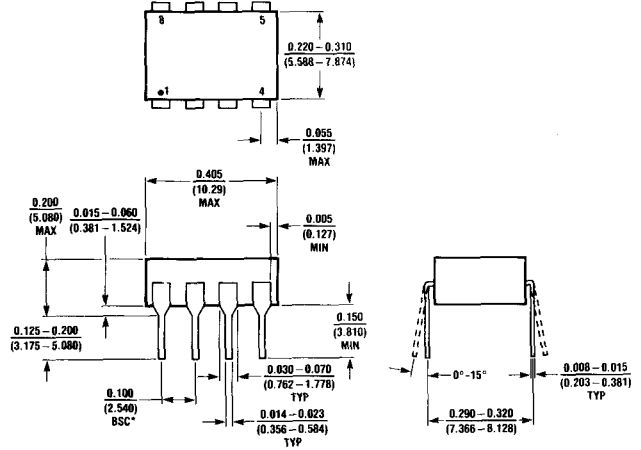
**H Package
Metal Can**



NOTE: DIMENSIONS IN INCHES

T_{fmax}	θ_{ja}	θ_{jc}
150°C	150°C/W	45°C/W

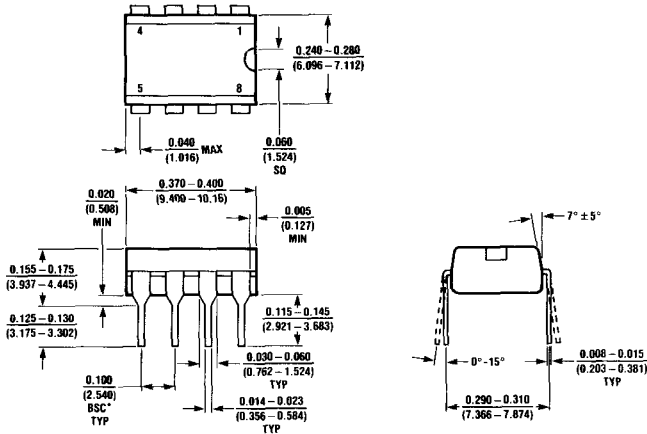
**J8 Package
8 Lead Hermetic DIP**



NOTE: DIMENSIONS IN INCHES UNLESS OTHERWISE NOTED
*LEADS WITHIN 0.007 OF TRUE POSITION (TP) AT GAUGE PLANE

T_{fmax}	θ_{ja}
150°C	100°C/W

**N8 Package
8 Lead Plastic**



NOTE: DIMENSIONS IN INCHES UNLESS OTHERWISE NOTED
*LEADS WITHIN 0.007 OF TRUE POSITION (TP) AT GAUGE PLANE

T_{fmax}	θ_{ja}
100°C	130°C/W

FEATURES

- Ultra Fast (10ns typ)
- Operates Off **Single** +5V Supply, or $\pm 5V$
- Complementary Output to TTL
- Low Offset Voltage
- No Minimum Input Slew Rate Requirement
- No Power Supply Current Spiking
- Output Latch Capability

APPLICATIONS

- High Speed A to D Converters
- High Speed Sampling Circuits
- Line Receiver
- Extended Range V to F Converters
- Fast Pulse Height/Width Discriminators

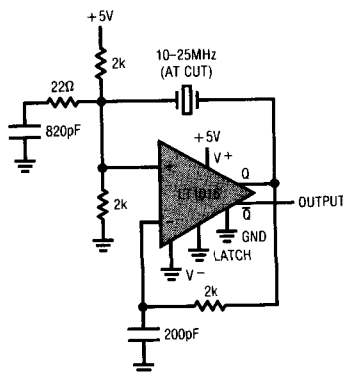
DESCRIPTION

The LT1016 is an ultra fast (10ns) comparator specifically designed to interface directly to TTL logic while operating off either a dual $\pm 5V$ supply or a single +5V supply. Tight offset voltage specifications and high gain allow the LT1016 to be used in precision applications. Matched complementary outputs further extend the versatility of this new comparator.

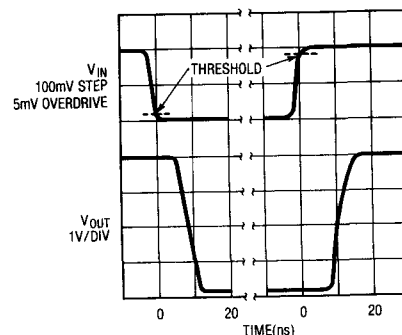
A unique output stage is featured on the LT1016. It provides active drive in both directions for maximum speed into TTL logic or passive loads, yet does not exhibit the large current spikes normally found in "totem pole" output stages. This eliminates the need for a minimum input slew rate typical of other very fast comparators. The ability of the LT1016 to remain stable with the outputs in the active region greatly reduces the problem of output "glitching" when the input signal is slow moving or is low level.

The LT1016 has a true latch pin for retaining input data at the outputs. The outputs will remain latched as long as the latch pin is held high. Quiescent negative power supply current is only 3mA—about ten times lower than competitive units. This reduces die temperature and allows the negative supply pin to be driven from virtually any supply voltage with a simple resistive divider. Device performance is not affected by variations in negative supply voltage.

10-25MHz Crystal Oscillator



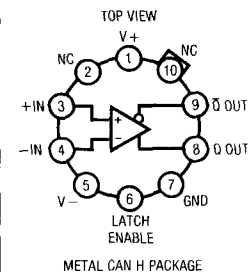
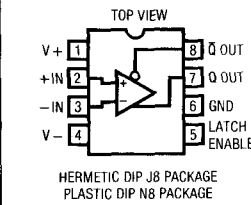
Response Time



ABSOLUTE MAXIMUM RATINGS

Positive Supply Voltage (Note 4) 7V
 Negative Supply Voltage 7V
 Differential Input Voltage ±5V
 Input Voltage (Either Input) Equal to Supplies
 Latch Pin Voltage Equal to Supplies
 Output Current (Continuous) ±20mA
 Operating Temperature Range
 LT1016M -55°C to +125°C
 LT1016C 0°C to +70°C
 Storage Temperature Range -65°C to +150°C
 Lead Temperature (Soldering, 10 sec) 300°C

PACKAGE/ORDER INFORMATION

 <p>TOP VIEW V+ NC +IN -IN V- GND LATCH ENABLE Q OUT Q OUT METAL CAN H PACKAGE</p>	ORDER PART NUMBER
	LT1016MH LT1016CH
 <p>TOP VIEW V+ +IN -IN V- LATCH ENABLE Q OUT Q OUT HERMETIC DIP J8 PACKAGE PLASTIC DIP N8 PACKAGE</p>	LT1016MJ LT1016CJ LT1016CN

ELECTRICAL CHARACTERISTICS

V+ = 5V, V- = 5V, V_{OUT(Q)} = 1.4V, V_{LATCH} = 0V, T_A = 25°C, unless otherwise noted.

SYMBOL	PARAMETERS	CONDITIONS	LT1016M			LT1016C			UNITS	
			MIN	TYP	MAX	MIN	TYP	MAX		
V _{OS}	Input Offset Voltage	R _S ≤ 100Ω (Note 1)		0.8	±2		1.0	±3	mV	
					3			3.5	mV	
$\frac{\Delta V_{OS}}{\Delta T}$	Input Offset Voltage Drift			4			4		μV/°C	
I _{OS}	Input Offset Current	(Note 1)		0.3	1		0.3	1	μA	
					1.3		0.3	1.3	μA	
I _B	Input Bias Current	(Note 2)		5	10		5	10	μA	
					13			13	μA	
	Input Voltage Range	(Note 5)	•	-3.75	+3.5	•	-3.75	+3.5	V	
		Single +5V Supply	•	+1.25	+3.5	•	+1.25	+3.5	V	
CMRR	Common-Mode Rejection	-3.75V ≤ V _{CM} ≤ +3.5V	•	80	96	•	80	96	dB	
PSRR	Supply Voltage Rejection	Positive Supply 4.6V ≤ V+ ≤ 5.4V	•	60	75	•	60	75	dB	
		Negative Supply 2V ≤ V- ≤ 7V	•	80	100	•	80	100	dB	
A _V	Small Signal Voltage Gain	1V ≤ V _{OUT} ≤ 2V		1400	3000		1400	3000	V/V	
V _{OH}	Output High Voltage	V+ ≤ 4.6V, I _{OUT} = 1mA	•	2.7	3.4	•	2.7	3.4	V	
		I _{OUT} = 10mA	•	2.4	3.0	•	2.4	3.0	V	
V _{OL}	Output Low Voltage	I _{SINK} = 4mA	•		0.3	0.5		0.3	0.5	V
		I _{SINK} = 10mA	•			0.4		0.4	V	
I+	Positive Supply Current		•	25	35		25	35	mA	
I-	Negative Supply Current		•	3	5		3	5	mA	
V _{IH}	Latch Pin Hi Input Voltage		•	2.0			2.0		V	
V _{IL}	Latch Pin Lo Input Voltage		•		0.8			0.8	V	
I _{IL}	Latch Pin Current	V _{LATCH} = 0V	•		500			500	μA	

ELECTRICAL CHARACTERISTICS

$V^+ = 5V$, $V^- = 5V$, $V_{OUT}(0) = 1.4V$, $V_{LATCH} = 0V$, $T_A = 25^\circ C$, unless otherwise noted.

SYMBOL	PARAMETERS	CONDITIONS	LT1016M			LT1016C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PD}	Propagation Delay (Note 3)	$\Delta V_{IN} = 100mV$, $OD = 5mV$	●	10	14	10	14	ns	
	(Note 3)	$\Delta V_{IN} = 100mV$, $OD = 20mV$	●	9	12	9	12	ns	
Δt_{PD}	Differential Propagation Delay	(Note 3) $\Delta V_{IN} = 100mV$, $OD = 5mV$			3		3	ns	
	Latch Setup Time			2		2		ns	

The ● denotes the specifications which apply over the full operating temperature range.

For MIL-STD components, please refer to LTC883 data sheet for test listing and parameters.

Note 1: Input offset voltage is defined as the average of the two voltages measured by forcing first one output, then the other to 1.4V. Input offset current is defined in the same way.

Note 2: Input bias current (I_B) is defined as the average of the two input currents.

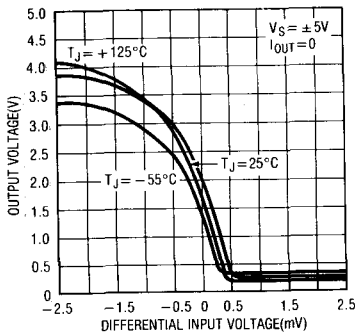
Note 3: t_{PD} and Δt_{PD} cannot be measured in automatic handling equipment with low values of overdrive. The LT1016 is 100% tested with a 1V step and 500mV overdrive at 25°C only. Correlation tests have shown that t_{PD} and Δt_{PD} limits shown can be guaranteed with this test, if additional DC tests are performed to guarantee that all internal bias conditions are correct. For low overdrive conditions V_{OS} is added to overdrive.

Note 4: Electrical specifications apply only up to 5.4V.

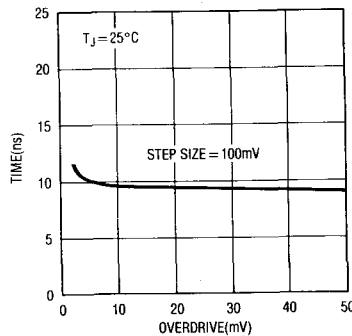
Note 5: See text for discussion of input voltage range for supplies other than $\pm 5V$, or $+5V$.

TYPICAL PERFORMANCE CHARACTERISTICS

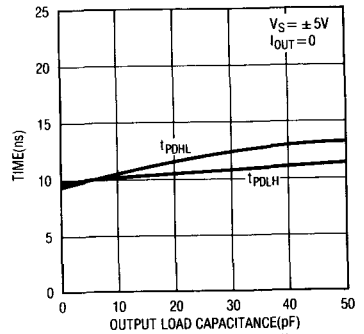
Gain Characteristics



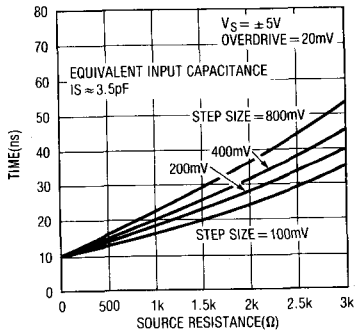
Propagation Delay vs Overdrive



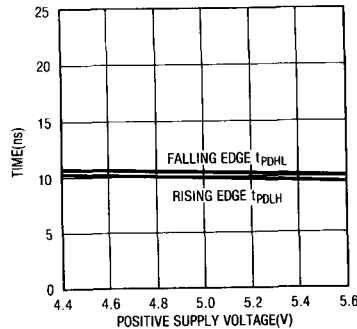
Propagation Delay vs Load Capacitance



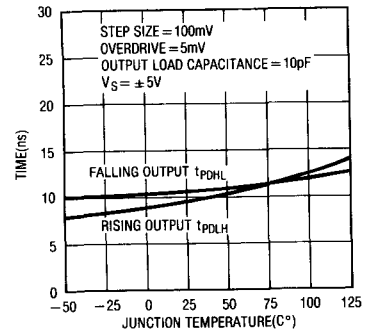
Propagation Delay vs Source Resistance



Propagation Delay vs Supply Voltage

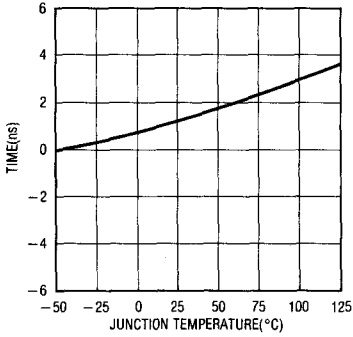


Propagation Delay vs Temperature

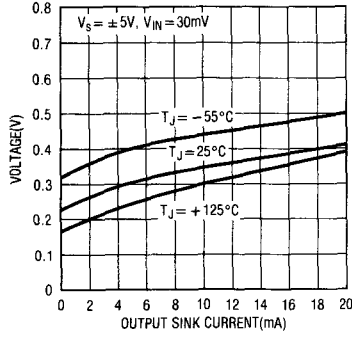


TYPICAL PERFORMANCE CHARACTERISTICS

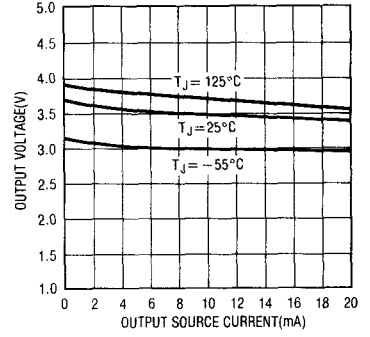
Latch Set-Up Time



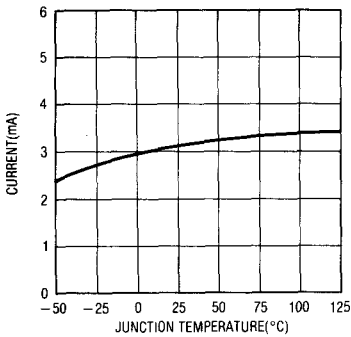
Output Low Voltage (V_{OL})



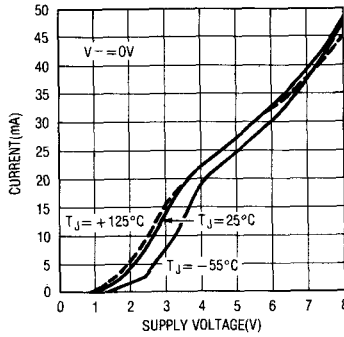
Output High Voltage (V_{OH})



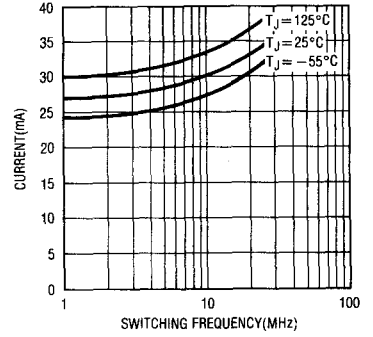
Negative Supply Current



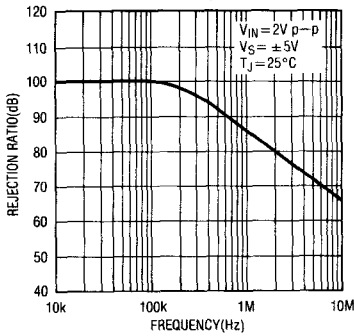
Positive Supply Current



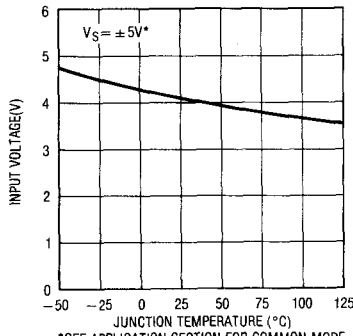
Positive Supply Current



Common-Mode Rejection

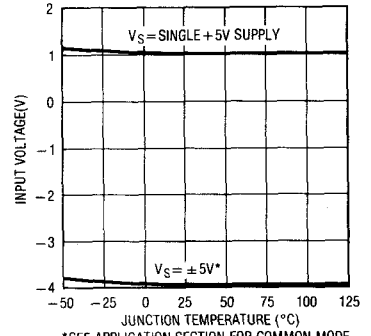


Positive Common-Mode Limit



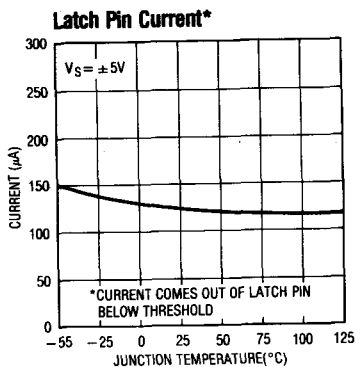
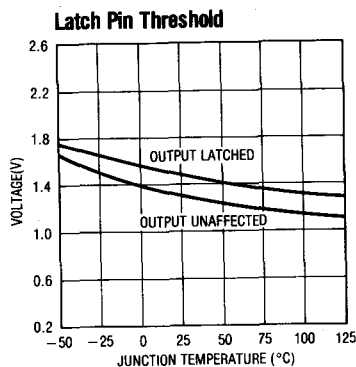
*SEE APPLICATION SECTION FOR COMMON-MODE LIMIT WITH VARYING SUPPLY VOLTAGE.

Negative Common-Mode Limit



*SEE APPLICATION SECTION FOR COMMON-MODE LIMIT WITH VARYING SUPPLY VOLTAGE.

TYPICAL PERFORMANCE CHARACTERISTICS



APPLICATIONS INFORMATION

Common-Mode Considerations

The LT1016 is specified for a common-mode range of -3.75V to $+3.5\text{V}$ with supply voltages of $\pm 5\text{V}$. A more general consideration is that the common-mode range is 1.25V above the negative supply and 1.5V below the positive supply, independent of the actual supply voltage. The criteria for common-mode limit is that the output still responds correctly to a small differential input signal. Either input may be outside the common-mode limit (up to the supply voltage) as long as the remaining input is within the specified limit, and the output will still respond correctly. There is one consideration, however, for inputs which exceed the positive common-mode limit. Propagation delay will be increased by up to 10ns if the signal input is more positive than the upper common-mode limit and then switches back to within the common-mode range. This effect is not seen for signals more negative than the lower common-mode limit.

Input Impedance and Bias Current

Input bias current is measured with the output held at 1.4V . As with any simple NPN differential input stage, the LT1016 bias current will go to zero on an input which is low and double on the input which is high. If both inputs are less than 0.8V above V^- , both input bias currents will go to zero. If either input exceeds the positive

common-mode limit, input bias current will increase rapidly, approaching several milliamperes at $V_{IN} = V^+$.

Differential input resistance at zero differential input voltage is about $10\text{k}\Omega$, rapidly increasing as larger DC differential input signals are applied. Common-mode input resistance is about $4\text{M}\Omega$ with zero differential input voltage. With large differential input signals, the high input will have an input resistance of about $2\text{M}\Omega$ and the low input, greater than $20\text{M}\Omega$.

Input capacitance is typically 3.5pF . This is measured by inserting a $1\text{k}\Omega$ resistor in series with the input and measuring the resultant change in propagation delay.

Latch Pin Dynamics

The latch pin is intended to retain input data (output latched) when the latch pin goes high. This pin will float to a high state when disconnected, so a flow-through condition requires that the latch pin be grounded. To guarantee data retention, the input signal must be valid at least 5ns before the latch goes high (set-up time) and must remain valid at least 3ns after the latch goes high (hold time). When the latch goes low, new data will appear at the output in approximately $8\text{--}10\text{ns}$. The latch pin is designed to be driven with TTL or CMOS gates. It has no built-in hysteresis.

APPLICATIONS INFORMATION

Measuring Response Time

The LT1016 is able to respond quickly to fast low level signals because it has a very high gain-bandwidth product ($\approx 50\text{GHz}$), even at very high frequencies. To properly measure the response of the LT1016 requires an input signal source with very fast rise times and exceptionally clean settling characteristics. This last requirement comes about because the standard comparator test calls for an input step size that is large compared to the overdrive amplitude. Typical test conditions are 100mV step size with only 5mV overdrive. This requires an input signal that settles to within 1% (1mV) of final value in only a few nanoseconds with no ringing or "long tailing". Ordinary high speed pulse generators are not capable of generating such a signal, and in any case, no ordinary oscilloscope is capable of displaying the waveform to check its fidelity. Some means must be used to inherently generate a fast, clean edge with known final value.

The circuit shown in Figure 1 is the best *electronic* means of generating a known fast, clean step to test comparators. It uses a very fast transistor in a common base configuration. The transistor is switched "off" with a fast edge from the generator and the collector voltage settles to exactly 0V in just a few nanoseconds. The most important feature of this circuit is the lack of feedthrough from the generator to the comparator input. This prevents overshoot on the comparator input which would give a false fast reading on comparator response time.

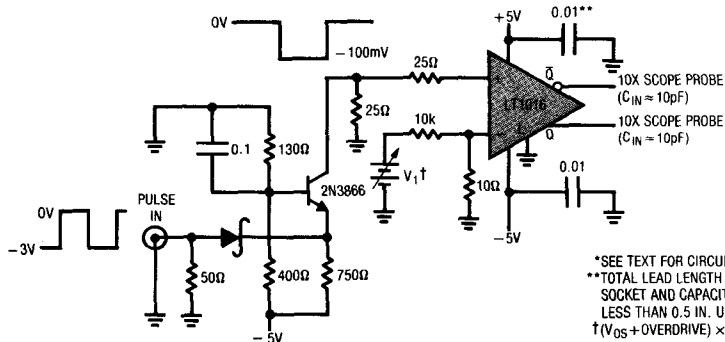
To adjust this circuit for exactly 5mV overdrive, V_1 is adjusted so that the LT1016 output under test settles to

1.4V (in the linear region). Then V_1 is *changed* -5V to set overdrive at 5mV.

The test circuit shown measures low to high transition on the "+" input. For opposite polarity transitions on the output, simply reverse the inputs of the LT1016.

High Speed Design Techniques

A substantial amount of design effort has made the LT1016 relatively easy to use. It is much less prone to oscillation and other vagaries than some slower comparators, even with slow input signals. In particular, the LT1016 is stable in its linear region, a feature no other high speed comparator has. Additionally, output stage switching does not appreciably change power supply current, further enhancing stability. These features make the application of the 50GHz gain-bandwidth LT1016 considerably easier than other fast comparators. Unfortunately, laws of physics dictate that the circuit *environment* the LT1016 works in must be properly prepared. The performance limits of high speed circuitry are often determined by parasitics such as stray capacitance, ground impedance, and layout. Some of these considerations are present in digital systems where designers are comfortable describing bit patterns and memory access times in terms of nanoseconds. The LT1016 can be used in such fast digital systems and Figure 2 shows just how fast the device is. The simple test circuit allows us to see that the LT1016's (Trace B)



*SEE TEXT FOR CIRCUIT EXPLANATION
 **TOTAL LEAD LENGTH INCLUDING DEVICE PIN,
 SOCKET AND CAPACITOR LEADS SHOULD BE
 LESS THAN 0.5 IN. USE GROUND PLANE
 † $(V_{OS} + \text{OVERDRIVE}) \times 1000$

Figure 1. Response Time Test Circuit

APPLICATIONS INFORMATION

response to the pulse generator (Trace A) is as fast as a TTL inverter (Trace C) even when the LT1016 has only millivolts of input signal! Linear circuits operating with this kind of speed make many engineers justifiably wary. Nanosecond domain linear circuits are widely associated with oscillations, mysterious shifts in circuit characteristics, unintended modes of operation and outright failure to function.

Other common problems include different measurement results using various pieces of test equipment, inability to make measurement connections to the circuit without inducing spurious responses and dissimilar operation between two "identical" circuits. If the components used in the circuit are good and the design is sound, all of the above problems can usually be traced to failure to provide a proper circuit "environment." To learn how to do this requires studying the causes of the aforementioned difficulties.

By far the most common error involves power supply bypassing. Bypassing is necessary to maintain low supply impedance. DC resistance and inductance in supply wires and PC traces can quickly build up to unacceptable levels. This allows the supply line to move as internal cur-

rent levels of the devices connected to it change. This will almost always cause unruly operation. In addition, several devices connected to an unbypassed supply can "communicate" through the finite supply impedances, causing erratic modes. Bypass capacitors furnish a simple way to eliminate this problem by providing a local reservoir of energy at the device. The bypass capacitor acts like an electrical flywheel to keep supply impedance low at high frequencies. The choice of what type of capacitors to use for bypassing is a critical issue and should be approached carefully. An unbypassed LT1016 is shown responding to a pulse input in Figure 3. The power supply the LT1016 sees at its terminals has high impedance at high frequency. This impedance forms a voltage divider with the LT1016, allowing the supply to move as internal conditions in the comparator change. This causes local feedback and oscillation occurs. Although the LT1016 responds to the input pulse, its output is a blur of 100MHz oscillation. *Always use bypass capacitors.*

In Figure 4 the LT1016's supplies are bypassed, but it still oscillates. In this case, the bypass units are either too far from the device or are lossy capacitors. *Use capacitors with good high frequency characteristics and mount*

6

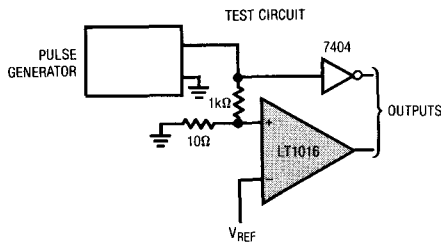


Figure 2. LT1016 vs a TTL Gate

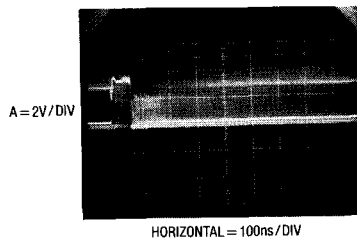
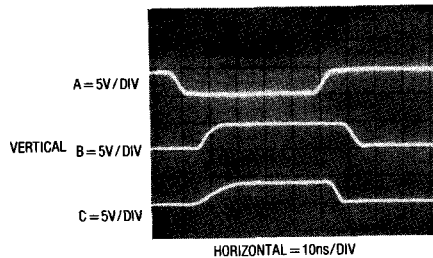


Figure 3. Unbypassed LT1016 Response

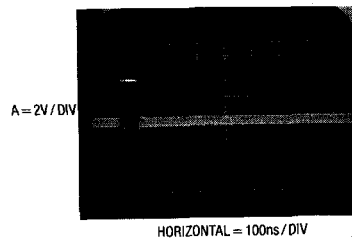


Figure 4. LT1016 Response with Poor Bypassing

APPLICATIONS INFORMATION

them as close as possible to the LT1016. An inch of wire between the capacitor and the LT1016 can cause problems. If operation in the linear region is desired, the LT1016 must be over a ground plate with good RF bypass capacitors ($\geq 0.01\mu F$) having lead lengths less than 0.2 inches. Do not use sockets.

In Figure 5 the device is properly bypassed but a new problem pops up. This photo shows both outputs of the comparator. Trace A appears normal, but Trace B shows an excursion of almost 8V — quite a trick for a device running from a +5V supply. This is a commonly reported problem in high speed circuits and can be quite confusing. It is not due to suspension of natural law, but is traceable to a grossly miscompensated or improperly selected oscilloscope probe. Use probes which match your oscilloscope's input characteristics and compensate them properly. Figure 6 shows another probe-induced problem. Here, the amplitude seems correct but the 10ns response time LT1016 appears to have 50ns edges! In this case, the

probe used is too heavily compensated or slow for the oscilloscope. Never use 1X or "straight" probes. Their bandwidth is 20MHz or less and capacitive loading is high. Check probe bandwidth to ensure it is adequate for the measurement. Similarly, use an oscilloscope with adequate bandwidth.

In Figure 7 the probes are properly selected and applied but the LT1016's output rings and distorts badly. In this case, the probe ground lead is too long. For general purpose work most probes come with ground leads about 6 inches long. At low frequencies this is fine. At high speed, the long ground lead looks inductive, causing the ringing shown. High quality probes are always supplied with some short ground straps to deal with this problem. Some come with very short spring clips which fix directly to the probe tip to facilitate a low impedance ground connection. For fast work, the ground connection to the probe should not exceed 1 inch in length. Keep the probe ground connection as short as possible.

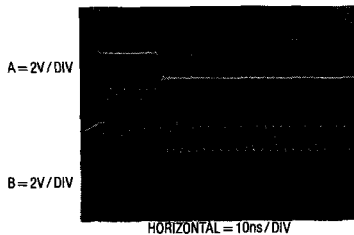


Figure 5. Improper Probe Compensation Causes Seemingly Unexplainable Amplitude Error

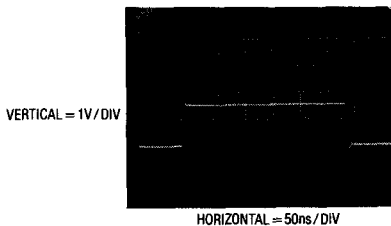


Figure 6. Overcompensated or Slow Probes Make Edges Look Too Slow

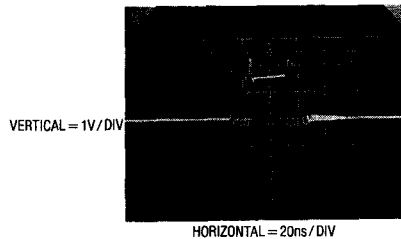


Figure 7. Typical Results Due to Poor Probe Grounding

APPLICATIONS INFORMATION

Figure 8 shows the LT1016's output (Trace B) oscillating near 40MHz as it responds to an input (Trace A). Note that the input signal shows artifacts of the oscillation. This example is caused by improper grounding of the comparator. In this case, the LT1016's ground pin connection is 1 inch long. The ground lead of the LT1016 must be as short as possible and connected directly to a low impedance ground point. Any substantial impedance in the LT1016's ground path will generate effects like this. The reason for this is related to the necessity of bypassing the power supplies. The inductance created by a long device ground lead permits mixing of ground currents, causing undesired effects in the device. The solution here is simple. *Keep the LT1016's ground pin connection as short (typically 1/4 inch) as possible and run it directly to a low impedance ground. Do not use sockets.*

Figure 9 addresses the issue of the "low impedance ground," referred to previously. In this example, the output is clean except for chattering around the edges. This photograph was generated by running the LT1016 without a "ground plane." A ground plane is formed by using a continuous conductive plane over the surface of the cir-

cuit board. The only breaks in this plane are for the circuit's necessary current paths. The ground plane serves two functions. Because it is flat (AC currents travel along the surface of a conductor) and covers the entire area of the board, it provides a way to access a low inductance ground from anywhere on the board. Also, it minimizes the effects of stray capacitance in the circuit by referring them to ground. This breaks up potential unintended and harmful feedback paths. *Always use a ground plane with the LT1016, when input signal levels are low or slow moving.*

"Fuzz" on the edges is the difficulty in Figure 10. This condition appears similar to Figure 10, but the oscillation is more stubborn and persists well after the output has gone low. This condition is due to stray capacitive feedback from the outputs to the inputs. A 3kΩ input source impedance and 3pF of stray feedback allowed this oscillation. The solution for this condition is not too difficult. *Keep source impedances as low as possible, preferably 1kΩ or less. Route output and input pins and components away from each other.*

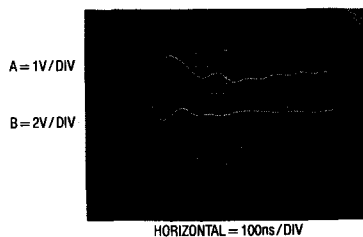


Figure 8. Excessive LT1016 Ground Path Resistance Causes Oscillation

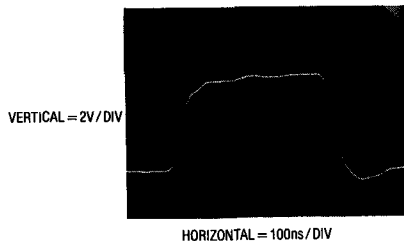


Figure 9. Transition Instabilities Due to No Ground Plane

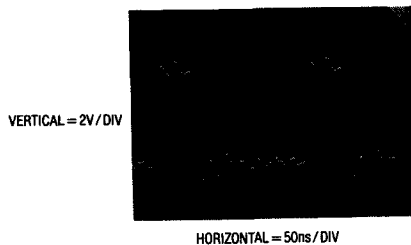


Figure 10. 3pF Stray Capacitive Feedback with 3kΩ Source Can Cause Oscillation

APPLICATIONS INFORMATION

The opposite of stray-caused oscillations appears in Figure 11. Here, the output response (Trace B) badly lags the input (Trace A). This is due to some combination of high source impedance and stray capacitance to ground at the input. The resulting RC forces a lagged response at the input, and output delay occurs. An RC combination of $2k\Omega$ source resistance and $10pF$ to ground gives a $20ns$ time constant — significantly longer than the LT1016's response time. *Keep source impedances low and minimize stray input capacitance to ground.*

Figure 12 shows another capacitance-related problem. Here the output does not oscillate, but the transitions are discontinuous and relatively slow. The villain of this situation is a large output load capacitance. This could be caused by cable driving, excessive output lead length or the input characteristics of the circuit being driven. In most situations this is undesirable and may be eliminated by buffering heavy capacitive loads. In a few cir-

cumstances it may not affect overall circuit operation and is tolerable. *Consider the comparator's output load characteristics and their potential effect on the circuit. If necessary, buffer the load.*

Another output-caused fault is shown in Figure 13. The output transitions are initially correct but end in a ringing condition. The key to the solution here is the ringing. What is happening is caused by an output lead which is too long. The output lead looks like an unterminated transmission line at high frequencies and reflections occur. This accounts for the abrupt reversal of direction on the leading edge and the ringing. If the comparator is driving TTL this may be acceptable, but other loads may not tolerate it. In this instance, the direction reversal on the leading edge might cause trouble in a fast TTL load. *Keep output lead lengths short. If they get much longer than a few inches, terminate with a resistor (typically 250Ω – 400Ω).*

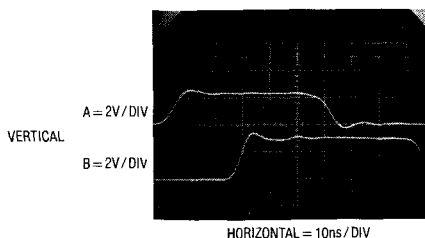


Figure 11. Stray 5pF Capacitance from Input to Ground Causes Delay

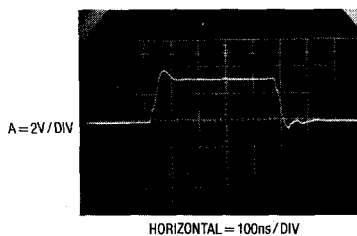


Figure 12. Excessive Load Capacitance Forces Edge Distortion

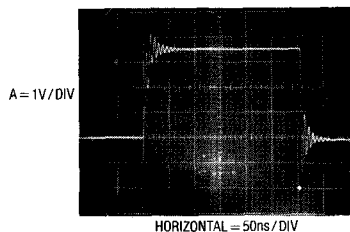


Figure 13. Lengthy, Unterminated Output Lines Ring from Reflections

APPLICATIONS INFORMATION

200ns-0.01% Sample-and-Hold Circuit

Figure 14's circuit uses the LT1016's high speed to improve upon a standard circuit function. The 200ns acquisition time is well beyond monolithic sample-and-hold capabilities. Other specifications exceed the best commercial unit's performance. This circuit also gets around many of the problems associated with standard sample-and-hold approaches, including FET switch errors and amplifier settling time. To achieve this, the LT1016's high speed is used in a circuit which completely abandons traditional sample-and-hold methods.

Important specifications for this circuit include:

Acquisition Time	< 200ns
Common-Mode Input Range	±3V
Droop	1μV/μs
Hold Step	2mV
Hold Settling Time	15ns
Feedthrough Rejection	>> 100dB

When the sample-hold line goes low, a linear ramp starts just below the input level and ramps upward. When the ramp voltage reaches the input voltage, A1 shuts off the ramp, latches itself off, and sends out a signal indicating sampling is complete.

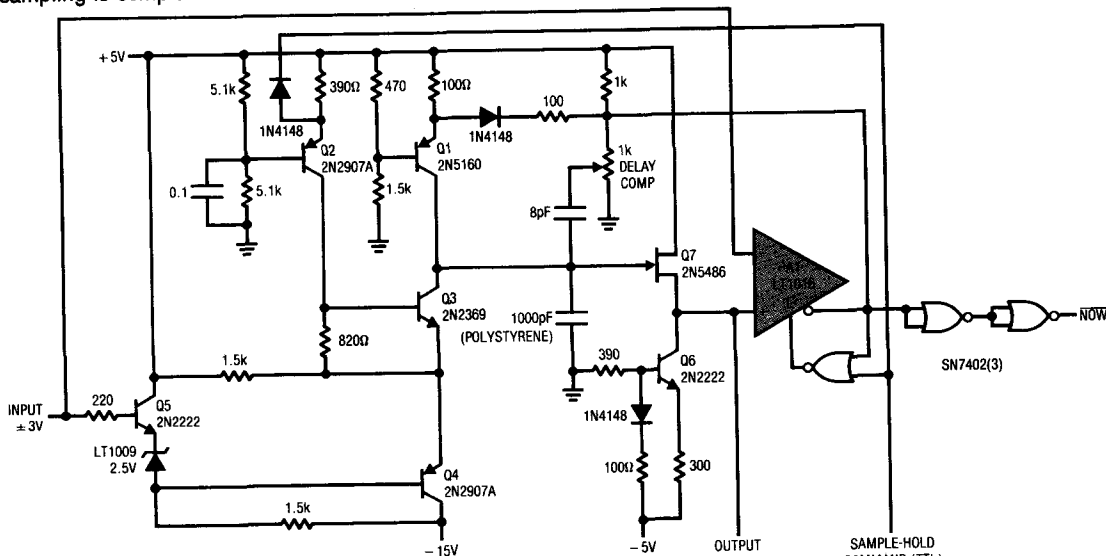


Figure 14. 200ns Sample-and Hold

1.8μs, 12-Bit A-D Converter

The LT1016's high speed is used to implement a very fast 12-bit A-D converter in Figure 15. The circuit is a modified form of the standard successive approximation approach and is faster than most commercial SAR 12-bit units. In this arrangement the 2504 successive approximation register (SAR), A1 and C1 test each bit, beginning with the MSB, and produce a digital word representing V_{IN} 's value. To get faster conversion time, the clock is controlled by the window comparator monitoring the DAC-input summing junction. Additionally, the DMOS FET clamps the DAC output to ground at the beginning of each clock cycle, shortening DAC settling time. After the fifth bit is converted, the clock runs at maximum speed.

1Hz-10MHz V→F Converter

The LT1016 and the LT1012 low drift amplifier combine to form a high speed V→F converter in Figure 16. A variety of circuit techniques is used to achieve a 1Hz to 10MHz output. Overrange to 12MHz ($V_{IN}=12V$) is provided. This circuit has a wider dynamic range (140dB, or 7 decades) than any commercially available unit. The 10MHz full-scale frequency is 10 times faster than currently available monolithic V→F's. The theory of operation is based on the identity $Q = CV$.

APPLICATIONS INFORMATION

Each time the circuit produces an output pulse, it feeds back a fixed quantity of charge (Q) to a summing node (Σ). The circuit's input furnishes a comparison current at the summing node. The difference signal at the node is integrated in a monitoring amplifier's feedback capacitor. The amplifier controls the circuit's output pulse generator, completing a feedback loop around the integrating amplifier. To maintain the summing node at zero, the pulse generator runs at a frequency which

permits enough charge pumping to offset the input signal. Thus, the output frequency will be linearly related to the input voltage. A1 is the integrating amplifier.

To trim this circuit, ground the input and adjust the 1k pot for 1Hz output. Next, apply 10.000V and set the 2k Ω unit for 10.000MHz output. The transfer linearity of the circuit is 0.06%. Full-scale drift is typically 50ppm/ $^{\circ}$ C and zero point error about 0.2 μ V/ $^{\circ}$ C (0.2Hz/ $^{\circ}$ C).

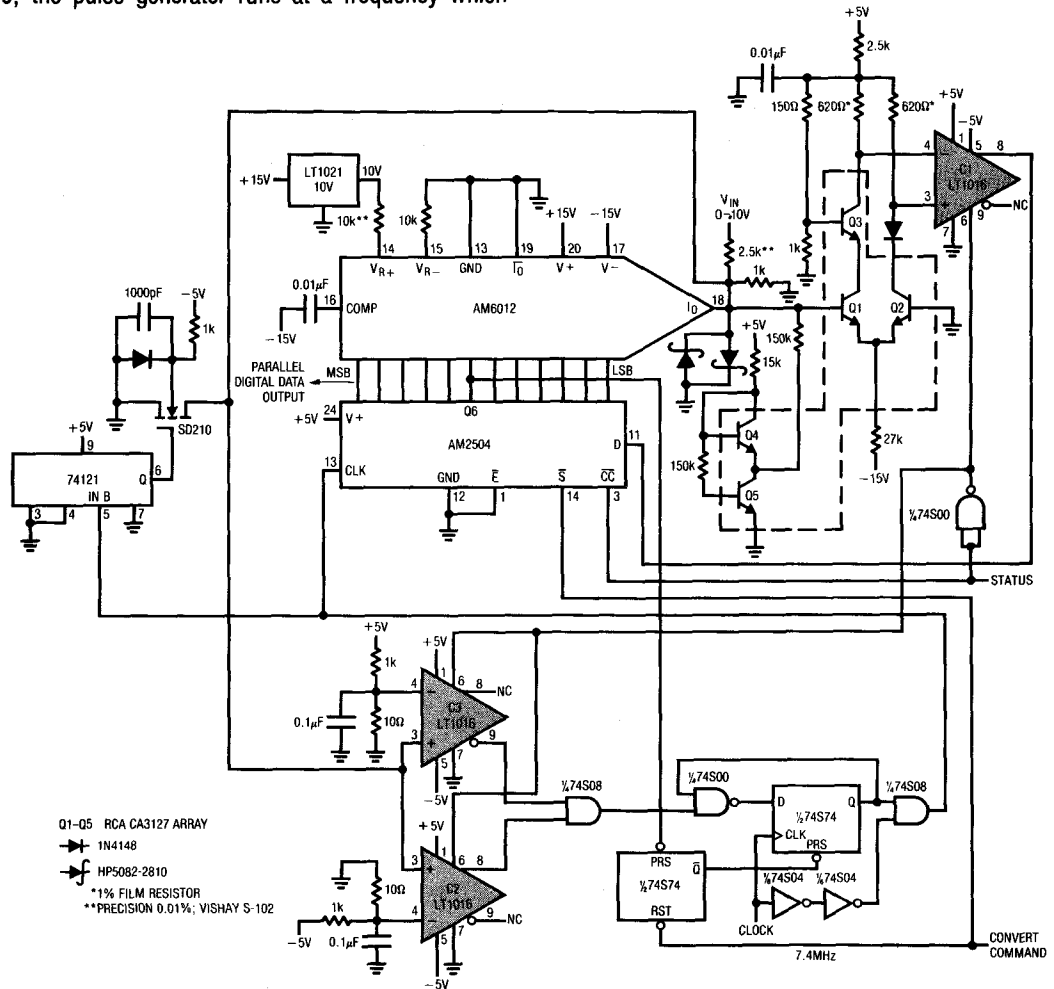
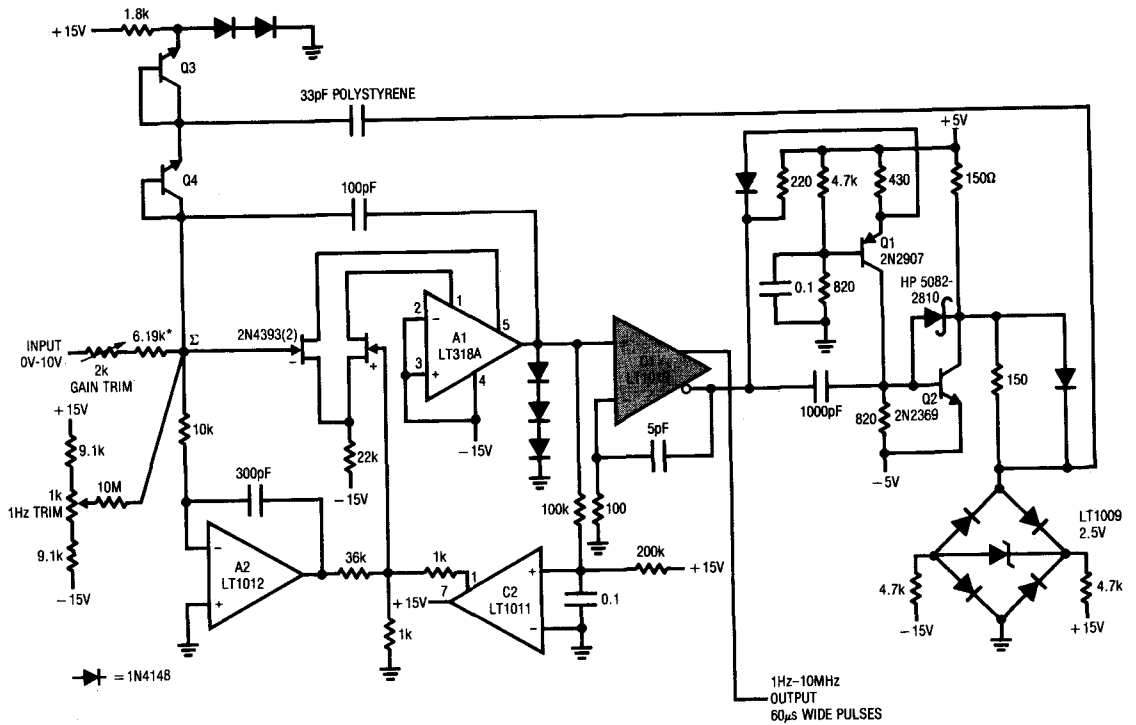


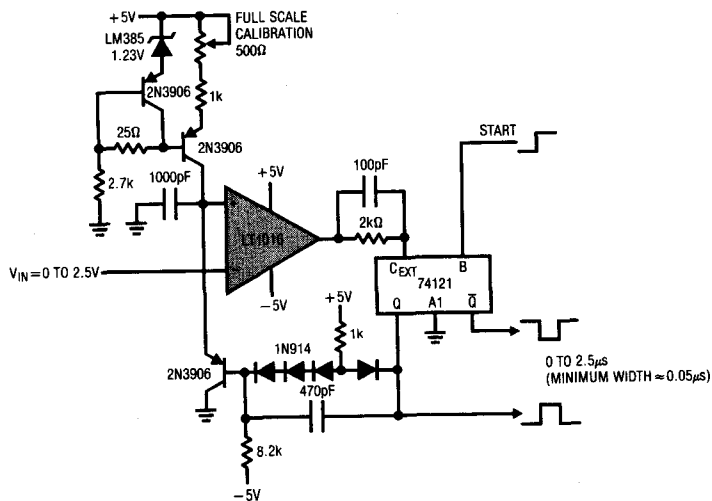
Figure 15. 12-Bit 1.8 μ s SAR A-D

APPLICATIONS INFORMATION

1Hz-10MHz V to F Converter

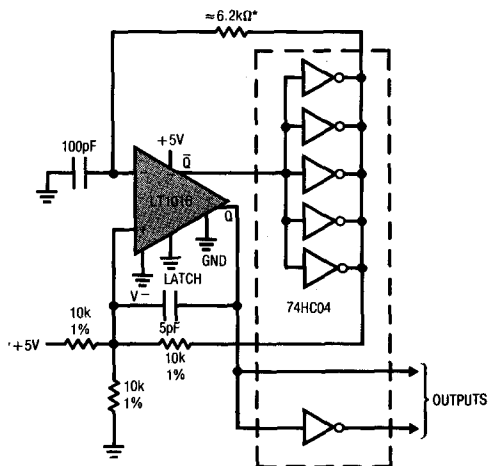


Voltage Controlled Pulse Width Generator



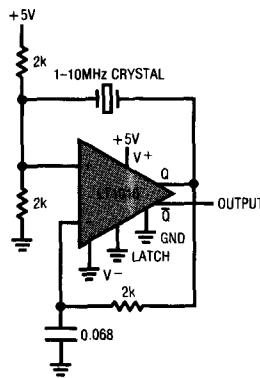
APPLICATIONS INFORMATION

Single Supply Precision RC 1MHz Oscillator



*SELECT OR TRIM FOR $f = 1.00\text{MHz}$

1-10MHz Crystal Oscillator



APPENDIX A

About Level Shifts

The TTL output of the LT1016 will interface with many circuits directly. Many applications, however, require some form of level shifting of the output swing. With LT1016-based circuits this is not trivial because it is desirable to maintain very low delay in the level shifting stage. When designing level shifters, keep in mind that the TTL output of the LT1016 is a sink-source pair (Figure A1) with good ability to drive capacitance (such as feedforward capacitors).

Figure A2 shows a non-inverting voltage gain stage with a 15V output. When the LT1016 switches, the base-emitter voltages at the 2N2369 reverse, causing it to switch very quickly. The 2N3866 emitter-follower gives a low im-

pedance output and the Schottky diode aids current sink capability.

Figure A3 is a very versatile stage. It features a bipolar swing which may be programmed by varying the output transistor's supplies. This 3ns delay stage is ideal for driving FET switch gates. Q1, a gated current source, switches the Baker-clamped output transistor, Q2. The heavy feedforward capacitor from the LT1016 is the key to low delay, providing Q2's base with nearly ideal drive. This capacitor loads the LT1016's output transition (Trace A, Figure A4), but Q2's switching is clean (Trace B, Figure A4) with 3ns delay on the rise and fall of the pulse.

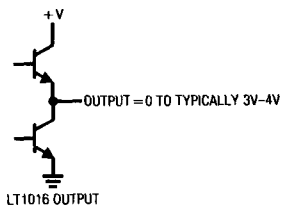


Figure A1

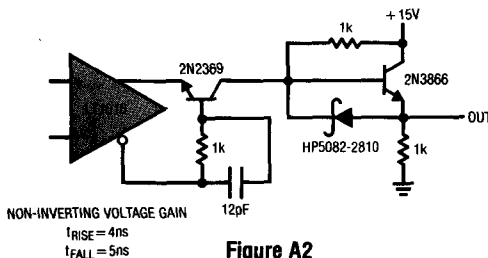


Figure A2

APPENDIX A

Figure A5 is similar to A2 except that a sink transistor has replaced the Schottky diode. The two emitter-followers drive a power MOSFET which switches 1A at 15V. Most of the 7ns–9ns delay in this stage occurs in the MOSFET and the 2N2369.

When designing level shifters, remember to use transistors with fast switching times and high f_T 's. To get the kind of results shown, switching times in the ns range and f_T 's approaching 1GHz are required.

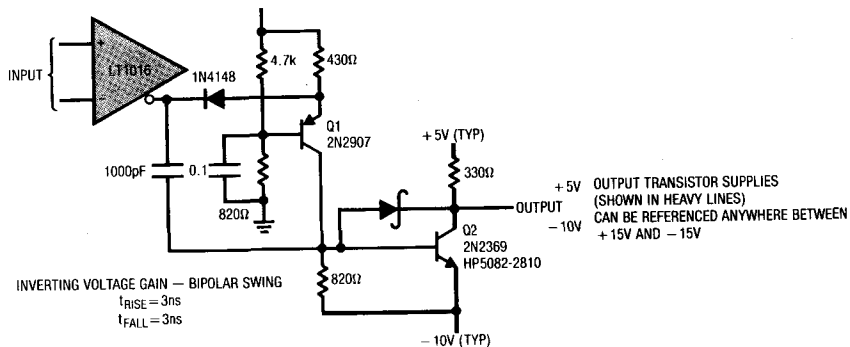


Figure A3

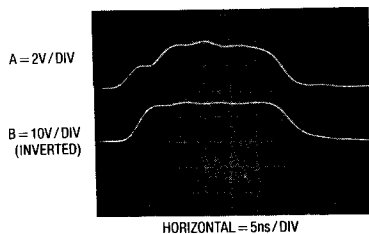


Figure A4. Figure A3's Waveforms

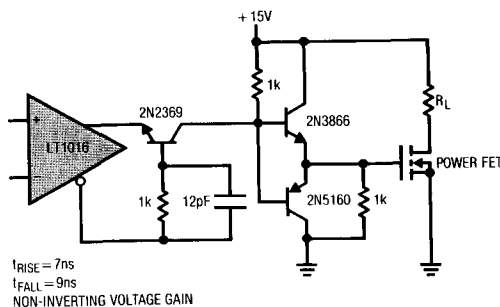
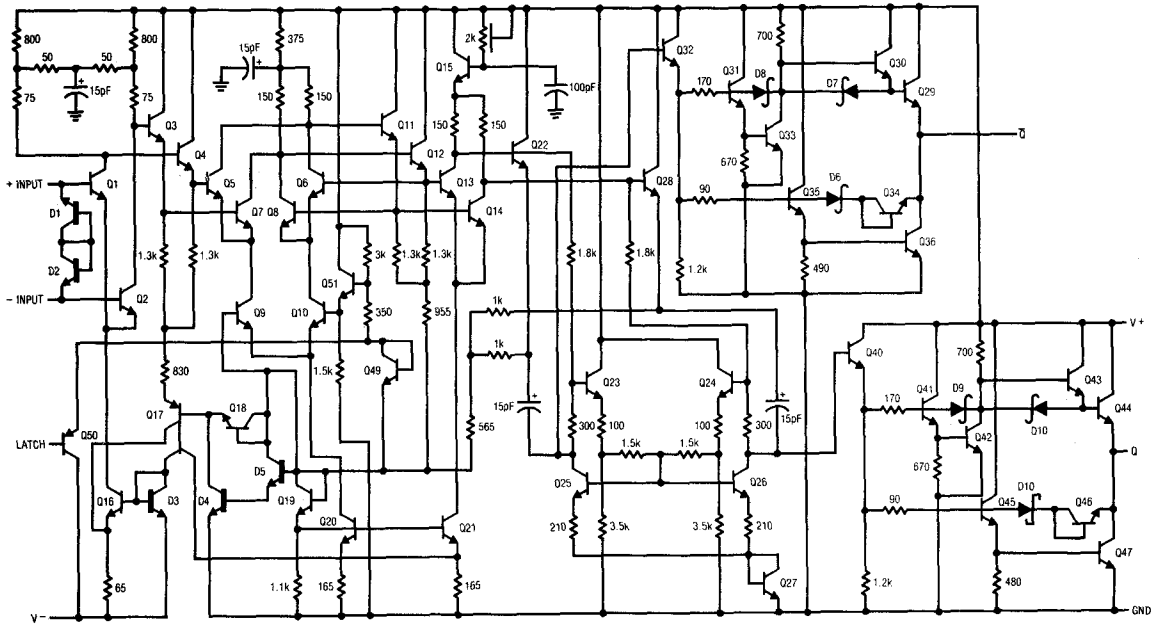


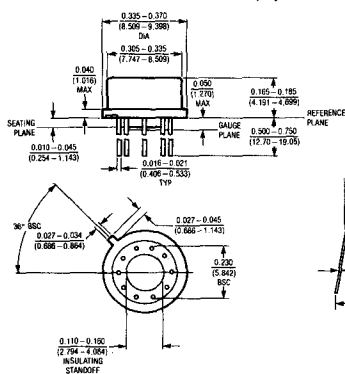
Figure A5

SCHEMATIC DIAGRAM



PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

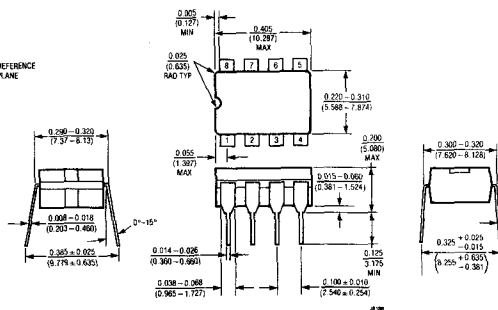
10 Lead TO-5 Metal Can (H)



NOTE: 1. LEAD DIAMETER IS UNCONTROLLED BETWEEN THE REFERENCE PLANE AND SEATING PLANE.

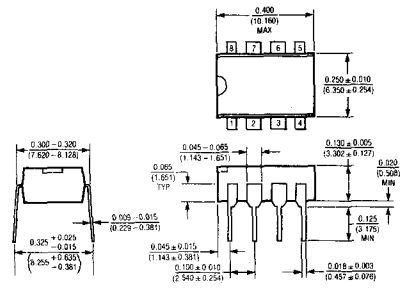
T_j max	θ_{ja}	θ_{jc}
150°C	150°C/W	45°C/W

**J8 Package
8 Lead Hermetic Dip**



T_j max	θ_{ja}
150°C	100°C/W

**N8 Package
8 Lead Plastic**



T_j max	θ_{ja}
100°C	130°C/W

FEATURES

- Ultra Fast (10ns typ)
- Operates Off **Single** +5V Supply, or $\pm 5V$
- Complementary Output to TTL
- Low Offset Voltage
- No Minimum Input Slew Rate Requirement
- No Power Supply Current Spiking
- Output Latch Capability

APPLICATIONS

- High Speed A to D Converters
- High Speed Sampling Circuits
- Line Receiver
- Extended Range V to F Converters
- Fast Pulse Height/Width Discriminators

DESCRIPTION

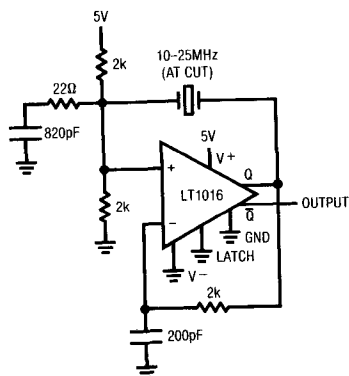
The LT1016 is an ultra fast (10ns) comparator specifically designed to interface directly to TTL logic while operating off either a dual $\pm 5V$ supply or a single +5V supply. Tight offset voltage specifications and high gain allow the LT1016 to be used in precision applications. Matched complementary outputs further extend the versatility of this new comparator.

A unique output stage is featured on the LT1016. It provides active drive in both directions for maximum speed into TTL logic or passive loads, yet does not exhibit the large current spikes normally found in "totem pole" output stages. This eliminates the need for a minimum input slew rate typical of other very fast comparators. The ability of the LT1016 to remain stable with the outputs in the active region greatly reduces the problem of output "glitching" when the input signal is slow moving or is low level.

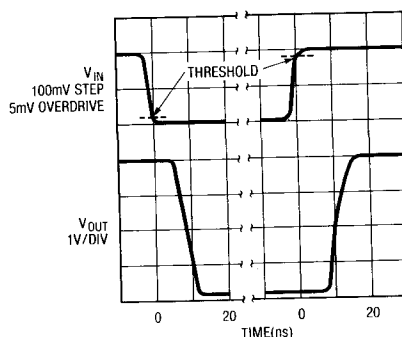
The LT1016 has a true latch pin for retaining input data at the outputs. The outputs will remain latched as long as the latch pin is held high. Quiescent negative power supply current is only 3mA — about ten times lower than competitive units. This reduces die temperature and allows the negative supply pin to be driven from virtually any supply voltage with a simple resistive divider. Device performance is not affected by variations in negative supply voltage.

6

10-25MHz Crystal Oscillator

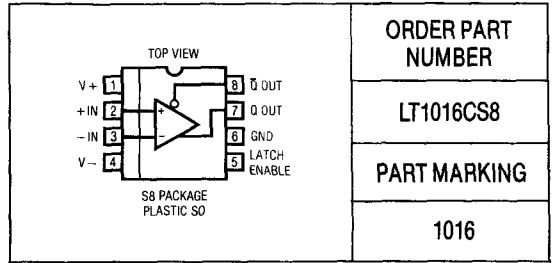


Response Time



ABSOLUTE MAXIMUM RATINGS **PACKAGE/ORDER INFORMATION**

Positive Supply Voltage (Note 4) 7V
 Negative Supply Voltage 7V
 Differential Input Voltage ± 5V
 Input Voltage (Either Input) Equal to Supplies
 Latch Pin Voltage Equal to Supplies
 Output Current (Continuous) ± 20mA
 Operating Temperature Range 0°C to 70°C
 Storage Temperature Range - 65°C to 150°C
 Lead Temperature (Soldering, 10 sec.) 300°C



ELECTRICAL CHARACTERISTICS

V⁺ = 5V, V⁻ = 5V, V_{OUT(Q)} = 1.4V, V_{LATCH} = 0V, T_A = 25°C, unless otherwise noted.

SYMBOL	PARAMETERS	CONDITIONS	LT1016C			UNITS
			MIN	TYP	MAX	
V _{OS}	Input Offset Voltage	R _S ≤ 100Ω (Note 1)	•	1.0	± 3	mV
$\frac{\Delta V_{OS}}{\Delta T}$	Input Offset Voltage Drift		•	4	± 3.5	μV/°C
I _{OS}	Input Offset Current	(Note 1)	•	0.3	1	μA
I _B	Input Bias Current	(Note 2)	•	0.3	1.3	μA
	Input Voltage Range	(Note 5)	•	- 3.75	+ 3.5	V
		Single +5V Supply	•	+ 1.25	+ 3.5	V
CMRR	Common-Mode Rejection	- 3.75V ≤ V _{CM} ≤ + 3.5V	•	80	96	dB
PSRR	Supply Voltage Rejection	Positive Supply 4.6V ≤ V ⁺ ≤ 5.4V	•	60	75	dB
		Negative Supply 2V ≤ V ⁻ ≤ 7V	•	80	100	dB
A _v	Small Signal Voltage Gain	1V ≤ V _{OUT} ≤ 2V		1400	3000	V/V
V _{OH}	Output High Voltage	V ⁺ ≥ 4.6V, I _{OUT} = 1mA I _{OUT} = 10mA	•	2.7	2.9	V
			•	2.4	2.8	V
V _{OL}	Output Low Voltage	I _{SINK} = 4mA I _{SINK} = 10mA	•	0.3	0.5	V
			•	0.4		V
I ⁺	Positive Supply Current		•	25	35	mA
I ⁻	Negative Supply Current		•	3	5	mA
V _{IH}	Latch Pin Hi Input Voltage		•	2.0		V
V _{IL}	Latch Pin Lo Input Voltage		•		0.8	V
I _{IL}	Latch Pin Current	V _{LATCH} = 0V	•		500	μA

ELECTRICAL CHARACTERISTICS

$V^+ = 5V$, $V^- = 5V$, $V_{OUT(Q)} = 1.4V$, $V_{LATCH} = 0V$, $T_A = 25^\circ C$, unless otherwise noted.

SYMBOL	PARAMETERS	CONDITIONS	LT1016C			UNITS
			MIN	TYP	MAX	
t_{PD}	Propagation Delay (Note 3)	$\Delta V_{IN} = 100mV$, $OD = 5mV$	●	10	14 16	ns ns
		$\Delta V_{IN} = 100mV$, $OD = 20mV$	●	9	12 15	ns ns
Δt_{PD}	Differential Propagation Delay	(Note 3) $\Delta V_{IN} = 100mV$, $OD = 5mV$			3	ns
	Latch Setup Time			2		ns

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: Input offset voltage is defined as the average of the two voltages measured by forcing first one output, then the other to 1.4V. Input offset current is defined in the same way.

Note 2: Input bias current (I_B) is defined as the average of the two input currents.

Note 3: Propagation delay is measured with the overdrive added to actual V_{OS} . Guaranteed but not tested.

Note 4: Electrical specifications apply only up to 5.4V.

Note 5: See text for discussion of input voltage range for supplies other than $\pm 5V$, or $+5V$.

NOTES

FEATURES

- Maximum Offset Voltage 1mV
- Maximum Bias Current 15nA
- Typical Output Drive 70mA
- Operates from 1.1V to 40V
- Internal Pull-Up Current
- Output Can Drive Loads Above V^+
- 30 μ A Supply Current (LT1017)
- 110 μ A Supply Current (LT1018)

APPLICATIONS

- Power Supply Monitors
- Relay Driving
- Oscillators

DESCRIPTION

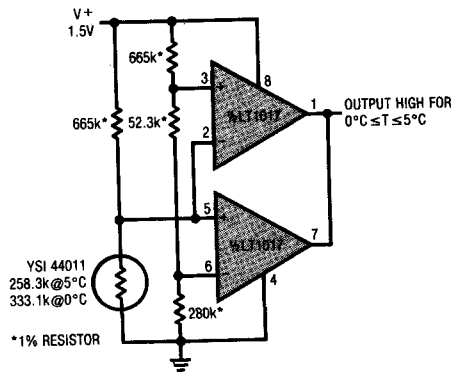
The LT1017 and LT1018 are general purpose micropower comparators. The LT1017 is optimized for lowest operating power while the LT1018 operates at higher power and higher speed. Both devices can operate from a single 1.1V cell up to 40V. The output stage includes a class "B" pull-up current source, eliminating the need for an external resistive pull-up and saving power. The output stage is also designed to allow driving loads connected to a supply more positive than the device, as can comparators with open collector output stages.

Input specifications are also excellent. On-chip trimming minimizes offset voltage, while high gain and common-mode rejection keep other input-referred errors low. Common-mode voltage range includes ground. Special circuitry prevents false output states even if the input is overdriven.

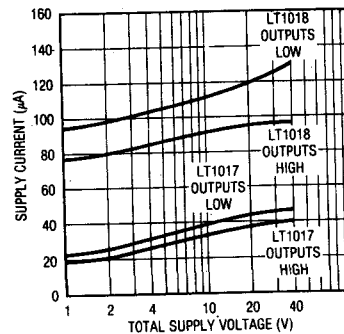
The LT1017 and LT1018 are pin compatible with older dual comparators such as 393 type devices.

REFER TO TABLE OF CONTENTS FOR REVISED DATA LOCATION

1.5V Powered Refrigerator Alarm



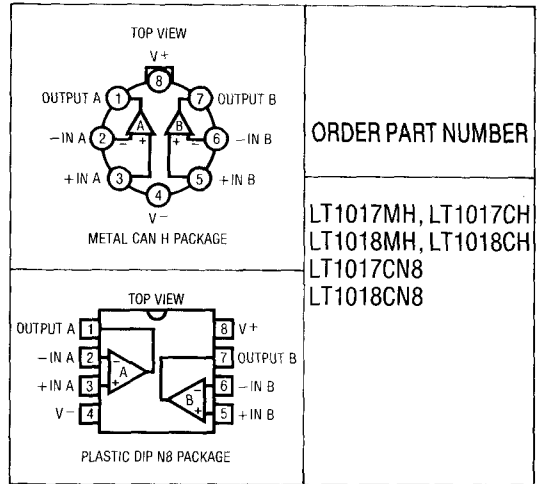
Supply Current



ABSOLUTE MAXIMUM RATINGS

Supply Voltage 40V
 Differential Input Voltage 40V
 Input Voltage -0.3V to 40V
 Short Circuit Duration Indefinite
 Operating Temperature Range
 LT1017M, LT1018M -55°C to 125°C
 LT1017C, LT1018C 0°C to 70°C
 Storage Temperature Range -65°C to 150°C
 Lead Temperature (Soldering, 10 sec) 300°C

PACKAGE/ORDER INFORMATION



ELECTRICAL CHARACTERISTICS

PARAMETER	CONDITIONS	LT1017			LT1018			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Offset Voltage (Note 1)	$\pm 0.75V \leq V_S \leq \pm 20V$	25°C	0.4	1	0.4	1	mV	
		● 125°C	0.5	1.4	0.5	1.4	mV	
Bias Current	$\pm 0.75V \leq V_S \leq \pm 20V$	25°C	5	15	15	75	nA	
		● 125°C	7	25	18	100	nA	
Offset Current	$\pm 0.75V \leq V_S \leq \pm 20V$	25°C	0.4	2	1	8	nA	
		● 125°C	0.5	3	1.6	12	nA	
Common-Mode Rejection Ratio	$V_S = \pm 20V, -20V \leq V_{CM} \leq 19.1V$	25°C	105	115	105	115	dB	
		● 125°C	100	115	100	115	dB	
Power Supply Rejection Ratio	$\pm 0.75V \leq V_S \leq \pm 20V$	25°C	96	110	96	110	dB	
		● 125°C	95	105	95	105	dB	
Gain	No Load, $V_{OUT} = \pm 19.9V$ (Note 2)	25°C	110	115	110	125	dB	
		● 125°C	105	115	105	120	dB	
Output Sink Current	$V^+ = 4.5V, V^- = 0$ Overdrive > 30mV	25°C	30	65	35	70	mA	
		● 125°C	25	50	25	50	mA	
Output Source Current	$V^+ = 40V, V^- = 0$ $V_{IN} = 5mV, V_{OUT} = 0.4V$	25°C	30	75	75	250	μA	
		● 125°C	25	70	50	220	μA	
Output Source Current	$V^+ = 1.2V, V^- = 0$ $V_{IN} = 5mV, V_{OUT} = 0.4V$	25°C	25	35	70	140	μA	
		● 125°C	15	20	45	120	μA	
Output Source Current	$V^+ = 1.2V, V^- = 0$ $V_{IN} = 5mV, V_{OUT} = 0.4V$	25°C	25	40	40	110	μA	
		● 125°C	25	40	40	110	μA	

ELECTRICAL CHARACTERISTICS

PARAMETER	CONDITIONS	LT1017			LT1018			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Negative Output Saturation	$I_{OUT} = 0$ $V^+ = 4.5V, V^- = 0$ $V_{IN} = -10mV$ $I_{OUT} = 0.1mA$ $I_{OUT} = 1mA$ $I_{OUT} = 10mA$ $I_{OUT} = 30mA$	25°C	5	20	5	15	mV	
		25°C	35	60	35	60	mV	
		25°C	60	120	60	120	mV	
		25°C	120	200	120	250	mV	
		25°C	350	600	350	700	mV	
		25°C	5	20	8	20	mV	
	$I_{OUT} = 0$ $I_{OUT} = 0.1mA$ $I_{OUT} = 1mA$ $I_{OUT} = 10mA$ $I_{OUT} = 30mA$	●	40	75	35	70	mV	
		●	75	150	70	150	mV	
		●	150	300	150	300	mV	
		●	600	900	500	900	mV	
		125°C	25	50	10	40	mV	
		125°C	60	100	60	100	mV	
Positive Output Saturation	$I_{OUT} = 0$ $I_{OUT} = 10\mu A$ $I_{OUT} = 0$	25°C	40	80	35	80	mV	
		25°C	175	250	175	250	mV	
		●	45	90	45	90	mV	
	$I_{OUT} = 0$ $I_{OUT} = 10\mu A$ $I_{OUT} = 0$	●	190	300	190	300	mV	
		125°C	50	100	50	100	mV	
		125°C	300	300	300	300	mV	
Leakage Current	$V_S = 5V, V_{OUT} = 40V$ $V_{IN} \geq 100mV$	25°C	0.5	3	1	8	μA	
		●	0.6	3	1.8	10	μA	
		125°C		5		15	μA	
Supply Current	$V_S = 5V$	25°C	30	60	110	250	μA	
		●	40	80	110	250	μA	
		125°C		80		300	μA	
	$V_S = 40V$	25°C	40	90	130	250	μA	
		●	55	100	140	270	μA	
		125°C		100		300	μA	
Minimum Operating Voltage	$I_{OUT} = 1mA$	25°C		1.15		1.2	V	
		●		1.15		1.2	V	
		125°C		1.15		1.2	V	

The ● denotes specifications which apply over operating temperature range of -55°C to 85°C for M grade parts and 0°C to 70°C for C grade parts.

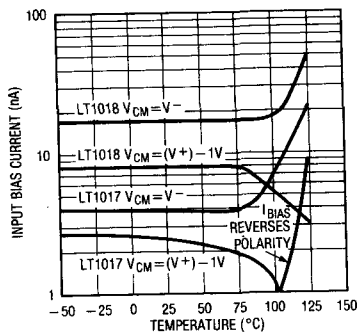
Note 1: Offset voltage is guaranteed over a common-mode voltage range of $V^- \leq V_{IN} \leq (V^+ - 0.9V)$.

Note 2: No load gain is guaranteed but not tested (LT1017 only).

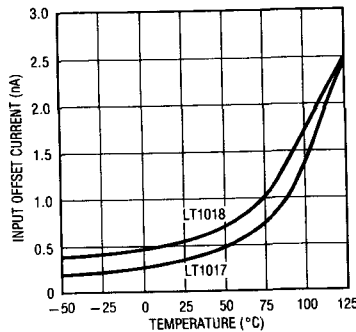
6

TYPICAL PERFORMANCE CHARACTERISTICS

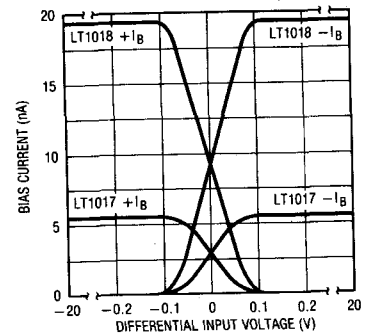
Input Bias Current



Input Offset Current

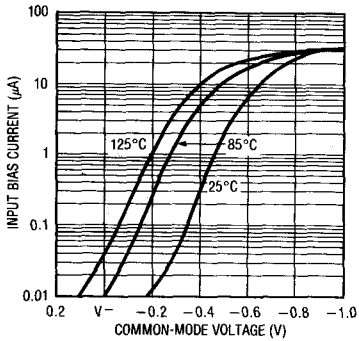


Bias Current vs Differential Input

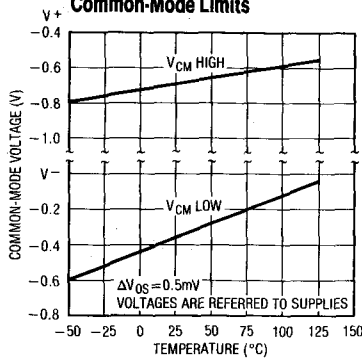


TYPICAL PERFORMANCE CHARACTERISTICS

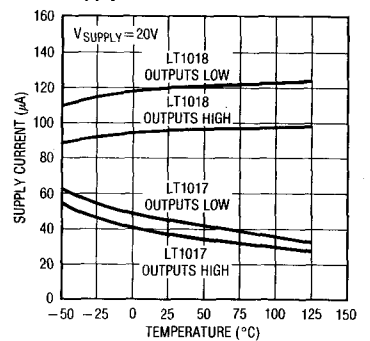
Input Bias Current with Inputs Driven Below the Supply



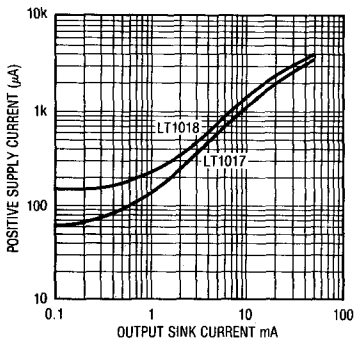
Common-Mode Limits



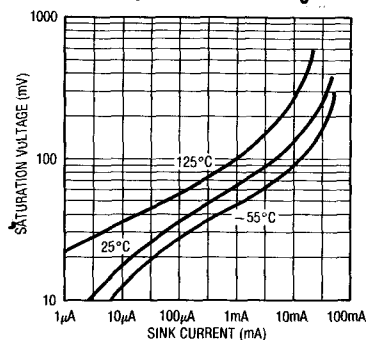
Supply Current



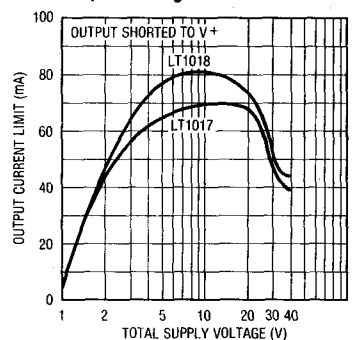
Positive Supply Current



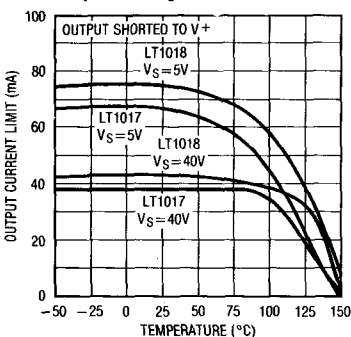
NPN Output Saturation Voltage



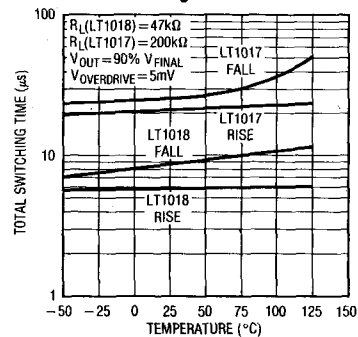
Output Sinking Current Limit



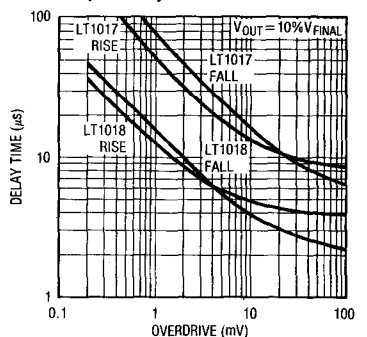
Output Sinking Current Limit



Total Switching Time

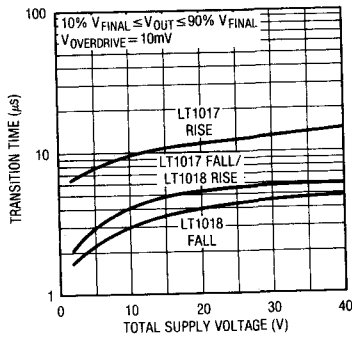


Output Delay

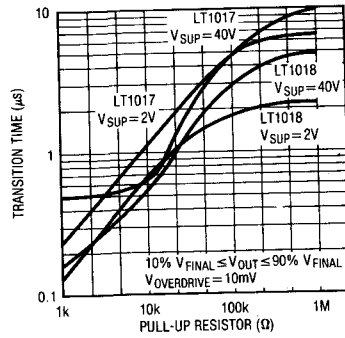


TYPICAL PERFORMANCE CHARACTERISTICS

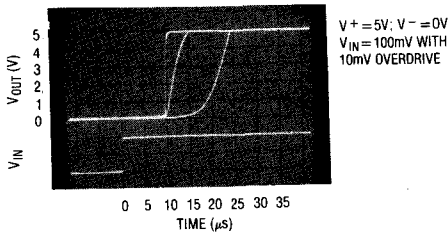
Transition Time



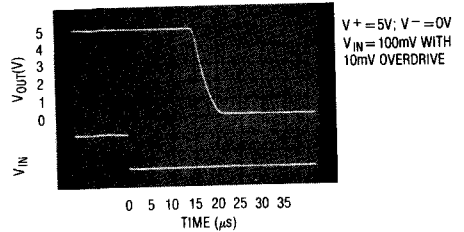
Positive Transition Time



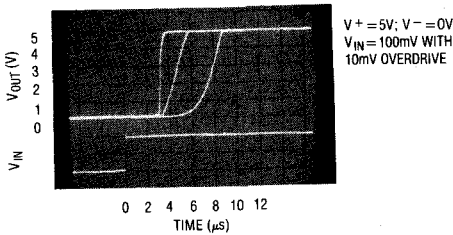
LT1017 Response Time



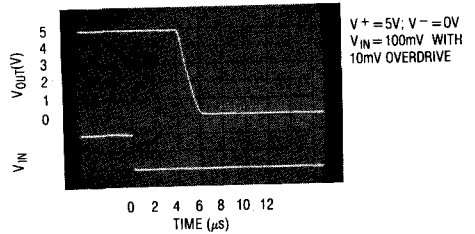
LT1017 Response Time



LT1018 Response Time



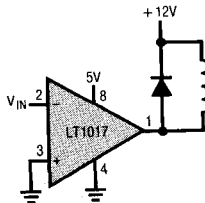
LT1018 Response Time



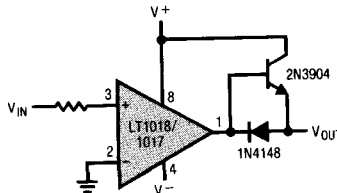
6

APPLICATIONS

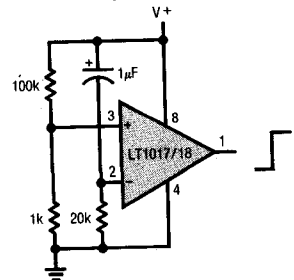
Driving Relays



Increasing Positive Output Current

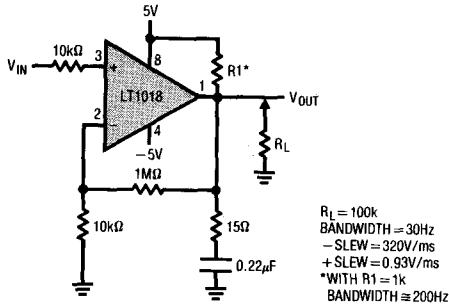


Delay On Power Up

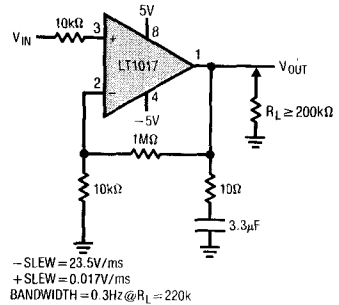


APPLICATIONS

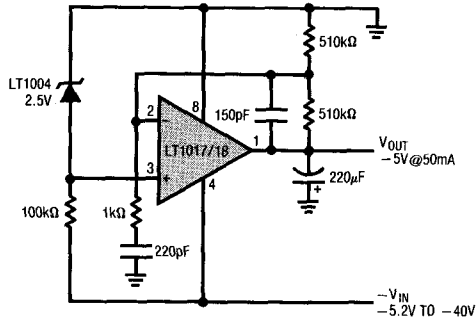
LT1018 Op Amp, $A_V = 100$



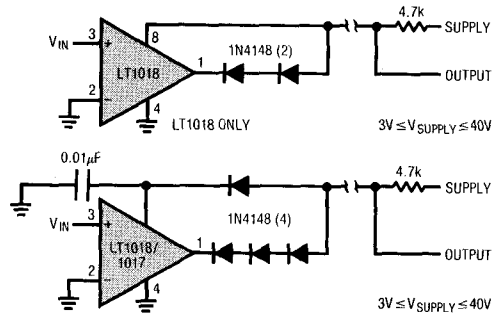
LT1017 Op Amp, $A_V = 100$



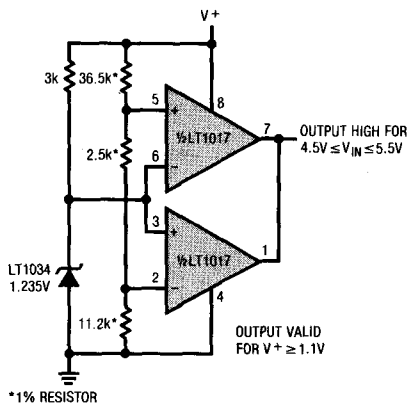
Negative Voltage Regulator



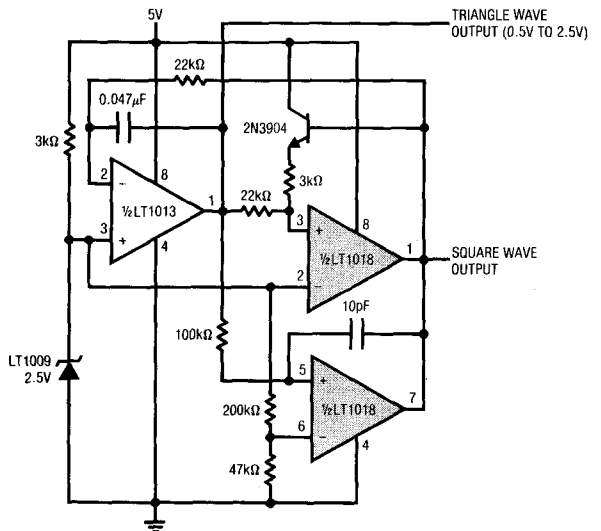
2-Wire Comparator



5V Power Supply Monitor

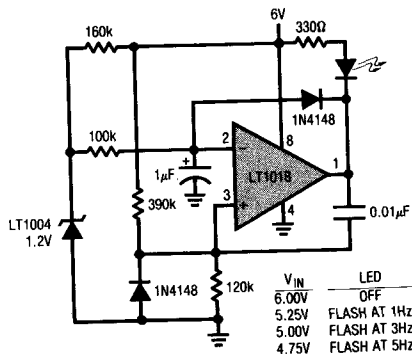


Precise Tri-Wave Generator

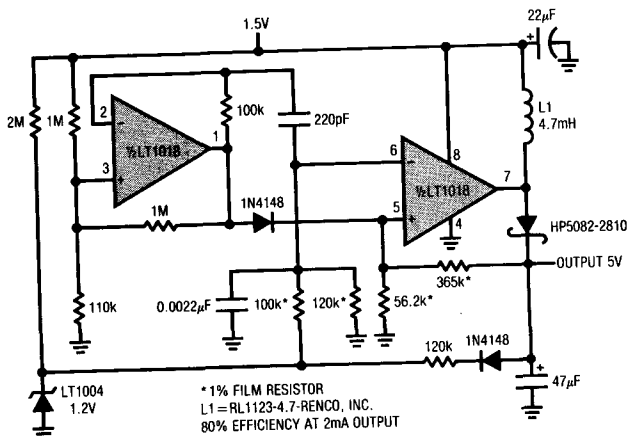


APPLICATIONS

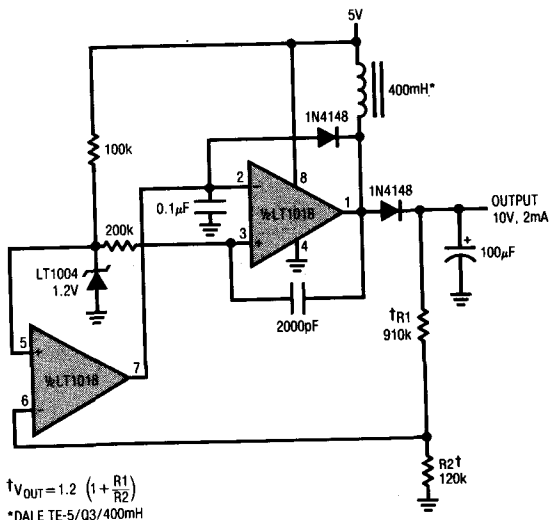
Power Supply Monitor



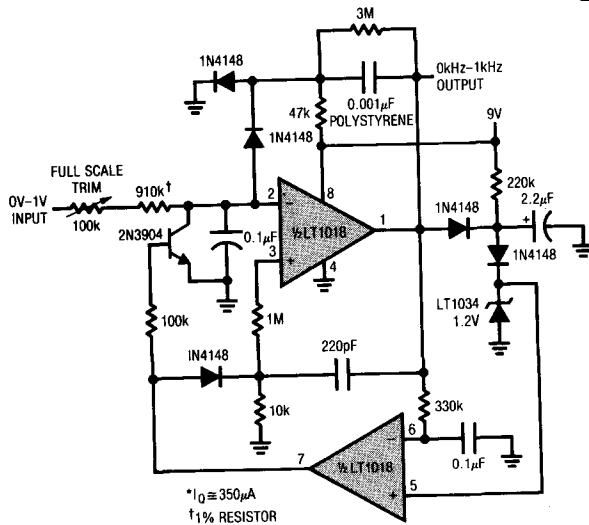
1.5V Input Flyback Regulator



Regulated Up Converter



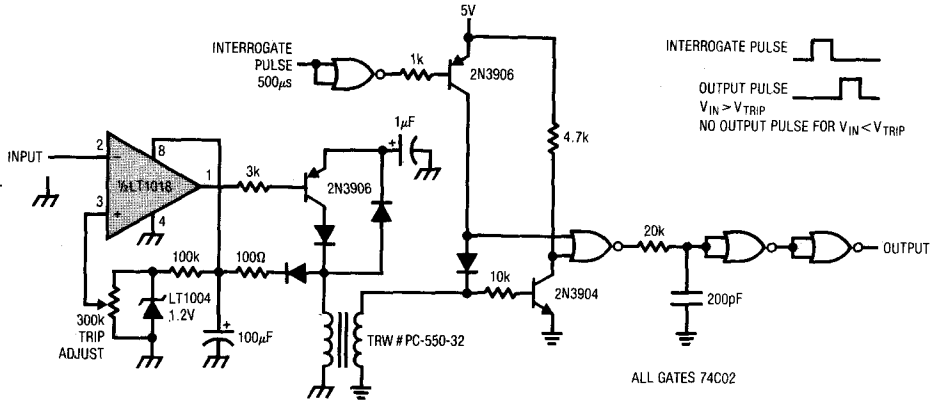
Low Power* V to F Converter



6

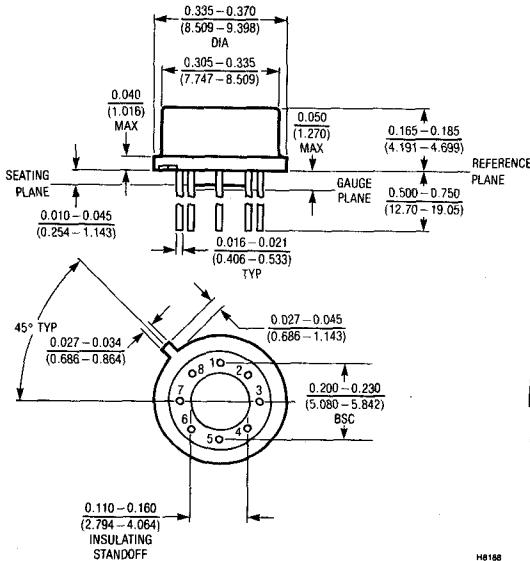
APPLICATIONS

Fully Isolated Limit Comparator



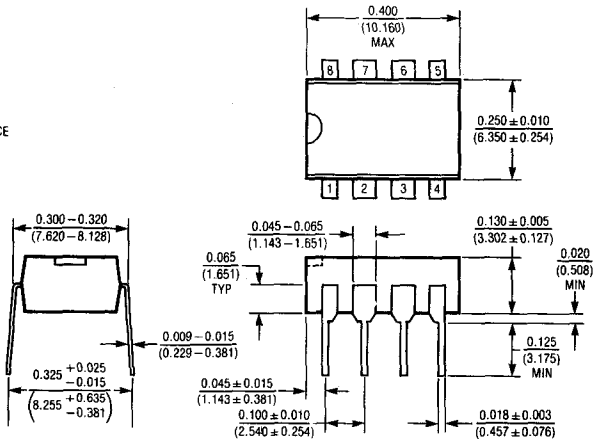
PACKAGE DESCRIPTION

H Package
8-Lead TO-5 Metal Can



T _J max	θ _{JA}	θ _{JC}
150°C	150°C/W	45°C/W

N Package
8-Lead Plastic DIP



T _J max	θ _{JA}
100°C	130°C/W

FEATURES

- Maximum Offset Voltage
- Maximum Bias Current
- Typical Output Drive
- Operates from 1.1V to 40V
- Internal Pull-Up Current
- Output Can Drive Loads Above V^+
- $30\mu\text{A}$ Supply Current (LT1017)
- $110\mu\text{A}$ Supply Current (LT1018)

APPLICATIONS

- Power Supply Monitors
- Relay Driving
- Oscillators

DESCRIPTION

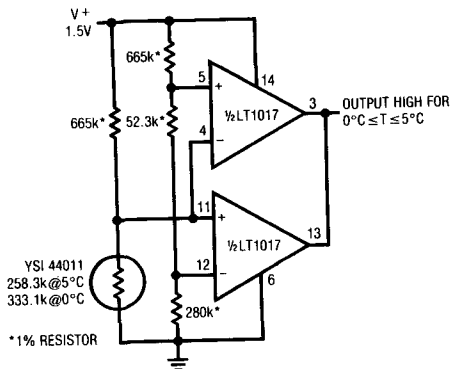
1mV
 15nA
 70mA

The LT1017 and LT1018 are general purpose micropower comparators. The LT1017 is optimized for lowest operating power while the LT1018 operates at higher power and higher speed. Both devices can operate from a single 1.1V cell up to 40V. The output stage includes a class "B" pull-up current source, eliminating the need for an external resistive pull-up and saving power. The output stage is also designed to allow driving loads connected to a supply more positive than the device, as can comparators with open collector output stages.

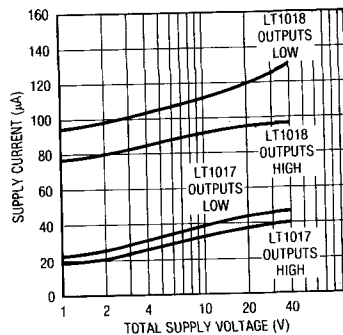
Input specifications are also excellent. On-chip trimming minimizes offset voltage, while the common-mode and common-mode rejection ratio keep both input-referred errors low. Common-mode voltage range includes ground. Special circuitry prevents false output states even if the input is partially driven.

REFER TO TABLE OF CONTENTS
 FOR REVISED DATA LOCATION

1.5V Powered Refrigerator Alarm



Supply Current



ABSOLUTE MAXIMUM RATINGS

Supply Voltage 40V
 Differential Input Voltage 40V
 Input Voltage -0.3V to 40V
 Short Circuit Duration Indefinite
 Operating Temperature Range 0°C to 70°C
 Storage Temperature Range -65°C to 150°C
 Lead Temperature (Soldering, 10 sec) 300°C

PACKAGE/ORDER INFORMATION

<p>TOP VIEW</p> <p>S16 PACKAGE PLASTIC SOL</p>	ORDER PART NUMBER
	LT1017CS LT1018CS
	PART MARKING
	LT1017CS LT1018CS

ELECTRICAL CHARACTERISTICS

PARAMETER	CONDITIONS		LT1017			LT1018			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Offset Voltage (Note 1)	$\pm 0.75V \leq V_S \leq \pm 20V$	25°C	0.4	1		0.4	1		mV
		●	0.5	1.4		0.5	1.4		mV
Bias Current	$\pm 0.75V \leq V_S \leq \pm 20V$	25°C	5	15		15	75		nA
		●	7	25		18	100		nA
Offset Current	$\pm 0.75V \leq V_S \leq \pm 20V$	25°C	0.4	2		1	8		nA
		●	0.5	3		1.6	12		nA
Common-Mode Rejection Ratio	$V_S = \pm 20V, -20V \leq V_{CM} \leq 19.1V$	25°C	105	115		105	115		dB
		●	100	115		100	115		dB
Power Supply Rejection Ratio	$\pm 0.75V \leq V_S \leq \pm 20V$	25°C	96	110		96	110		dB
		●	95	105		95	105		dB
Gain	No Load, $V_{OUT} = \pm 19.9V$ (Note 2)	25°C	110	115		110	125		dB
		●	105	115		105	120		dB
		25°C	100	110		100	110		dB
		●	94			94			dB
Output Sink Current	$V^+ = 4.5V, V^- = 0$ Overdrive > 30mV	25°C	30	65		35	70		mA
		●	25	50		25	50		mA
Output Source Current	$V^+ = 40V, V^- = 0$ $V_{IN} = 5mV, V_{OUT} = 0.4V$	25°C	30	75		75	250		μA
		●	25	70		50	220		μA
Output Source Current	$V^+ = 1.2V, V^- = 0$ $V_{IN} = 5mV, V_{OUT} = 0.4V$	25°C	25	35		70	140		μA
		●	15	20		45	120		μA

ELECTRICAL CHARACTERISTICS

PARAMETER	CONDITIONS	LT1017			LT1018		UNITS
		MIN	TYP	MAX	MIN	TYP	
Negative Output Saturation	$V^+ = 4.5V, V^- = 0$ $V_{IN} = -10mV$ $I_{OUT} = 0$ $= 0.1mA$ $= 1mA$ $= 10mA$ $= 30mA$ $I_{OUT} = 0$ $= 0.1mA$ $= 1mA$ $= 10mA$ $= 30mA$	25°C	5	20	5	15	mV
		25°C	35	60	35	60	mV
		25°C	60	120	60	120	mV
		25°C	120	200	120	250	mV
		25°C	350	600	350	700	mV
		●	5	20	8	20	mV
		●	40	75	35	70	mV
		●	75	150	70	150	mV
		●	150	300	150	300	mV
		●	600	900	500	900	mV
Positive Output Saturation	$I_{OUT} = 0$ $= 10\mu A$ $= 0$ $= 10\mu A$	25°C	40	80	35	80	mV
		25°C	175	250	175	250	mV
		●	45	90	45	90	mV
		●	190	300	190	300	mV
Leakage Current	$V_S = 5V, V_{OUT} = 40V$ $V_{IN} \geq 100mV$	25°C	0.5	3	1	8	μA
		●	0.6	3	1.8	10	μA
Supply Current	$V_S = 5V$ $V_S = 40V$	25°C	30	60	110	250	μA
		●	40	80	110	250	μA
		25°C	40	90	130	250	μA
		●	55	100	140	270	μA
Minimum Operating Voltage	$I_{OUT} = 1mA$	25°C		1.15		1.2	V
		●		1.15		1.2	V

The ● denotes specifications which apply over operating temperature range of 0°C to 70°C.

Note 1: Offset voltage is guaranteed over a common-mode voltage range of $V^- \leq V_{IN} \leq (V^+ - 0.9V)$.

Note 2: No load gain is guaranteed but not tested (LT1017 only).

NOTES

FEATURES

- Micropower
1.5 μ W (1 Sample/Second)
- Power Supply Flexibility
Single Supply +2.8V to +16V
Split Supply \pm 2.8V to \pm 8V
- *Guaranteed* Max. Offset 0.5mV
- *Guaranteed* Max. Tracking Error between Input Pairs \pm 0.1%
- Input Common-Mode Range to Both Supply Rails
- TTL/CMOS Compatible with \pm 5V or Single +5V Supply
- Input Errors are Stable with Time and Temperature

APPLICATIONS

- Battery Powered Systems
- Remote Sensing
- Window Comparator
- BANG-BANG Controllers

DESCRIPTION

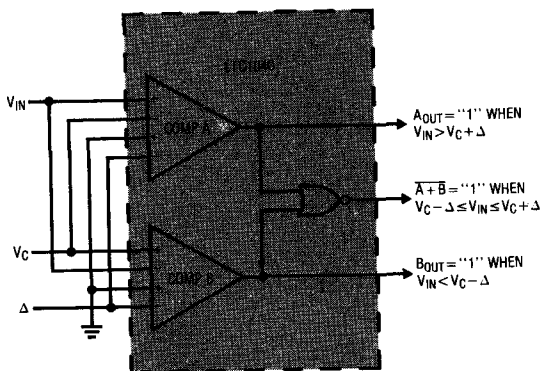
The LTC1040 is a monolithic CMOS dual comparator manufactured using Linear Technology's enhanced LTCMOS™ silicon gate process. Extremely low operating power levels are achieved by internally switching the comparator ON for short periods of time. The CMOS output logic holds the output information continuously while not consuming any power.

In addition to switching power ON, a switched output is provided to drive external loads during the comparator's active time. This allows not only low comparator power, but low total system power.

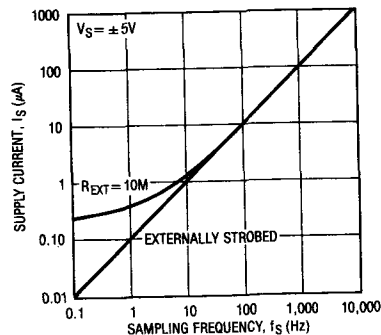
Sampling is controlled by an external strobe input or an internal oscillator. The oscillator frequency is set by an external RC network.

Each comparator has a unique input structure, giving two differential inputs. The output of the comparator will be high if the algebraic sum of the inputs is positive and low if the algebraic sum of the inputs is negative.

Window Comparator with Symmetric Window Limits



Typical LTC1040 Supply Current vs Sampling Frequency



LTC1040

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V^+ to V^-)	18V
Input Voltage	($V^+ + 0.3V$) to ($V^- - 0.3V$)
Operating Temperature Range	
LTC1040C	-40°C to 85°C
LTC1040M	-55°C to 125°C
Storage Temperature Range	-55°C to 150°C
Lead Temperature (Soldering, 10 sec.)	300°C
Output Short Circuit Duration	Continuous

PACKAGE/ORDER INFORMATION

	TEMPERATURE RANGE	ORDER PART NUMBER
	-55°C to 125°C -40°C to 85°C	LTC1040MJ LTC1040CN LTC1040CJ

ELECTRICAL CHARACTERISTICS

Test conditions: $V^+ = 5V$, $V^- = -5V$, $T_{MIN} \leq T_A \leq T_{MAX}$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	LTC1040M/LTC1040C			UNITS	
			MIN	TYP	MAX		
V_{OS}	Offset Voltage (Note 1)	Split Supplies $\pm 2.8V$ to $\pm 6V$ Single Supply ($V^- = GND$) + 2.8V to 6V	•	± 0.3	± 0.5	mV	
		Split Supplies $\pm 6V$ to $\pm 8V$ Single Supply ($V^- = GND$) + 6V to + 15V	•	± 1	± 3	mV	
	Tracking Error between Input Pairs (Notes 1 and 2)	Split Supplies $\pm 2.8V$ to $\pm 8V$ Single Supplies ($V^- = GND$) + 2.8 to + 16V	•	0.05	0.1	%	
I_{BIAS}	Input Bias Current	$T_A = 25^\circ C$, OSC = GND		± 0.3		nA	
R_{IN}	Average Input Resistance	$f_S = 1kHz$ (Note 3)	•	20	30	M Ω	
CMR	Common-Mode Range		•	V^-	V^+	V	
PSR	Power Supply Range	Split Supplies	•	± 2.8	± 8	V	
		Single Supplies ($V^- = GND$)	•	+ 2.8	+ 16	V	
$I_{S(ON)}$	Power Supply ON Current (Note 4)	$V^+ = 5V$, V_{PP} On	•	1.2	3	mA	
$I_{S(OFF)}$	Power Supply OFF Current (Note 4)	$V^+ = 5V$, V_{PP} Off	•	0.001	0.5	μA	
		LTC1040C LTC1040M	•	0.001	5	μA	
t_D	Response Time (Note 5)	$T_A = 25^\circ C$		60	80	100	μs
V_{OH} V_{OL}	A, B, $A+B$ and ON/OFF Outputs (Note 6)						
	Logic '1' Output Voltage	$V^+ = 4.75V$, $I_{OUT} = -360\mu A$	•	2.4	4.4	V	
	Logic '0' Output Voltage	$V^+ = 4.75V$, $I_{OUT} = 1.6mA$	•	0.25	0.4	V	
V_{IH} V_{IL}	STROBE Input (Note 6)						
	Logic '1' Input Voltage	$V^+ = 5.25V$	•	2.0	1.6	V	
	Logic '0' Input Voltage	$V^+ = 4.75V$	•	1.0	0.8	V	
R_{EXT}	External Timing Resistor	Resistor Tied between V^+ and OSC Pin	•	100	10,000	k Ω	
f_S	Sampling Frequency	$T_A = 25^\circ C$, $R_{EXT} = 1M\Omega$, $C_{EXT} = 0.1\mu F$		5		Hz	

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: Applies over input voltage range limit and includes gain uncertainty.

Note 2: Tracking error = $(V_{IN1} - V_{IN2}) / V_{IN1}$.

Note 3: R_{IN} is guaranteed by design and is not tested.

R_{IN} = 1 / (f_S × 33pF).

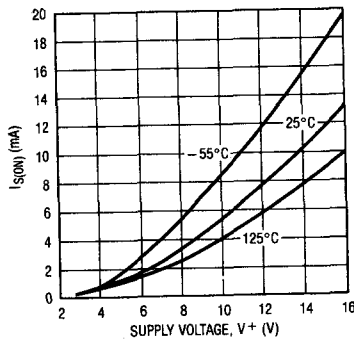
Note 4: Average supply current = $t_D \times I_S(ON) \times f_S + (1 - t_D \times f_S) \times I_S(OFF)$.

Note 5: Response time is set by an internal oscillator and is independent of overdrive voltage.

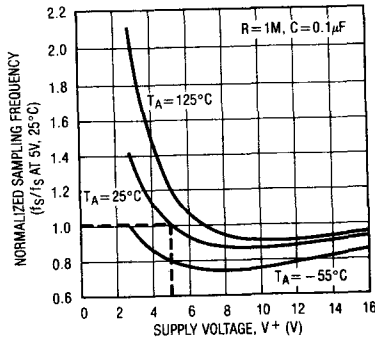
Note 6: Inputs and outputs also capable of meeting EIA / JEDEC B series CMOS specifications.

TYPICAL PERFORMANCE CHARACTERISTICS

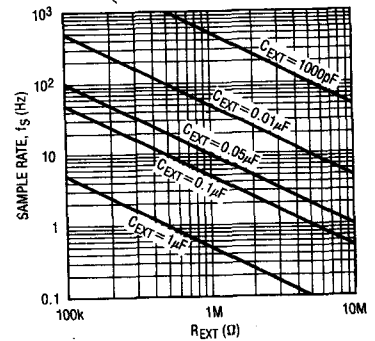
Peak Supply Current vs Supply Voltage



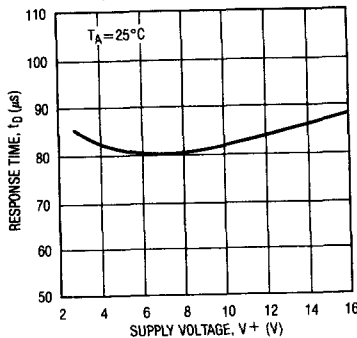
Normalized Sampling Frequency vs Supply Voltage and Temperature



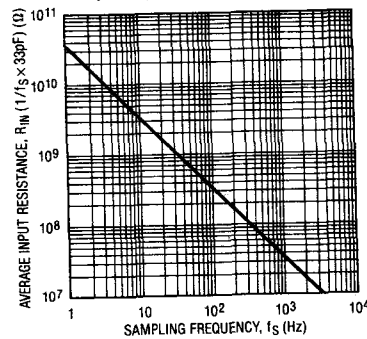
Sampling Rate vs R_{EXT}, C_{EXT}



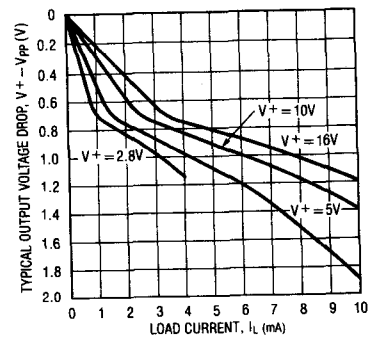
Response Time vs Supply Voltage



Input Resistance vs Sampling Frequency

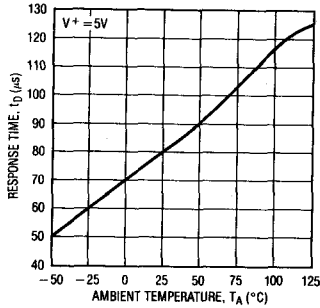


V_{PP} Output Voltage vs Load Current



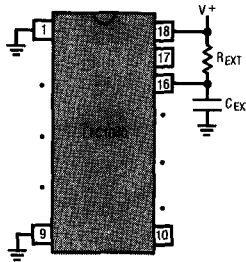
TYPICAL PERFORMANCE CHARACTERISTICS

Response Time vs Temperature

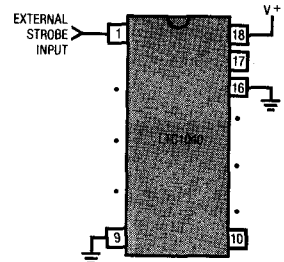


Quick Hookup Guide

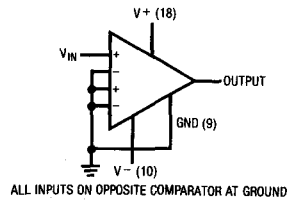
Self-Oscillating



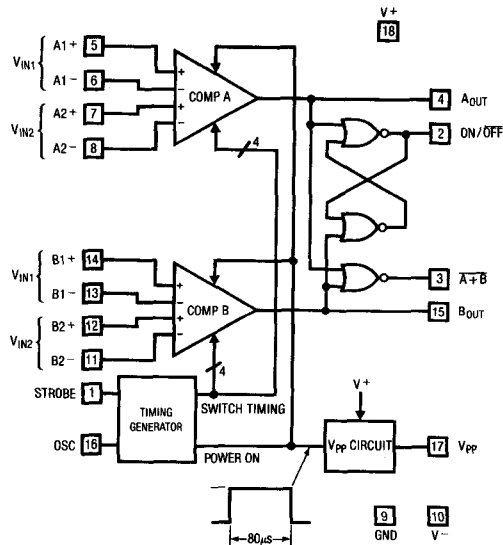
External Strobe



TEST CIRCUIT



BLOCK DIAGRAM



APPLICATIONS INFORMATION

The LTC1040 uses sampled data techniques to achieve its unique characteristics. Some of the experience acquired using classic linear comparators does not apply to this circuit, so a brief description of internal operation is essential to proper application.

The most obvious difference between the LTC1040 and other comparators is the dual differential input structure. Functionally, when the sum of inputs is positive, the comparator output is high and when the sum of the inputs is negative, the output is low. This unique input structure is achieved with CMOS switches and a precision capacitor array. Because of the switching nature of the inputs, the concept of input current and input impedance needs to be examined.

The equivalent input circuit is shown in Figure 1. Here, the input is being driven by a resistive source, R_S , with a bypass capacitor, C_S . The bypass capacitor may or may not be needed, depending on the size of the source resistance and the magnitude of the input voltage, V_{IN} .

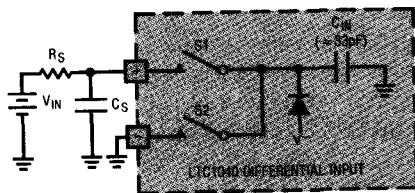


Figure 1. Equivalent Input Circuit

For $R_S < 10k\Omega$

Assuming C_S is zero, the input capacitor, C_{IN} , charges to V_{IN} with a time constant of $R_S C_{IN}$. When R_S is too large, C_{IN} does not have a chance to fully charge during the sampling interval ($\approx 80\mu s$) and errors will result. If R_S exceeds $10k\Omega$ a bypass capacitor is necessary to minimize errors.

For $R_S > 10k\Omega$

For R_S greater than $10k\Omega$, C_{IN} cannot fully charge and a bypass capacitor, C_S , is needed. When switch S1 closes,

charge is shared between C_S and C_{IN} . The change in voltage on C_S because of this charge sharing is:

$$\Delta V = V_{IN} \times \frac{C_{IN}}{C_{IN} + C_S}$$

This represents an error and can be made arbitrarily small by increasing C_S .

With the addition of C_S a second error term caused by the finite input resistance of the LTC1040 must be considered. Switches S1 and S2 alternately open and close, charging and discharging C_{IN} between V_{IN} and ground. The alternate charge and discharge of C_{IN} causes a current to flow into the positive input and out of the negative input. The magnitude of this current is:

$$I_{IN} = q \times f_s = V_{IN} C_{IN} f_s$$

where f_s is the sampling frequency. Because the input current is directly proportional to input voltage, the LTC1040 can be said to have an average input resistance of:

$$R_{IN} = \frac{V_{IN}}{I_{IN}} = \frac{1}{f_s C_{IN}} = \frac{1}{f_s \times 33pF}$$

(see typical curve of R_{IN} vs f_s). A voltage divider is set up between R_S and R_{IN} causing error.

The input voltage error caused by these two effects is:

$$V_{ERROR} = V_{IN} \left(\frac{C_{IN}}{C_{IN} + C_S} + \frac{R_S}{R_S + R_{IN}} \right)$$

$$\text{Example: } f_s = 10\text{Hz}, R_S = 1\text{M}\Omega, \\ C_S = 1\mu\text{F}, V_{IN} = 1\text{V}$$

$$V_{ERROR} = 1\text{V} \left(\frac{33 \times 10^{-12}}{1 \times 10^{-6}} + \frac{10^6}{10^6 + 3 \times 10^9} \right) \\ = 33\mu\text{V} + 330\mu\text{V} = 363\mu\text{V}$$

Notice that most of the error is caused by R_{IN} . If the sampling frequency is reduced to 1Hz, the voltage error is reduced to $66\mu\text{V}$.

APPLICATIONS INFORMATION

Minimizing Comparison Errors

The two differential input voltages, V1 and V2, are converted to charge by the input capacitors C_{IN1} and C_{IN2} (see Figure 2). The charge is summed at the virtual ground point and if the net charge is positive, the comparator output is high and if negative, it is low. There is an optimum way to connect these inputs, in a specific application, to minimize error.

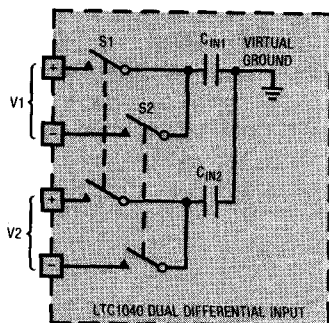


Figure 2. Dual Differential Equivalent Input Circuit

Ignoring internal offset, the LTC1040 will be at its switching point when:

$$V1 \times C_{IN1} + V2 \times C_{IN2} = 0.$$

Optimum error will be achieved when the differential voltages, V1 and V2, are individually minimized. Figure 3 shows two ways to connect the LTC1040 to compare an input voltage, V_{IN}, to a reference voltage, V_{REF}. Using the above equation, each method will be at null when:

- (a) $(V_{REF} - 0V) C_{IN1} - (0V - V_{IN}) C_{IN2} = 0$
or $V_{IN} = V_{REF} (C_{IN1} / C_{IN2})$
- (b) $(V_{REF} - V_{IN}) C_{IN1} - (0V - 0V) C_{IN2} = 0$
or $V_{IN} = V_{REF}$.

Notice that in method (a) the null point depends on the ratio of C_{IN1} / C_{IN2}, but method (b) is independent of this ratio. Also, because method (b) has zero differential input voltage, the errors due to finite input resistance are negligible. The LTC1040 has a high accuracy capacitor array and even the non-optimum connection will only result in ±0.1% more error worst-case compared to the optimum connection.

Tracking Error

Tracking error is caused by the ratio error between C_{IN1} and C_{IN2} and is expressed as a percentage. For example, consider Figure 3(a) with V_{REF} = 1V. Then at null,

$$V_{IN} = V_{REF} \frac{C_{IN1}}{C_{IN2}} = 1V \pm 1mV$$

because C_{IN1} is guaranteed to equal C_{IN2} to within 0.1%.

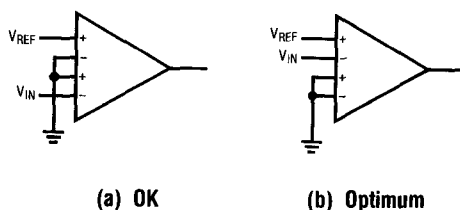


Figure 3. Two Ways to Do It

Common-Mode Range

The input switches of the LTC1040 are capable of switching to either the V⁺ or V⁻ supply. This means that the input common-mode range includes both supply rails. Many applications, not feasible with conventional comparators, are possible with the LTC1040. In the load current detector shown in Figure 4, a 0.1Ω resistor is used to sense the current in the V⁺ supply. This application requires the dual differential input and common-mode capabilities of the LTC1040.

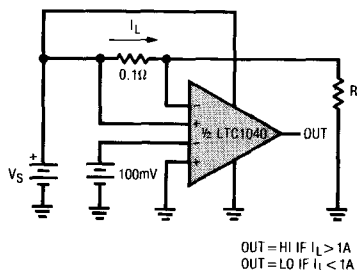


Figure 4. Load Current Detector

APPLICATIONS INFORMATION

Offset Voltage Error

The errors due to offset, common-mode, power supply variation, gain and temperature are all included in the offset voltage specification. This makes it easy to compute the error when using the LTC1040.

Example: error computation for Figure 4.

Assume: $2.8V \leq V_S \leq 6V$.

Then total worst-case error is:

$$I_{L(EROR)} = \pm (100mV \times 0.001 + 0.5mV) \times \frac{1A}{100mV} = \pm 6mA$$

↑ Tracking Error ↑ V_{OS}

$$I_{L(EROR)}\% = \frac{6mA}{1A} \times 100 = \pm 0.6\%$$

Note: If source resistance exceeds $10k\Omega$, bypass capacitors should be used and the associated errors must be included.

Pulsed Power (V_{PP}) Output

It is often desirable to use comparators with resistive networks such as bridges. Because of the extremely low power consumption of the LTC1040, the power consumed by these resistive networks can far exceed that of the device itself.

At low sample rates the LTC1040 spends most of its time off. To take advantage of this, a pulsed power (V_{PP}) output is provided. V_{PP} is switched to V^+ when the comparator is on and to a high impedance (open circuit) when the comparator is off. The ON time is nominally $80\mu s$. Figure 5 shows the V_{PP} output circuit.

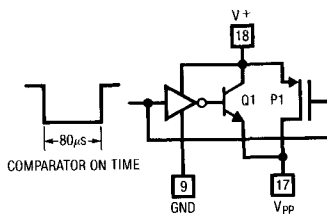


Figure 5. V_{PP} Output Switch

The V_{PP} output voltage is not precise (see V_{PP} Output Voltage versus Load Current curve). There are two ways V_{PP} can be used to power external networks without excessive errors: (1) ratiometric networks and (2) fast settling references.

In a ratiometric network (see Figure 6), the inputs are all proportional to V_{PP} . Consequently, for small changes, the absolute value of V_{PP} does not affect accuracy.

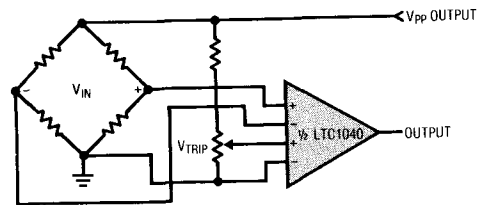


Figure 6. Ratiometric Network Driven by V_{PP}

It is critical that the inputs to the LTC1040 completely settle within $4\mu s$ of the start of the comparison cycle and that they do not change during the $80\mu s$ ON time. When driving resistive networks with V_{PP} , capacitive loading on the network should be minimized to meet the $4\mu s$ settling time requirement. It is not recommended that V_{PP} be used to drive networks with source impedances, as seen by the inputs, of greater than $10k\Omega$.

In applications where an absolute reference is required, the V_{PP} output can be used to drive a fast settling reference. The LT1009 2.5V reference, ideal in this application, settles in approximately $2\mu s$ (see Figure 7). The current through R1 must be large enough to supply the LT1009 minimum bias current ($\approx 1mA$) and the load current, I_L .

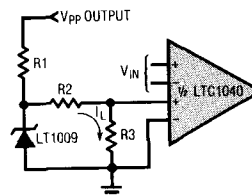


Figure 7. Driving Reference with V_{PP} Output

APPLICATIONS INFORMATION

Output Logic

In addition to the normal outputs (A_{OUT} and B_{OUT}), two additional outputs, $\overline{A+B}$ and ON/OFF , are provided (see Figure 8 and Table I). All logic is powered from V^+ and ground, thus input and output logic levels are independent of the V^- supply. The LTC1040 is directly compatible with CMOS logic and is TTL compatible for $4.75V \leq V^+ \leq 5.25V$. No external pull-up resistors are required.

Table I. Output Logic Truth Table

ΣA INPUTS	ΣB INPUTS	A_{OUT}	B_{OUT}	$\overline{A+B}$	ON/OFF
+	+	H	H	L	L
+	-	H	L	L	L
-	+	L	H	L	H
-	-	L	L	H	I*

*I = indeterminate. When both A and B outputs are low, the ON/OFF output remains in the state it was in prior to entering $A_{OUT} = B_{OUT} = L$.

Using External Strobe

A positive pulse on the strobe input, with the OSC input tied to ground, will initiate a comparison cycle. The STROBE input is edge-sensitive and pulse widths of 50ns will typically trigger the device.

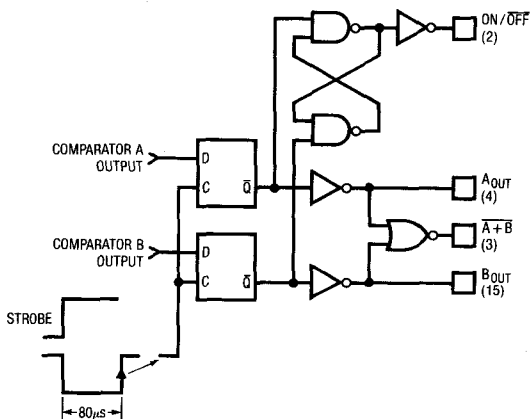


Figure 8. LTC1040 Logic Diagram

Because of the sampling nature of the LTC1040, some sensitivity exists between the offset voltage and the falling edge of the input strobe. When the falling edge of the strobe signal falls within the comparator's active time ($80\mu s$ after rising edge), offset changes of as much as 2mV can occur. To eliminate this problem, make sure the strobe pulse width is greater than the response time, t_D .

Using Internal Strobe

An internal oscillator allows the LTC1040 to strobe itself. The frequency of oscillation, and hence sampling rate, is set by an external RC network (see typical curve of frequency versus R_{EXT} , C_{EXT}).

For self-oscillation, the STROBE pin must be tied to ground. The external RC network is connected as shown in Figure 9.

To assure oscillation, R_{EXT} must be between 100k and 10M. There is no limit to the size of C_{EXT} .

R_{EXT} is very important in determining the power consumption. The average voltage at the oscillator pin is approximately $V^+ / 2$. The power consumed by R_{EXT} is then: $P_{R_{EXT}} = (V^+ / 2)^2 / R_{EXT}$.

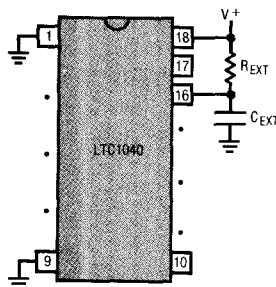


Figure 9. External RC Connection

APPLICATIONS INFORMATION

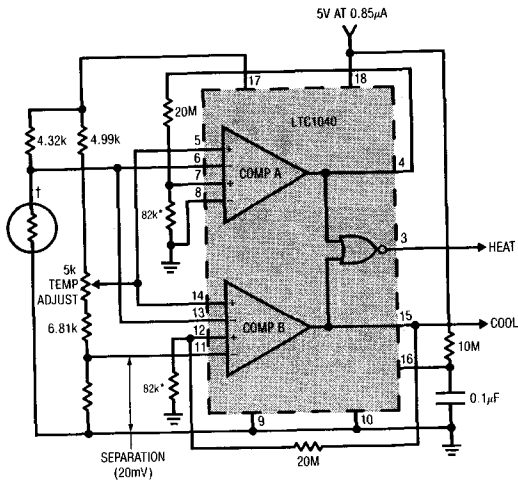
Example: $R_{EXT} = 1M$, $V^+ = 5V$, $P_{REXT} = (2.5)^2 / 10^6 = 6.25 \times 10^{-6}W$.

This is about four times the power consumed by the LTC1040 at $V^+ = 5V$ and $f_s = 1$ sample/second. Where

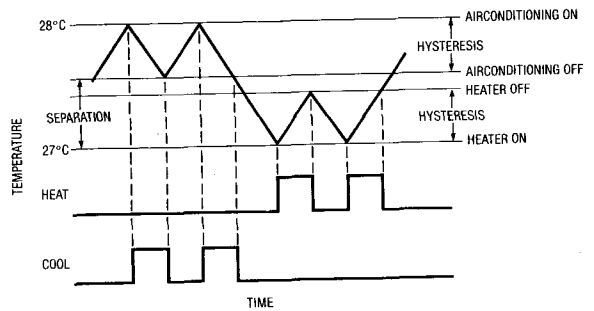
power is a premium R_{EXT} should be made as large as possible. Note that the power consumed by R_{EXT} is *not* a function of f_s or C_{EXT} .

TYPICAL APPLICATIONS

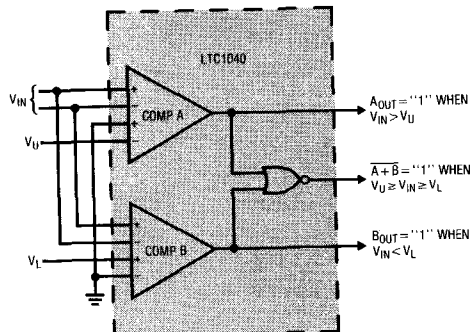
Complete Heating/Cooling Automatic Thermostat



† THERMISTOR # 44007
YELLOW SPRINGS INSTRUMENT CO., INC.
*HYSTERESIS = $5V \times \frac{82k}{20M} = 20mV$

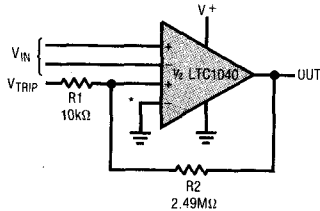


Window Comparator with Independent Window Limits and Fully Floating Differential Input



TYPICAL APPLICATIONS

Hysteresis Comparator with Fully Floating Differential Input

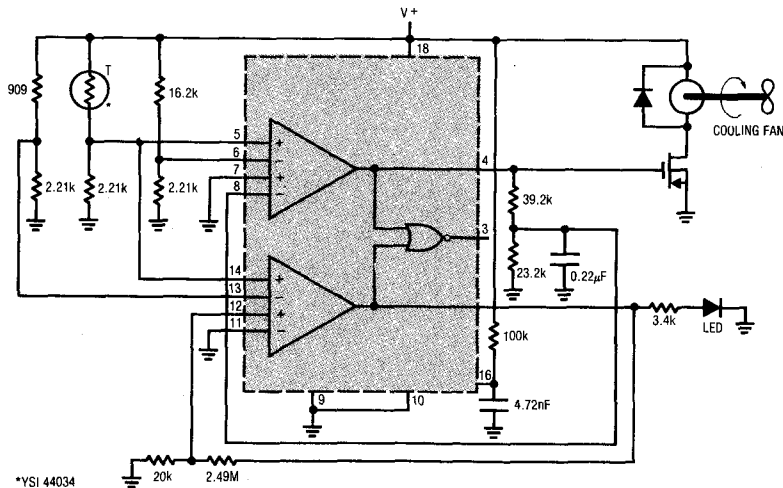


$$\text{OUT} = \text{"0"} \text{ WHEN } V_{IN} > V_{U} = \frac{V_{TRIP} R_2 + (5V) R_1}{R_1 + R_2} = 0.996 V_{TRIP} + 20\text{mV}$$

$$\text{OUT} = \text{"1"} \text{ WHEN } V_{IN} < V_{L} = \frac{V_{TRIP} R_2}{R_1 + R_2} = 0.996 V_{TRIP}$$

*TO CENTER HYSTERESIS ABOUT V_{TRIP} FORCE THIS INPUT TO HYSTERESIS / 2 (10mV)

Temperature Controlled Cooling Fan to Reduce Fan Noise, Power Consumption and Wear



*YSI 44034

The LTC1040 as a Linear Amplifier

With a simple RC filter the LTC1040 can be made to function as a linear amplifier. By filtering the logic output and feeding it back to the negative input, the loop forces the output duty cycle $[t_{ON} / (t_{ON} + t_{OFF})]$ so that V_{OUT} equals V_{IN} (Figure 10).

The RC time constant is set to keep the ripple on the output small. The maximum output ripple is: $\Delta V = V^+ / f_s RC$ and should be set to 0.5mV to 1mV for best results. Notice that the higher the sampling frequency, f_s , the lower RC can be. This is important because the RC filter also sets the loop response. A convenient way to keep f_s as high as possible under all conditions is to connect a 100k resistor to pin 16 (OSC) with no capacitance to ground.

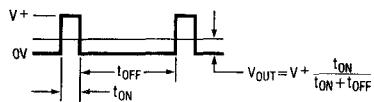
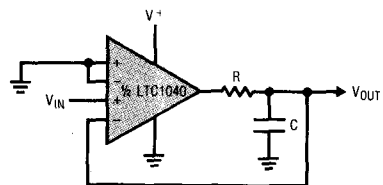
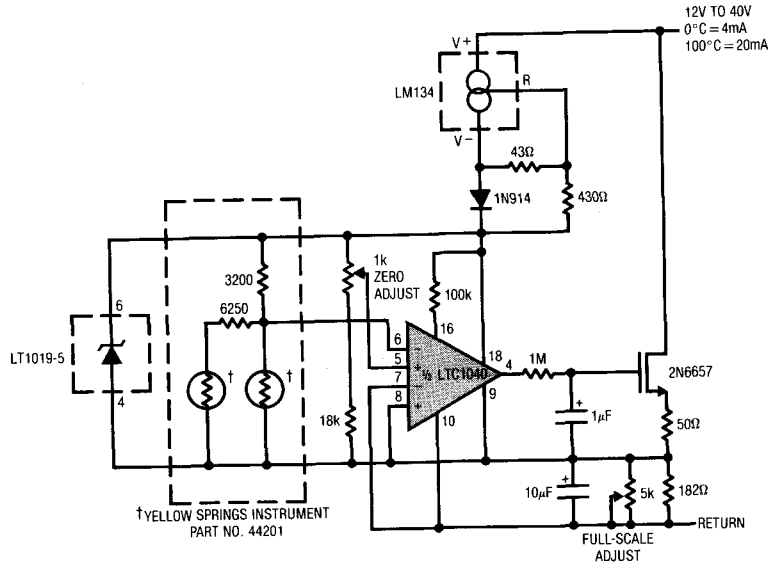


Figure 10. The LTC1040 as a Linear Amplifier

TYPICAL APPLICATIONS

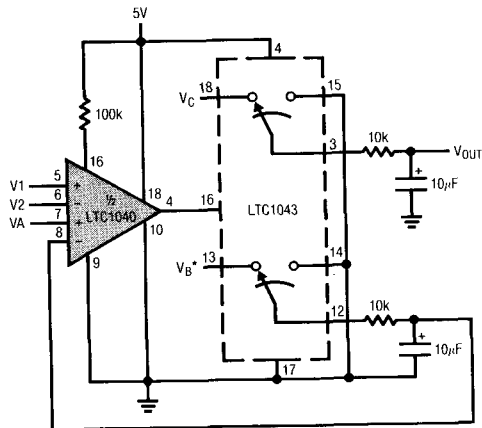
2-Wire 0°C to 100°C Temperature Transducer with 4mA to 20mA Output



ACCURACY = $\pm 0.1^\circ\text{C}$ + $\pm 0.2^\circ\text{C}$ = $\pm 0.3^\circ\text{C}$
 CIRCUIT ERROR AT 25°C TRANSDUCER ERROR

6

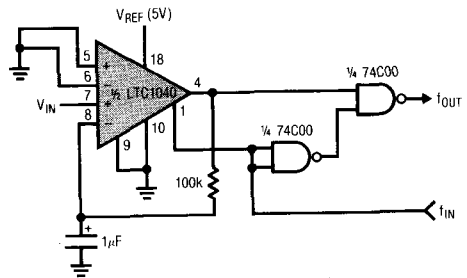
Analog Multiplier / Divider



$$V_{OUT} = \frac{(V_A + V_1 - V_2) \times V_C}{V_B}$$

ACCURACY = $\pm 10\text{mV}$ NO TRIM
 * V_B MUST BE $> V_A + (V_1 - V_2)$

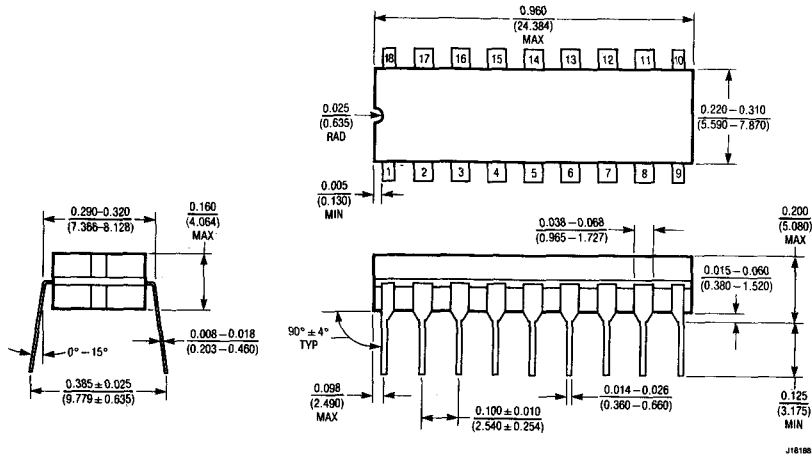
Single +5V Voltage-to-Frequency Converter



$$f_{OUT} (\text{AVERAGE}) = f_{IN} \frac{V_{IN}}{V_{REF}} \pm 0.1\% \text{ FS}$$

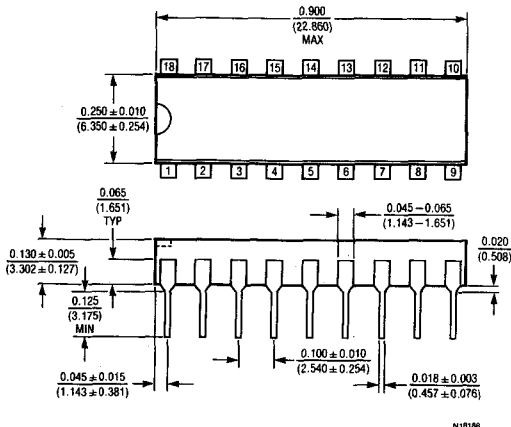
PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

J Package
18 Lead Hermetic DIP



T_{jmax}	Θ_{JA}
150°C	80°C/W

N Package
18 Lead Plastic DIP



T_{jmax}	Θ_{JA}
110°C	120°C/W

FEATURES

- Micropower 1.5 μ W (1 Sample/Second)
- Wide Supply Range 2.8V to 16V
- High Accuracy
 - Guaranteed SET POINT Error ± 0.5 mV Max.
 - Guaranteed Deadband $\pm 0.1\%$ of Value Max.
- Wide Input Voltage Range V^+ to Ground
- TTL Outputs with 5V Supply
- Two Independent Ground-Referenced Control Inputs
- Small Size 8-Pin MiniDIP

APPLICATIONS

- Temperature Control (Thermostats)
- Motor Speed Control
- Battery Charger
- Any ON-OFF Control Loop

DESCRIPTION

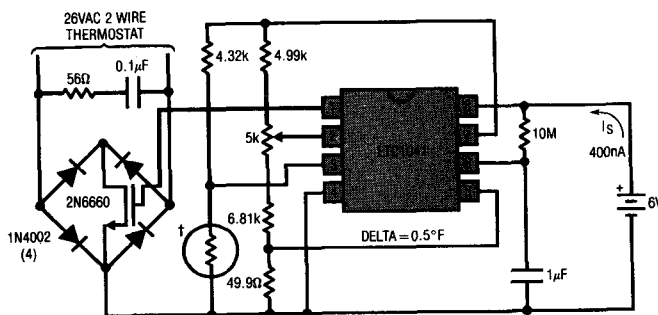
The LTC1041 is a monolithic CMOS BANG-BANG controller manufactured using Linear Technology's enhanced LTCMOS™ silicon gate process. BANG-BANG loops are characterized by turning the control element fully ON or fully OFF to regulate the average value of the parameter to be controlled. The SET POINT input determines the average control value and the DELTA input sets the deadband. The deadband is always $2 \times$ DELTA and is centered around the SET POINT. Independent control of the SET POINT and deadband, with no interaction, is made possible by the unique sampling input structure of the LTC1041.

An external RC connected to the OSC pin sets the sampling rate. At the start of each sample, internal power to the analog section is switched on for $\approx 80\mu$ s. During this time the analog inputs are sampled and compared. After the comparison is complete, power is switched off. This achieves extremely low average power consumption at low sampling rates. CMOS logic holds the output continuously while consuming virtually no power.

To keep system power at an absolute minimum, a switched power output (V_{PP}) is provided. External loads, such as bridge networks and resistive dividers, can be driven by this switched output.

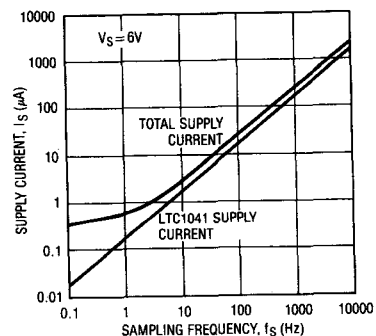
The output logic sense (i.e., ON = V^+) can be reversed (i.e., ON = GND) by interchanging the V_{IN} and SET POINT inputs. This has no other effect on the operation of the LTC1041.

Ultra Low Power 50°F to 100°F (2.4 μ W) Thermostat



ALL RESISTORS 1%.
 †YELLOW SPRINGS INSTRUMENT CO., INC. P/N 44007
 DRIVING THERMISTOR WITH V_{PP} ELIMINATES 3.8°F
 ERROR DUE TO SELF-HEATING.

Supply Current vs Sampling Frequency



LTCMOS™ is a trademark of Linear Technology Corporation.

LTC1041

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V^+ to V^-)	18V
Input Voltage	($V^+ + 0.3V$) to ($V^- - 0.3V$)
Operating Temperature Range	
LTC1041C	-40°C to 85°C
LTC1041M	-55°C to 125°C
Storage Temperature Range	-55°C to 150°C
Lead Temperature (Soldering, 10 sec.)	300°C
Output Short Circuit Duration	Continuous

PACKAGE/ORDER INFORMATION

	TEMPERATURE RANGE	ORDER PART NUMBER
	-55°C to 125°C -40°C to 85°C	LTC1041MJ8 LTC1041CN8

ELECTRICAL CHARACTERISTICS

Test Conditions: $V^+ = 5V$, $T_{MIN} \leq T_A \leq T_{MAX}$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	LTC1041M/LTC1041C			UNITS	
			MIN	TYP	MAX		
	SET POINT Error (Note 2)	$V^+ = 2.8V$ to $6V$ (Note 1)	•	± 0.3 +	± 0.5 +	mV	
		$V^+ = 6V$ to $15V$ (Note 1)	•	± 0.05 +	± 0.1 +	% of DELTA	
	Deadband Error (Note 3)	$V^+ = 2.8V$ to $6V$ (Note 1)	•	± 1 +	± 3 +	mV	
		$V^+ = 6V$ to $15V$ (Note 1)	•	± 0.05 +	± 0.1 +	% of DELTA	
	Input Current	$V^+ = 2.8V$ to $6V$ (Note 1)	•	± 0.6 +	± 1 +	mV	
		$V^+ = 6V$ to $15V$ (Note 1)	•	± 0.1 +	± 0.2 +	% of DELTA	
I_{OS}	Input Current	$V^+ = 5V$, $T_A = 25^\circ C$, OSC = GND (V_{IN} , SET POINT and DELTA Inputs)		± 0.3		nA	
R_{IN}	Equivalent Input Resistance	$f_S = 1kHz$ (Note 4)	•	10	15	M Ω	
	Input Voltage Range		•	GND	V^+	V	
PSR	Power Supply Range		•	2.8	16	V	
$I_{S(ON)}$	Power Supply ON Current (Note 5)	$V^+ = 5V$, V_{PP} ON	•	1.2	3	mA	
$I_{S(OFF)}$	Power Supply OFF Current (Note 5)	$V^+ = 5V$, V_{PP} OFF	•	0.001	0.5	μA	
		LTC1041C	•	0.001	5	μA	
t_D	Response Time (Note 6)	$V^+ = 5V$		60	80	100	μs
V_{OH}	ON/OFF Output (Note 7)						
	Logical '1' Output Voltage	$V^+ = 4.75V$, $I_{OUT} = -360\mu A$	•	2.4	4.4	V	
V_{OL}	Logical '0' Output Voltage	$V^+ = 4.75V$, $I_{OUT} = 1.6mA$	•	0.25	0.4	V	
R_{EXT}	External Timing Resistor	Resistor Connected between V^+ and OSC Pin	•	100	10,000	k Ω	
f_S	Sampling Frequency	$V^+ = 5V$, $T_A = 25^\circ C$, $R_{EXT} = 1M$, $C_{EXT} = 0.1\mu F$		5		Hz	

The ● denotes the specifications which apply over the full operating temperature range. The shaded electrical specifications indicate those parameters which have been improved or guaranteed test limits provided for the first time.

Note 1: Applies over input voltage range limit and includes gain uncertainty.

Note 2: SET POINT error = $\left(\frac{V_U + V_L}{2} \right) - \text{SET POINT}$

where V_U = upper band limit and V_L = lower band limit.

Note 3: Deadband error = $(V_U - V_L) - 2 \times \text{DELTA}$ where V_U = upper band limit and V_L = lower band limit.

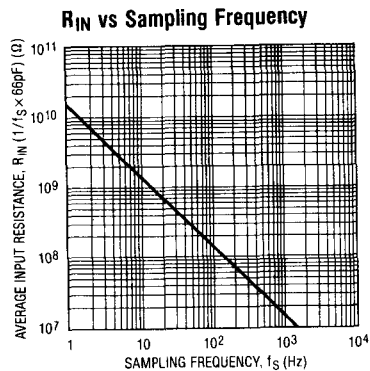
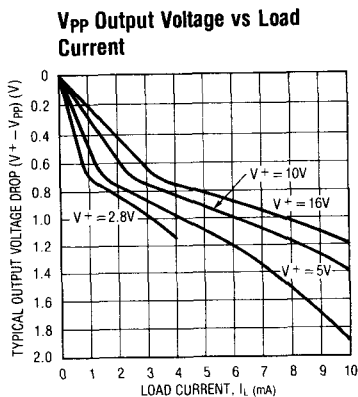
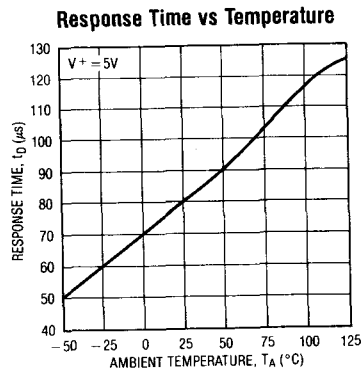
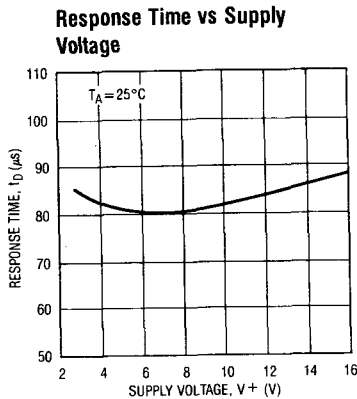
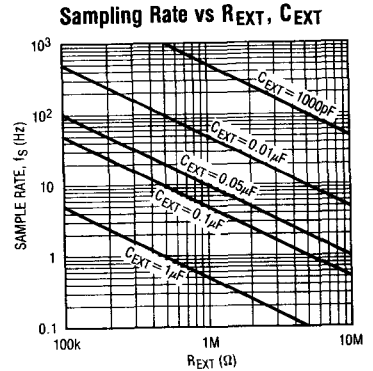
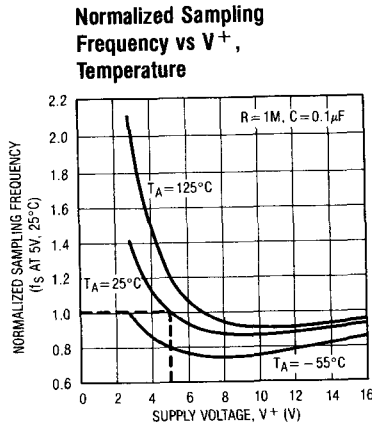
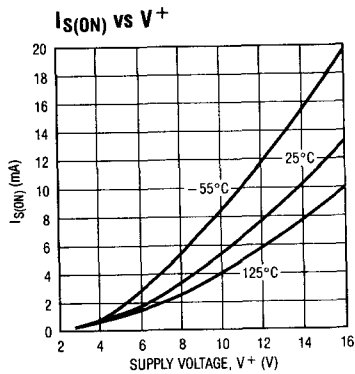
Note 4: R_{IN} is guaranteed by design and is not tested.
 $R_{IN} = 1 / (f_S \times 66pF)$.

Note 5: Average supply current = $t_D \times I_{S(ON)} \times f_S + (1 - t_D \times f_S) I_{S(OFF)}$.

Note 6: Response time is set by an internal oscillator and is independent of overdrive voltage. $t_D = V_{PP}$ pulse width.

Note 7: Output also capable of meeting EIA/JEDEC standard B series CMOS drive specifications.

TYPICAL PERFORMANCE CHARACTERISTICS



6

APPLICATIONS INFORMATION

The LTC1041 uses sampled data techniques to achieve its unique characteristics. It consists of two comparators, each of which has two differential inputs (Figure 1). When the sum of the voltages on a comparator's inputs is positive, the output is high and when the sum is negative, the output is low. The inputs are interconnected such that the RS flip-flop is reset ($ON/OFF = GND$) when $V_{IN} > (SET\ POINT + \Delta)$ and is set ($ON/OFF = V^+$) when $V_{IN} < (SET\ POINT - \Delta)$. This makes a very precise hysteresis loop of $2 \times \Delta$ centered around the SET POINT. See Figure 1(b).

For $R_s < 10k\Omega$

The dual differential input structure is made with CMOS switches and a precision capacitor array. Input impedance characteristics of the LTC1041 can be determined from the equivalent circuit shown in Figure 2. The input capacitance will charge with a time constant of $R_s \times C_{IN}$. The ability to fully charge C_{IN} from the signal source during the controller's active time is critical in determining errors caused by the input charging current. For source resistances less than $10k\Omega$, C_{IN} fully charges and no error is caused by the charging current.

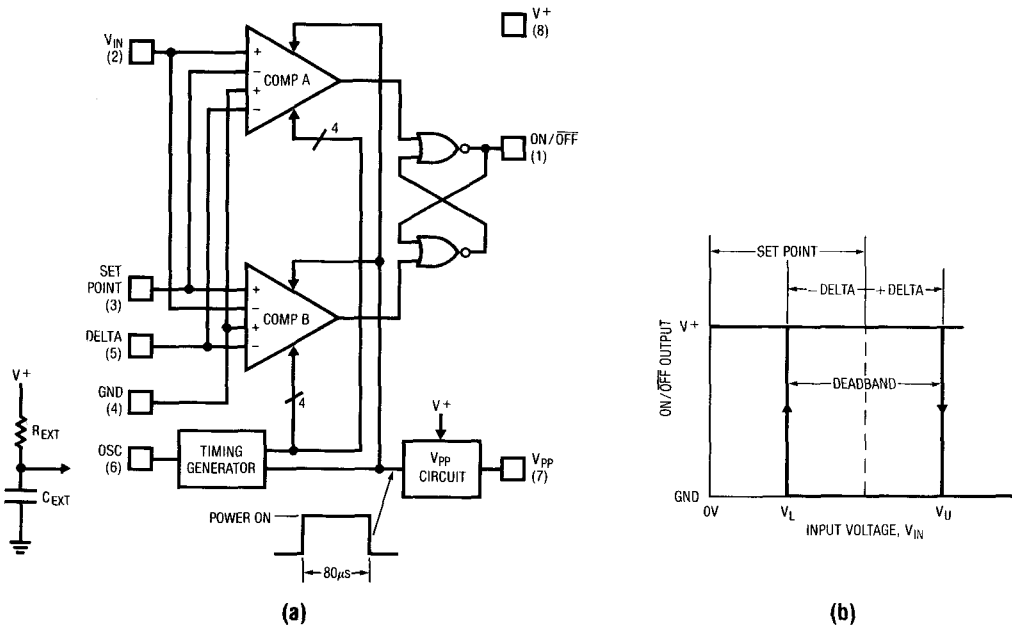


Figure 1. LTC1041 Block Diagram

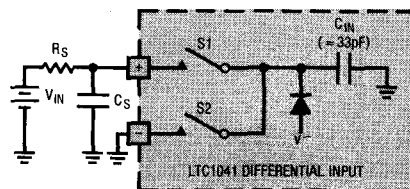


Figure 2. Equivalent Input Circuit

APPLICATIONS INFORMATION

For $R_S > 10k\Omega$

For source resistances greater than $10k\Omega$, C_{IN} cannot fully charge, causing voltage errors. To minimize these errors, an input bypass capacitor, C_S , should be used. Charge is shared between C_{IN} and C_S , causing a small voltage error. The magnitude of this error is $\Delta V = V_{IN} \times C_{IN} / (C_{IN} + C_S)$. This error can be made arbitrarily small by increasing C_S .

The averaging effect of the bypass capacitor, C_S , causes another error term. Each time the input switches cycle between the plus and minus inputs, C_{IN} is charged and discharged. The average input current due to this is $I_{AVG} = V_{IN} \times C_{IN} \times f_s$, where f_s is the sampling frequency. Because the input current is directly proportional to the differential input voltage, the LTC1041 can be said to have an average input resistance of $R_{IN} = V_{IN} / I_{AVG} = 1 / (f_s \times C_{IN})$.

Since two comparator inputs are connected in parallel, R_{IN} is one half of this value (see typical curve of R_{IN} versus f_s). This finite input resistance causes an error due to the voltage divider between R_S and R_{IN} .

The input voltage error caused by both of these effects is $V_{ERROR} = V_{IN} [2C_{IN} / (2C_{IN} + C_S) + R_S / (R_S + R_{IN})]$.

Example: assume $f_s = 10\text{Hz}$, $R_S = 1\text{M}$, $C_S = 1\mu\text{F}$, $V_{IN} = 1\text{V}$, $V_{ERROR} = 1\text{V}(66\mu\text{V} + 660\mu\text{V}) = 726\mu\text{V}$. Notice that most of the error is caused by R_{IN} . If the sampling frequency is reduced to 1Hz , the voltage error from the input impedance effects is reduced to $136\mu\text{V}$.

Input Voltage Range

The input switches of the LTC1041 are capable of switching either to the V^+ supply or ground. Consequently, the input voltage range includes both supply rails. This is a further benefit of the sampling input structure.

Error Specifications

The only measurable errors on the LTC1041 are the deviations from "ideal" of the upper and lower switching levels [Figure 1(b)]. From a control standpoint, the error

in the SET POINT and deadband is critical. These errors may be defined in terms of V_U and V_L .

$$\text{SET POINT error} \equiv \left(\frac{V_U + V_L}{2} \right) - \text{SET POINT}$$

$$\text{deadband error} \equiv (V_U - V_L) - 2 \times \text{DELTA}$$

The specified error limits (see electrical characteristics) include error due to offset, power supply variation, gain, time and temperature.

Pulsed Power (V_{PP}) Output

It is often desirable to use the LTC1041 with resistive networks such as bridges and voltage dividers. The power consumed by these resistive networks can far exceed that of the LTC1041 itself.

At low sample rates the LTC1041 spends most of its time off. A switched power output, V_{PP} , is provided to drive the input network, reducing its average power as well. V_{PP} is switched to V^+ during the controller's active time ($\approx 80\mu\text{s}$) and to a high impedance (open circuit) when internal power is switched off.

Figure 3 shows the V_{PP} output circuit. The V_{PP} output voltage is not precisely controlled when driving a load (see typical curve of V_{PP} output voltage versus load current). In spite of this, high precision can be achieved in two ways: (1) driving ratiometric networks and (2) driving fast settling references.

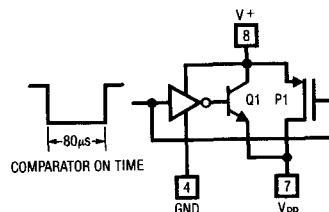


Figure 3. V_{PP} Output Switch

APPLICATIONS INFORMATION

In ratiometric networks (Figure 4) all the inputs are proportional to V_{PP} . Consequently, the absolute value of V_{PP} does not affect accuracy.

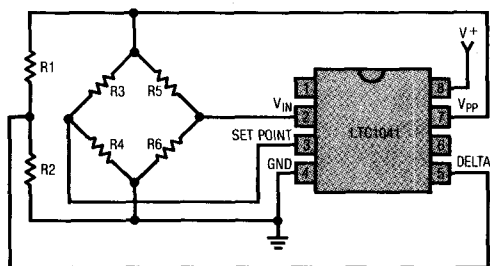


Figure 4. Ratiometric Network Driven by V_{PP}

If the best possible performance is needed, the inputs to the LTC1041 must completely settle within $4\mu s$ of the start of the comparison cycle (V_{PP} high impedance to V^+ transition). Also, it is critical that the input voltages do not change during the $80\mu s$ active time. When driving resistive input networks with V_{PP} , capacitive loading should be minimized to meet the $4\mu s$ settling time requirement. Further, care should be exercised in layout when driving networks with source impedances, as seen by the LTC1041, of greater than $10k\Omega$ (see For $R_s > 10k\Omega$).

In applications where an absolute reference is required, the V_{PP} output can be used to drive a fast settling reference. The LTC1009 2.5V reference settles in $\approx 2\mu s$ and is ideal for this application (Figure 5). The current through R_1 must be large enough to supply the LT1009 minimum bias current ($\approx 1mA$) and the load current, I_L .

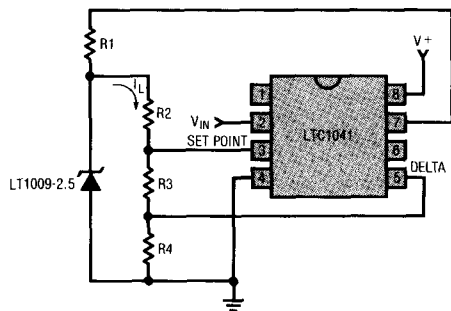


Figure 5. Driving Reference with V_{PP} Output

Internal Oscillator

An internal oscillator allows the LTC1041 to strobe itself. The frequency of the oscillation, and hence the sampling rate, is set with an external RC network (see typical curve, OSC frequency versus R_{EXT} , C_{EXT}). R_{EXT} and C_{EXT} are connected as shown in Figure 1. To assure oscillation, R_{EXT} must be between $100k\Omega$ and $10M\Omega$. There is no limit to the size of C_{EXT} .

At low sampling rates, R_{EXT} is very important in determining the power consumption. R_{EXT} consumes power continuously. The average voltage at the OSC pin is approximately $V^+/2$, giving a power dissipation of $P_{REXT} = (V^+/2)^2 / R_{EXT}$.

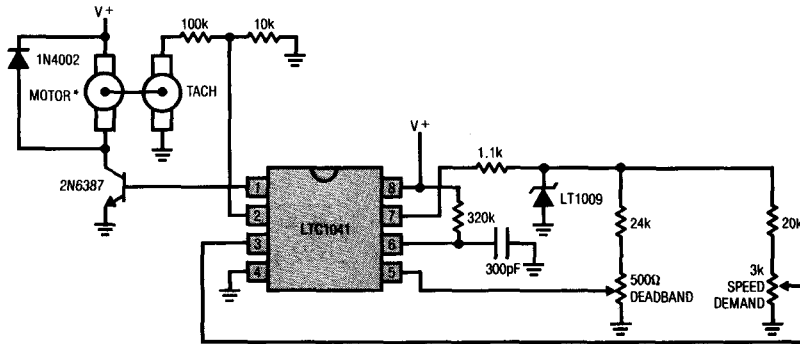
Example: assume $R_{EXT} = 1M\Omega$, $V^+ = 5V$, $P_{REXT} = (2.5)^2 / 10^6 = 6.25\mu W$. This is approximately four times the power consumed by the LTC1041 at $V^+ = 5V$ and $f_s = 1$ sample/second. Where power is a premium, R_{EXT} should be made as large as possible. Note that the power dissipated by R_{EXT} is *not* a function of f_s or C_{EXT} .

If high sampling rates are needed and power consumption is of secondary importance, a convenient way to get the maximum possible sampling rate is to make $R_{EXT} = 100k\Omega$ and $C_{EXT} = 0$. The sampling rate, set by the controller's active time, will nominally be $\approx 10kHz$.

To synchronize the sampling of the LTC1041 to an external frequency source, the OSC pin can be driven by a CMOS gate. A CMOS gate is necessary because the input trip points of the oscillator are close to the supply rails and TTL does not have enough output swing. Externally driven, there will be a delay from the rising edge of the OSC input and the start of the sampling cycle of approximately $5\mu s$.

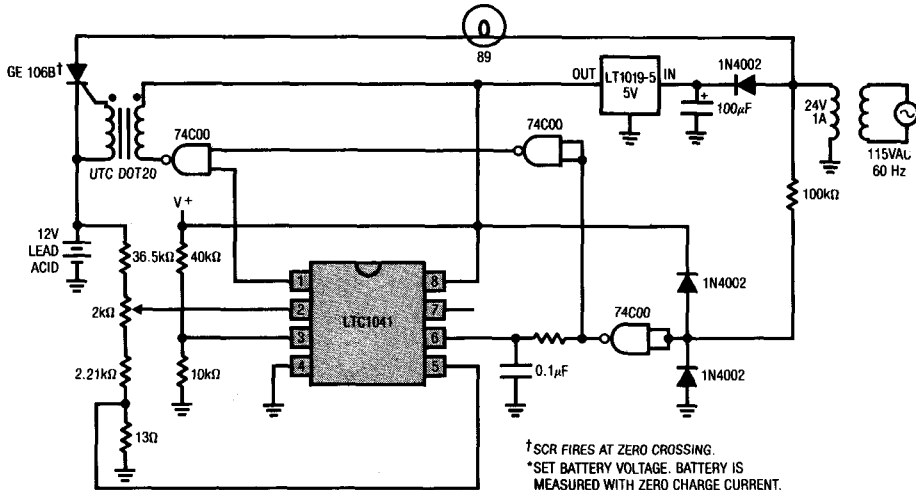
TYPICAL APPLICATIONS

Motor Speed Controller



*CANNON GKT26-T5-3SAE

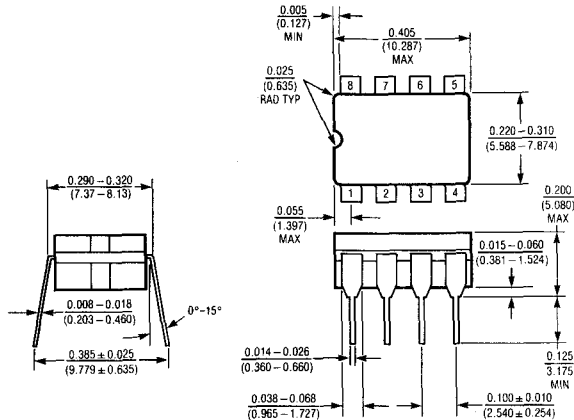
Battery Charger



6

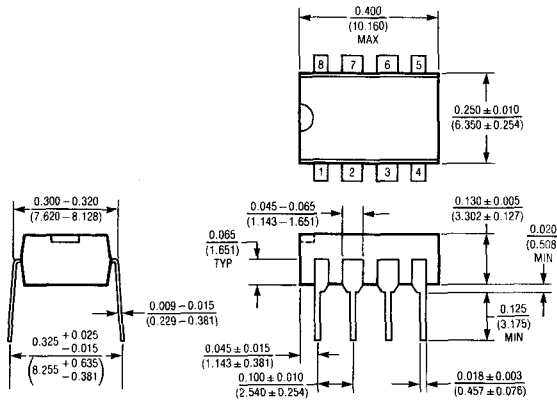
PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

J Package
8 Lead Hermetic DIP



T_{jmax} 150°C	Θ_{JA} 100°C/W
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N Package
8 Lead Plastic



T_{jmax} 110°C	Θ_{JA} 150°C/W
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FEATURES

- Micropower 1.5 μ W (1 Sample/Second)
- Wide Supply Range— +2.8V to +16V
- High Accuracy
 - Center Error \pm 1mV Max
 - Width Error \pm 0.15% Max
- Wide Input Voltage Range
V⁺ to Ground
- TTL Outputs with 5V Supply
- Two Independent Ground-Referred Control Inputs
- Small Size 8-Pin MiniDIP

APPLICATIONS

- Fault Detectors
- Go/No-Go Testing
- Microprocessor Power Supply Monitor

DESCRIPTION

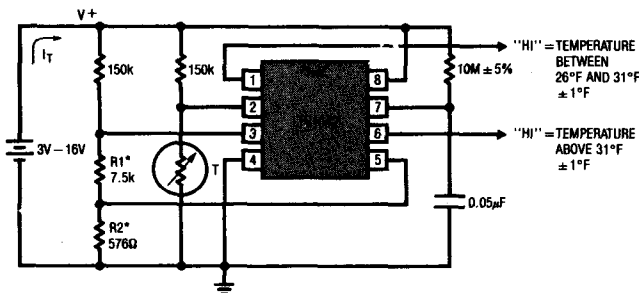
The LTC1042 is a monolithic CMOS window comparator manufactured using Linear Technology's enhanced LTCMOS™ silicon gate process. Two high impedance voltage inputs, CENTER and WIDTH/2, define the middle and width of the comparison window. Whenever the input voltage, V_{IN}, is inside the window the WITHIN WINDOW output is high. The ABOVE WINDOW output is high whenever V_{IN} is above the window. By interchanging V_{IN} and CENTER the ABOVE WINDOW output becomes BELOW WINDOW and is high if V_{IN} is below the window.

Sampling techniques provide high impedance voltage inputs that can common-mode to both supply rails (V⁺ and GND). An important feature of the inputs is their non-interaction. Also the device is effectively "chopper stabilized", giving it extremely high accuracy over all conditions of temperature, power supply and input voltage range.

Another benefit of the sampling techniques used to design the LTC1042 is the extremely low power consumption. When the device is strobed, it internally turns on the power to the comparators, samples the inputs, stores the outputs in CMOS latches and then turns off power to the comparators. This all happens in about 80 μ s. Average power can be made small, almost arbitrarily, by lowering the strobe rate. The device can be self-strobed using an external RC network or strobed externally by driving the OSC pin with a CMOS gate.

LTCMOS™ is a trademark of Linear Technology Corp.

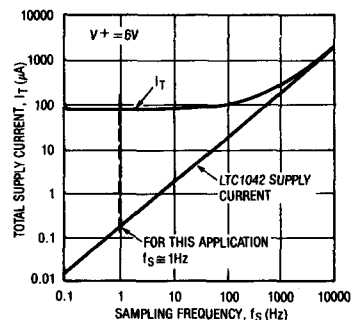
Battery Powered Remote Freezer Alarm



T = YELLOW SPRINGS INSTRUMENT CO., INC. P/N 44007.
 ALL RESISTORS \pm 1% UNLESS OTHERWISE SPECIFIED.

*OTHER TEMPERATURE BANDS MAY BE SELECTED BY CHOOSING APPROPRIATE VALUES FOR R1 AND R2.

Total Supply Current vs Sampling Frequency

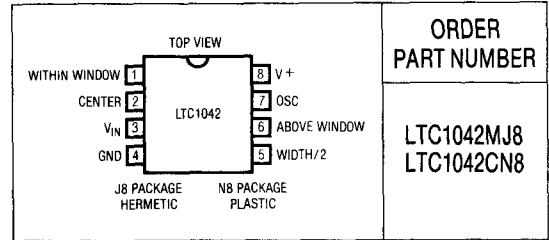


LTC1042

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V^+ to GND)	18V
Input Voltage	$V^+ + 0.3V$ to $-0.3V$
Operating Temperature Range	
LTC1042C	-40°C to 85°C
LTC1042M	-55°C to 125°C
Storage Temperature Range	-55°C to 150°C
Lead Temperature (Soldering, 10 sec)	300°C
Output Short Circuit Duration	Continuous

PACKAGE/ORDER INFORMATION



ELECTRICAL CHARACTERISTICS

Test Conditions: $T_{MIN} \leq T_A \leq T_{MAX}$ unless otherwise specified

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS	
	Center Error (Note 2)	$V^+ = 2.8V$ to $6V$ (Note 1)	●	± 0.3	± 1	mV	
		$V^+ = 6V$ to $15V$ (Note 1)	●	± 0.05	± 0.15	% WIDTH/2	
	Width Error (Note 3)	$V^+ = 2.8V$ to $6V$ (Note 1)	●	± 1	± 3	mV	
		$V^+ = 6V$ to $15V$ (Note 1)	●	± 0.05	± 0.15	% WIDTH/2	
	Width Error (Note 3)	$V^+ = 2.8V$ to $6V$ (Note 1)	●	± 0.6	± 2	mV	
		$V^+ = 6V$ to $15V$ (Note 1)	●	± 0.1	± 0.3	% WIDTH/2	
		Input Bias Current	$V^+ = 5V$, $T_A = 25^\circ\text{C}$, OSC = GND V_{IN} , CENTER and WIDTH/2 Inputs	●	± 0.3		nA
				●			
R_{IN}	Average Input Resistance	$f_S = 1\text{kHz}$ (Note 4)	●	10	15	M Ω	
	Input Voltage Range		●	GND	V^+	V	
PSR	Power Supply Range		●	2.8	16	V	
$I_{S(ON)}$	Power Supply ON Current (Note 5)	$V^+ = 5V$	●	1.2	3	mA	
$I_{S(OFF)}$	Power Supply OFF Current (Note 5)	$V^+ = 5V$ LTC1042C	●	0.001	0.5	μA	
		$V^+ = 5V$ LTC1042M	●	0.001	5.0	μA	
T_D	Response Time (Note 6)	$V^+ = 5V$		80	100	μs	
V_{OH} V_{OL}	Output Levels						
	Logic 1 Output	$V^+ = 4.75V$, $I_{OUT} = -360\mu\text{A}$	●	2.4	4.4	V	
R_{EXT}	External Timing Resistor	$V^+ = 4.75V$, $I_{OUT} = 1.6\text{mA}$	●		0.25	0.45	V
		Resistor Connected between V^+ and OSC Pin	●	100		10,000	k Ω
f_S	Sampling Frequency	$V^+ = 5V$, $T_A = 25^\circ\text{C}$ $R_{EXT} = 1\text{M}\Omega$, $C_{EXT} = 0.1\mu\text{F}$		5		Hz	

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: Applies over input voltage range limit and includes gain uncertainty.

Note 2: Center error = $[(V_U + V_L)/2 - \text{CENTER}]$ (where V_U = upper band limit and V_L = lower band limit).

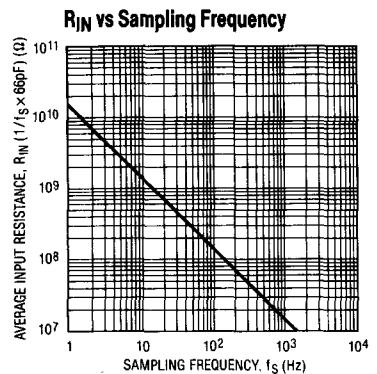
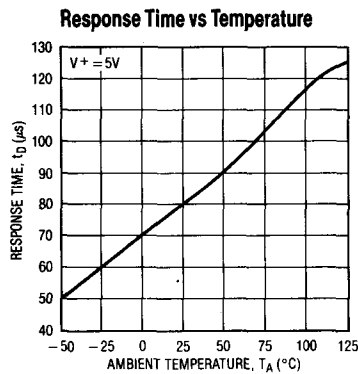
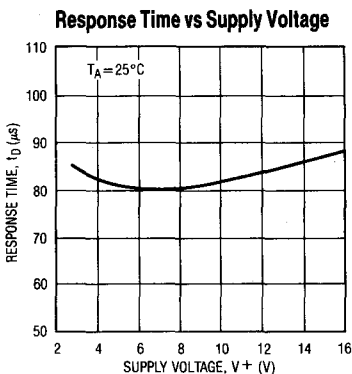
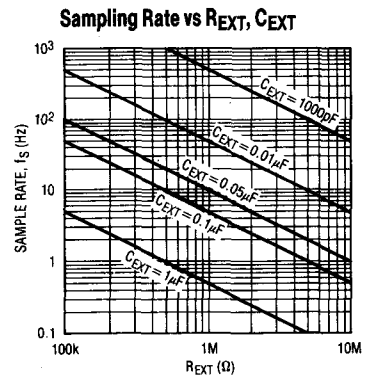
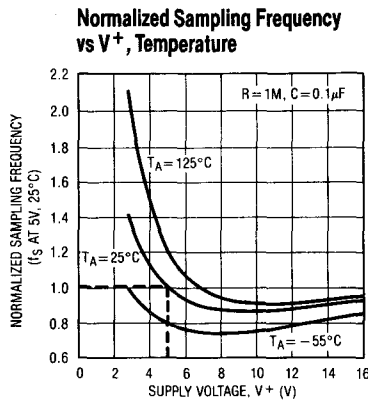
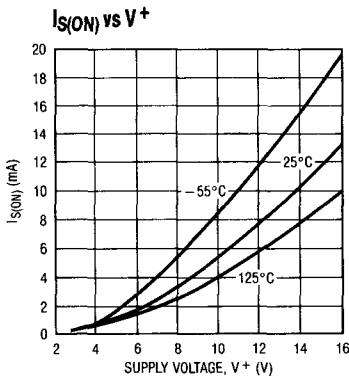
Note 3: Width error = $(V_U - V_L - 2 \times \text{WIDTH}/2)$ (where V_U = upper band limit and V_L = lower band limit).

Note 4: R_{IN} is guaranteed by design and is not tested. $R_{IN} = 1/(f_S \times 66\text{pF})$.

Note 5: Average supply current = $T_D \times I_{S(ON)} \times f_S + (1 - T_D f_S) I_{S(OFF)}$.

Note 6: Response time is set by an internal oscillator and is independent of overdrive voltage. T_D is guaranteed by correlation test and is not directly measured.

TYPICAL PERFORMANCE CHARACTERISTICS



APPLICATIONS INFORMATION

The LTC1042 uses sampled data techniques to achieve its unique characteristics. It consists of two comparators, each of which has two differential inputs (Figure 1). When the sum of the voltages on a comparator's inputs is positive, the output is high; when the sum is negative, the output is low. The inputs are interconnected such that

when $(\text{CENTER} - \text{WIDTH}/2) \leq V_{IN} \leq (\text{CENTER} + \text{WIDTH}/2)$ both comparator outputs are low. In this condition V_{IN} is within the window and the WITHIN WINDOW output is high. When $V_{IN} > \text{CENTER} + \text{WIDTH}/2$, V_{IN} is above the window and the ABOVE WINDOW output is high.

APPLICATIONS INFORMATION

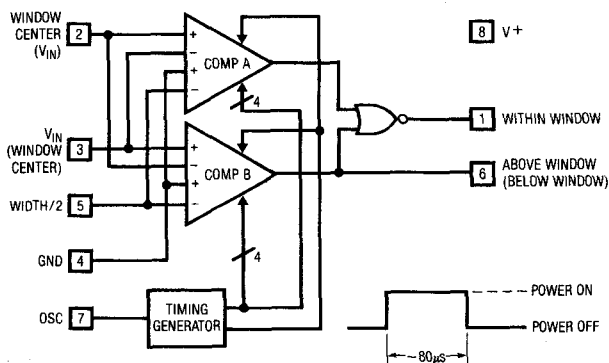
An important feature of the LTC1042 is the non-interaction of the inputs. This means the center and width of the window can be changed without one affecting the other. Also note that the width of the window is set by a ground-referred signal (WIDTH/2).

Strobing

An internal oscillator allows the LTC1042 to strobe itself. The frequency of oscillation sets the sampling rate and is set with an external RC network (see typical curve, OSC frequency vs R_{EXT} , C_{EXT}). To assure oscillation, under all conditions, R_{EXT} must be between 100k Ω and 10M Ω . There is no limit to the size of C_{EXT} .

A sampling cycle is initiated on the positive going transition of the voltage on the OSC pin. When this voltage is near the positive supply, a Schmitt trigger trips and initiates the sampling cycle. A sampling cycle consists of applying power to both comparators, sampling the inputs, storing the results in CMOS output latches and turning power off. This whole process takes approximately 80 μ s. During the 80 μ s "active" time, the LTC1042 draws typically 1.2mA ($I_{S(ON)}$) at $V^+ = 5V$. Because power is consumed only during the "active" time, extremely low average power consumption can be achieved at low sample rates. For example at a sample rate of 1 sample/second the average power consumption is:

$$\text{Power} = (V^+) (I_{S(AVG)}) = 5V \times 1.2mA \times 80\mu s/1sec = 0.48\mu W$$



(A)

Figure 1. LTC1042 Block Diagram

At low sampling rates, R_{EXT} dominates the power consumption. R_{EXT} consumes power continuously. The average voltage at the OSC pin is approximately $V^+/2$. The power consumed by R_{EXT} is:

$$P(R_{EXT}) = (V^+/2)^2/R_{EXT}$$

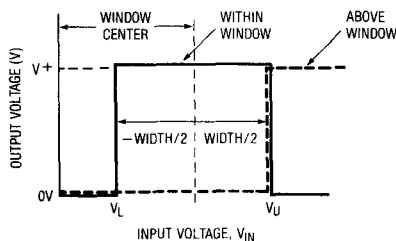
EXAMPLE: Assume $R_{EXT} = 1M\Omega$ and $V^+ = 5V$. Then:

$$P(R_{EXT}) = (2.5)^2/1M\Omega = 6.25\mu W$$

This is more than ten times the typical power consumed by the LTC1042 at $V^+ = 5V$ and 1 sample/second. Where power is a premium, R_{EXT} should be made as large as possible. Note that the power dissipated by R_{EXT} is *not* a function of the sampling frequency or C_{EXT} .

If high sampling rates are needed and power consumption is of secondary importance, a convenient way to get the maximum possible sampling rate is to make $R_{EXT} = 100k\Omega$ and $C_{EXT} = 0$. The sampling rate, set by the LTC1042's active time, will nominally be $\approx 10kHz$.

To synchronize the sampling of the LTC1042 to an external frequency source, the OSC pin can be driven by a CMOS gate. A CMOS gate is necessary because the input trip points of the oscillator are close to the supply rails and TTL does not have enough output swing. Externally driven, there will be a delay from the rising edge of the OSC input and the start of the sampling cycle of approximately 5 μ s.



(B)

APPLICATIONS INFORMATION

Input Impedance

The input impedance of the LTC1042 does not look like a classic linear comparator. CMOS switches and a precision capacitor array form the dual differential input structure. Input impedance characteristics can be determined from the equivalent circuit shown in Figure 2. The input capacitance will charge with a time constant of $R_S \times C_{IN}$. It is critical, in determining errors caused by the input charging current, that C_{IN} be fully charged during the "active" time.

For $R_S \leq 10k\Omega$

For R_S less than or equal to $10k\Omega$, C_{IN} fully charges and no error is caused by the charging current.

For $R_S > 10k\Omega$

For source resistances greater than $10k\Omega$, C_{IN} cannot fully charge, causing voltage errors. To minimize these errors an input bypass capacitor, C_S , should be used. Charge is shared between C_{IN} and C_S , causing a voltage error. The magnitude of this error is $\Delta V = V_{IN} \times C_{IN} / (C_{IN} + C_S)$. This error can be made arbitrarily small by increasing C_S .

The averaging effect of the bypass capacitor C_S causes another error term. Each time the input switches cycle between the plus and minus inputs, C_{IN} is charged and discharged. The average input current due to this is $I_{AVG} = V_{IN} \times C_{IN} \times f_S$, where f_S is the sampling frequency. Because the input current is directly proportional to the differential input voltage, the LTC1042 can be said to have an average input resistance of $R_{IN} = V_{IN} / I_{AVG} = 1 / (f_S \times C_{IN})$.

Since two comparator inputs are connected in parallel, R_{IN} is one half this value (see typical curve of R_{IN} vs Sampling Frequency). This finite input resistance causes an error due to voltage divider between R_S and R_{IN} .

The input error caused by both of these effects is $V_{ERROR} = V_{IN} [2C_{IN} / (2C_{IN} + C_S) + R_S / (R_S + R_{IN})]$.

EXAMPLE: Assume $f_S = 10\text{Hz}$, $R_S = 1M\Omega$, $C_S = 1\mu\text{F}$ and $V_{IN} = 1\text{V}$. Then $V_{ERROR} = 1\text{V}(66\mu\text{V} + 660\mu\text{V}) = 726\mu\text{V}$. If the sampling frequency is reduced to 1Hz , the voltage error from input impedance effects is reduced to $136\mu\text{V}$.

Input Voltage Range

The input switches of the LTC1042 are capable of switching either to the V^+ supply or ground. Consequently, the input voltage range includes both supply rails. This is a further benefit of the input sampling structure.

Error Specifications

The only measurable errors on the LTC1042 are the deviations from "ideal" of the upper and lower window limits [Figure 1(B)]. The critical parameters for a window comparator are the width and center of the window. These errors may be expressed in terms of V_U and V_L .

$$\text{center error} = [(V_U + V_L) / 2] - \text{CENTER}$$

$$\text{width error} = (V_U - V_L) - 2 \times (\text{WIDTH} / 2)$$

The specified error limits (see Electrical Characteristics) include error due to offset, power supply variation, gain, time and temperature.

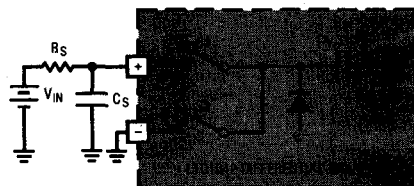
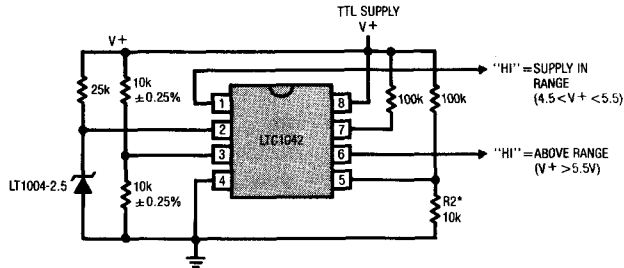


Figure 2. Equivalent Input Circuit

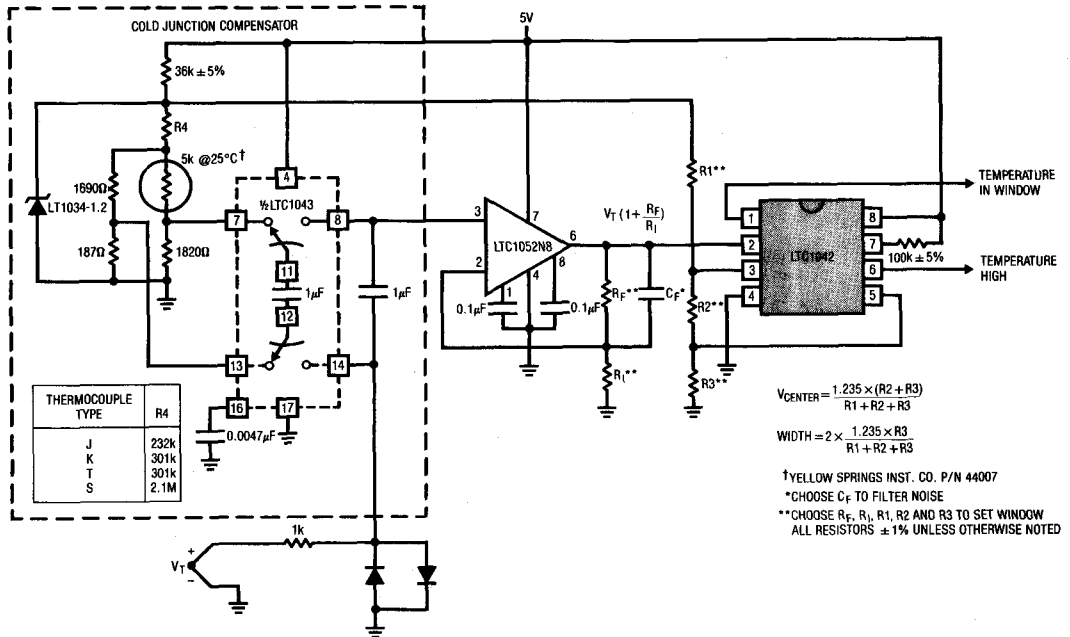
APPLICATIONS INFORMATION

TTL Power Supply Monitor



ALL RESISTORS ± 5% UNLESS OTHERWISE NOTED.
 *SUPPLY TOLERANCE EQUALS R2 IN kΩ. I.E., 10k = ± 10%.

Single 5V Thermocouple Over Temperature Alarm



APPLICATIONS INFORMATION

Wind Powered Battery Charger

A simple wind powered battery charger can be constructed using the new LTC1042, a 12V DC permanent magnet motor, and low cost power FET transistor.

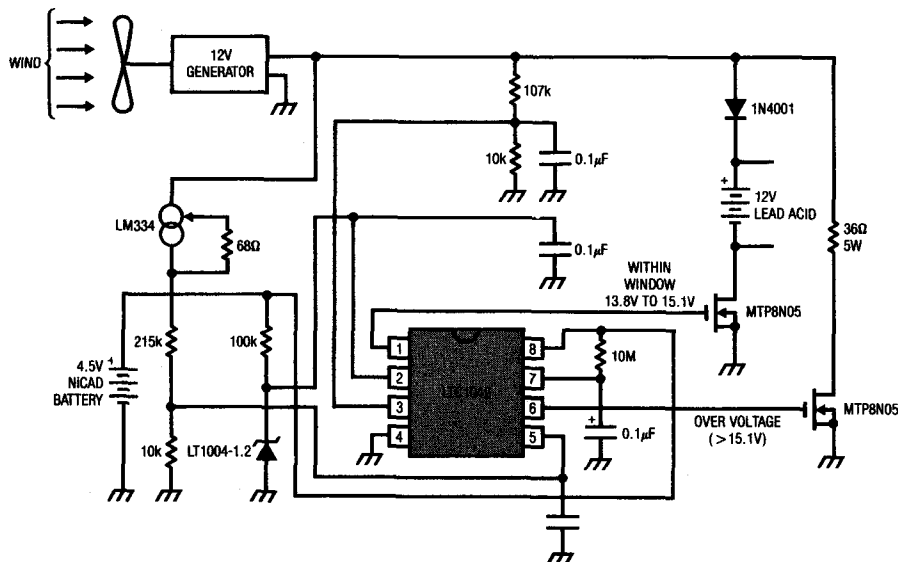
The DC motor is used as a generator with the voltage output being proportional to its RPM. The LTC1042 monitors the voltage output and provides the following control functions.

1) If generator voltage output is below 13.8V, the control circuit is active and the NiCad battery is charging through the LM334 current source. The lead acid battery is not being charged.

2) If the generator voltage output is between 13.8V and 15.1V, the 12V lead acid battery is being charged at about a 1 amp/hour rate (limited by the power FET).

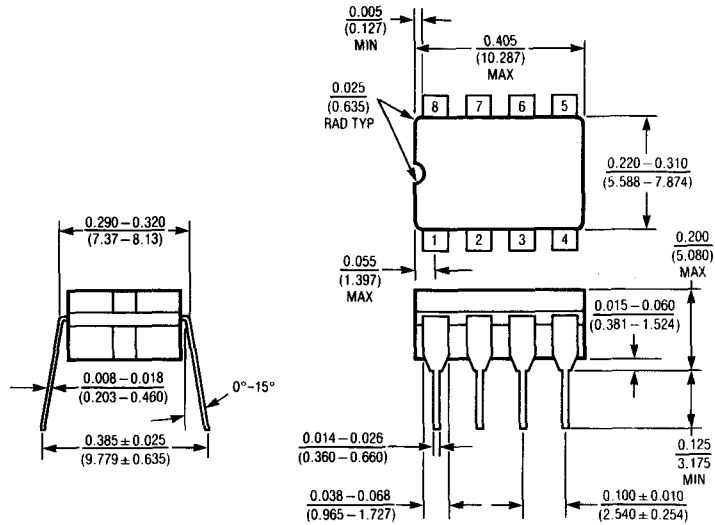
3) If generator voltage exceeds 15.1V (a condition caused by excessive wind speed or 12V battery being fully charged) then a fixed load is connected thus limiting the generator RPM to prevent damage.

This charger can be used as a remote source of power where wind energy is plentiful such as on sailboats or remote radio repeater sites. Unlike solar powered panels, this system will function in bad weather and at night.



PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

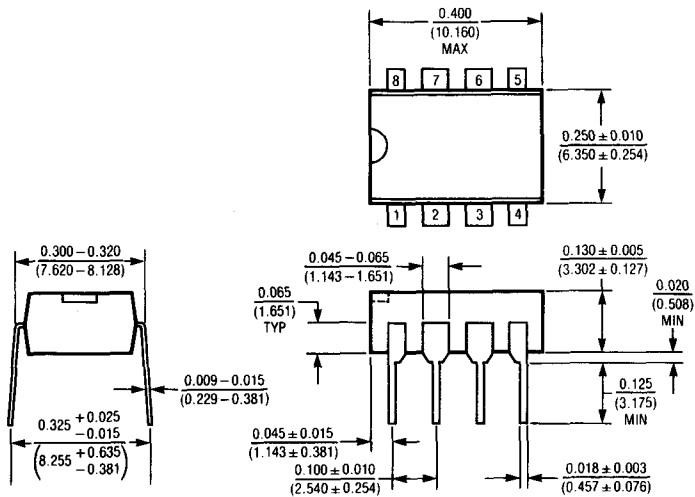
**J8 Package
8 Lead Hermetic DIP**



J8188

T_{jmax} 150°C	θ_{JA} 100°C/W
---------------------	--------------------------

**N8 Package
8 Lead Plastic**



N8166

T_{jmax} 110°C	θ_{JA} 150°C/W
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FEATURES

- *Guaranteed* Max Input Offset Voltage 1.0mV
- *Guaranteed* Max Input Offset Current 5nA
- *Guaranteed* Max Response Time 250ns
- *Guaranteed* Min. Voltage Gain 200,000
- $\pm 30V$ Differential Input Voltage
- Drives 50mA Loads At Up To 50V.
- $\frac{1}{2}$ The Power Dissipation For LT111A/LT311A

DESCRIPTION

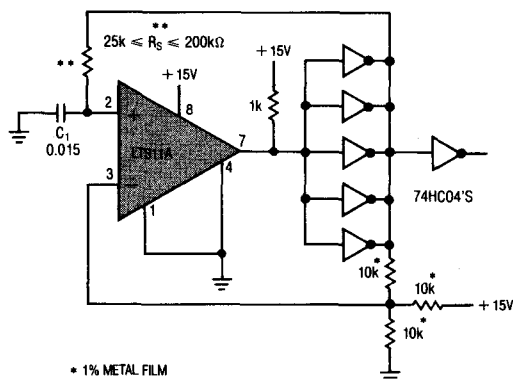
The LT111A is an improved version of the LM111 general purpose comparator. These new devices offer maximum input offset voltage of 1.0mV and input offset current of 5.0nA with a maximum response time of 250ns. The LT111A operates from a single 5V supply to $\pm 15V$ supplies and can drive up to 50mA loads referred to ground or either supply. A separate output ground pin allows output signals to be isolated from analog ground.

The versatility of the LT111A is enhanced by an input stage design which allows differential input signals of up to $\pm 30V$. Offset balancing, strobe capability and the ability to "OR" the output is also included. These features plus Linear Technology Corporation's advanced processing and reliability enhancements make the LT111A an ideal choice for most comparator applications. For higher performance requirements, see the LT1011. For operation up to 200°C, see LT111X data sheet.

APPLICATIONS

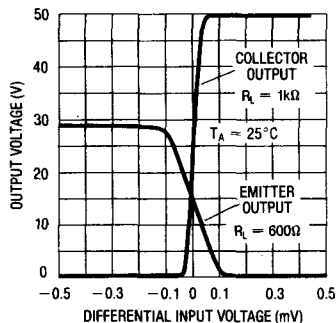
- General Purpose Comparator
- Zero Crossing Detector
- Voltage To Frequency Converter

Low Drift R/C Oscillator



* 1% METAL FILM
 ** = TRW TYPE MTR-5/ + 120ppm/°C.
 C₁ = .015 = POLYSTYRENE - 120ppm/°C ± 30ppm WESCO TYPE 32-P
 NOTE: COMPARATOR CONTRIBUTES ≤ 10 ppm/°C DRIFT FOR FREQUENCIES BELOW 10kHz.

Transfer Function



ABSOLUTE MAXIMUM RATINGS

Supply Voltage (pin 8 to pin 4) 36V

Output to Negative Supply (pin 7 to pin 4)
LT111A/LM111 50V
LT311A/LM311 40V

Ground to Negative Supply (pin 1 to pin 4) 30V

Differential Input Voltage ±30V

Voltage at Strobe Pin (pin 6 to pin 8) 5V

Input Voltage (Note 1) ±15V

Output Short Circuit Duration 10 sec.

Operating Temperature Range (Note 2)
LT111A/LM111 -55°C to 125°C
LT311A/LM311 0°C to 70°C

Storage Temperature Range -65°C to 150°C

Lead Temperature (Soldering, 10 sec.) 300°C

PACKAGE/ORDER INFORMATION

<p>H PACKAGE TO-5 METAL CAN</p>	<p>ORDER PART NUMBER</p> <p>LT111AH LM111H LT311AH LM311H</p>
<p>TOP VIEW</p> <p>NOTE: PIN 4 CONNECTED TO CASE. J8 PACKAGE 8 PIN CERDIP N8 PACKAGE 8 PIN PLASTIC</p>	<p>LT111AJ8 LM111J8 LT311AJ8 LM311J8 LT311AN8 LM311N8</p>

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $T_A = 25^\circ C$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT 111A			LM111			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	$R_S \leq 50k$ (Note 3, 4)	●	0.5	1.0	0.7	3.0	mV	
I_{OS}	Input Offset Current	(Note 3,4)	●	2.0	5.0	4.0	10.0	nA	
I_B	Input Bias Current	Note 3	●	60	100	60	100	nA	
A_{VOL}	Large Signal Voltage Gain	Note 7	●	200	500	40	200	V/mV	
	Response Time	Note 5	●	200	250	200		nS	
	Saturation Voltage	$V_{IN} \leq -5mV$, $I_{OUT} = 50mA$ $V_+ \geq 4.5V$, $V_- = 0$ $V_{IN} \leq -6mV$, $I_{SNK} \leq 8mA$	●	0.75	1.5	0.75	1.5	V	
	Strobe ON Current	Note 6	●	3.0	4.0	3.0		mA	
	Output Leakage Current	$V_{IN} \geq 5mV$, $V_{OUT} = 35V$ $I_{STROBE} = 3mA$	●	0.2	10.0	0.2	10.0	nA	
	Input Voltage Range	$V_+ = 15V$, $V_- = 15V$ Pin 7 Pull up may go to 5V	●	-14.5	{ 13.8 } { -14.7 }	13.0	-14.5	{ 13.8 } { -14.7 }	V
	Positive Supply Current		●	3.0	4.0	5.1	6.0	mA	
	Negative Supply Current		●	1.5	2.5	4.1	5.0	mA	

Shading of a specification highlights those items which offer key improvements in parametric performance or guaranteed test limits provided for the first time.

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $T_A = 25^\circ C$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT 311A			LM311			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	$R_S \leq 50k$ (Note 3, 4)	●	0.5	1.0 2.0	2.0	7.5 10	mV	
I_{OS}	Input Offset Current	(Note 3, 4)	●	2.0	10 20	6.0	50 70	nA	
I_B	Input Bias Current	Note 3		60	100 150	100	250 300	nA	
A_{VOL}	Large Signal Voltage Gain			200	500	40	200	V/mV	
	Response Time	Note 5		200	250	200		nS	
	Saturation Voltage	$V_{IN} \leq -10mV$, $I_{OUT} = 50mA$ $V_+ \geq 4.5V$, $V_- = 0$ $V_{IN} \leq -10mV$, $I_{SNK} \leq 8mA$	●	0.75	1.5	0.75	1.5	V	
	Strobe ON Current	Note 6		3.0	4.0	3.0		mA	
	Output Leakage Current	$V_{IN} \geq 10mV$, $V_{OUT} = 35V$ $I_{STROBE} = 3mA$	●	0.2	50	0.2	50	nA μA	
	Input Voltage Range		●	-14.5 { 13.8 } {-14.7}	13.0	-14.5 { 13.8 } {-14.7}	13.0	V	
	Positive Supply Current			3.0	4.0	5.1	7.5	mA	
	Negative Supply Current			1.5	2.5	4.1	5.0	mA	

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: Applicable for $\pm 15V$ supplies. The positive input voltage limit is 30V above the negative supply. The negative input voltage limit is the negative supply.

Note 2: T_j max. = $150^\circ C$ for the LT111A and $95^\circ C$ for the LT311A.

Note 3: Offset voltage, offset current and bias current specifications apply for any supply voltage from a single 5V up to $\pm 15V$ supplies.

Note 4: Offset voltages and offset currents shown are the maximum values required to drive the output within a volt of either supply with a 1mA load. These parameters define an error band and take into account the worst case effects of voltage gain and input impedance.

Note 5: Response time is specified for a 100mV input step with 5mV overdrive with the collector output terminated with a 500 Ω pullup resistor tied to 5V.

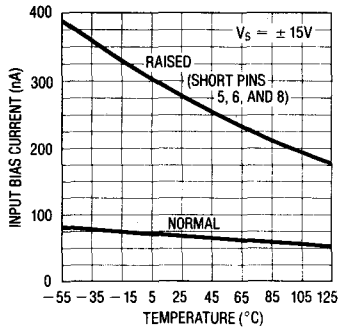
Note 6: Do not short the strobe pin to ground. It should be current driven at 3 to 5mA for the shortest strobe time. Currents as low as 500 μA will strobe the LT111A if speed is not important. External leakage on the strobe pin in excess of 0.2 μA when the strobe is "off" can cause offset voltage shifts.

Note 7: $R_L = 1k\Omega$, $-10V \leq V_{OUT} \leq 14.5V$

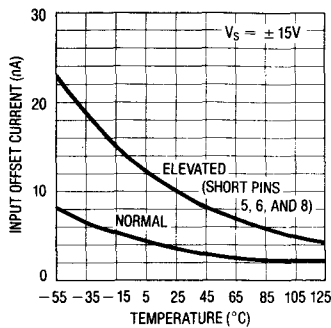
6

TYPICAL PERFORMANCE CHARACTERISTICS

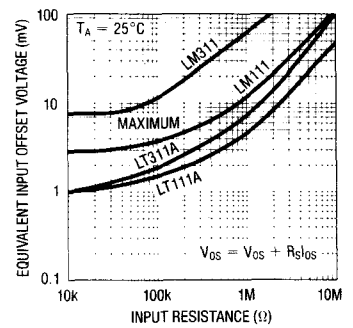
Input Bias Current



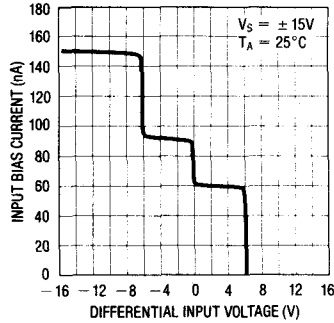
Input Offset Current



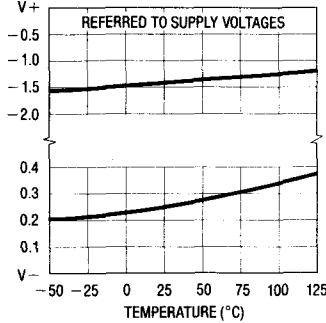
Offset Error



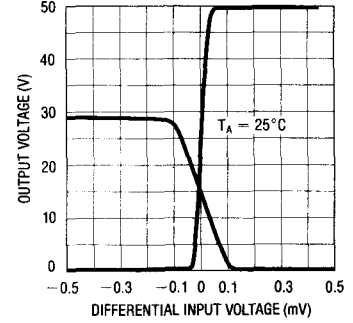
Input Characteristics



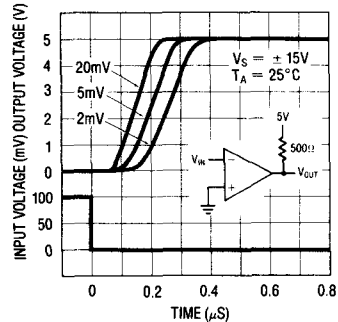
Common Mode Limits



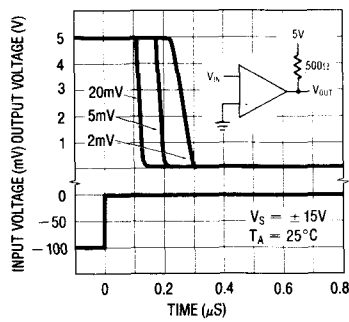
Transfer Function



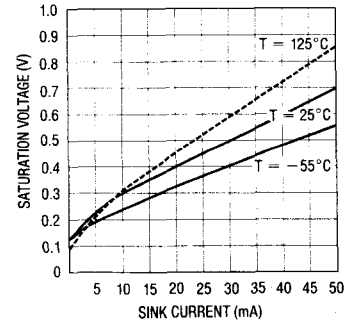
Response Time for Various Input Overdrives



Response Time for Various Input Overdrives

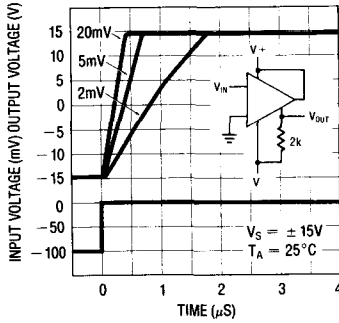


Collector Output Saturation Voltage

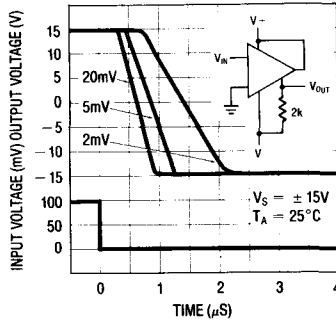


TYPICAL PERFORMANCE CHARACTERISTICS

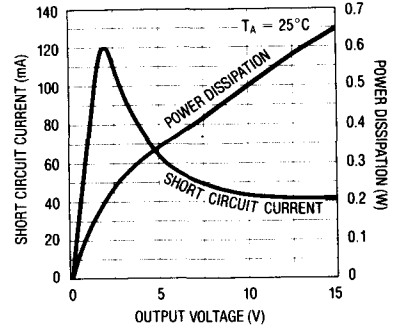
Response Time Using GND Pin as Output



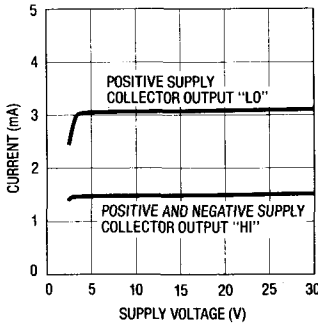
Response Time Using GND Pin as Output



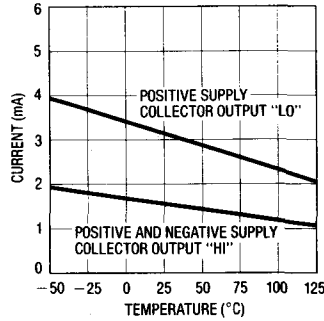
Output Limiting Characteristics



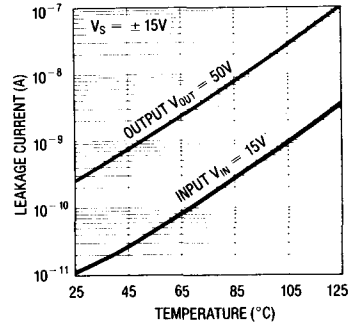
Supply Current vs Supply Voltage



Supply Current vs Temperature



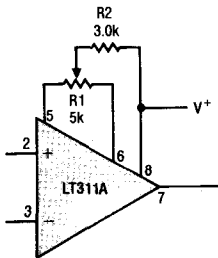
Leakage Current vs Temperature



6

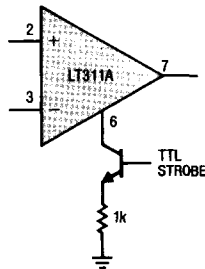
TYPICAL APPLICATIONS

Offset Balancing



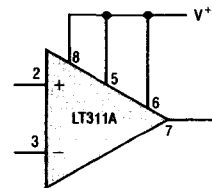
Note: Pin Connections Shown are for TO-5 package

Strobing



Note: Do Not Ground Strobe Pin.

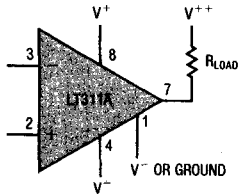
Increasing Input Stage Current



Increases typical common mode slew rate from 7.0 V/μs to 18V/μs.

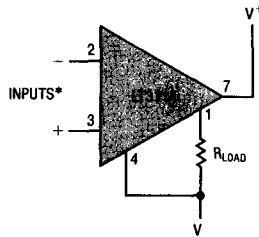
TYPICAL APPLICATIONS

**Driving Load Referenced
To Positive Supply**



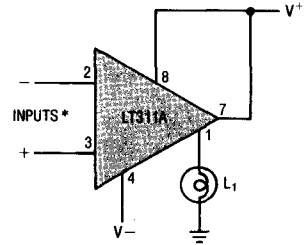
V^{++} CAN BE GREATER OR LESS THAN V^+

**Driving Load Referenced
To Negative Supply**



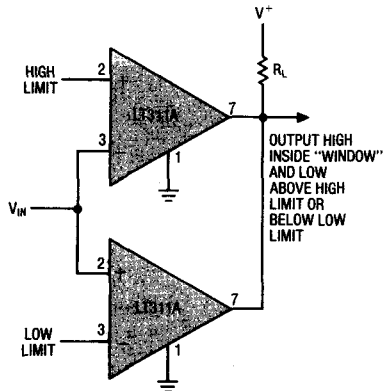
* NOTE THAT INPUT
POLARITY IS REVERSED
WHEN USING PIN 1 AS
OUTPUT

Driving Ground Referred Load

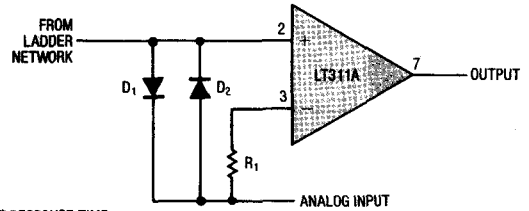


* NOTE THAT INPUT
POLARITY IS REVERSED
WHEN USING PIN 1 AS
OUTPUT

Window Detector

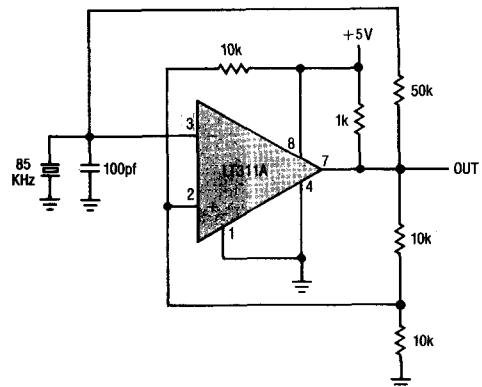


Using Clamp Diodes To Improve Frequency Response*

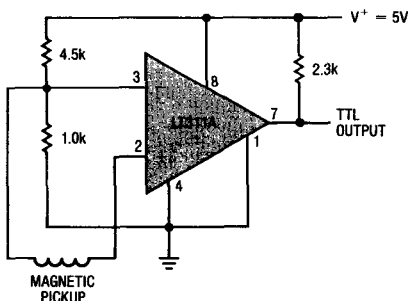


* RESPONSE TIME
INCREASES TO ~500ns
IF INPUT MUST SLEW 5V
TO REACH THRESHOLD.

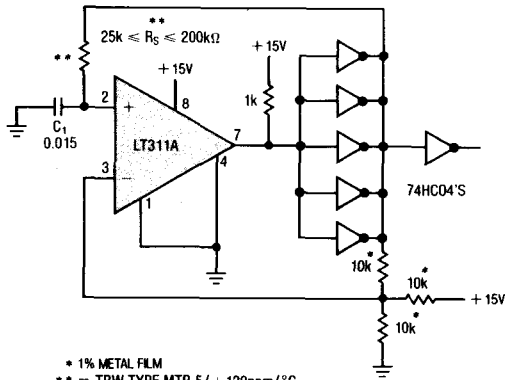
Crystal Oscillator



Detector For Magnetic Transducer

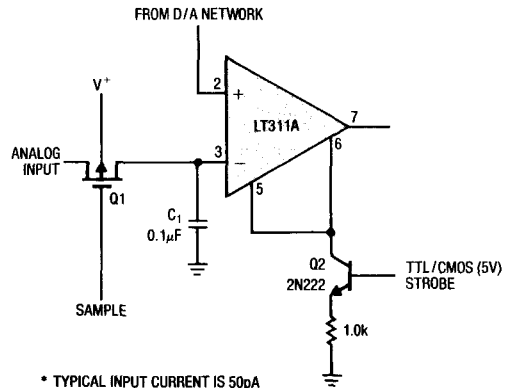


Low Drift R/C Oscillator



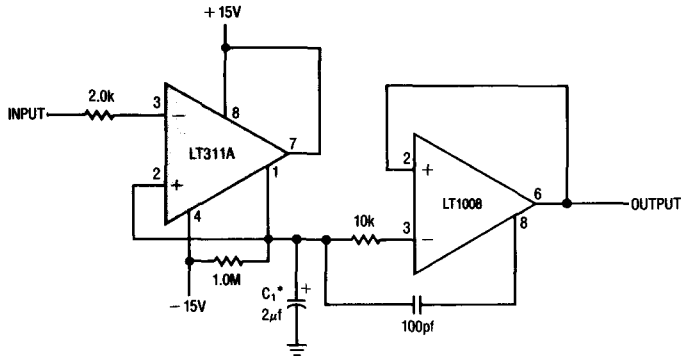
* 1% METAL FILM
 ** = TRW TYPE MTR-5/ + 120ppm/°C.
 C₁ = .015 = POLYSTYRENE - 120ppm/°C ± 30ppm WESCO TYPE 32-P
 NOTE: COMPARTOR CONTRIBUTES ≈ 10ppm/°C DRIFT FOR
 FREQUENCIES BELOW 10kHz.

Strobing Off Both Input* And Output Stages



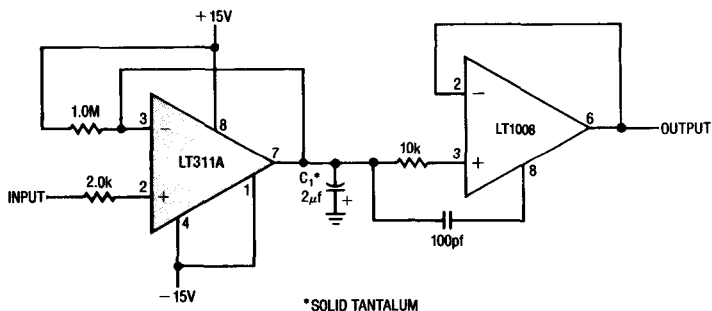
* TYPICAL INPUT CURRENT IS 50pA
 WITH INPUTS STROBED OFF.
 DO NOT GROUND STROBE PIN

Positive Peak Detector



* SOLID TANTALUM

Negative Peak Detector

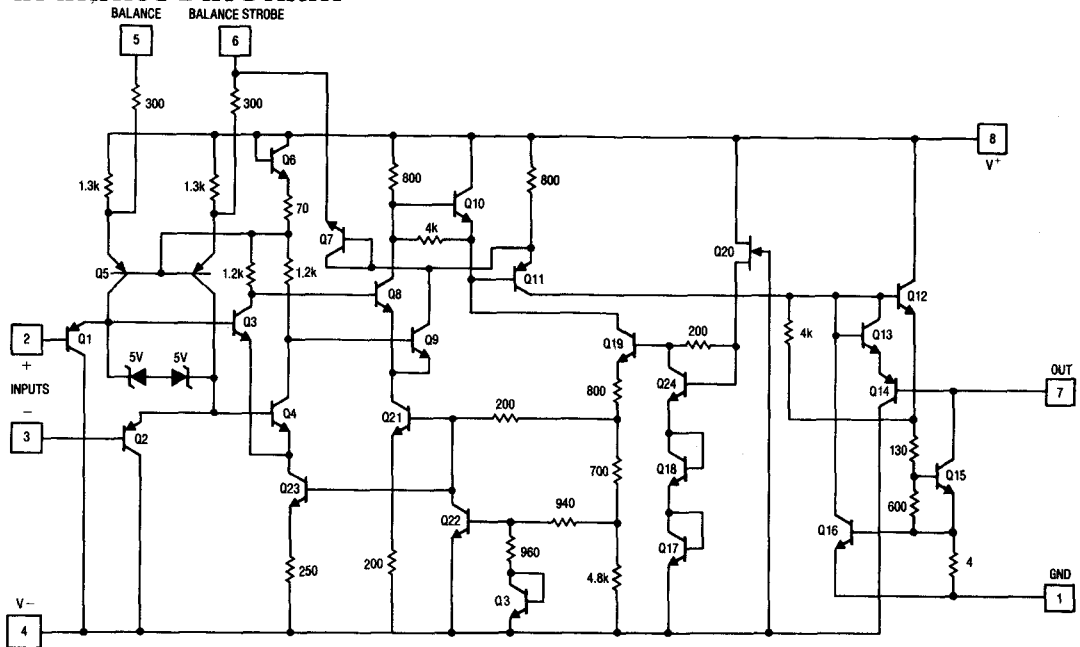


* SOLID TANTALUM

6

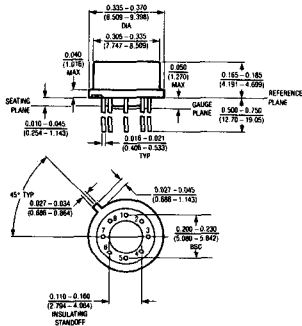
LT111A/LT311A LM111/LM311

SCHEMATIC DIAGRAM



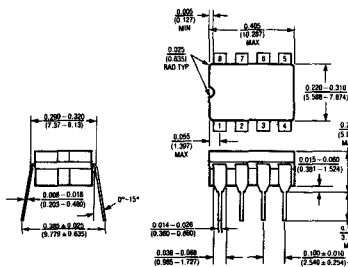
PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

H Package
Metal Can



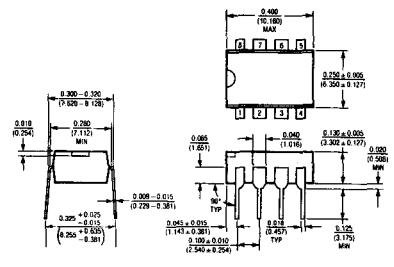
T_{jmax}	θ_{ja}	θ_{jc}
150°C	150°C/W	45°C/W

J8 Package
8 Lead Hermetic Dip



T_{jmax}	θ_{ja}
150°C	100°C/W

N8 Package
8 Lead Plastic



T_{jmax}	θ_{ja}
100°C	130°C/W

FEATURES

- *Guaranteed* max 0.5 mV input offset voltage
- Input Protection Diodes
- Operates from single 5V supply
- 25mA drive capability
- 80nS response time

APPLICATIONS

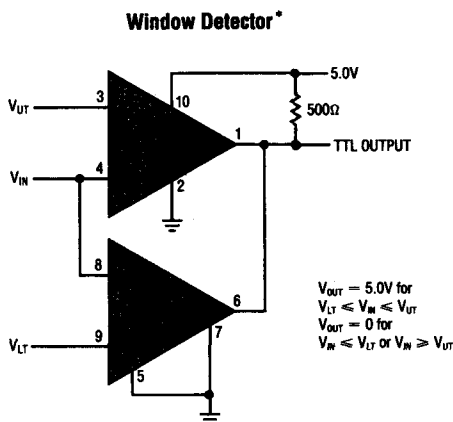
- Window detectors
- High speed one shot
- Relay/lamp drivers
- Voltage controlled oscillators

DESCRIPTION

The LT119A is an improved version of the LM119 dual comparator. It features lower input offset voltage and offset current, higher voltage gain, guaranteed common mode rejection, and input protection diodes.

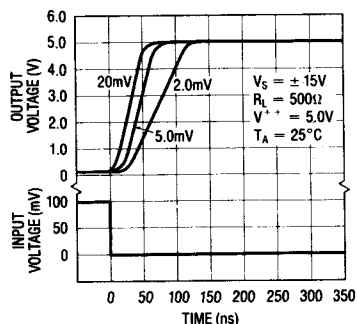
The LT119A is capable of operation over a supply range from 5 Volts to ± 15 Volts and can drive 25mA loads from each open collector output. A separate ground pin allows the LT119A to isolate system grounds.

Linear Technology Corporation's advanced processing, design techniques and reliability make the LT119A/LT319A an ideal choice over previous devices in most comparator applications.



* Allowed window for single +5V supply is 1.2V to 3.8V

Response Time for Various Input Overdrives



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	36V
Output to Negative Supply Voltage	36V
Ground to Negative Supply Voltage	25V
Ground to Positive Supply Voltage	18V
Differential Input Voltage	±5V
Differential Input Current	±5mA
Input Voltage (See Note 1)	
Output Short Circuit Duration	10 Sec
Operating Temperature Range	
LT119A, LM119	-55°C to 125°C
LT319A, LM319	0°C to 70°C
Storage Temperature Range	-65°C to 150°C
Lead Temperature (Soldering, 10 sec)	300°C

PACKAGE ORDER INFORMATION

<p>TOP VIEW</p> <p>H PACKAGE METAL CAN</p>	<p>ORDER PART NUMBER</p> <p>LT119AH LM119H LT319AH LM319H</p>
<p>J PACKAGE 14-PIN HERMETIC</p> <p>N PACKAGE 14-PIN PLASTIC</p>	<p>LT119AJ LM119J LT319AJ LM319J</p>

ELECTRICAL CHARACTERISTICS (See Note 2)

SYMBOL	PARAMETER	CONDITIONS	LT 119A			LM119			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	$V_S = \pm 15V$, $V_{CM} = 0$		0.3	0.5			4.0	mV
V_{OS}	Input Offset Voltage	(See Note 3)	●	0.5 1.2	1.0 2.0		0.7	4.0 7.0	mV mV
CMRR	Common Mode Rejection Ratio			106					dB
I_{OS}	Input Offset Current	(See Note 3)	●	90 20	40 75		30	75 100	nA nA
I_B	Input Bias Current	(See Note 3)	●	150	500 1000		150	500 1000	nA nA
A_V	Voltage Gain			20	40		10	40	V/mV
	Response Time	(See Note 4)		80			80		nS
V_{SAT}	Saturation Voltage	$V_{IN} \leq -5mV$, $I_O = 25mA$ $V^+ \geq 4.5V$, $V^- = 0V$ $V_{IN} \leq -6mV$, $I_{SNK} \leq 3.2mA$ $T_A \geq 0^\circ C$ $T_A \leq 0^\circ C$		0.75	1.5		0.75	1.5	V
	Output Leakage Current	$V_{IN} \geq 5mV$, $V_{OUT} = 35V$	●	0.2 1	2 10		0.2 1	2 10	μA μA
	Input Voltage Range	$V_S = \pm 15V$ $V^+ = 5V$, $V^- = 0$	●	-12 ± 13	+ 12		-12 ± 13	+ 12	V
	Differential Input Voltage		●	1	3		1	3	V
I_S	Supply Current	$V^+ = 5V$, $V^- = 0$		4.3			4.3		mA
I_S	Positive Supply Current	$V_S = \pm 15V$		8	11.5		8	11.5	mA
I_S	Negative Supply Current	$V_S = \pm 15V$		3	4.5		3	4.5	mA

ELECTRICAL CHARACTERISTICS (See Note 2)

SYMBOL	PARAMETER	CONDITIONS	LT 319A			LM319			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	$V_S = \pm 15V$ $V_{CM} = 0$		0.3	0.5			8.0	mV
V_{OS}	Input Offset Voltage	$R_S \leq 5k$ (See Note 3)	●	0.5	1		2.0	8.0	mV
				2			10		mV
CMRR	Common Mode Rejection Ratio			90	106				dB
I_{OS}	Input Offset Current	(See Note 3)	●	30	40		80	200	nA
				60			300		nA
I_b	Input Bias Current	(See Note 3)	●	150	500		250	1000	nA
				1000			1200		nA
A_V	Voltage Gain			20	40		8	40	V/mV
	Response Time	(See Note 4)		80			80		nS
V_{SAT}	Saturation Voltage	$V_{IN} \leq -10mV$, $I_{SNK} = 25mA$ $T_A = 25^\circ C$ $V^+ \geq 4.5V$, $V^- = 0$ $V_{IN} \leq -10mV$, $I_{SNK} \leq 3.2mA$	●	0.75	1.5		0.75	1.5	V
	Output Leakage Current	$V_{IN} \geq 10mV$, $V_{OUT} = 35V$	●	0.2	10		0.2	10	μA
	Input Voltage Range	$V_S = \pm 15V$ $V^+ = 5V$, $V^- = 0V$	●	± 13			± 13		V
			●	1	3		1	3	V
	Differential Input Voltage		●		± 5			± 5	V
I_S	Supply Current	$V^+ = 5V$, $V^- = 0V$		4.3			4.3		mA
I_S	Positive Supply Current	$V_S = \pm 15V$		8	12.5		8	12.5	mA
I_S	Negative Supply Current	$V_S = \pm 15V$		3	5		3	5	mA

The ● denotes the specifications which apply over the full operating temperature range.

The shaded electrical specifications indicate those parameters which have been improved or guaranteed test limits provided for the first time.

Note 1: For supply voltages less than $\pm 15V$, the maximum input voltage is equal to the supply voltage.

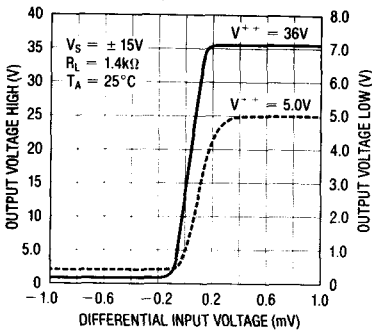
Note 2: Unless otherwise noted, supply voltage equals $\pm 15V$ and $T_A = 25^\circ C$. The ground pin is grounded. Note that the maximum voltage allowed between the ground pin and V^+ is 18V. Do not tie the ground pin to V^- when the power supply voltage exceeds $\pm 9V$. The offset voltage, offset current and bias current specifications apply for all supply voltages between $\pm 15V$ and $+5V$ unless otherwise specified.

Note 3: The offset voltages and currents given are the maximum values required to drive the output within 1 volt of either supply with a 1mA load — thus, these parameters define an error band and take into account the worst case effects of voltage gain and input impedance.

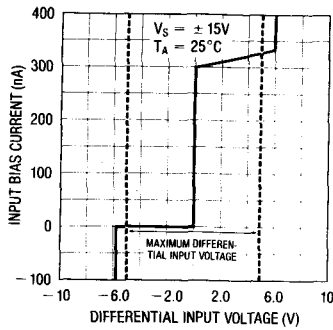
Note 4: Response time specified is for a 100mV input step with 5mV overdrive.

TYPICAL PERFORMANCE CHARACTERISTICS

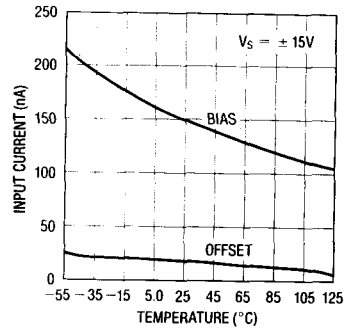
Transfer Function



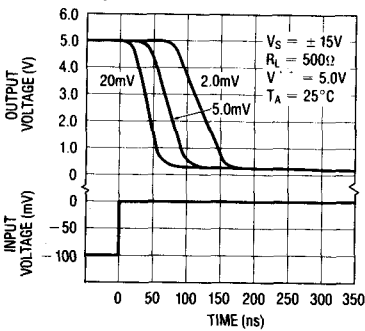
Input Characteristics



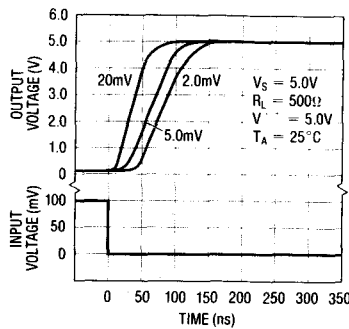
Input Currents



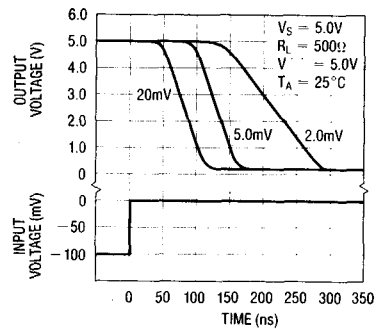
Response Time for Various Input Overdrives



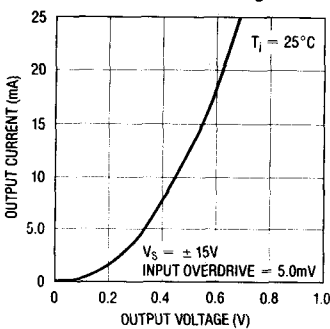
Response Time for Various Input Overdrives



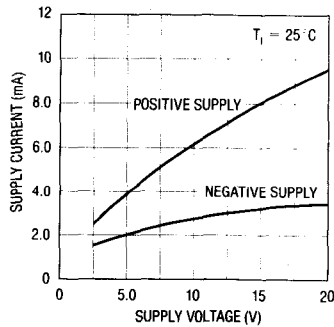
Response Time for Various Input Overdrives



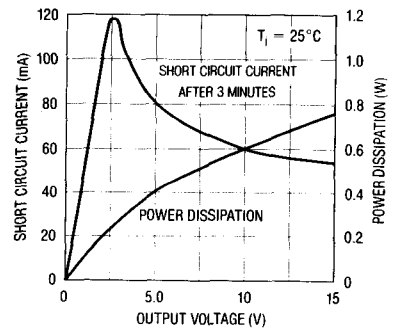
Output Saturation Voltage



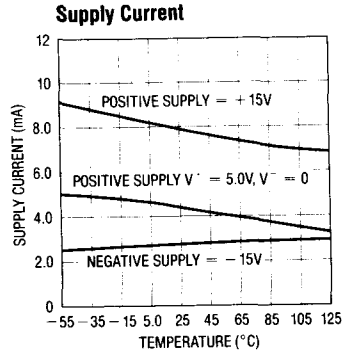
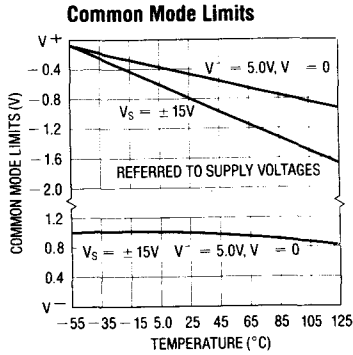
Supply Current



Output Limiting Characteristics

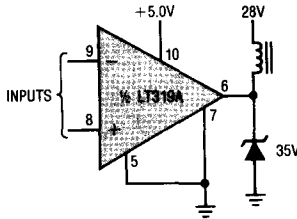


TYPICAL PERFORMANCE CHARACTERISTICS

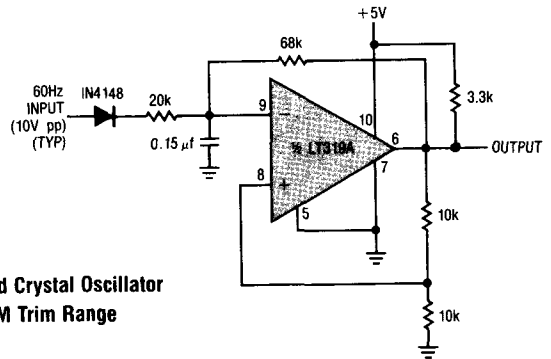


TYPICAL APPLICATIONS

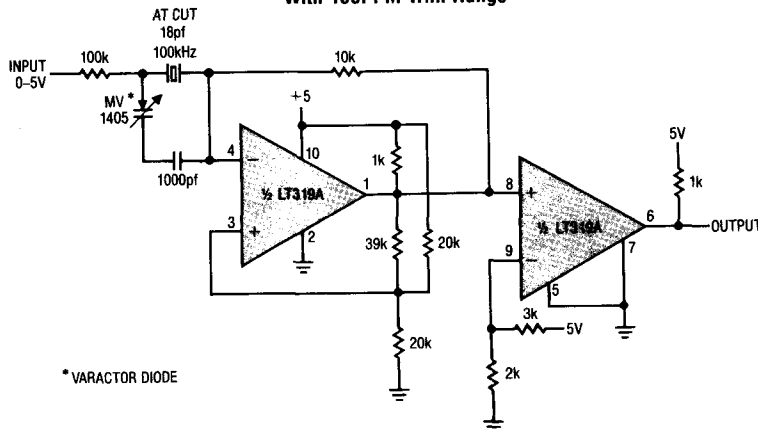
Relay Driver



High Noise Immunity 60Hz Sync Circuit

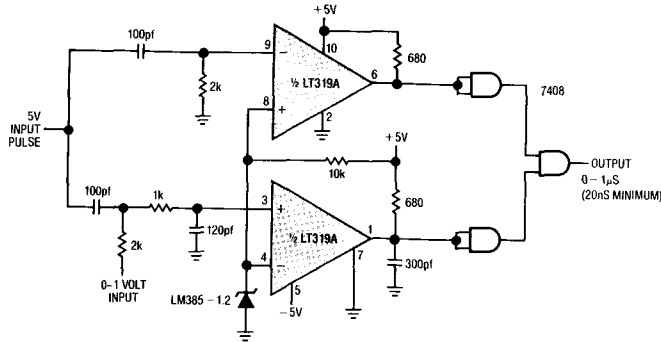


**Voltage Controlled Crystal Oscillator
With 100PPM Trim Range**

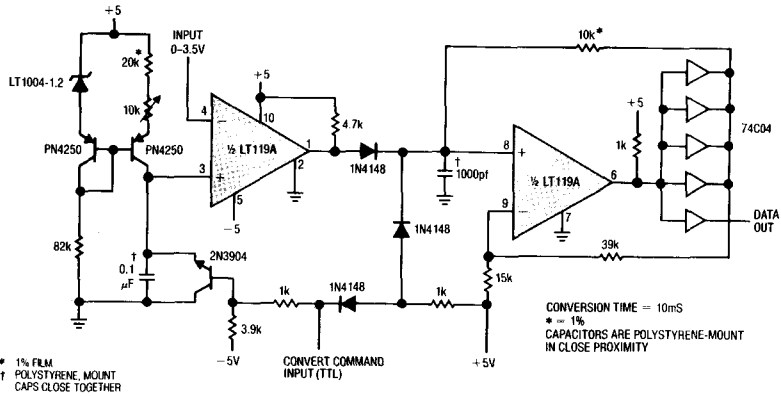


TYPICAL APPLICATIONS

Voltage Controlled High Speed One Shot

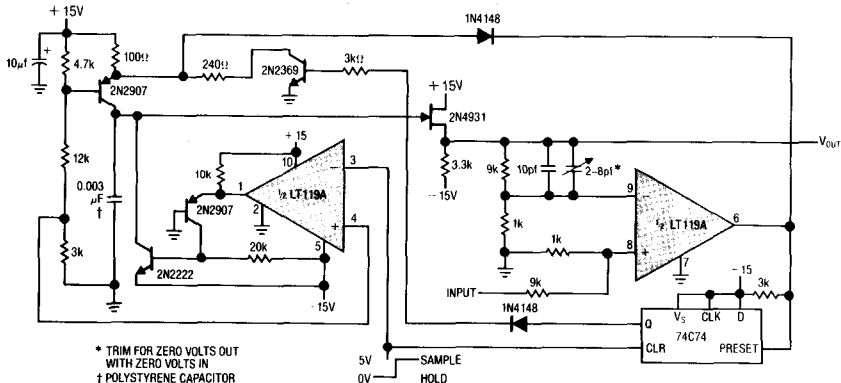


10 Bit Serial Output A/D Converter



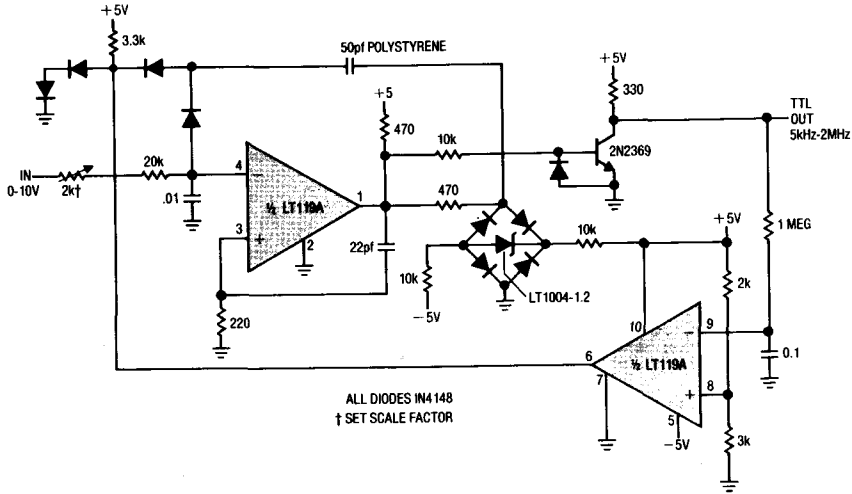
* 1% FILM
† POLYSTYRENE MOUNT CAPS CLOSE TOGETHER

5 Microsecond Sample and Hold with Zero Hold Step



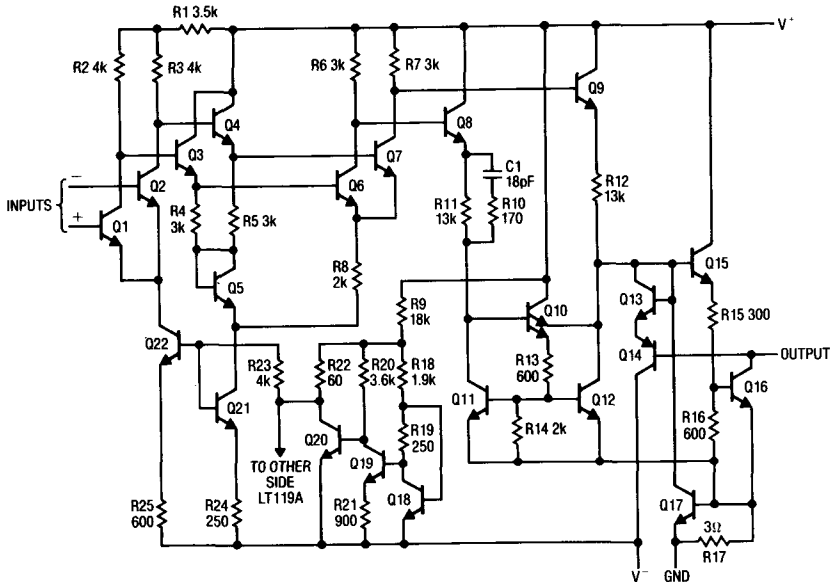
TYPICAL APPLICATIONS

5kHz to 2MHz V → F Converter



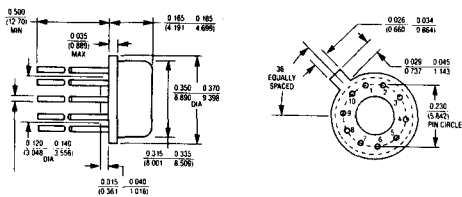
SCHEMATIC DIAGRAM

6



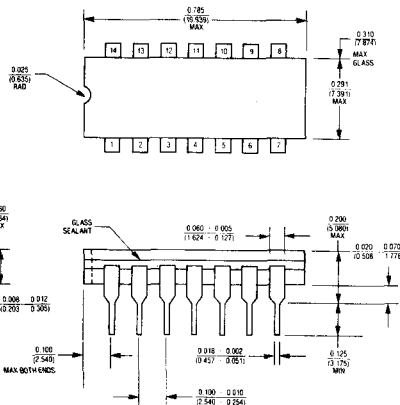
PACKAGE DESCRIPTION

10 Lead TO-5 Metal Can (H)



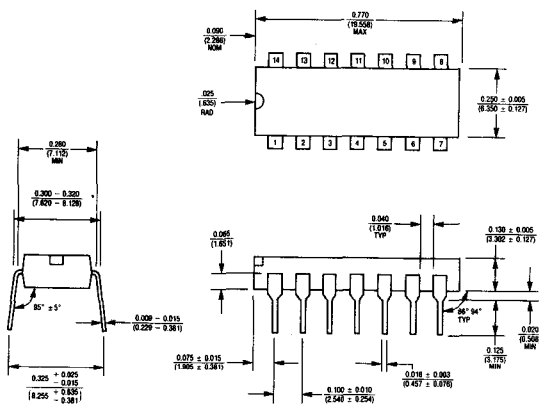
	T _J MAX	θ _{JA}	θ _{JC}
LT119AH LM119H	150°C	150°C/W	45°C/W
LT319AH LM319H	85°C	150°C/W	45°C/W

14-Lead Cavity DIP (J)



	T _J MAX	θ _{JA}
LT119AJ	150°C	100°C/W
LM119J	150°C	100°C/W
LT319AJ	85°C	100°C/W
LM319J	85°C	100°C/W

14-Lead Molded DIP (N)



	T _J MAX	θ _{JA}
LT319AN LM319N	85°C	100°C/W

SECTION 7—FILTERS

SECTION 7—FILTERS

INDEX	7-2
PROPRIETARY PRODUCTS	
<i>LTC1059, High Performance Switched Capacitor Universal Filter</i>	7-3
<i>LTC1059CS, High Performance Switched Capacitor Universal Filter</i>	7-11
<i>LTC1060, Universal Dual Filter Building Block</i>	7-15
<i>LTC1060CS, Universal Dual Filter Building Block</i>	7-35
<i>LTC1061, High Performance Triple Universal Filter Building Block</i>	7-39
<i>LTC1061CS, High Performance Triple Universal Filter Building Block</i>	7-55
<i>LTC1062, 5th Order Low Pass Filter</i>	7-59
<i>LTC1062CS, 5th Order Low Pass Filter</i>	7-71
<i>LTC1064, Low Noise, Fast, Quad Universal Filter Building Block</i>	7-73
<i>LTC1064-1, Low Noise, 8th Order, Clock Sweepable Elliptic Lowpass Filter</i>	7-89
<i>LTC1064-2, Low Noise, High Frequency 8th Order Butterworth Lowpass Filter</i>	13-15
<i>LTC1064-3, Low Noise, High Frequency 8th Order Linear Phase Lowpass Filter</i>	13-19
<i>LTC1064-4, Low Noise, 8th Order, Clock Sweepable Cauer Lowpass Filter</i>	13-20

High Performance Switched Capacitor Universal Filter

FEATURES

- All Filter Parameters *Guaranteed* over Temperature
- Wide Center Frequency Range (0.1Hz to 40kHz)
- Low Noise Wide Dynamic Range
- *Guaranteed* Operation for $\pm 2.37V$ and $\pm 5V$ Supply
- Low Power Consumption
- *Guaranteed* Clock to Center Frequency Accuracy of 0.3% (LTC1059A)
- *Guaranteed* Low Offset Voltages over Temperature
- Very Low Center Frequency and Q Tempco
- Clock Input T²L or CMOS Compatible
- Separate Highpass (or Notch or Allpass), Bandpass, Lowpass Outputs

APPLICATIONS

- Sinewave Oscillators
- Sweepable Bandpass/Notch Filters
- Full Audio Frequency Filters
- Tracking Filters

DESCRIPTION

The LTC1059 consists of a general purpose, high performance, active filter building block and an uncommitted op amp. The filter building block together with an external clock and 2 to 5 resistors can produce various second order functions which are available at its three output pins. Two out of three always provide lowpass and bandpass functions while the third output pin can produce notch or highpass or allpass. The center frequency of these functions can be tuned from 0.1Hz to 40kHz and it is dependent on an external clock or an external clock and a resistor ratio. The filter can handle input frequencies up to 100kHz. The uncommitted op amp can be used to obtain additional allpass and notch functions, for gain adjustment or for cascading techniques.

Higher than second order filter functions can be obtained by cascading the LTC1059 with the LTC1060 dual universal filter or LTC1061 triple universal filter. Any classical filter realization (such as Butterworth, Cauer, Bessel and Chebyshev) can be formed.

The LTC1059 can be operated with single or dual supplies ranging from $\pm 2.37V$ to $\pm 8V$ (or 4.74V to 16V single supply) and is pinout compatible with MF5.

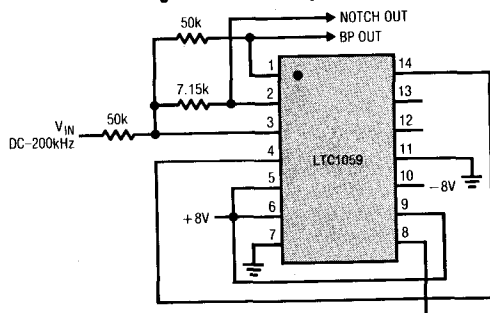
The LTC1059 is manufactured by using Linear Technology's enhanced LTCMOSTM silicon gate process.

LTCMOSTM is a trademark of Linear Technology Corp.

7

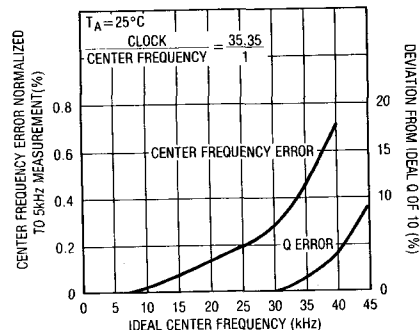
TYPICAL APPLICATION

Wide Range 2nd Order Bandpass/Notch Filter with Q = 10



T²L CLOCK IN $\leq 2MHz$

Center Frequency and Q Error

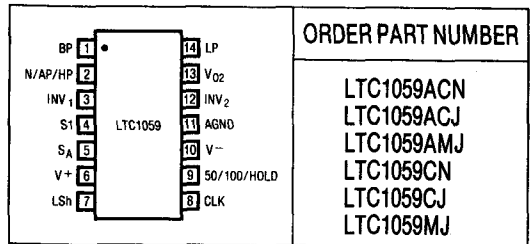


LTC1059

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	18V
Power Dissipation	500mW
Operating Temperature Range	
LTC1059AC, LTC1059C	$-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$
LTC1059AM, LTC1059M	$-55^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$
Storage Temperature Range	-65°C to 150°C
Lead Temperature (Soldering, 10sec)	300°C

PACKAGE/ORDER INFORMATION



ELECTRICAL CHARACTERISTICS

(Complete Filter) $V_S = \pm 5\text{V}$, $T_A = 25^{\circ}\text{C}$, $T^2\text{L}$ clock input level unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Center Frequency Range, f_0	$f_0 \times Q \leq 400\text{kHz}$, Mode 1 $f_0 \times Q \leq 1.6\text{MHz}$, Mode 1 $f_0 \times Q \leq 250\text{kHz}$, Mode 3, $V_S = \pm 7.5\text{V}$ $f_0 \times Q \leq 1\text{MHz}$, Mode 3, $V_S = \pm 7.5\text{V}$		0.1-40k 0.1-18k 0.1-20k 0.1-16k		Hz Hz Hz Hz
Input Frequency Range			0-200k		Hz
Clock to Center Frequency Ratio					
LTC1059A	Mode 1, 50:1, $f_{\text{CLK}} = 250\text{kHz}$, $Q = 10$	●		50 ± 0.3%	
LTC1059	Mode 1, 50:1, $f_{\text{CLK}} = 250\text{kHz}$, $Q = 10$	●		50 ± 0.8%	
LTC1059A	Mode 1, 100:1, $f_{\text{CLK}} = 500\text{kHz}$, $Q = 10$	●		100 ± 0.3%	
LTC1059	Mode 1, 100:1, $f_{\text{CLK}} = 500\text{kHz}$, $Q = 10$	●		100 ± 0.8%	
Q Accuracy					
LTC1059A	Mode 1, 50:1 or 100:1, $f_0 = 5\text{kHz}$	●	± 0.5	3	%
LTC1059	$Q = 10$	●	± 0.5	5	%
f_0 Temperature Coefficient	Mode 1, $f_{\text{CLK}} < 500\text{kHz}$		5		ppm/°C
Q Temperature Coefficient	Mode 1, $f_{\text{CLK}} < 500\text{kHz}$, $Q = 10$		15		ppm/°C
DC Offset V_{OS1}		●	2	15	mV
V_{OS2}	$f_{\text{CLK}} = 250\text{kHz}$, 50:1, $S_{\text{A/B}}$ High	●	3	30	mV
V_{OS2}	$f_{\text{CLK}} = 500\text{kHz}$, 100:1, $S_{\text{A/B}}$ High	●	6	60	mV
V_{OS2}	$f_{\text{CLK}} = 250\text{kHz}$, 50:1, $S_{\text{A/B}}$ Low	●	2	20	mV
V_{OS2}	$f_{\text{CLK}} = 500\text{kHz}$, 100:1, $S_{\text{A/B}}$ Low	●	4	40	mV
V_{OS3}	$f_{\text{CLK}} = 250\text{kHz}$, 50:1	●	2	20	mV
V_{OS3}	$f_{\text{CLK}} = 500\text{kHz}$, 100:1	●	4	40	mV
DC Low Pass Gain Accuracy	Mode 1, $R1 = R2 = 50\text{k}\Omega$	●	± 0.1	2	%
BP Gain Accuracy at f_0	Mode 1, $Q = 10$, $f_0 = 5\text{kHz}$		± 0.1		%
Clock Feedthrough	$f_{\text{CLK}} \leq 1\text{MHz}$		10		mV
Max. Clock Frequency	Mode 1, $Q < 5$, $V_S \geq \pm 5\text{V}$		2		MHz
Power Supply Current		●	3.5	5.5 7	mA mA

ELECTRICAL CHARACTERISTICS (Complete Filter) $V_S = \pm 2.37V$, $T_A = 25^\circ C$ unless otherwise specified

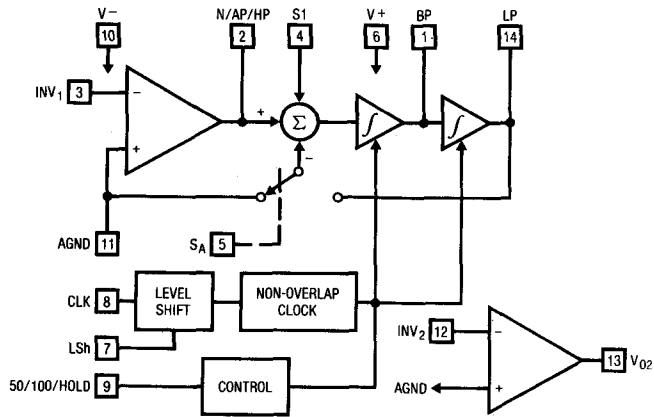
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Center Frequency Range	$f_o \times Q \leq 120kHz$, Mode 1, 50:1 $f_o \times Q \leq 120kHz$, Mode 3, 50:1		0.1-12k		Hz
			0.1-10k		Hz
Input Frequency Range			60k		Hz
Clock to Center Frequency Ratio LTC1059A LTC1059 LTC1059A LTC1059	Mode 1, 50:1, $f_{CLK} = 250kHz$, $Q = 10$ Mode 1, 50:1, $f_{CLK} = 250kHz$, $Q = 10$ Mode 1, 100:1, $f_{CLK} = 250kHz$, $Q = 10$ Mode 1, 100:1, $f_{CLK} = 250kHz$, $Q = 10$			50 ± 0.5%	
				50 ± 0.8%	
				100 ± 0.5%	
				100 ± 0.8%	
Q Accuracy LTC1059A LTC1059	Mode 1, $f_{CLK} = 250kHz$, $Q = 10$ 50:1 and 100:1		±1		%
			±2		%
Max. Clock Frequency Power Supply Current			700k		Hz
			1.5	2.5	mA

ELECTRICAL CHARACTERISTICS (Internal Op Amps) $T_A = 25^\circ C$ unless otherwise specified

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage Range		±2.375		±8	V
Voltage Swings LTC1059A LTC1059 LTC1059, LTC1059A	$V_S = \pm 5V$, $R_L = 5k$ (Pins 1, 14) $R_L = 3.5k$ (Pins 2, 13)		±4	±4.2	V
			±3.8	±4.2	V
			±3.6		V
					V
Input Offset Voltage			1	15	mV
Input Bias Current			3		pA
Output Short Circuit Current	$V_S = \pm 5V$		40/3		mA
Source/Sink DC Open Loop Gain	$V_S = \pm 5V$		80		dB
GBW	$V_S = \pm 5V$		2		MHz
Slew Rate	$V_S = \pm 5V$		7		V/μs

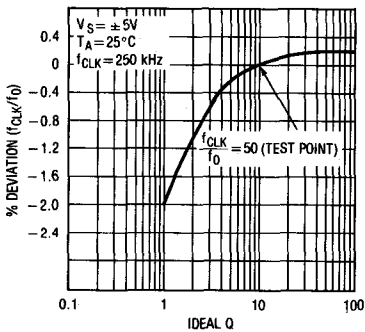
The ● denotes the specifications which apply over the full operating temperature range.

BLOCK DIAGRAM

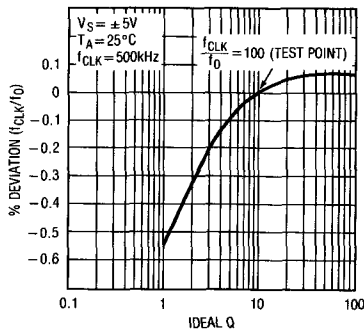


TYPICAL PERFORMANCE CHARACTERISTICS

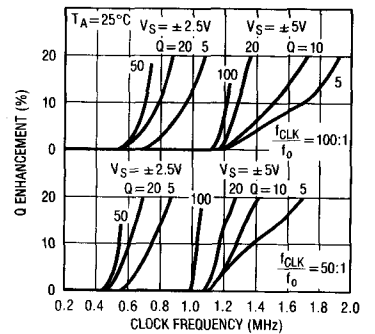
Graph 1. Mode 1:
(f_{CLK}/f_o) Deviation vs Q



Graph 2. Mode 1:
(f_{CLK}/f_o) Deviation vs Q

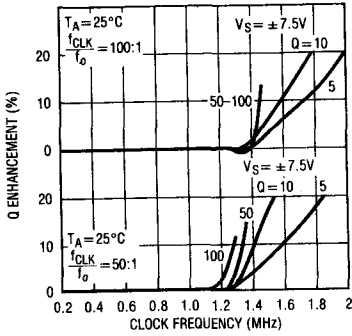


Graph 3. Mode 1: Q Error vs Clock Frequency

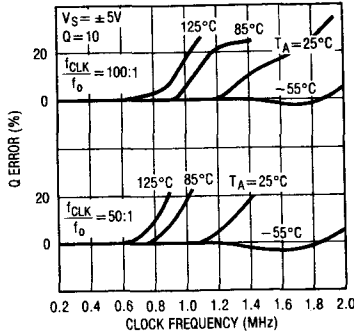


TYPICAL PERFORMANCE CHARACTERISTICS

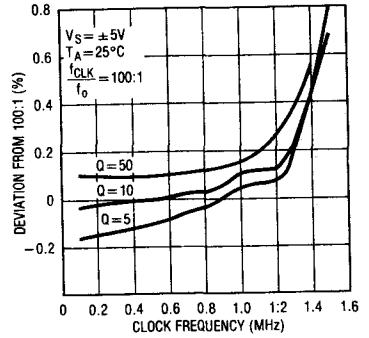
Graph 4. Mode 1: Q Error vs Clock Frequency



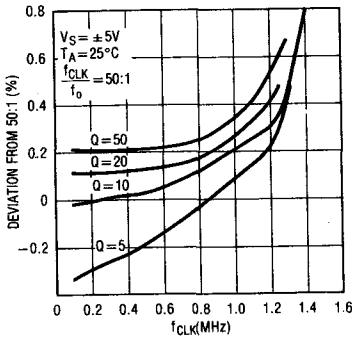
Graph 5. Mode 1: Measured Q vs f_{CLK} and Temperature



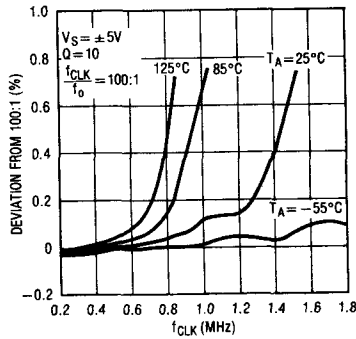
Graph 6. Mode 1: (f_{CLK}/f_o) vs f_{CLK} and Q



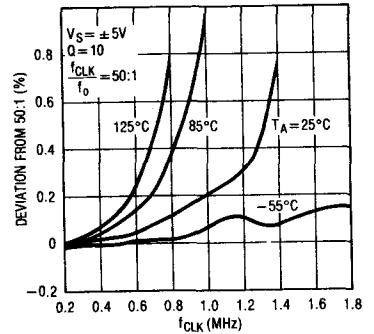
Graph 7. Mode 1: (f_{CLK}/f_o) vs f_{CLK} and Q



Graph 8. Mode 1: (f_{CLK}/f_o) vs f_{CLK} and Temperature

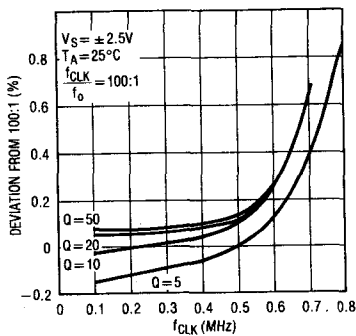


Graph 9. Mode 1: (f_{CLK}/f_o) vs f_{CLK} and Temperature

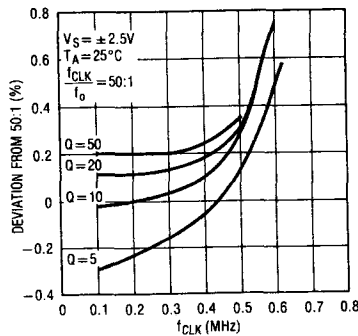


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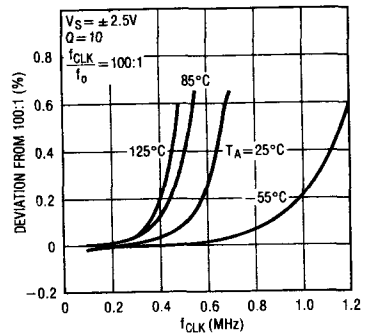
Graph 10. Mode 1: (f_{CLK}/f_o) vs f_{CLK} and Q



Graph 11. Mode 1: (f_{CLK}/f_o) vs f_{CLK} and Q

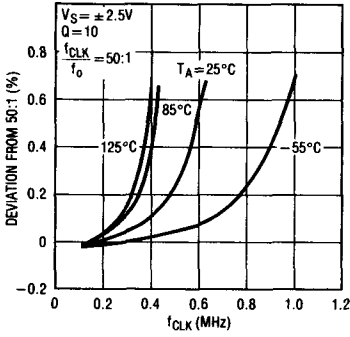


Graph 12. Mode 1: (f_{CLK}/f_o) vs f_{CLK} and Temperature

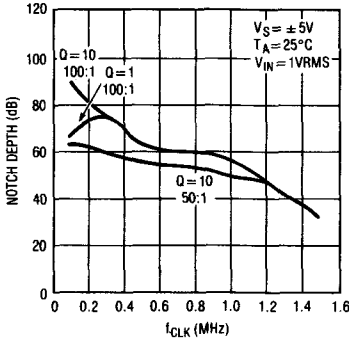


TYPICAL PERFORMANCE CHARACTERISTICS

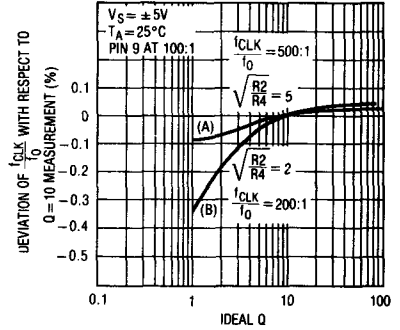
Graph 13. Mode 1: (f_{CLK}/f_o) vs f_{CLK} and Temperature



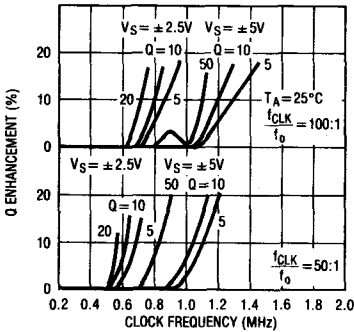
Graph 14. Mode 1: Notch Depth vs Clock Frequency



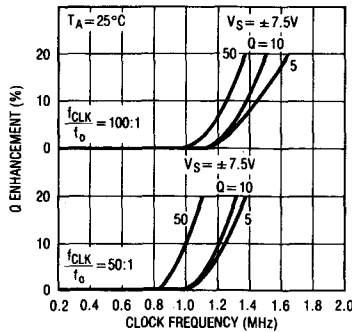
Graph 15. Mode 3: Deviation of (f_{CLK}/f_o) with Respect to Q = 10 Measurement



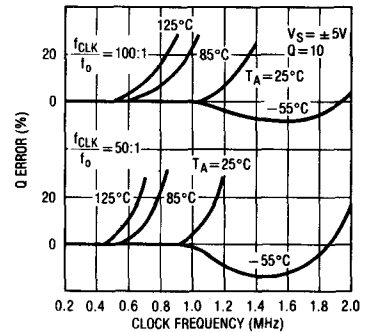
Graph 16. Mode 3: Q Error vs Clock Frequency



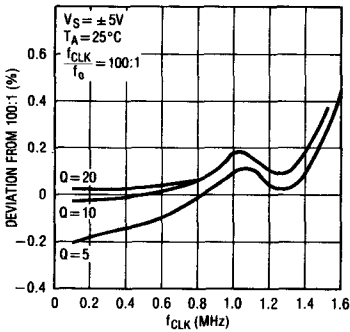
Graph 17. Mode 3 (R2 = R4): Q Error vs Clock Frequency



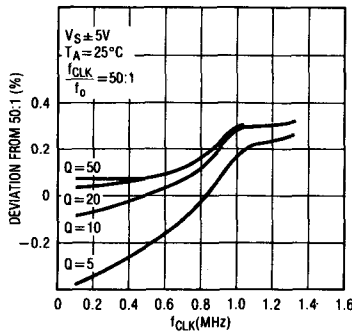
Graph 18. Mode 3 (R2 = R4): Measured Q vs f_{CLK} and Temperature



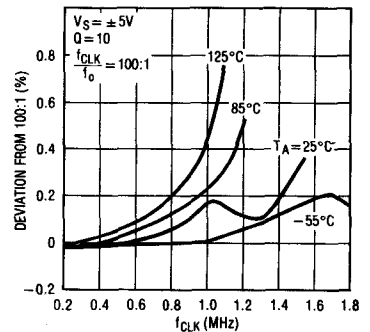
Graph 19. Mode 3 (R2 = R4): (f_{CLK}/f_o) vs f_{CLK} and Q



Graph 20. Mode 3 (R2 = R4): (f_{CLK}/f_o) vs f_{CLK} and Q

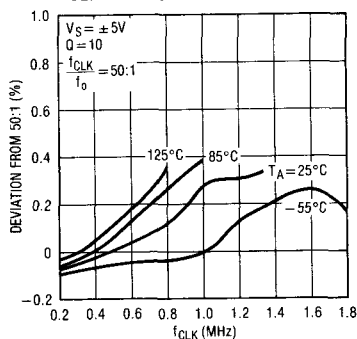


Graph 21. Mode 3 (R2 = R4): (f_{CLK}/f_o) vs f_{CLK} and Temperature

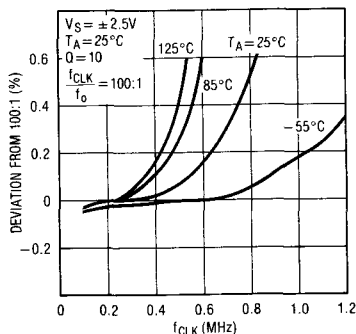


TYPICAL PERFORMANCE CHARACTERISTICS

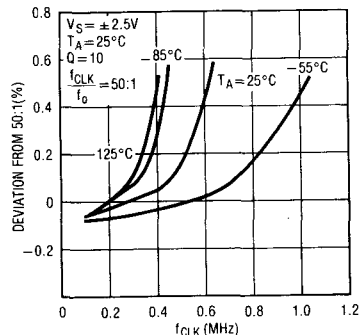
Graph 22. Mode 3 (R2 = R4):
(f_{CLK}/f_o) vs f_{CLK} and Temperature



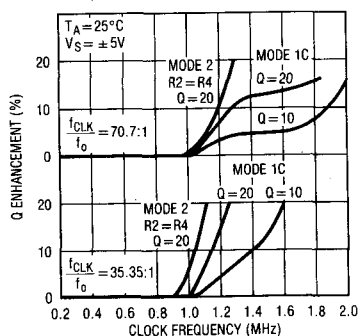
Graph 23. Mode 3 (R2 = R4):
(f_{CLK}/f_o) vs f_{CLK} and Temperature



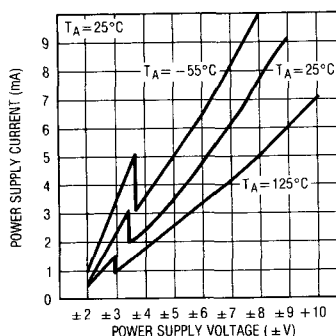
Graph 24. Mode 3 (R2 = R4):
(f_{CLK}/f_o) vs f_{CLK} and Temperature



Graph 25. Mode 1c (R5 = 0),
Mode 2 (R2 = R4) Q Error vs Clock
Frequency



Graph 26. Supply Current vs
Supply Voltage



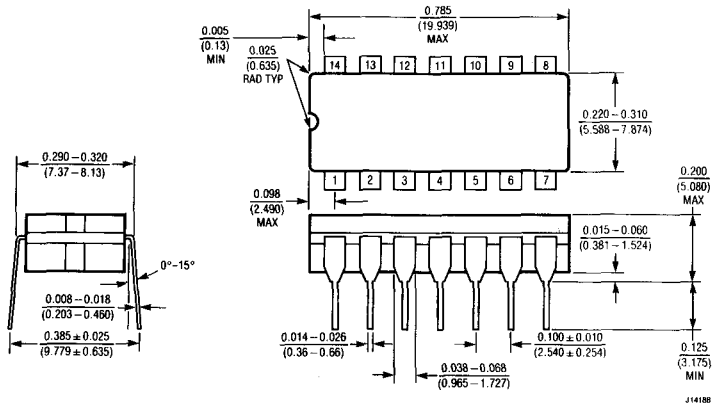
APPLICATIONS INFORMATION

The LTC1059 is compatible with the LTC1060. All the LTC1059 pins are functionally equivalent to the LTC1060 pins bearing the same title. For a detailed pin description and definition of various modes of operation refer to the LTC1060 data sheet. The LTC1059 is typically “faster” than the LTC1060 especially under single 5V (or ±2.5V)

supply operation. This becomes apparent through the typical performance characteristics of the part. All the graphs shown in this data sheet have been drawn under the same test conditions as in the LTC1060 data sheet; they are also numbered in the same order. For a complete discussion of the filter characteristics see the LTC1060 data sheet.

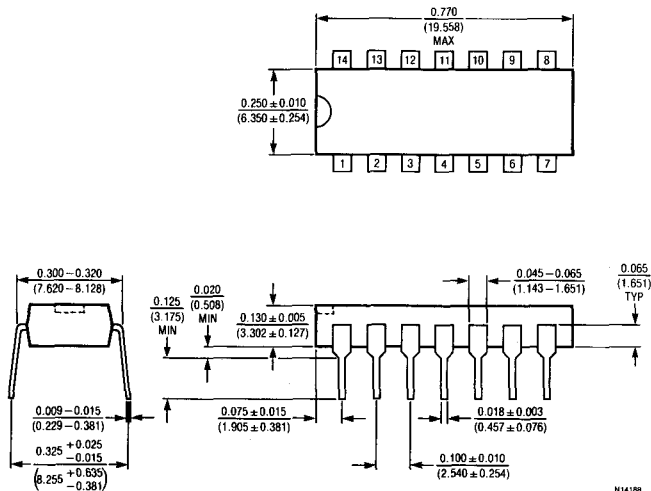
PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

J Package
14-Lead Ceramic DIP



T_{jmax} 150°C	Θ_{ja} 80°C/W
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N Package
14-Lead Plastic DIP



T_{jmax} 110°C	Θ_{ja} 130°C/W
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FEATURES

- All Filter Parameters *Guaranteed* over Temperature
- Wide Center Frequency Range (0.1Hz to 40kHz)
- Low Noise Wide Dynamic Range
- Operates from $\pm 2.5V$ Supply up to $\pm 8V$
- Low Power Consumption
- *Guaranteed* Clock to Center Frequency Accuracy of 0.8% or Better
- *Guaranteed* Low Offset Voltages over Temperature
- Very Low Center Frequency and Q Tempo
- Clock Input T²L or CMOS Compatible
- Separate Highpass (or Notch or Allpass), Bandpass, Lowpass Outputs

APPLICATIONS

- Sinewave Oscillators
- Sweepable Bandpass/Notch Filters
- Full Audio Frequency Filters
- Tracking Filters

DESCRIPTION

The LTC1059 consists of a general purpose, high performance, active filter building block and an uncommitted op amp. The filter building block together with an external clock and 2 to 5 resistors can produce various second order functions which are available at its three output pins. Two out of three always provide lowpass and bandpass functions while the third output pin can produce notch or highpass or allpass. The center frequency of these functions can be tuned from 0.1Hz to 40kHz and it is dependent on an external clock or an external clock and a resistor ratio. The filter can handle input frequencies up to 100kHz. The uncommitted op amp can be used to obtain additional allpass and notch functions, for gain adjustment or for cascading techniques.

Higher than second order filter functions can be obtained by cascading the LTC1059 with the LTC1060 dual universal filter or LTC1061 triple universal filter. Any classical filter realization (such as Butterworth, Cauer, Bessel and Chebyshev) can be formed.

The LTC1059 can be operated with single or dual supplies ranging from $\pm 2.37V$ to $\pm 8V$ (or 4.74V to 16V single supply).

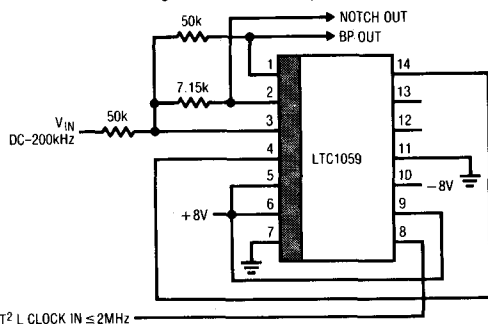
The LTC1059 is manufactured by using Linear Technology's enhanced LTCMOS™ silicon gate process.

LTCMOS™ is a trademark of Linear Technology Corp.

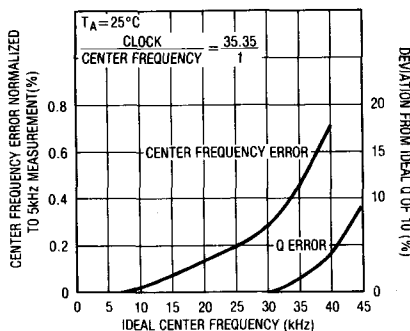
7

TYPICAL APPLICATION

Wide Range 2nd Order Bandpass/Notch Filter with Q = 10



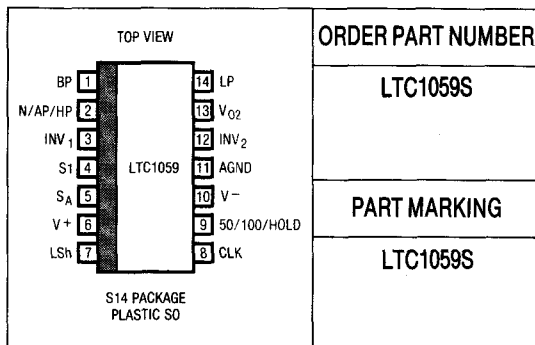
Center Frequency and Q Error



ABSOLUTE MAXIMUM RATINGS

Supply Voltage 18V
 Operating Temperature Range $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$
 Storage Temperature Range -65°C to 150°C
 Lead Temperature (Soldering, 10sec) 300°C

PACKAGE/ORDER INFORMATION



ELECTRICAL CHARACTERISTICS

(Complete Filter) $V_S = \pm 5\text{V}$, $T_A = 25^{\circ}\text{C}$, $T^2\text{L}$ clock input level unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Center Frequency Range, f_0	$f_0 \times Q \leq 400\text{kHz}$, Mode 1 $f_0 \times Q \leq 1.6\text{MHz}$, Mode 1 $f_0 \times Q \leq 250\text{kHz}$, Mode 3, $V_S = \pm 7.5\text{V}$ $f_0 \times Q \leq 1\text{MHz}$, Mode 3, $V_S = \pm 7.5\text{V}$		0.1–40k 0.1–18k 0.1–20k 0.1–16k		Hz Hz Hz Hz
Input Frequency Range			0–200k		Hz
Clock to Center Frequency Ratio (Note 1)	Mode 1, 50:1, $f_{\text{CLK}} = 250\text{kHz}$, $Q = 10$ Mode 1, 100:1, $f_{\text{CLK}} = 500\text{kHz}$, $Q = 10$	●		$50 \pm 0.8\%$ $100 \pm 0.8\%$	
Q Accuracy (Note 1)	Mode 1, 50:1 or 100:1, $f_0 = 5\text{kHz}$ $Q = 10$	●	± 0.5	5	%
f_0 Temperature Coefficient	Mode 1, $f_{\text{CLK}} < 500\text{kHz}$		5		ppm/ $^{\circ}\text{C}$
Q Temperature Coefficient	Mode 1, $f_{\text{CLK}} < 500\text{kHz}$, $Q = 10$		15		ppm/ $^{\circ}\text{C}$
DC Offset V_{OS1} (Note 2)		●	2	15	mV
V_{OS2}	$f_{\text{CLK}} = 250\text{kHz}$, 50:1, $S_{\text{A/B}}$ High	●	3	40	mV
V_{OS2}	$f_{\text{CLK}} = 500\text{kHz}$, 100:1, $S_{\text{A/B}}$ High	●	6	80	mV
V_{OS2}	$f_{\text{CLK}} = 250\text{kHz}$, 50:1, $S_{\text{A/B}}$ Low	●	2	30	mV
V_{OS2}	$f_{\text{CLK}} = 500\text{kHz}$, 100:1, $S_{\text{A/B}}$ Low	●	4	60	mV
V_{OS3}	$f_{\text{CLK}} = 250\text{kHz}$, 50:1	●	2	30	mV
V_{OS3}	$f_{\text{CLK}} = 500\text{kHz}$, 100:1	●	4	60	mV
DC Low Pass Gain Accuracy	Mode 1, $R1 = R2 = 50\text{k}\Omega$	●	± 0.1	2	%
BP Gain Accuracy at f_0	Mode 1, $Q = 10$, $f_0 = 5\text{kHz}$		± 0.1		%
Clock Feedthrough	$f_{\text{CLK}} \leq 1\text{MHz}$		10		mV
Max. Clock Frequency	Mode 1, $Q < 5$, $V_S \geq \pm 5\text{V}$		2		MHz
Power Supply Current		●	3.5	5.5 7	mA mA

Note 1: An LTC1059S with improved Q and clock to center frequency ratio accuracy can be made available upon special request.

Note 2: For definition of the DC offset voltages, refer to the LTC1059 data sheet. An LTC1059S with improved DC offset specifications can be made available upon special request.

ELECTRICAL CHARACTERISTICS (Complete Filter) $V_S = \pm 2.37V$, $T_A = 25^\circ C$ unless otherwise specified

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Center Frequency Range	$f_0 \times Q \leq 120kHz$, Mode 1, 50:1		0.1-12k		Hz
	$f_0 \times Q \leq 120kHz$, Mode 3, 50:1		0.1-10k		Hz
Input Frequency Range			60k		Hz
Clock to Center Frequency Ratio	Mode 1, 50:1, $f_{CLK} = 250kHz$, $Q = 10$		$50 \pm 0.8\%$		
	Mode 1, 100:1, $f_{CLK} = 250kHz$, $Q = 10$		$100 \pm 0.8\%$		
Q Accuracy	Mode 1, $f_{CLK} = 250kHz$, $Q = 10$ 50:1 and 100:1		± 2		%
Max. Clock Frequency			700k		Hz
Power Supply Current			1.5	2.5	mA

ELECTRICAL CHARACTERISTICS (Internal Op Amps) $T_A = 25^\circ C$ unless otherwise specified

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage Range		± 2.375		± 8	V
Voltage Swings	$V_S = \pm 5V$, $R_L = 5k$ (Pins 1, 14) $R_L = 3.5k$ (Pins 2, 13)	± 3.8	± 4.2		V
		± 3.6			V
Input Offset Voltage			1	15	mV
Input Bias Current			3		pA
Output Short Circuit Current Source/Sink	$V_S = \pm 5V$		25/3		mA
DC Open Loop Gain	$V_S = \pm 5V$		80		dB
GBW	$V_S = \pm 5V$		2		MHz
Slew Rate	$V_S = \pm 5V$		7		V/ μs

The ● denotes the specifications which apply over the full operating temperature range.

NOTES

FEATURES

- *Guaranteed* Filter Specification for $\pm 2.37V$ and $\pm 5V$ Supply
- Operates up to 30kHz
- Low Power and 88dB Dynamic Range at $\pm 2.5V$ Supply
- Center Frequency Q Product up to 1.6MHz
- *Guaranteed* Offset Voltages
- *Guaranteed* Clock to Center Frequency Accuracy over Temperature
 - 0.3% for LTC1060A
 - 0.8% for LTC1060
- *Guaranteed* Q Accuracy over Temperature
- Low Temperature Coefficient of Q and Center Frequency
- Low Crosstalk, 70dB
- Clock Inputs TTL and CMOS Compatible

DESCRIPTION

The LTC1060 consists of two high performance, switched capacitor filters. Each filter, together with 2 to 5 resistors, can produce various 2nd order filter functions such as low-pass, bandpass, highpass notch and allpass. The center frequency of these functions can be tuned by an external clock, or by an external clock and resistor ratio. Up to 4th order full biquadratic functions can be achieved by cascading the two filter blocks. Any of the classical filter configurations (like Butterworth, Chebyshev, Bessel, Cauer) can be formed.

The LTC1060 operates with either a single or dual supply from $\pm 2.37V$ to $\pm 8V$. When used with low supply (i.e. single 5V supply), the filter typically consumes 12mW and can operate with center frequencies up to 10kHz. With $\pm 5V$ supply, the frequency range extends to 30kHz and very high Q values can also be obtained.

The LTC1060 is manufactured by using Linear Technology's enhanced LTCMOS™ silicon gate process. Because of this, low offsets, high dynamic range, high center frequency Q product and excellent temperature stability are obtained.

The LTC1060 is pinout compatible with MF10.

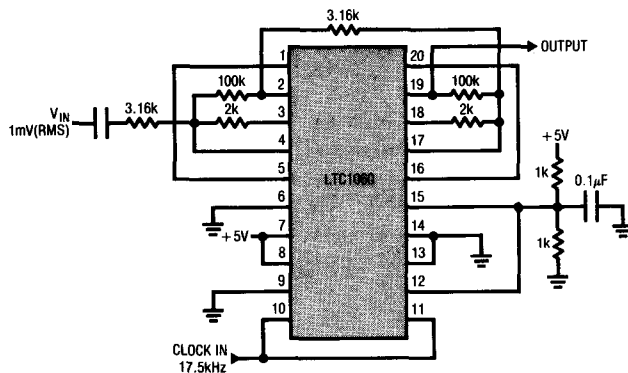
LTCMOS™ is a trademark of Linear Technology Corp.

APPLICATIONS

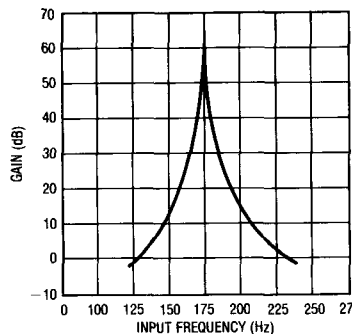
- Single 5V Supply Medium Frequency Filters
- Very High Q and High Dynamic Range Bandpass, Notch Filters
- Tracking Filters
- Telecom Filters

7

Single 5V, Gain of 1000 4th Order Bandpass Filter



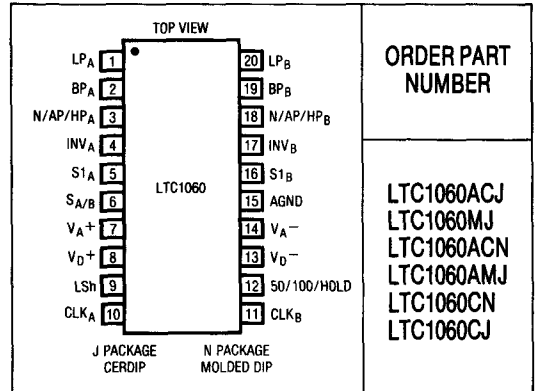
Amplitude Response



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	18V
Power Dissipation	500mW
Operating Temperature Range	
LTC1060AC, LTC1060C	$-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$
LTC1060AM, LTC1060M	$-55^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$
Storage Temperature Range	-65°C to 150°C
Lead Temperature (Soldering, 10sec.)	300°C

PACKAGE/ORDER INFORMATION



ORDER PART NUMBER

- LTC1060ACJ
- LTC1060MJ
- LTC1060ACN
- LTC1060AMJ
- LTC1060CN
- LTC1060CJ

ELECTRICAL CHARACTERISTICS (Complete Filter) $V_S = \pm 5V$, $T_A = 25^{\circ}\text{C}$ unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Center Frequency Range (see Applications Information)	$f_0 \times Q \leq 400\text{kHz}$, Mode 1, Figure 4 $f_0 \times Q \leq 1.6\text{MHz}$, Mode 1, Figure 4		0.1-20K 0.1-16K		Hz Hz
Clock to Center Frequency Ratio LTC1060A LTC1060 LTC1060A LTC1060	Mode 1, 50:1, $f_{\text{CLK}} = 250\text{kHz}$, $Q = 10$ Mode 1, 50:1, $f_{\text{CLK}} = 250\text{kHz}$, $Q = 10$ Mode 1, 100:1, $f_{\text{CLK}} = 500\text{kHz}$, $Q = 10$ Mode 1, 100:1, $f_{\text{CLK}} = 500\text{kHz}$, $Q = 10$	• • • •		$50 \pm 0.3\%$ $50 \pm 0.8\%$ $100 \pm 0.3\%$ $100 \pm 0.8\%$	
Q accuracy LTC1060A LTC1060	Mode 1, 50:1 or 100:1, $f_0 = 5\text{kHz}$ $Q = 10$	• •	± 0.5 ± 0.5	3 5	% %
f_0 Temperature Coefficient Q Temperature Coefficient	Mode 1, $f_{\text{CLK}} < 500\text{kHz}$ Mode 1, $f_{\text{CLK}} < 500\text{kHz}$, $Q = 10$		-10 +20		ppm/ $^{\circ}\text{C}$ ppm/ $^{\circ}\text{C}$
DC Offset V_{OS1} V_{OS2} V_{OS2} V_{OS2} V_{OS3} V_{OS3}	$f_{\text{CLK}} = 250\text{kHz}$, 50:1, $S_{\text{A/B}}$ High $f_{\text{CLK}} = 500\text{kHz}$, 100:1, $S_{\text{A/B}}$ High $f_{\text{CLK}} = 250\text{kHz}$, 50:1, $S_{\text{A/B}}$ Low $f_{\text{CLK}} = 500\text{kHz}$, 100:1, $S_{\text{A/B}}$ Low $f_{\text{CLK}} = 250\text{kHz}$, 50:1, $S_{\text{A/B}}$ Low $f_{\text{CLK}} = 500\text{kHz}$, 100:1, $S_{\text{A/B}}$ Low	• • • • • •	2 3 6 2 4 2 4	15 30 60 20 40 20 40	mV mV mV mV mV mV mV
DC Low Pass Gain Accuracy BP Gain Accuracy at f_0 Clock Feedthrough Max. Clock Frequency Power Supply Current	Mode 1, $R_1 = R_2 = 50\text{k}$ Mode 1, $Q = 10$, $f_0 = 5\text{kHz}$ $f_{\text{CLK}} \leq 1\text{MHz}$		± 0.1 ± 0.1 10 1.5 3	2 8 12	% % mV(p-p) MHz mA mA
Crosstalk		•	70		dB

ELECTRICAL CHARACTERISTICS (Complete Filter) $V_S = \pm 2.37V$, $T_A = 25^\circ C$

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Center Frequency Range	$f_o \times Q \leq 100kHz$		0.1-10k		Hz
Clock to Center Frequency Ratio LTC1060A LTC1060 LTC1060A LTC1060	Mode 1, 50:1, $f_{CLK} = 250kHz$, $Q = 10$ Mode 1, 50:1, $f_{CLK} = 250kHz$, $Q = 10$ Mode 1, 100:1, $f_{CLK} = 250kHz$, $Q = 10$ Mode 1, 100:1, $f_{CLK} = 250kHz$, $Q = 10$	• •	50 ± 0.8% 100 ± 0.5% 100 ± 0.8%	50 ± 0.5%	
Q Accuracy LTC1060A LTC1060	Mode 1, $f_o = 2.5kHz$, $Q = 10$		± 2 ± 4		% %
Max Clock Frequency			500		kHz
Power Supply Current			2.5	4	mA

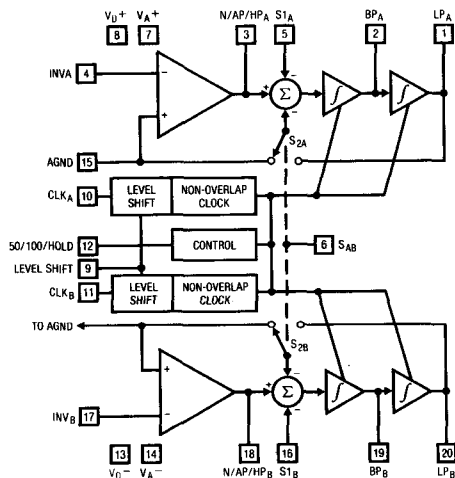
ELECTRICAL CHARACTERISTICS (Internal Op Amps) $T_A = 25^\circ C$

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage Range		± 2.37		± 8	V
Voltage Swings LTC1060A LTC1060 LTC1060, LTC1060A	$V_S = \pm 5V$, $R_L = 5k$ (Pins 1, 2, 19, 20) $R_L = 3.5k$ (Pins 3, 18)	± 4 ± 3.8 ± 3.6	± 4 ± 4 ± 4		V V V
Output Short Circuit Current Source Sink	$V_S = \pm 5V$		25 3		mA mA
Op Amp GBW Product	$V_S = \pm 5V$		2		MHz
Op Amp Slew Rate	$V_S = \pm 5V$		7		V/μs
Op Amp DC Open Loop Gain	$R_L = 10k$, $V_S = \pm 5V$		85		dB

The • denotes the specifications which apply over the full operating temperature range.

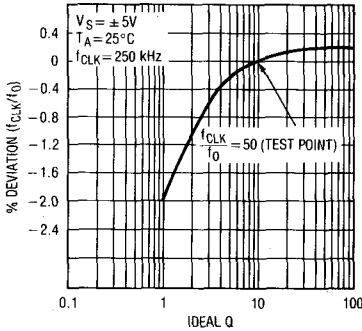
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BLOCK DIAGRAM

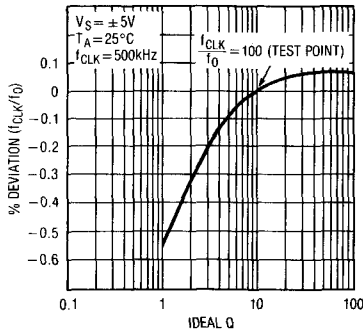


TYPICAL PERFORMANCE CHARACTERISTICS

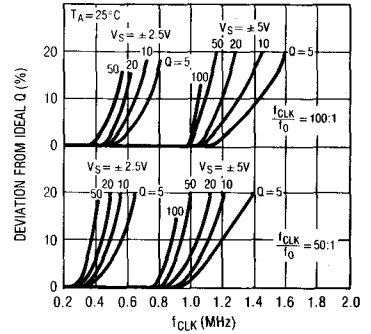
**Graph 1. Mode 1:
(f_{CLK}/f_0) Deviation vs Q**



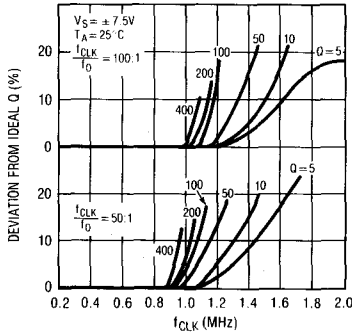
**Graph 2. Mode 1:
(f_{CLK}/f_0) Deviation vs Q**



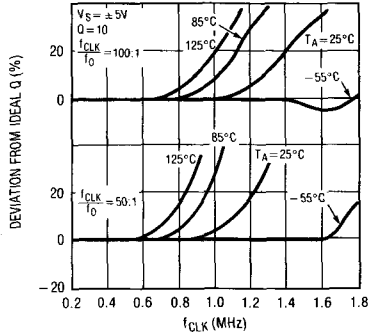
Graph 3. Mode 1: Q Error vs Clock Frequency



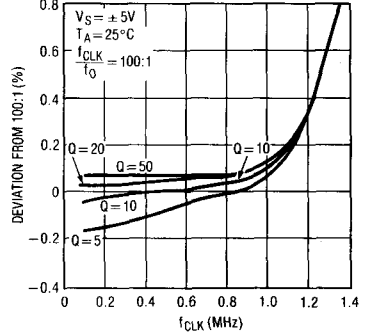
Graph 4. Mode 1: Q Error vs Clock Frequency



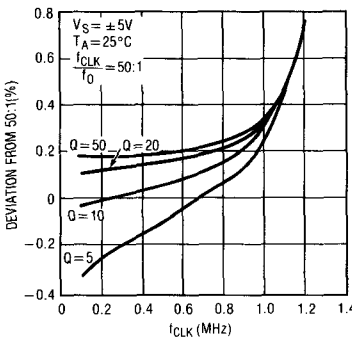
Graph 5. Mode 1: Measured Q vs f_{CLK} and Temperature



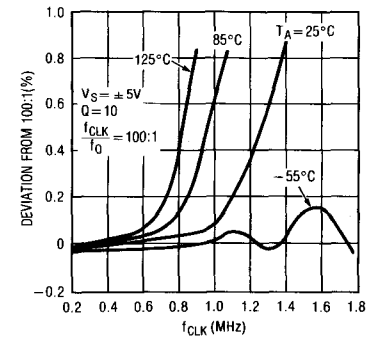
Graph 6. Mode 1: (f_{CLK}/f_0) vs f_{CLK} and Q



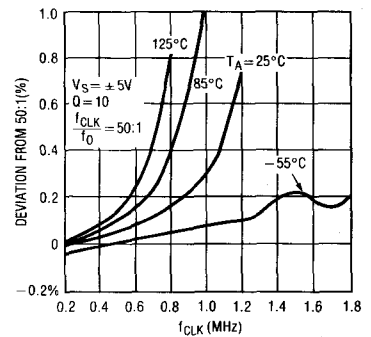
Graph 7. Mode 1: (f_{CLK}/f_0) vs f_{CLK} and Q



Graph 8. Mode 1: (f_{CLK}/f_0) vs f_{CLK} and Temperature

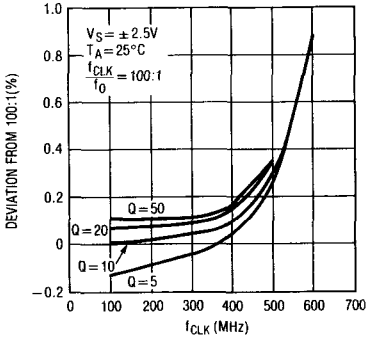


Graph 9. Mode 1: (f_{CLK}/f_0) vs f_{CLK} and Temperature

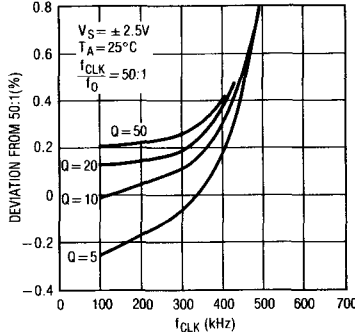


TYPICAL PERFORMANCE CHARACTERISTICS

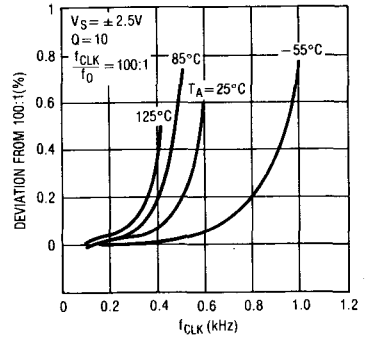
Graph 10. Mode 1: (f_{CLK}/f_0) vs f_{CLK} and Q



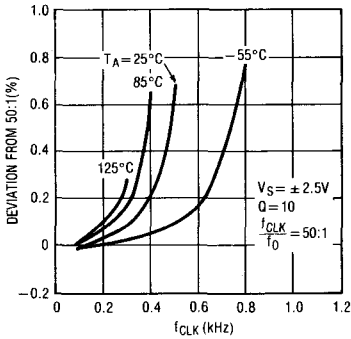
Graph 11. Mode 1: (f_{CLK}/f_0) vs f_{CLK} and Q



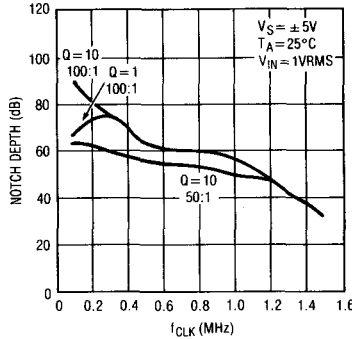
Graph 12. Mode 1: (f_{CLK}/f_0) vs f_{CLK} and Temperature



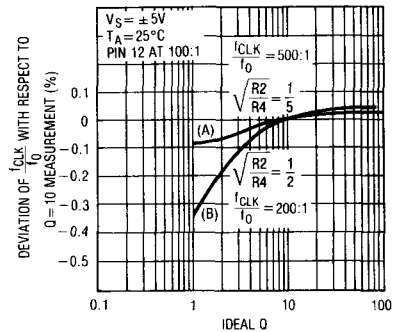
Graph 13. Mode 1: (f_{CLK}/f_0) vs f_{CLK} and Temperature



Graph 14. Mode 1: Notch Depth vs Clock Frequency

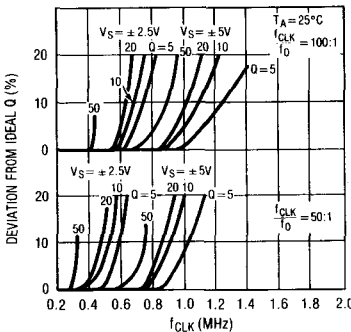


Graph 15. Mode 3: Deviation of (f_{CLK}/f_0) with Respect to Q = 10 Measurement

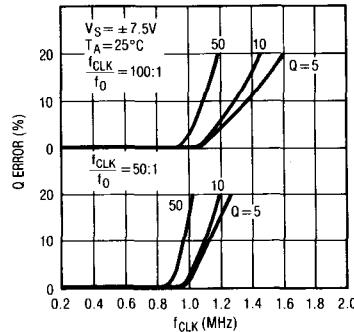


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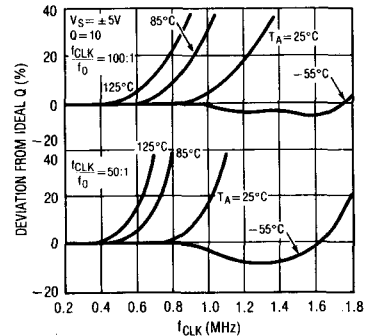
Graph 16. Mode 3: Q Error vs Clock Frequency



Graph 17. Mode 3 (R2 = R4): Q Error vs Clock Frequency

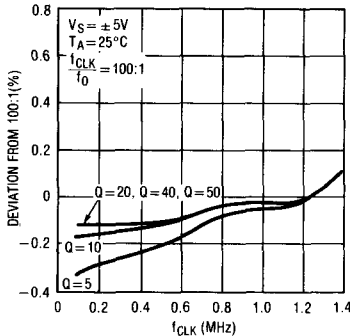


Graph 18. Mode 3 (R2 = R4): Measured Q vs f_{CLK} and Temperature

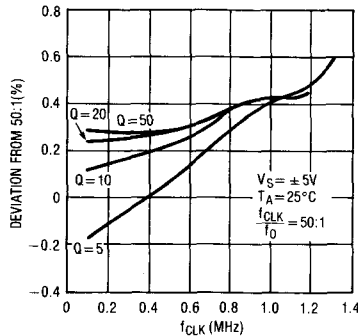


TYPICAL PERFORMANCE CHARACTERISTICS

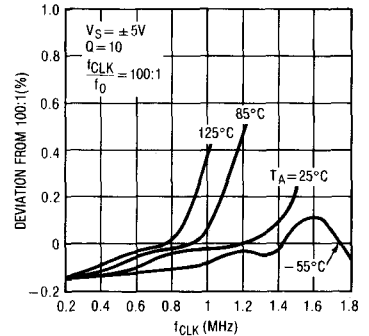
Graph 19. Mode 3 (R2 = R4):
 f_{CLK}/f_{ϕ} vs f_{CLK} and Q



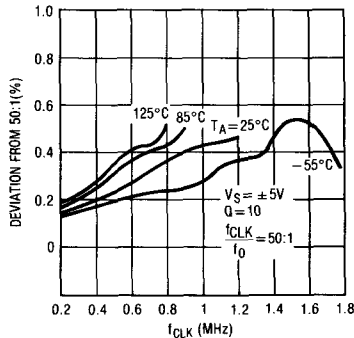
Graph 20. Mode 3 (R2 = R4):
 (f_{CLK}/f_{ϕ}) vs f_{CLK} and Q



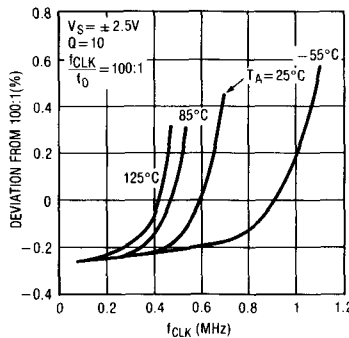
Graph 21. Mode 3 (R2 = R4):
 (f_{CLK}/f_{ϕ}) vs f_{CLK} and Temperature



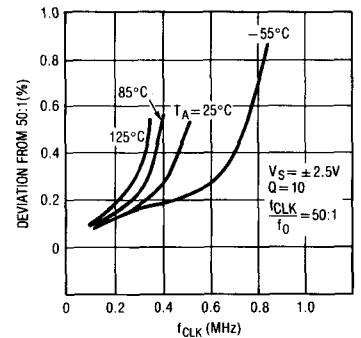
Graph 22. Mode 3 (R2 = R4):
 (f_{CLK}/f_{ϕ}) vs f_{CLK} and Temperature



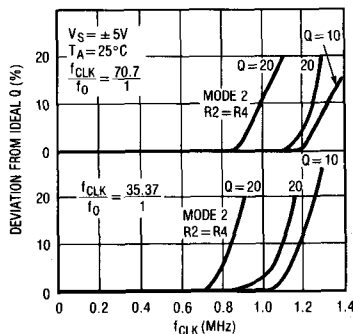
Graph 23. Mode 3 (R2 = R4):
 (f_{CLK}/f_{ϕ}) vs f_{CLK} and Temperature



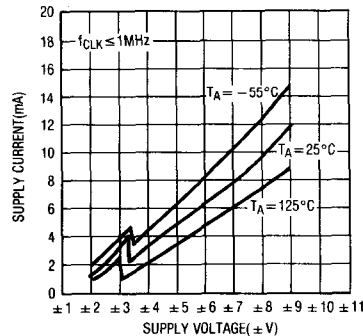
Graph 24. Mode 3 (R2 = R4):
 (f_{CLK}/f_{ϕ}) vs f_{CLK} and Temperature



Graph 25. Mode 1c (R5 = 0),
 Mode 2 (R2 = R4) Q Error vs Clock
 Frequency



Graph 26. Supply Current vs
 Supply Voltage



PIN DESCRIPTION AND APPLICATIONS INFORMATION

Power Supplies

The V_A^+ and V_B^+ (pins 7 and 8) and the V_A^- , V_B^- (pins 14 and 13) are, respectively, the analog and digital positive and negative supply pins. For most cases, pins 7 and 8 should be tied together and bypassed by a $0.1\mu\text{F}$ disc ceramic capacitor. The same holds for pins 14 and 13. If the LTC1060 operates in high digital noise environment, the supply pins can be bypassed separately. Pins 7 and 8 are internally connected through the IC substrate and should be biased from the same DC source. Pins 14 and 13 should also be biased from the same DC source.

The LTC1060 is designed to operate with $\pm 2.5\text{V}$ supply (or single 5V) and with $\pm 5\text{V}$ to $\pm 8\text{V}$ supplies. The minimum supply, where the filter operates reliably, is $\pm 2.37\text{V}$. With low supply operation, the maximum input clock frequency is about 500kHz. Beyond this, the device exhibits excessive Q enhancement and center frequency errors.

Clock Input Pins and Level Shift

The level shift (LSh) pin 9 is used to accommodate T^2L or CMOS clock levels. With dual supplies equal or higher to $\pm 4.5\text{V}$, pin 9 should be connected to ground (same potential as the AGND pin). Under these conditions the clock levels can be T^2L or CMOS. With single supply operation, the negative supply pins and the LSh pin should be tied to the system ground. The AGND, pin 15, should be biased at 1/2 supplies, as shown in the "Single 5V Gain of 1000 4th Order Bandpass Filter" circuit. Again, under these conditions, the clock levels can be T^2L or CMOS. The input clock pins (10, 11) share the same level shift pin. The clock logic threshold level over temperature is typically $1.5\text{V} \pm 0.1\text{V}$ above the LSh pin potential. The duty cycle of the input clock should be close to 50%. For clock frequencies below 1MHz, the (f_{CLK}/f_0) ratio is independent from the clock input levels and from its rise and fall times. Fast rising clock edges, however, improve the filter DC offsets. For clock frequencies above 1MHz, T^2L level clocks are recommended.

50/100/Hold (Pin 12)

By tying pin 12 to (V_A^+, V_B^+) , the filter operates in the 50:1 mode. With $\pm 5\text{V}$ supplies pin 12 can be typically 1V below the positive supply without affecting the 50:1 operation of

the device. By tying pin 12 to 1/2 supplies (which should be the AGND potential), the LTC1060 operates in the 100:1 mode. The 1/2 supply bias of pin 12 can vary around the 1/2 supply potential without affecting the 100:1 filter operation. This is shown in Table 1.

When pin 12 is shorted to the negative supply pin, the filter operation is stopped and the bandpass and lowpass outputs act as a S/H circuit holding the last sample. The hold step is 20mV and the droop rate is $150\mu\text{V}/\text{second}$!

Table 1

Total Power Supply	Voltage Range of Pin 12 for 100:1 Operation
+5V	$2.5\text{V} \pm 0.5\text{V}$
+10V	$+5\text{V} \pm 1\text{V}$
+15V	$+7.5\text{V} \pm 1.5\text{V}$

S1A, S1B (Pins 5 and 16)

These are voltage signal input pins and, if used, they should be driven with a source impedance below $5\text{k}\Omega$. The S1A, S1B pins can be used to alter the CLK to center frequency ratio (f_{CLK}/f_0) of the filter (see Modes 1b, 1c, 2a, 2b) or to feedforward the input signal for allpass filter configurations (see Modes 4 and 5). When these pins are not used, they should be tied to the AGND pin.

S_{A/B} (Pin 6)

When S_{A/B} is high, the S2 input of the filter's voltage summer (see Block Diagram) is tied to the lowpass output. This frees the S1 pin to realize various modes of operation for improved applications flexibility. When the S_{A/B} pin is connected to the negative supply, the S2 input switches to ground and internally becomes inactive. This improves the filter noise performance and typically lowers the value of the offset V_{OS2} .

AGND (Pin 15)

This should be connected to the system ground for dual supply operation. When the LTC1060 operates with a single positive supply, the analog ground pin should be tied to 1/2 supply and bypassed with a $0.1\mu\text{F}$ capacitor, as shown in the application, "Single 5V, Gain of 1000 4th Order Bandpass Filter". The positive inputs of all the internal op amps, as well as the reference point of all the internal

APPLICATIONS INFORMATION

switches are connected to the AGND pin. Because of this, a “clean” ground is recommended.

f_{CLK}/f_0 Ratio

The (f_{CLK}/f_0) reference of 100:1 or 50:1 is derived from the filter center frequency measured in mode 1, with a $Q = 10$ and $V_S = \pm 5V$. The clock frequencies are, respectively, 500kHz/250kHz for the 100:1/50:1 measurement. All the curves shown in the Typical Performance Characteristics section are normalized to the above references.

Graphs 1 and 2 in the Typical Performance Characteristics show the (f_{CLK}/f_0) variation versus values of ideal Q . The LTC1060 is a sampled data filter and it only approximates continuous time filters. In this data sheet, the LTC1060 is treated in the frequency domain because this approximation is good enough for most filter applications. The LTC1060 deviates from its ideal continuous filter model when the (f_{CLK}/f_0) ratio decreases and when the Q 's are low. Since low Q filters are not selective, the frequency domain approximation is well justified. In graph 15 the LTC1060 is connected in mode 3 and its (f_{CLK}/f_0) ratio is adjusted to 200:1 and 500:1. Under these conditions, the filter is over-sampled and the (f_{CLK}/f_0) curves are nearly independent of the Q values. In mode 3, the (f_{CLK}/f_0) ratio typically deviates from the tested one in mode 1 by $\pm 0.1\%$.

$f_0 \times Q$ Product Ratio

This is a figure of merit of general purpose active filter building blocks. The $f_0 \times Q$ product of the LTC1060 depends on the clock frequency, the power supply voltages, the junction temperature and the mode of operation.

At 25°C ambient temperature for $\pm 5V$ supplies, and for clock frequencies below 1MHz, in mode 1 and its derivatives, the $f_0 \times Q$ product is mainly limited by the desired f_0 and Q accuracy. For instance, from graph 4 at 50:1 and for f_{CLK} below 800kHz a predictable ideal Q of 400 can be obtained. Under this condition, a respectable $f_0 \times Q$ product of 6.4MHz is achieved. The 16kHz center frequency will be about 0.22% off from the tested value at 250kHz clock (see graph 1). For the same clock frequency of 800kHz and for the same Q value of 400, the $f_0 \times Q$ product can be further increased if the clock to center frequency ratio is low-

ered below 50:1. In mode 1c with $R5 = 0$ and $R6 = \infty$, the (f_{CLK}/f_0) ratio is $50/\sqrt{2}$. The $f_0 \times Q$ product can now be increased to 9MHz since, with the same clock frequency and same Q value, the filter can handle a center frequency of $16kHz \times \sqrt{2}$.

For clock frequencies above 1MHz, the $f_0 \times Q$ product is limited by the clock frequency itself. From graph 4 at $\pm 7.5V$ supply, 50:1, and 1.4MHz clock, a Q of 5 has about 8% error; the measured 28kHz center frequency was skewed by 0.8% with respect to the guaranteed value at 250kHz clock. Under these conditions, the $f_0 \times Q$ product is only 140kHz, but the filter can handle higher input signal frequencies than the 800kHz clock frequency—very high Q case described above.

Mode 3, Figure 11, and the modes of operation where $R4$ is finite, are “slower” than the basic mode 1. This is shown in graph 16 and 17. The resistor $R4$ places the input op amp inside the resonant loop. The finite GBW of this op amp creates an additional phase shift and enhances the Q value at high clock frequencies. Graph 16 was drawn with a small capacitor, C_C , placed across $R4$ and as such, at $V_S = \pm 5V$, the $(1/2\pi R4 C_C) = 2MHz$. With $V_S = \pm 2.5V$ the $(1/2\pi R4 C_C)$ should be equal to 1.4MHz. This allows the Q curve to be slightly “flatter” over a wider range of clock frequencies. If, at $\pm 5V$ supply, the clock is below 900kHz (or 400kHz for $V_S = \pm 2.5V$), this capacitor, C_C , is not needed.

For graph 25, the clock to center frequency ratios are altered to 70.7:1 and 35.35:1. This is done by using mode 1c with $R5 = 0$, Figure 7, or mode 2 with $R2 = R4 = 10k\Omega$. The mode 1c, where the input op amp is outside the main loop, is much faster. Mode 2, however, is more versatile. At 50:1, and for $T_A = 25^\circ C$ the mode 1c can be tuned for center frequencies up to 30kHz.

Output Noise

The wideband rms noise of the LTC1060 outputs is nearly independent from the clock frequency provided that the clock itself does not become part of the noise. The LTC1060 noise slightly decreases with $\pm 2.5V$ supply. The noise at the BP and LP outputs increases for high Q 's. Table 2 shows typical values of wideband rms noise. The numbers in parentheses are the noise measurement in mode 1 with the $S_{A/B}$ pin shorted to V^- as shown in Figure 25.

APPLICATIONS INFORMATION

Table 2. Wideband rms Noise

V_s	$\frac{f_{CLK}}{f_0}$	Notch/HP (μV_{rms})	BP (μV_{rms})	LP (μV_{rms})	CONDITIONS
$\pm 5V$	50:1	49 (42)	52 (43)	75 (65)	Mode 1, R1 = R2 = R3 Q = 1
$\pm 5V$	100:1	70 (55)	80 (58)	90 (88)	
$\pm 2.5V$	50:1	33 (31)	36 (32)	48 (43)	
$\pm 2.5V$	100:1	48 (40)	52 (40)	66 (55)	
$\pm 5V$	50:1	20 (18)	150(125)	186 (155)	Mode 1, Q = 10 R1 = R3 for BP out R1 = R2 for LP out
$\pm 5V$	100:1	25 (21)	220 (160)	240 (180)	
$\pm 2.5V$	50:1	16 (15)	100 (80)	106 (87)	
$\pm 2.5V$	100:1	20 (17)	150 (105)	150 (119)	
$\pm 5V$	50:1	57	57	62	Mode 3, R1 = R2 = R3 = R4 Q = 1
$\pm 5V$	100:1	72	72	80	
$\pm 2.5V$	50:1	40	40	42	
$\pm 2.5V$	100:1	50	50	53	
$\pm 5V$	50:1	135	120	140	Mode 3, R2 = R4, Q = 10 R3 = R1 for BP out R4 = R1 for LP and HP out
$\pm 5V$	100:1	170	160	185	
$\pm 2.5V$	50:1	100	88	100	
$\pm 2.5V$	100:1	125	115	130	

Short Circuit Currents

Short circuits to ground, positive or negative power supply are allowed as long as the power supplies do not exceed $\pm 5V$ and the ambient temperature stays below $85^\circ C$. Above $\pm 5V$ and at elevated temperatures, continuous

short circuits to the negative power supply will cause excessive currents to flow. Under these conditions, the device will get damaged if the short circuit current is allowed to exceed 80mA.

7

DEFINITION OF FILTER FUNCTIONS

Each building block of the LTC1060, together with an external clock and a few resistors, closely approximates 2nd order filter functions. These are tabulated below in the frequency domain.

Q = Quality factor of the complex pole pair. It is the ratio of f_0 to the $-3dB$ bandwidth of the 2nd order bandpass function. The Q is always measured at the filter BP output.

1. **Bandpass function:** available at the bandpass output pins (2, 19), Figure 1.

$$G(s) = H_{BP} \frac{s\omega_0/Q}{s^2 + (s\omega_0/Q) + \omega_0^2}$$

H_{BP} = Gain at $\omega = \omega_0$

$f_0 = \omega_0/2\pi$; f_0 is the center frequency of the complex pole pair. At this frequency, the phase shift between input and output is -180° .

2. **Lowpass function:** available at the LP output pins (1, 20), Figure 2.

$$G(s) = H_{LP} \frac{\omega_0^2}{s^2 + s(\omega_0/Q) + \omega_0^2}$$

H_{LP} = DC gain of the LP output.

DEFINITION OF FILTER FUNCTIONS

3. **Highpass function:** available only in mode 3 at the output pins (3, 18), Figure 3.

$$G(s) = H_{OHP} \frac{s^2}{s^2 + s(\omega_0/Q) + \omega_0^2}$$

H_{OHP} = gain of the HP output for $f \rightarrow \frac{f_{CLK}}{2}$

4. **Notch function:** available at pins 3 (18) for several modes of operation.

$$G(s) = (H_{ON2}) \frac{(s^2 + \omega_n^2)}{s^2 + s(\omega_0/Q) + \omega_0^2}$$

H_{ON2} = gain of the notch output for $f \rightarrow \frac{f_{CLK}}{2}$

H_{ON1} = gain of the notch output for $f \rightarrow 0$

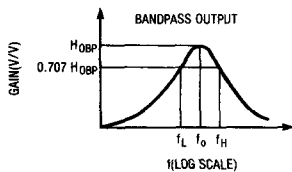
$f_n = \omega_n/2\pi$; f_n is the frequency of the notch occurrence.

5. **Allpass function:** available at pins 3(18) for mode 4, 4a.

$$G(s) = H_{OAP} \frac{[s^2 - s(\omega_0/Q) + \omega_0^2]}{s^2 + s(\omega_0/Q) + \omega_0^2}$$

H_{OAP} = gain of the allpass output for $0 < f < \frac{f_{CLK}}{2}$

For allpass functions, the center frequency and the Q of the numerator complex zero pair is the same as the denominator. Under these conditions, the magnitude response is a straight line. In mode 5, the center frequency f_z of the numerator complex zero pair, is different than f_0 . For high numerator Q's, the magnitude response will have a notch at f_z .

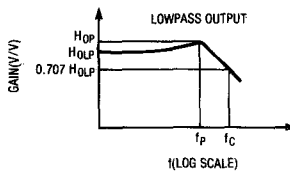


$$Q = \frac{f_0}{f_H - f_L}; f_0 = \sqrt{f_L f_H}$$

$$f_L = f_0 \left(\frac{1}{2Q} + \sqrt{\left(\frac{1}{2Q}\right)^2 + 1} \right)$$

$$f_H = f_0 \left(\frac{1}{2Q} - \sqrt{\left(\frac{1}{2Q}\right)^2 + 1} \right)$$

Figure 1

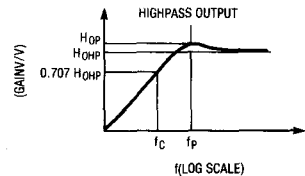


$$f_c = f_0 \times \sqrt{\left(1 - \frac{1}{2Q^2}\right) + \sqrt{\left(1 - \frac{1}{2Q^2}\right)^2 + 1}}$$

$$f_p = f_0 \sqrt{1 - \frac{1}{2Q^2}}$$

$$H_{OP} = H_{OHP} \times \frac{1}{Q \sqrt{1 - \frac{1}{4Q^2}}}$$

Figure 2



$$f_c = f_0 \times \left[\sqrt{\left(1 - \frac{1}{2Q^2}\right) + \sqrt{\left(1 - \frac{1}{2Q^2}\right)^2 + 1}} \right]^{-1}$$

$$f_p = f_0 \times \left[\sqrt{1 - \frac{1}{2Q^2}} \right]^{-1}$$

$$H_{OP} = H_{OHP} \times \frac{1}{Q \sqrt{1 - \frac{1}{4Q^2}}}$$

Figure 3

MODES OF OPERATION

Table 3. Modes of Operation: 1st Order Functions

Mode	Pin 2 (19)	Pin 3 (18)	f_c	f_z
6a	LP	HP	$\frac{f_{CLK}}{100(50)} \times \frac{R2}{R3}$	
6b	LP	LP	$\frac{f_{CLK}}{100(50)} \times \frac{R2}{R3}$	
7	LP	AP	$\frac{f_{CLK}}{100(50)} \times \frac{R2}{R3}$	$\frac{f_{CLK}}{100(50)} \times \frac{R2}{R3}$

MODES OF OPERATION

Table 4. Modes of Operation: 2nd Order Functions

Mode	Pin 1 (20)	Pin 2 (19)	Pin 3 (18)	f_o	f_n
1	LP	BP	Notch	$\frac{f_{CLK}}{100(50)}$	f_o
1a	LP	BP	BP	$\frac{f_{CLK}}{100(50)}$	
1b	LP	BP	Notch	$\frac{f_{CLK}}{100(50)} \times \sqrt{\frac{R6}{R5 + R6}}$	$\frac{f_{CLK}}{100(50)} \times \sqrt{\frac{R6}{R5 + R6}}$
1c	LP	BP	Notch	$\frac{f_{CLK}}{100(50)} \times \sqrt{1 + \frac{R6}{R5 + R6}}$	$\frac{f_{CLK}}{100(50)} \times \sqrt{1 + \frac{R6}{R5 + R6}}$
2	LP	BP	Notch	$\frac{f_{CLK}}{100(50)} \times \sqrt{1 + \frac{R2}{R4}}$	$\frac{f_{CLK}}{100(50)}$
2a	LP	BP	Notch	$\frac{f_{CLK}}{100(50)} \times \sqrt{1 + \frac{R2}{R4} + \frac{R6}{R5 + R6}}$	$\frac{f_{CLK}}{100(50)} \times \sqrt{1 + \frac{R6}{R5 + R6}}$
2b	LP	BP	Notch	$\frac{f_{CLK}}{100(50)} \times \sqrt{\frac{R2}{R4} + \frac{R6}{R5 + R6}}$	$\frac{f_{CLK}}{100(50)} \times \sqrt{\frac{R6}{R5 + R6}}$
3	LP	BP	HP	$\frac{f_{CLK}}{100(50)} \times \sqrt{\frac{R2}{R4}}$	
3a	LP	BP	Notch	$\frac{f_{CLK}}{100(50)} \times \sqrt{\frac{R2}{R4}}$	$\frac{f_{CLK}}{100(50)} \times \sqrt{\frac{R_n}{R_i}}$
4	LP	BP	AP	$\frac{f_{CLK}}{100(50)}$	
4a	LP	BP	AP	$\frac{f_{CLK}}{100(50)} \times \sqrt{\frac{R2}{R4}}$	
5	LP	BP	C.Z	$\frac{f_{CLK}}{100(50)} \times \sqrt{1 + \frac{R2}{R4}}$	$\frac{f_{CLK}}{100(50)} \times \sqrt{1 - \frac{R1}{R4}}$

7

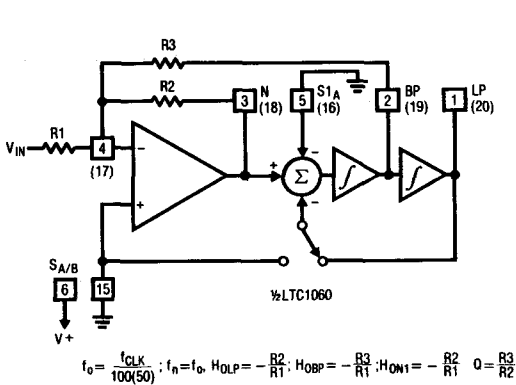


Figure 4. Mode 1: 2nd Order Filter Providing Notch, Bandpass, Lowpass

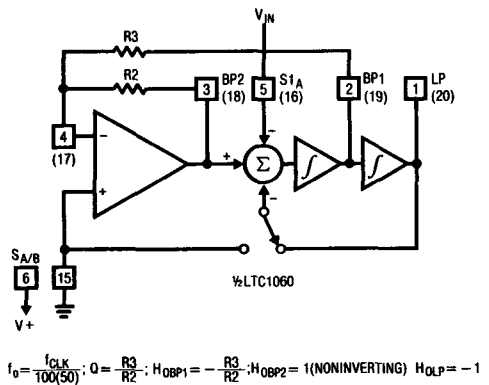
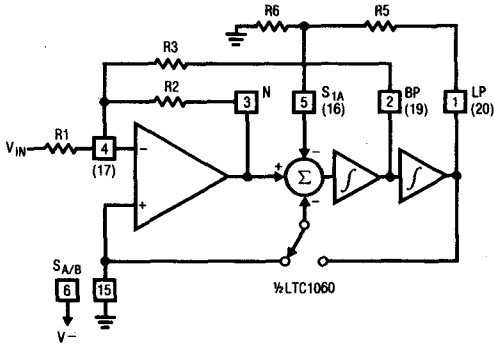


Figure 5. Mode 1a: 2nd Order Filter Providing Bandpass, Lowpass

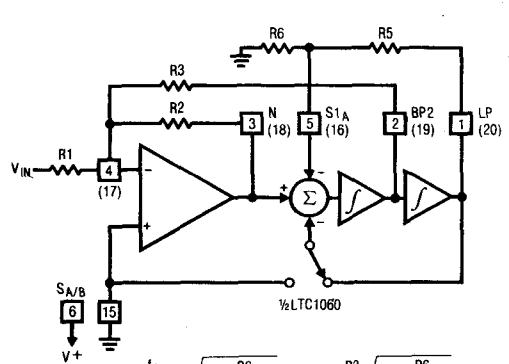
MODES OF OPERATION



$$f_o = \frac{f_{CLK}}{100(50)} \sqrt{\frac{R_6}{R_5 + R_6}}; f_n = f_o; Q = \frac{R_3}{R_2} \sqrt{\frac{R_6}{R_5 + R_6}}$$

$$H_{ON1}(f \rightarrow 0) = H_{ON2} \left(f \rightarrow \frac{f_{CLK}}{2} \right) = -\frac{R_2}{R_1}; H_{OLP} = \frac{-R_2/R_1}{R_6/(R_5 + R_6)}; H_{OBP} = -\frac{R_3}{R_1}; R_5 < 5k\Omega$$

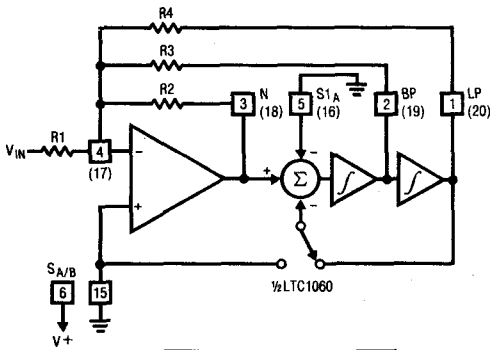
Figure 6. Mode 1b: 2nd Order Filter Providing Notch, Bandpass, Lowpass



$$f_o = \frac{f_{CLK}}{100(50)} \sqrt{1 + \frac{R_6}{R_5 + R_6}}; f_n = f_o; Q = \frac{R_3}{R_2} \sqrt{1 + \frac{R_6}{R_5 + R_6}}$$

$$H_{ON1}(f \rightarrow 0) = H_{ON2} \left(f \rightarrow \frac{f_{CLK}}{2} \right) = -\frac{R_2}{R_1}; H_{OBP} = -\frac{R_3}{R_1}; H_{OLP} = \frac{-R_2/R_1}{1 + R_6/(R_5 + R_6)}; R_5 < 5k\Omega$$

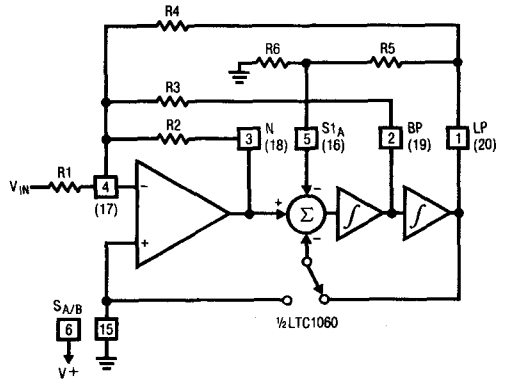
Figure 7. Mode 1c: 2nd Order Filter Providing Notch, Bandpass, Lowpass



$$f_o = \frac{f_{CLK}}{100(50)} \sqrt{1 + \frac{R_2}{R_4}}; f_n = \frac{f_{CLK}}{100(50)}; Q = \frac{R_3}{R_2} \sqrt{1 + \frac{R_2}{R_4}}; H_{OLP} = \frac{-R_2/R_1}{1 + (R_2/R_4)}$$

$$H_{OBP} = -R_3/R_1; H_{ON1}(f \rightarrow 0) = \frac{-R_2/R_1}{1 + (R_2/R_4)}; H_{ON2} \left(f \rightarrow \frac{f_{CLK}}{2} \right) = -R_2/R_1$$

Figure 8. Mode 2: 2nd Order Filter Providing Notch, Bandpass, Lowpass



$$f_o = \frac{f_{CLK}}{100(50)} \sqrt{1 + \frac{R_2}{R_4} + \frac{R_6}{R_5 + R_6}}; f_n = \frac{f_{CLK}}{100(50)} \sqrt{1 + \frac{R_6}{R_5 + R_6}}; Q = \frac{R_3}{R_2} \sqrt{1 + \frac{R_2}{R_4} + \frac{R_6}{R_5 + R_6}}$$

$$H_{ON1}(f \rightarrow 0) = -\frac{R_2}{R_1} \left\{ \frac{1 + R_6/(R_5 + R_6)}{1 + (R_2/R_4) + [R_6/(R_5 + R_6)]} \right\}; H_{ON2} \left(f \rightarrow \frac{f_{CLK}}{2} \right) = -R_2/R_1$$

$$H_{OBP} = -R_3/R_1; H_{OLP} = \frac{-R_2/R_1}{1 + (R_2/R_4) + [R_6/(R_5 + R_6)]}$$

Figure 9. Mode 2a: 2nd Order Filter Providing Notch, Bandpass, Lowpass

MODES OF OPERATION

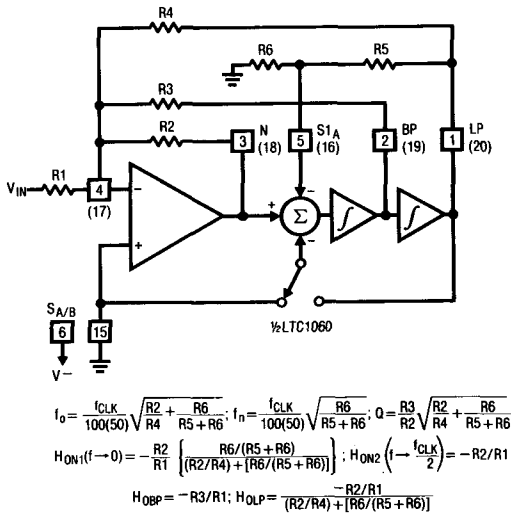


Figure 10. Mode 2b: 2nd Order Filter Providing Notch, Bandpass, Lowpass

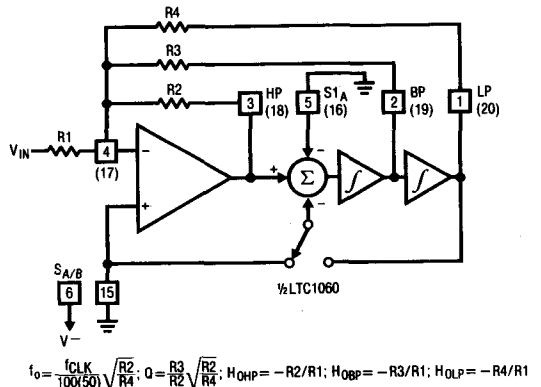


Figure 11. Mode 3: 2nd Order Filter Providing Highpass, Bandpass, Lowpass

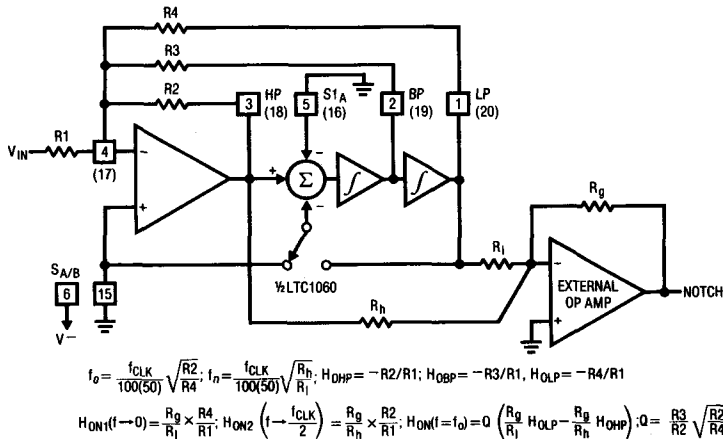


Figure 12. Mode 3a: 2nd Order Filter Providing Highpass, Bandpass, Lowpass, Notch

MODES OF OPERATION

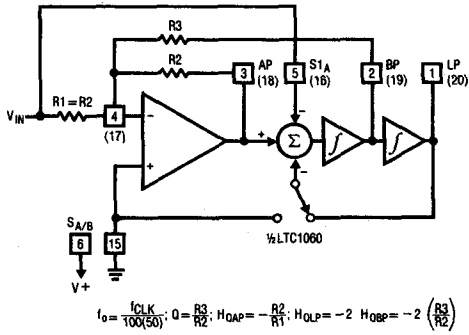


Figure 13. Mode 4: 2nd Order Filter Providing Allpass, Bandpass, Lowpass

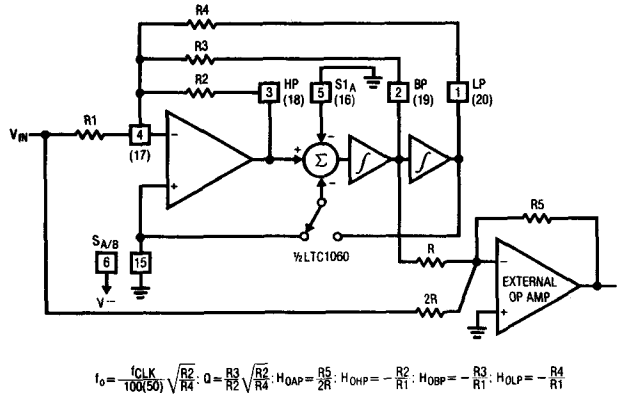


Figure 14. Mode 4a: 2nd Order Filter Providing Highpass, Bandpass, Lowpass, Allpass

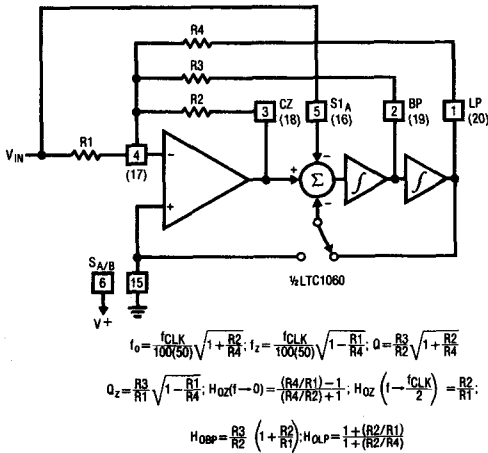


Figure 15. Mode 5: 2nd Order Filter Providing Numerator Complex Zeros, Bandpass, Lowpass

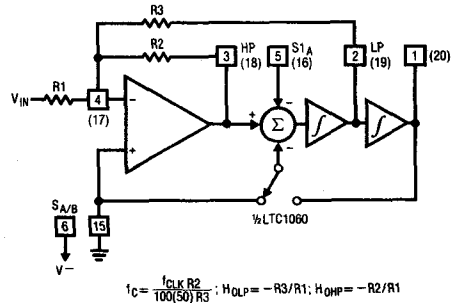


Figure 16. Mode 6a: 1st Order Filter Providing Highpass, Lowpass

MODES OF OPERATION

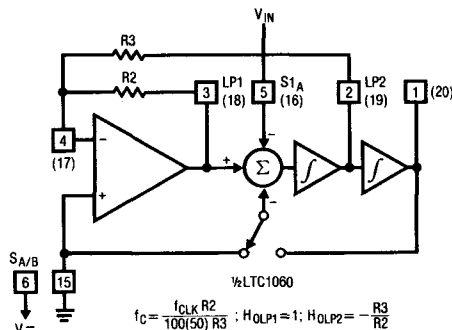


Figure 17. Mode 6b: 1st Order Filter Providing Lowpass

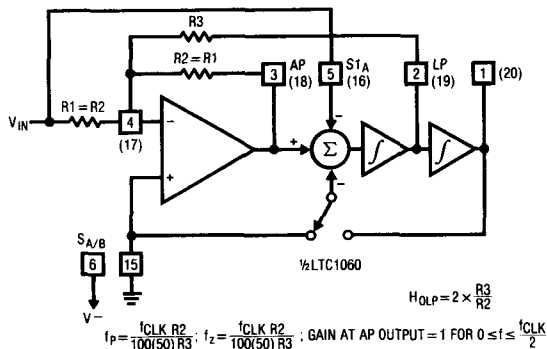


Figure 18. Mode 7: 1st Order Filter Providing Allpass, Lowpass

COMMENTS ON THE MODES OF OPERATION

There are basically three modes of operation: mode 1, mode 2, mode 3. In the mode 1, Figure 4, the input amplifier is outside the resonant loop. Because of this, mode 1 and its derivatives (mode 1a, 1b, 1c) are faster than modes 2 and 3. In mode 1, for instance, the Q errors are becoming noticeable above 1MHz clock frequency.

Mode 1a, (Figure 5), represents the most simple hook-up of the LTC1060. Mode 1a is useful when voltage gain at the bandpass output is required. The bandpass voltage gain, however, is equal to the value of Q; if this is acceptable, a second order, clock tunable, BP resonator can be achieved with only 2 resistors. The filter center frequency directly depends on the external clock frequency. For high order filters, mode 1a is not practical since it may require several clock frequencies to tune the overall filter response.

Mode 1, Figure 4, provides a clock tunable notch; the depth is shown in graph 14. Mode 1 is a practical configuration for second order clock tunable bandpass/notch filters. In mode 1, a bandpass output with a very high Q, together with unity gain, can be obtained without creating problems with the dynamics of the remaining notch and lowpass outputs.

Modes 1b and 1c, Figures 6,7 are similar. They both produce a notch with a frequency which is always equal to the filter building block center frequency. The notch and the center frequency, however, can be adjusted with an external resistor ratio.

The practical clock to center frequency ratio is:

$$\frac{500}{1} \geq \frac{f_{CLK}}{f_0} \geq \frac{100}{1} \left(\text{or } \frac{50}{1} \right); \text{ mode 1b}$$

$$\frac{100}{1} \text{ or } \frac{50}{1} \geq \frac{f_{CLK}}{f_0} \geq \frac{100}{\sqrt{2}} \text{ or } \frac{50}{\sqrt{2}}; \text{ mode 1c}$$

The input impedance of the S1 pin is clock dependent, and in general R5 should not be larger than 5k. Mode 1b can be used to increase the clock to center frequency ratio beyond 100:1. For this mode, a practical limit for the (f_{CLK}/f_0) ratio is 500:1. Beyond this, the filter will exhibit large output offsets. Mode 1c is the fastest mode of operation: In the 50:1 mode and with ($R5 = 0, R6 = \infty$) the clock to center frequency ratio becomes ($50/\sqrt{2}$) and center frequencies beyond 20kHz can easily be achieved as shown in graph 25. Figure 19, illustrates how to cascade the two sections of the LTC1060 connected in mode 1c to obtain a sharp fourth order, 1dB ripple, BP Chebyshev filter. Note that the center frequency to the BW ratio for this fourth order bandpass filter is 20/1. By varying the clock frequency to sweep the filter, the center frequency of the overall filter will increase proportionally and, so will the BW to maintain the 20:1 ratio constant. All the modes of operation yield constant Q's; with any filter realization the BW's will vary when the filter is swept. This is shown in Figure 19, where the BP filter is swept from 1kHz to 20kHz center frequency.

COMMENTS ON THE MODES OF OPERATION

Modes 2, 2a, and 2b have a notch output which frequency, f_n , can be tuned independently from the center frequency, f_0 . For all cases, however, $f_n < f_0$. These modes are useful when cascading second order functions to create an over-

all elliptic highpass, bandpass or notch response. The input amplifier and its feedback resistors (R_2/R_4) are now part of the resonant loop. Because of this, mode 2 and its derivatives are slower than mode 1's.

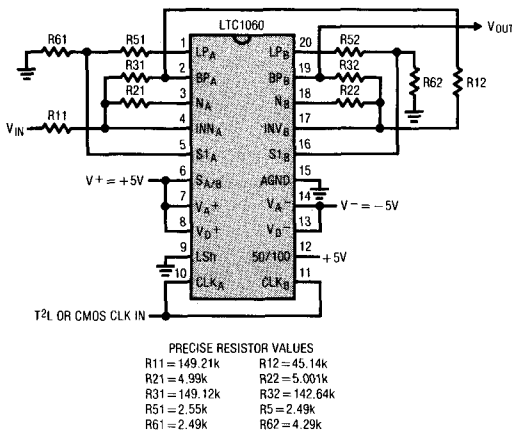


Figure 19. Cascading the 2 sections of the LTC1060 connected in mode 1c to obtain a clock tunable 4th order 1dB ripple bandpass Chebyshev filter with (center frequency) / (Ripple Bw) = 20/1.

In mode 3, Figure 11, a single resistor ratio (R_2/R_4) can tune the center frequency below or above the $f_{CLK}/100$ (or $f_{CLK}/50$) ratio. Mode 3 is a state variable configuration since it provides a highpass, bandpass, lowpass output through progressive integration; notches are obtained by summing the highpass and lowpass outputs (mode 3a, Figure 12). The notch frequency can be tuned below or above the center frequency through the resistor ratio (R_i/R_j). Because of this, modes 3 and 3a are the most versatile and useful modes for cascading second order sections to obtain high order elliptic filters. Figure 20, shows the 2 sections of an LTC1060 connected in mode 3a to obtain a clock tunable 4th order sharp elliptic bandpass filter. The first notch is created by summing directly the HP and LP outputs of the first section into the inverting input of the second section op amp. The individual Q 's are 29.6 and the filter maintains its shape and performance up to 20kHz center frequency, Figure 21. For this circuit an external op amp is required to obtain the 2nd notch. The dynamics of

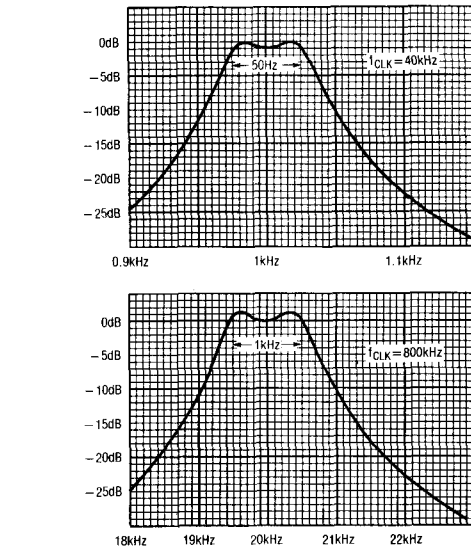
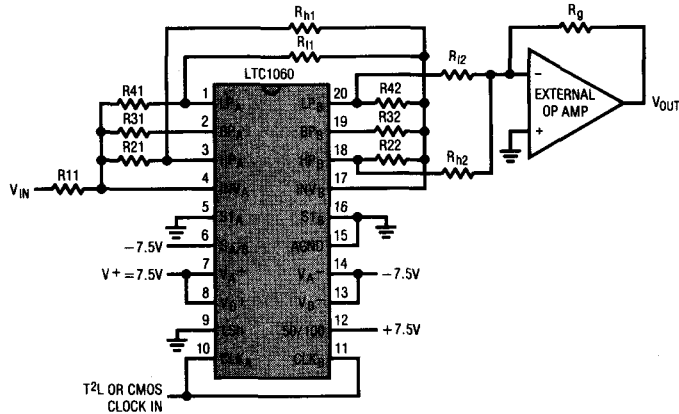


Figure 20 are excellent because the amplitude response at each output pin does not exceed 0dB. The gain in the passband depends on the ratio of $(R_g/R_{h2}) \times (R_{22}/R_{h1}) \times (R_{21}/R_{11})$. Any gain value can be obtained by acting on the (R_g/R_{h2}) ratio of the external op amp, meanwhile the remaining ratios are adjusted for optimum dynamics of the LTC1060 output nodes. The external op amp of Figure 20 is not always required. In Figure 22, one section of the LTC1060 in mode 3a is cascaded with the other section in mode 2b to obtain a 4th order function with two different notches is realized without requiring an external op amp. The clock to center frequency ratio is adjusted to 200:1; this is done in order to better approximate a linear R,C notch filter. The amplitude response of the filter is shown in Figure 23 with up to 1MHz clock frequency. The 0dB bandwidth to the stop bandwidth ratio is 9/1. When the filter is centered at 1kHz, it should theoretically have a 44dB rejection with a 50Hz

COMMENTS ON THE MODES OF OPERATION

stop bandwidth. For a more narrow filter than the above, the unused BP output of the mode 2b section, Figure 22, has a gain exceeding unity which limits the dynamic range of the overall filter. For very selective bandpass/band-

reject filters, the mode 3a approach as in Figure 20, yields better dynamic range since the external op amp helps to optimize the dynamics of the output nodes of the LTC1060.



RESISTOR VALUES

R11 = 155.93k	R21 = 5k	R31 = 152k	R41 = 5.27k
R _{h1} = 13.2k	R _{h1} = 10.74k	R22 = 5.26k	R32 = 151.8k
R42 = 5k	R _{h2} = 6.11k	R _{h2} = 5k	R _g = 37.3k

NOTE: FOR CLOCK FREQUENCIES ABOVE 700kHz A 12pF CAPACITOR ACROSS R41 AND A 20pF CAPACITOR ACROSS R42 WERE USED TO PREVENT THE PASSBAND RIPPLE FROM ANY ADDITIONAL PEAKING.

Figure 20. Combining mode 3 with mode 3a to make the 4th order BP filter of Figure 21 with improved dynamics. The gain at each output node is ≤ 0 dB for all input frequencies.

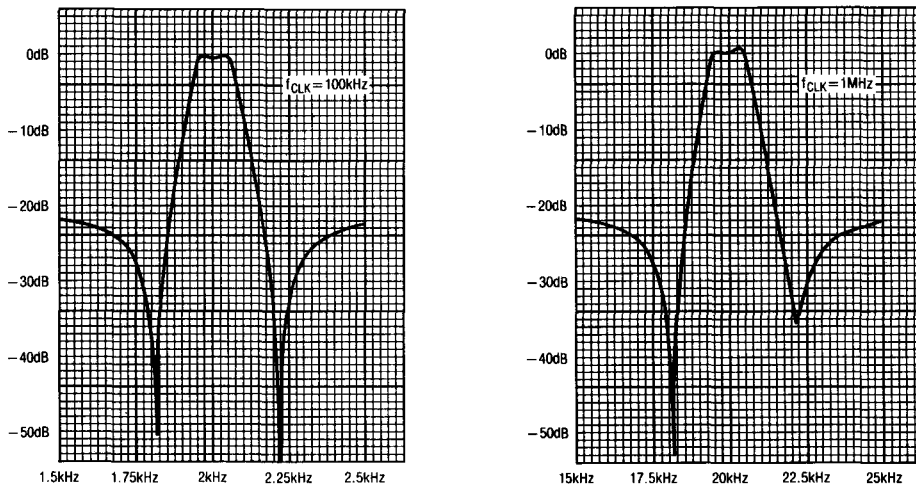


Figure 21. The BP filter of Figure 20, when swept from a 2kHz to 20kHz center frequency.

COMMENTS ON THE MODES OF OPERATION

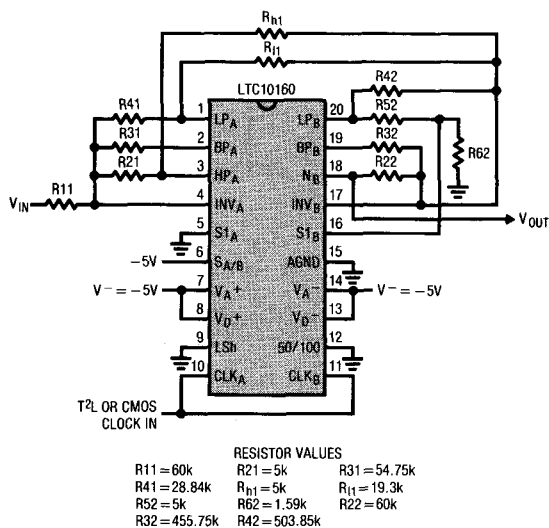


Figure 22. Combining mode 3 with mode 2b to create a 4th order BR elliptic filter with 1dB ripple and a ratio of 0dB to stop bandwidth equal to 9/1.

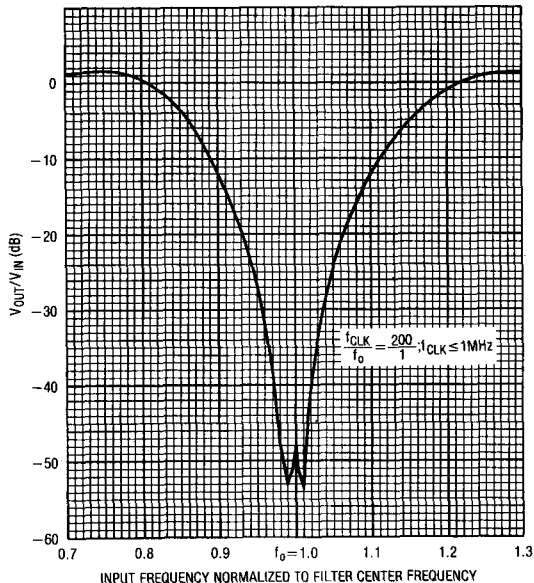


Figure 23. Amplitude Response of the notch filter of Figure 22.

LTC1060 OFFSETS

Switched capacitor integrators generally exhibit higher input offsets than discrete R,C integrators.

These offsets are mainly due to the charge injection of the CMOS switches into the integrating capacitors and they are temperature independent. The internal op amp offsets also add to the overall offset budget and they are typically a couple of millivolts.

Because of this, the DC output offsets of switched capacitor filters are usually higher than the offsets of discrete active filters.

Figure 24 shows half of an LTC1060 filter building block with its equivalent input offsets V_{OS1} , V_{OS2} , V_{OS3} . All three are 100% tested for both sides of the LTC1060. V_{OS2} is generally the larger offset. When the $S_{A/B}$, pin 6, of the LTC 1060 is shorted to the negative supply (i.e., mode 3), the value of the V_{OS2} decreases. Additionally, with $S_{A/B}$ low, a 20%–30% noise reduction is observed. Mode 1 can still be achieved, if desired, by shorting the S1 pin to the lowpass output, Figure 25.

LTC1060 OFFSETS

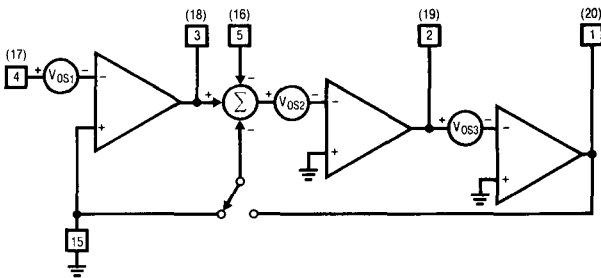


Figure 24. Equivalent Input Offsets of 1/2 LTC1060 Filter Building Block

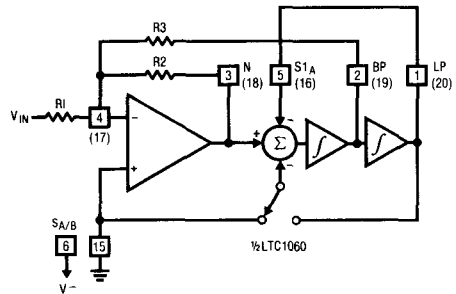


Figure 25. Mode 1(LN): Same Operation as Mode 1 but Lower Vos2 Offset and Lower Noise

Output Offsets

The DC offset at the filter bandpass output is always equal to Vos3. The DC offsets at the remaining two outputs (Notch and LP) depend on the mode of operation and external resistor ratios. Table 5 illustrates this.

It is important to know the value of the DC output offsets,

especially when the filter handles input signals with large dynamic range. As a rule of thumb, the output DC offsets increase when:

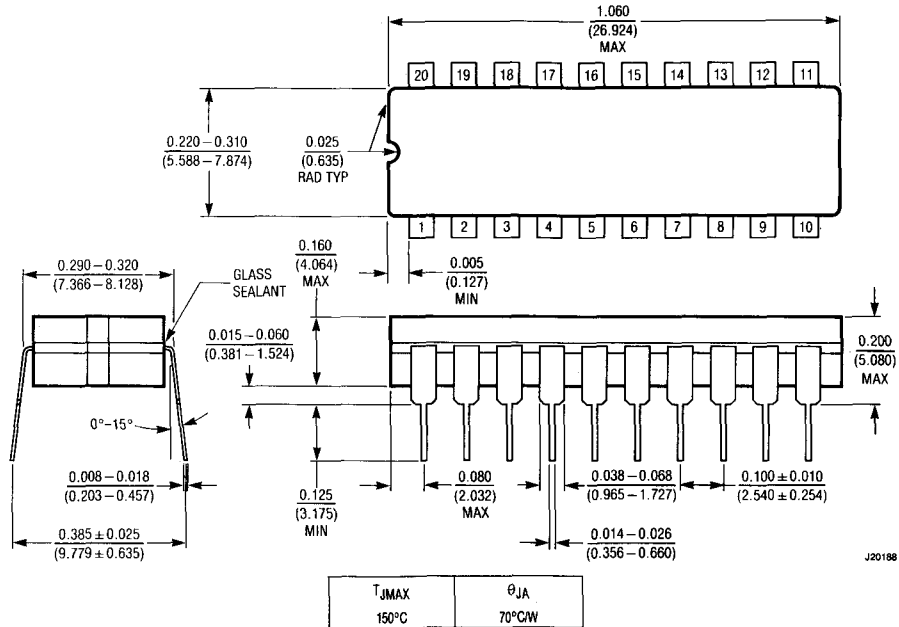
1. The Q's decrease
2. The ratio (fCLK/f0) increases beyond 100:1. This is done by decreasing either the (R2/R4) or the R6/(R5 + R6) resistor ratios.

Table 5

Mode	V _{OSN} Pin 3 (18)	V _{OSBP} Pin 2 (19)	V _{OSLP} Pin 1 (20)
1,4	$V_{OS1}[(1/Q) + 1 + 1H_{OLP}] - V_{OS3}/Q$	V _{OS3}	V _{OSN} - V _{OS2}
1a	$V_{OS1}[1 + (1/Q)] - V_{OS3}/Q$	V _{OS3}	V _{OSN} - V _{OS2}
1b	$V_{OS1}[(1/Q) + 1 + R2/R1] - V_{OS3}/Q$	V _{OS3}	$-(V_{OSN} - V_{OS2})(1 + R5/R6)$
1c	$V_{OS1}[(1/Q) + 1 + R2/R1] - V_{OS3}/Q$	V _{OS3}	$-(V_{OSN} - V_{OS2}) \frac{(R5 + R6)}{(R5 + 2R6)}$
2, 5	$[V_{OS1}(1 + R2/R1 + R2/R3 + R2/R4) - V_{OS3}(R2/R3)] \times [R4/(R2 + R4)] + V_{OS2}[R2/(R2 + R4)]$	V _{OS3}	V _{OSN} - V _{OS2}
2a	$[V_{OS1}(1 + R2/R1 + R2/R3 + R2/R4) - V_{OS3}(R2/R3)] \times \left[\frac{R4(1+k)}{R2 + R4(1+k)} \right] + V_{OS2} \left[\frac{R2}{R2 + R4(1+k)} \right]; k = \frac{R6}{R5 + R6}$	V _{OS3}	$-(V_{OSN} - V_{OS2}) \frac{(R5 + R6)}{(R5 + 2R6)}$
2b	$[V_{OS1}(1 + R2/R1 + R2/R3 + R2/R4) - V_{OS3}(R2/R3)] \times \left[\frac{R4k}{R2 + R4k} \right] + V_{OS2} \left[\frac{R2}{R2 + R4k} \right]; k = \frac{R6}{R5 + R6}$	V _{OS3}	$-(V_{OSN} - V_{OS2})(1 + R5/R6)$
3, 4a	V _{OS2}	V _{OS3}	$V_{OS1} \left[1 + \frac{R4}{R1} + \frac{R4}{R2} + \frac{R4}{R3} \right] - V_{OS2} \left(\frac{R4}{R2} \right) - V_{OS3} \left(\frac{R4}{R3} \right)$

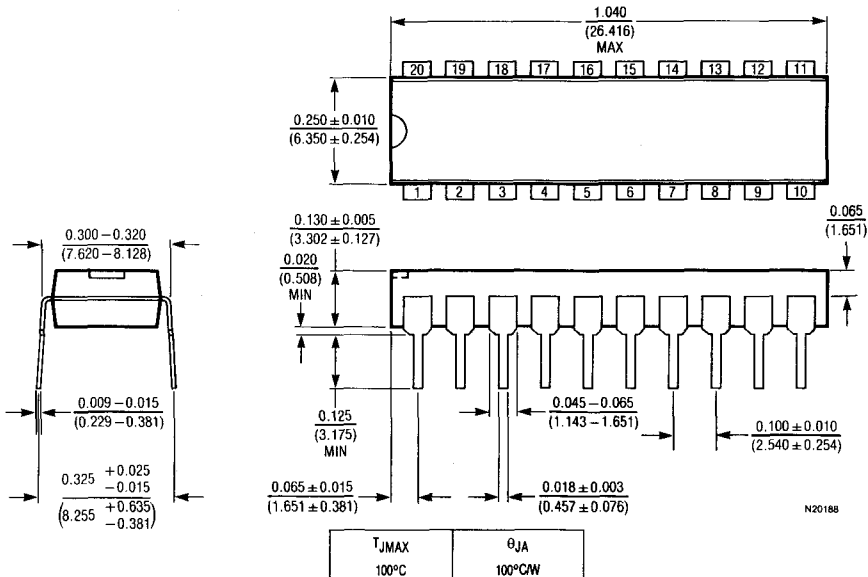
PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

**J Package
20 Lead CERDIP**



J20188

**N Package
20 Lead Molded DIP**



N20188

FEATURES

- Operates from $\pm 2.5V$ supply up to $\pm 8V$
- Operates up to 30kHz
- Low Power and 88dB Dynamic Range at $\pm 2.5V$ Supply
- Center Frequency Q Product up to 1.6MHz
- *Guaranteed* Offset Voltages
- *Guaranteed* Clock to Center Frequency Accuracy over Temperature, 0.8% or Better
- *Guaranteed* Q Accuracy over Temperature
- Low Temperature Coefficient of Q and Center Frequency
- Low Crosstalk, 70dB
- Clock Inputs TTL and CMOS Compatible

APPLICATIONS

- Single 5V Supply Medium Frequency Filters
- Very High Q and High Dynamic Range Bandpass, Notch Filters
- Tracking Filters
- Telecom Filters

DESCRIPTION

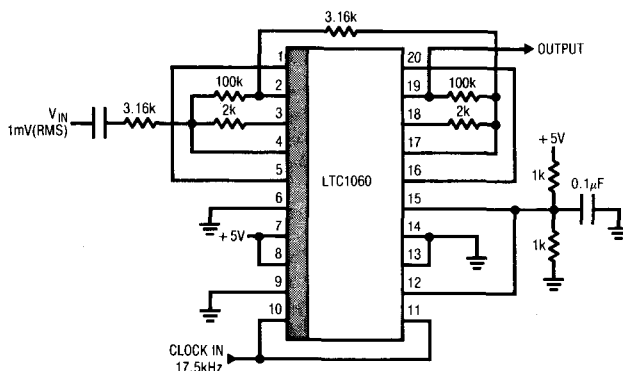
The LTC1060 consists of two high performance, switched capacitor filters. Each filter, together with 2 to 5 resistors, can produce various 2nd order filter functions such as low-pass, bandpass, highpass notch and allpass. The center frequency of these functions can be tuned by an external clock, or by an external clock and resistor ratio. Up to 4th order full biquadratic functions can be achieved by cascading the two filter blocks. Any of the classical filter configurations (like Butterworth, Chebyshev, Bessel, Cauer) can be formed.

The LTC1060 operates with either a single or dual supply from $\pm 2.37V$ to $\pm 8V$. When used with low supply (i.e., single 5V supply), the filter typically consumes 12mW and can operate with center frequencies up to 10kHz. With $\pm 5V$ supply, the frequency range extends to 30kHz and very high Q values can also be obtained.

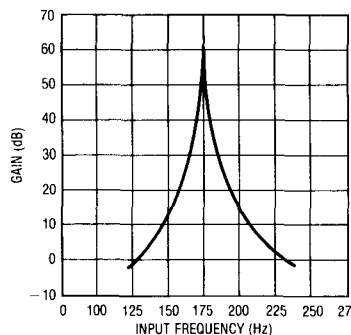
The LTC1060 is manufactured by using Linear Technology's enhanced LTCMOS™ silicon gate process. Because of this, low offsets, high dynamic range, high center frequency Q product and excellent temperature stability are obtained.

LTCMOS™ is a trademark of Linear Technology Corp.

Single 5V, Gain of 1000 4th Order Bandpass Filter



Amplitude Response

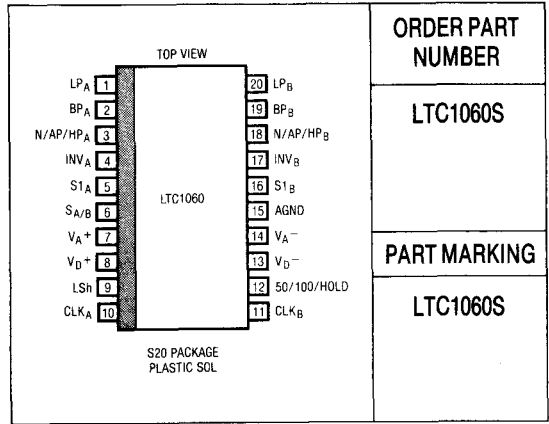


LTC1060CS

ABSOLUTE MAXIMUM RATINGS

Supply Voltage 18V
 Operating Temperature Range $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$
 Storage Temperature Range -65°C to 150°C
 Lead Temperature (Soldering, 10 sec.) 300°C

PACKAGE/ORDER INFORMATION



ORDER PART NUMBER

LTC1060S

PART MARKING

LTC1060S

ELECTRICAL CHARACTERISTICS (Complete Filter) $V_S = \pm 5\text{V}$, $T_A = 25^{\circ}\text{C}$ unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Center Frequency Range	$f_o \times Q \leq 400\text{kHz}$, Mode 1 $f_o \times Q \leq 1.6\text{MHz}$, Mode 1		0.1-20k 0.1-16k		Hz Hz
Clock to Center Frequency Ratio (Note 1)	Mode 1, 50:1, $f_{\text{CLK}} = 250\text{kHz}$, $Q = 10$ Mode 1, 100:1, $f_{\text{CLK}} = 500\text{kHz}$, $Q = 10$	●		50 ± 0.8% 100 ± 0.8%	
Q Accuracy (Note 1)	Mode 1, 50:1 or 100:1, $f_o = 5\text{kHz}$ $Q = 10$	●	± 0.5	5	%
f_o Temperature Coefficient Q Temperature Coefficient	Mode 1, $f_{\text{CLK}} < 500\text{kHz}$ Mode 1, $f_{\text{CLK}} < 500\text{kHz}$, $Q = 10$		- 10 + 20		ppm/°C ppm/°C
DC Offset V_{OS1} (Note 2)	●		2	15	mV
V_{OS2}	●		3	40	mV
V_{OS2}	●		6	80	mV
V_{OS2}	●		2	30	mV
V_{OS2}	●		4	60	mV
V_{OS3}	●		2	30	mV
V_{OS3}	●		4	60	mV
DC Low Pass Gain Accuracy	Mode 1, $R1 = R2 = 50\text{k}$		± 0.1	2	%
BP Gain Accuracy at f_o	Mode 1, $Q = 10$, $f_o = 5\text{kHz}$		± 0.1		%
Clock Feedthrough	$f_{\text{CLK}} \leq 1\text{MHz}$		10		mV(p-p)
Max. Clock Frequency			1.5		MHz
Power Supply Current	●	3	5	8	mA
Crosstalk				12	mA
			70		dB

Note 1: An LTC1060S with improved Q and clock to center frequency ratio accuracy can be made available upon special request.

Note 2: For definition of the DC offset voltages refer to the LTC1060 data sheet. An LTC1060S with improved DC offset specifications can be made available upon special request.

ELECTRICAL CHARACTERISTICS (Complete Filter) $V_S = \pm 2.37V, T_A = 25^\circ C$

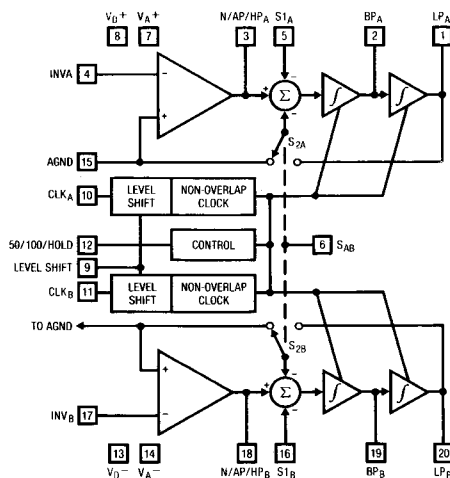
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Center Frequency Range	$f_0 \times Q \leq 100kHz$		0.1-10k		Hz
Clock to Center Frequency Ratio	Mode 1, 50:1, $f_{CLK} = 250kHz, Q = 10$ Mode 1, 100:1, $f_{CLK} = 250kHz, Q = 10$		$50 \pm 0.8\%$ $100 \pm 0.8\%$		
Q Accuracy	Mode 1, $f_0 = 2.5kHz, Q = 10$ 50:1 and 100:1		± 2		%
Max Clock Frequency			500		kHz
Power Supply Current			2.5	4	mA

ELECTRICAL CHARACTERISTICS (Internal Op Amps) $T_A = 25^\circ C$

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage Range		± 2.37		± 8	V
Voltage Swings	$V_S = \pm 5V, R_L = 5k$ (Pins 1, 2, 19, 20) $R_L = 3.5k$ (Pins 3, 18)	± 3.8 ± 3.6	± 4 ± 4		V V
Output Short Circuit Current	$V_S = \pm 5V$				
Source			25		mA
Sink			3		mA
Op Amp GBW Product	$V_S = \pm 5V$		2		MHz
Op Amp Slew Rate	$V_S = \pm 5V$		7		V/ μs
Op Amp DC Open Loop Gain	$R_L = 10k, V_S = \pm 5V$		85		dB

The ● denotes the specifications which apply over the full operating temperature range.

BLOCK DIAGRAM



NOTES

High Performance Triple Universal Filter Building Block

FEATURES

- Up to 6th Order Filter Functions with a Single 20 Pin 0.3" Wide Package
- Center Frequency Range up to 35kHz
- $f_0 \times Q$ Product Up to 1 MHz
- *Guaranteed* Center Frequency and Q Accuracy Over Temperature
- *Guaranteed* Low Offset Voltages Over Temperature
- 90dB Signal to Noise Ratio
- Filter Operates From Single 4.7V Supply and Up to $\pm 8V$ Supplies
- *Guaranteed* Filter Specifications with $\pm 5V$ Supply and $\pm 2.37V$ Supply
- Low Power Consumption with Single 5V Supply
- Clock Inputs T²L and CMOS Compatible

APPLICATIONS

- High Order, Wide Frequency Range Bandpass, Lowpass, Notch Filters
- Low Power Consumption, Single 5V Supply Clock Tunable Filters
- Tracking Filters
- Antialiasing Filters

LTCMOS™ is a trademark of Linear Technology Corp.

DESCRIPTION

The LTC1061 consists of three high performance, universal filter building blocks. Each filter building block together with an external clock and 2 to 5 resistors can produce various second order functions which are available at its three output pins. Two out of three always provide lowpass and bandpass functions while the third output pin can produce highpass or notch or allpass. The center frequency of these functions can be tuned with an external clock or an external clock and a resistor ratio. For $Q < 5$, the center frequency ranges from 0.1Hz to 35kHz. For Q's of 10 or above, the center frequency ranges from 0.1Hz to 28kHz.

The LTC1061 can be used with single or dual supplies ranging from $\pm 2.37V$ to $\pm 8V$ (or 4.74V to 16V). When the filter operates with supplies of $\pm 5V$ and above, it can handle input frequencies up to 100kHz.

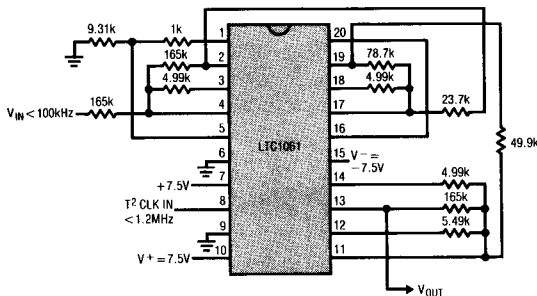
The LTC1061 is compatible with the LTC1059 single universal filter and the LTC1060 dual. Higher than 6th order functions can be obtained by cascading the LTC1061 with the LTC1059 or LTC1060. Any classical filter realization can be obtained.

The LTC1061 is manufactured by using Linear Technology's enhanced LTCMOS™ silicon gate process.

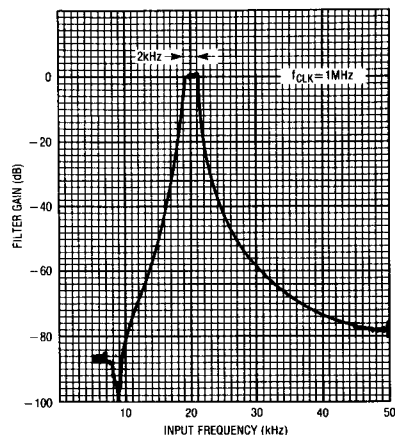
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TYPICAL APPLICATION

6th Order, Clock Tunable, 0.5dB Ripple Chebyshev BP Filter



Amplitude Response

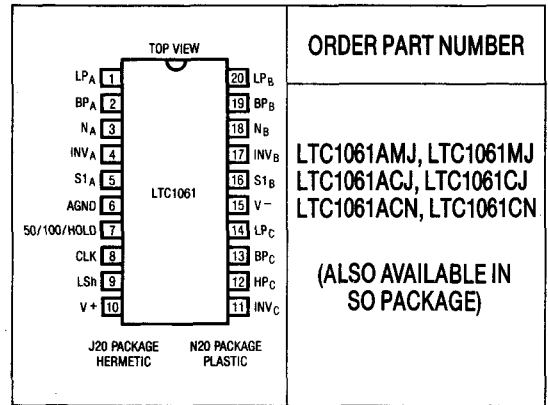


LTC1061

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	18V
Power Dissipation	500mW
Operating Temperature Range	
LTC1061AC, LTC1061C	$-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$
LTC1061AM, LTC1061M	$-55^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$
Storage Temperature Range	-65°C to 150°C
Lead Temperature (Soldering, 10sec)	300°C

PACKAGE/ORDER INFORMATION



ELECTRICAL CHARACTERISTICS

(Complete Filter) $V_S = \pm 5V$, $T_A = 25^{\circ}\text{C}$, T^2L clock input level, unless otherwise specified

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Center Frequency Range, f_o	$f_o \times Q \leq 175\text{kHz}$, Mode 1, $V_S = \pm 7.5V$ $f_o \times Q \leq 1.6\text{MHz}$, Mode 1, $V_S = \pm 7.5V$ $f_o \times Q \leq 75\text{kHz}$, Mode 3, $V_S = \pm 7.5V$ $f_o \times Q \leq 1\text{MHz}$, Mode 3, $V_S = \pm 7.5V$ (Note 1)		0.1-35k 0.1-25k 0.1-25k 0.1-17k		Hz Hz Hz Hz
Input Frequency Range			0-200k		Hz
Clock to Center Frequency Ratio, f_{CLK}/f_o					
LTC1061A LTC1061	Sides A, B: Mode 1, $R1 = R3 = 50\text{k}\Omega$ $R2 = 5\text{k}\Omega$, $Q = 10$, $f_{CLK} = 250\text{kHz}$ Pin 7 High.	● ●		50 ± 0.6% 50 ± 1.2%	
LTC1061A LTC1061	Side C: Mode 3, $R1 = R3 = 50\text{k}\Omega$ $R2 = R4 = 5\text{k}\Omega$, $f_{CLK} = 250\text{kHz}$ Same as Above, Pin 7 at Mid-Supplies, $f_{CLK} = 500\text{kHz}$	● ●		100 ± 0.6% 100 ± 1.2%	
Clock to Center Frequency Ratio, Side to Side Matching LTC1061				1.2%	
Q Accuracy LTC1061A LTC1061	Sides A, B, Mode 1 Side C, Mode 3 $f_o \times Q \leq 50\text{kHz}$, $f_o \leq 5\text{kHz}$	● ●	± 2 ± 3	5 5	% %
f_o Temperature Coefficient	Mode 1, 50:1, $f_{CLK} < 300\text{kHz}$		± 1		ppm/°C
Q Temperature Coefficient	Mode 1, 100:1, $f_{CLK} < 500\text{kHz}$		± 5		ppm/°C
	Mode 3, $f_{CLK} < 500\text{kHz}$		± 5		ppm/°C

ELECTRICAL CHARACTERISTICS(Complete Filter) $V_S = \pm 5V$, $T_A = 25^\circ C$, T^2L clock input level, unless otherwise specified

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
DC Offset Voltage V_{OS1} , Figure 23			2	15	mV
V_{OS2}	$f_{CLK} = 250kHz, 50:1$		3	30	mV
V_{OS2}	$f_{CLK} = 500kHz, 100:1$		6	60	mV
V_{OS3}	$f_{CLK} = 250kHz, 50:1$		3	20	mV
V_{OS3}	$f_{CLK} = 500kHz, 100:1$		6	40	mV
Clock Feedthrough	$f_{CLK} < 1MHz$		0.4		mV _{RMS}
Max. Clock Frequency	Mode 1, $Q < 5$, $V_S \geq \pm 5V$		2.5		MHz
Power Supply Current		6	8	11	mA
				15	mA

ELECTRICAL CHARACTERISTICS (Complete Filter) $V_S = \pm 2.37V$, $T_A = 25^\circ C$ unless otherwise specified

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Center Frequency Range, f_o	$f_o \times Q \leq 120kHz$, Mode 1, 50:1 $f_o \times Q \leq 120kHz$, Mode 3, 50:1		0.1-12k 0.1-10k		Hz Hz
Input Frequency Range			0-20k		Hz
Clock to Center Frequency Ratio LTC1061A LTC1061 LTC1061A LTC1061	50:1, $f_{CLK} = 250kHz$, $Q = 10$ Sides A, B: Mode 1 Side C: Mode 3 100:1, $f_{CLK} = 250kHz$, $Q = 10$ Sides A, B: Mode 1 Side C: Mode 3			50 ± 0.6%	
Q Accuracy LTC1061A LTC1061	Same as Above		± 2 ± 3		% %
Max. Clock Frequency			700k		Hz
Power Supply Current			4.5	6	mA

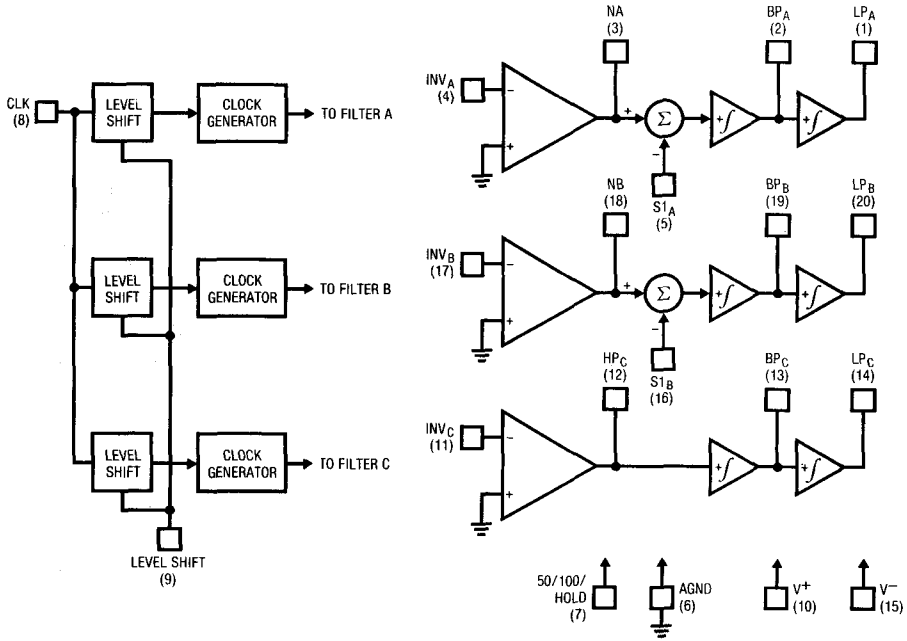
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ELECTRICAL CHARACTERISTICS (Internal Op Amps) $T_A = 25^\circ C$ unless otherwise specified

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage Range		± 2.37		± 9	V
Voltage Swings LTC1061A LTC1061 LTC1061, LTC1061A	$V_S = \pm 5V$, $R_L = 5k$ (Pins 1, 2, 13, 14, 19, 20) $R_L = 3.5k$ (Pins 3, 12, 18)	± 4 ± 3.8 ± 3.6	± 4.2 ± 4.2		V V V
Output Short Circuit Current Source/Sink	$V_S = \pm 5V$		40/3		mA
DC Open Loop Gain	$V_S = \pm 5V$, $R_L = 5k$		80		dB
GBW Product	$V_S = \pm 5V$		3		MHz
Slew Rate	$V_S = \pm 5V$		7		V/ μs

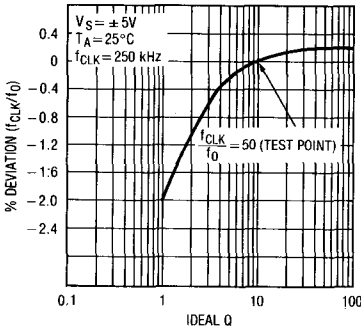
The ● denotes the specifications which apply over the full operating temperature range.

BLOCK DIAGRAM

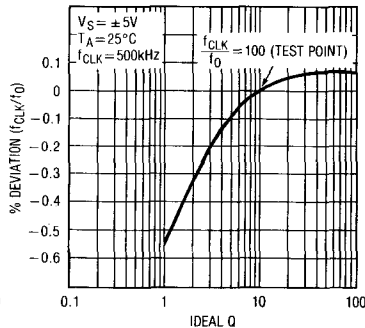


TYPICAL PERFORMANCE CHARACTERISTICS

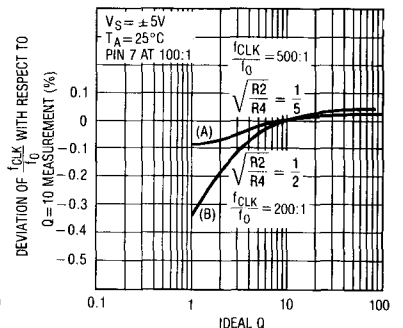
**Graph 1. Mode 1, Mode 3
(f_{CLK}/f_o) Deviation vs Q**



**Graph 2. Mode 1, Mode 3
(f_{CLK}/f_o) Deviation vs Q**

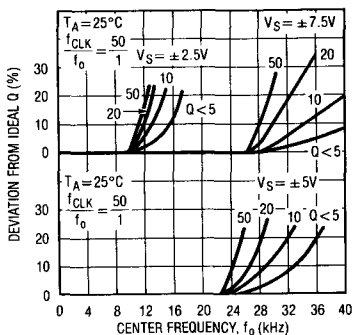


**Graph 3. Mode 3: Deviation of
(f_{CLK}/f_o) with Respect to Q = 10
Measurement**

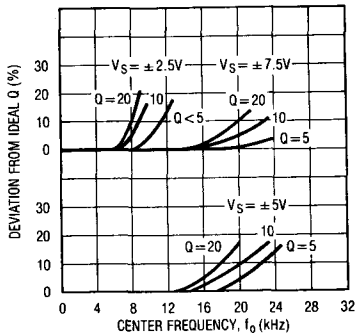


TYPICAL PERFORMANCE CHARACTERISTICS

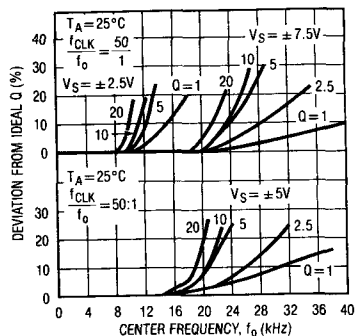
Graph 4. Mode 1: (f_{CLK}/f_o) = 50:1



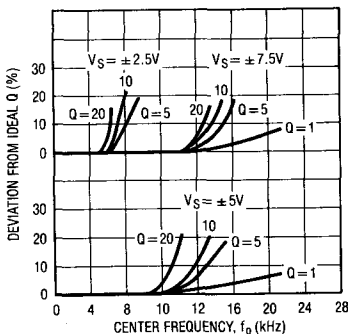
Graph 5. Mode 1: (f_{CLK}/f_o) = 100:1



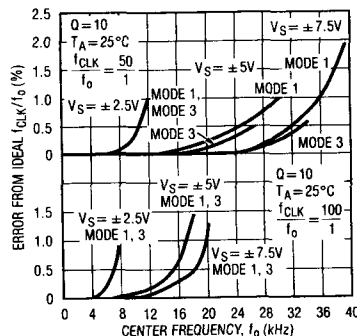
Graph 6. Mode 3: (f_{CLK}/f_o) = 50:1



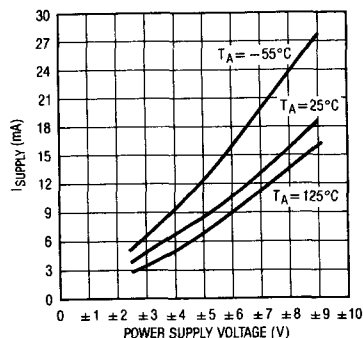
Graph 7. Mode 3: (f_{CLK}/f_o) = 100:1



Graph 8. f_{CLK}/f_o vs f_o



Graph 9. Power Supply Current vs Supply Voltage



PIN DESCRIPTION AND APPLICATION HINTS

Power Supplies (Pins 10, 15)

They should be bypassed with 0.1 μ F disc ceramic. Low noise, non-switching, power supplies are recommended. The device operates with a single 5V supply, Figure 1, and with dual supplies. The absolute maximum operating power supply voltage is ± 9 V.

Clock and Level Shift (Pins 8, 9)

When the LTC1061 operates with symmetrical dual supplies the level shift Pin 9 should be tied to analog ground.

For single 5V supply operation the level shift pin should be tied to Pin 15 which will be the system ground. The typical logic threshold levels of the clock pin are as follows: 1.65V above the level shift pin for ± 5 V supply operation, 1.75V for ± 7.5 V and above, and 1.4V for single 5V supply operation. The logic threshold levels vary ± 100 mV over the full military temperature range. The recommended duty cycle of the input clock is 50% although for clock frequencies below 500kHz the clock "on" time can be as low as 300ns. The maximum clock frequency for ± 5 V supplies and above is 2.4MHz.

PIN DESCRIPTION AND APPLICATION HINTS

S1A, S1B (Pins 5, 16)

These are voltage input pins. If used, they should be driven with a source impedance below 5kΩ. When they are not used, they should be tied to the analog ground Pin 6.

AGND (Pin 6)

When the LTC1061 operates with dual supplies, Pin 6 should be tied to system ground. When the LTC1061 operates with a single positive supply, the analog ground pin should be tied to 1/2 supply, Figure 1. The positive input of all the internal op amps, as well as the common reference of all the internal switches, are internally tied to the analog ground pin. Because of this, a “clean” ground is recommended.

50/100/Hold (Pin 7)

By tying Pin 7 to V^+ , the filter operates with a clock to center frequency internally set at 50:1. When Pin 7 is at mid-supplies, the filter operates with a 100:1 clock to center frequency ratio. Table 1 shows the allowable variation of the potential at Pin 7 when the 100:1 mode is sought.

When Pin 7 is shorted to the negative supply pin, the filter operation is stopped and the bandpass and lowpass output act as a sample and hold circuit holding the last sample of the input voltage. The hold step is around 2mV and the droop rate is 150μV/sec.

Table 1

Total Power Supply	Voltage Range of Pin 7 for 100:1 Operation
5V	2.5V ± 0.5V
10V	5V ± 1V
15V	7.5V ± 1.5V

Clock Feedthrough

This is defined as the amplitude of the clock frequency appearing at the output pins of the device, Figure 2. Clock feedthrough is measured with all three sides of the LTC1061 connected as filters. The clock feedthrough mainly depends on the magnitude of the power supplies and it is independent from the input clock levels, clock frequency and modes of operation.

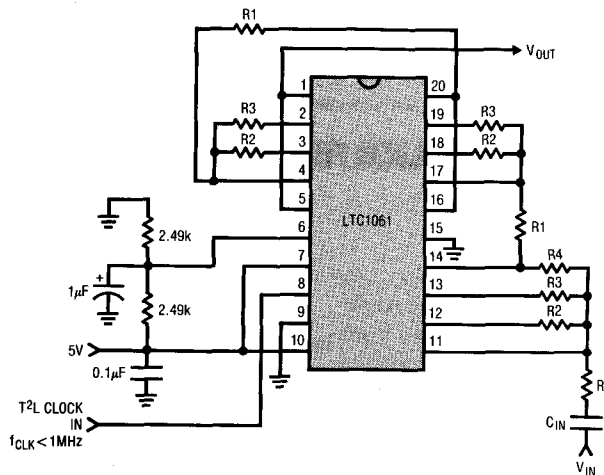


Figure 1. The 6th order LP Butterworth Filter of Figure 5 Operating with a Single 5V Supply.

PIN DESCRIPTION AND APPLICATION HINTS

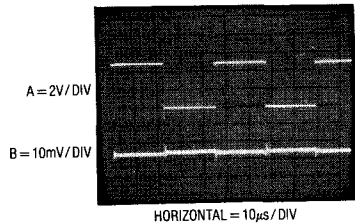


Figure 2. Typical Clock Feedthrough of the LTC1061 Operating with ±5V Supplies. Top Trace is the Input Clock Swinging 0-5V and Bottom Trace is One of the Lowpass Outputs with Zero or DC Input Signals.

Table 2 illustrates the typical clock feedthrough numbers for various power supplies.

Table 2

Power Supply	Clock Feedthrough
±2.5V	0.2mV _{RMS}
±5V	0.4mV _{RMS}
±8V	0.8mV _{RMS}

Definition of Filter Functions

Refer to LTC1060 datasheet.

MODES OF OPERATION

Description and Applications

1. Primary Modes: There are two basic modes of operation, Mode 1 and Mode 3. In Mode 1, the ratio of the external clock frequency to the center frequency of each 2nd order section is internally fixed at 50:1 or 100:1. In Mode 3, this ratio can be adjusted above or below 50:1 or 100:1. The side C of the LTC1061 can be connected only in Mode 3. Figure 3 illustrates Mode 1 providing 2nd order notch, lowpass, and bandpass outputs (for definition of filter func-

tions refer to the LTC1060 datasheet). Mode 1 can be used to make high order Butterworth lowpass filters; it can also be used to make low Q notches and for cascading 2nd order bandpass functions tuned at the same center frequency and with unity gain. Mode 3, Figure 4, is the classical state variable configuration providing highpass, bandpass and lowpass second order filter functions.

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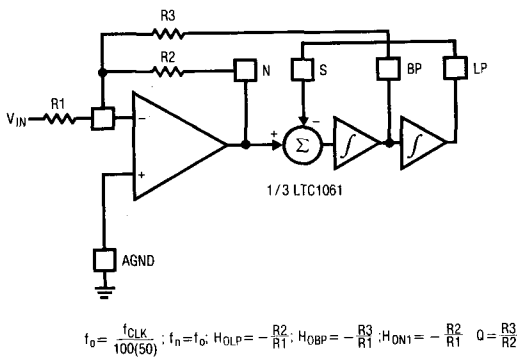


Figure 3. Mode 1: 2nd Order Filter Providing Notch, Bandpass, Lowpass.

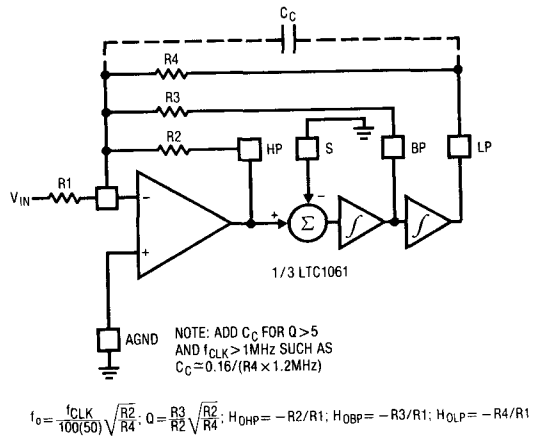


Figure 4. Mode 3: 2nd Order Filter Providing Highpass, Bandpass, Lowpass.

MODES OF OPERATION

Since the input amplifier is within the resonant loop, its phase shift affects the high frequency operation of the filter and therefore, Mode 3 is slower than Mode 1. Mode 3 can be used to make high order all-pole bandpass, low-pass, highpass and notch filters. Mode 3 as well as Mode 1 is a straightforward mode to use and the filter's dynamics can easily be optimized. Figure 5 illustrates a 6th order lowpass Butterworth filter operating with up to 40kHz cutoff frequency and with up to 200kHz input frequency. Sides A, B are connected in Mode 1 while side C is connected in Mode 3. The lower Q section was placed in side C, Mode 3, to eliminate any early Q enhancement. This could happen when the clock approaches 2MHz. The measured frequency response is shown in Figure 6. The attenuation floor is limited by the crosstalk between the three different sections operating with a clock frequency above 1MHz. The measured wideband noise was $150\mu\text{VRMS}$. For limited temperature range the filter of Figure 5 works up to 2.5MHz clock frequency thus yielding a 50kHz cutoff.

2. Secondary Modes: Mode 1b—It is derived from Mode 1. In Mode 1b, Figure 7, two additional resistors, R5 and R6, are added to attenuate the amount of voltage fed back from the lowpass output into the input of the SA (SB)

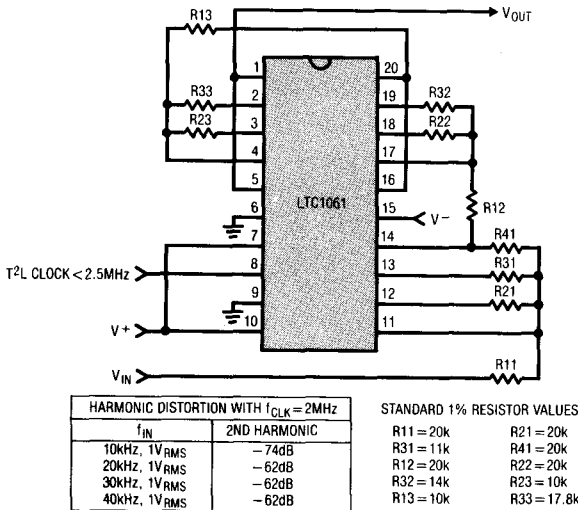


Figure 5. 6th Order Butterworth Lowpass Filter with Cutoff Frequency up to 45kHz.

switched capacitor summer. This allows the filter clock to center frequency ratio to be adjusted beyond 50:1 (or 100:1). Mode 1b still maintains the speed advantages of Mode 1. Figure 8 shows the 3 lowpass sections of the LTC1061 in cascade resulting in a Chebyshev lowpass filter. The side A of the IC is connected in Mode 1b to provide the first resonant frequency below the cutoff frequency of the filter. The practical ripple, obtained by using a non-A version of the LTC1061 and 1% standard resistor values, was 0.15dB. For this 6th order lowpass, the textbook Q's and center frequencies normalized to the ripple bandwidth are: $Q_1 = 0.55$, $f_{o1} = 0.71$, $Q_2 = 1.03$, $f_{o2} = 0.969$, $Q_3 = 3.4$, $f_{o3} = 1.17$. The design was done with speed in mind. The higher (Q_3 , f_{o3}) section was in Mode 1 and placed in the side B of the LTC1061. The remaining two center frequencies were then normalized with respect to the center frequency of side B; this changes the ratio of clock to cutoff frequency from 50:1 to $50 \times 1.17 = 58.5:1$. As shown in Figure 9, the maximum cutoff frequency is about 33kHz. The total wideband output noise is $220\mu\text{VRMS}$ and the measured output DC offset voltage is 60mV. Another example of Mode 1b is illustrated on the front page of the datasheet. The cascading sequence of this 6th order bandpass filter is shown in block diagram form, Figure 10A. The filter is geometrically centered around the

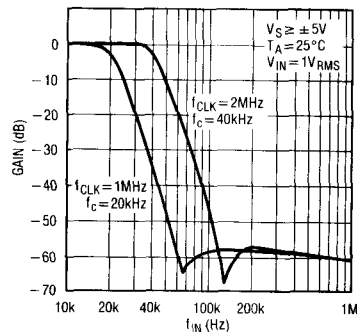
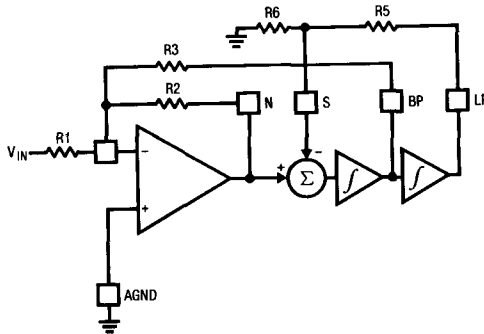


Figure 6. Measures Frequency Response of the Lowpass Butterworth Filter of Figure 3.

MODES OF OPERATION

side B of the LTC1061 connected in Mode 1. This dictates a clock to center frequency ratio of 50:1 or 100:1. The side A of the IC operates in Mode 1b to provide the lower center frequency of 0.95 and still share the same clock with the rest of the filter. With this approach the bandpass filter

can operate with center frequencies up to 24kHz. The speed of the filter could be further improved by using Mode 1 to lock the higher resonant frequency of 1.05 and higher Q of 31.9 to the clock, Figure 10B, thus changing the clock to center frequency ratio to 52.6:1.



$$f_o = \frac{f_{CLK}}{100(50)} \sqrt{\frac{R_6}{R_5 + R_6}}; f_n = f_o; Q = \frac{R_3}{R_2} \sqrt{\frac{R_6}{R_5 + R_6}}$$

$$H_{ON}(f \rightarrow 0) = H_{ON2} \left(f \rightarrow \frac{f_{CLK}}{2} \right) = -\frac{R_2}{R_1}; H_{OLP} = -\frac{R_2/R_1}{R_6/(R_5 + R_6)}; H_{OBP} = -\frac{R_3}{R_1} \cdot (R_5//R_6) < 5k\Omega$$

Figure 7. Mode 1b: 2nd Order Filter Providing Notch, Bandpass, Lowpass.

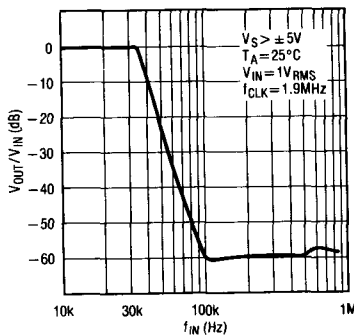
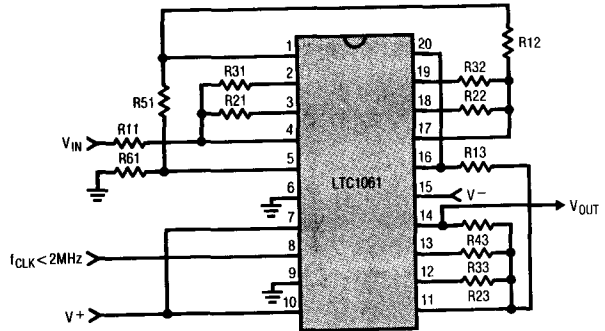


Figure 9. Amplitude Response of the 6th Order Chebyshev Lowpass Filter of Figure 8.



STANDARD 1% RESISTOR VALUES

R11 = 35.7k	R33 = 13k
R31 = 11.5k	R21 = 12.1k
R51 = 5.49k	R61 = 2.87k
R12 = 11k	R22 = 11k
R32 = 36.5k	R23 = 10.5k
R13 = 15.8k	R43 = 15.8k

Figure 8. 6th Order Chebyshev, Lowpass Filter using 3 Different Modes of Operation for Speed Optimization.

7

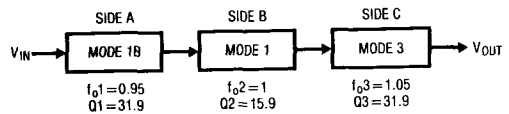


Figure 10A. Cascading Sequence of the Bandpass Filter Shown on the Front Page, with (fCLK/f0) = 50:1 or 100:1.

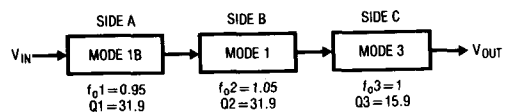
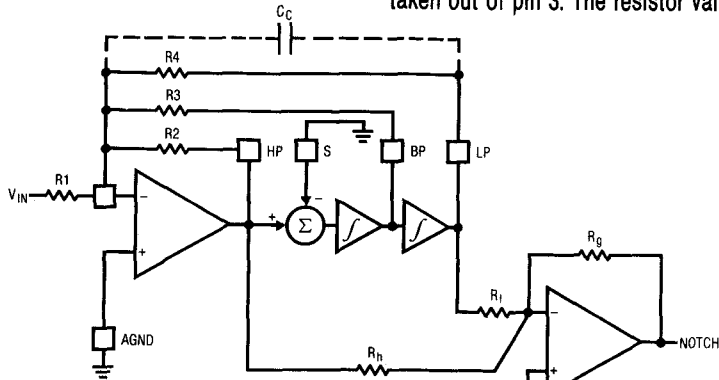


Figure 10B. Cascading Sequence of the Same Filter for Speed Optimization, and with (fCLK/f0) = 52.6:1.

MODES OF OPERATION

Mode 3a—This is an extension of Mode 3 where the highpass and lowpass outputs are summed through two external resistors R_h and R_l to create a notch, Figure 11. Mode 3a is very versatile because the notch frequency can be higher or lower than the center frequency of the 2nd order section. The external op amp of Figure 11 is not always required. When cascading the sections of the LTC1061, the highpass and lowpass outputs can be summed directly into the inverting input of the next section. Figure 12

shows an LTC1061 providing a 6th order elliptic bandpass or notch response. Sides C and B are connected in Mode 3a while side A is connected in Mode 1 and uses only two resistors. The resulting filter response is then geometrically symmetrical around either the center frequency of side A (for bandpass responses) or the notch frequency of side A (for notch responses). Figure 13 shows the measured frequency response of the circuit Figure 12 configured to provide a notch function. The filter output is taken out of pin 3. The resistor values are standard 1%.



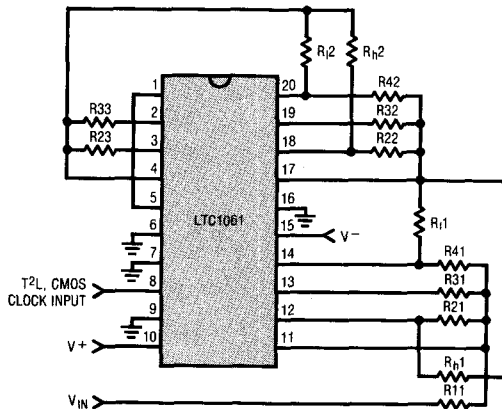
NOTE: FOR $Q > 5$ AND $f_{CLK} > 1\text{MHz}$
ADD C_C SUCH AS $C_C = 0.16 / (R_4 \times 1.2\text{MHz})$

EXTERNAL OP AMP OR
INPUT OP AMP OF THE
LTC1061, SIDE A, B, C

$$f_o = \frac{f_{CLK}}{100(50)} \sqrt{\frac{R_2}{R_4}}, f_n = \frac{f_{CLK}}{100(50)} \sqrt{\frac{R_h}{R_l}}, H_{OHP} = -R_2/R_1, H_{OBP} = -R_3/R_1, H_{OLP} = -R_4/R_1$$

$$H_{ON1}(f=0) = \frac{R_g \times R_4}{R_l}, H_{ON2}(f \rightarrow \frac{f_{CLK}}{2}) = \frac{R_g \times R_2}{R_h \times R_1}, H_{ON}(f=f_o) = 0 \left(\frac{R_g}{R_l} H_{OLP} - \frac{R_g}{R_h} H_{OH} \right), Q = \frac{R_3}{R_2} \sqrt{\frac{R_2}{R_4}}$$

Figure 11. Mode 3a: 2nd Order Filter Providing Highpass, Bandpass, Lowpass, Notch.



NOTE: FOR NOTCH RESPONSES,
PIN 7 SHOULD BE PREFERABLY
CONNECTED TO GROUND AND
THE FILTER OUTPUT IS PIN 3.
FOR BANDPASS OR LOWPASS
RESPONSES PIN 7 CAN BE EITHER
AT GROUND OR POSITIVE SUPPLY,
AND THE FILTER OUTPUT IS PIN 2
OR PIN 1.

Figure 12. 6th Order Elliptic Bandpass, Lowpass or Notch Topology.

MODES OF OPERATION

The ratio of the 0dB width, BW1, to the notch width BW2, is 5:1 and matches the theoretical design value. The measured notch depth was -53dB versus -56dB theoretical and the clock to center notch frequency ratio is 100:1.

Figure 14 shows the measured frequency response of the circuit topology, Figure 12, but with pole/zero locations configured to provide a high Q, 6th order elliptic bandpass filter operating with a clock to center frequency ratio of 50:1 or 100:1. The theoretical passband ripple, stopband attenuation and stopband to ripple bandwidth ratio are 0.5dB, 56dB, 5:1 respectively. The obtained results with 1% standard resistor values closely match the theoretical center frequencies, Q's, and notch frequencies are ($f_{o1} = 0.969$, $Q1 = 54.3$, $f_{n1} = 0.84$, $f_{o2} = 1.031$, $Q2 = 54.3$,

$f_{n2} = 1.187$, $f_{o3} = 1$, $Q3 = 26.2$). The output of the filter is the BP output of Side A, Pin 2.

Lowpass filters with stopband notches can also be realized by using Figure 12 provided that 6th order lowpass filter approximations with 2 stopband notches can be synthesized. Literature describing elliptic double terminated (RLC) passive ladder filters provide enough data to synthesize the above filters. The measured amplitude response of such a lowpass is shown in Figure 15 where the filter output is taken out of side A's Pin 1, Figure 12. The clock to center frequency ratio can be either 50:1 or 100:1 because the last stage of the LTC1061 operates in Mode 1 with a center frequency very close to the overall cutoff frequency of the lowpass filter.

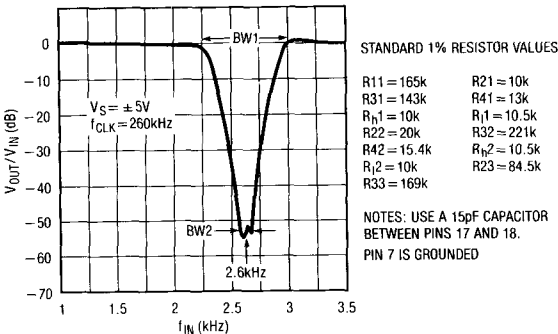


Figure 13. Resistor Values and Amplitude Response of Figure 12 Topology. The Notch is Centered at 2600Hz.

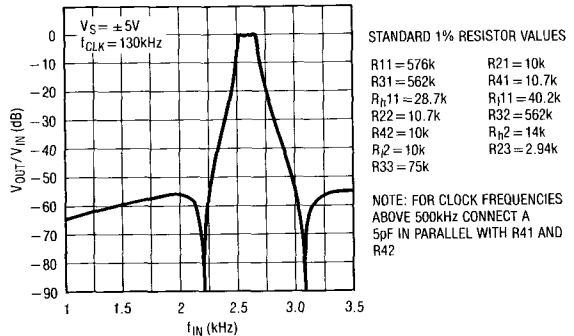


Figure 14. Resistor Values and Amplitude Response of Figure 12 Topology. The Bandpass Filter is Centered Around 2600Hz when Operating with a 130kHz Clock.

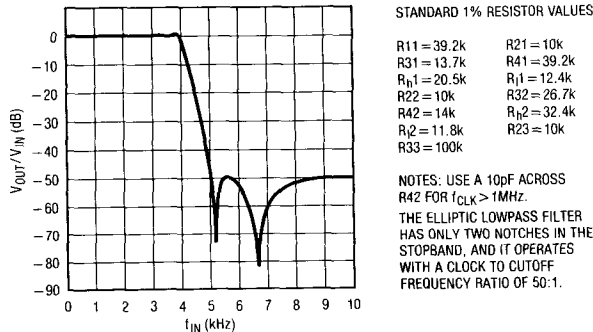


Figure 15. Resistor Values and Amplitude Response of the Topology of Figure 12.

MODES OF OPERATION

In Figure 16, all three sides of the LTC1061 are connected in Mode 3a. This topology is useful for elliptic highpass and notch filters with clock to cutoff (or notch) frequency ratio higher than 100:1. This is often required to extend the allowed input signal frequency range and to avoid premature aliasing. Figure 16 is also a versatile, general purpose architecture providing 3 notches and 3 pole pairs, and there is no restriction on the location of the poles with respect to the notch frequencies. The drawbacks, when

compared to Figure 12, are the use of an external op amp and the increased number of the required external resistors. Figure 17 shows the measured frequency of a 6th order highpass elliptic filter operating with 250:1 clock to cutoff frequency ratio. With a 1MHz clock, for instance, the filter yields a 4kHz cutoff frequency, thus allowing an input frequency range beyond 100kHz. Band limiting can be easily added by placing a capacitor across the feedback resistor of the external op amp of Figure 16.

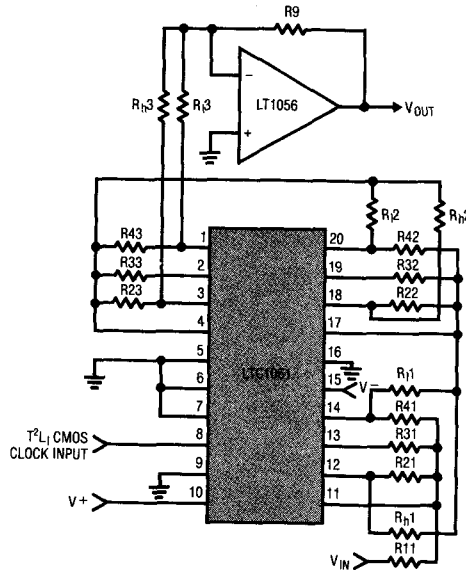


Figure 16. Using an External Op Amp to Connect all 3 Sides of the LTC1061 in Mode 3a.

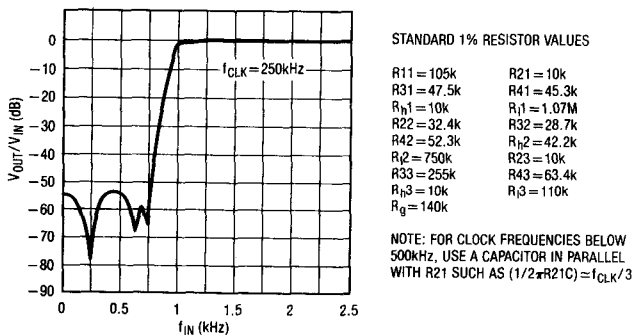


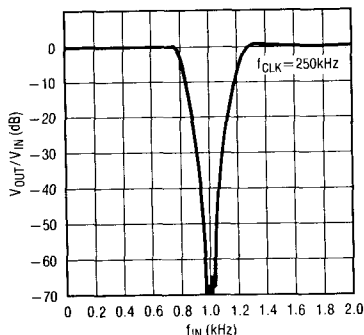
Figure 17. Measured Amplitude Response of the Topology of Figure 16, Configured to Provide a 6th Order Elliptic Highpass Filter Operating with a Clock to Cutoff Frequency Ratio of 250:1.

MODES OF OPERATION

Figure 18 shows the plotted amplitude responses of a 6th order notch filter operating again with a clock to center notch frequency ratio of 250:1. The theoretical notch depth is 70dB and when the notch is centered at 1kHz its width is 50Hz. Two small, noncritical capacitors were used across the R21 and R22 resistors of Figure 16, to bandlimit the first two highpass outputs such that the practical notch depth will approach the theoretical value. With these two fixed capacitors, the notch frequency can be swept within a 3:1 range.

When the circuit of Figure 16 is used to realize lowpass elliptic filters, a capacitor across R_g raises the order of the filter and at the same time eliminates any small clock

feedthrough. This is shown in Figure 19 where the amplitude response of the filter is plotted for 3 different cutoff frequencies. When the clock frequency equals or exceeds 1MHz, the stopband notches lose their depth due to the finite bandwidth of the internal op amps and to the small crosstalk between the different sides of the LTC1061. The lowpass filter, however, does not lose its passband accuracy and it maintains nearly all of its attenuation slope. The theoretical performance of the 7th order lowpass filter of Figure 19 is 0.2dB passband ripple, 1.5:1 stopband to cutoff frequency ratio, and 73dB stopband attenuation. Without any tuning, the obtained results closely approximate the textbook response.

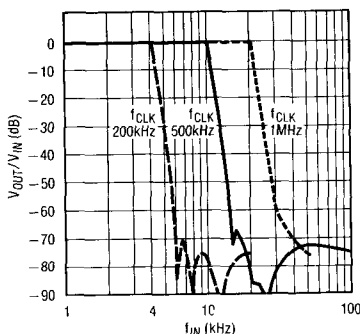


STANDARD 1% RESISTOR VALUES

R11 = 84.5k	R21 = 10.2k
R31 = 31.6k	R41 = 63.4k
R _h 1 = 48.7k	R _h 1 = 287k
R22 = 10k	R32 = 232k
R42 = 97.6k	R _h 2 = 10.2k
R _p 2 = 66.5k	R23 = 20k
R33 = 300k	R43 = 80.6k
R _h 3 = 10.2k	R _p 3 = 63.4k
R _g = 210k	

NOTE: CONNECT 39pF AND 100pF ACROSS R21 AND R22 RESPECTIVELY.

Figure 18. 6th Order Band Reject Filter Operating with a Clock to Center Notch Frequency Ratio of 250:1. The Ratio of 0dB to the -65dB Notch Width is 8:1.



STANDARD 1% RESISTOR VALUES

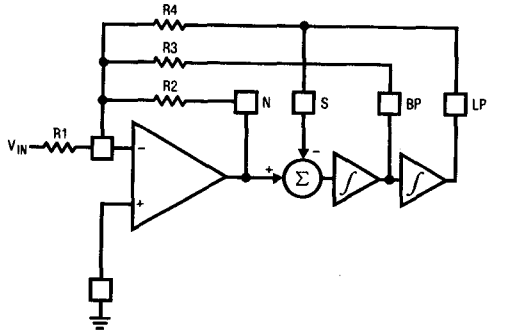
R11 = 30.9k	R21 = 10k
R31 = 16.2k	R41 = 26.7k
R _h 1 = 45.3k	R _h 1 = 19.6k
R22 = 10.5k	R32 = 100k
R42 = 10k	R _h 2 = 52.3k
R _p 2 = 15.8k	R23 = 10k
R33 = 28.7k	R43 = 12.7k
R _h 3 = 95.3k	R _p 3 = 10k
R _g = 28k	

NOTE: ADD A CAPACITOR C ACROSS R_g TO CREATE A 7TH ORDER LOWPASS SUCH AS $(1/2\pi R_g C) = (\text{CUTOFF FREQUENCY}) \times 0.38$

Figure 19. Frequency Responses of a 7th Order Lowpass Elliptic Filter Realized with Figure 16 Topology.

MODES OF OPERATION

Mode 2—This is a combination of Mode 1 and Mode 3, Figure 20. With Mode 2, the clock to center frequency ratio, f_{CLK}/f_o , is always less than 50:1 or 100:1. When compared to Mode 3 and for applications requiring 2nd order sections with f_{CLK}/f_o slightly less than 100 or 50:1, Mode 2 provides less sensitivity to resistor tolerances. As in Mode 1, Mode 2 has a notch output which directly depends on the clock frequency and therefore the notch frequency is always less than the center frequency, f_o , of the 2nd order section. Figure 21 shows the side A of the LTC1061 connected in Mode 2 while sides B and C are in Mode 3a. This topology can be used to synthesize elliptic bandpass, highpass and notch filters. The elliptic highpass of



$$f_o = \frac{f_{CLK}}{100(50)} \sqrt{1 + \frac{R_2}{R_4}}; f_n = \frac{f_{CLK}}{100(50)}; Q = \frac{R_3}{R_2} \sqrt{1 + \frac{R_2}{R_4}}; H_{OLP} = \frac{-R_2/R_1}{1 + (R_2/R_4)}$$

$$H_{OBP} = -R_3/R_1; H_{ON}(f \rightarrow 0) = \frac{-R_2/R_1}{1 + (R_2/R_4)}; H_{ON2} \left(f = \frac{f_{CLK}}{2} \right) = -R_2/R_1$$

Figure 20. Mode 2: 2nd Order Filter Providing Notch, Bandpass, Lowpass.

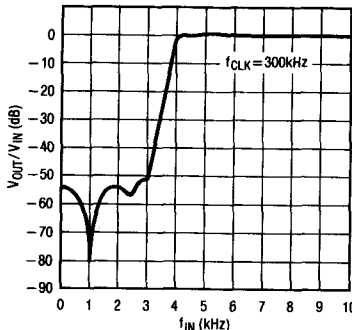


Figure 22. 6th Order Elliptic Highpass Filter Operating with a Clock to Cutoff Frequency Ratio of 75:1, and Using the Topology of Figure 21.

Figure 17 is synthesized again, Figure 22, but the clock is now locked onto the higher frequency notch provided by the side A of the LTC1061. As shown in Figure 22, the highpass corner frequency is 3.93kHz and the higher notch frequency is 3kHz while the filter operates with a 300kHz clock. The center frequencies, Q's, and notches of Figure 22, when normalized to the highpass cutoff frequency, are ($f_{o1} = 1.17$, $Q_1 = 2.24$, $f_{n1} = 0.242$, $f_{o2} = 1.96$, $Q_2 = 0.7$, $f_{n2} = 0.6$, $f_{o3} = 0.987$, $f_{n3} = 0.753$, $Q = 10$). When compared with the topology of Figure 16, this approach uses lower and more restricted clock frequencies. The obtained notch in Mode 2 is shallower; however, this topology is more efficient.

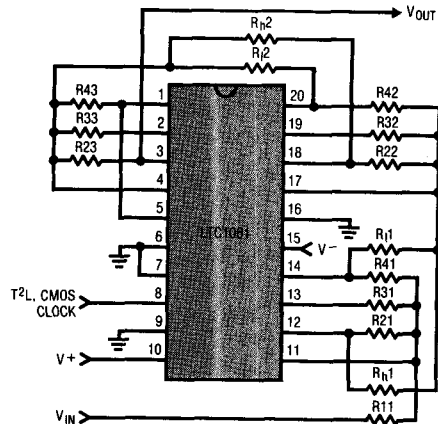


Figure 21. LTC1061 with Side A is Connected in Mode 2 while Sides B, C are in Mode 3a. Topology is Useful for Elliptic Highpass, Notch and Bandpass Filters.

STANDARD 1% RESISTOR VALUES

R11 = 54.9k	R21 = 24.3k
R31 = 34.8k	R41 = 10k
R _{n1} = 28.7k	R _{n1} = 280k
R22 = 68.1k	R32 = 18.2k
R42 = 10k	R _{n2} = 10.2k
R _{n2} = 16.2k	R23 = 10k
R33 = 75k	R43 = 14k

NOTE: FOR CLOCK FREQUENCIES ABOVE 300kHz ADD A CAPACITOR, C, ACROSS R21 AND R22 SUCH AS $(1/2 * R21C) = f_{CLK}$

MODES OF OPERATION

Output Noise

The wideband RMS noise of the LTC1061 outputs is nearly independent from the clock frequency. The LTC1061 noise when operating with $\pm 2.5V$ supply is lower, as Table 3 indicates. The noise at the bandpass and lowpass outputs increases roughly as the \sqrt{Q} . Also the noise increases when the clock to center frequency ratio is altered with external resistors to exceed the internally set 100:1 or 50:1 ratios. Under this condition, the noise increases square root-wise.

Output Offsets

The equivalent input offsets of the LTC1061 are shown in Figure 23. The DC offset at the filter bandpass output is al-

ways equal to V_{OS3} . The DC offsets at the remaining two outputs (Notch and LP) depend on the mode of operation and external resistor ratios. Table 4 illustrates this.

It is important to know the value of the DC output offsets, especially when the filter handles input signals with large dynamic range. As a rule of thumb, the output DC offsets increase when:

1. The Q's decrease
2. The ratio (f_{CLK}/f_o) increases beyond 100:1. This is done by decreasing either the (R2/R4) or the R6/(R5 + R6) resistor ratios.

Table 3. Wideband RMS Noise

V_s	$\frac{f_{CLK}}{f_o}$	Notch/HP (μV_{RMS})	BP (μV_{RMS})	LP (μV_{RMS})	CONDITIONS
$\pm 5V$	50:1	45	55	70	Mode 1, R1 = R2 = R3 Q = 1
$\pm 5V$	100:1	65	65	85	
$\pm 2.5V$	50:1	30	30	45	
$\pm 2.5V$	100:1	40	40	60	
$\pm 5V$	50:1	18	150	150	Mode 1, Q = 10 R1 = R3 for BP out R1 = R2 for LP out
$\pm 5V$	100:1	20	200	200	
$\pm 2.5V$	50:1	15	100	100	
$\pm 2.5V$	100:1	17	140	140	
$\pm 5V$	50:1	57	57	62	Mode 3, R1 = R2 = R3 = R4 Q = 1
$\pm 5V$	100:1	72	72	80	
$\pm 2.5V$	50:1	40	40	42	
$\pm 2.5V$	100:1	50	50	53	
$\pm 5V$	50:1	135	120	140	Mode 3, R2 = R4, Q = 10 R3 = R1 for BP out R4 = R1 for LP and HP out
$\pm 5V$	100:1	170	160	185	
$\pm 2.5V$	50:1	100	88	100	
$\pm 2.5V$	100:1	125	115	130	

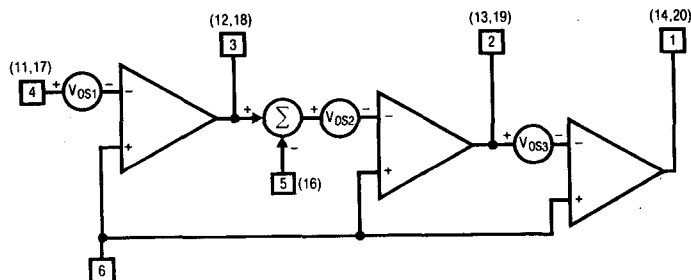


Figure 23. Equivalent Input Offsets of 1/3 LTC1061 Filter Building Block.

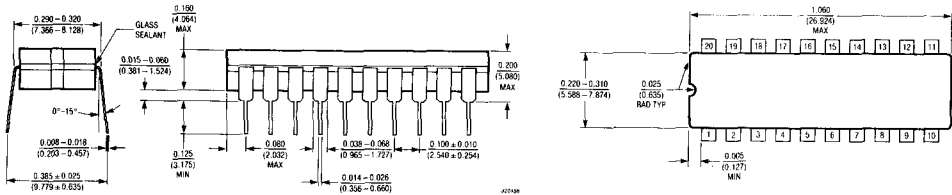
MODES OF OPERATION

Table 4

Mode	V_{OSN} Pin 3 (18)	V_{OSBP} Pin 2 (19)	V_{OSLP} Pin 1 (20)
1	$V_{OS1}[(1/Q) + 1 + I_{HOLP}] - V_{OS3}/Q$	V_{OS3}	$V_{OSN} - V_{OS2}$
1b	$V_{OS1}[(1/Q) + 1 + R2/R1] - V_{OS3}/Q$	V_{OS3}	$-(V_{OSN} - V_{OS2})(1 + R5/R6)$
2	$[V_{OS1}(1 + R2/R1 + R2/R3 + R2/R4) - V_{OS3}(R2/R3)] \times$ $\times [R4/(R2 + R4)] + V_{OS2}[R2/(R2 + R4)]$	V_{OS3}	$V_{OSN} - V_{OS2}$
3	V_{OS2}	V_{OS3}	$V_{OS1} \left[1 + \frac{R4}{R1} + \frac{R4}{R2} + \frac{R4}{R3} \right] - V_{OS2} \left(\frac{R4}{R2} \right)$ $- V_{OS3} \left(\frac{R4}{R3} \right)$

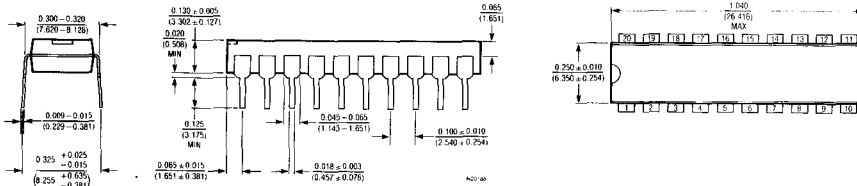
PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

J20 Package Ceramic DIP



T_{jmax} 125°C	θ_{ja} 100°C/W
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N20 Package Molded DIP



T_{jmax} 100°C	θ_{ja} 100°C/W
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High Performance Triple Universal Filter Building Block

FEATURES

- Up to 6th Order Filter Functions with a Single 20 Pin Surface Mount Package
- Center Frequency Range up to 35kHz
- $f_0 \times Q$ Product Up to 1 MHz
- *Guaranteed* Center Frequency and Q Accuracy Over Temperature
- *Guaranteed* Low Offset Voltages Over Temperature
- 90dB Dynamic Range
- Filter Operates From Single 4.7V Supply and Up to $\pm 8V$ Supplies
- Low Power
- Clock Inputs T²L and CMOS Compatible

APPLICATIONS

- High Order, Wide Frequency Range Bandpass, Lowpass, Notch Filters
- Low Power Consumption, Single 5V Supply Clock Tunable Filters
- Tracking Filters

DESCRIPTION

The LTC1061 consists of three high performance, universal filter building blocks. Each filter building block together with an external clock and 2 to 5 resistors can produce various second order functions which are available at its three output pins. Two out of three always provide lowpass and bandpass functions while the third output pin can produce highpass or notch or allpass. The center frequency of these functions can be tuned from 0.1Hz to 35kHz and is dependent on an external clock or an external clock and a resistor ratio.

The LTC1061 can be used with single or dual supplies ranging from $\pm 2.37V$ to $\pm 8V$ (or 4.74V to 16V). When the filter operates with supplies of $\pm 5V$ and above, it can handle input frequencies up to 100kHz.

The LTC1061 is compatible with the LTC1059 single universal filter and the LTC1060 dual. Higher than 6th order functions can be obtained by cascading the LTC1061 with the LTC1059 or LTC1060. Any classical filter realization (such as Butterworth, Cauer, Bessel and Chebyshev) can be obtained by the appropriate choice of the external resistors.

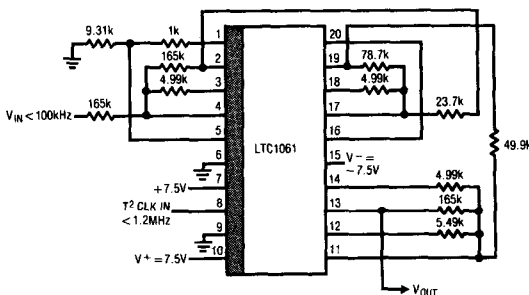
The LTC1061 is manufactured by using Linear Technology's enhanced LTCMOS™ silicon gate process.

LTCMOS™ is a trademark of Linear Technology Corp.

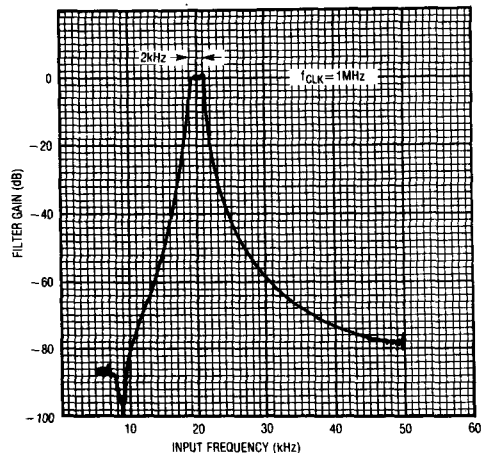
7

TYPICAL APPLICATION

6th Order, Clock Tunable, 0.5dB Ripple Chebyshev BP Filter



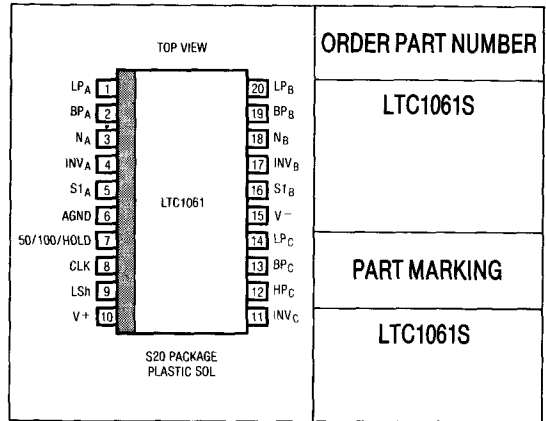
Amplitude Response



ABSOLUTE MAXIMUM RATINGS

Supply Voltage 18V
 Operating Temperature Range $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$
 Storage Temperature Range..... -65°C to 150°C
 Lead Temperature (Soldering, 10sec)..... 300°C

PACKAGE/ORDER INFORMATION



ELECTRICAL CHARACTERISTICS

(Complete Filter) $V_S = \pm 5V$, $T_A = 25^{\circ}\text{C}$, T^2L clock input level, unless otherwise specified

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Center Frequency Range, f_0	$f_0 \times Q \leq 175\text{kHz}$, Mode 1, $V_S = \pm 7.5V$ $f_0 \times Q \leq 1.6\text{MHz}$, Mode 1, $V_S = \pm 7.5V$ $f_0 \times Q \leq 75\text{kHz}$, Mode 3, $V_S = \pm 7.5V$ $f_0 \times Q \leq 1\text{MHz}$, Mode 3, $V_S = \pm 7.5V$ (Note 1)		0.1-35k 0.1-25k 0.1-25k 0.1-17k		Hz Hz Hz Hz
Input Frequency Range			0-200k		Hz
Clock to Center Frequency Ratio, f_{CLK}/f_0 (Note 1)	Sides A, B: Mode 1, $R1 = R3 = 50k\Omega$ $R2 = 5k\Omega$, $Q = 10$, $f_{CLK} = 250\text{kHz}$ Pin 7 High. Side C: Mode 3, $R1 = R3 = 50k$ $R2 = R4 = 5k$, $f_{CLK} = 250\text{kHz}$ Same as Above but Pin 7 at Mid-Supplies, $f_{CLK} = 500\text{kHz}$	●		$50 \pm 1.2\%$	
Clock to Center Frequency Ratio, Side to Side Matching		●		$100 \pm 1.2\%$ 1.2%	
Q Accuracy (Note 1)	Sides A, B, Mode 1 $\left\{ \begin{array}{l} 50:1 \text{ or } 100:1 \\ \text{Side C, Mode 3 } \end{array} \right. f_0 = 5\text{kHz}, Q = 10$	●	± 3	5	%
f_0 Temperature Coefficient	Mode 1, 50:1, $f_{CLK} < 300\text{kHz}$		± 1		ppm/ $^{\circ}\text{C}$
Q Temperature Coefficient	Mode 1, 100:1, $f_{CLK} < 500\text{kHz}$ Mode 3, $f_{CLK} < 500\text{kHz}$		± 5 ± 5		ppm/ $^{\circ}\text{C}$ ppm/ $^{\circ}\text{C}$

ELECTRICAL CHARACTERISTICS(Complete Filter) $V_S = \pm 5V$, $T_A = 25^\circ C$, T^2L clock input level, unless otherwise specified

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
DC Offset Voltage (Note 2)					
V_{os1}	$f_{CLK} = 250kHz, 50:1$ $f_{CLK} = 500kHz, 100:1$ $f_{CLK} = 250kHz, 50:1$ $f_{CLK} = 500kHz, 100:1$	●	2	15	mV
V_{os2}		●	3	25	mV
V_{os3}		●	6	50	mV
V_{oss}		●	3	25	mV
V_{oss}		●	6	50	mV
Clock Feedthrough	$f_{CLK} < 1MHz$		0.4		mV _{RMS}
Max. Clock Frequency	Mode 1, $Q < 5$, $V_S \geq \pm 5V$		2.5		MHz
Power Supply Current		6	8	12	mA
				16	mA

ELECTRICAL CHARACTERISTICS (Complete Filter) $V_S = \pm 2.37V$, $T_A = 25^\circ C$ unless otherwise specified

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Center Frequency Range, f_o	$f_o \times Q \leq 120kHz$, Mode 1, 50:1 $f_o \times Q \leq 120kHz$, Mode 3, 50:1		0.1–12k 0.1–10k		Hz
Input Frequency Range			0–20k		Hz
Clock to Center Frequency Ratio	50:1, $f_{CLK} = 250kHz$, $Q = 10$ Sides A, B: Mode 1 Side C: Mode 3 100:1, $f_{CLK} = 500kHz$, $Q = 10$ Sides A, B: Mode 1 Side C: Mode 3		50 \pm 1% 100 \pm 1%		
Q Accuracy	Same as Above, 100:1 or 50:1		± 3		%
Max. Clock Frequency			700k		Hz
Power Supply Current			4.5	6	mA

7

ELECTRICAL CHARACTERISTICS (Internal Op Amps) $T_A = 25^\circ C$ unless otherwise specified

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage Range		± 2.37		± 9	V
Voltage Swings	$V_S = \pm 5V$, $R_L = 5k$ (Pins 1, 2, 13, 14, 19, 20) $R_L = 3.5k$ (Pins 3, 12, 18)	± 3.8 ± 3.6	± 4.2		V
Output Short Circuit Current Source/Sink	$V_S = \pm 5V$		40/3		mA
DC Open Loop Gain	$V_S = \pm 5V$, $R_L = 5k$		80		dB
GBW Product	$V_S = \pm 5V$		3		MHz
Slew Rate	$V_S = \pm 5V$		7		V/ μs

The ● denotes the specifications which apply over the full operating temperature range.

Note 2: For definition of the DC offset voltages refer to the LTC1061 data sheet. An LTC1061S with improved DC offset specifications can be made available upon special request.

Note 1: An LTC1061S with improved Q and clock to center frequency ratio accuracy can be made available upon special request.

NOTES

FEATURES

- Lowpass Filter with No DC Error
- Low Passband Noise
- Operates DC to 20kHz
- Operates on a Single 5V Supply or Up to $\pm 8V$
- 5th Order Filter
- Maximally Flat Response
- Internal or External Clock
- Cascadable for Faster Roll-off
- Buffer Available
- 8 Pin DIP Package

APPLICATIONS

- 60Hz Lowpass Filters
- Anti-Aliasing Filter
- Low Level Filtering
- Rolling Off AC Signals from High DC Voltages
- Digital Voltmeters
- Scales
- Strain Gauges

DESCRIPTION

The LTC1062 is a 5th order all pole maximally flat lowpass filter with no DC error. Its unusual architecture puts the filter outside the DC path so DC offset and low frequency noise problems are eliminated. This makes the LTC1062 very useful for lowpass filters where DC accuracy is important.

The filter input and output are simultaneously taken across an external resistor. The LTC1062 is coupled to the signal through an external capacitor. This R,C reacts with the internal switched capacitor network to form a 5th order rolloff at the output.

The filter cutoff frequency is set by an internal clock which can be externally driven. The clock to cutoff frequency ratio is typically 100, allowing the clock ripple to be easily removed.

Two LTC1062s can be cascaded to form a 10th order quasi max flat lowpass filter. The device can be operated with single or dual supplies ranging from $\pm 2.5V$ to $\pm 9V$.

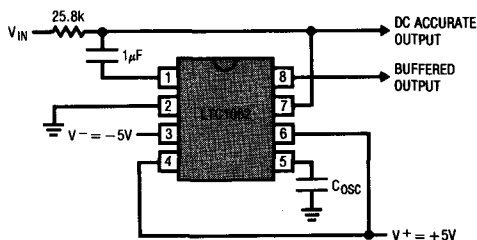
The LTC1062 is manufactured using Linear Technology's enhanced LTCMOS™ silicon gate process.

LTCMOS™ is a trademark of Linear Technology Corp.

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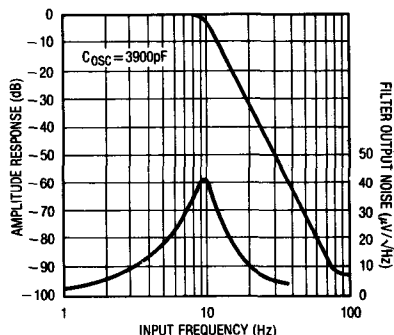
TYPICAL APPLICATION

10Hz 5th Order Butterworth Lowpass Filter



NOTE: TO ADJUST OSCILLATOR FREQUENCY, USE A 6800pF CAPACITOR IN SERIES WITH A 50K POT FROM PIN 5 TO GROUND.

Filter Amplitude Response and Noise



ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V^+ to V^-)	18V
Input Voltage at Any Pin	$V^- - 0.3V \leq V_{IN} \leq V^+ + 0.3V$
Operating Temperature Range	
LTC1062M	$-55^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$
LTC1062C	$-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$
Storage Temperature Range	-65°C to 150°C
Lead Temperature Range (Soldering, 10 sec.)	300°C

PACKAGE/ORDER INFORMATION

	ORDER PART NUMBER
	LTC1062MJ8 LTC1062CJ8 LTC1062CN8

ELECTRICAL CHARACTERISTICS

Test Conditions: $V^+ = +5V$, $V^- = -5V$, $T_A = 25^\circ\text{C}$ unless otherwise specified, AC output measured at pin 7, Figure 1

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply Current	C_{OSC} (Pin 5 to V^-) = 100 pF	●	4.5	7 10	mA mA
Input Frequency Range			0–20k		Hz
Filter Gain at $f_{IN} = 0$	$f_{CLK} = 100\text{kHz}$, Pin 4 at V^+ $C = 0.01\mu\text{F}$, $R = 25.78\text{k}$		0		dB
$f_{IN} = 0.5f_C$ (Note 1)		●	-0.02	-0.3	dB
$f_{IN} = f_C$		●	-3		dB
$f_{IN} = 2f_C$		●	-28	-30	dB
$f_{IN} = 4f_C$		●	-54	-60	dB
Clock to Cutoff Frequency Ratio, f_{CLK}/f_C	Same as above		100 ± 1		%
Filter Gain at $f_{IN} = 16\text{kHz}$	$f_{CLK} = 400\text{kHz}$, Pin 4 at V^+ $C = 0.01\mu\text{F}$, $R = 6.5\text{k}$	●	-45	-52	dB
f_{CLK}/f_C Tempco	Same as above		10		ppm/ $^\circ\text{C}$
Filter Output (Pin 7) DC Swing	Pin 7 buffered with an external op amp	●	± 3.5	± 3.8	V
Clock Feedthrough			1		mVp-p
Internal Buffer					
Bias Current			2	50	pA
Offset Voltage		●	170	1000	pA
Offset Voltage			2	20	mV
Voltage Swing	$R_{LOAD} = 20\text{k}\Omega$	●	± 3.5	± 3.8	V
Short Circuit Current Source/Sink			40/3		mA
Clock (Note 3)					
Internal Oscillator Frequency	C_{OSC} (Pin 5 to V^-) = 100pF C_{OSC} (Pin 5 to V^-) = 100pF	●	25 15	32 65	kHz kHz
Max Clock Frequency			4		MHz
Pin 5 Source or Sink Current		●	40	80	μA

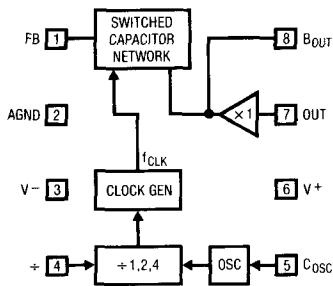
The ● denotes the specifications which apply over the full operating temperature range.

Note 1: f_C is the frequency where the gain is -3dB with respect to the input signal.

Note 2: The LTC1062M operates from $-55^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$, the LTC1062C operates from $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$.

Note 3: The external or driven clock frequency is divided by either 1, 2, or 4 depending upon the voltage at pin 4. When pin 4 = V^+ , ratio = 1; when pin 4 = GND, ratio = 2; when pin 4 = V^- , ratio = 4.

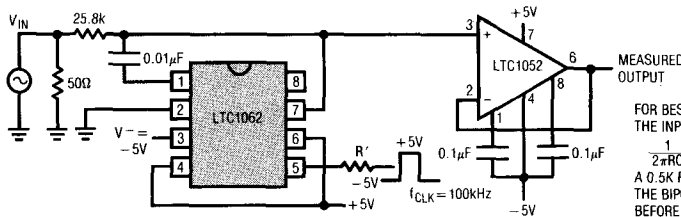
BLOCK DIAGRAM



BY CONNECTING PIN 4 TO V^+ , AGND, OR V^- , THE OUTPUT FREQUENCY OF THE INTERNAL CLOCK GENERATOR IS THE OSCILLATOR FREQUENCY DIVIDED BY 1.24. THE (f_{CLK}/f_C) RATIO OF 100:1 IS WITH RESPECT TO THE INTERNAL CLOCK GENERATOR OUTPUT FREQUENCY. PIN 5 CAN BE DRIVEN WITH AN EXTERNAL CMOS LEVEL CLOCK. THE LTC1062 CAN ALSO BE SELF-CLOCKED BY CONNECTING AN EXTERNAL CAPACITOR (C_{OSC}) TO GROUND (OR TO V^- IF C_{OSC} IS POLARIZED). UNDER THIS CONDITION AND WITH $\pm 5V$ SUPPLIES, THE INTERNAL OSCILLATOR FREQUENCY IS:

$$f_{OSC} = 140kHz [33pF / (33pF + C_{OSC})]$$

For Adjusting Oscillator Frequency, Insert a 50K Pot in Series with C_{OSC} . Use Two Times Calculated C_{OSC} .



FOR BEST MAX. FLAT APPROXIMATION, THE INPUT R, C SHOULD BE SUCH AS:

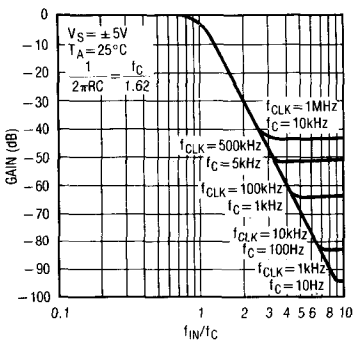
$$\frac{1}{2\pi RC} = \frac{f_{CLK}}{100} \times 1.63$$

A 0.5K RESISTOR, R' , SHOULD BE USED IF THE BIPOLAR EXTERNAL CLOCK IS APPLIED BEFORE THE POWER SUPPLIES TURN ON.

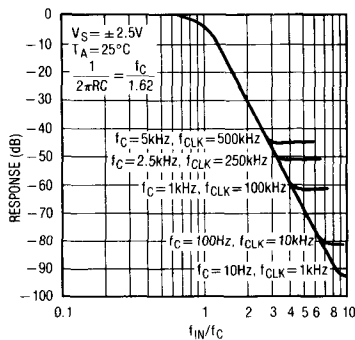
Figure 1. AC Test Circuit

TYPICAL PERFORMANCE CHARACTERISTICS

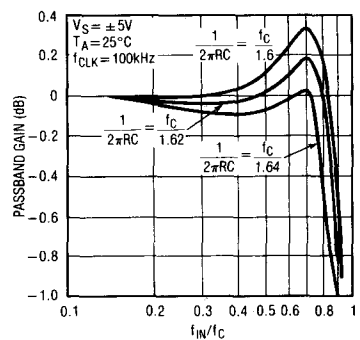
Amplitude Response Normalized to the Cutoff Frequency



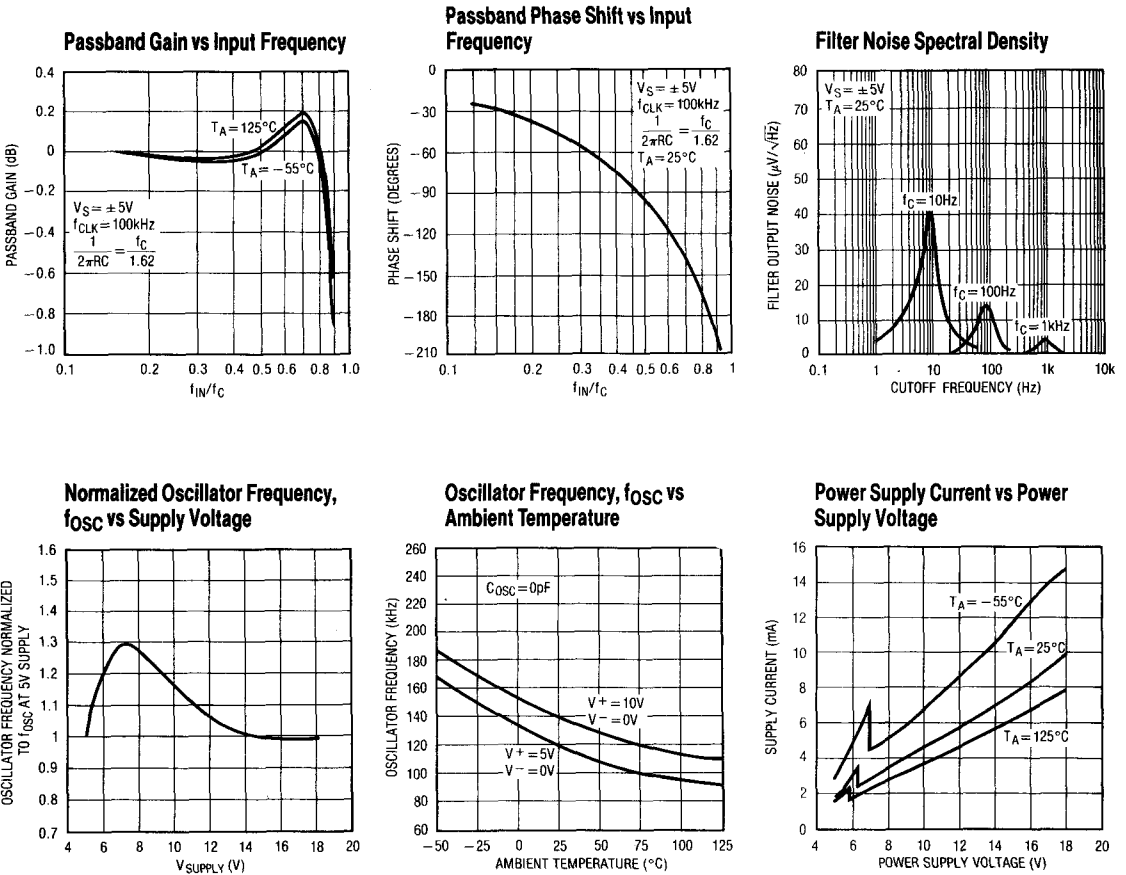
Amplitude Response Normalized to the Cutoff Frequency



Passband Gain vs Input Frequency



TYPICAL PERFORMANCE CHARACTERISTICS



APPLICATIONS INFORMATION

Filter Input Voltage Range

Every node of the LTC1062 typically swings within 1V of either voltage supply, positive or negative. With the appropriate external (R,C) values, the amplitude response of all the internal or external nodes does not exceed a gain of 0 dB with the exception of pin 1. The amplitude response of the feedback node (pin 1) is shown in Figure 2. For an input frequency around $0.8 \times f_C$, the gain is 1.7 V/V and, with

$\pm 5\text{V}$ supplies, the peak-to-peak input voltage should not exceed 4.7V. If the input voltage goes beyond this value, clipping and distortion of the output waveform occur, but the filter will not get damaged nor will it oscillate. Also, the absolute maximum input voltage should not exceed the power supplies.

APPLICATIONS INFORMATION

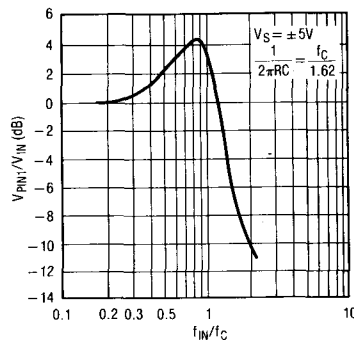


Figure 2. Amplitude Response of Pin 1

Internal Buffer

The internal buffer out (pin 8) and pin 1 are part of the signal AC path. Excessive capacitive loading will cause gain errors in the passband, especially around the cutoff frequency. The internal buffer gain at DC is typically 0.006dB. The internal buffer output can be used as a filter output, however it has a few millivolts of DC offset. The temperature coefficient of the internal buffer is typically $1\mu\text{V}/^\circ\text{C}$.

Filter Attenuation

The LTC1062 rolloff is typically 30dB/octave. When the clock, and the cutoff frequencies increase, the filter's maximum attenuation decreases. This is shown in the Typical Performance Characteristics. The decrease of the maximum attenuation, is due to the roll off at higher frequencies of the loop gains of the various internal feedback paths and not to the increase of the noise floor. For instance, for a 100kHz clock and 1kHz cutoff frequency, the maximum attenuation is about 64dB. A 4kHz, 1Vrms input signal will be predictably attenuated by 60dB at the output. A 6kHz, 1Vrms input signal will be attenuated by 64dB and not by 77dB as an ideal 5th order maximum flat filter would have dictated. The LTC1062 output at 6kHz will be about $630\mu\text{Vrms}$. The measured rms noise from DC to 17kHz was $100\mu\text{Vrms}$ which is 16dB below the filter output.

COSC, Pin 5

The C_{OSC} , pin 5, can be used with an external capacitor, C_{OSC} , connected from pin 5 to ground. If C_{OSC} is polarized it should be connected from pin 5 to the negative supply, pin 3. C_{OSC} lowers the internal oscillator frequency. If pin 5 is floating, an internal 33pF capacitor plus the external interpin capacitance set the oscillator frequency around 140kHz with $\pm 5\text{V}$ supply. An external C_{OSC} will bring the oscillator frequency down by the ratio $(33\text{pF})/(33\text{pF} + C_{OSC})$. The typical performance characteristics curves provide the necessary information to get the internal oscillator frequency for various power supply ranges. Pin 5 can also be driven with an external CMOS clock to override the internal oscillator. Although standard 7400 series CMOS gates do not guarantee CMOS levels with the current source and sink requirements of pin 5, they will, in reality, drive the C_{OSC} pin. CMOS gates conforming to standard B series output drive have the appropriate voltage levels and more than enough output current to simultaneously drive several LTC1062 C_{OSC} pins. The typical trip levels of the internal Schmitt trigger which input is pin 5, are given below.

V SUPPLY	V_{th+}	V_{th-}
$\pm 2.5\text{V}$	+ 0.9V	- 1V
$\pm 5\text{V}$	+ 1.3V	- 2.1V
$\pm 6\text{V}$	+ 1.7V	- 2.5V
$\pm 7\text{V}$	+ 1.75V	- 2.9V

APPLICATIONS INFORMATION

Divide By 1, 2, 4 (Pin 4)

By connecting pin 4 to V^+ , to mid supplies or to V^- , the clock frequency driving the internal switched capacitor network is the oscillator frequency divided by 1, 2, 4, respectively. Note that the f_{CLK}/f_C ratio of 100:1 is with respect to the internal clock generator output frequency. The internal divider is useful for applications where octave tuning is required. The ± 2 threshold is typically $\pm 1V$ from the mid supply voltage.

Transient Response

Figure 3 shows the LTC1062 response to a 1V input step.

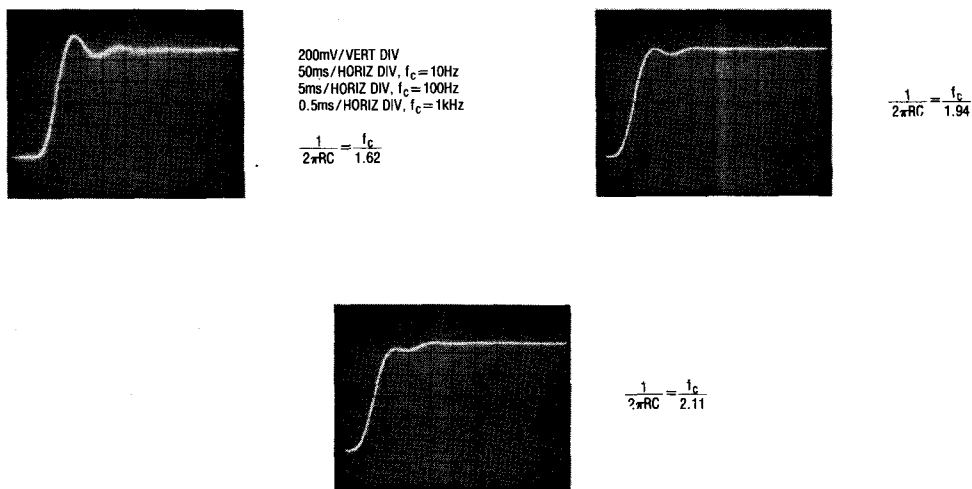


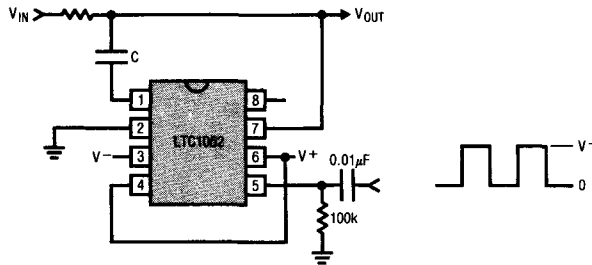
Figure 3. Step Response to a 1V Peak Input Step

Table 1

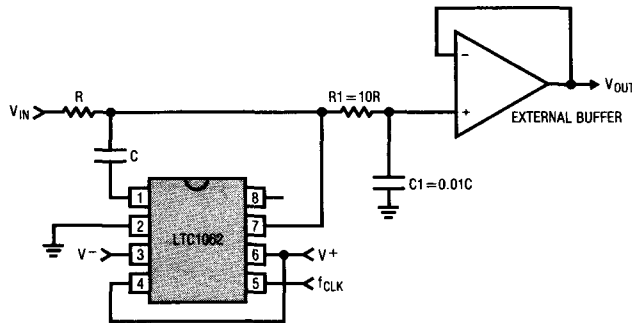
NOISE BW	rms NOISE $V_S = \pm 5V$
DC - $0.1 \times f_C$	2 μ V
DC - $0.25 \times f_C$	8 μ V
DC - $0.5 \times f_C$	20 μ V
DC - $1 \times f_C$	62 μ V
DC - $2 \times f_C$	100 μ V

TYPICAL APPLICATIONS

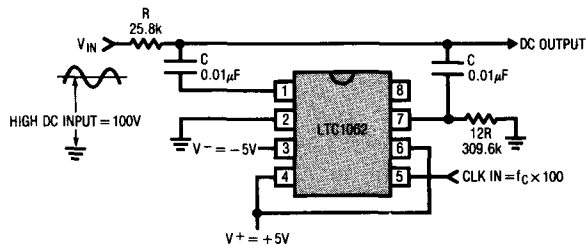
AC Coupling an External CMOS Clock Powered from a Single Positive Supply, V+



Adding an External (R1, C1) to Eliminate the Clock Feedthrough and to Improve the High Frequency Attenuation Floor



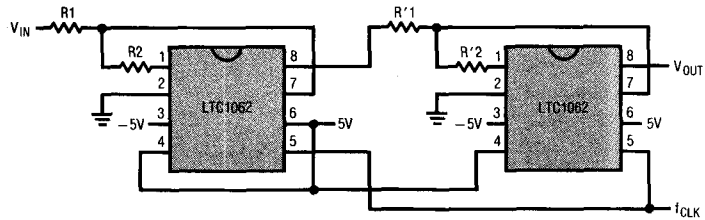
Filtering AC Signals from High DC Voltages



EX $f_{CLK} = 100\text{kHz}$, $f_C = 1\text{kHz}$. THE FILTER ACCURATELY PASSES THE HIGH DC INPUT AND ACTS AS 5th ORDER LP FILTER FOR THE AC SIGNALS RIDING ON THE DC. THE AMPLITUDE RESPONSE IN THE PASSBAND IS SHOWN BELOW.

TYPICAL APPLICATIONS

Cascading Two LTC1062s to Form a Very Selective Clock Sweepable Bandpass Filter

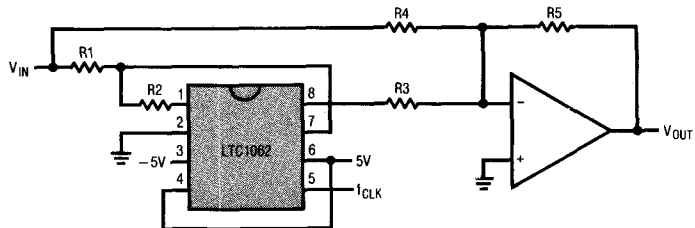


R1 = 10k, R2 = 10k
R'1 = 10k, R'2 = 12.5k

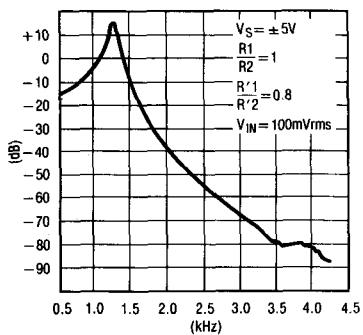
Clock Tunable Notch Filter

For simplicity use R3 = R4 = R5 = 10k;

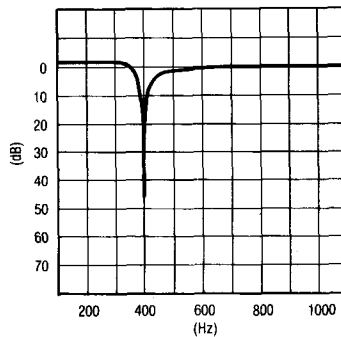
$$\frac{R1}{R2} = 1.234, \frac{f_{CLK}}{f_{notch}} = \frac{79.3}{1}$$



Frequency Response of the Bandpass Filter

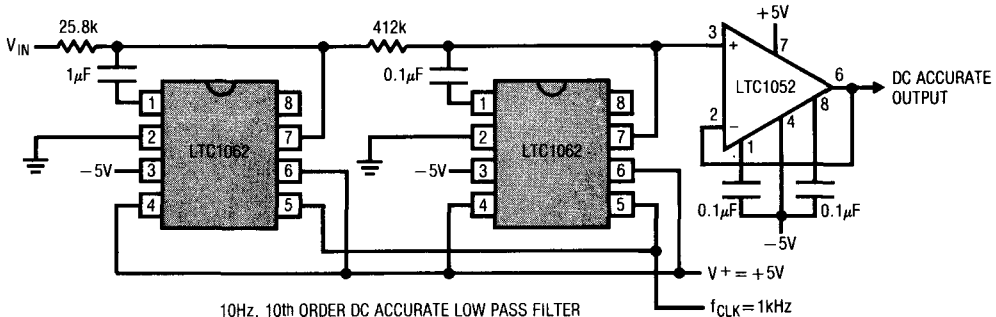


Notch Response



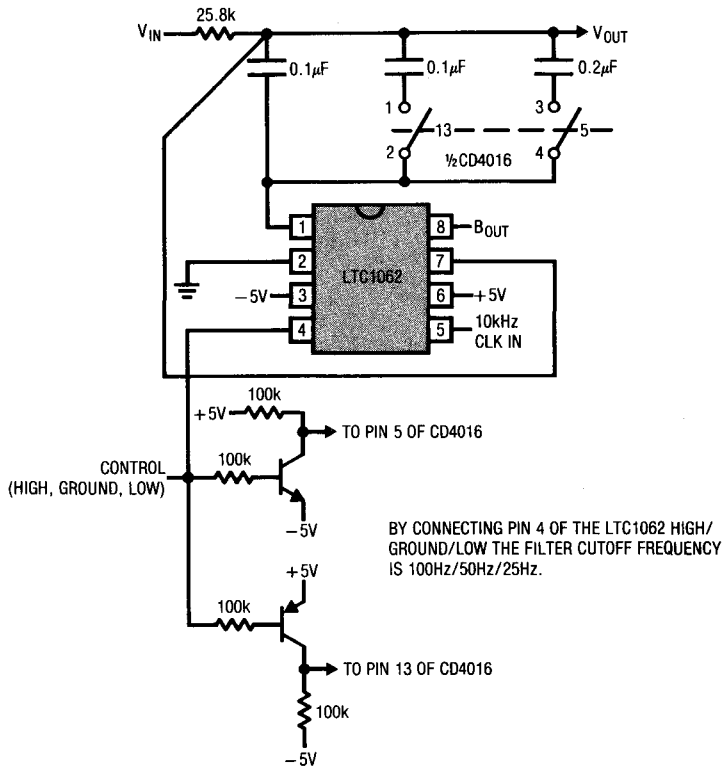
TYPICAL APPLICATIONS

Simple Cascading Technique



10Hz, 10th ORDER DC ACCURATE LOW PASS FILTER
 60dB/OCTAVE ROLLOFF
 0.5dB PASSBAND ERROR, 0dB DC GAIN
 MAXIMUM ATTENUATION 110dB ($f_{CLK} = 10kHz$)
 100dB ($f_{CLK} = 1kHz$)
 95dB ($f_{CLK} = 1MHz$)

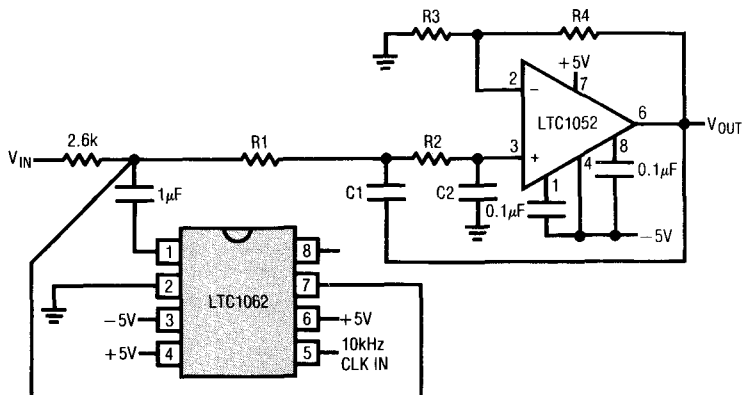
100Hz, 50Hz, 25Hz 5th Order DC Accurate LP Filter



7

TYPICAL APPLICATIONS

7th Order 100Hz Lowpass Filter with Continuous Output Filtering, Output Buffering and Gain Adjustment



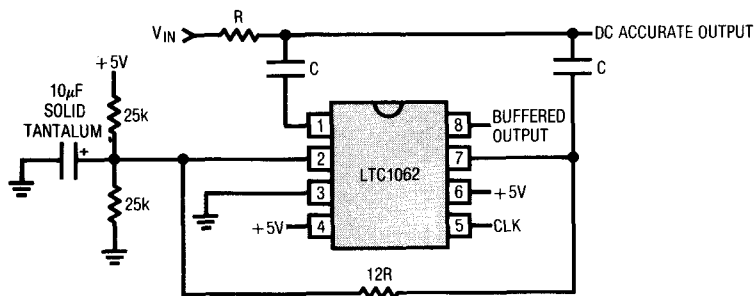
THE LTC1052 IS CONNECTED AS A 2ND ORDER SALLEN AND KEY LOWPASS FILTER WITH A CUTOFF FREQUENCY EQUAL TO THE LTC1062. THE ADDITIONAL FILTERING ELIMINATES ANY 10kHz CLOCK FEED THROUGH PLUS DECREASES THE WIDEBAND NOISE OF THE FILTER.

DC OUTPUT OFFSET (REFERRED TO A DC GAIN OF UNITY) = 5µV MAX.

WIDEBAND NOISE (REFERRED TO A DC GAIN OF UNITY) = 60µVrms

OUTPUT FILTER COMPONENT VALUES						
DC GAIN	R3	R4	R1	R2	C1	C2
1	∞	0	14.3k	53.6k	0.1µF	0.033µF
10	3.57k	32.4k	46k	274k	0.01µF	0.02µF

Single 5V Supply 5th Order LP Filter

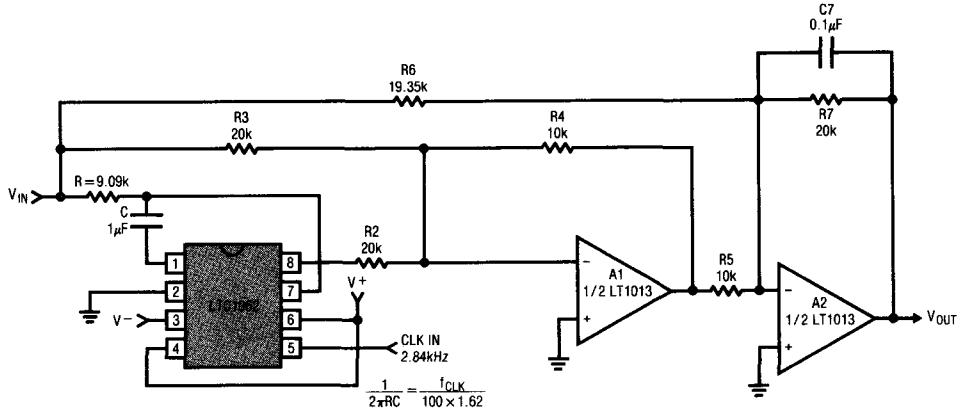


FOR A 10Hz FILTER $R = 29.4k$, $C = 1µF$, $f_{CLK} = 1kHz$

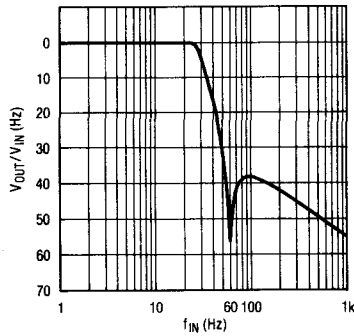
THE FILTER IS MAXIMALLY FLAT FOR $\frac{1}{2\pi RC} = \frac{f_c}{1.84}$

TYPICAL APPLICATIONS

A Lowpass Filter with a 60Hz Notch

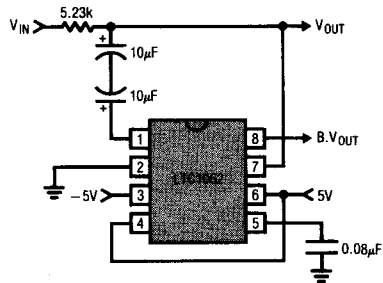


Frequency Response of the Above Lowpass Filter with the Notch $f_{NOTCH} = \frac{f_{CLK}}{47.3}$



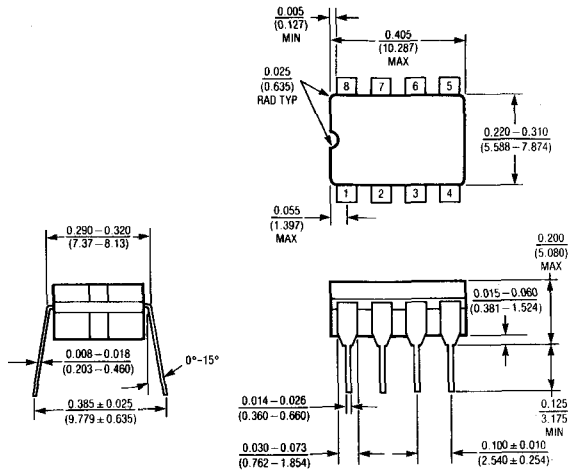
7

A Low Frequency, 5Hz Filter using Back-to-Back Solid Tantalum Capacitors



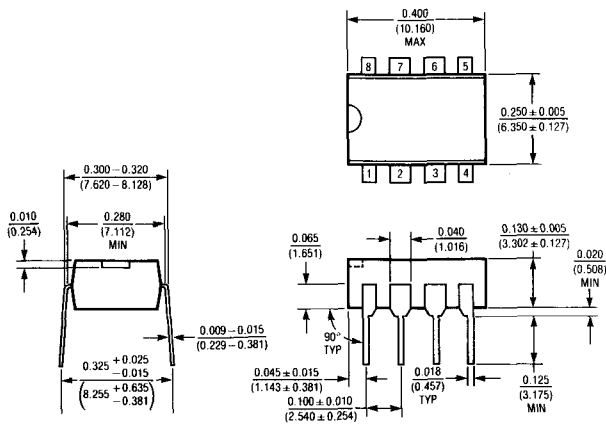
PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

J8 Package
8 Lead Hermetic DIP



T_{jmax} 150°C	Θ_{ja} 100°C/W
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N8 Package
8 Lead Plastic



T_{jmax} 100°C	Θ_{ja} 130°C/W
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FEATURES

- Lowpass Filter with No DC Error
- Low Passband Noise
- Operates DC to 20kHz
- Operates on a Single 5V Supply or Up to $\pm 8V$
- 5th Order Filter
- Maximally Flat Response
- Internal or External Clock
- Cascadable for Faster Roll-off
- Buffer Available

APPLICATIONS

- 60Hz Lowpass Filters
- Anti-Aliasing Filter
- Low Level Filtering
- Rolling Off AC Signals from High DC Voltages
- Digital Voltmeters
- Scales
- Strain Gauges

DESCRIPTION

The LTC1062 is a 5th order all pole maximally flat lowpass filter with no DC error. Its unusual architecture puts the filter outside the DC path so DC offset and low frequency noise problems are eliminated. This makes the LTC1062 very useful for lowpass filters where DC accuracy is important.

The filter input and output are simultaneously taken across an external resistor. The LTC1062 is coupled to the signal through an external capacitor. This R,C reacts with the internal switched capacitor network to form a 5th order rolloff at the output.

The filter cutoff frequency is set by an internal clock which can be externally driven. The 5th order cutoff frequency ratio is typically 100:1 allowing the clock ripple to be easily removed.

Two LTC1062s can be cascaded to form a 10th order quasi max flat lowpass filter. The device can be operated with single or dual supplies ranging from $\pm 2.5V$ to $\pm 9V$.

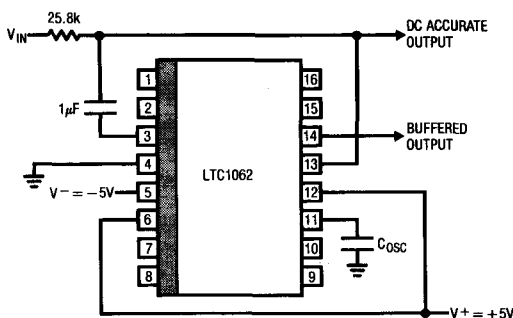
The LTC1062 is manufactured using Linear Technology's enhanced LTCMOS™ silicon gate process.

LTCMOS™ is a trademark of Linear Technology Corp.

7

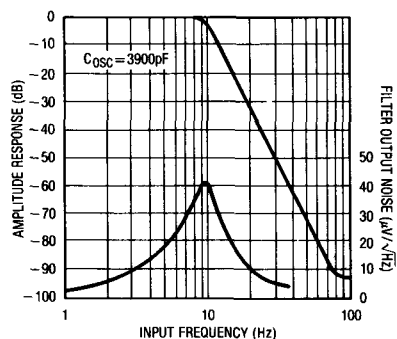
TYPICAL APPLICATION

10Hz 5th Order Butterworth Lowpass Filter



NOTE: TO ADJUST OSCILLATOR FREQUENCY, USE A 6800pF CAPACITOR IN SERIES WITH A 50k POT FROM PIN 5 TO GROUND.

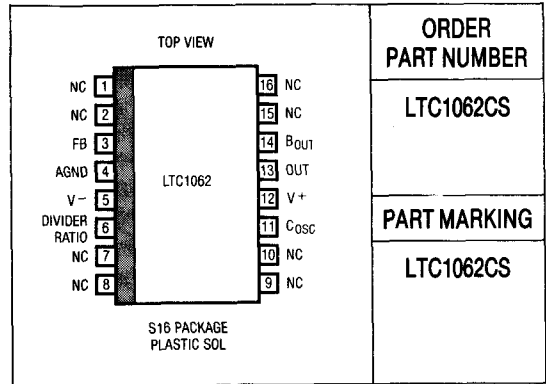
Filter Amplitude Response and Noise



ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V^+ to V^-) 18V
 Input Voltage at Any Pin $V^- - 0.3V \leq V_{IN} \leq V^+ + 0.3V$
 Operating Temperature Range $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$
 Storage Temperature Range -65°C to 150°C
 Lead Temperature Range (Soldering, 10 sec.) 300°C

PACKAGE/ORDER INFORMATION



ELECTRICAL CHARACTERISTICS

Test Conditions: $V^+ = +5V$, $V^- = -5V$, $T_A = 25^\circ\text{C}$ unless otherwise specified, AC output measured at pin 7

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	
Power Supply Current	C_{OSC} (Pin 5 to V^-) = 100 pF	•	4.5	7 10	mA	
Input Frequency Range			0-20k		Hz	
Filter Gain at $f_{IN} = 0$	$f_{CLK} = 100\text{kHz}$, Pin 4 at V^+ $C = 0.01\mu\text{F}$, $R = 25.78\text{k}$		0	-0.02	-0.3	dB
$f_{IN} = 0.5f_C$ (Note 1)		•	-2	-3		dB
$f_{IN} = f_C$		•	-28	-30		dB
$f_{IN} = 2f_C$		•	-54	-60		dB
$f_{IN} = 4f_C$						dB
Clock to Cutoff Frequency Ratio, f_{CLK}/f_C	Same as above		100 ± 1		%	
Filter Gain at $f_{IN} = 16\text{kHz}$	$f_{CLK} = 400\text{kHz}$, Pin 4 at V^+ $C = 0.01\mu\text{F}$, $R = 6.5\text{k}$	•	-46	-52		dB
f_{CLK}/f_C Tempco	Same as above		10		ppm/°C	
Filter Output (Pin 7) DC Swing	Pin 7 buffered with an external op amp	•	± 3.5	± 3.8	V	
Clock Feedthrough			10		mVp-p	
Internal Buffer						
Bias Current			2	50	pA	
Bias Current		•	170	1000	pA	
Offset Voltage			2	20	mV	
Voltage Swing	$R1 = 20\text{k}\Omega$	•	± 3.5	± 3.8	V	
Short Circuit Current Source/Sink			40/3		mA	
Clock (Note 3)						
Internal Oscillator Frequency	C_{OSC} (Pin 5 to V^-) = 100pF	•	25	32	50	kHz
	C_{OSC} (Pin 5 to V^-) = 100pF	•	15		65	kHz
Max Clock Frequency			4			MHz
Pin 5 Source or Sink Current		•	40	80		μA

The • denotes the specifications which apply over the full operating temperature range.

Note 1: f_C is the frequency where the gain is -3dB with respect to the input signal.

Note 2: The LTC1062C operates from $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$.

Note 3: The external or driven clock frequency is divided by either 1, 2, or 4 depending upon the voltage at pin 4. When pin 4 = V^+ , ratio = 1; when pin 4 = GND, ratio = 2; when pin 4 = V^- , ratio = 4.

FEATURES

- 4 Filters in a 0.3" Wide Package
- 1/2 the Noise of the LTC1059, 60, 61 Devices
- 140kHz Maximum Center Frequency
- 7MHz Maximum Clock Frequency
- Clock to Center Frequency Ratio of 50:1 and 100:1 Simultaneously Available
- Operates from $\pm 2.37V$ to $\pm 8V$ Power Supplies
- Low Offsets
- Low Harmonic Distortion
- Customized Version with Internal Resistors Available

APPLICATIONS

- Antialiasing Filters
- Wide Frequency Range Tracking Filters
- Spectral Analysis
- Loop Filters

DESCRIPTION

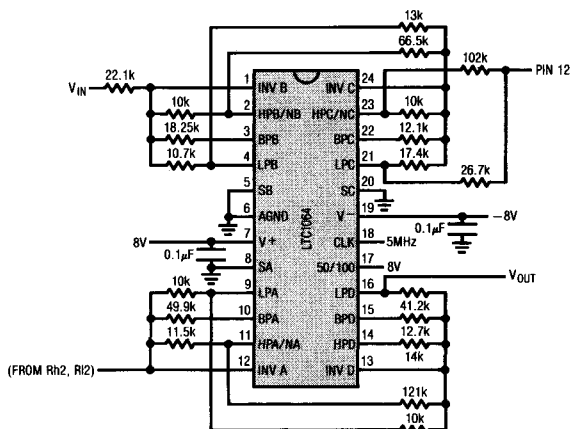
The LTC1064 consists of four high speed, low noise switched capacitor filter building blocks. Each filter building block, together with an external clock and 3 to 5 resistors can provide various 2nd order functions like low pass, high pass, bandpass and notch. The center frequency of each 2nd order function can be tuned with an external clock, or a clock and a resistor ratio. For $Q \leq 5$, the center frequency range is from 0.1Hz to 100kHz. For $Q \leq 3$, the center frequency range can be extended to 140kHz. Up to 8th order filters can be realized by cascading all four 2nd order sections. Any classical filter realization (such as Butterworth, Cauer, Bessel and Chebyshev) can be formed.

A customized monolithic version of the LTC1064 including internal thin film resistors can be obtained for high volume applications. Consult LTC marketing for details.

The LTC1064 is manufactured using Linear Technology's enhanced LTCMOS™ silicon gate process.

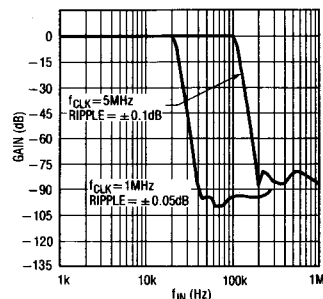
TYPICAL APPLICATION

Clock Tunable 8th Order Cauer Low Pass Filter with f_{CUTOFF} up to 100kHz



FOR $f_{CLK} = 5MHz$, ADD $C1 = 10pF$ BETWEEN PINS 4, 1
 $C2 = 10pF$ BETWEEN PINS 21, 24
 $C3 = 27pF$ BETWEEN PINS 9, 12
 WIDEBAND NOISE = $140\mu V_{RMS}$

Gain vs Frequency



LTC1064

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V^+ to V^-) 18V
 Power Dissipation 500mW
 Operating Temperature Range
 LTC1064AM, LTC1064M -55°C to 125°C
 LTC1064AC, LTC1064C -40°C to 85°C

Storage Temperature Range -65°C to 150°C
 Lead Temperature (Soldering, 10 sec.) 300°C

PACKAGE/ORDER INFORMATION

<p style="text-align: center;">TOP VIEW</p> <p style="text-align: center;">LTC1064</p> <p>J PACKAGE 24-LEAD CERAMIC DIP</p> <p>N PACKAGE 24-LEAD PLASTIC DIP</p>	<p style="text-align: center;">ORDER PART NUMBER</p> <p style="text-align: center;">LTC1064AMJ LTC1064MJ LTC1064ACJ LTC1064CJ LTC1064ACN LTC1064CN</p>	<p style="text-align: center;">TOP VIEW</p> <p style="text-align: center;">LTC1064</p> <p>SO PACKAGE 24-LEAD PLASTIC SOIC</p>	<p style="text-align: center;">ORDER PART NUMBER</p> <p style="text-align: center;">LTC1064CS</p>
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ELECTRICAL CHARACTERISTICS

(Internal Op Amps) $T_A = 25^\circ\text{C}$, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Supply Voltage Range		± 2.37		± 8	V
Voltage Swings	$V_S = \pm 5\text{V}$, $R_L = 5\text{k}\Omega$	± 3.3 ± 3.2	± 3.6		V V
Output Short Circuit Current (Source/Sink)	$V_S = \pm 5\text{V}$		3		mA
DC Open Loop Gain	$V_S = \pm 5\text{V}$, $R_L = 5\text{k}\Omega$		80		dB
GBW Product	$V_S = \pm 5\text{V}$		7		MHz
Slew Rate	$V_S = \pm 5\text{V}$		10		V/ μs

ELECTRICAL CHARACTERISTICS(Complete Filter) $V_S = \pm 5V$, $T_A = 25^\circ C$, TTL clock input level, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	
Center Frequency Range, f_o	$V_S = \pm 8V$, $Q \leq 3$		0.1-140		kHz	
Input Frequency Range			0-1		MHz	
Clock to Center Frequency Ratio, f_{CLK}/f_o	LTC1064A (Note 1) LTC1064	●	50 ± 0.3	50 ± 0.8	%	
	LTC1064A (Note 1) LTC1064			50 ± 0.9	%	
Clock to Center Frequency Ratio, Side to Side Matching	LTC1064A (Note 1) LTC1064	●	100 ± 0.3	100 ± 0.8	%	
	LTC1064A (Note 1) LTC1064			100 ± 0.9	%	
Clock to Center Frequency Ratio, Side to Side Matching	LTC1064A (Note 1) LTC1064	●	0.4	1	%	
	LTC1064A (Note 1) LTC1064			1	%	
Clock to Center Frequency Ratio, f_{CLK}/f_o (Note 2)	LTC1064A (Note 1) LTC1064	●	50 ± 0.6	50 ± 1.3	%	
	LTC1064A (Note 1) LTC1064			50 ± 1.3	%	
Q Accuracy	LTC1064A (Note 1) LTC1064	●	± 2	6	%	
	LTC1064A (Note 1) LTC1064			± 3	8	%
f_o Temperature Coefficient	Mode 1, 50:1, $f_{CLK} < 2MHz$		± 1		ppm/°C	
Q Temperature Coefficient	Mode 1, 100:1, $f_{CLK} < 2MHz$		± 5		ppm/°C	
	Mode 3, $f_{CLK} < 2MHz$		± 5		ppm/°C	
DC Offset Voltage	V_{OS1}	●	2	15	mV	
	V_{OS2}	●	3	45	mV	
	V_{OS3}	●	3	45	mV	
Clock Feedthrough	$f_{CLK} < 1MHz$		0.2		mV _{RMS}	
Maximum Clock Frequency	Mode 1, $Q < 5$, $V_S \geq \pm 5V$		7		MHz	
Power Supply Current		●	9	12	16	mA
				22	mA	

The ● denotes the specifications which apply over the full operating temperature range.

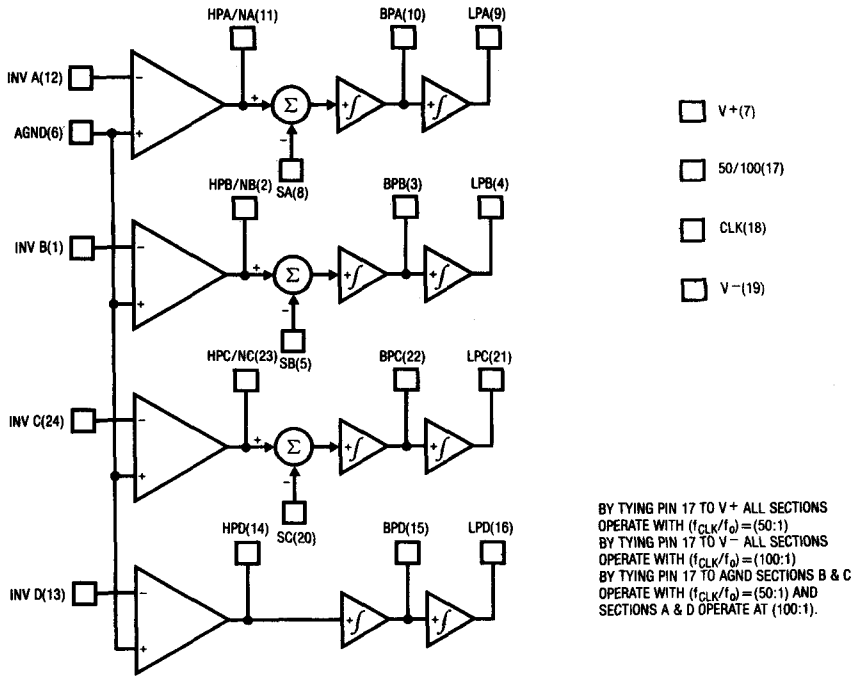
Note 1: Contact LTC Marketing.

Note 2: Not tested, guaranteed by design.

Table 1. Output DC Offsets One 2nd Order Section

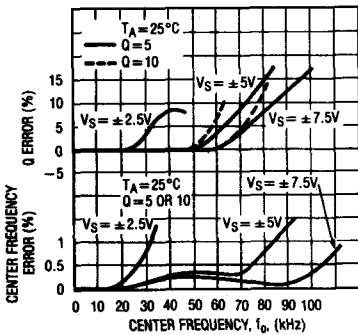
MODE	V_{OSN} PIN 2, 11, 14, 23	V_{OSBP} PIN 3, 10, 15, 22	V_{OSLP} PIN 4, 9, 16, 21
1	$V_{OS1}[(1/Q) + 1 + IH_{OLP}] - V_{OS3}/Q$	V_{OS3}	$V_{OSN} - V_{OS2}$
1b	$V_{OS1}[(1/Q) + 1 + R2/R1] - V_{OS3}/Q$	V_{OS3}	$-(V_{OSN} - V_{OS2})(1 + R5/R6)$
2	$[V_{OS1}(1 + R2/R1 + R2/R3 + R2/R4) - V_{OS3}(R2/R3)] \times [R4/(R2 + R4)] + V_{OS2}[R2/(R2 + R4)]$	V_{OS3}	$V_{OSN} - V_{OS2}$
3	V_{OS2}	V_{OS3}	$V_{OS1} \left[1 + \frac{R4}{R1} + \frac{R4}{R2} + \frac{R4}{R3} \right] - V_{OS2} \left(\frac{R4}{R2} \right) - V_{OS3} \left(\frac{R4}{R3} \right)$

BLOCK DIAGRAM

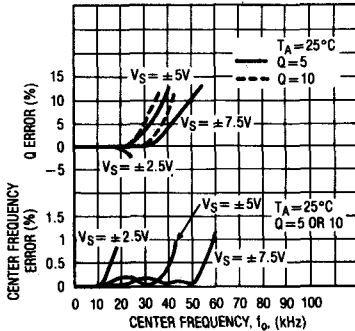


TYPICAL PERFORMANCE CHARACTERISTICS

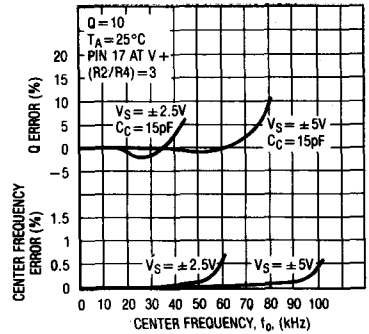
Graph 1. Mode 1, (f_{CLK}/f_o) = 50:1



Graph 2. Mode 1, (f_{CLK}/f_o) = 100:1

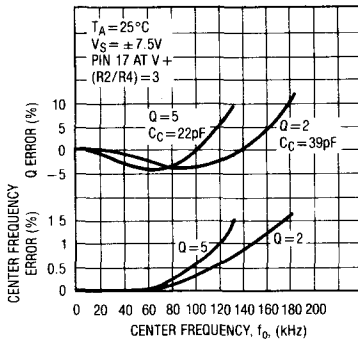


Graph 3. Mode 2, (f_{CLK}/f_o) = 25:1

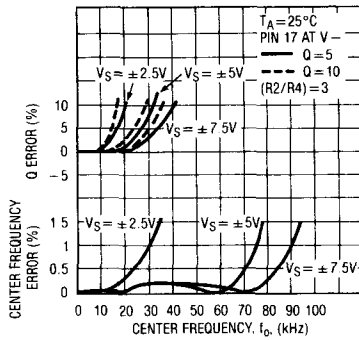


TYPICAL PERFORMANCE CHARACTERISTICS

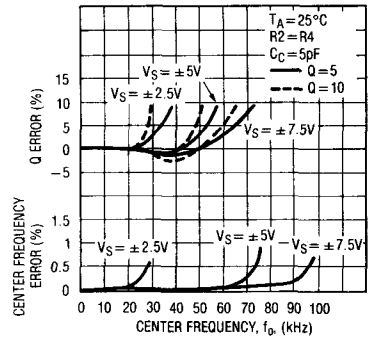
Graph 4. Mode 2, (f_{CLK}/f_o) = 25:1



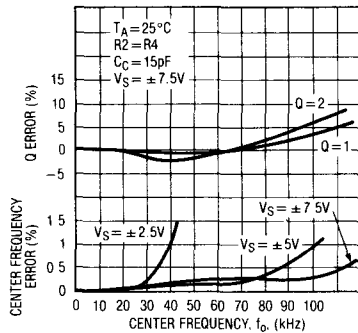
Graph 5. Mode 2, (f_{CLK}/f_o) = 50:1



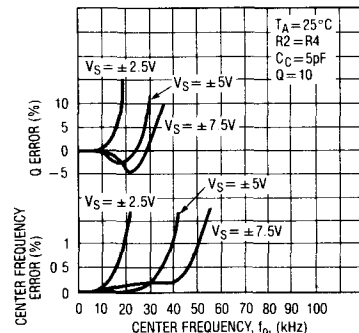
Graph 6. Mode 3, (f_{CLK}/f_o) = 50:1



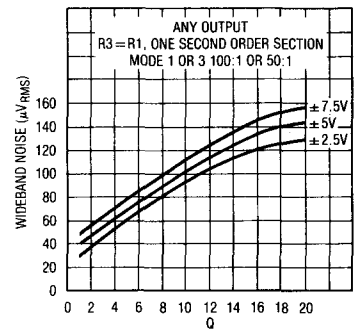
Graph 7. Mode 3, (f_{CLK}/f_o) = 50:1



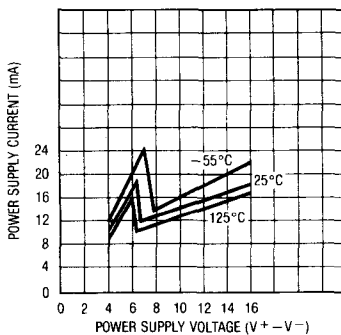
Graph 8. Mode 3, (f_{CLK}/f_o) = 100:1



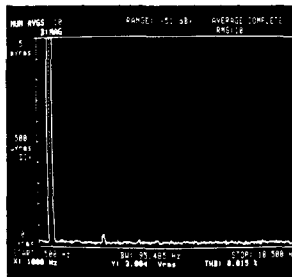
Graph 9. Wideband Noise vs Q



Graph 10. Power Supply Current vs Supply Voltage



Graph 11. Harmonic Distortion, 8th Order LP Butterworth $f_c = 20\text{kHz}$ THD = 0.015% for $3V_{RMS}$ Input



PIN DESCRIPTION

Power Supplies (Pins 7, 19)

They should be bypassed with 0.1 μ F ceramic disc. Low noise, non-switching, power supplies are recommended. The device operates with a single 5V supply and with dual supplies. The absolute maximum operating power supply voltage is $\pm 9V$.

Clock (Pin 18)

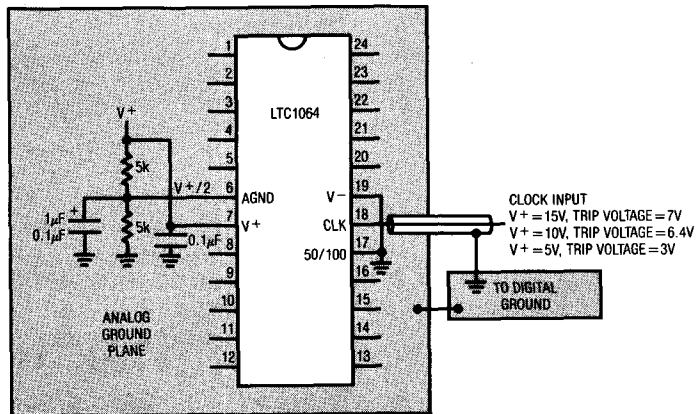
For $\pm 5V$ supplies the logic threshold level is 1.4V. For $\pm 8V$ and 0 to 5V supplies the logic threshold levels are 2.2V and 3V respectively. The logic threshold levels vary $\pm 100mV$ over the full military temperature range. The recommended duty cycle of the input clock is 50% although for clock frequencies below 500kHz the clock "on" time can be as low as 200ns. The maximum clock frequency for $\pm 5V$ supplies is 4MHz. For $\pm 7V$ supplies and above, the maximum clock frequency is 7MHz.

AGND (Pin 6)

When the LTC1064 operates with dual supplies, Pin 6 should be tied to system ground. When the LTC1064 operates with a single positive supply, the analog ground pin should be tied to 1/2 supply and it should be bypassed with a 1 μ F solid tantalum in parallel with a 0.1 μ F ceramic disc, Figure 1. The positive input of all the internal op amps, as well as the common reference of all the internal switches, are internally tied to the analog ground pin. Because of this, a very "clean" ground is recommended.

50/100 (Pin 17)

By tying Pin 17 to V^+ , all filter sections operate with a clock to center frequency ratio internally set at 50:1. When Pin 17 is at mid-supplies, sections B and C operate with $(f_{CLK}/f_0) = 50:1$ and sections A and D operate at $(100:1)$. When Pin 17 is shorted to the negative supply pin, all filter sections operate with $(f_{CLK}/f_0) = 100:1$.



NOTE: PIN 5, 8, 20, IF NOT USED, SHOULD BE CONNECTED TO PIN 6.

Figure 1. Single Supply Operation

APPLICATIONS INFORMATION

ANALOG CONSIDERATIONS

1. Grounding and Bypassing

The LTC1064 should be used with separated analog and digital ground planes and single point grounding techniques.

Pin 6 (AGND) should be tied directly to the analog ground plane.

Pin 7 (V^+) should be bypassed to the ground plane with a $0.1\mu\text{F}$ ceramic disk with leads as short as possible. Pin 19 (V^-) should be bypassed with a $0.1\mu\text{F}$ ceramic disk. For single supply applications, V^- can be tied to the analog ground plane.

For good noise performance, V^+ and V^- must be free of noise and ripple.

All analog inputs should be referenced directly to the single point ground. The clock inputs should be shielded from and/or routed away from the analog circuitry and a separate digital ground plane used.

Figure 2 shows an example of an ideal ground plane design for a two sided board. Of course this much ground plane will not always be possible, but users should strive to get as close to this as possible. Proto boards are not recommended.

2. Buffering the Filter Output

When driving coaxial cables and $1\times$ scope probes, the filter output should be buffered. This is important especially when high Q s are used to design a specific filter. *Inadequate buffering may cause errors in noise, distortion, Q , and gain measurements.* When $10\times$ probes are used, buffering is usually not required. An inverting buffer is recommended especially when THD tests are performed. As shown in Figure 3, the buffer should be adequately bypassed to minimize clock feedthrough.

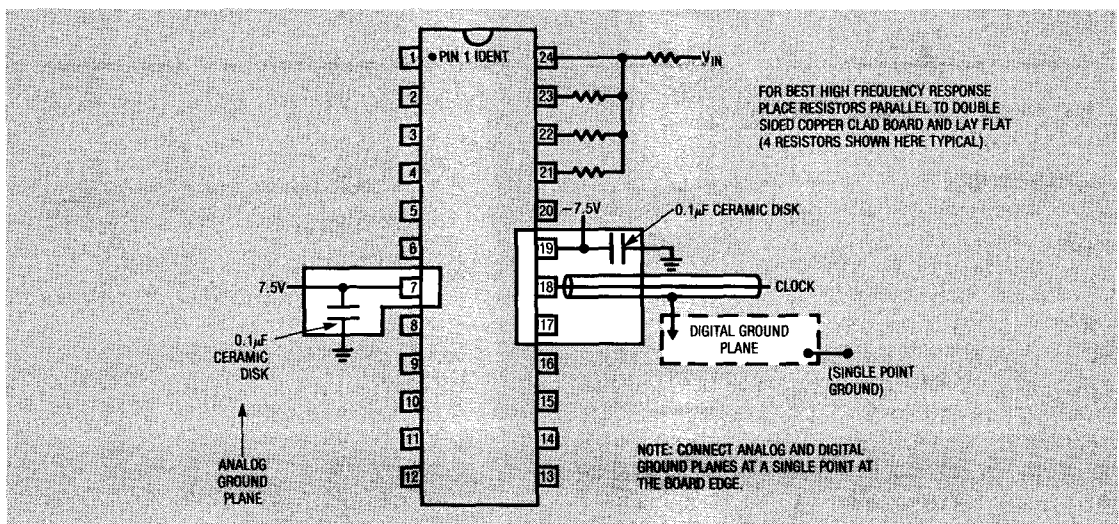


Figure 2. Example Ground Plane Breadboard Technique for LTC1064

APPLICATIONS INFORMATION

3. Offset Nulling

Low pass filters may have too much DC offset for some users. A servo circuit may be used to actively null the offsets of the LTC1064 or any LTC switched capacitor filter. The circuit shown in Figure 4 will null offsets to better than $300\mu\text{V}$. This circuit takes seconds to settle because of the integrator pole frequency.

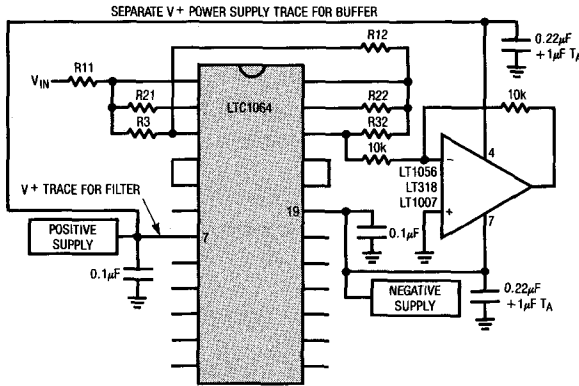


Figure 3. Buffering the Output of a 4th Order Bandpass Realization

4. Noise

All the noise performance mentioned excludes the clock feedthrough. Noise measurements will degrade if, the already described grounding, bypassing, and buffering techniques are not practiced. Graph 9 is a very good representation of the noise performance of this device.

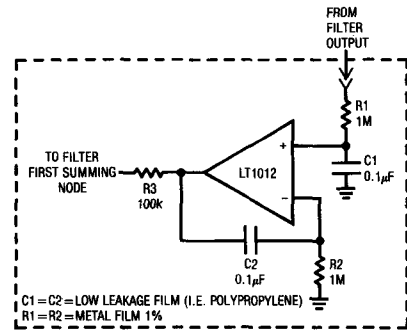


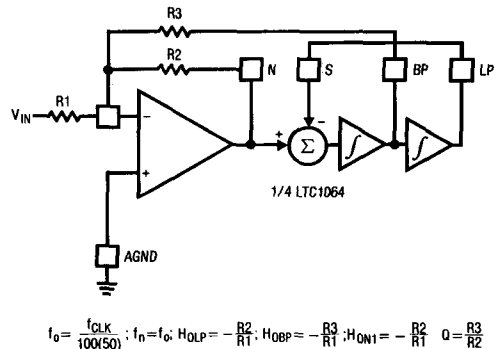
Figure 4. Servo Amplifier

MODES OF OPERATION

PRIMARY MODES

Mode 1

In Mode 1, the ratio of the external clock frequency to the center frequency of each second order section is internally fixed at 50:1 or 100:1. Figure 5 illustrates Mode 1 providing 2nd order notch, low pass, and bandpass outputs. Mode 1 can be used to make high order Butterworth low pass filters; it can also be used to make low Q notches and for cascading 2nd order bandpass functions tuned at the same center frequency with unity gain. Mode 1 is faster than Mode 3. Note that Mode 1 can only be implemented with 3 of the 4 LTC1064 sections because section D has no



$$f_0 = \frac{f_{CLK}}{100(50)}; f_n = f_0; H_{OLP} = -\frac{R_2}{R_1}; H_{OBP} = -\frac{R_3}{R_1}; H_{ON1} = -\frac{R_2}{R_1}; Q = \frac{R_3}{R_2}$$

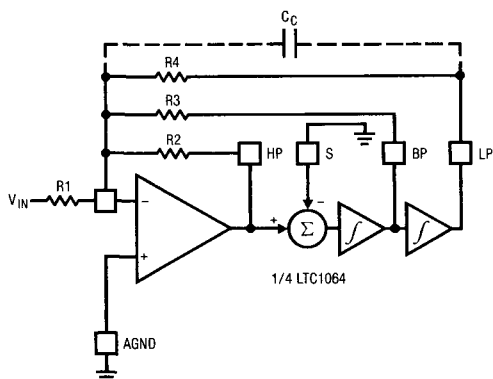
Figure 5. Mode 1: 2nd Order Filter Providing Notch, Bandpass, Low Pass

MODES OF OPERATION

externally available summing node. Section D, however, can be internally connected in Mode 1 upon special request.

Mode 3

Mode 3 is the second of the primary modes. In Mode 3, the ratio of the external clock frequency to the center frequency of each 2nd order section can be adjusted above or below 50:1 or 100:1. Side D of the LTC1064 can only be connected in Mode 3. Figure 6 illustrates Mode 3, the classical state variable configuration, providing high pass, bandpass, and low pass second order filter functions. Mode 3 is slower than Mode 1. Mode 3 can be used to make high order all-pole bandpass, low pass, high pass and notch filters.



$$\text{MODE 3 (100:1): } f_0 = \frac{f_{\text{CLK}}}{100} \sqrt{\frac{R_2}{R_4}}; Q = \frac{R_3}{R_2} \sqrt{\frac{R_2}{R_4}}; H_{\text{OHP}} = -R_2/R_1;$$

$$H_{\text{OBP}} = -R_3/R_1; H_{\text{OLP}} = -R_4/R_1$$

$$\text{MODE 3 (50:1): } f_0 = \frac{f_{\text{CLK}}}{50} \sqrt{\frac{R_2}{R_4}}; Q = \frac{1.005(\sqrt{R_2/R_4})}{(R_2/R_3) - (R_2/16R_4)};$$

$$H_{\text{OHP}} = -R_2/R_1; H_{\text{OBP}} = -\frac{R_3/R_1}{1 - (R_3/16R_4)}; H_{\text{OLP}} = -R_4/R_1$$

NOTE: THE 50:1 EQUATIONS FOR MODE 3 ARE DIFFERENT FROM THE EQUATIONS FOR MODE 3 OPERATION OF THE LTC1059, LTC1060 AND LTC1061. START WITH f_0 . CALCULATE R_2/R_4 . SET R_4 ; FROM THE Q VALUE, CALCULATE R_3 :

$$R_3 = \frac{R_2}{\frac{1.005}{Q} \sqrt{\frac{R_2}{R_4}} + \frac{R_2}{16R_4}}; \text{ THEN CALCULATE } R_1 \text{ TO SET THE DESIRED GAIN.}$$

Figure 6. Mode 3: 2nd Order Filter Providing High Pass, Bandpass, Low Pass

When the internal clock to center frequency ratio is set at 50:1, the design equations for Q and bandpass gain are different from the 100:1 case. This was done to provide speed without penalizing the noise performance.

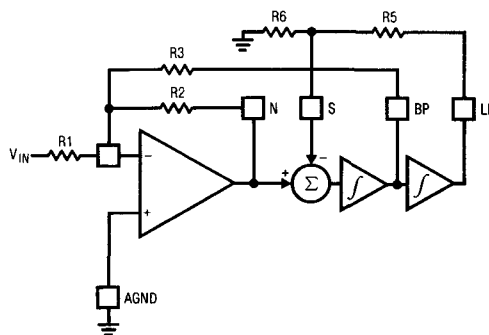
SECONDARY MODES

Mode 1b

Mode 1b is derived from Mode 1. In Mode 1b, Figure 7, two additional resistors R_5 and R_6 , are added to alternate the amount of voltage fed back from the low pass output into the input of the SA (or SB or SC) switched capacitor summer. This allows the filter clock to center frequency ratio to be adjusted beyond 50:1 or 100:1. Mode 1b maintains the speed advantages of Mode 1.

Mode 2

Mode 2 is a combination of Mode 1 and Mode 3, as shown in Figure 8. With Mode 2, the clock to center frequency ratio, f_{CLK}/f_0 , is always less than 50:1 or 100:1. The advantage of Mode 2 is that it provides less sensitivity to resistor tolerances than does Mode 3. As in Mode 1, Mode 2 has



$$f_0 = \frac{f_{\text{CLK}}}{100(50)} \sqrt{\frac{R_6}{R_5 + R_6}}; f_n = f_0; Q = \frac{R_3}{R_2} \sqrt{\frac{R_6}{R_5 + R_6}};$$

$$H_{\text{ON1}}(f \rightarrow 0) = H_{\text{ON2}} \left(f \rightarrow \frac{f_{\text{CLK}}}{2} \right) = -\frac{R_2}{R_1}; H_{\text{OLP}} = -\frac{R_2/R_1}{R_6/(R_5 + R_6)};$$

$$H_{\text{OBP}} = -\frac{R_3}{R_1}; (R_5/R_6) < 5k\Omega$$

Figure 7. Mode 1b: 2nd Order Filter Providing Notch, Bandpass, Low Pass

MODES OF OPERATION

a notch output which depends on the clock frequency, and the notch frequency is therefore less than the center frequency, f_0 .

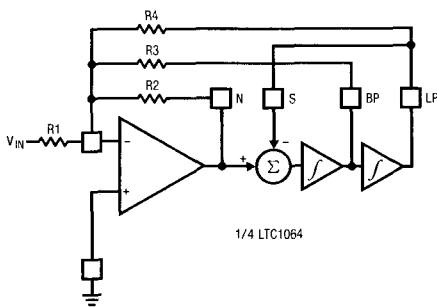
When the internal clock to center frequency ratio is set at 50:1, the design equations for Q and bandpass gain are different from the 100:1 case.

Mode 3A

This is an extension of Mode 3 where the high pass and low pass output are summed through two external resistors R_h and R_l to create a notch. This is shown in Figure 9. Mode 3A is more versatile than Mode 2 because the notch

frequency can be higher or lower than the center frequency of the 2nd order section. The external op amp of Figure 9 is not always required. When cascading the sections of the LTC1064, the high pass and low pass outputs can be summed directly into the inverting input of the next section. The topology of Mode 3A is useful for elliptic high pass and notch filters with clock to cutoff frequency ratios higher than 100:1. This is often required to extend the allowed input signal frequency range and to avoid premature aliasing.

When the internal clock to center frequency ratio is set at 50:1, the design equations for Q and bandpass gain are different from the 100:1 case.



$$\text{MODE 2 (100:1): } f_0 = \frac{f_{\text{CLK}}}{100} \sqrt{1 + \frac{R_2}{R_4}}; f_n = \frac{f_{\text{CLK}}}{50}; Q = \frac{R_3}{R_2} \sqrt{1 + \frac{R_2}{R_4}}; H_{\text{OLP}} = \frac{-R_2/R_1}{1 + (R_2/R_4)}$$

$$H_{\text{OBP}} = -R_3/R_1; H_{\text{ON1}}(f=0) = \frac{-R_2/R_1}{1 + (R_2/R_4)}; H_{\text{ON2}}\left(1 - \frac{f_{\text{CLK}}}{2}\right) = -R_2/R_1$$

$$\text{MODE 2 (50:1): } f_0 = \frac{f_{\text{CLK}}}{50} \sqrt{1 + \frac{R_2}{R_4}}; f_n = \frac{f_{\text{CLK}}}{50}; Q = \frac{1.005\sqrt{1 + R_2/R_4}}{(R_2/R_3) - (R_2/16R_4)}; H_{\text{OLP}} = \frac{-R_2/R_1}{1 + (R_2/R_4)}$$

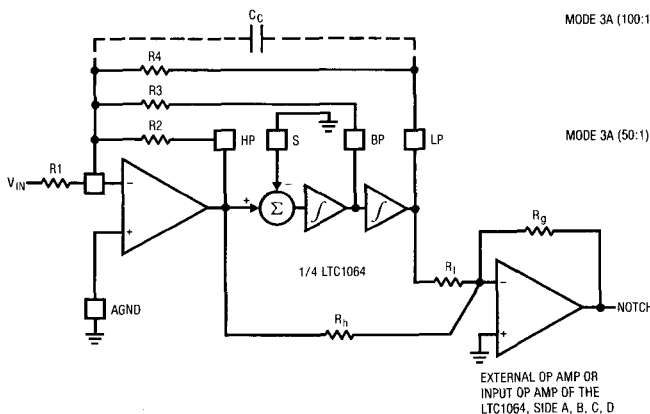
$$H_{\text{OBP}} = \frac{-R_3/R_1}{1 - (R_3/16R_4)}; H_{\text{ON1}}(f=0) = \frac{-R_2/R_1}{1 + (R_2/R_4)}$$

$$H_{\text{ON2}}\left(1 - \frac{f_{\text{CLK}}}{2}\right) = -R_2/R_1$$

NOTE: THE 50:1 EQUATIONS FOR MODE 2 ARE DIFFERENT FROM THE EQUATIONS FOR MODE 2 OPERATION OF THE LTC1059, LTC1060 AND LTC1061. START WITH f_0 , CALCULATE R_2/R_4 , SET R_4 ; FROM THE Q VALUE, CALCULATE R_3 .

$$R_3 = \frac{1.005}{Q} \sqrt{1 + \frac{R_2}{R_4}} + \frac{R_2}{16R_4}; \text{ THEN CALCULATE } R_1 \text{ TO SET THE DESIRED GAIN.}$$

Figure 8. Mode 2: 2nd Order Filter Providing Notch, Bandpass, Low Pass



$$\text{MODE 3A (100:1): } f_0 = \frac{f_{\text{CLK}}}{100} \sqrt{\frac{R_2}{R_4}}; f_n = \frac{f_{\text{CLK}}}{100} \sqrt{\frac{R_h}{R_l}}; H_{\text{OHP}} = -R_2/R_1; H_{\text{OBP}} = -R_3/R_1$$

$$H_{\text{OLP}} = -R_4/R_1; H_{\text{ON1}}(f=0) = \frac{R_g}{R_l} \times \frac{R_4}{R_1}; H_{\text{ON2}}\left(1 - \frac{f_{\text{CLK}}}{2}\right) = \frac{R_g}{R_h} \times \frac{R_2}{R_1}$$

$$H_{\text{ON1}}(f=f_0) = Q \left(\frac{R_g}{R_l} H_{\text{OLP}} - \frac{R_g}{R_h} H_{\text{OHP}} \right); Q = \frac{R_3}{R_2} \sqrt{\frac{R_2}{R_4}}$$

$$\text{MODE 3A (50:1): } f_0 = \frac{f_{\text{CLK}}}{50} \sqrt{\frac{R_2}{R_4}}; f_n = \frac{f_{\text{CLK}}}{50} \sqrt{\frac{R_h}{R_l}}; H_{\text{OHP}}\left(1 - \frac{f_{\text{CLK}}}{2}\right) = -R_2/R_1$$

$$H_{\text{OBP}} = \frac{-R_3/R_1}{1 - (R_3/16R_4)}; H_{\text{OLP}}(f=0) = -R_4/R_1; Q = \frac{1.005\sqrt{R_2/R_4}}{(R_2/R_3) - (R_2/16R_4)}$$

NOTE: THE 50:1 EQUATIONS FOR MODE 3A ARE DIFFERENT FROM THE EQUATIONS FOR MODE 3A OPERATION OF THE LTC1059, LTC1060 AND LTC1061. START WITH f_0 , CALCULATE R_2/R_4 , SET R_4 ; FROM THE Q VALUE, CALCULATE R_3 .

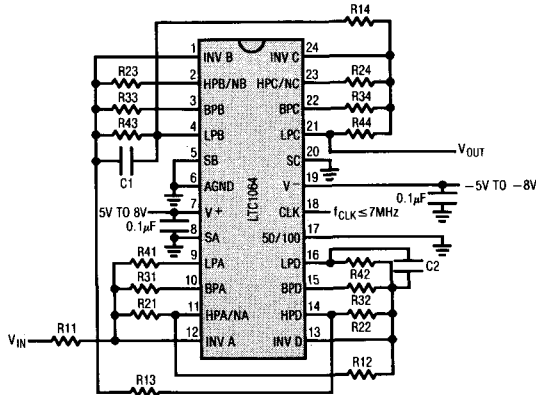
$$R_3 = \frac{1.005}{Q} \sqrt{\frac{R_2}{R_4}} + \frac{R_2}{16R_4}; \text{ THEN CALCULATE } R_1 \text{ TO SET THE DESIRED GAIN.}$$

EXTERNAL OP AMP OR INPUT OP AMP OF THE LTC1064, SIDE A, B, C, D

Figure 9. Mode 3A: 2nd Order Filter Providing High Pass, Bandpass, Low Pass, Notch

APPLICATION CIRCUITS

Wideband Bandpass: Ratio of High to Low Corner Frequency Equal to 2

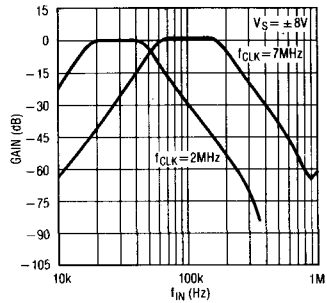


RESISTOR VALUES

R11 = 16k	R21 = 16k	R31 = 7.32k	R41 = 10k
R12 = 10k	R22 = 10k	R32 = 22.6k	R42 = 13.3k
R13 = 23.2k	R23 = 13.3k	R33 = 21.5k	R43 = 10k
R14 = 6.8k	R24 = 20k	R34 = 15.4k	R44 = 32.4k

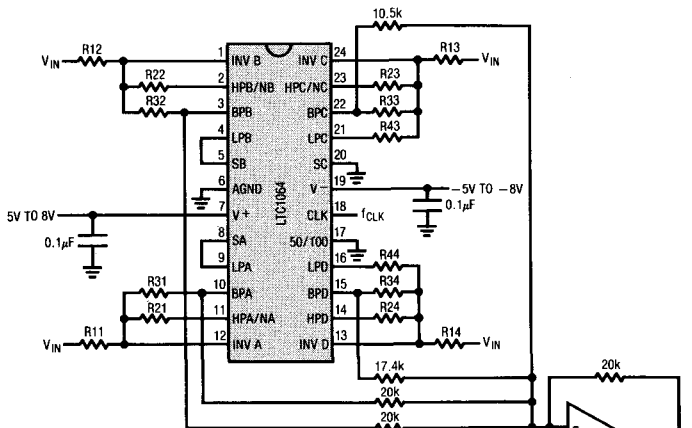
NOTE 1: FOR $f_{CLK} \geq 3MHz$, USE $C1 = C2 = 22pF$

Amplitude Response



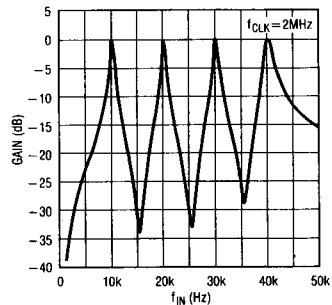
Quad Bandpass Filter with Center Frequency Equal to $f_0, 2f_0, 3f_0, 4f_0$

Amplitude Response



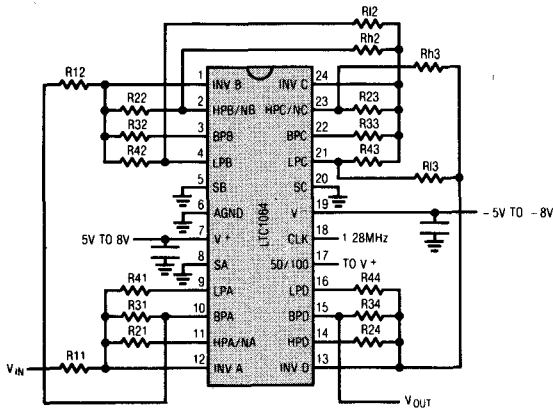
RESISTOR VALUES

R11 = 249k	R21 = 10k	R31 = 249k	R41 = 17.8k
R12 = 249k	R22 = 10k	R32 = 249k	R42 = 40.2k
R13 = 499k	R23 = 10k	R33 = 174k	
R14 = 453k	R24 = 10k	R34 = 249k	



APPLICATION CIRCUITS

8th Order Bandpass Filter with 2 Stopband Notches

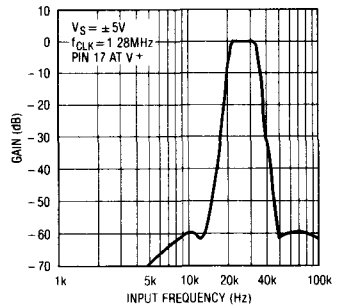


RESISTOR VALUES

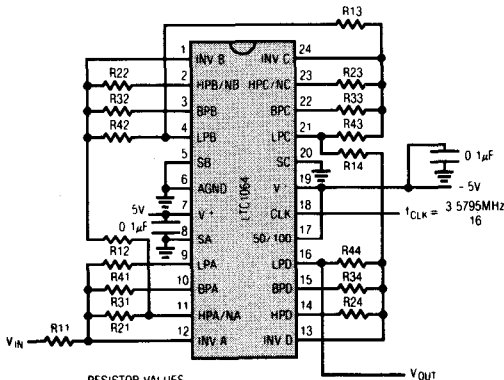
R11 = 46 95k	R21 = 10k	R31 = 38 25k	R41 = 11 81k
R12 = 93 93k	R22 = 10k	R32 = 81 5k	R42 = 14 72k
	Rh2 = 6 9k	Rh1 = 27 46k	
	R23 = 16 3k	R33 = 70 3k	R43 = 10k
		Rh3 = 69 7k	R3 = 17 9k
	R24 = 13 19k	R34 = 39 42k	R44 = 10 5k

- NOTE 1 THE V+ V- V PINS SHOULD BE BYPASSED WITH A 0.1μF-0.22μF CERAMIC DISC RIGHT AT THE PINS
- NOTE 2 THE RATIOS OF ALL (R2/R4) RESISTORS SHOULD BE MATCHED TO BETTER THAN 0.25% THE REMAINING RESISTORS SHOULD BE BETTER THAN 0.5% ACCURATE

Amplitude Response



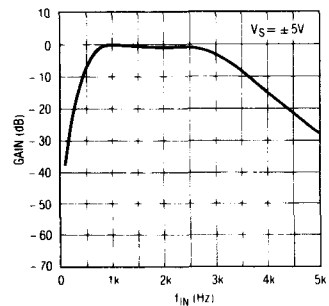
C-Message Filter



RESISTOR VALUES

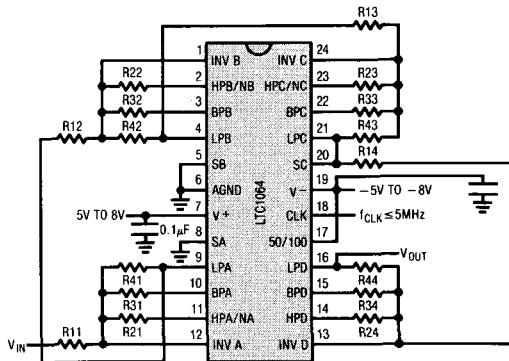
R11 = 88 7k	R21 = 10k	R31 = 35 7k	R41 = 88 7k
R12 = 10k	R22 = 44 8k	R32 = 33 2k	R42 = 24 9k
R13 = 15 8k	R23 = 48 9k	R33 = 63 5k	R43 = 25 5k
R14 = 15 8k	R24 = 44 8k	R34 = 16 5k	R44 = 24 9k

Amplitude Response



APPLICATION CIRCUITS

8th Order Chebyshev Low Pass Filter with a Passband Ripple of 0.1dB and Cutoff Frequency up to 100kHz



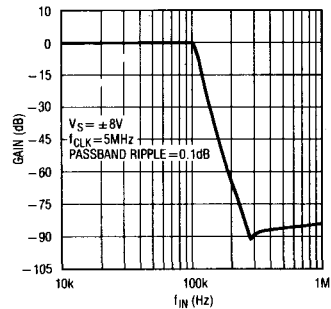
RESISTOR VALUES

R11 = 100.86k R21 = 16.75k R31 = 23.6k R41 = 99.73k
 R12 = 25.72k R22 = 20.93k R32 = 45.2k R42 = 25.52k
 R13 = 16.61k R23 = 10.18k R33 = 68.15k R43 = 99.83k
 R14 = 13.84k R24 = 11.52k R34 = 17.72k R44 = 25.42k

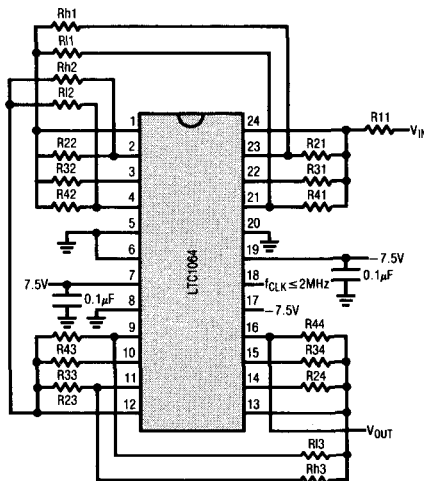
NOTE 1: FOR $f_{CLK} > 3MHz$, ADD C2 = 10pF ACROSS R42
 C3 = 10pF ACROSS R43
 C4 = 10pF ACROSS R44

WIDEBAND NOISE = 170µV_{RMS}

Amplitude Response



8th Order Clock Sweeplable Low Pass Elliptic Antialiasing Filter

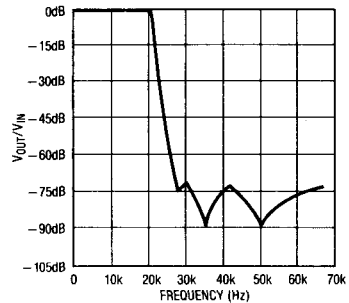


RESISTOR VALUES

R11 = 19.1k R21 = 10k R31 = 13.7k R41 = 15.4k
 Rh1 = 30.9k Rh1 = 14k R22 = 10k R32 = 23.7k
 R42 = 10.2k Rh2 = 76.8k R12 = 26.7k R23 = 11.3k
 R33 = 84.5k R43 = 10k
 Rh3 = 60.2k R13 = 10k
 R24 = 15.4k R34 = 15.2k R44 = 42.7k

NOTE: FOR $f_{CUTOFF} > 15kHz$, ADD A 5pF CAPACITOR ACROSS R41 AND R43

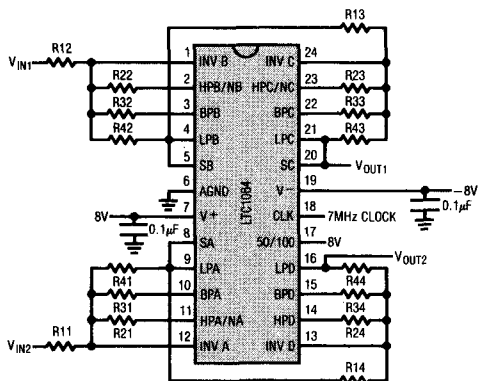
Amplitude Response



8TH ORDER CLOCK SWEEPABLE LOW PASS ELLIPTIC ANTIALIASING FILTER MAINTAINS, FOR $0.1Hz \leq f_{CUTOFF} \leq 20kHz$, A $\pm 0.1dB$ MAX. PASSBAND ERROR AND 72dB MIN. STOPBAND ATTENUATION AT $1.5 \times f_{CUTOFF}$. TOTAL WIDEBAND NOISE = 150µV_{RMS}. THD = 70dB (0.03%) FOR $V_{IN} = 3V_{RMS}$. $f_{CLK}/f_{CUTOFF} = 100:1$. THIS FILTER AVAILABLE AS LTC1064-1 WITH INTERNAL THIN FILM RESISTORS.

APPLICATION CIRCUITS

Dual 4th Order Bessel Filter with 140kHz Cutoff Frequency

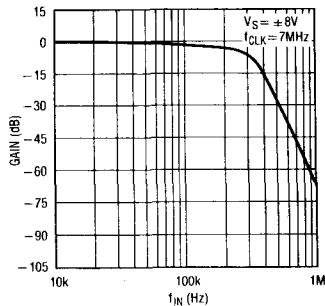


RESISTOR VALUES

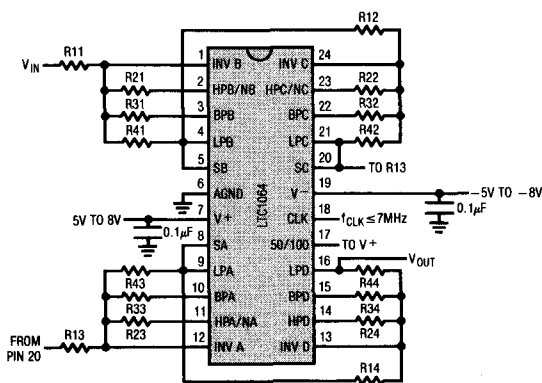
R11 = 14.3k	R21 = 13k	R31 = 7.5k	R41 = 10k
R12 = 15.4k	R22 = 15.4k	R32 = 7.5k	R42 = 10k
R13 = 3.92k	R23 = 20k	R33 = 27.4k	R43 = 40k
R14 = 3.92k	R24 = 20k	R34 = 6.8k	R44 = 10k

WIDEBAND NOISE = 64µV_{RMS}

Amplitude Response



8th Order Linear Phase (Bessel) Filter with $\frac{f_{CLK}}{f} - 3dB = \frac{65}{1}$

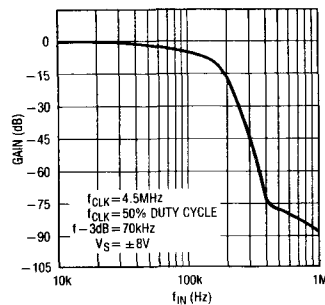


RESISTOR VALUES

R11 = 34.8k	R21 = 34.8k	R31 = 14.3k	R41 = 40.2k
R12 = 10.5k	R22 = 45.3k	R32 = 22.1k	R42 = 39.2k
R13 = 12.7k	R23 = 34.8k	R33 = 24.3k	R43 = 20k
R14 = 20k	R24 = 34.8k	R34 = 13.3k	R44 = 20k

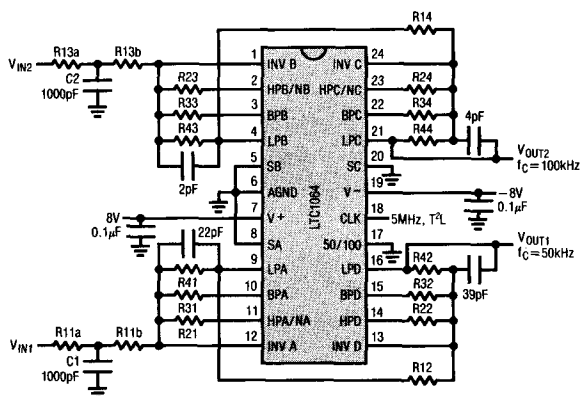
WIDEBAND NOISE = 70µV_{RMS}

Amplitude Response



APPLICATION CIRCUITS

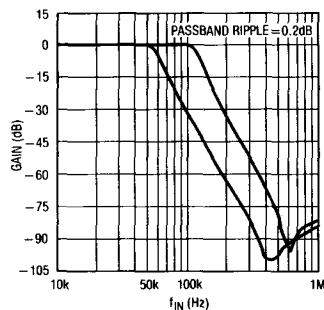
Dual 5th Order Chebyshev Low Pass Filter with 50kHz and 100kHz Cutoff Frequencies



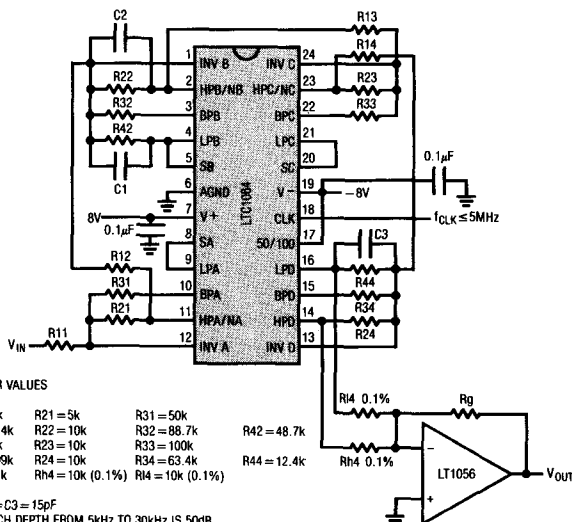
RESISTOR VALUES

R11a = 4.32k	R11b = 27.4k	R21 = 11.8k	R31 = 29.4k	R41 = 10k
R12 = 10.5k	R22 = 20k	R32 = 21.5k	R42 = 31.6k	
R13a = 3k	R13b = 29.4k	R23 = 11.8k	R33 = 29.4k	R43 = 10k
	R14 = 10.5k	R24 = 20k	R34 = 21.6k	R44 = 31.6k

Amplitude Response



Clock Tunable, 30kHz to 90kHz 8th Order Notch Filter Providing Notch Depth in Excess of 60dB

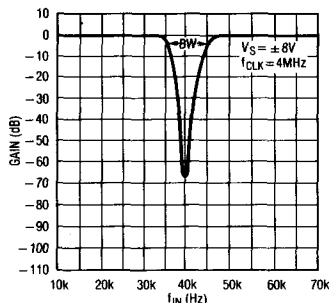


RESISTOR VALUES

R11 = 50k	R21 = 5k	R31 = 50k		
R12 = 15.4k	R22 = 10k	R32 = 88.7k	R42 = 48.7k	
R13 = 10k	R23 = 10k	R33 = 100k		
R14 = 9.09k	R24 = 10k	R34 = 63.4k	R44 = 12.4k	
Rg = 68.1k	Rh4 = 10k (0.1%)	R4 = 10k (0.1%)		

C1 = C2 = C3 = 15pF
 THE NOTCH DEPTH FROM 5kHz TO 30kHz IS 50dB
 WIDEBAND NOISE = 300µV_{RMS}

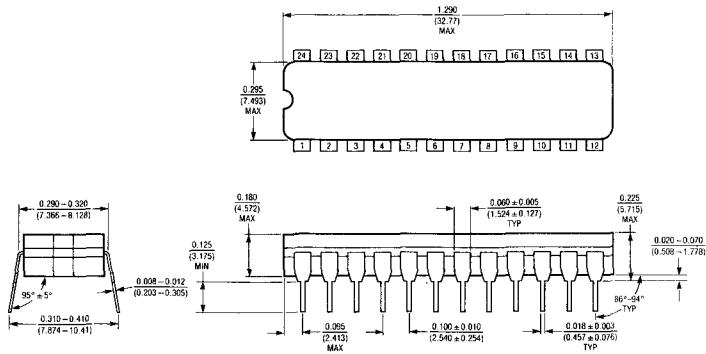
Amplitude Response



7

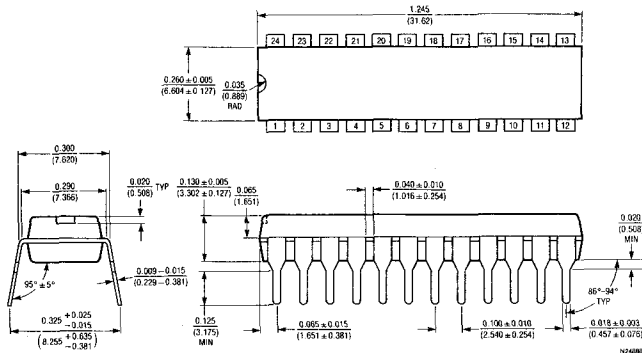
PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

J Package
24-Lead Ceramic DIP



J24088

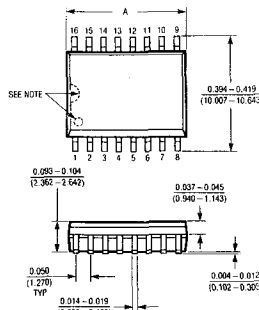
N Package
24-Lead Plastic DIP



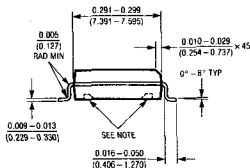
N24088

SO Package
24-Lead Plastic SOIC

NO. OF LEADS	"A" DIM
16	0.595 - 0.615 (15.003 - 15.541)
18	0.450 - 0.470 (11.430 - 11.938)
20	0.499 - 0.515 (12.579 - 13.081)
24	0.600 - 0.615 (15.240 - 15.621)
28	0.700 - 0.715 (17.780 - 18.161)



NOTE:
PIN 1 IDENT. NOTCH ON TOP AND CAVITIES ON THE BOTTOM OF PACKAGE ARE THE MANUFACTURING OPTIONS. THE PART MAY BE SUPPLIED WITH OR WITHOUT ANY OF THE OPTIONS.



SO0091

Low Noise, 8th Order, Clock Sweepable Elliptic Lowpass Filter

FEATURES

- 8th Order Filter in a 14-Pin Package
- No External Components
- 100:1 Clock to Center Ratio
- $150\mu\text{V}_{\text{RMS}}$ Total Wideband Noise
- 0.03% THD or Better
- 50kHz Maximum Corner Frequency
- Operates from $\pm 2.37\text{V}$ to $\pm 8\text{V}$ Power Supplies
- Passband Ripple Guaranteed Over Full Military Temperature Range

APPLICATIONS

- Antialiasing Filters
- Telecom PCM Filters

DESCRIPTION

The LTC1064-1 is an 8th order, clock sweepable elliptic (Cauer) lowpass switched capacitor filter. The passband ripple is typically $\pm 0.15\text{dB}$, and the stopband attenuation at 1.5 times the cutoff frequency is 68dB or more.

An external TTL or CMOS clock programs the value of the filter's cutoff frequency. The clock to cutoff frequency ratio is 100:1.

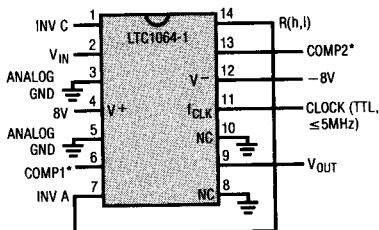
No external components are needed for cutoff frequencies up to 20kHz. For cutoff frequencies over 20kHz two low value capacitors are required to maintain passband flatness. The LTC1064-1 features low wideband noise and low harmonic distortion even for input voltages up to 3V_{RMS} . In fact the LTC1064-1 overall performance competes with equivalent multi op amp RC active realizations.

The LTC1064-1 is available in a 14-pin DIP or 16-pin surface mounted SOL package.

The LTC1064-1 is pin compatible with the LTC1064-2.

TYPICAL APPLICATION

8th Order Clock Sweepable Lowpass Elliptic Antialiasing Filter

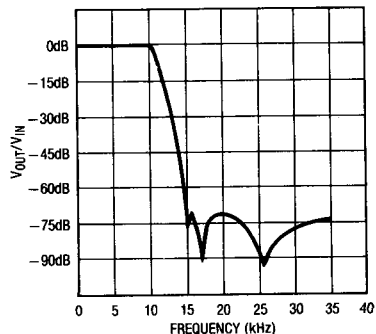


NOTE: THE POWER SUPPLIES SHOULD BE BYPASSED BY A $0.1\mu\text{F}$ CAPACITOR CLOSE TO THE PACKAGE.

FOR SERVO OFFSET NULLING APPLICATIONS, PIN 1 IS THE 2ND STAGE SUMMING JUNCTION.

*FOR CUTOFF FREQUENCY ABOVE 20kHz, USE COMPENSATION CAPACITORS (5pF – 56pF) BETWEEN PINS 13 AND 1 AND 6 AND 7.

Frequency Response

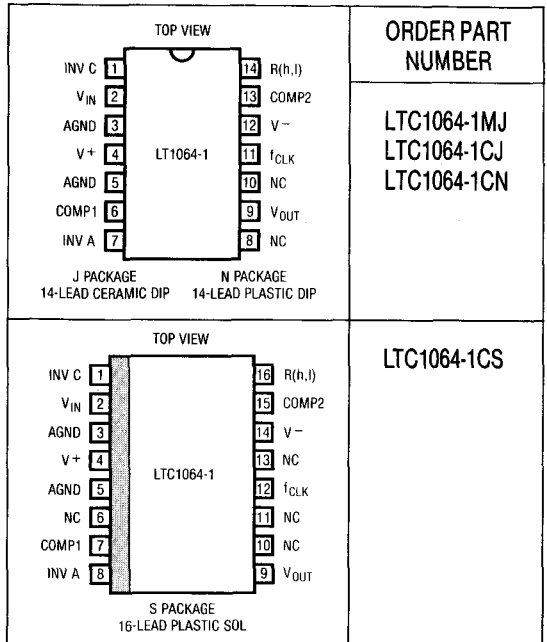


8TH ORDER CLOCK SWEEPABLE LOWPASS ELLIPTIC ANTIALIASING FILTER MAINTAINS, FOR $0.1\text{Hz} \leq f_{\text{CUTOFF}} \leq 10\text{kHz}$, a $\pm 0.15\text{dB}$ PASSBAND RIPPLE AND 72dB STOPBAND ATTENUATION AT $1.50 \times f_{\text{CUTOFF}}$.
 TOTAL WIDEBAND NOISE = $150\mu\text{V}_{\text{RMS}}$, THD = 0.03% FOR $V_{\text{IN}} = 1\text{V}_{\text{RMS}}$.

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V^+ to V^-)	16.5V
Power Dissipation	400mW
Storage Temperature Range	-65°C to 150°C
Lead Temperature (Soldering, 10 sec.)	300°C
Operating Temperature Range	
LTC1064-1M	-55°C to 125°C
LTC1064-1C	-40°C to 85°C

PACKAGE/ORDER INFORMATION



ORDER PART NUMBER

LTC1064-1MJ
LTC1064-1CJ
LTC1064-1CN

LTC1064-1CS

ELECTRICAL CHARACTERISTICS

$V_S = \pm 7.5V$, $f_{CLK} = 1MHz$, $R_I = 10k\Omega$, $C_I = 10pF$, $T_A = 25^\circ$, TTL or CMOS clock input level unless otherwise specified.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Passband Gain, LTC1064-1, 1A	Referenced to 0dB, 1Hz to 0.1 f_C	•		± 0.1	± 0.35	dB
Gain TempCo				0.0002		dB/°C
Passband Edge Frequency, f_C	Referenced to Passband Gain			$10 \pm 1\%$		kHz
Gain at f_C		•	-1.25		0.85	dB
LTC1064-1A		•	-0.75		0.65	dB
-3dB Frequency				10.7		kHz
Passband Ripple (Note 1)	0.1 f_C to 0.85 f_C Referenced to Passband Gain, Measured at 6.25kHz and 8.5kHz	•		± 0.15	± 0.32	dB
LTC1064-1A		•		± 0.1	± 0.19	dB
Ripple TempCo				0.0004		dB/°C
Stopband Attenuation	At 1.5 f_C , Referenced to 0dB	•	66	72		dB
LTC1064-1A		•	68	72		dB
Stopband Attenuation	At 2 f_C , Referenced to 0dB	•	67	72		dB
LTC1064-1A		•	68	72		dB
Input Frequency Range			0		$f_{CLK}/2$	kHz
Output Voltage Swing and	$V_S = \pm 2.37V$	•	-1.0		1	V
Operating Input Voltage Range	$V_S = \pm 5V$	•	-3.2		3.2	V
	$V_S = \pm 7.5V$	•	-5.0		5.2	V

ELECTRICAL CHARACTERISTICS

$V_S = \pm 7.5V$, $f_{CLK} = 1MHz$, $R_I = 10k\Omega$, $C_I = 10pF$, $T_A = 25^\circ$, TTL or CMOS clock input level unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Total Harmonic Distortion	$V_S = \pm 5V$, Input = $1V_{RMS}$ at 1kHz		0.015		%
	$V_S = \pm 7.5V$, Input = $3V_{RMS}$ at 1kHz		0.03		%
Wideband Noise	$V_S = \pm 5V$, Input = GND 1Hz-999kHz		150		μV_{RMS}
	$V_S = \pm 7.5V$, Input = GND 1Hz-999kHz		165		μV_{RMS}
Output DC Offset LTC1064-1	$V_S = \pm 7.5V$, Pin 2 Grounded		50	175	mV
		LTC1064-1A	50	125	mV
Output DC Offset TempCo	$V_S = \pm 5V$		-100		$\mu V/^\circ C$
Input Impedance		10	20		k Ω
Output Impedance	$f_{OUT} = 10kHz$		2		Ω
Output Short Circuit Current	Source/Sink		3/1		mA
Clock Feedthrough			200		μV_{RMS}
Maximum Clock Frequency	50% Duty Cycle, $V_S = \pm 7.5V$			5	MHz
Power Supply Current	$V_S = \pm 2.37V$	●	10	16	mA
	$V_S = \pm 5V$	●	12	18	mA
	$V_S = \pm 8V$	●	16	22	mA
		●		16	22
Power Supply Voltage Range		●	± 2.37	± 8	V

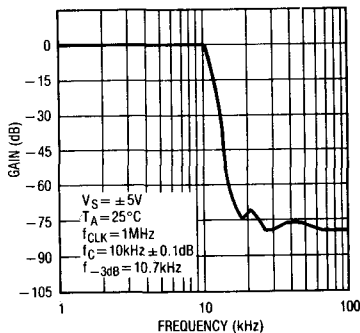
The ● denotes the specifications which apply over the full operating temperature range.

Note 1: For tighter specifications please contact LTC Marketing.

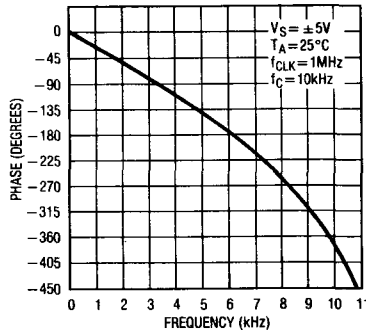
TYPICAL APPLICATIONS

7

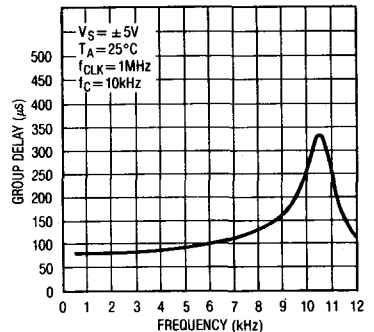
Graph 1. Gain vs Frequency



Graph 2. Phase vs Frequency

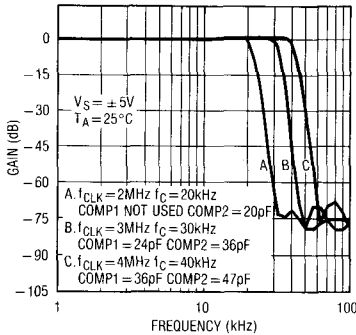


Graph 3. Group Delay

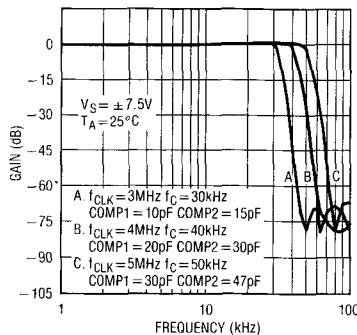


TYPICAL APPLICATIONS

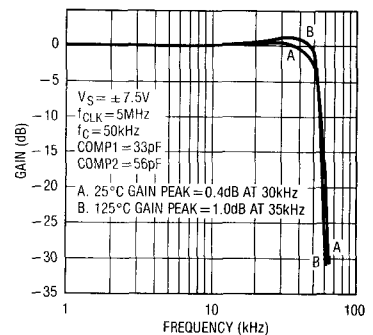
Graph 4. Gain vs Frequency



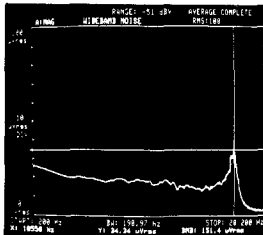
Graph 5. Gain vs Frequency



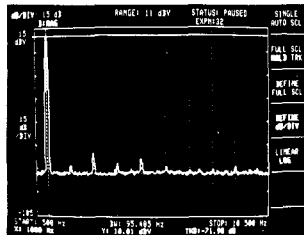
Graph 6. Gain vs Frequency



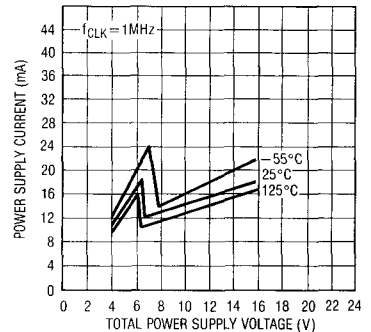
Graph 7. Typical Wideband Noise (151µVRMS) $V_S = \pm 5V$ $T_A = 25^\circ C$
 $f_{CLK} = 1MHz$ $f_C = 10kHz$ Input Grounded



Graph 8. Total Harmonic Distortion (0.025%) $V_S = \pm 7.5V$
 $T_A = 25^\circ C$ $f_{CLK} = 1MHz$ $f_C = 10kHz$
Input = 1kHz at 3VRMS



Graph 9. Power Supply Current vs Power Supply Voltage



PIN DESCRIPTION

Power Supply Pins (4, 12)

The V^+ (pin 4) and V^- (pin 12) should be bypassed with a 0.1µF capacitor to an adequate analog ground. Low noise, non-switching power supplies are recommended. **To avoid latch up when the power supplies exhibit high turn-on transients, a 1N5817 schottky diode should be added from the V^+ and V^- pins to ground, Figure 1.**

Clock Pin (11)

For ±5V supplies the logic threshold level is 1.4V. For ±8V and 0V to 5V supplies the logic threshold levels are

2.2V and 3V respectively. The logic threshold levels vary ±100mV over the full military temperature range. The recommended duty cycle of the input clock is 50% although for clock frequencies below 500kHz the clock "on" time can be as low as 200ns. The maximum clock frequency for ±5V supplies is 4MHz. For ±7V supplies and above, the maximum clock frequency is 5MHz. Do not allow the clock levels to exceed the power supplies. For clock level shifting, see Figure 3.

Analog Ground Pins (3, 5)

For dual supply operation these pins should be connected to a ground plane. For single supply operation both pins

PIN DESCRIPTION

should be tied to one half supply, Figure 2. Also pins 8 and 10, although they are not internally connected should be tied to analog ground or system ground. This improves the clock feedthrough performance.

Connection Pins (7, 14)

A very short connection between pins 14 and 7 is recommended. This connection should be preferably done under the IC package. In a breadboard, use a one inch, or less, shielded coaxial cable; the shield should be grounded. In a PC board, use a one inch trace or less; surround the trace by a ground plane.

Compensation Pins (13 and 1, 6 and 7)

For filter cutoff frequencies higher than 20kHz, in order to minimize the passband ripple, compensation capacitors should be added between pins 6 and 7 (comp1) and pins 1 and 13 (comp2). For comp1 (comp2), add 1pF (1.5pF) mica

capacitor for each kHz increase in cutoff frequency above 20kHz. For more details refer to graphs 4, 5, and 6.

Input, Output Pins (2, 9)

The input pin 2 is connected to an 18k Ω resistor tied to the inverting input of an op amp. Pin 2 is protected against static discharge. The device's output, pin 9, is the output of an op amp which can typically source/sink 3/1mA. Although the internal op amps are unity gain stable, driving long coax cables is not recommended.

When testing the device for noise and distortion, the output, pin 9, should be buffered, Figure 4. **The op amp power supply wire (or trace) should be connected directly to the power source.**

NC Pins (8, 9)

The "no connection" pins preferably should be grounded.

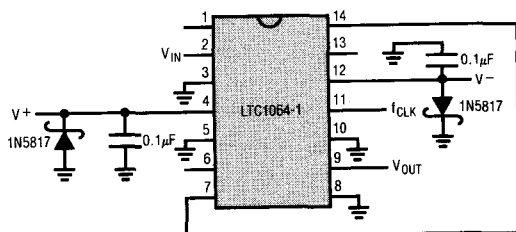


Figure 1. Using Schottky Diodes to Protect the IC from Power Supply Spikes.

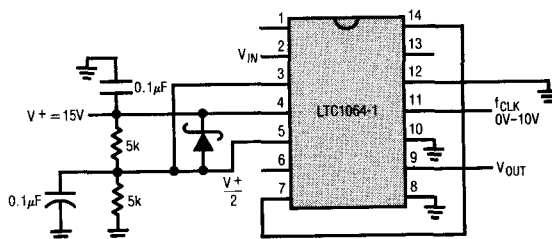


Figure 2. Single Supply Operation. If Fast Power Up or Down Transients are Expected, Use a 1N5817 Schottky Diode Between Pins 4 and 5.

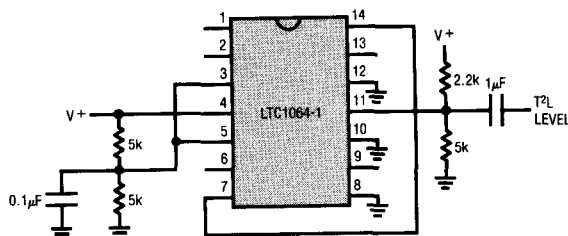
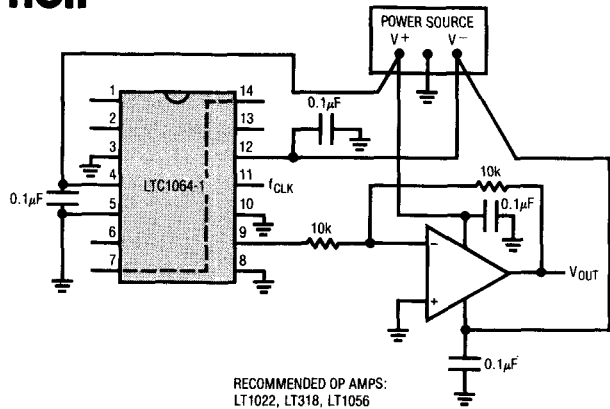


Figure 3. Level Shifting the Input T²L Clock for Single Supply Operation, V⁺ > 6V

PIN DESCRIPTION

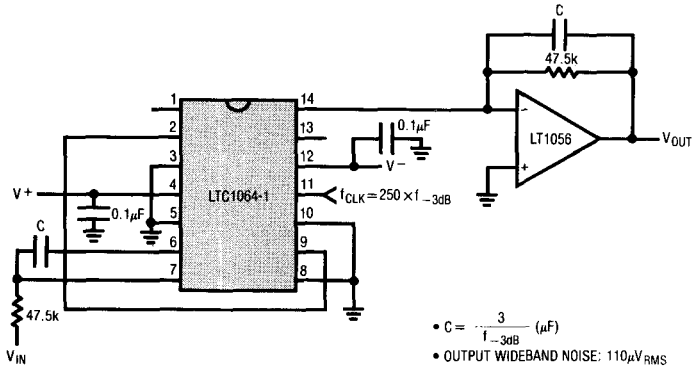


RECOMMENDED OP AMPS:
LT1022, LT318, LT1056

Figure 4. Buffering the Filter Output. The Buffer Op Amp Should Not Share the LTC1064-1 Power Lines.

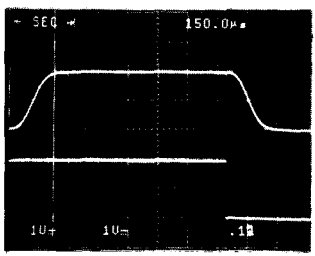
TYPICAL APPLICATIONS

Transitional Elliptic-Bessel 10th Order Lowpass Filter

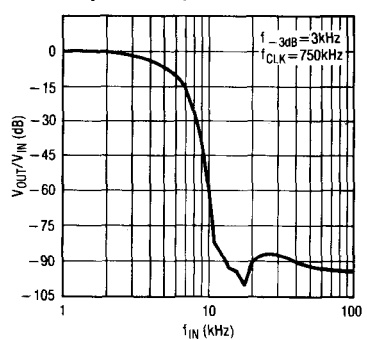


- $C = \frac{3}{f_{-3dB}}$ (μF)
- OUTPUT WIDEBAND NOISE: $110 \mu V_{RMS}$

Transient Response to a 2V Step Input
Horizontal: 0.1ms/Div
Vertical: 1V/Div

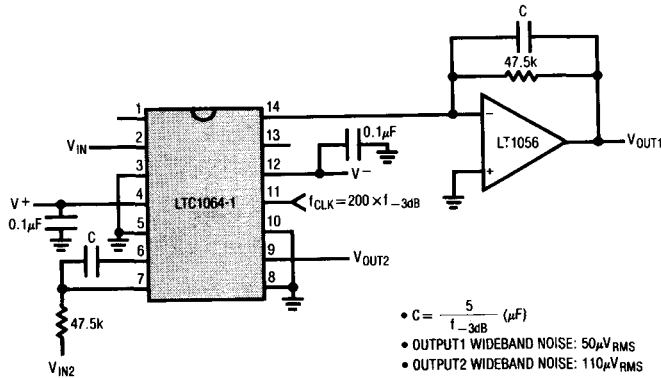


Amplitude Response

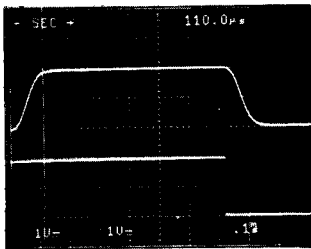


TYPICAL APPLICATIONS

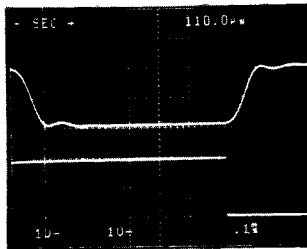
Transitional Elliptic-Bessel Dual 5th Order Lowpass Filter



Transient Response to a 2V Step Input
 Horizontal: 0.1ms/Div
 Vertical: 1V/Div

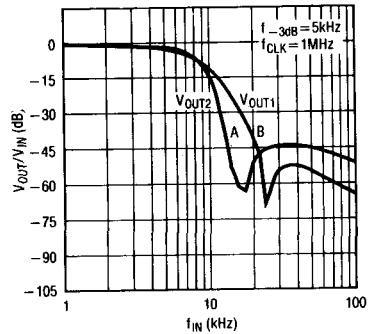


VOUT2

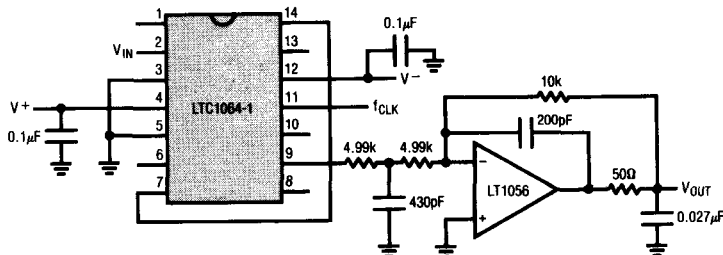


VOUT1

Amplitude Response

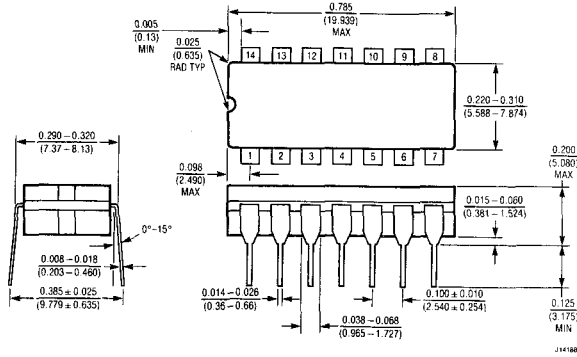


Adding an Output Buffer-Filter to Eliminate Any Clock Feedthrough Over a 10:1 Clock Range, for $f_C = 2kHz$ to $20kHz$

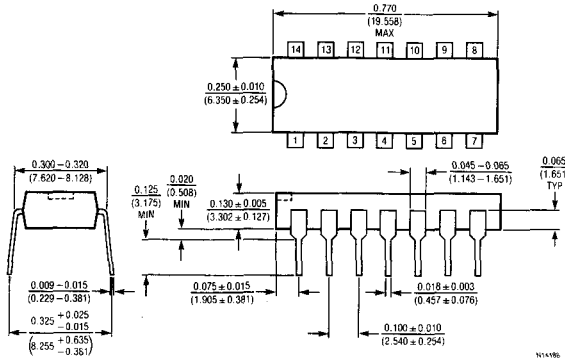


PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

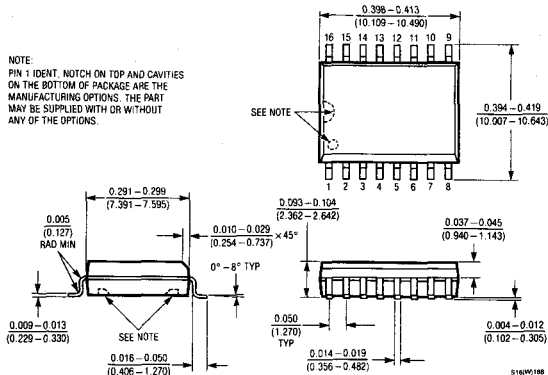
J Package
14-Lead Ceramic DIP



N Package
14-Lead Plastic DIP



S Package
16-Lead Plastic SOL



SECTION 8—INSTRUMENTATION AMPLIFIERS

8

SECTION 8—INSTRUMENTATION AMPLIFIERS

INDEX	8-2
PROPRIETARY PRODUCTS	
<i>LTC1043, Dual Instrumentation Switched-Capacitor Building Block</i>	11-15
<i>LTC1100, Precision, Single Supply, Instrumentation Amplifier (Fixed Gain = 100)</i>	13-35
<i>LT1101, Precision, Micropower, Single Supply Instrumentation Amplifier (Fixed Gain = 10 or 100)</i>	13-36
<i>LT1102, High Speed, JFET Input Instrumentation Amplifier (Fixed Gain = 10 or 100)</i>	13-48

SECTION 9—DATA CONVERSION

SECTION 9—DATA CONVERSION

INDEX	9-2
SELECTION GUIDE	9-3
PROPRIETARY PRODUCTS	
<i>LTC1090, Single Chip 10-Bit Data Acquisition System</i>	9-5
<i>LTC1091, 1-Channel, 10-Bit Serial I/O Data Acquisition System</i>	9-29
<i>LTC1092, 2-Channel, 10-Bit Serial I/O Data Acquisition System</i>	9-29
<i>LTC1093, 6-Channel, 10-Bit Serial I/O Data Acquisition System</i>	9-29
<i>LTC1094, 8-Channel, 10-Bit Serial I/O Data Acquisition System</i>	9-29
<i>LTC1095, Complete 10-Bit Data Acquisition System with On Board Reference</i>	9-57
<i>LTC1099, High Speed 8-Bit A/D Converter with Built-In Sample-and-Hold</i>	9-81
<i>LTC1290, Single Chip 12-Bit Data Acquisition System</i>	13-62
<i>LTC1291, 1-Channel, 12-Bit Serial I/O Data Acquisition System</i>	13-70
<i>LTC1292, 2-Channel, 12-Bit Serial I/O Data Acquisition System</i>	13-70
<i>LTC1293, 6-Channel, 12-Bit Serial I/O Data Acquisition System</i>	13-70
<i>LTC1294, 8-Channel, 12-Bit Serial I/O Data Acquisition System</i>	13-70
SECOND SOURCE PRODUCTS	
LF198A/LF398A, Precision Sample and Hold Amplifier	9-97
LF198/LF398, Precision Sample and Hold Amplifier	9-97
LF398S8, Precision Sample and Hold Amplifier	9-113

MILITARY AND COMMERCIAL

PART NUMBER	DESCRIPTION	RESOLUTION	TOTAL UNADJUSTED ERROR	CONVERSION TIME	MAXIMUM SUPPLY CURRENT	PACKAGES AVAILABLE	IMPORTANT FEATURES
LTC1090C, M	10 Bit Serial I/O, Analog to Digital Converter with 8 Channel Multiplexer. Full Duplex Serial Interface.	10 Bits	$\pm 1/2\text{LSB}$ (LTC1090A) Over Full Temperature Range	22 μs	2.5mA	J, N, S	10 Bit A to D with Built In 8 Channel Analog MUX and Sample/Hold. Compatible with All Microprocessors with Serial Ports. Software Configurable Bipolar or Unipolar Operation. Full Duplex Serial I/O.
LTC1091C, M	10 Bit Serial I/O, Analog to Digital Converter with 2 Channel Analog Multiplexer	10 Bits	$\pm 1/2\text{LSB}$ (LTC1091A) Over Full Temperature Range	20 μs	3.5mA	J8, N8	10 Bit A to D with Built In 2 Channel Analog MUX and Sample/Hold. Compatible with All Microprocessors with Serial Ports. Unipolar Operation.
LTC1092C, M	10 Bit, 8 Pin Analog to Digital Converter with Serial Output	10 Bits	$\pm 1/2\text{LSB}$ (LTC1092A) Over Full Temperature Range	20 μs	2.5mA	J8, N8	Separate Reference Pin Allows Reduced Span (Down to 200mV) Operation. Unipolar A to D Conversions are Performed on a Differential Input Pair. Compatible with All Microprocessors with Serial Ports.
LTC1093C, M	10 Bit Serial I/O, Analog to Digital Converter with 6 Channel Multiplexer	10 Bits	$\pm 1/2\text{LSB}$ (LTC1093A) Over Full Temperature Range	20 μs	2.5mA	J, N	10 Bit A to D with Built In 6 Channel Analog MUX and Sample/Hold. Compatible with All Microprocessors with Serial Ports. Software Configurable Bipolar or Unipolar Operation. Half Duplex Serial I/O.
LTC1094C, M	10 Bit Serial I/O, Analog to Digital Converter System with 8 Channel Multiplexer	10 Bits	$\pm 1/2\text{LSB}$ (LTC1094A) Over Full Temperature Range	20 μs	2.5mA	J, N	10 Bit A to D with Built In 8 Channel Analog MUX and Sample/Hold. Compatible with All Microprocessors with Serial Ports. Software Configurable Bipolar or Unipolar Operation. Half Duplex Serial I/O.
LTC1099C, M	8 Bit, 2 μs Analog to Digital Converter with Built In Sample-and-Hold	8 Bits	$\pm 1\text{LSB}$ Over Full Temperature Range	2 μs	15mA	J, N, S	Built In S/H Allows Direct Conversion of 5Vp-p Signals up to 167kHz. Pin Compatible with ADC0820 and AD7820.
LTC1290C, M	12 Bit, Serial I/O, Analog to Digital Converter with 8 Channel Multiplexer. Full Duplex Serial Interface.	12 Bits	$\pm 1\text{LSB}$ Over Full Temperature Range	13 μs	5mA	J, N, S	12 Bit ADC with Built In 8 Channel Analog MUX and Sample/Hold. Compatible with All Microprocessors with Serial Ports. Software Configurable Bipolar or Unipolar Operation. Full Duplex Serial I/O.

REFER TO TABLE OF CONTENTS
FOR REVISED DATA LOCATION

NOTES

FEATURES

- Software Programmable Features:
 - Unipolar/Bipolar Conversions
 - 4 Differential/8 Single Ended Inputs
 - MSB or LSB First Data Sequence
 - Variable Data Word Length
- Built-In Sample and Hold
- Single Supply 5V, 10V or $\pm 5V$ Operation
- Direct 4 Wire Interface to Most MPU Serial Ports and All MPU Parallel Ports
- 30kHz Maximum Throughput Rate

KEY SPECIFICATIONS

- | | |
|-------------------------------------|-------------------------|
| ■ Resolution | 10 Bits |
| ■ Total Unadjusted Error (LTC1090A) | $\pm 1/2\text{LSB}$ Max |
| ■ Conversion Time | 22 μs |
| ■ Supply Current | 2.5mA Max, 1.0mA Typ |

DESCRIPTION

The LTC1090 is a data acquisition component which contains a serial I/O successive approximation A/D converter. It uses LTCMOST™ switched capacitor technology to perform either 10-bit unipolar, or 9-bit plus sign bipolar A/D conversions. The 8-channel input multiplexer can be configured for either single ended or differential inputs (or combinations thereof). An on-chip sample and hold is included for all single ended input channels.

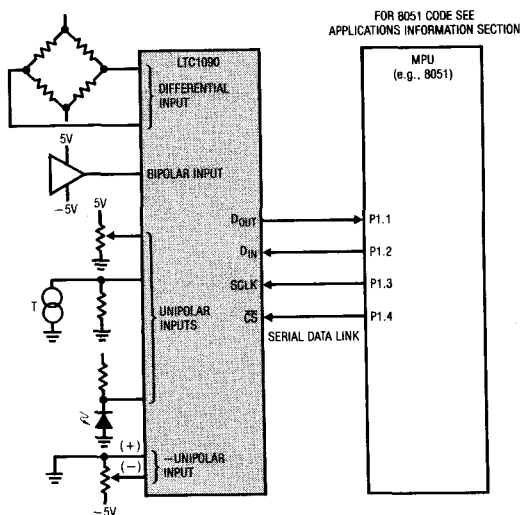
The serial I/O is designed to be compatible with industry standard full duplex serial interfaces. It allows either MSB or LSB first data and automatically provides 2's complement output coding in the bipolar mode. The output data word can be programmed for a length of 8, 10, 12 or 16 bits. This allows easy interface to shift registers and a variety of processors.

The LTC1090A is specified with total unadjusted error (including the effects of offset, linearity and gain errors) less than $\pm 0.5\text{LSB}$.

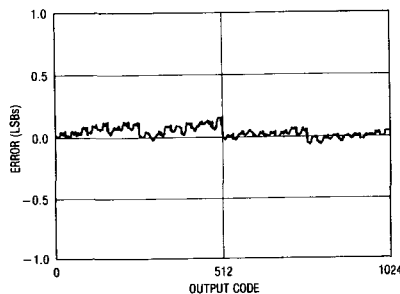
The LTC1090 is specified with offset and linearity less than $\pm 0.5\text{LSB}$ but with a gain error limit of $\pm 2\text{LSB}$ for applications where gain is adjustable or less critical.

LTCMOST is a trademark of Linear Technology Corp.

TYPICAL APPLICATION



Linearity Plot

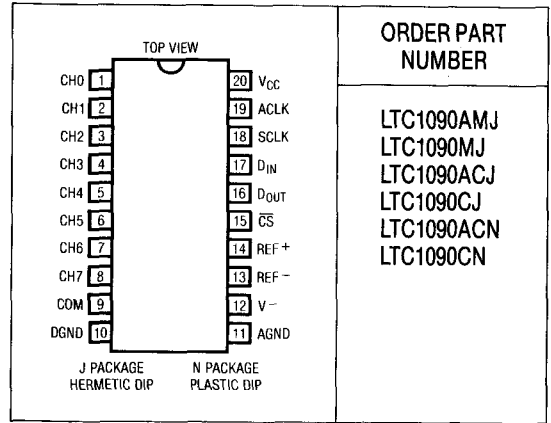


ABSOLUTE MAXIMUM RATINGS

PACKAGE/ORDER INFORMATION

(Notes 1 and 2)

Supply Voltage (V_{CC}) to GND or V^-	12V
Negative Supply Voltage (V^-)	-6V to GND
Voltage	
Analog and Reference	
Inputs	(V^-) - 0.3V to $V_{CC} + 0.3V$
Digital Inputs	- 0.3V to 12V
Digital Outputs	- 0.3V to $V_{CC} + 0.3V$
Power Dissipation	500mW
Operating Temperature Range	
LTC1090AC, LTC1090C	- 40°C to 85°C
LTC1090AM, LTC1090M	- 55°C to 125°C
Storage Temperature Range	- 65°C to 150°C
Lead Temperature (Soldering, 10 sec.)	300°C



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LTC1090/LTC1090A		UNITS
			MIN	MAX	
V_{CC}	Positive Supply Voltage	$V^- = 0V$	4.5	10	V
V^-	Negative Supply Voltage	$V_{CC} = 5V$	-5.5	0	V
f_{SCLK}	Shift Clock Frequency	$V_{CC} = 5V$	0	1.0	MHz
f_{ACLK}	A/D Clock Frequency	$V_{CC} = 5V$	f_{SCLK}	2.0	MHz
t_{CYC}	Total Cycle Time	See Operating Sequence	10 SCLK + 48 ACLK		Cycles
t_{hCS}	Hold Time, \overline{CS} Low After Last SCLK1	$V_{CC} = 5V$	0		ns
t_{hDI}	Hold Time, D_{IN} After SCLK1	$V_{CC} = 5V$	150		ns
t_{suCS}	Setup Time \overline{CS} Before Clocking in First Address Bit (Note 9)	$V_{CC} = 5V$	2 ACLK Cycles + 1 μ s		
t_{suDI}	Setup Time, D_{IN} Stable Before SCLK1	$V_{CC} = 5V$	400		ns
t_{WHACK}	ACLK High Time	$V_{CC} = 5V$	127		ns
t_{WLACK}	ACLK Low Time	$V_{CC} = 5V$	200		ns
t_{WHCS}	\overline{CS} High Time During Conversion	$V_{CC} = 5V$	44		ACLK Cycles

CONVERTER AND MULTIPLEXER CHARACTERISTICS (Note 3)

PARAMETER	CONDITIONS	LTC1090A		LTC1090		UNITS	
		MIN	TYP	MIN	TYP		MAX
Offset Error	(Note 4)	•				± 0.5	LSB
Linearity Error	(Notes 4 and 5)	•				± 0.5	LSB
Gain Error	(Note 4)	•				± 0.5	LSB
Total Unadjusted Error	$V_{REF} = 5.000V$ (Notes 4 and 6)	•				± 0.5	LSB

CONVERTER AND MULTIPLEXER CHARACTERISTICS (Note 3)

PARAMETER	CONDITIONS	LTC1090A		LTC1090		UNITS	
		MIN	TYP	MAX	MIN		TYP
Reference Input Resistance			10		10	k Ω	
Analog and REF Input Range	(Note 7)			$(V^-) - 0.05V$ to $V_{CC} + 0.05V$		V	
On Channel Leakage Current (Note 8)	On Channel = 5V Off Channel = 0V	•		1		1	μ A
	On Channel = 0V Off Channel = 5V	•		-1		-1	μ A
Off Channel Leakage Current (Note 8)	On Channel = 5V Off Channel = 0V	•		-1		-1	μ A
	On Channel = 0V Off Channel = 5V	•		1		1	μ A

AC CHARACTERISTICS (Note 3)

SYMBOL	PARAMETER	CONDITIONS	LTC1090/LTC1090A			UNITS
			MIN	TYP	MAX	
t_{ACC}	Delay Time From \overline{CS}_1 to D_{OUT} Data Valid	(Note 9)		2		ACLK Cycles
t_{SMPL}	Analog Input Sample Time	See Operating Sequence		5		SCLK Cycles
t_{CONV}	Conversion Time	See Operating Sequence		44		ACLK Cycles
t_{dDO}	Delay Time, $SCLK_1$ to D_{OUT} Data Valid	See Test Circuits	•	250	450	ns
t_{dis}	Delay Time, \overline{CS}_1 to D_{OUT} Hi-Z	See Test Circuits	•	140	300	ns
t_{en}	Delay Time, 2nd CLK_1 to D_{OUT} Enabled	See Test Circuits	•	150	400	ns
t_{hDO}	Time Output Data Remains Valid After SCLK1			50		ns
t_f	D_{OUT} Fall Time	See Test Circuits	•	90	300	ns
t_r	D_{OUT} Rise Time	See Test Circuits	•	60	300	ns
C_{IN}	Input Capacitance	Analog Inputs On Channel		65		pF
		Off Channel		5		pF
		Digital Inputs		5		pF

DIGITAL AND DC ELECTRICAL CHARACTERISTICS (Note 3)

SYMBOL	PARAMETER	CONDITIONS	LTC1090/LTC1090A			UNITS
			MIN	TYP	MAX	
V_{IH}	High Level Input Voltage	$V_{CC} = 5.25V$	•	2.0		V
V_{IL}	Low Level Input Voltage	$V_{CC} = 4.75V$	•		0.8	V
I_{IH}	High Level Input Current	$V_{IN} = V_{CC}$	•		2.5	μ A
I_{IL}	Low Level Input Current	$V_{IN} = 0V$	•		-2.5	μ A
V_{OH}	High Level Output Voltage	$V_{CC} = 4.75V, I_O = 10\mu A$	•	4.7		V
		$I_O = 360\mu A$	•	2.4	4.0	V
V_{OL}	Low Level Output Voltage	$V_{CC} = 4.75V, I_O = 1.8mA$	•		0.4	V
I_{OZ}	Hi-Z Output Leakage	$V_{OUT} = V_{CC}, \overline{CS}$ High	•		3	μ A
		$V_{OUT} = 0V, \overline{CS}$ High	•		-3	μ A
I_{SOURCE}	Output Source Current	$V_{OUT} = 0V$		-10		mA
I_{SINK}	Output Sink Current	$V_{OUT} = V_{CC}$		10		mA
I_{CC}	Positive Supply Current	\overline{CS} High, REF ⁺ Open	•	1.0	2.5	mA
I_{REF}	Reference Current	$V_{REF} = 5V$	•	0.5	1.0	mA
I^-	Negative Supply Current	\overline{CS} High, $V^- = -5V$	•	1	50	μ A

Note 1: Absolute maximum ratings are those values beyond which the life of a device may be impaired.

Note 2: All voltage values are with respect to ground with DGND, AGND and REF⁻ wired together (unless otherwise noted).

Note 3: $V_{CC} = 5V$, $V_{REF+} = 5V$, $V_{REF-} = 0V$, $V^- = 0V$ for unipolar mode and $-5V$ for bipolar mode, $ACLK = 2.0\text{ MHz}$, $SCLK = 0.5\text{ MHz}$ unless otherwise specified. The ● indicates specs which apply over the full operating temperature range; all other limits and typicals $T_A = 25^\circ\text{C}$.

Note 4: These specs apply for both unipolar and bipolar modes. In bipolar mode, one LSB is equal to the bipolar input span ($2V_{REF}$) divided by 1024. For example, when $V_{REF} = 5V$, $1\text{ LSB (bipolar)} = 2(5V)/1024 = 9.77\text{ mV}$.

Note 5: Linearity error is specified between the actual end points of the A/D transfer curve.

Note 6: Total unadjusted error includes offset, gain, linearity, multiplexer and hold step errors.

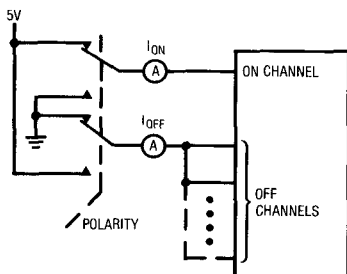
Note 7: Two on-chip diodes are tied to each reference and analog input which will conduct for reference or analog input voltages one diode drop below V^- or one diode drop above V_{CC} . Be careful during testing at low V_{CC} levels (4.5V), as high level reference or analog inputs (5V) can cause this input diode to conduct, especially at elevated temperatures, and cause errors for inputs near full-scale. This spec allows 50mV forward bias of either diode. This means that as long as the reference or analog input does not exceed the supply voltage by more than 50mV, the output code will be correct. To achieve an absolute 0V to 5V input voltage range will therefore require a minimum supply voltage of 4.950V over initial tolerance, temperature variations and loading.

Note 8: Channel leakage current is measured after the channel selection.

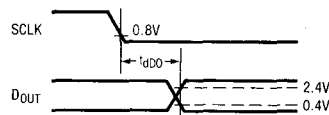
Note 9: To minimize errors caused by noise at the chip select input, the internal circuitry waits for two ACLK falling edges after a chip select falling edge is detected before responding to control input signals. Therefore, no attempt should be made to clock an address in or data out until the minimum chip select setup time has elapsed.

TEST CIRCUITS

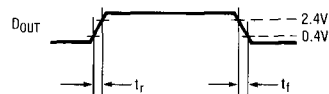
On and Off Channel Leakage Current



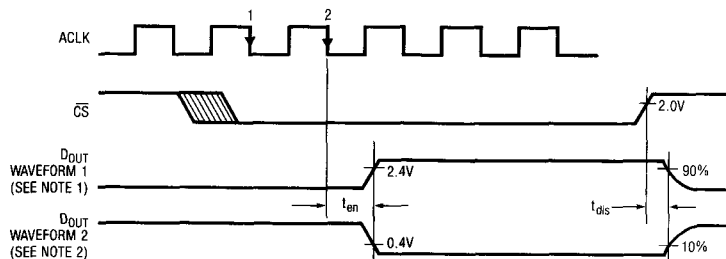
Voltage Waveforms for D_{OUT} Delay Time, t_{dDQ}



Voltage Waveform for D_{OUT} Rise and Fall Times, t_r, t_f



Voltage Waveforms for t_{en} and t_{dis}

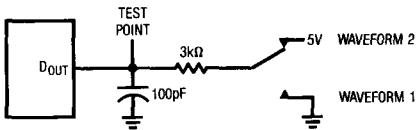


NOTE 1: WAVEFORM 1 IS FOR AN OUTPUT WITH INTERNAL CONDITIONS SUCH THAT THE OUTPUT IS HIGH UNLESS DISABLED BY THE OUTPUT CONTROL.

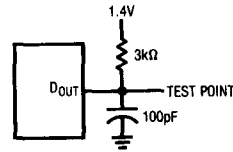
NOTE 2: WAVEFORM 2 IS FOR AN OUTPUT WITH INTERNAL CONDITIONS SUCH THAT THE OUTPUT IS LOW UNLESS DISABLED BY THE OUTPUT CONTROL.

TEST CIRCUITS

Load Circuit for t_{dis} and t_{en}



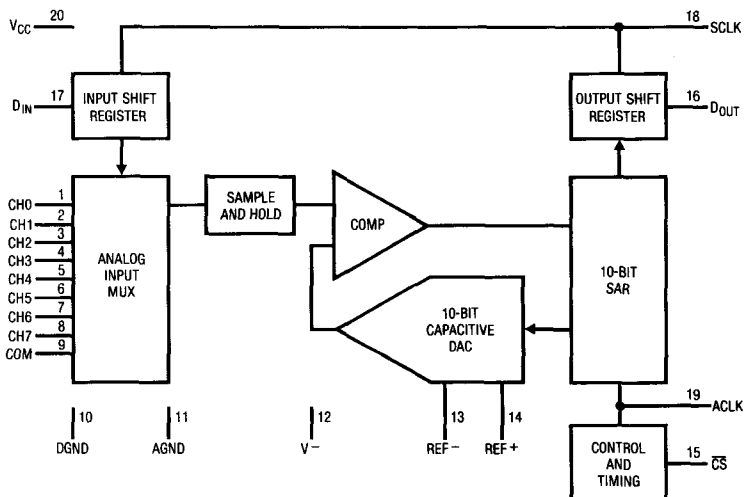
Load Circuit for t_{dpo} , t_r , and t_f



PIN FUNCTIONS

#	PIN	FUNCTION	DESCRIPTION
1-8	CH0-CH7	Analog Inputs	The analog inputs must be free of noise with respect to AGND.
9	COM	Common	The common pin defines the zero reference point for all single ended inputs. It must be free of noise and is usually tied to the analog ground plane.
10	DGND	Digital Ground	This is the ground for the internal logic. Tie to the ground plane.
11	AGND	Analog Ground	AGND should be tied directly to the analog ground plane.
12	V ⁻	Negative Supply	Tie V ⁻ to most negative potential in the circuit. (Ground in single supply applications.)
13, 14	REF ⁻ , REF ⁺	Reference Inputs	The reference inputs must be kept free of noise with respect to AGND
15	CS	Chip Select Input	A logic low on this input enables data transfer.
16	D _{OUT}	Digital Data Output	The A/D conversion result is shifted out of this output.
17	D _{IN}	Data Input	The A/D configuration word is shifted into this input.
18	SCLK	Shift Clock	This clock synchronizes the serial data transfer.
19	ACLK	A/D Conversion Clock	This clock controls the A/D conversion process.
20	V _{CC}	Positive Supply	This supply must be kept free of noise and ripple by bypassing directly to the analog ground plane.

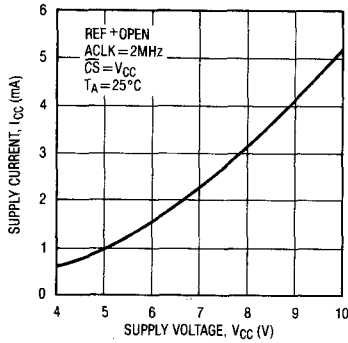
BLOCK DIAGRAM



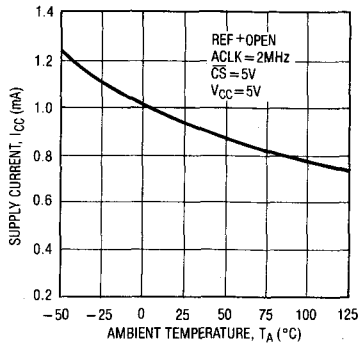
9

TYPICAL PERFORMANCE CHARACTERISTICS

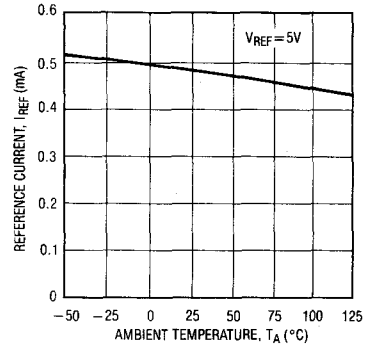
Supply Current vs Supply Voltage



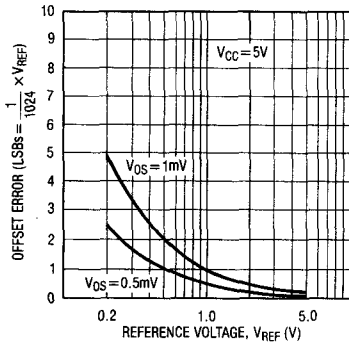
Supply Current vs Temperature



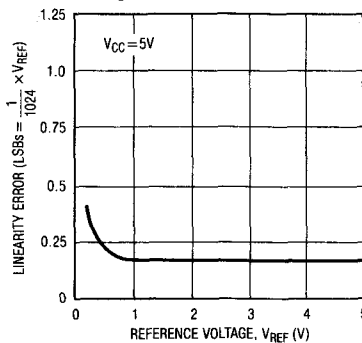
Reference Current vs Temperature



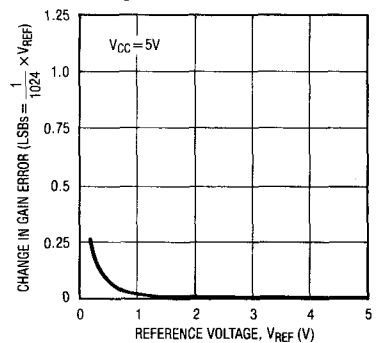
Unadjusted Offset Error vs Reference Voltage



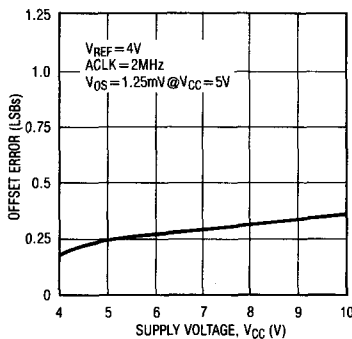
Linearity Error vs Reference Voltage



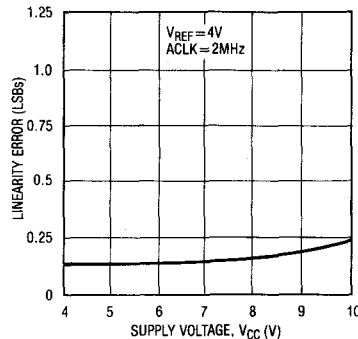
Change in Gain Error vs Reference Voltage



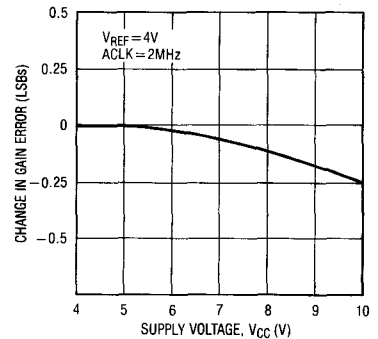
Offset Error vs Supply Voltage



Linearity Error vs Supply Voltage

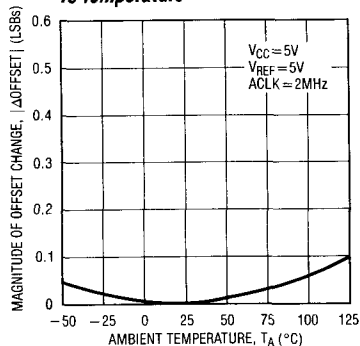


Change in Gain Error vs Supply Voltage

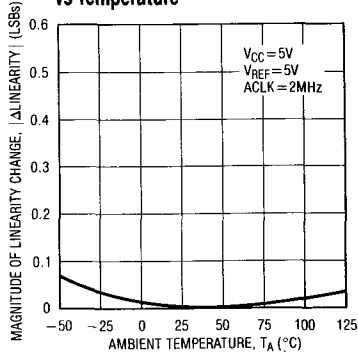


TYPICAL PERFORMANCE CHARACTERISTICS

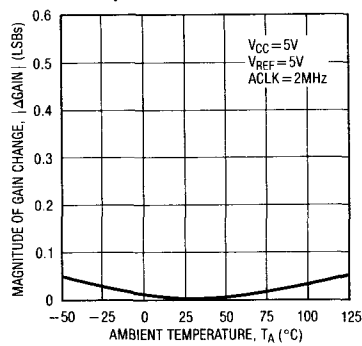
Change in Offset Error vs Temperature



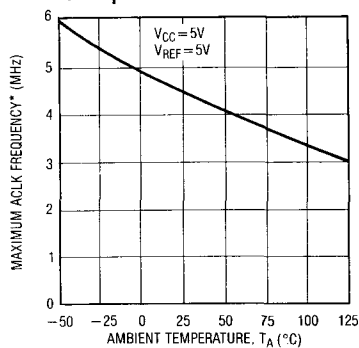
Change in Linearity Error vs Temperature



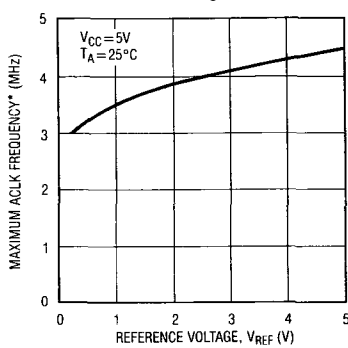
Change in Gain Error vs Temperature



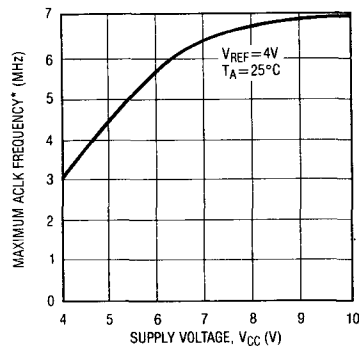
Maximum Conversion Clock Rate vs Temperature



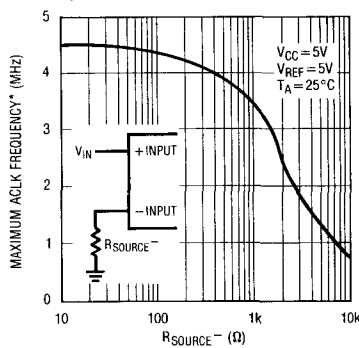
Maximum Conversion Clock Rate vs Reference Voltage



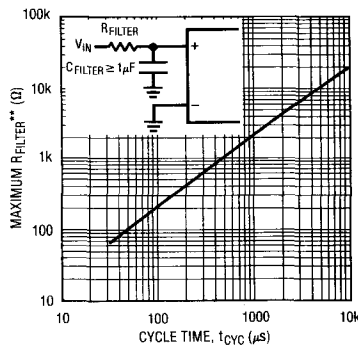
Maximum Conversion Clock Rate vs Supply Voltage



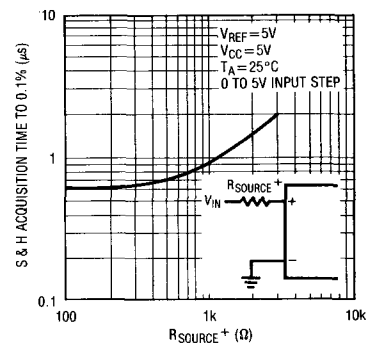
Maximum Conversion Clock Rate vs Source Resistance



Maximum Filter Resistor vs Cycle Time



Sample and Hold Acquisition Time vs Source Resistance

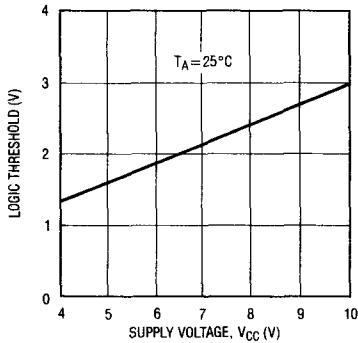


*MAXIMUM ACLK FREQUENCY REPRESENTS THE ACLK FREQUENCY AT WHICH A 0.1LSB SHIFT IN THE ERROR AT ANY CODE TRANSITION FROM ITS 2MHz VALUE IS FIRST DETECTED.

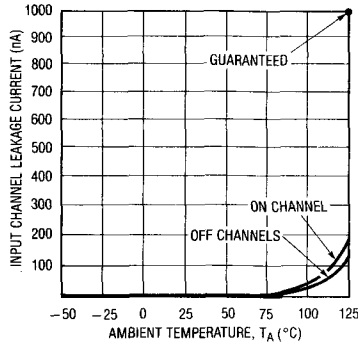
**MAXIMUM R_{FILTER} REPRESENTS THE FILTER RESISTOR VALUE AT WHICH A 0.1LSB CHANGE IN FULL-SCALE ERROR FROM ITS VALUE AT R_{FILTER} = 0 IS FIRST DETECTED.

TYPICAL PERFORMANCE CHARACTERISTICS

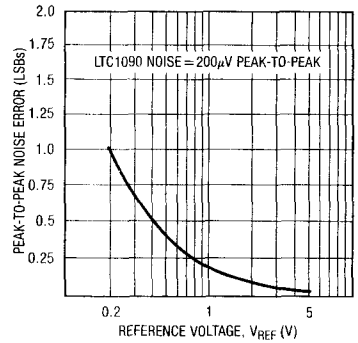
Digital Input Logic Threshold vs Supply Voltage



Input Channel Leakage Current vs Temperature



Noise Error vs Reference Voltage



APPLICATIONS INFORMATION

The LTC1090 is a data acquisition component which contains the following functional blocks:

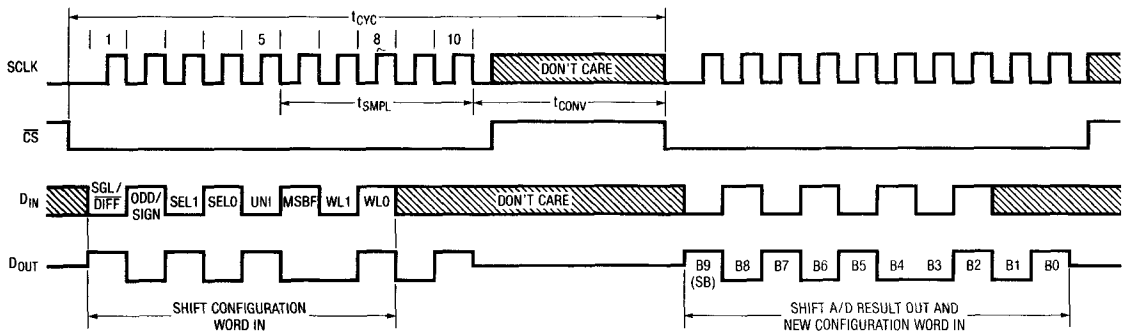
1. 10-bit successive approximation capacitive A/D converter
2. Analog multiplexer (MUX)
3. Sample and hold (S/H)
4. Synchronous, full duplex serial interface
5. Control and timing logic

DIGITAL CONSIDERATIONS

1. Serial Interface

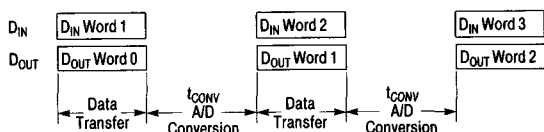
The LTC1090 communicates with microprocessors and other external circuitry via a synchronous, full duplex, four wire serial interface (see Operating Sequence). The shift clock (SCLK) synchronizes the data transfer with each bit being transmitted on the falling SCLK edge and captured on the rising SCLK edge in both transmitting and receiving systems. The data is transmitted and received simultaneously (full duplex).

Operating Sequence
(Example: Differential Inputs (CH3-CH2), Bipolar, MSB First and 10-Bit Word Length)



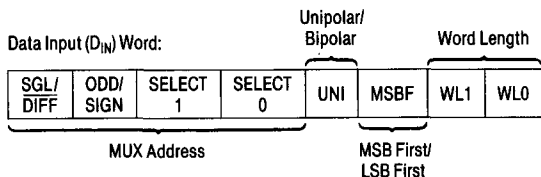
APPLICATIONS INFORMATION

Data transfer is initiated by a falling chip select (\overline{CS}) signal. After the falling \overline{CS} is recognized, an 8-bit input word is shifted into the D_{IN} input which configures the LTC1090 for the next conversion. Simultaneously, the result of the previous conversion is output on the D_{OUT} line. At the end of the data exchange the requested conversion begins and \overline{CS} should be brought high. After t_{CONV} , the conversion is complete and the results will be available on the next data transfer cycle. As shown below, the result of a conversion is delayed by one \overline{CS} cycle from the input word requesting it.



2. Input Data Word

The LTC1090 8-bit input data word is clocked into the D_{IN} input on the first eight rising SCLK edges after chip select is recognized. Further inputs on the D_{IN} pin are then ignored until the next \overline{CS} cycle. The eight bits of the input word are defined as follows:



Multiplexer (MUX) Address

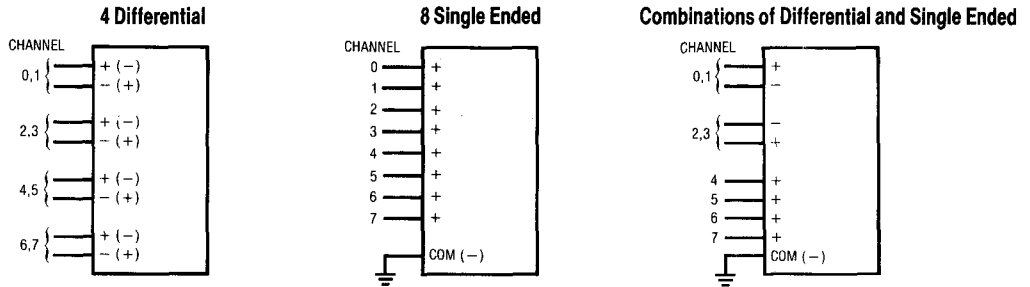
The first four bits of the input word assign the MUX configuration for the requested conversion. For a given channel selection, the converter will measure the voltage between the two channels indicated by the + and - signs in the selected row of Table 1. Note that in differential mode ($SGL/DIFF=0$) measurements are limited to four adjacent input pairs with either polarity. In single ended mode, all input channels are measured with respect to COM. Figure 1 shows some examples of multiplexer assignments.

Table 1. Multiplexer Channel Selection

MUX ADDRESS			DIFFERENTIAL CHANNEL SELECTION									
SGL/DIFF	ODD/SIGN	SELECT	1	0	0	1	2	3	4	5	6	7
0	0	0	0	0	+	-						
0	0	0	1				+	-				
0	0	1	0						+	-		
0	0	1	1								+	-
0	1	0	0	-	+							
0	1	0	1			-	+					
0	1	1	0					-	+			
0	1	1	1								-	+

MUX ADDRESS			SINGLE ENDED CHANNEL SELECTION										
SGL/DIFF	ODD/SIGN	SELECT	1	0	0	1	2	3	4	5	6	7	COM
1	0	0	0	0	+								-
1	0	0	1			+							-
1	0	1	0					+					-
1	0	1	1								+		-
1	1	0	0			+							-
1	1	0	1					+					-
1	1	1	0							+			-
1	1	1	1									+	-

APPLICATIONS INFORMATION



Changing the MUX Assignment "On the Fly"

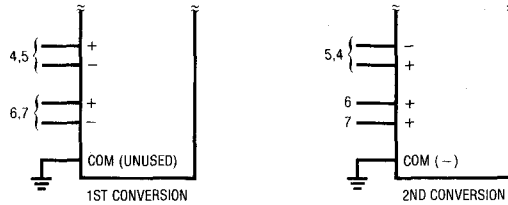


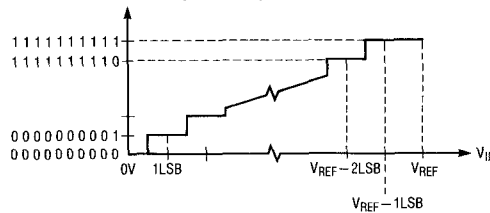
Figure 1. Examples of Multiplexer Options on the LTC1090

Unipolar/Bipolar (UNI)

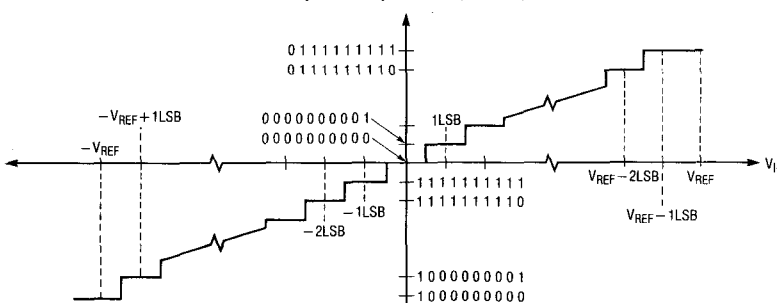
The fifth input bit (UNI) determines whether the conversion will be unipolar or bipolar. When UNI is a logical one, a unipolar conversion will be performed on the selected in-

put voltage. When UNI is a logical zero, a bipolar conversion will result. The input span and code assignment for each conversion type are shown in the figures below.

Unipolar Output Code (UNI = 1)



Bipolar Output Code (UNI = 0)



APPLICATIONS INFORMATION

Unipolar Transfer Curve (UNI = 1)

OUTPUT CODE	INPUT VOLTAGE	INPUT VOLTAGE ($V_{REF} = 5V$)
1111111111	$V_{REF} - 1LSB$	4.9951V
1111111110	$V_{REF} - 2LSB$	4.9902V
⋮	⋮	⋮
0000000001	1LSB	0.0049V
0000000000	0V	0V

Bipolar Transfer Curve (UNI = 0)

OUTPUT CODE	INPUT VOLTAGE	INPUT VOLTAGE ($V_{REF} = 5V$)
0111111111	$V_{REF} - 1LSB$	4.9902V
0111111110	$V_{REF} - 2LSB$	4.9805V
⋮	⋮	⋮
0000000001	1LSB	0.0098V
0000000000	0V	0V
1111111111	-1LSB	-0.0098V
1111111110	-2LSB	-0.0195V
⋮	⋮	⋮
1000000001	$-(V_{REF}) + 1LSB$	-4.9902V
1000000000	$-(V_{REF})$	-5.000V

MSB First/LSB First Format (MSBF)

The output data of the LTC1090 is programmed for MSB first or LSB first sequence using the MSBF bit. For MSB first output data the input word clocked to the LTC1090 should always contain a logical one in the sixth bit location (MSBF bit). Likewise for LSB first output data, the input word clocked to the LTC1090 should always contain a zero in the MSBF bit location. The MSBF bit in a given D_{IN} word will control the order of the next D_{OUT} word. The MSBF bit affects only the order of the output data word. The order of the input word is unaffected by this bit.

MSBF	OUTPUT FORMAT
0	LSB First
1	MSB First

Word Length (WL1, WL0)

The last two bits of the input word (WL1 and WL0) program the output data word length of the LTC1090. Word lengths of 8, 10, 12 or 16 bits can be selected according to the following table. The WL1 and WL0 bits in a given D_{IN} word

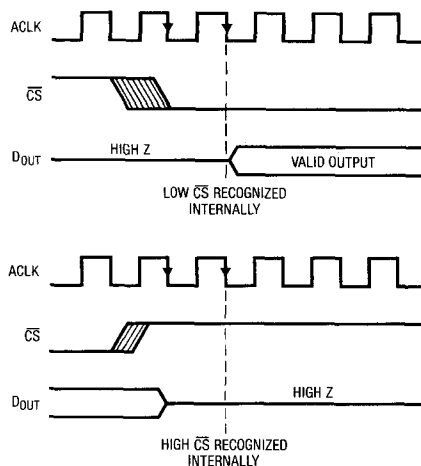
control the length of the present, not the next, D_{OUT} word. **WL1 and WL0 are never “don’t cares”** and must be set for the correct D_{OUT} word length even when a “dummy” D_{IN} word is sent. On any transfer cycle, the word length should be made equal to the number of SCLK cycles sent by the MPU.

WL1	WL0	OUTPUT WORD LENGTH
0	0	8 Bits
0	1	10 Bits
1	0	12 Bits
1	1	16 Bits

Figure 2 shows how the data output (D_{OUT}) timing can be controlled with word length selection and MSB/LSB first format selection.

3. Deglitcher

A deglitching circuit has been added to the Chip Select input of the LTC1090 to minimize the effects of errors caused by noise on that input. This circuit ignores changes in state on the \overline{CS} input that are shorter in duration than 1 ACLK cycle. After a change of state on the \overline{CS} input, the LTC1090 waits for two falling edges of the ACLK before recognizing a valid chip select. One indication of \overline{CS} low recognition is the D_{OUT} line becoming active (leaving the Hi-Z state). Note that the deglitching applies to both the rising and falling \overline{CS} edges.



APPLICATIONS INFORMATION

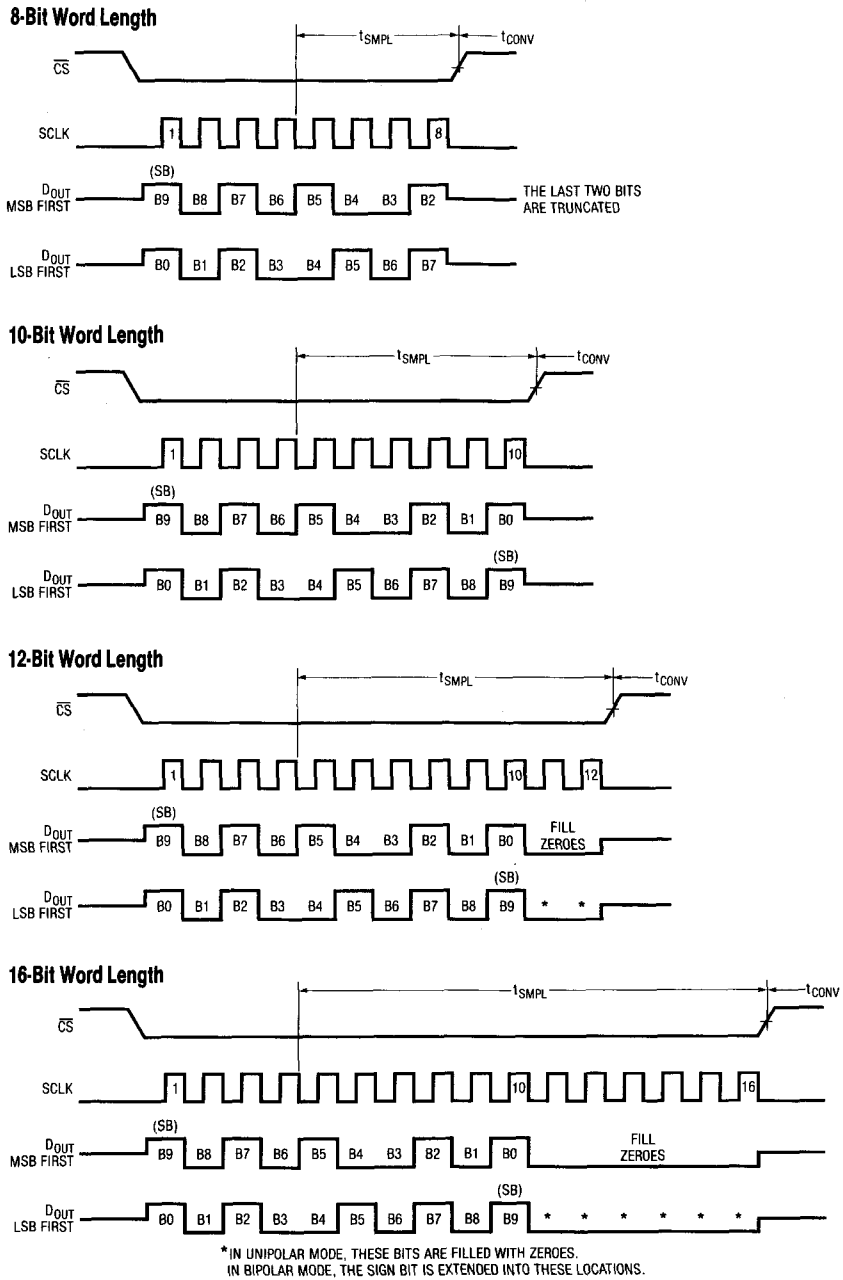


Figure 2. Data Output (D_{OUT}) Timing with Different Word Lengths

APPLICATIONS INFORMATION

4. \overline{CS} Low During Conversion

In the normal mode of operation, \overline{CS} is brought high during the conversion time (see Figure 3). The serial port ignores any SCLK activity while \overline{CS} is high. The LTC1090 will also operate with \overline{CS} low during the conversion. In this mode, SCLK must remain low during the conversion as shown in Figure 4. After the conversion is complete, the D_{OUT} line

will become active with the first output bit. Then the data transfer can begin as normal.

5. Microprocessor Interfaces

The LTC1090 can interface directly (without external hardware) to most popular microprocessor (MPU) synchronous

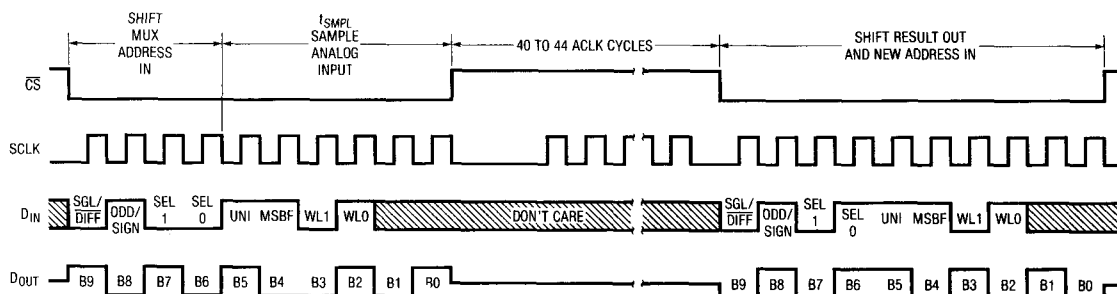


Figure 3. \overline{CS} High During Conversion

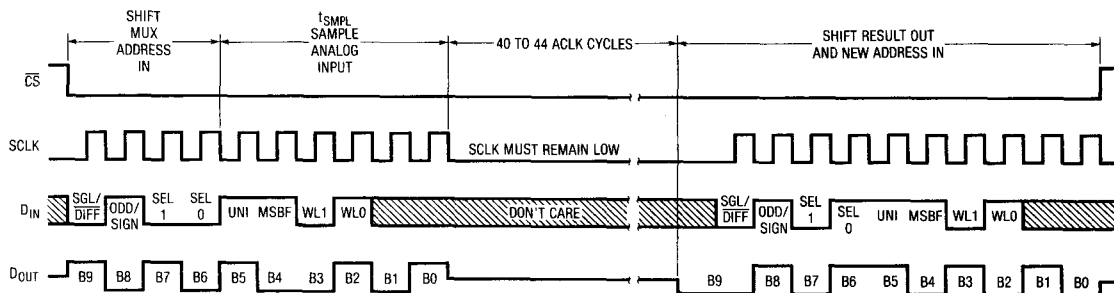


Figure 4. \overline{CS} Low During Conversion

APPLICATIONS INFORMATION

serial formats (see Table 2). If an MPU without a serial interface is used, then 4 of the MPU's parallel port lines can be programmed to form the serial link to the LTC1090. Included here are three serial interface examples and one example showing a parallel port programmed to form the serial interface.

Table 2. Microprocessors with Hardware Serial Interfaces Compatible with the LTC1090**

PART NUMBER	TYPE OF INTERFACE
Motorola	
MC6805S2, S3	SPI
MC68HC11	SPI
MC68HC05	SPI
RCA	
CDP68HC05	SPI
Hitachi	
HD6305	SCI Synchronous
HD63705	SCI Synchronous
HD6301	SCI Synchronous
HD63701	SCI Synchronous
HD6303	SCI Synchronous
National Semiconductor	
COP400 Family	MICROWIRE†
COP800 Family	MICROWIRE/PLUS†
NS8050U	MICROWIRE/PLUS
HPC16000 Family	MICROWIRE/PLUS
Texas Instruments	
TMS7002	Serial Port
TMS7042	Serial Port
TMS70C02	Serial Port
TMS70C42	Serial Port
TMS32011*	Serial Port
TMS32020*	Serial Port

*Requires external hardware

**Contact factory for interface information for processors not on this list

†MICROWIRE and MICROWIRE/PLUS are trademarks of National Semiconductor Corp.

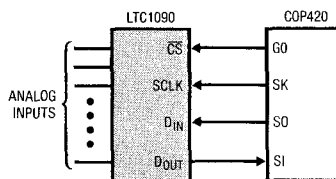
Serial Port Microprocessors

Most synchronous serial formats contain a shift clock (SCLK) and two data lines, one for transmitting and one for receiving. In most cases data bits are transmitted on the falling edge of the clock (SCLK) and captured on the rising edge. However, serial port formats vary among MPU manufacturers as to the smallest number of bits that can be sent in one group (e.g., 4-bit, 8-bit or 16-bit transfers). They also vary as to the order in which the bits are transmitted (LSB or MSB first). The following examples show how the LTC1090 accommodates these differences.

National MICROWIRE (COP420)

The COP420 transfers data MSB first and in 4-bit increments (nibbles). This is easily accommodated by setting the LTC1090 to MSB first format and 12-bit word length. The data output word is then received by the COP420 in three 4-bit blocks with the final two unused bits filled with zeroes by the LTC1090.

Hardware and Software Interface to National Semiconductor COP420 Processor



DOUT from LTC1090 stored in COP420 RAM

	MSB†	
Location A	B9 B8 B7 B6	first 4 bits
Location A + 1	B5 B4 B3 B2	second 4 bits
	LSB	
Location A + 2	B1 B0 0 0	third 4 bits

†B9 is MSB in unipolar or sign bit in bipolar

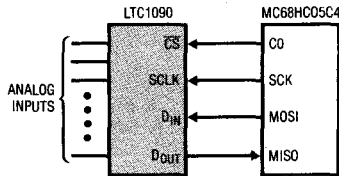
MNEMONIC	DESCRIPTION
LEI	Enable SIO
SC	Set Carry flag
OGI	G0 is set to 0 (CS goes low)
LDD	Load first 4 bits of D _{IN} to ACC
XAS	Swap ACC with SIO reg. Starts SK Clk
LDD	Load 2nd 4 bits of D _{IN} to ACC
NOP	Timing
XAS	Swap first 4 bits from A/D with ACC. SK continues.
XIS	Put first 4 bits in RAM (location A)
NOP	Timing
XAS	Swap 2nd 4 bits from A/D with ACC. SK continues.
XIS	Put 2nd 4 bits in RAM (location A + 1)
RC	Clear Carry
NOP	Timing
XAS	Swap 3rd 4 bits from A/D with ACC. SK off
XIS	Put 3rd 4 bits in RAM (location A + 2)
OGI	G0 is set to 1 (CS goes high)
LEI	Disable SIO

APPLICATIONS INFORMATION

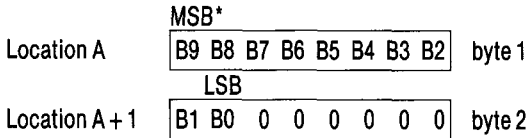
Motorola SPI (MC68HC05C4)

The MC68HC05C4 transfers data MSB first and in 8-bit increments. Programming the LTC1090 for MSB first format and 16-bit word length allows the 10-bit data output to be received by the MPU as two 8-bit bytes with the final 6 unused bits filled with zeroes by the LTC1090.

Hardware and Software Interface to Motorola MC68HC05C4 Processor



D_{OUT} from LTC1090 stored in MC68HC05C4 RAM



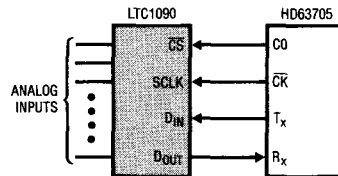
*B9 is MSB in unipolar or sign bit in bipolar

MNEMONIC	DESCRIPTION
BCLR n	C0 is cleared (\overline{CS} goes low)
LDA	Load D _{IN} for LTC1090 into ACC
STA	Load D _{IN} from ACC to SPI data reg. Start SCK
↓	
NOP	8 NOPs for timing
↓	
LDA	Load contents of SPI status reg. into ACC
LDA	Load LTC1090 D _{OUT} from SPI data reg. into ACC (byte 1)
STA	Load LTC1090 D _{OUT} into RAM (location A)
STA	Start next SPI cycle
↓	
NOP	6 NOPs for timing
↓	
BSET n	C0 is set (\overline{CS} goes high)
LDA	Load contents of SPI status reg. into ACC
LDA	Load LTC1090 D _{OUT} from SPI data reg. into ACC (byte 2)
STA	Load LTC1090 D _{OUT} into RAM (location A + 1)

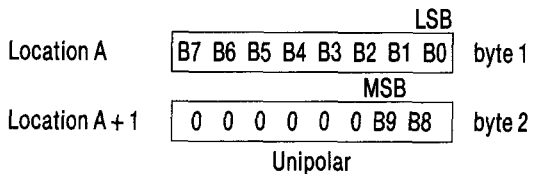
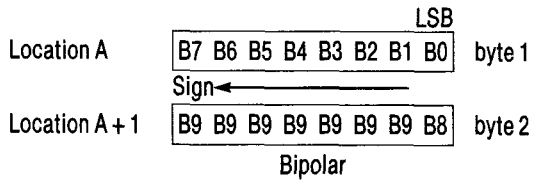
Hitachi Synchronous SCI (HD63705)

The HD63705 transfers serial data in 8-bit increments, LSB first. To accommodate this, the LTC1090 is programmed for 16-bit word length and LSB first format. The 10-bit output data is received by the processor as two 8-bit bytes, LSB first. The LTC1090 fills the final 6 unused bits (after the MSB) with zeroes in unipolar mode and with the sign bit in bipolar mode.

Hardware and Software Interface to Hitachi HD63705 Processor



D_{OUT} from LTC1090 stored in HD63705 RAM



MNEMONIC	DESCRIPTION
LDA	Load D _{IN} word for LTC1090 into ACC from RAM
BCLR n	C0 cleared (\overline{CS} goes low)
STA	Load D _{IN} word for LTC1090 into SCI data reg from ACC and start clocking data (LSB first)
↓	
NOP	6 NOPs for timing
↓	
LDA	Load contents of SCI data reg into ACC (byte 1)
STA	Start next SCI cycle
STA	Load LTC1090 D _{OUT} word into RAM (Location A)
NOP	Timing
BSET n	C0 set (\overline{CS} goes high).
LDA	Load contents of SCI data reg into ACC (byte 2)
STA	Load LTC1090 D _{OUT} word into RAM (Location A + 1)

APPLICATIONS INFORMATION

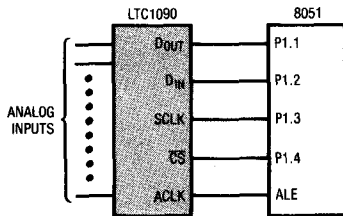
Parallel Port Microprocessors

When interfacing the LTC1090 to an MPU which has a parallel port, the serial signals are created on the port with software. Three MPU port lines are programmed to create the \overline{CS} , SCLK and D_{IN} signals for the LTC1090. A fourth port line reads the D_{OUT} line. An example is made of the Intel 8051/8052/80C252 family.

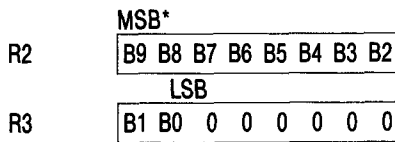
Intel 8051

To interface to the 8051, the LTC1090 is programmed for MSB first format and 10-bit word length. The 8051 generates \overline{CS} , SCLK and D_{IN} on three port lines and reads D_{OUT} on the fourth.

Hardware and Software Interface to Intel 8051 Processor



D_{OUT} from LTC1090 stored in 8051 RAM



*B9 is MSB in unipolar or sign bit in bipolar

8051 Code

MNEMONIC	DESCRIPTION
MOV P1,#02H	Initialize port 1 (bit 1 is made an input)
CLR P1.3	SCLK goes low
SETB P1.4	\overline{CS} goes high
CONTINUE: MOV A,#0DH	D_{IN} word for the LTC1090 is placed in ACC.
	\overline{CS} goes low
	Load counter
LOOP: CLR P1.4	Delay for deglitcher
MOV R4,#08	Read data bit into carry
NOP	Rotate data bit into ACC
MOV C,P1.1	Output D_{IN} bit to LTC1090
RLC A	SCLK goes high
MOV P1.2,C	SCLK goes low
SETB P1.3	Next bit
CLR P1.3	Store MSBs in R2
DJNZ R4, LOOP	Read data bit into carry
MOV R2,A	Clear ACC
MOV C,P1.1	Rotate data bit into ACC
CLR A	SCLK goes high
RLC A	SCLK goes low
SETB P1.3	Read data bit into carry
CLR P1.3	Rotate right into ACC
MOV C,P1.1	Rotate right into ACC
RRC A	Store LSBs in R3
RRC A	SCLK goes high
MOV R3,A	SCLK goes low
SETB P1.3	\overline{CS} goes high
CLR P1.3	\overline{CS} goes low
SETB P1.4	Load counter
MOV R5,#07H	Delay for LTC1090 to perform conversion
DJNZ R5, DELAY	Delay for LTC1090 to perform conversion
DELAY: AJMP CONTINUE	Repeat program

6. Sharing the Serial Interface

The LTC1090 can share the same 3 wire serial interface with other peripheral components or other LTC1090s (see Figure 5). In this case, the \overline{CS} signals decide which LTC1090 is being addressed by the MPU.

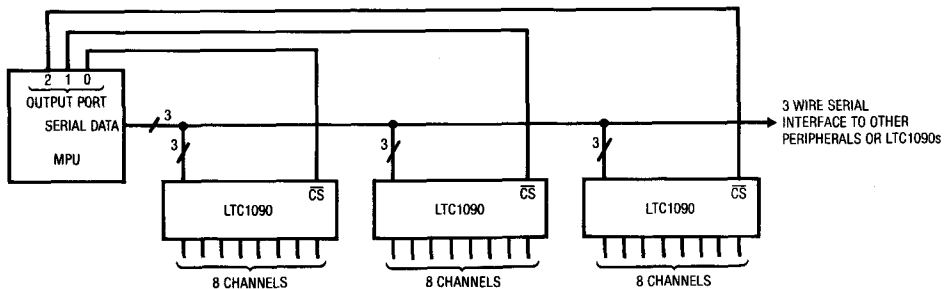


Figure 5. Several LTC1090s Sharing One 3 Wire Serial Interface

APPLICATIONS INFORMATION

ANALOG CONSIDERATIONS

1. Grounding

The LTC1090 should be used with an analog ground plane and single point grounding techniques.

Pin 11 (AGND) should be tied directly to this ground plane.

Pin 10 (DGND) can also be tied directly to this ground plane because minimal digital noise is generated within the chip itself.

Pin 20 (V_{CC}) should be bypassed to the ground plane with a $4.7\mu\text{F}$ tantalum with leads as short as possible. Pin 12 (V^-) should be bypassed with a $0.1\mu\text{F}$ ceramic disk. For single supply applications, V^- can be tied to the ground plane.

It is also recommended that pin 13 (REF^-) and pin 9 (COM) be tied directly to the ground plane. All analog inputs should be referenced directly to the single point ground. Digital inputs and outputs should be shielded from and/or routed away from the reference and analog circuitry.

Figure 6 shows an example of an ideal ground plane design for a two sided board. Of course this much ground plane will not always be possible, but users should strive to get as close to this ideal as possible.

2. Bypassing

For good performance, V_{CC} must be free of noise and ripple. Any changes in the V_{CC} voltage with respect to analog ground during a conversion cycle can induce errors or noise in the output code. V_{CC} noise and ripple can be kept below 1mV by bypassing the V_{CC} pin directly to the analog ground plane with a $4.7\mu\text{F}$ tantalum with leads as short as possible. Figures 7 and 8 show the effects of good and poor V_{CC} bypassing.

3. Analog Inputs

Because of the capacitive redistribution A/D conversion techniques used, the analog inputs of the LTC1090 have capacitive switching input current spikes. These current spikes settle quickly and do not cause a problem.

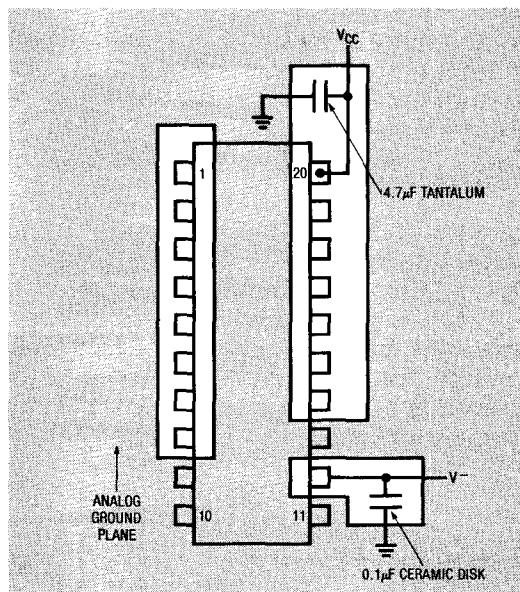


Figure 6. Example Ground Plane for the LTC1090

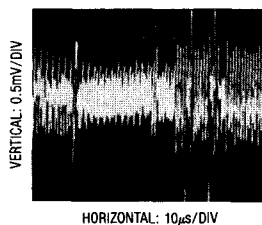


Figure 7. Poor V_{CC} Bypassing. Noise and Ripple can Cause A/D Errors

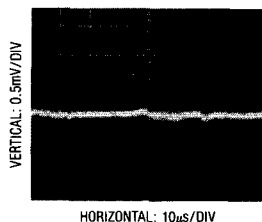


Figure 8. Good V_{CC} Bypassing Keeps Noise and Ripple on V_{CC} Below 1mV

APPLICATIONS INFORMATION

However, if large source resistances are used or if slow settling op amps drive the inputs, care must be taken to insure that the transients caused by the current spikes settle completely before the conversion begins.

Source Resistance

The analog inputs of the LTC1090 look like a 60pF capacitor (C_{IN}) in series with a 500Ω resistor (R_{ON}) as shown in Figure 9. C_{IN} gets switched between the selected “+” and “-” inputs once during each conversion cycle. Large external source resistors and capacitances will slow the settling of the inputs. It is important that the overall RC time constants be short enough to allow the analog inputs to completely settle within the allowed time.

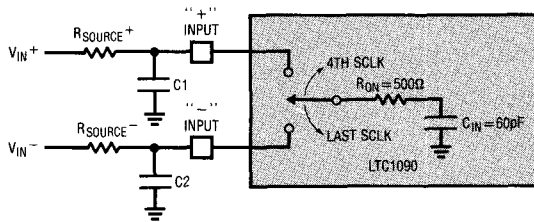


Figure 9. Analog Input Equivalent Circuit

“+” Input Settling

This input capacitor is switched onto the “+” input during the sample phase (t_{SMPL} , see Figure 10). The sample phase starts at the 4th SCLK cycle and lasts until the falling edge of the last SCLK (the 8th, 10th, 12th or 16th SCLK cycle depending on the selected word length). The voltage on the “+” input must settle completely within this sample time. Minimizing $R_{SOURCE+}$ and $C1$ will improve the input settling time. If large “+” input source resistance must be used, the sample time can be increased by using a slower SCLK frequency or selecting a longer word length. With the minimum possible sample time of 4μs, $R_{SOURCE+} < 2k$ and $C1 < 20pF$ will provide adequate settling.

“-” Input Settling

At the end of the sample phase the input capacitor switches to the “-” input and the conversion starts (see Figure 10). During the conversion, the “+” input voltage is effectively “held” by the sample and hold and will not affect the conversion result. However, it is critical that the “-” input voltage be free of noise and settle completely during the first four ACLK cycles of the conversion time. Minimizing $R_{SOURCE-}$ and $C2$ will improve settling time. If large “-” input source resistance must be used, the time allowed for settling can be extended by using a slower ACLK frequency. At the maximum ACLK rate of 2MHz, $R_{SOURCE-} < 1k\Omega$ and $C2 < 20pF$ will provide adequate settling.

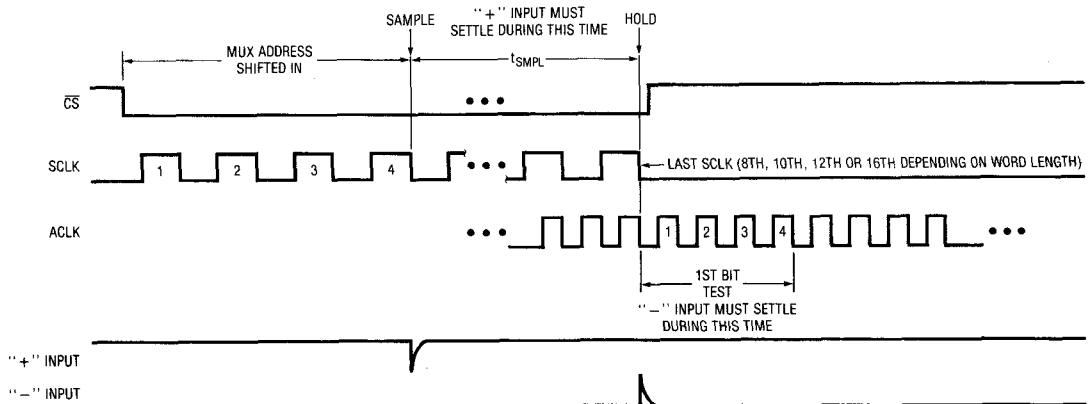


Figure 10. “+” and “-” Input Settling Windows

APPLICATIONS INFORMATION

Input Op Amps

When driving the analog inputs with an op amp it is important that the op amp settle within the allowed time (see Figure 10). Again, the “+” and “-” input sampling times can be extended as described above to accommodate slower op amps. Most op amps including the LT1006 and LT1013 single supply op amps can be made to settle well even with the minimum settling windows of $4\mu\text{s}$ (“+” input) and $2\mu\text{s}$ (“-” input) which occur at the maximum clock rates ($\text{ACLK} = 2\text{MHz}$ and $\text{SCLK} = 1\text{MHz}$). Figures 11 and 12 show examples of adequate and poor op amp settling.

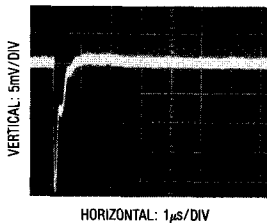


Figure 11. Adequate Settling of Op Amp Driving Analog Input

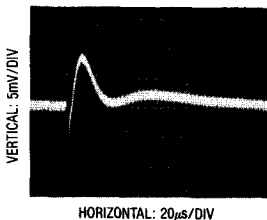


Figure 12. Poor Op Amp Settling can Cause A/D Errors

RC Input Filtering

It is possible to filter the inputs with an RC network as shown in Figure 13. For large values of C_F (e.g., $1\mu\text{F}$), the capacitive input switching currents are averaged into a net DC current. Therefore, a filter should be chosen with a small resistor and large capacitor to prevent DC drops across the resistor. The magnitude of the DC current is approximately $I_{DC} = 60\text{pF} \times V_{IN}/t_{CYC}$ and is roughly proportional to V_{IN} . When running at the minimum cycle time of $33\mu\text{s}$, the input current equals $9\mu\text{A}$ at $V_{IN} = 5\text{V}$. In this case, a filter resistor of 50Ω will cause 0.1LSB of full-scale error. If a larger filter resistor must be used, errors can be elim-

inated by increasing the cycle time as shown in the typical curve of Maximum Filter Resistor vs Cycle Time.

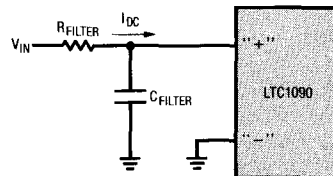


Figure 13. RC Input Filtering

Input Leakage Current

Input leakage currents can also create errors if the source resistance gets too large. For instance, the maximum input leakage specification of $1\mu\text{A}$ (at 125°C) flowing through a source resistance of $1\text{k}\Omega$ will cause a voltage drop of 1mV or 0.2LSB. This error will be much reduced at lower temperatures because leakage drops rapidly (see typical curve of Input Channel Leakage Current vs Temperature).

Noise Coupling into Inputs

High source resistance input signals ($>5000\Omega$) are more sensitive to coupling from external sources. It is preferable to use channels near the center of the package (i.e., CH2-CH7) for signals which have the highest output resistance because they are essentially shielded by the pins on the package ends (DGND and CH0). Grounding any unused inputs (especially the end pin, CH0) will also reduce outside coupling into high source resistances.

4. Sample and Hold

Single Ended Inputs

The LTC1090 provides a built-in sample and hold (S&H) function for all signals acquired in the single ended mode (COM pin grounded). This sample and hold allows the LTC1090 to convert rapidly varying signals (see typical curve of S&H Acquisition Time vs Source Resistance). The input voltage is sampled during the t_{SMPL} time as shown in Figure 10. The sampling interval begins after the fourth MUX address bit is shifted in and continues during the remainder of the data transfer. On the falling edge of the

APPLICATIONS INFORMATION

final SCLK, the S&H goes into hold mode and the conversion begins. The voltage will be held on either the 8th, 10th, 12th or 16th falling edge of the SCLK depending on the word length selected.

Differential Inputs

With differential inputs or when the COM pin is not tied to ground, the A/D no longer converts just a single voltage but rather the difference between two voltages. In these cases, the voltage on the selected “+” input is still sampled and held and therefore may be rapidly time varying just as in single ended mode. However, the voltage on the selected “-” input must remain constant and be free of noise and ripple throughout the conversion time. Otherwise, the differencing operation may not be performed accurately. The conversion time is 44 ACLK cycles. Therefore, a change in the “-” input voltage during this interval can cause conversion errors. For a sinusoidal voltage on the “-” input this error would be:

$$V_{\text{ERROR (MAX)}} = V_{\text{PEAK}} \times 2 \times \pi \times f(\text{“-”}) \times 44/f_{\text{ACLK}}$$

Where $f(\text{“-”})$ is the frequency of the “-” input voltage, V_{PEAK} is its peak amplitude and f_{ACLK} is the frequency of the ACLK. In most cases V_{ERROR} will not be significant. For a 60Hz signal on the “-” input to generate a 1/4LSB error (1.25mV) with the converter running at $\text{ACLK} = 2\text{MHz}$, its peak value would have to be 150mV.

5. Reference Inputs

The voltage between the reference inputs of the LTC1090 defines the voltage span of the A/D converter. The reference inputs look primarily like a 10kΩ resistor but will have transient capacitive switching currents due to the switched capacitor conversion technique (see Figure 14). During each bit test of the conversion (every 4 ACLK cycles), a capacitive current spike will be generated on the reference pins by the A/D. These current spikes settle quickly and do not cause a problem. However, if slow settling circuitry is used to drive the reference inputs, care must be taken to insure that transients caused by these current spikes settle completely during each bit test of the conversion.

When driving the reference inputs, three things should be kept in mind:

1. The source resistance (R_{OUT}) driving the reference inputs should be low (less than 1Ω) to prevent DC drops caused by the 1mA maximum reference current (I_{REF}).
2. Transients on the reference inputs caused by the capacitive switching currents must settle completely during each bit test (each 4 ACLK cycles). Figures 15 and 16 show examples of both adequate and poor settling. Using a slower ACLK will allow more time for the reference to settle. However, even at the maximum ACLK rate of 2MHz most references and op amps can be made to settle within the 2μs bit time.
3. It is recommended that the REF⁻ input be tied directly to the analog ground plane. If REF⁻ is biased at a voltage other than ground, the voltage must not change during a conversion cycle. This voltage must also be free of noise and ripple with respect to analog ground.

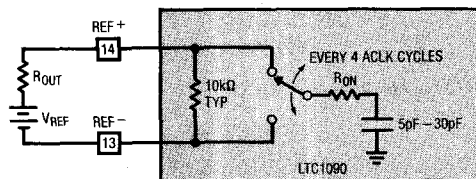


Figure 14. Reference Input Equivalent Circuit

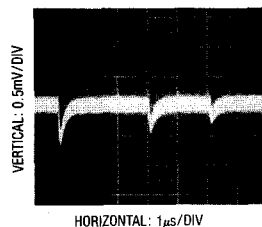


Figure 15. Adequate Reference Settling

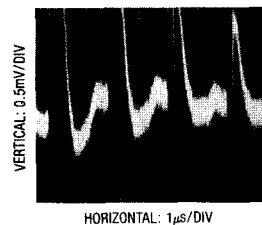


Figure 16. Poor Reference Settling Can Cause A/D Errors

APPLICATIONS INFORMATION

6. Reduced Reference Operation

The effective resolution of the LTC1090 can be increased by reducing the input span of the converter. The LTC1090 exhibits good linearity and gain over a wide range of reference voltages (see typical curves of Linearity and Gain Error vs Reference Voltage). However, care must be taken when operating at low values of V_{REF} because of the reduced LSB step size and the resulting higher accuracy requirement placed on the converter. The following factors must be considered when operating at low V_{REF} values.

1. Conversion speed (ACLK frequency)
2. Offset
3. Noise

Conversion Speed with Reduced V_{REF}

With reduced reference voltages, the LSB step size is reduced and the LTC1090 internal comparator overdrive is reduced. With less overdrive, more time is required to perform a conversion. Therefore, the maximum ACLK frequency should be reduced when low values of V_{REF} are used. This is shown in the typical curve of Maximum Conversion Clock Rate vs Reference Voltage.

Offset with Reduced V_{REF}

The offset of the LTC1090 has a larger effect on the output code when the A/D is operated with reduced reference voltage. The offset (which is typically a fixed voltage) becomes a larger fraction of an LSB as the size of the LSB is reduced. The typical curve of Unadjusted Offset Error vs Reference Voltage shows how offset in LSBs is related to reference voltage for a typical value of V_{OS} . For example, a V_{OS} of 0.5mV which is 0.1LSB with a 5V reference be-

comes 0.5LSB with a 1V reference and 2.5LSBs with a 0.2V reference. If this offset is unacceptable, it can be corrected digitally by the receiving system or by offsetting the “-” input to the LTC1090.

Noise with Reduced V_{REF}

The total input referred noise of the LTC1090 can be reduced to approximately 200 μ V peak-to-peak using a ground plane, good bypassing, good layout techniques and minimizing noise on the reference inputs. This noise is insignificant with a 5V reference but will become a larger fraction of an LSB as the size of the LSB is reduced. The typical curve of Noise Error vs Reference Voltage shows the LSB contribution of this 200 μ V of noise.

For operation with a 5V reference, the 200 μ V noise is only 0.04LSB peak-to-peak. In this case, the LTC1090 noise will contribute virtually no uncertainty to the output code. However, for reduced references, the noise may become a significant fraction of an LSB and cause undesirable jitter in the output code. For example, with a 1V reference, this same 200 μ V noise is 0.2LSB peak-to-peak. This will reduce the range of input voltages over which a stable output code can be achieved by 0.2LSB. If the reference is further reduced to 200mV, the 200 μ V noise becomes equal to one LSB and a stable code may be difficult to achieve. In this case averaging readings may be necessary.

This noise data was taken in a very clean setup. Any setup induced noise (noise or ripple on V_{CC} , V_{REF} , V_{IN} or V^-) will add to the internal noise. The lower the reference voltage to be used, the more critical it becomes to have a clean, noise-free setup.

TYPICAL APPLICATIONS

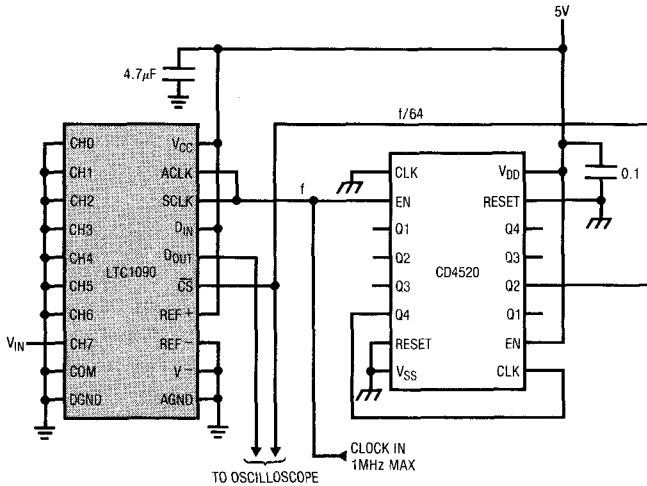
A “Quick Look” Circuit for the LTC1090

Users can get a quick look at the function and timing of the LTC1090 by using the following simple circuit. REF⁺ and D_{IN} are tied to V_{CC} selecting a 5V input span, CH7 as a single ended input, unipolar mode, MSB first format and 16-bit word length. ACLK and SCLK are tied together and

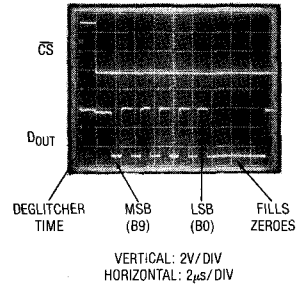
driven by an external clock. \overline{CS} is driven at 1/64 the clock rate by the CD4520 and D_{OUT} outputs the data. All other pins are tied to a ground plane. The output data from the D_{OUT} pin can be viewed on an oscilloscope which is set up to trigger on the falling edge of \overline{CS} .

TYPICAL APPLICATIONS

A "Quick Look" Circuit for the LTC1090



Scope Trace of LTC1090 "Quick Look" Circuit Showing A/D Output of 0101010101 (155_{HEX})

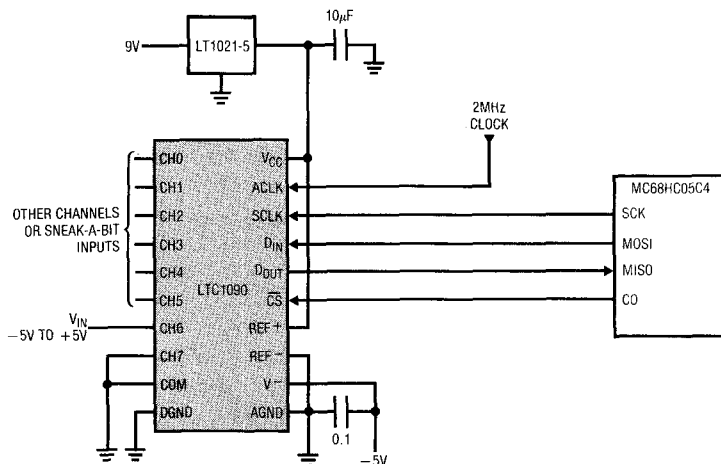


SNEAK-A-BIT™

The LTC1090's unique ability to software select the polarity of the differential inputs and the output word length is used to achieve one more bit of resolution. Using the circuit below with two conversions and some software, a 2's complement 10-bit + sign word is returned to memory inside the MPU. The MC68HC05C4 was chosen as an example; however, any processor could be used.

Two 10-bit unipolar conversions are performed: the first over a 0 to 5V span and the second over a 0 to -5V span (by reversing the polarity of the inputs). The sign of the input is determined by which of the two spans contained it. Then the resulting number (ranging from -1023 to +1023 decimal) is converted to 2's complement notation and stored in RAM.

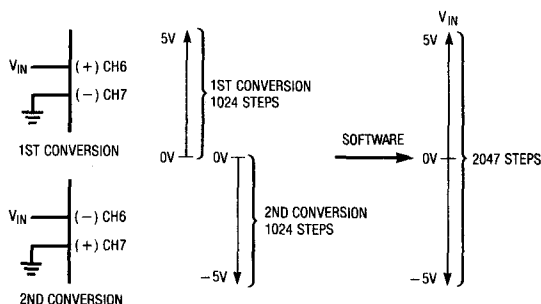
SNEAK-A-BIT Circuit



SNEAK-A-BIT is a trademark of Linear Technology Corp.

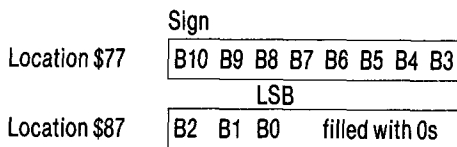
TYPICAL APPLICATIONS

SNEAK-A-BIT

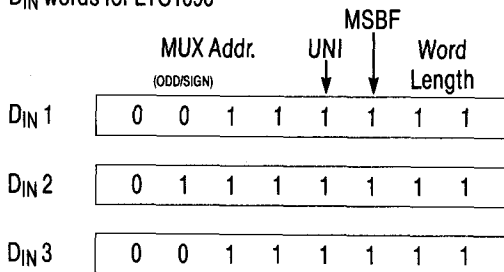


SNEAK-A-BIT Code

D_{OUT} from LTC1090 in MC68HC05C4 RAM



D_{IN} words for LTC1090



Sneak-A-Bit Code for the LTC1090 Using the MC68HC05C4

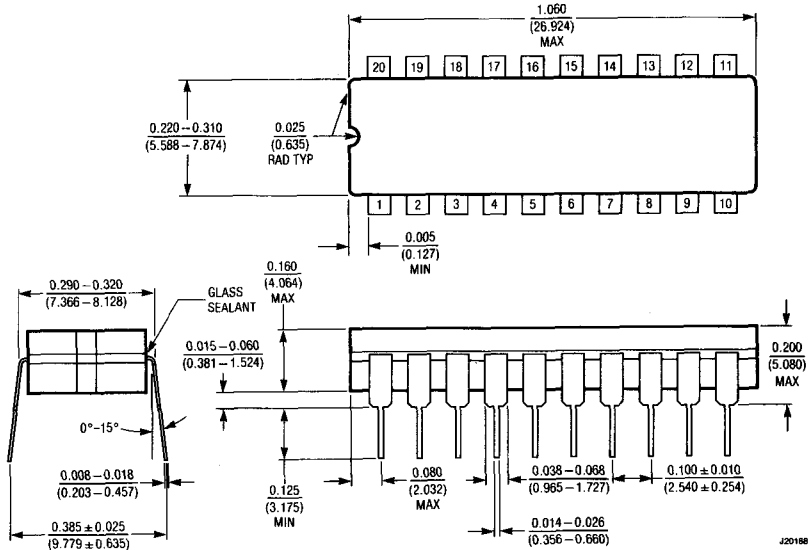
MNEMONIC	DESCRIPTION
LDA #50	Configuration data for SPCR
STA \$0A	Load configuration data into \$0A
LDA #\$FF	Configuration data for port C DDR
STA \$06	Load configuration data into port C DDR
BSET 0, \$02	Make sure CS is high
JSR READ -/+	Dummy read configures LTC1090 for next read
JSR READ +/-	Read CH6 with respect to CH7
JSR READ -/+	Read CH7 with respect to CH6
JSR CHK SIGN	Determines which reading has valid data, converts to 2's complement and stores in RAM

Sneak-A-Bit Code for the LTC1090 Using the MC68HC05C4

MNEMONIC	DESCRIPTION
READ -/+ : LDA #3F	Load D_{IN} word for LTC1090 into ACC
JSR TRANSFER	Read LTC1090 routine
LDA \$60	Load MSBs from LTC1090 into ACC
STA \$71	Store MSBs in \$71
LDA \$61	Load LSBs from LTC1090 into ACC
STA \$72	Store LSBs in \$72
RTS	Return
READ +/- : LDA #7F	Load D_{IN} word for LTC1090 into ACC
JSR TRANSFER	Read LTC1090 routine
LDA \$60	Load MSBs from LTC1090 into ACC
STA \$73	Store MSBs in \$73
LDA \$61	Load LSBs from LTC1090 into ACC
STA \$74	Store LSBs in \$74
RTS	Return
TRANSFER: BCLR 0, \$02	CS goes low
STA \$0C	Load D_{IN} into SPI. Start transfer
TST \$0B	Test status of SPIF
BPL LOOP 1	Loop to previous instruction if not done
LDA \$0C	Load contents of SPI data reg into ACC
STA \$0C	Start next cycle
STA \$60	Store MSBs in \$60
TST \$0B	Test status of SPIF
BPL LOOP 2	Loop to previous instruction if not done
BSET 0, \$02	CS goes high
LDA \$0C	Load contents of SPI data reg into ACC
STA \$61	Store LSBs in \$61
RTS	Return
CHK SIGN: LDA \$73	Load MSBs of +/- read into ACC
ORA \$74	Or ACC (MSBs) with LSBs of +/- read
BEQ MINUS	If result is 0 goto minus
CLC	Clear carry
ROR \$73	Rotate right \$73 through carry
ROR \$74	Rotate right \$74 through carry
LDA \$73	Load MSBs of +/- read into ACC
STA \$77	Store MSBs in RAM location \$77
LDA \$74	Load LSBs of +/- read into ACC
STA \$87	Store LSBs in RAM location \$87
BRA END	Goto end of routine
MINUS: CLC	Clear carry
ROR \$71	Shift MSBs of -/+ read right
ROR \$72	Shift LSBs of -/+ read right
COM \$71	1's complement of MSBs
COM \$72	1's complement of LSBs
LDA \$72	Load LSBs into ACC
ADD #301	Add 1 to LSBs
STA \$72	Store ACC in \$72
CLRA	Clear ACC
ADC \$71	Add with carry to MSBs. Result in ACC
STA \$71	Store ACC in \$71
STA \$77	Store MSBs in RAM location \$77
LDA \$72	Load LSBs in ACC
STA \$87	Store LSBs in RAM location \$87
END: RTS	Return

PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

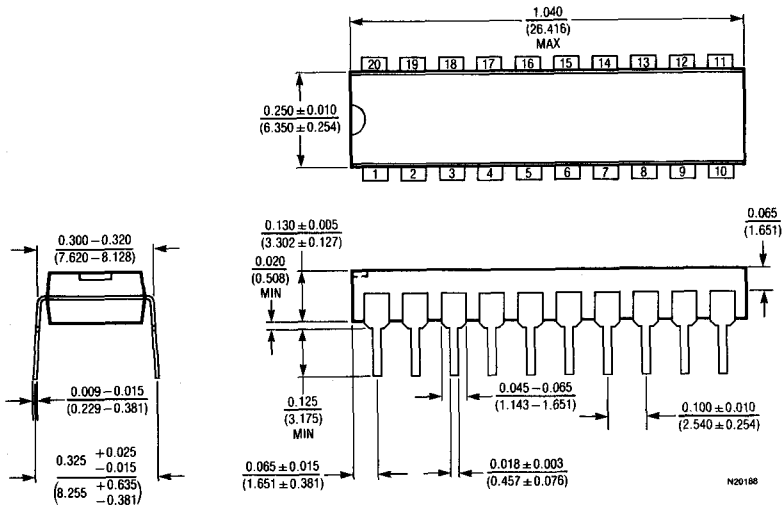
J20 Package Ceramic DIP



J20188

T_{jmax} 150°C	θ_{JA} 70°C/W
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N20 Package Molded DIP



N20188

T_{jmax} 110°C	θ_{JA} 90°C/W
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1, 2, 6 and 8 Channel, 10-Bit Serial I/O Data Acquisition Systems

FEATURES

- Programmable Features
 - Unipolar/Bipolar Conversions
 - Differential/Single Ended Multiplexer Configurations
- Sample and Holds
- Single Supply 5V, 10V or $\pm 5V$ Operation
- Direct 3 or 4 Wire Interface to Most MPU Serial Ports and All MPU Parallel I/O Ports
- Analog Inputs Common-Mode to Supply Rails
- Resolution 10 Bits
- Total Unadjusted Error (A Grade) $\pm 1/2\text{LSB}$ Over Temp
- Fast Conversion Time 20 μ s
- Low Supply Current LTC1091 3.5mA Max, 1.5mA Typ
LTC1092/3/4 2.5mA Max, 1mA Typ

as well as on chip sample and holds. On-chip serial ports allow efficient data transfer to a wide range of microprocessors and microcontrollers. These circuits can provide a complete data acquisition system in ratiometric applications or can be used with an external reference in others.

The high impedance analog inputs and the ability to operate with reduced spans (below 1V full scale) allow direct connection to sensors and transducers in many applications, eliminating the need for gain stages.

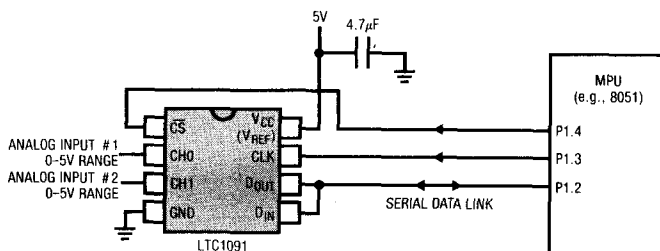
An efficient serial port communicates without external hardware to most MPU serial ports and all MPU parallel I/O ports allowing eight channels of data to be transmitted over as few as 3 wires. This, coupled with low power consumption, makes remote location possible and facilitates transmitting data through isolation barriers.

DESCRIPTION

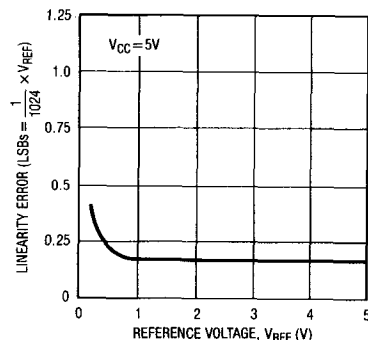
The LTC1091/2/3/4 10-bit data acquisition systems are designed to provide complete function, excellent accuracy and ease of use when digitizing analog data from a wide variety of signal sources and transducers. Built around a 10-bit, switched capacitor, successive approximation A/D core, these devices include software configurable analog multiplexers and bipolar and unipolar conversion modes

Temperature drift of offset, linearity, and full scale error are all extremely low (1ppm/ $^{\circ}$ C typically) allowing all grades to be specified with offset and linearity errors of $\pm 0.5\text{LSB}$ maximum over temperature. In addition, the A grade devices are specified with full scale error and total unadjusted error (including the effects of offset, linearity, and full scale errors) of $\pm 0.5\text{LSB}$ maximum over temperature. The lower grade has a full scale specification of $\pm 2\text{LSB}$ for applications where full scale is adjustable or less critical.

TYPICAL APPLICATION



FOR 8051 CODE SEE APPLICATIONS INFORMATION SECTION



LTC1091/LTC1092 LTC1093/LTC1094

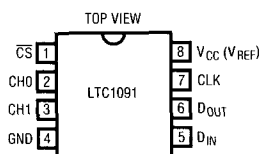
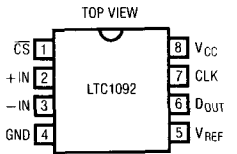
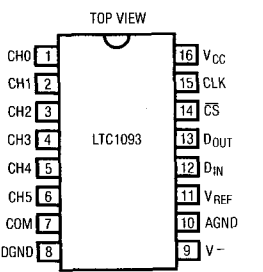
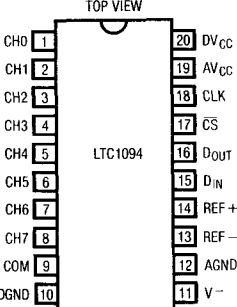
ABSOLUTE MAXIMUM RATINGS

(Notes 1 and 2)

Supply Voltage (V_{CC}) to GND or V^- 12V
 Negative Supply Voltage (V^-) -6V to GND
 Voltage
 Analog Reference and LTC1091/2 \overline{CS}
 Inputs (V^-) - 0.3V to $V_{CC} + 0.3V$
 Digital Inputs (except LTC1091/2 \overline{CS}) -0.3V to 12V
 Digital Outputs -0.3V to $V_{CC} + 0.3V$

Power Dissipation 500mW
 Operating Temperature Range
 LTC1091-4AC, LTC1091-4C -40°C to 85°C
 LTC1091-4AM, LTC1091-4M -55°C to 125°C
 Storage Temperature Range -65°C to 150°C
 Lead Temperature (Soldering, 10 sec.) 300°C

PACKAGE/ORDER INFORMATION

TOP VIEW	ORDER PART NUMBER	TOP VIEW	ORDER PART NUMBER
 <p>TOP VIEW</p> <p>CS 1, CH0 2, CH1 3, GND 4, 8, 7, 6, 5, V_{CC} (V_{REF}) 8, CLK 7, D_{OUT} 6, D_{IN} 5</p> <p>LTC1091</p> <p>J PACKAGE: 8 LEAD CERAMIC DIP N PACKAGE: 8 LEAD PLASTIC DIP</p>	LTC1091AMJ8 LTC1091MJ8 LTC1091ACJ8 LTC1091CJ8 LTC1091ACN8 LTC1091CN8	 <p>TOP VIEW</p> <p>CS 1, +IN 2, -IN 3, GND 4, 8, 7, 6, 5, V_{CC}, CLK 7, D_{OUT} 6, V_{REF} 5</p> <p>LTC1092</p> <p>J PACKAGE: 8 LEAD CERAMIC DIP N PACKAGE: 8 LEAD PLASTIC DIP</p>	LTC1092AMJ8 LTC1092MJ8 LTC1092ACJ8 LTC1092CJ8 LTC1092ACN8 LTC1092CN8
 <p>TOP VIEW</p> <p>CH0 1, CH1 2, CH2 3, CH3 4, CH4 5, CH5 6, COM 7, DGND 8, 16, 15, 14, 13, 12, 11, 10, 9, V_{CC}, CLK 15, \overline{CS} 14, D_{OUT} 13, D_{IN} 12, V_{REF} 11, AGND 10, V^- 9</p> <p>LTC1093</p> <p>J PACKAGE: 16 LEAD CERAMIC DIP N PACKAGE: 16 LEAD PLASTIC DIP</p>	LTC1093AMJ LTC1093MJ LTC1093ACJ LTC1093CJ LTC1093ACN LTC1093CN	 <p>TOP VIEW</p> <p>CH0 1, CH1 2, CH2 3, CH3 4, CH4 5, CH5 6, CH6 7, CH7 8, COM 9, DGND 10, 20, 19, 18, 17, 16, 15, 14, 13, 12, 11, DV_{CC}, AV_{CC}, CLK 18, \overline{CS} 17, D_{OUT} 16, D_{IN} 15, REF+ 14, REF- 13, AGND 12, V^- 11</p> <p>LTC1094</p> <p>J PACKAGE: 20 LEAD CERAMIC DIP N PACKAGE: 20 LEAD PLASTIC DIP</p>	LTC1094AMJ LTC1094MJ LTC1094ACJ LTC1094CJ LTC1094ACN LTC1094CN

PRODUCT GUIDE

PART NUMBER	# CHANNELS	CONVERSION MODES		REDUCED SPAN CAPABILITY (SEPARATE V_{REF})	$\pm 5V$ CAPABILITY	
		UNIPOLAR	BIPOLAR			
LTC1091	2	•				Pin for pin 10-bit upgrade of ADC0832
LTC1092	1	•		•		Pin for pin 10-bit upgrade of ADC0831
LTC1093	6	•	•	•	•	
LTC1094	8	•	•	•	•	

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LTC1091-4/LTC1091-4A		UNITS
			MIN	MAX	
V_{CC}	Supply Voltage		4.5	10	V
V^-	Negative Supply Voltage	$V_{CC} = 5V$ LTC1093/4	-5.5	0	V
f_{CLK}	Clock Frequency	$V_{CC} = 5V$	0.01	0.5	MHz
t_{CYC}	Total Cycle Time	LTC1091	15 CLK Cycles + 2 μ s		
		LTC1092	12 CLK Cycles + 2 μ s		
		LTC1093/4	18 CLK Cycles + 2 μ s		
t_{HDI}	Hold Time, D_{IN} After SCLK1	$V_{CC} = 5V$	150		ns
t_{suCS}	Setup Time \overline{CS} Before CLK1	$V_{CC} = 5V$	1		μ s
t_{suDI}	Setup Time, D_{IN} Stable Before CLK1	$V_{CC} = 5V$	400		ns
t_{WHCLK}	CLK High Time	$V_{CC} = 5V$	0.8		μ s
t_{WLCLK}	CLK Low Time	$V_{CC} = 5V$	1		μ s
t_{WHCS}	\overline{CS} High Time Between Data Transfer Cycles	$V_{CC} = 5V$	2		μ s
t_{WLCS}	\overline{CS} Low Time During Data Transfer	LTC1091	15		CLK Cycles
		LTC1092	12		CLK Cycles
		LTC1093/4	18		CLK Cycles

CONVERTER AND MULTIPLEXER CHARACTERISTICS (Note 3)

PARAMETER	CONDITIONS		LTC1091-4A			LTC1091-4			UNITS	
			MIN	TYP	MAX	MIN	TYP	MAX		
Offset Error	(Note 4)	●			±0.5			±0.5	LSB	
Linearity Error	(Notes 4 and 5)	●			±0.5			±0.5	LSB	
Full Scale Error	(Note 4)	●			±0.5			±2.0	LSB	
Total Unadjusted Error	$V_{REF} = 5.000V$ (Notes 4 and 6)	●			±0.5				LSB	
Reference Input Resistance	$V_{REF} = 5V$, LTC1092/3/4	●	5	10		5	10		k Ω	
Analog and REF Input Range	(Note 7)		(V ⁻) - 0.05V to $V_{CC} + 0.05V$							V
On Channel Leakage Current (Note 8)	On Channel = 5V Off Channel = 0V	●			1			1	μ A	
	On Channel = 0V Off Channel = 5V	●			-1			-1	μ A	
Off Channel Leakage Current (Note 8)	On Channel = 5V Off Channel = 0V	●			-1			-1	μ A	
	On Channel = 0V Off Channel = 5V	●			1			1	μ A	

LTC1091/LTC1092 LTC1093/LTC1094

AC CHARACTERISTICS (Note 3)

SYMBOL	PARAMETER	CONDITIONS	LTC1091-4/LTC1091-4A			UNITS
			MIN	TYP	MAX	
t_{SMPL}	Analog Input Sample Time	See Operating Sequence		1.5		CLK Cycles
t_{CONV}	Conversion Time	See Operating Sequence		10		CLK Cycles
t_{dDO}	Delay Time, CLK \downarrow to D $_{OUT}$ Data Valid	See Test Circuits	●	400	850	ns
t_{dis}	Delay Time, \overline{CS} \downarrow to D $_{OUT}$ Hi-Z	See Test Circuits	●	180	450	ns
t_{en}	Delay Time, CLK \downarrow to D $_{OUT}$ Enabled	See Test Circuits	●	160	450	ns
t_{hDO}	Time Output Data Remains Valid After SCLK \downarrow			150		ns
t_f	D $_{OUT}$ Fall Time	See Test Circuits	●	90	300	ns
t_r	D $_{OUT}$ Rise Time	See Test Circuits	●	60	300	ns
C_{IN}	Input Capacitance	Analog Inputs On Channel		65		pF
		Off Channel		5		pF
		Digital Inputs		5		pF

DIGITAL AND DC ELECTRICAL CHARACTERISTICS (Note 3)

SYMBOL	PARAMETER	CONDITIONS	LTC1091-4/LTC1091-4A			UNITS
			MIN	TYP	MAX	
V_{IH}	High Level Input Voltage	$V_{CC} = 5.25V$	●	2.0		V
V_{IL}	Low Level Input Voltage	$V_{CC} = 4.75V$	●		0.8	V
I_{IH}	High Level Input Current	$V_{IN} = V_{CC}$	●		2.5	μA
I_{IL}	Low Level Input Current	$V_{IN} = 0V$	●		-2.5	μA
V_{OH}	High Level Output Voltage	$V_{CC} = 4.75V, I_O = 10\mu A$	●	4.7		V
		$I_O = 360\mu A$	●	2.4	4.0	V
V_{OL}	Low Level Output Voltage	$V_{CC} = 4.75V, I_O = 1.6mA$	●		0.4	V
I_{OZ}	Hi-Z Output Leakage	$V_{OUT} = V_{CC}, \overline{CS}$ High	●		3	μA
		$V_{OUT} = 0V, \overline{CS}$ High	●		-3	μA
I_{SOURCE}	Output Source Current	$V_{OUT} = 0V$		-10		mA
I_{SINK}	Output Sink Current	$V_{OUT} = V_{CC}$		10		mA
I_{CC}	Positive Supply Current	\overline{CS} High, LTC1091	●	1.5	3.5	mA
		\overline{CS} High, REF $^+$ Open, LTC1092/3/4	●	1.0	2.5	mA
I_{REF}	Reference Current	$V_{REF} = 5V$, LTC1092/3/4	●	0.5	1.0	mA
I^-	Negative Supply Current	\overline{CS} High, $V^- = -5V$, LTC1093/4	●	1	50	μA

Note 1: Absolute maximum ratings are those values beyond which the life of a device may be impaired.

Note 2: All voltage values are with respect to ground with DGND, AGND, GND and REF $^-$ wired together (unless otherwise noted). REF $^-$ is internally connected to the AGND pin on the LTC1093. DGND, AGND, REF $^-$ and V $^-$ are internally connected to the GND pin on the LTC1091/2.

Note 3: $V_{CC} = 5V$, $V_{REF}^+ = 5V$, $V_{REF}^- = 0V$, $V^- = 0V$ for unipolar mode and $-5V$ for bipolar mode, CLK = 0.5MHz unless otherwise specified. The ● indicates specs which apply over the full operating temperature range; all other limits and typicals $T_A = 25^\circ C$.

Note 4: These specs apply for both unipolar (LTC1091-4) and bipolar (LTC1093/4 only) modes. In bipolar mode, one LSB is equal to the bipolar input span ($2V_{REF}$) divided by 1024. For example, when $V_{REF} = 5V$, 1LSB bipolar) = $2(5V)/1024 = 9.77mV$.

Note 5: Linearity error is specified between the actual end points of the A/D transfer curve.

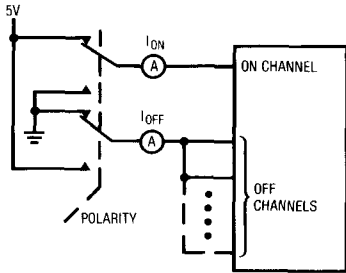
Note 6: Total unadjusted error includes offset, full scale, linearity, multiplexer and hold step errors.

Note 7: Two on-chip diodes are tied to each reference and analog input which will conduct for reference or analog input voltages one diode drop below V $^-$ or one diode drop above V_{CC} . Be careful during testing at low V_{CC} levels (4.5V), as high level reference or analog inputs (5V) can cause this input diode to conduct, especially at elevated temperatures, and cause errors for inputs near full-scale. This spec allows 50mV forward bias of either diode. This means that as long as the reference or analog input does not exceed the supply voltage by more than 50mV, the output code will be correct. To achieve an absolute 0V to 5V input voltage range will therefore require a minimum supply voltage of 4.950V over initial tolerance, temperature variations and loading.

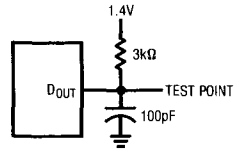
Note 8: Channel leakage current is measured after the channel selection.

TEST CIRCUITS

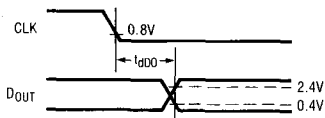
On and Off Channel Leakage Current



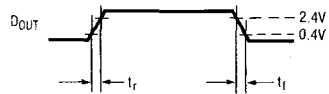
Load Circuit for t_{dD} , t_r , and t_f



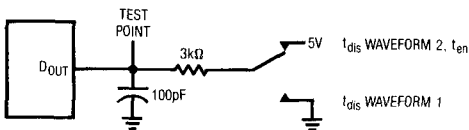
Voltage Waveforms for D_{OUT} Delay Time, t_{dD}



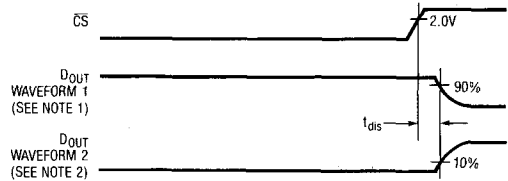
Voltage Waveforms for D_{OUT} Rise and Fall Times, t_r , t_f



Load Circuit for t_{dis} and t_{en}



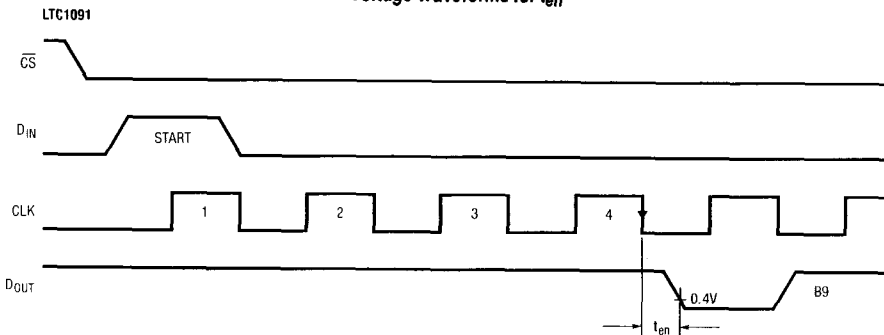
Voltage Waveforms for t_{dis}



NOTE 1: WAVEFORM 1 IS FOR AN OUTPUT WITH INTERNAL CONDITIONS SUCH THAT THE OUTPUT IS HIGH UNLESS DISABLED BY THE OUTPUT CONTROL.

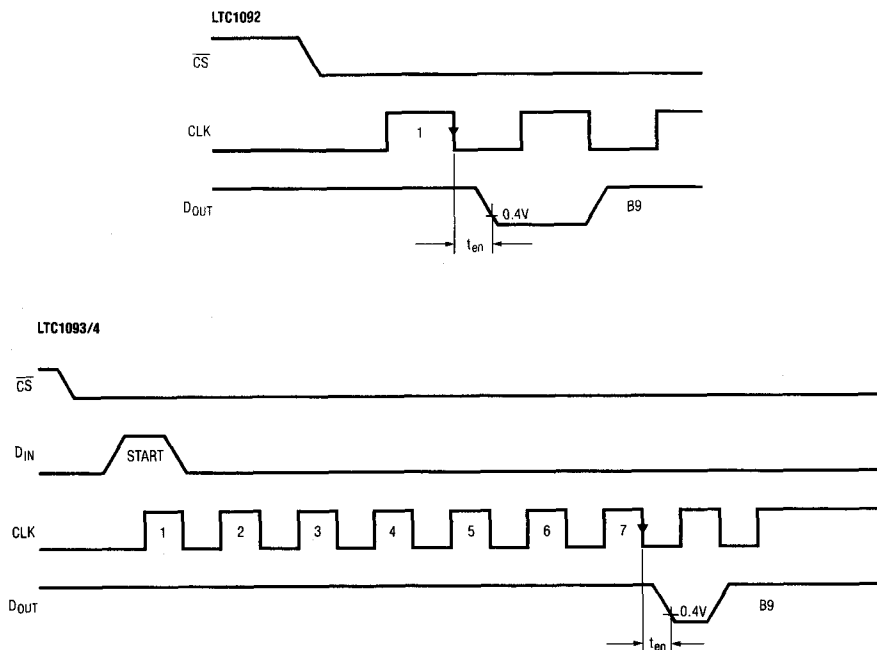
NOTE 2: WAVEFORM 2 IS FOR AN OUTPUT WITH INTERNAL CONDITIONS SUCH THAT THE OUTPUT IS LOW UNLESS DISABLED BY THE OUTPUT CONTROL.

Voltage Waveforms for t_{en}



TEST CIRCUITS

Voltage Waveforms for t_{en}



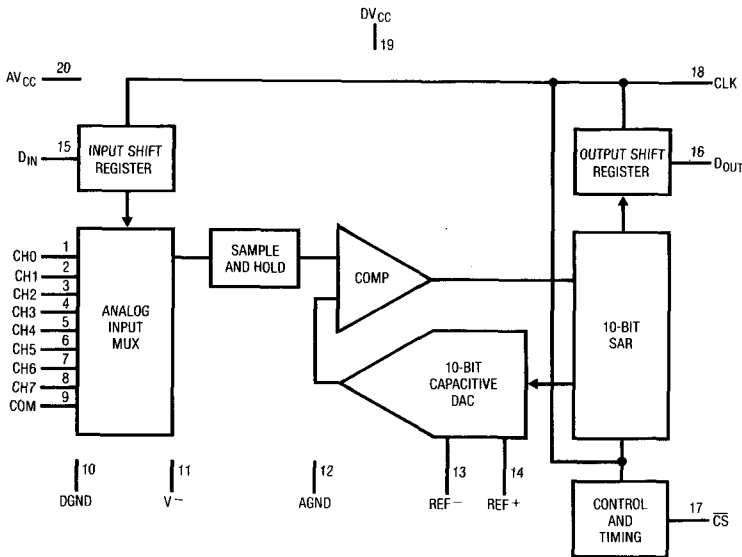
PIN FUNCTIONS LTC1091/2

LTC1091 #	LTC1092 #	PIN	FUNCTION	DESCRIPTION
1	1	\overline{CS}	Chip Select Input	A logic low on this input enables the LTC1091/2.
2,3	2,3	CH0, CH1	Analog Inputs	These inputs must be free of noise with respect to GND.
4	4	IN +, IN -	Analog Inputs	These inputs must be free of noise with respect to GND.
4	4	GND	Analog Ground	GND should be tied directly to an analog ground plane.
5	5	D _{IN}	Digital Data Input	The multiplexer address is shifted into this input.
5	5	V _{REF}	Reference Input	The reference input defines the span of the A/D converter and must be kept free of noise with respect to AGND.
6	6	D _{OUT}	Digital Data Output	The A/D conversion result is shifted out of this output.
7	7	CLK	Shift Clock	This clock synchronizes the serial data transfer.
8	7	V _{CC} (V _{REF})	Positive Supply and Reference Voltage	This pin provides power and defines the span of the A/D converter. It must be kept free of noise and ripple by bypassing directly to the analog ground plane.
8	8	V _{CC}	Positive Supply Voltage	This pin provides power to the A/D converter. It must be kept free of noise and ripple by bypassing directly to the analog ground plane.

PIN FUNCTIONS LTC1093/4

LTC1093 #	LTC1094 #	PIN	FUNCTION	DESCRIPTION
1-6	1-8	CH0-CH5	Analog Inputs	The analog inputs must be free of noise with respect to AGND.
7	9	CH0-CH7 COM	Analog Inputs Common	The analog inputs must be free of noise with respect to AGND. The common pin defines the zero reference point for all single ended inputs. It must be free of noise and is usually tied to the analog ground plane.
8	10	DGND	Digital Ground	This is the ground for the internal logic. Tie to the ground plane.
9	11	V ⁻	Negative Supply	Tie V ⁻ to most negative potential in the circuit. (Ground in single supply applications.)
10	12	AGND	Analog Ground	AGND should be tied directly to the analog ground plane.
11		V _{REF}	Reference Input	The reference input must be kept free of noise with respect to AGND.
	13, 14	REF +, REF -	Reference Input	The reference input must be kept free of noise with respect to AGND.
12	15	D _{IN}	Data Input	The A/D configuration word is shifted into this input.
13	16	D _{OUT}	Digital Data Output	The A/D conversion result is shifted out of this output.
14	17	CS	Chip Select Input	A logic low on this input enables the LTC1093/4.
15	18	CLK	Shift Clock	This clock synchronizes the serial data transfer.
16		V _{CC}	Positive Supply	This supply must be kept free of noise and ripple by bypassing directly to the analog ground plane.
	19, 20	AV _{CC} , DV _{CC}	Positive Supply	This supply must be kept free of noise and ripple by bypassing directly to the analog ground plane. AV _{CC} and DV _{CC} should be tied together on the LTC1094.

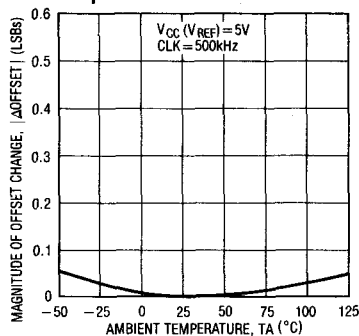
BLOCK DIAGRAM (Pin numbers refer to LTC1094)



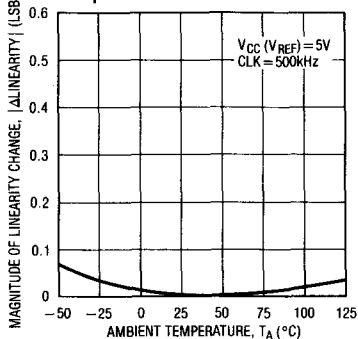
9

TYPICAL PERFORMANCE CHARACTERISTICS LTC1091-4

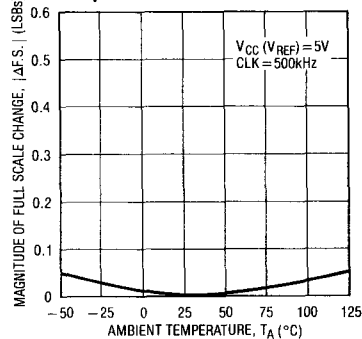
Change in Offset Error vs Temperature



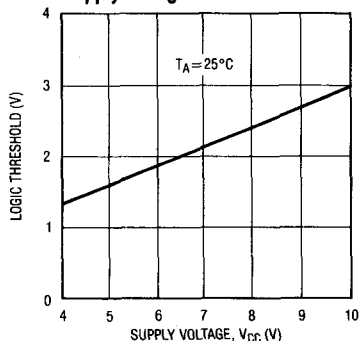
Change in Linearity Error vs Temperature



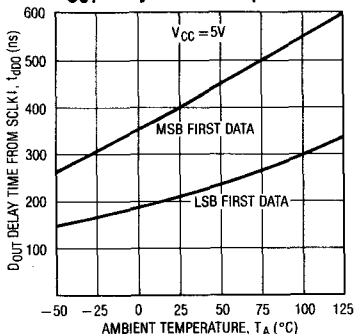
Change in Full Scale Error vs Temperature



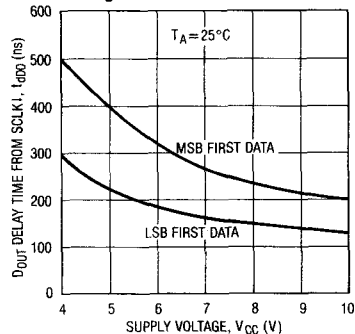
Digital Input Logic Threshold vs Supply Voltage



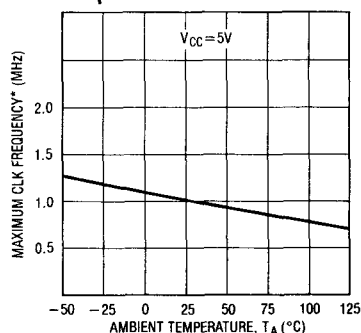
DOUT Delay Time vs Temperature



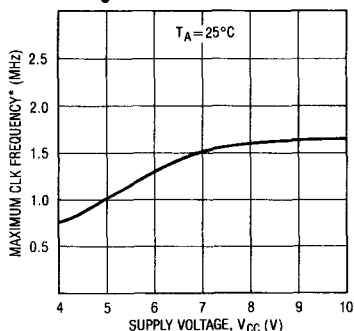
DOUT Delay Time vs Supply Voltage



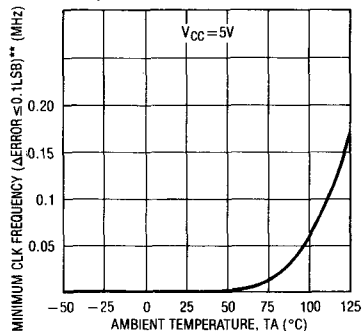
Maximum Clock Rate vs Temperature



Maximum Clock Rate vs Supply Voltage



Minimum Clock Rate vs Temperature

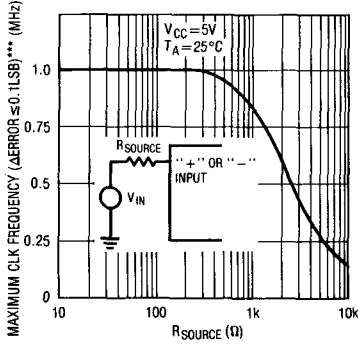


*MAXIMUM CLK FREQUENCY REPRESENTS THE HIGHEST FREQUENCY AT WHICH CLK CAN BE OPERATED (WITH 50% DUTY CYCLE) WHILE STILL PROVIDING 100ns SETUP TIME FOR THE DEVICE RECEIVING THE DOUT DATA.

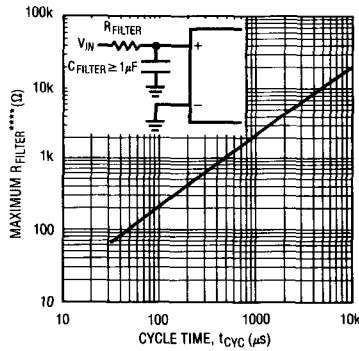
**AS THE CLK FREQUENCY IS DECREASED FROM 500kHz, MINIMUM CLK FREQUENCY (Δ ERROR ≤ 0.1 LSB) REPRESENTS THE FREQUENCY AT WHICH A 0.1LSB SHIFT IN ANY CODE TRANSITION FROM ITS 500kHz VALUE IS FIRST DETECTED.

TYPICAL PERFORMANCE CHARACTERISTICS

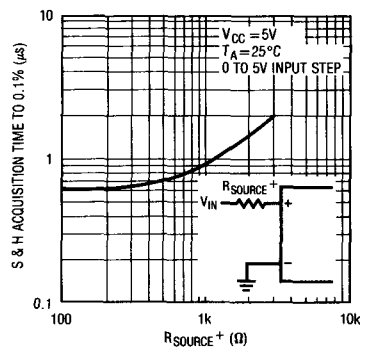
Maximum Clock Rate vs Source Resistance LTC1091-4



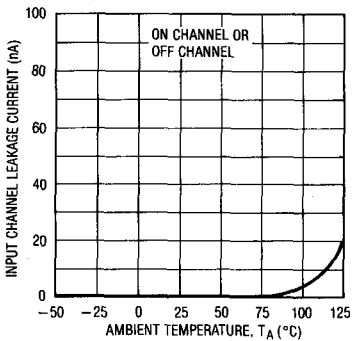
Maximum Filter Resistor vs Cycle Time LTC1091-4



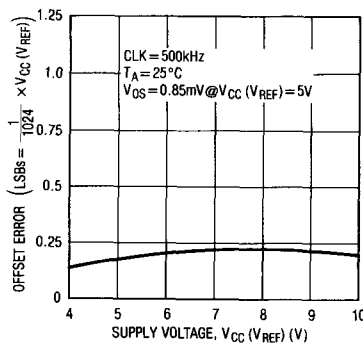
Sample and Hold Acquisition Time vs Source Resistance LTC1091-4



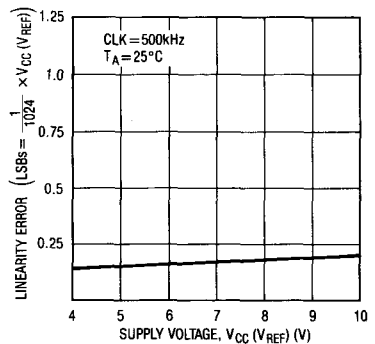
Input Channel Leakage Current vs Temperature LTC1091/2



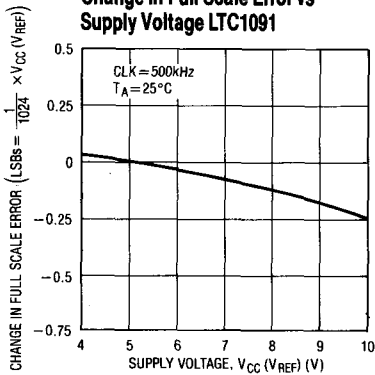
Offset Error vs Supply Voltage LTC1091



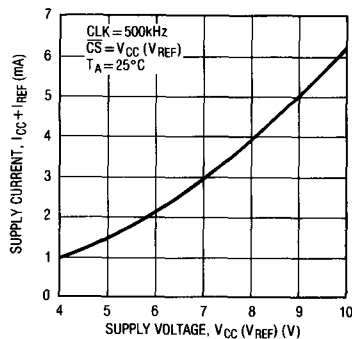
Linearity Error vs Supply Voltage LTC1091



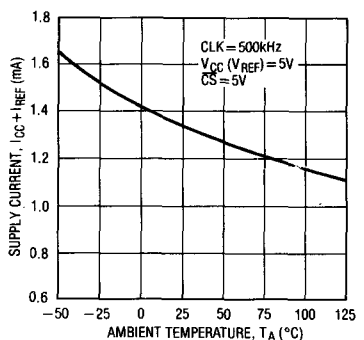
Change in Full Scale Error vs Supply Voltage LTC1091



Supply Current vs Supply Voltage LTC1091



Supply Current vs Temperature LTC1091

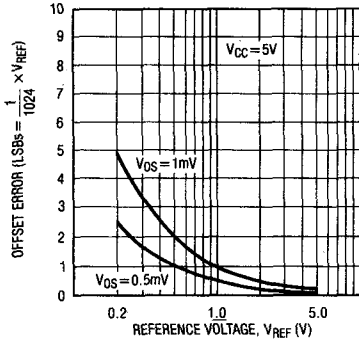


*** AS THE CLK FREQUENCY AND SOURCE RESISTANCE ARE INCREASED, MAXIMUM CLK FREQUENCY (Δ ERROR \leq 0.1LSB) REPRESENTS THE FREQUENCY AT WHICH A 0.1LSB SHIFT IN ANY CODE TRANSITION FROM ITS 500kHz, 0 Ω VALUE IS FIRST DETECTED.

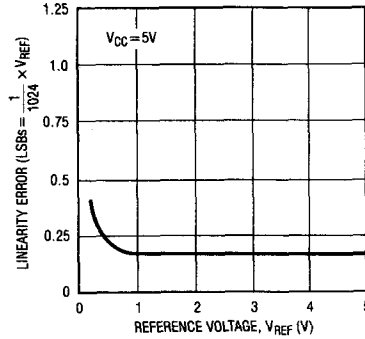
**** MAXIMUM R_{FILTER} REPRESENTS THE FILTER RESISTOR VALUE AT WHICH A 0.1LSB CHANGE IN FULL-SCALE ERROR FROM ITS VALUE AT $R_{FILTER}=0$ IS FIRST DETECTED.

TYPICAL PERFORMANCE CHARACTERISTICS

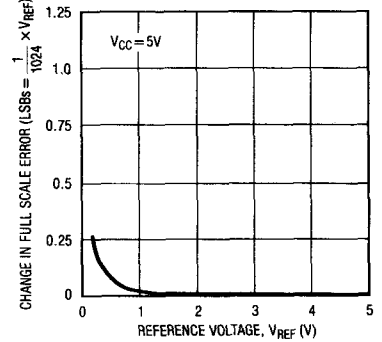
Unadjusted Offset Error vs Reference Voltage LTC1092/3/4



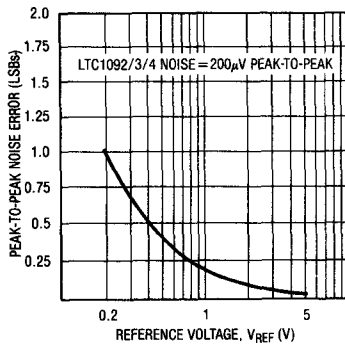
Linearity Error vs Reference Voltage LTC1092/3/4



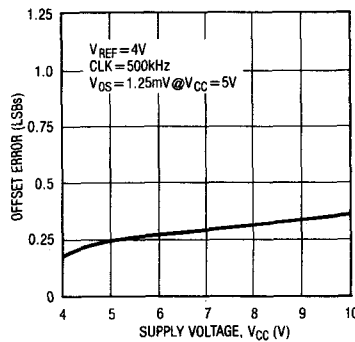
Change in Full Scale Error vs Reference Voltage LTC1092/3/4



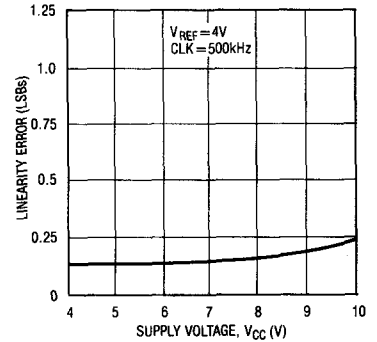
Noise Error vs Reference Voltage LTC1092/3/4



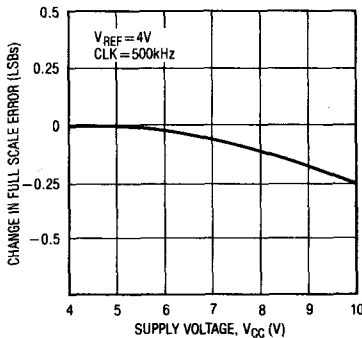
Offset Error vs Supply Voltage LTC1092/3/4



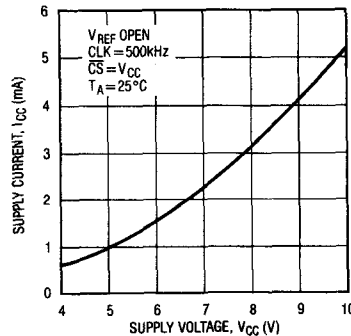
Linearity Error vs Supply Voltage LTC1092/3/4



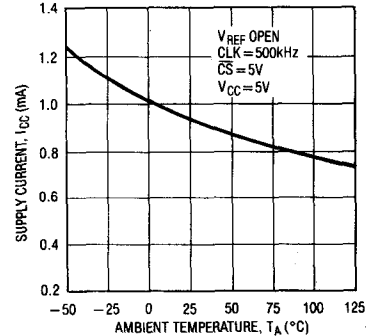
Change in Full Scale Error vs Supply Voltage LTC1092/3/4



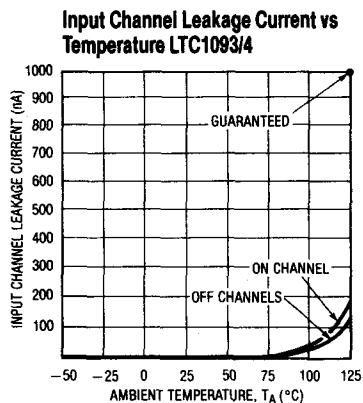
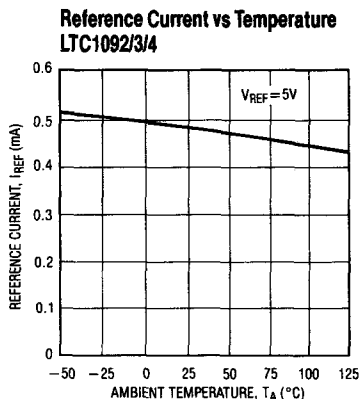
Supply Current vs Supply Voltage LTC1092/3/4



Supply Current vs Temperature LTC1092/3/4



TYPICAL PERFORMANCE CHARACTERISTICS



APPLICATIONS INFORMATION

The LTC1091-4 are data acquisition components which contain the following functional blocks:

- 10-bit successive approximation A/D converter
- Analog multiplexer (MUX)
- Sample and hold (S/H)
- Synchronous, half duplex serial interface
- Control and timing logic

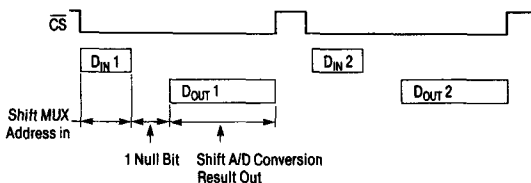
DIGITAL CONSIDERATIONS

1. Serial Interface

The LTC1091/3/4 communicates with microprocessors and other external circuitry via a synchronous, half duplex, four wire serial interface while the LTC1092 uses a three wire interface (see Operating Sequence). The clock (CLK) synchronizes the data transfer with each bit being transmitted on the falling CLK edge and captured on the rising CLK edge in both transmitting and receiving systems. The LTC1091/3/4 first receives input data and then transmits back the A/D conversion result (half duplex). Because of

the half duplex operation, D_{IN} and D_{OUT} may be tied together allowing transmission over just 3 wires: \overline{CS} , CLK and DATA (D_{IN}/D_{OUT}).

Data transfer is initiated by a falling chip select (\overline{CS}) signal. After \overline{CS} falls the LTC1091/3/4 looks for a start bit. After the start bit is received, a 3-bit input word (6-bits for the LTC1093/4) is shifted into the D_{IN} input which configures the LTC1091/3/4 and starts the conversion. After one null bit, the result of the conversion is output on the D_{OUT} line. At the end of the data exchange \overline{CS} should be brought high. This resets the LTC1091/3/4 in preparation for the next data exchange.



APPLICATIONS INFORMATION

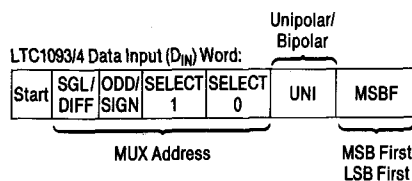
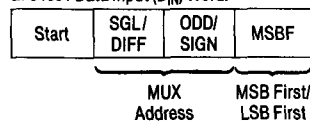
The LTC1092 does not require a configuration input word and has no D_{IN} pin. A falling \overline{CS} initiates data transfer as shown in the LTC1092 operating sequence. After \overline{CS} falls, the first CLK pulse enables D_{OUT} . After one null bit, the A/D conversion result is output on the D_{OUT} line. Bringing \overline{CS} high resets the LTC1092 for the next data exchange.

2. Input Data Word

The LTC1092 requires no D_{IN} word. It is permanently configured to have a single differential input and to operate in unipolar mode. The conversion result is output on the D_{OUT} line in MSB first sequence, followed by LSB sequence providing easy interface to MSB or LSB first serial ports. The following discussion applies to the configuration of the LTC1091/3/4.

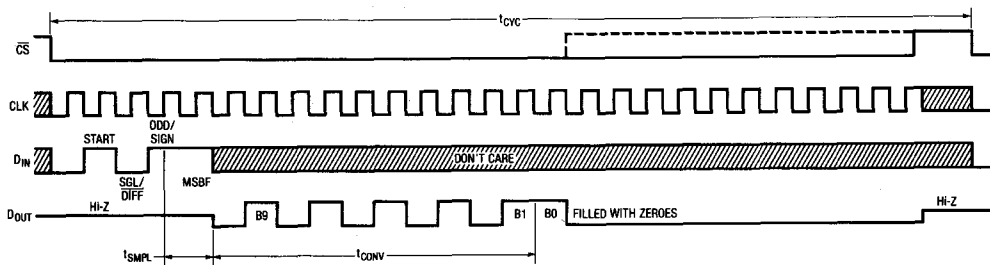
The LTC1091/3/4 clocks data into the D_{IN} input on the rising edge of the clock. The input data words are defined as follows:

LTC1091 Data Input (D_{IN}) Word:

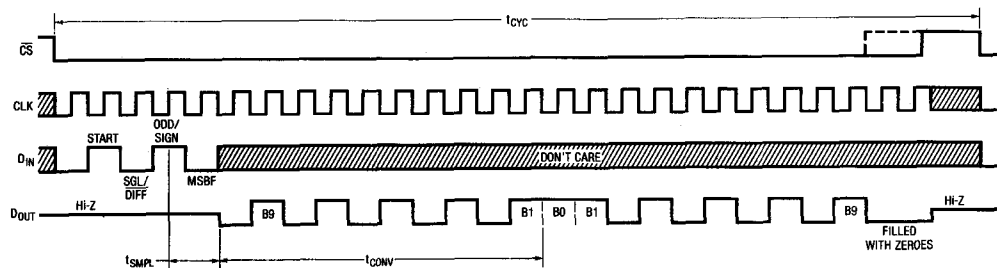


LTC1091 Operating Sequence
Example: Differential Inputs (CH1 +, CH0 -)

MSB First Data (MSBF = 1)

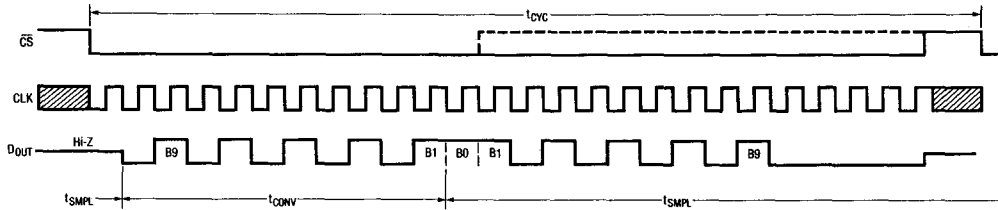


LSB First Data (MSBF = 0)



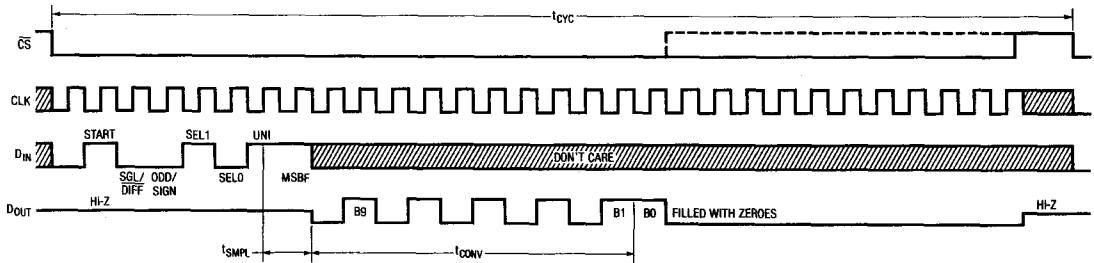
APPLICATIONS INFORMATION

LTC1092 Operating Sequence

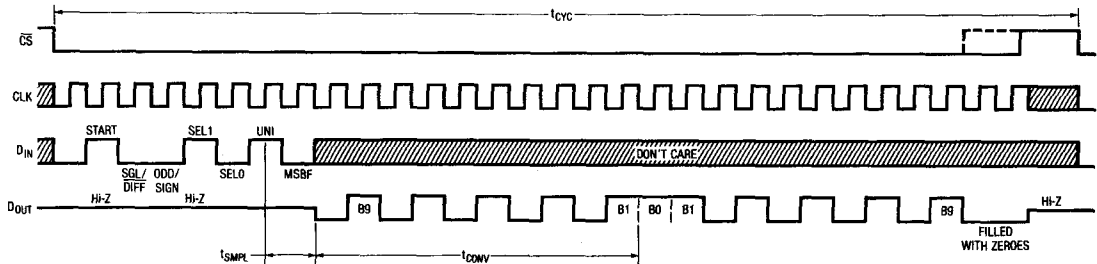


LTC1093/4 Operating Sequence Example: Differential Inputs (CH4 +, CH5 -), Unipolar Mode

MSB First Data (MSBF = 1)



LSB First Data (MSBF = 0)



9

APPLICATIONS INFORMATION

Start Bit

The first "logical one" clocked into the D_{IN} input after \overline{CS} goes low is the start bit. The start bit initiates the data transfer. The LTC1091/3/4 will ignore all leading zeros which precede this logical one. After the start bit is received, the remaining bits of the input word will be clocked in. Further inputs on the D_{IN} pin are then ignored until the next \overline{CS} cycle.

Multiplexer (MUX) Address

The bits of the input word following the START bit assign the MUX configuration for the requested conversion. For a

given channel selection, the converter will measure the voltage between the two channels indicated by the + and - signs in the selected row of the following tables. In single ended mode, all input channels are measured with respect to GND on the LTC1091 and COM on the LTC1093/4.

LTC1091 Channel Selection

	MUX ADDRESS		CHANNEL #		GND
	SGL/DIFF	ODD/SIGN	0	1	
Single-ended MUX mode	1	0	+		-
	1	1		+	-
Differential MUX mode	0	0	+	-	
	0	1	-	+	

LTC1093 Channel Selection

MUX ADDRESS				DIFFERENTIAL CHANNEL SELECTION								
SGL/DIFF	ODD/SIGN	SELECT		0	1	2	3	4	5			
		1	0									
0	0	0	0	+	-							
0	0	0	1			+	-					
0	0	1	0					+	-			
0	0	1	1	NOT USED								
0	1	0	0	-	+							
0	1	0	1			-	+					
0	1	1	0					-	+			
0	1	1	1	NOT USED								

LTC1094 Channel Selection

MUX ADDRESS				DIFFERENTIAL CHANNEL SELECTION									
SGL/DIFF	ODD/SIGN	SELECT		0	1	2	3	4	5	6	7		
		1	0										
0	0	0	0	+	-								
0	0	0	1			+	-						
0	0	1	0					+	-				
0	0	1	1								+	-	
0	1	0	0	-	+								
0	1	0	1			-	+						
0	1	1	0					-	+				
0	1	1	1								-	+	

MUX ADDRESS				SINGLE ENDED CHANNEL SELECTION								
SGL/DIFF	ODD/SIGN	SELECT		0	1	2	3	4	5	COM		
		1	0									
1	0	0	0	+								-
1	0	0	1			+						-
1	0	1	0					+				-
1	0	1	1	NOT USED								
1	1	0	0		+							-
1	1	0	1				+					-
1	1	1	0						+			-
1	1	1	1	NOT USED								

MUX ADDRESS				SINGLE ENDED CHANNEL SELECTION										
SGL/DIFF	ODD/SIGN	SELECT		0	1	2	3	4	5	6	7	COM		
		1	0											
1	0	0	0	+										-
1	0	0	1			+								-
1	0	1	0					+						-
1	0	1	1								+			-
1	1	0	0		+									-
1	1	0	1				+							-
1	1	1	0						+					-
1	1	1	1									+		-

APPLICATIONS INFORMATION

MSB First/LSB First (MSBF)

The output data of the LTC1091/3/4 is programmed for MSB first or LSB first sequence using the MSBF bit. When the MSBF bit is a logical one, data will appear on the D_{OUT} line in MSB first format. Logical zeros will be filled in indefinitely following the last data bit to accommodate longer word lengths required by some microprocessors. When the MSBF bit is a logical zero, LSB first data will follow the normal MSB first data on the D_{OUT} line. (See operating sequence).

Unipolar/Bipolar (UNI)

The UNI bit of the LTC1093/4 determines whether the conversion will be unipolar or bipolar. When UNI is a logical one, a unipolar conversion will be performed on the selected input voltage. When UNI is a logical zero, a bipolar conversion will result. The input span and code assignment for each conversion type are shown in the figures below.

The LTC1091/2 are permanently configured for unipolar mode.

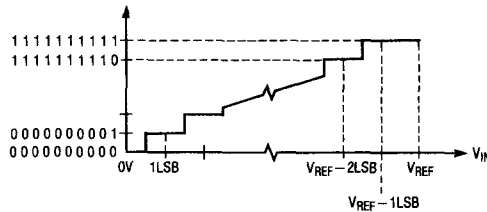
Unipolar Output Code (UNI = 1)

OUTPUT CODE	INPUT VOLTAGE	INPUT VOLTAGE (V _{REF} = 5V)
1111111111	V _{REF} - 1LSB	4.9951V
1111111110	V _{REF} - 2LSB	4.9902V
⋮	⋮	⋮
0000000001	1LSB	0.0049V
0000000000	0V	0V

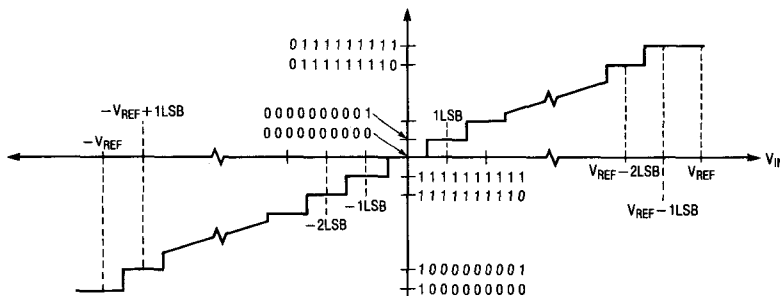
Bipolar Output Code (UNI = 0) LTC1093/4 Only

OUTPUT CODE	INPUT VOLTAGE	INPUT VOLTAGE (V _{REF} = 5V)
0111111111	V _{REF} - 1LSB	4.9902V
0111111110	V _{REF} - 2LSB	4.9805V
⋮	⋮	⋮
0000000001	1LSB	0.0098V
0000000000	0V	0V
1111111111	-1LSB	-0.0098V
1111111110	-2LSB	-0.0195V
⋮	⋮	⋮
1000000001	-(V _{REF}) + 1LSB	-4.9902V
1000000000	-(V _{REF})	-5.000V

Unipolar Transfer Curve (UNI = 1)



Bipolar Transfer Curve (UNI = 0) LTC1093/4 Only



APPLICATIONS INFORMATION

3. Accommodating Microprocessors with Different Word Lengths

The LTC1091/3/4 will fill zeroes indefinitely after the transmitted data until CS is brought high. At that time the D_{OUT} line is disabled. This makes interfacing easy to MPU serial ports with different transfer increments including 4 bits (e.g., COP400) and 8 bits (e.g., SPI and MICROWIRE/PLUS). Any word length can be accommodated by the correct positioning of the start bit in the LTC1091 input word.

Figure 1 shows examples of LTC1091 input and output words for 4-bit and 8-bit processors. A complete data exchange can be implemented with two 4-bit MPU outputs and three inputs in 4-bit systems and one 8-bit output and two inputs in 8-bit systems. The resulting data winds up left justified in the MPU with zeroes automatically filled in the unused low order bits by the LTC1091. In section 5 another example is given using the MC68HC05C4 which eliminates one 8-bit transfer and positions data right justified inside the MPU.

4. Operation with D_{IN} and D_{OUT} Tied Together

The LTC1091/3/4 can be operated with D_{IN} and D_{OUT} tied together. This eliminates one of the lines required to communicate to the MPU. Data is transmitted in both directions on a single wire. The processor pin connected to this data line should be configurable as either an input or an output. The LTC1091, for example, will take control of the data line and drive it low on the 4th falling CLK edge after the start bit is received (see Figure 2). Therefore the processor port line must be switched to an input before this happens, to avoid a conflict.

In the next section, an example is made of interfacing the LTC1091 with D_{IN} and D_{OUT} tied together to the Intel 8051 MPU.

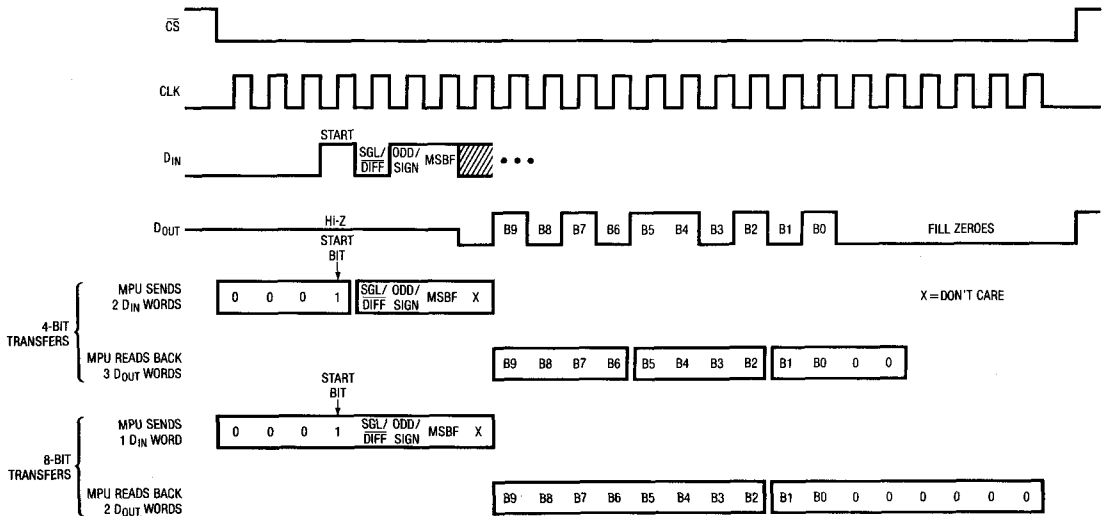


Figure 1. LTC1091 Input and Output Word Arrangements for 4-Bit and 8-Bit Serial Port Microprocessors

APPLICATIONS INFORMATION

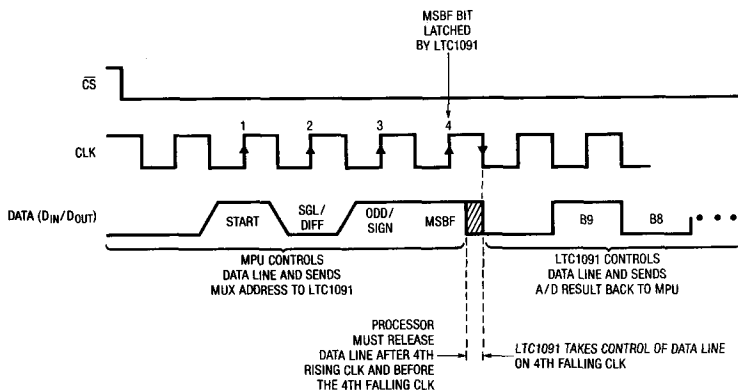


Figure 2. LTC1091 Operation with D_{IN} and D_{OUT} Tied Together

5. Microprocessor Interfaces

The LTC1091-4 can interface directly (without external hardware) to most popular microprocessor (MPU) synchronous serial formats (see Table 1). If an MPU without a dedicated serial port is used, then 3 or 4 of the MPU's parallel port lines can be programmed to form the serial link to the LTC1091-4. Included here are one serial interface example and one example showing a parallel port programmed to form the serial interface.

Table 1. Microprocessors with Hardware Serial Interfaces Compatible with the LTC1091-4

PART NUMBER	TYPE OF INTERFACE
Motorola	
MC6805S2, S3	SPI
MC68HC11	SPI
MC68HC05	SPI
RCA	
CDP68HC05	SPI
Hitachi	
HD6305	SCI Synchronous
HD63705	SCI Synchronous
HD6301	SCI Synchronous
HD63701	SCI Synchronous
HD6303	SCI Synchronous
HD64180	CSI/O
National Semiconductor	
COP400 Family	MICROWIRE†
COP800 Family	MICROWIRE/PLUS†
NS8050U	MICROWIRE/PLUS
HPC16000 Family	MICROWIRE/PLUS
Texas Instruments	
TMS7002	Serial Port
TMS7042	Serial Port
TMS70C02	Serial Port
TMS70C42	Serial Port
TMS32011*	Serial Port
TMS32020	Serial Port

*Requires external hardware

†MICROWIRE and MICROWIRE/PLUS are trademarks of National Semiconductor Corp.

APPLICATIONS INFORMATION

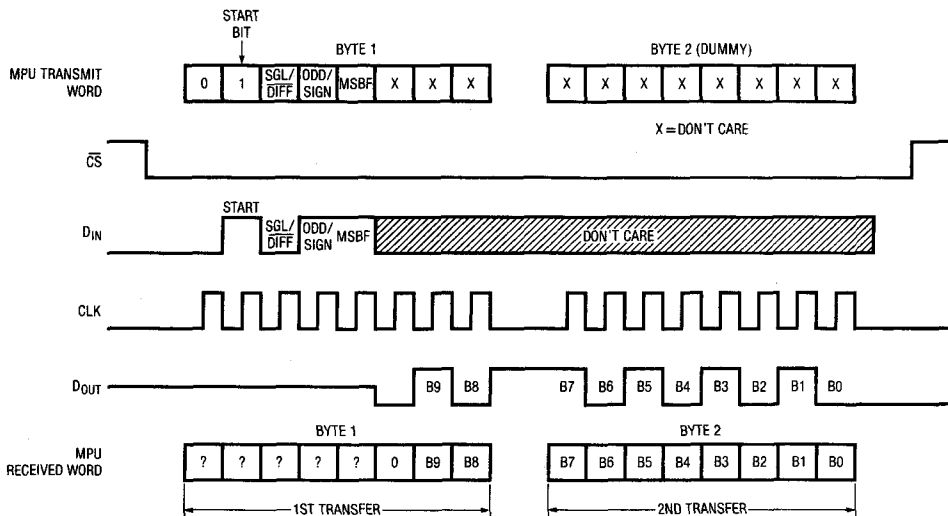
Motorola SPI (MC68HC05C4, MC68HC11)

The MC68HC05C4 has been chosen as an example of an MPU with a dedicated serial port. This MPU transfers data MSB first and in 8-bit increments. With two 8-bit transfers, the A/D result is read into the MPU. The first 8-bit transfer sends the D_{IN} word to the LTC1091 and clocks B9 and B8 of the A/D conversion result into the processor. The sec-

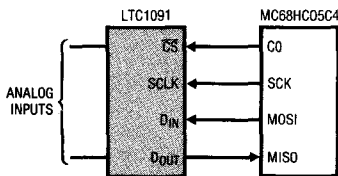
ond 8-bit transfer clocks the remaining bits, B7 through B0, into the MPU.

ANDing the first MPU received byte with 03 Hex clears the 6 most significant bits. Notice how the position of the start bit in the first MPU transmit word is used to position the A/D result right justified in two memory locations.

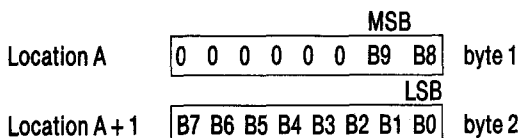
Data Exchange Between LTC1091 and MC68HC05C4



Hardware and Software Interface to Motorola MC68HC05C4 Microcontroller



D_{OUT} from LTC1091 stored in MC68HC05C4 RAM



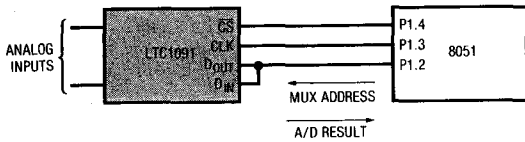
LABEL	MNEMONIC	COMMENTS
START	BCLRn	Bit 0 Port C goes low (\overline{CS} goes low)
	LDA	Load LTC1090 D_{IN} word into Acc.
	STA	Load LTC1090 D_{IN} word into SPI from Acc. Transfer begins.
	TST	Test status of SPIF
	BPL	Loop to previous instruction if not done with transfer
	LDA	Load contents of SPI data register into Acc. (D_{OUT} MSBs)
	STA	Start next SPI cycle
	AND	Clear 6 MSBs of first D_{OUT} word
	STA	Store in memory location A (MSBs)
	TST	Test status of SPIF
	BPL	Loop to previous instruction if not done with transfer
	BSETn	Set B0 of Port C (\overline{CS} goes high)
	LDA	Load contents of SPI data register into Acc. (D_{OUT} LSBs)
	STA	Store in memory location A + 1 (LSBs)

APPLICATIONS INFORMATION

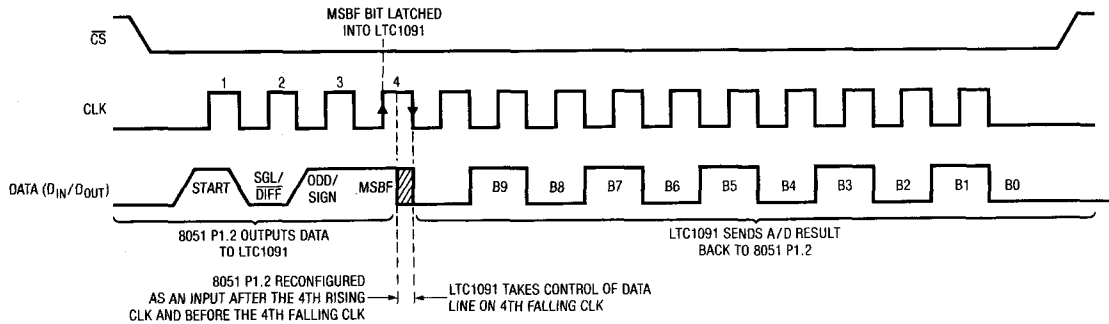
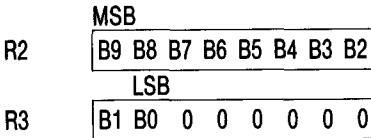
Interfacing to the Parallel Port of the Intel 8051 Family

The Intel 8051 has been chosen to demonstrate the interface between the LTC1091 and parallel port microprocessors. Normally the CS, SCLK and D_{IN} signals would be generated on 3 port lines and the D_{OUT} signal read on a 4th port line. This works very well. However, we will demonstrate here an interface with the D_{IN} and D_{OUT} of the LTC1091 tied together as described in section 4. This saves one wire.

The 8051 first sends the start bit and MUX address to the LTC1091 over the data line connected to P1.2. Then P1.2 is reconfigured as an input (by writing to it a one) and the 8051 reads back the 10-bit A/D result over the same data line.



D_{OUT} from LTC1091 stored in 8051 RAM



LABEL	MNEMONIC	OPERAND	COMMENTS
LOOP1	MOV	A, #FFH	D _N word for LTC1091
	SETB	P1.4	Make sure CS is high
	CLR	P1.4	CS goes low
	MOV	R4, #04	Load counter
	RLC	A	Rotate D _{IN} bit into Carry
LOOP	CLR	P1.3	SCLK goes low
	MOV	P1.2, C	Output D _{IN} bit to LTC1091
	SETB	P1.3	SCLK goes high
	DJNZ	R4, LOOP1	Next bit
	MOV	P1, #04	Bit 2 becomes an input
	CLR	P1.3	SCLK goes low
	MOV	R4, #09	Load counter
	MOV	C, P1.2	Read data bit into Carry
	RLC	A	Rotate data bit into Acc.
	SETB	P1.3	SCLK goes high
	CLR	P1.3	SCLK goes low
	DJNZ	R4, LOOP	Next bit
	MOV	R2, A	Store MSBs in R2
	MOV	C, P1.2	Read data bit into Carry
	SETB	P1.3	SCLK goes high
	CLR	P1.3	SCLK goes low
	CLR	A	Clear Acc.
	RLC	A	Rotate data bit from Carry to Acc.
	MOV	C, P1.2	Read data bit into Carry
RRC	A	Rotate right into Acc.	
RRC	A	Rotate right into Acc.	
MOV	R3, A	Store LSBs in R3	
SETB	P1.4	CS goes high	

APPLICATIONS INFORMATION

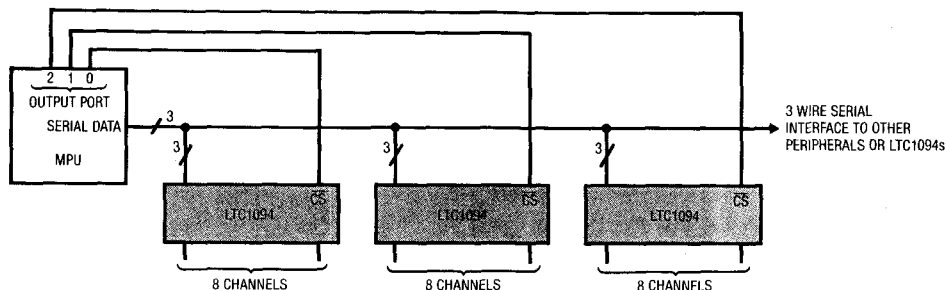


Figure 3. Several LTC1094s Sharing One 3 Wire Serial Interface

Sharing the Serial Interface

The LTC1094 can share the same 2 or 3 wire serial interface with other peripheral components or other LTC1094s (see Figure 3). In this case, the CS signals decide which LTC1094 is being addressed by the MPU.

ANALOG CONSIDERATIONS

1. Grounding

The LTC1091-4 should be used with an analog ground plane and single point grounding techniques.

The AGND pin (GND on the LTC1091/2) should be tied directly to this ground plane.

The DGND pin of the LTC1093/4 can also be tied directly to this ground plane because minimal digital noise is generated within the chip itself.

The V_{CC} pin should be bypassed to the ground plane with a $4.7\mu\text{F}$ tantalum with leads as short as possible. AV_{CC} and DV_{CC} should be tied together on the LTC1094. The V^- pin (LTC1093/4) should be bypassed with a $0.1\mu\text{F}$ ceramic disk. For single supply applications, V^- can be tied to the ground plane.

It is also recommended that the REF^- pin and the COM pin be tied directly to the ground plane. All analog inputs should be referenced directly to the single point ground. Digital inputs and outputs should be shielded from and/or routed away from the reference and analog circuitry.

Figure 4 shows an example of an ideal LTC1091 ground plane design for a two sided board. Of course this much ground plane will not always be possible, but users should strive to get as close to this ideal as possible.

2. Bypassing

For good performance, V_{CC} must be free of noise and ripple. Any changes in the V_{CC} voltage with respect to analog ground during a conversion cycle can induce errors or noise in the output code. Because the V_{CC} (V_{REF}) pin of the LTC1091 defines the voltage span of the A/D converter, its bypassing is especially important. V_{CC} noise and ripple can be kept below 1mV by bypassing the V_{CC} pin directly to the analog ground plane with a $4.7\mu\text{F}$ tantalum with leads as short as possible. AV_{CC} and DV_{CC} should be tied together on the LTC1094. Figures 5 and 6 show the effects of good and poor V_{CC} bypassing.

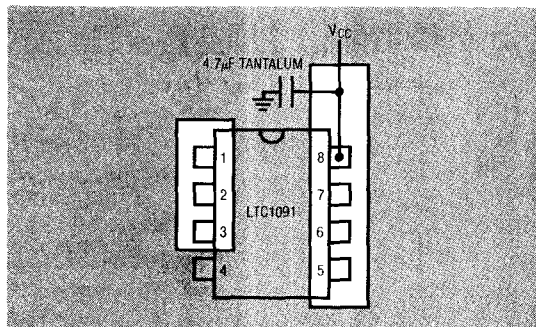


Figure 4. Example Ground Plane for the LTC1091

APPLICATIONS INFORMATION

3. Analog Inputs

Because of the capacitive redistribution A/D conversion techniques used, the analog inputs of the LTC1091-4 have capacitive switching input current spikes. These current spikes settle quickly and do not cause a problem. However, if large source resistances are used or if slow settling op amps drive the inputs, care must be taken to insure that the transients caused by the current spikes settle completely before the conversion begins.

Source Resistance

The analog inputs of the LTC1091-4 look like a 60pF capacitor (C_{IN}) in series with a 500 Ω resistor (R_{ON}) as shown in Figure 7. C_{IN} gets switched between the selected “+” and “-” inputs once during each conversion cycle. Large external source resistors and capacitances will slow the settling of the inputs. It is important that the overall RC time constants be short enough to allow the analog inputs to completely settle within the allowed time.

“+” Input Settling

This input capacitor is switched onto the “+” input during the sample phase (t_{SMPL} , see Figure 8). The sample phase is the 1 1/2 CLK cycles before the conversion starts. The voltage on the “+” input must settle completely within this sample time. Minimizing R_{SOURCE}^+ and $C1$ will improve the input settling time. If large “+” input source resistance must be used, the sample time can be increased by using a slower CLK frequency. With the minimum possible sample time of 3 μ s, $R_{SOURCE}^+ < 2k$ and $C1 < 20pF$ will provide adequate settling.

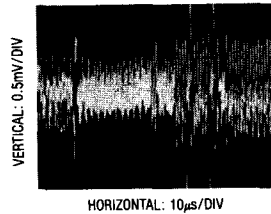


Figure 5. Poor V_{CC} Bypassing. Noise and Ripple Can Cause A/D Errors

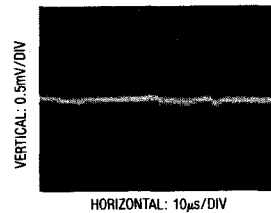


Figure 6. Good V_{CC} Bypassing Keeps Noise and Ripple On V_{CC} Below 1mV

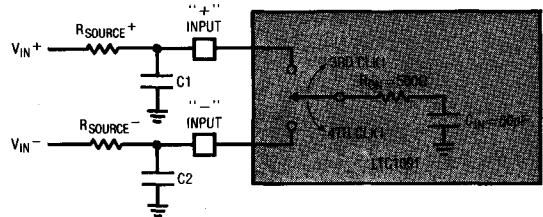


Figure 7. Analog Input Equivalent Circuit

APPLICATIONS INFORMATION

"-" Input Settling

At the end of the sample phase the input capacitor switches to the "-" input and the conversion starts (see Figure 8). During the conversion, the "+" input voltage is effectively "held" by the sample and hold and will not affect the conversion result. However, it is critical that the "-" input voltage settle completely during the first CLK cycle of the conversion time and be free of noise. Minimizing R_{SOURCE^-} and C2 will improve settling time. If large "-" input source resistance must be used, the time allowed for settling can be extended by using a slower CLK frequency. At the maximum CLK rate of 500kHz, $R_{SOURCE^-} < 1k\Omega$ and $C2 < 20pF$ will provide adequate settling.

Input Op Amps

When driving the analog inputs with an op amp it is important that the op amp settle within the allowed time (see Figure 8). Again, the "+" and "-" input sampling times can be extended as described above to accommodate slower op amps. Most op amps including the LT1006 and LT1013 single supply op amps, can be made to settle well even with the minimum settling windows of $3\mu s$ ("+" input) and $2\mu s$ ("- input) which occur at the maximum clock rate of 500kHz. Figures 9 and 10 show examples of adequate and poor op amp settling.

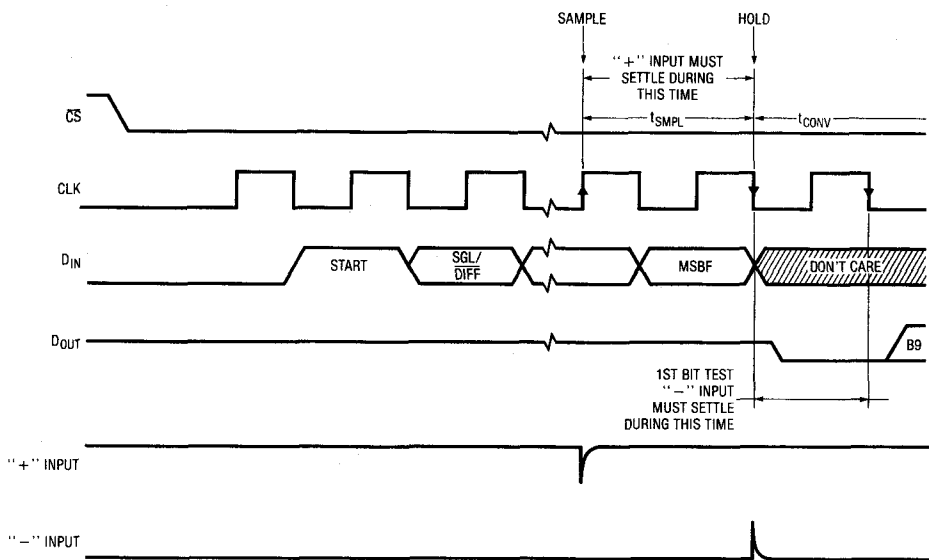


Figure 8. "+" and "-" Input Settling Windows

APPLICATIONS INFORMATION

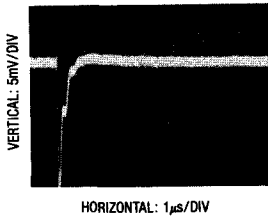


Figure 9. Adequate Settling of Op Amp Driving Analog Input

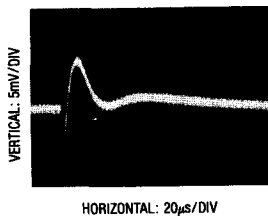


Figure 10. Poor Op Amp Settling Can Cause A/D Errors

RC Input Filtering

It is possible to filter the inputs with an RC network as shown in Figure 11. For large values of C_F (e.g., $1\mu\text{F}$), the capacitive input switching currents are averaged into a net DC current. Therefore, a filter should be chosen with a small resistor and large capacitor to prevent DC drops across the resistor. The magnitude of the DC current is approximately $I_{DC} = 60\text{pF} \times V_{IN}/t_{CYC}$ and is roughly proportional to V_{IN} . When running at the minimum cycle time of $32\mu\text{s}$, the input current equals $9\mu\text{A}$ at $V_{IN} = 5\text{V}$. In this case, a filter resistor of 50Ω will cause 0.1LSB of full-scale error. If a larger filter resistor must be used, errors can be eliminated by increasing the cycle time as shown in the typical curve of Maximum Filter Resistor vs Cycle Time.

Input Leakage Current

Input leakage currents can also create errors if the source resistance gets too large. For instance, the maximum input leakage specification of $1\mu\text{A}$ (at 125°C) flowing through a source resistance of $1\text{k}\Omega$ will cause a voltage drop of 1mV or 0.2LSB . This error will be much reduced at lower temperatures because leakage drops rapidly (see typical curve of Input Channel Leakage Current vs Temperature).

4. Sample and Hold

Single Ended Inputs

The LTC1091, LTC1093 and LTC1094 provide a built-in sample and hold (S&H) function for signals acquired in the single ended mode. This sample and hold allows conversion of rapidly varying signals (see typical curve of S&H Acquisition Time vs Source Resistance). The input voltage is sampled during the t_{SAMPL} time as shown in Figure 8. The sampling interval begins as the bit preceding the MSBF bit is shifted in and continues until the falling CLK edge after the MSBF bit is received. On this falling edge, the S&H goes into hold mode and the conversion begins.

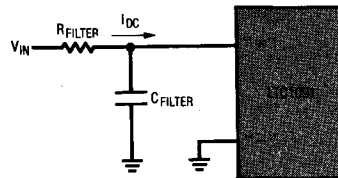


Figure 11. RC Input Filtering

APPLICATIONS INFORMATION

Differential Inputs

With differential inputs, the A/D no longer converts just a single voltage but rather the difference between two voltages. In this case, the voltage on the selected “+” input is still sampled and held and therefore may be rapidly time varying just as in single ended mode. However, the voltage on the selected “-” input must remain constant and be free of noise and ripple throughout the conversion time. Otherwise, the differencing operation may not be performed accurately. The conversion time is 10 CLK cycles. Therefore, a change in the “-” input voltage during this interval can cause conversion errors. For a sinusoidal voltage on the “-” input this error would be:

$$V_{\text{ERROR (MAX)}} = V_{\text{PEAK}} \times 2 \times \pi \times f(\text{“-”}) \times 10/f_{\text{CLK}}$$

Where $f(\text{“-”})$ is the frequency of the “-” input voltage, V_{PEAK} is its peak amplitude and f_{CLK} is the frequency of the CLK. In most cases V_{ERROR} will not be significant. For a 60Hz signal on the “-” input to generate a 1/4LSB error (1.25mV) with the converter running at $\text{CLK} = 500\text{kHz}$, its peak value would have to be 150mV.

5. Reference Inputs

The voltage on the reference inputs of the LTC1091-4 defines the voltage span of the A/D converter. The reference inputs look primarily like a 10kΩ resistor but will have transient capacitive switching currents due to the switched capacitor conversion technique (see Figure 12). During each bit test of the conversion (every CLK cycle), a capacitive current spike will be generated on the reference pins by the A/D. These current spikes settle quickly and do not cause a problem. However, if slow settling circuitry is used to drive the reference inputs, care must be taken to ensure that transients caused by these current spikes settle completely during each bit test of the conversion.

When driving the reference inputs, three things should be kept in mind:

1. The source resistance (R_{OUT}) driving the reference inputs should be low (less than 1Ω) to prevent DC drops caused by the 1mA maximum reference current (I_{REF}).

2. Transients on the reference inputs caused by the capacitive switching currents must settle completely during each bit test (each CLK cycle). Figures 13 and 14 show examples of both adequate and poor settling. Using a slower CLK will allow more time for the reference to settle. However, even at the maximum CLK rate of 500kHz most references and op amps can be made to settle within the 2μs bit time.
3. It is recommended that the REF- input of the LTC1094 be tied directly to the analog ground plane. If REF- is biased at a voltage other than ground, the voltage must not change during a conversion cycle. This voltage must also be free of noise and ripple with respect to analog ground.

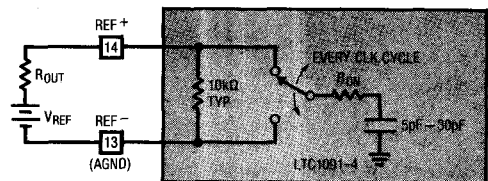


Figure 12. Reference Input Equivalent Circuit

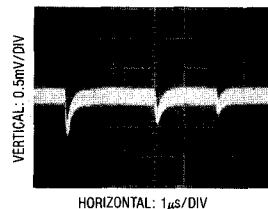


Figure 13. Adequate Reference Settling

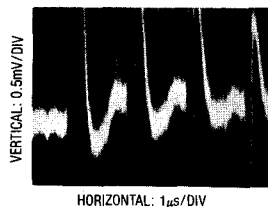


Figure 14. Poor Reference Settling Can Cause A/D Errors

APPLICATIONS INFORMATION

6. Reduced Reference Operation

The minimum reference voltage of the LTC1091 is limited to 4.5V because the V_{CC} supply and reference are internally tied together. However, the LTC1092/3/4 can operate with reference voltages below 1V.

The effective resolution of the LTC1092/3/4 can be increased by reducing the input span of the converter. The LTC1092/3/4 exhibits good linearity and gain over a wide range of reference voltages (see typical curves of Linearity and Full Scale Error vs Reference Voltage). However, care must be taken when operating at low values of V_{REF} because of the reduced LSB step size and the resulting higher accuracy requirement placed on the converter. The following factors must be considered when operating at low V_{REF} values.

1. Offset
2. Noise
3. Conversion speed (CLK frequency)

Offset with Reduced V_{REF}

The offset of the LTC1092/3/4 has a larger effect on the output code when the A/D is operated with reduced reference voltage. The offset (which is typically a fixed voltage) becomes a larger fraction of an LSB as the size of the LSB is reduced. The typical curve of Unadjusted Offset Error vs Reference Voltage shows how offset in LSBs is related to reference voltage for a typical value of V_{OS} . For example, a V_{OS} of 0.5mV which is 0.1LSB with a 5V reference becomes 0.5LSB with a 1V reference and 2.5LSBs with a 0.2V reference. If this offset is unacceptable, it can be corrected digitally by the receiving system or by offsetting the “-” input to the LTC1092/3/4.

Noise with Reduced V_{REF}

The total input referred noise of the LTC1092/3/4 can be reduced to approximately 200 μ V peak-to-peak using a ground plane, good bypassing, good layout techniques and minimizing noise on the reference inputs. This noise is insignificant with a 5V reference but will become a larger fraction of an LSB as the size of the LSB is reduced. The typical curve of Noise Error vs Reference Voltage shows the LSB contribution of this 200 μ V of noise.

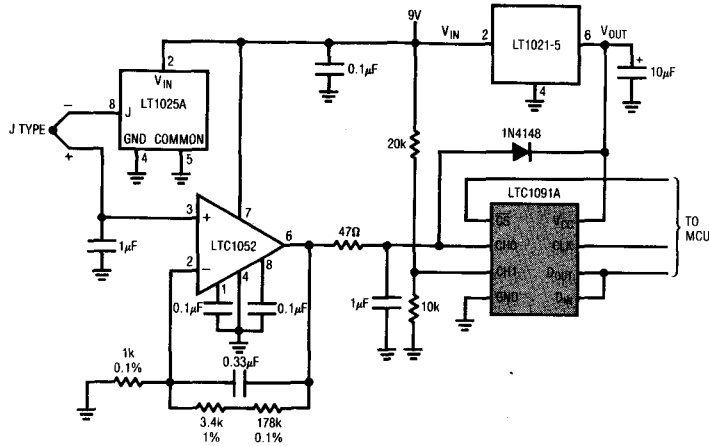
For operation with a 5V reference, the 200 μ V noise is only 0.04LSB peak-to-peak. In this case, the LTC1092/3/4 noise will contribute virtually no uncertainty to the output code. However, for reduced references, the noise may become a significant fraction of an LSB and cause undesirable jitter in the output code. For example, with a 1V reference, this same 200 μ V noise is 0.2LSB peak-to-peak. This will reduce the range of input voltages over which a stable output code can be achieved by 0.2LSB. If the reference is further reduced to 200mV, the 200 μ V noise becomes equal to one LSB and a stable code may be difficult to achieve. In this case averaging readings may be necessary.

This noise data was taken in a very clean setup. Any setup induced noise (noise or ripple on V_{CC} , V_{REF} , V_{IN} or V^-) will add to the internal noise. The lower the reference voltage to be used, the more critical it becomes to have a clean, noise-free setup.

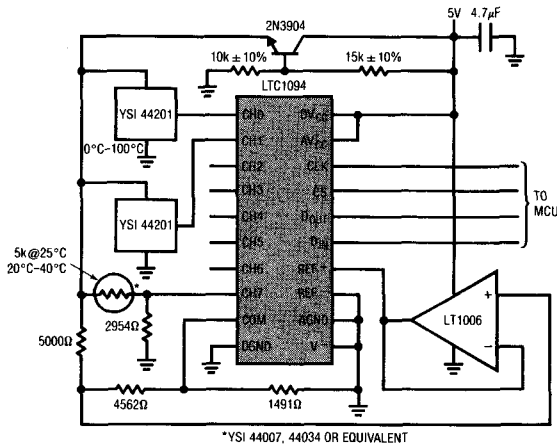
Conversion Speed with Reduced V_{REF}

With reduced reference voltages, the LSB step size is reduced and the LTC1092/3/4 internal comparator overdrive is reduced. Therefore, it may be necessary to reduce the maximum CLK frequency when low values of V_{REF} are used.

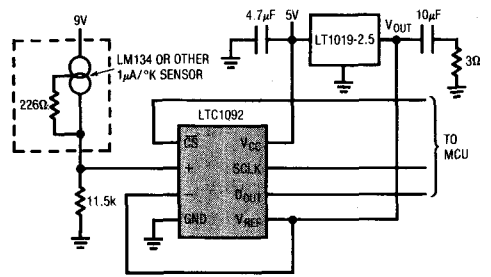
TYPICAL APPLICATIONS



0°C-500°C Furnace Exhaust Gas Temperature Monitor with Low Supply Detection



0°C-100°C 0.25°C Accurate Thermistor Based Temperature Measurement System



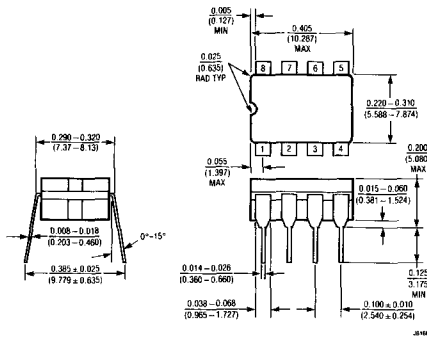
-55°C to +125°C Thermometer Using Current Output Silicon Sensors

LTC1091/LTC1092
LTC1093/LTC1094

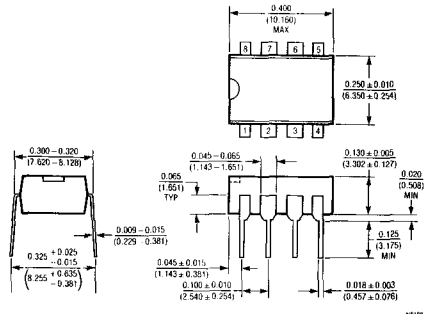
PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

J Package	T _{jmax} 150°C	θ _{JA} 100°C/W
N Package	T _{jmax} 110°C	θ _{JA} 150°C/W

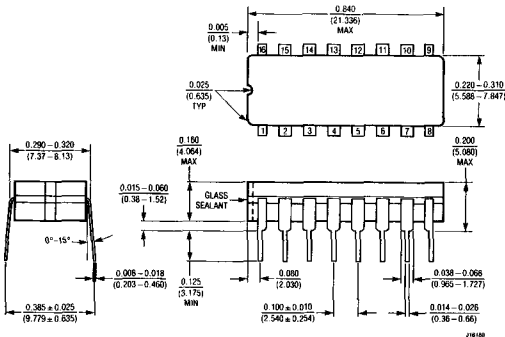
J Package
8 Lead Ceramic DIP



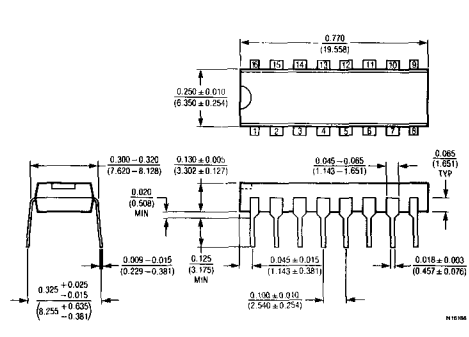
N Package
8 Lead Plastic DIP



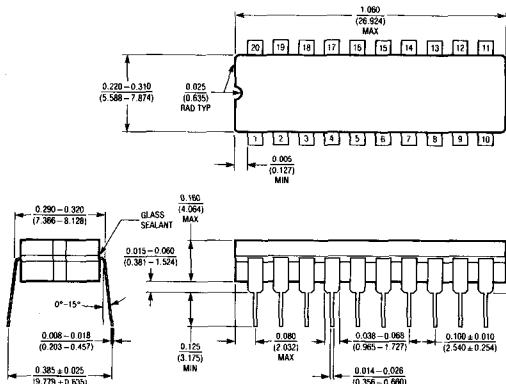
J Package
16 Lead Ceramic DIP



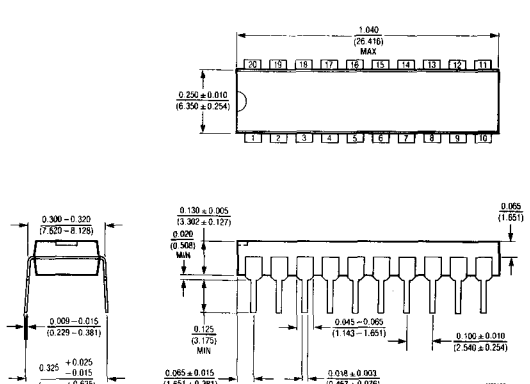
N Package
16 Lead Plastic DIP



J Package
20 Lead Ceramic DIP



N Package
20 Lead Plastic DIP



Complete 10-Bit Data Acquisition System with On Board Reference

FEATURES

- On Board 5V Precision Buried Zener Reference
- Software Controlled 6 Channel Multiplexer
- Differential and Single Ended Input Capability
- Built-In Sample and Hold for Single Ended Inputs
- Analog Inputs Common Mode to Both Supply Rails
- Single Supply (7.2V to 40V) or Split Supply Operation
- 10 Bit Unipolar or 9 Bit Plus Sign Bipolar
- 2's Complement Output Coding on Bipolar Conversions
- Direct Interface to Most Microprocessor Serial Data Ports Including Motorola SPI, Hitachi SCI and National MICROWIRE/PLUS*
- Software Interface to Other Microprocessor Parallel Ports
- MSB or LSB First Data

KEY SPECIFICATIONS

- Resolution 10 Bits
- Linearity Error $\pm 0.5\text{LSB}$ (0.05% FSR) Max
- Total Unadjusted Error $\pm 0.15\%$ FSR
- Conversion Time 20 μs
- Sampling Rate 25kHz
- Supply Current 4.7mA Max, 2.3mA Typ
- Full Scale Error Temperature Drift (B Grade) 23ppm/ $^{\circ}\text{C}$ Max

*MICROWIRE/PLUS is a trademark of National Semiconductor.

DESCRIPTION

The LTC1095 is a complete data acquisition component which contains a serial I/O, successive approximation A/D converter, a 6 channel multiplexer, a sample and hold, and an on board reference. It uses LTCMOS™ switched capacitor technology to perform either 10 bit unipolar, or 9 bit plus sign bipolar A/D conversions. The 6 channel input multiplexer can be software configured for either single ended or differential inputs (or combinations thereof). The on chip sample and hold is included for all single ended input channels. The LTC1095 is specified as a complete system. This specification includes the error contribution of the A/D, MUX, S&H, and reference.

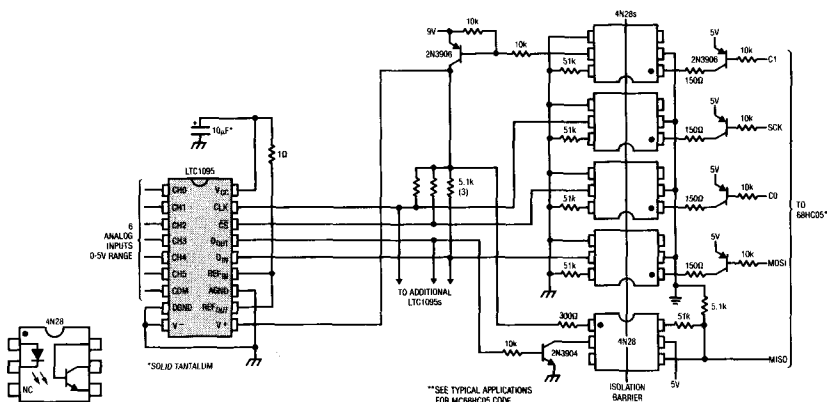
The serial I/O is designed to be compatible with industry standard serial interfaces. It allows either MSB or LSB first data and automatically provides 2's complement output coding in the bipolar mode. This allows easy interface to shift registers and a variety of processors.

All grades of the LTC1095 have guaranteed maximum offset and linearity errors of $\pm 0.5\text{LSB}$ over the full operating temperature range. The LTC1095B is specified with gain error less than $\pm 0.1\%$ maximum.

The LTC1095C is specified with a gain error limit of $\pm 0.2\%$ FSR maximum.

TYPICAL APPLICATIONS

Micropower, 500V Opto Isolated, Multichannel, 10-Bit Data Acquisition System



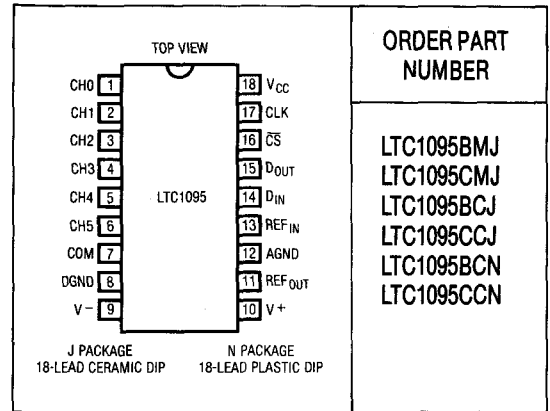
LTC1095

ABSOLUTE MAXIMUM RATINGS

(Notes 1 and 2)

Supply Voltage (V^+) to GND	40V
Supply Voltage (V_{CC}) to GND or V^-	12V
Negative Supply Voltage (V^-)	-6V to GND Voltage
Analog and Reference Inputs .. (V^-) - 0.3V to $V_{CC} + 0.3V$	
Digital Inputs	-0.3V to 12V
Digital Outputs	-0.3V to $V_{CC} + 0.3V$
Power Dissipation	500mW
Operating Temperature Range	
LTC1095BC, LTC1095CC	0°C to 70°C
LTC1095BM, LTC1095CM	-55°C to 125°C
Storage Temperature Range	-65°C to 150°C
Lead Temperature (Soldering, 10 sec.)	300°C

PACKAGE/ORDER INFORMATION



CONVERTER AND MULTIPLEXER CHARACTERISTICS (Note 3)

(With internal reference)

PARAMETER	CONDITIONS (See Schematic of Figure 1)	LTC1095B			LTC1095C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Offset Error	(Notes 4 and 5)	●		±0.5			±0.5	LSB
Linearity Error		●		±0.5			±0.5	
Gain Error	(Note 4)			±0.1			±0.2	%FSR
	Commercial Range	●		±0.15			±0.3	
	Military Range	●		±0.2			±0.4	
Total Unadjusted Error	(Notes 4 and 6)			±0.15			±0.25	%FSR
	Commercial Range	●		±0.2			±0.35	
	Military Range	●		±0.25			±0.45	
Full Scale Error Temperature Coefficient	Commercial Grade		(Note 9)			(Note 9)		ppm/°C
	Military Grade (Note 10)	●		23			45	

INTERNAL REFERENCE CHARACTERISTICS (Note 3)

PARAMETER	CONDITIONS	LTC1095B			LTC1095C			UNITS	
		MIN	TYP	MAX	MIN	TYP	MAX		
Output Voltage			5.000			5.000		V	
Output Voltage Temperature Coefficient			2			5		ppm/°C	
Line Regulation	$7.2V \leq V^+ \leq 10V$	●	4	12	20	4	12	20	ppm/V
	$10V \leq V^+ \leq 40V$	●	2	6	10	2	6	10	
Load Regulation (Sourcing Current)	$0 \leq I_{REF_OUT} \leq 10mA$	●	10	25	40	10	25	40	ppm/mA
Load Regulation (Sinking Current)	$0 \leq I_{REF_OUT} \leq 10mA$	●	60	150	200	60	150	200	

DIGITAL AND DC ELECTRICAL CHARACTERISTICS (Note 3)

SYMBOL	PARAMETER	CONDITIONS	LTC1095B/LTC1095C			UNITS
			MIN	TYP	MAX	
V_{IH}	High Level Input Voltage	$V_{CC} = 5.25V$	●	2.0		V
V_{IL}	Low Level Input Voltage	$V_{CC} = 4.75V$	●		0.8	V
I_{IH}	High Level Input Current	$V_{IN} = V_{CC}$	●		2.5	μA
I_{IL}	Low Level Input Current	$V_{IN} = 0V$	●		-2.5	μA
V_{OH}	High Level Output Voltage	$V_{CC} = 4.75V, I_O = 10\mu A$ $I_O = 360\mu A$	●	2.4	4.7	V
			●		4.0	V
V_{OL}	Low Level Output Voltage	$V_{CC} = 4.75V, I_O = 1.6mA$	●		0.4	V
I_{OZ}	Hi-Z Output Leakage	$V_{OUT} = V_{CC}, CS \text{ High}$ $V_{OUT} = 0V, CS \text{ High}$	●		3	μA
			●		-3	μA
I_{SOURCE}	Output Source Current	$V_{OUT} = 0V$		-10		mA
I_{SINK}	Output Sink Current	$V_{OUT} = V_{CC}$		10		mA
I_{CC}	Positive Supply Current	$CS \text{ High}, REF^+ \text{ Open}$	●	1.0	2.5	mA
I_{REFIN}	Reference Input Current	$REF_{IN} = 5V$	●	0.5	1.0	mA
I^-	Negative Supply Current	$CS \text{ High}$	●	1	50	μA
I^+	On Chip Reference Current	$V^+ = 10V, REF_{OUT} \text{ Open}$	●	0.8	1.2	mA
	Reference Input Resistance			10		k Ω
	Analog and REF Input Range	(Note 7)		$(V^-) - 0.05V \text{ to } V_{CC} + 0.05V$		V
	On Channel Leakage Current (Note 8)	On Channel = 5V Off Channel = 0V	●		1	μA
		On Channel = 0V Off Channel = 5V	●		-1	
	Off Channel Leakage Current (Note 8)	On Channel = 5V Off Channel = 0V	●		-1	μA
		On Channel = 0V Off Channel = 5V	●		1	

AC CHARACTERISTICS (Note 3)

SYMBOL	PARAMETER	CONDITIONS	LTC1095B/LTC1095C		UNITS
			MIN	TYP MAX	
t_{SMP}	Analog Input Sample Time	See Operating Sequence		1.5	CLK Cycles
t_{CONV}	Conversion Time	See Operating Sequence		10	CLK Cycles
t_{D0}	Delay Time, CLK1 to D_{OUT} Data Valid	See Parameter Measurement Section	●	400 850	ns
t_{dis}	Delay Time, $\overline{CS1}$ to D_{OUT} Hi-Z	See Parameter Measurement Section	●	180 450	ns
t_{en}	Delay Time, CLK1 to D_{OUT} Enabled	See Parameter Measurement Section	●	160 450	ns
t_{D0}	Time Output Data Remains Valid After CLK1			150	ns
t_f	D_{OUT} Fall Time	See Parameter Measurement Section	●	90 300	ns
t_r	D_{OUT} Rise Time	See Parameter Measurement Section	●	60 300	ns
C_{IN}	Input Capacitance	Analog Inputs On Channel		65	pF
		Off Channel		5	pF
		Digital Inputs		5	pF

Note 1: Absolute maximum ratings are those values beyond which the life of a device may be impaired.

Note 2: All voltage values are with respect to ground with DGND, AGND, and REF^- wired together (unless otherwise noted).

Note 3: $V_{CC} = 5V$, $REF_{IN} = REF_{OUT}$, $V^+ = 10V$, $I_{REF_{OUT}} = 0$, $V^- = 0V$ for unipolar mode and $-5V$ for bipolar mode, $CLK = 0.5MHz$ unless otherwise specified. The ● indicates specs which apply over the full operating temperature range; all other limits and typicals $T_A = 25^\circ C$.

Note 4: These specs apply for both unipolar and bipolar modes. In bipolar mode, one LSB is equal to the bipolar input span ($2REF_{IN}$) divided by 1024. For example, when $REF_{IN} = 5V$, $1LSB$ (bipolar) = $2(5V)/1024 = 9.77mV$.

Note 5: Linearity error is specified between the actual end points of the A/D transfer curve.

Note 6: Total unadjusted error includes offset, full scale, linearity, multiplexer, reference and hold step errors.

Note 7: Two on-chip diodes are tied to each reference and analog input which will conduct for reference or analog input voltages one diode drop

below V^- or one diode drop above V_{CC} . Be careful during testing at low V_{CC} levels (4.5V), as high level reference or analog inputs (5V) can cause this input diode to conduct, especially at elevated temperatures, and cause errors for inputs near full-scale. This spec allows 50mV forward bias of either diode. This means that as long as the reference or analog input does not exceed the supply voltage by more than 50mV, the output code will be correct. To achieve an absolute 0V to 5V input voltage range will therefore require a minimum supply voltage of 4.950V over initial tolerance, temperature variations and loading.

Note 8: Channel leakage current is measured after the channel selection.

Note 9: For commercial grade parts with tested and specified T.C. consult the factory.

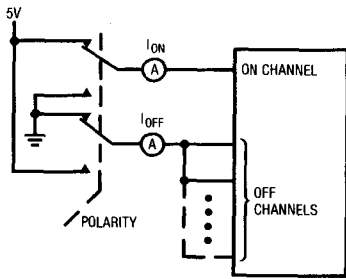
Note 10: This is specified for both unipolar and bipolar modes via the "box" method. The lowest of three readings (T_{MIN} , T_{ROOM} , T_{MAX}) subtracted from the highest and divided by $T_{MAX} - T_{MIN}$ is guaranteed to be less than the specified T.C. These numbers are guaranteed by the MIL range gain error test limits. For tighter T.C. specifications, consult the factory.

RECOMMENDED OPERATING CONDITIONS

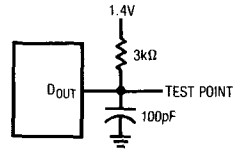
SYMBOL	PARAMETER	CONDITIONS	LTC1095B/LTC1095C		UNITS
			MIN	MAX	
V_{CC}	Supply Voltage		4.5	10	V
V^-	Negative Supply Voltage	$V_{CC} = 5V$	-5.5	0	V
f_{CLK}	Clock Frequency	$V_{CC} = 5V$	0.01	0.5	MHz
t_{CYC}	Total Cycle Time		18 CLK Cycles + $2\mu s$		
t_{HDI}	Hold Time, D_{IN} After SCLK1	$V_{CC} = 5V$	150		ns
$t_{SU\overline{CS}}$	Setup Time $\overline{CS1}$ Before CLK1	$V_{CC} = 5V$	1		μs
t_{SUDI}	Setup Time, D_{IN} Stable Before CLK1	$V_{CC} = 5V$	400		ns
t_{WHCLK}	CLK High Time	$V_{CC} = 5V$	0.8		μs
t_{WLCLK}	CLK Low Time	$V_{CC} = 5V$	1		μs
$t_{WH\overline{CS}}$	\overline{CS} High Time Between Data Transfer Cycles	$V_{CC} = 5V$	2		μs
$t_{WL\overline{CS}}$	\overline{CS} Low Time During Data Transfer		18		CLK Cycles

TEST CIRCUITS

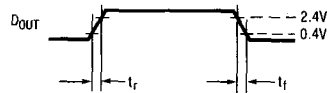
On and Off Channel Leakage Current



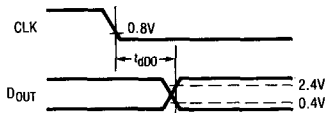
Load Circuit for t_{dDO} , t_r , and t_f



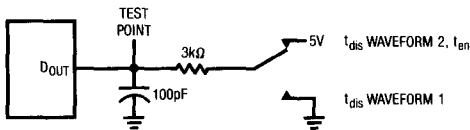
Voltage Waveforms for D_{OUT} Rise and Fall Times, t_r , t_f



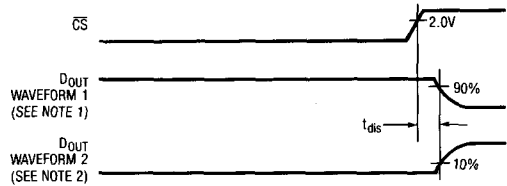
Voltage Waveforms for D_{OUT} Delay Time, t_{dDO}



Load Circuit for t_{dis} and t_{en}



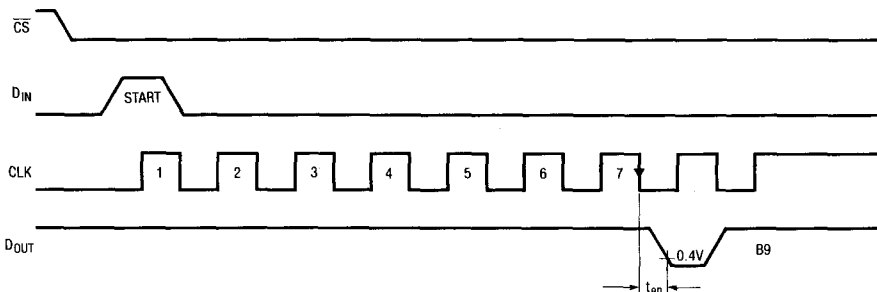
Voltage Waveforms for t_{dis}



NOTE 1: WAVEFORM 1 IS FOR AN OUTPUT WITH INTERNAL CONDITIONS SUCH THAT THE OUTPUT IS HIGH UNLESS DISABLED BY THE OUTPUT CONTROL.

NOTE 2: WAVEFORM 2 IS FOR AN OUTPUT WITH INTERNAL CONDITIONS SUCH THAT THE OUTPUT IS LOW UNLESS DISABLED BY THE OUTPUT CONTROL.

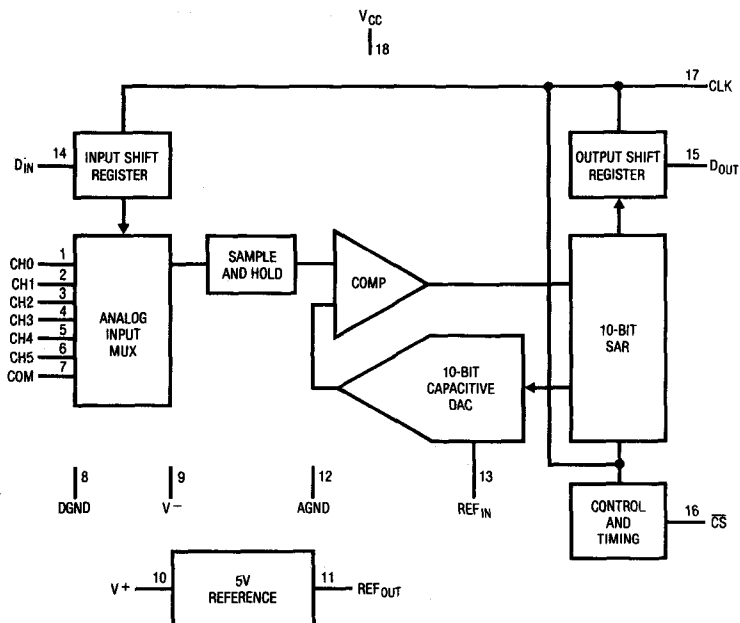
Voltage Waveforms for t_{en}



PIN FUNCTIONS

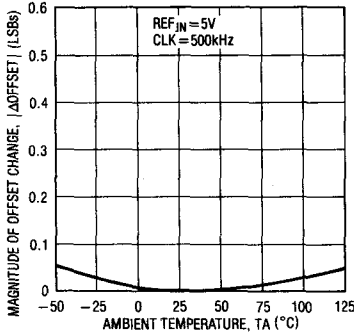
LTC1095 #	PIN	FUNCTION	DESCRIPTION
1-6 7	CH0-CH5 COM	Analog Inputs Common	The analog inputs must be free of noise with respect to AGND. The common pin defines the zero reference point for all single ended inputs. It must be free of noise and is usually tied to the analog ground plane.
8	DGND	Digital Ground	This is the ground for the internal logic. Tie to the ground plane.
9	V-	Negative Supply	Tie V- to most negative potential in the circuit. (Ground in single supply applications.)
10	V+	Reference Supply	Supply pin for on board reference.
11	REF _{OUT}	Reference Output	Output of on board reference.
12	AGND	Analog Ground	AGND should be tied directly to the analog ground plane.
13	REF _{IN}	Reference Input	The reference input must be kept free of noise with respect to AGND.
14	D _{IN}	Data Input	The A/D configuration word is shifted into this input.
15	D _{OUT}	Digital Data Output	The A/D conversion result is shifted out of this output.
16	CS	Chip Select Input	A logic low on this input enables the LTC1095.
17	CLK	Shift Clock	This clock synchronizes the serial data transfer.
18	V _{CC}	Positive Supply	This supply must be kept free of noise and ripple by bypassing directly to the analog ground plane.

BLOCK DIAGRAM

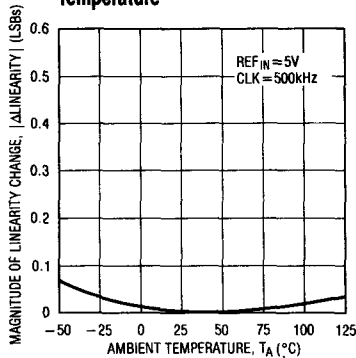


TYPICAL PERFORMANCE CHARACTERISTICS

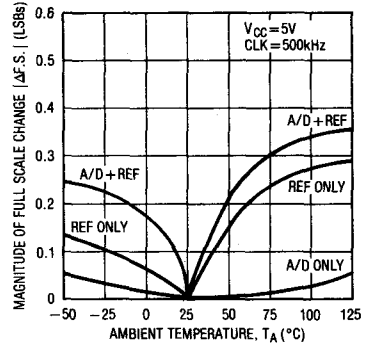
Change in Offset Error vs Temperature



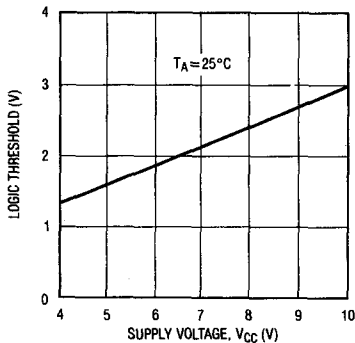
Change in Linearity Error vs Temperature



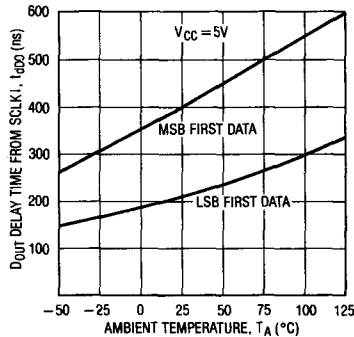
Change in Full Scale Error vs Temperature



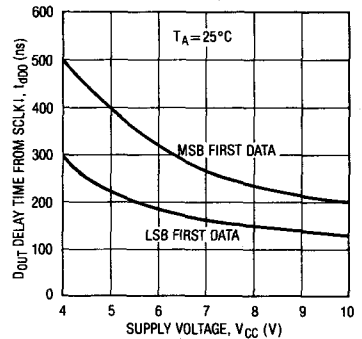
Digital Input Logic Threshold vs VCC Supply Voltage



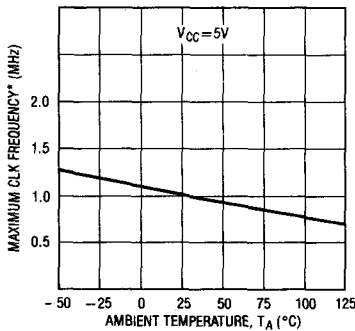
DOUT Delay Time vs Temperature



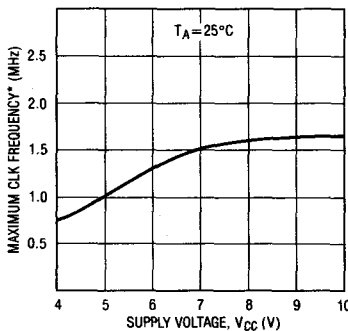
DOUT Delay Time vs VCC Supply Voltage



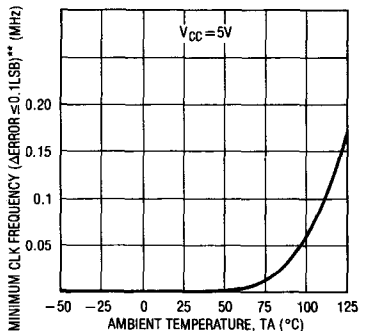
Maximum Clock Rate vs Temperature



Maximum Clock Rate vs VCC Supply Voltage



Minimum Clock Rate vs Temperature

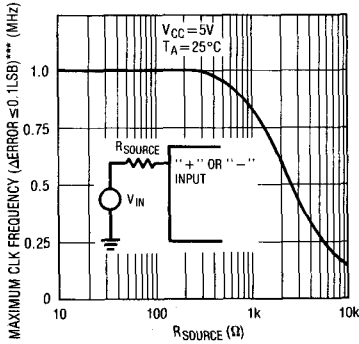


*MAXIMUM CLK FREQUENCY REPRESENTS THE HIGHEST FREQUENCY AT WHICH CLK CAN BE OPERATED (WITH 50% DUTY CYCLE) WHILE STILL PROVIDING 100ns SETUP TIME FOR THE DEVICE RECEIVING THE DOUT DATA.

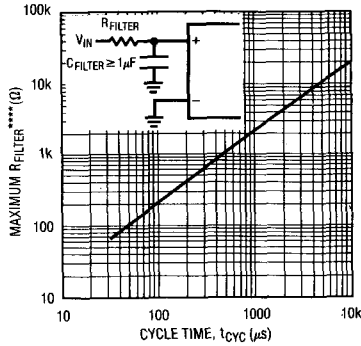
**AS THE CLK FREQUENCY IS DECREASED FROM 500kHz, MINIMUM CLK FREQUENCY (ΔERROR ≤ 0.1LSB) REPRESENTS THE FREQUENCY AT WHICH A 0.1LSB SHIFT IN ANY CODE TRANSITION FROM ITS 500kHz VALUE IS FIRST DETECTED.

TYPICAL PERFORMANCE CHARACTERISTICS

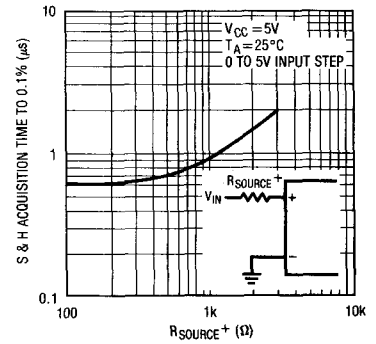
Maximum Clock Rate vs Source Resistance



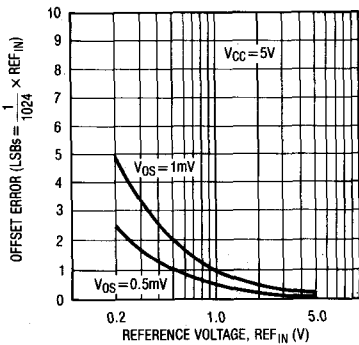
Maximum Filter Resistor vs Cycle Time



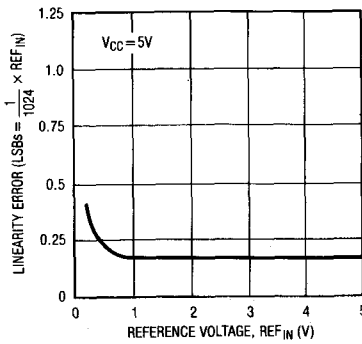
Sample and Hold Acquisition Time vs Source Resistance



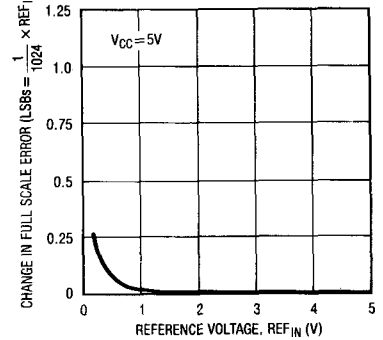
Unadjusted Offset Error vs Reference Voltage



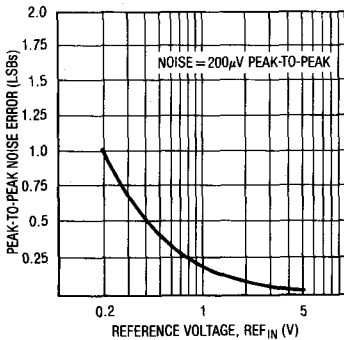
Linearity Error vs Reference Voltage



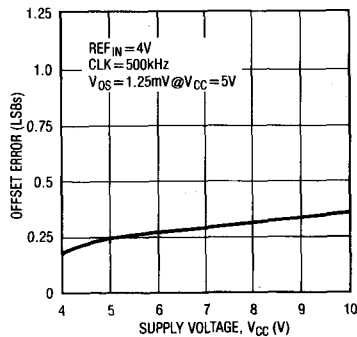
Change in Full Scale Error vs Reference Voltage



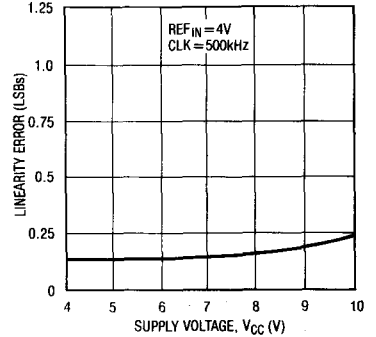
Noise Error vs Reference Voltage



Offset Error vs Supply Voltage



Linearity Error vs Supply Voltage

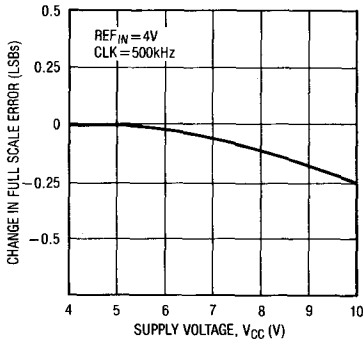


*** AS THE CLK FREQUENCY AND SOURCE RESISTANCE ARE INCREASED, MAXIMUM CLK FREQUENCY (Δ ERROR \leq 0.1LSB) REPRESENTS THE FREQUENCY AT WHICH A 0.1LSB SHIFT IN ANY CODE TRANSITION FROM ITS 500kHz, 0Q VALUE IS FIRST DETECTED.

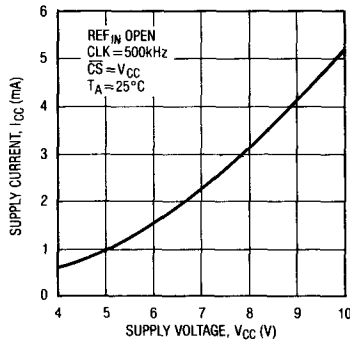
**** MAXIMUM R_{FILTER} REPRESENTS THE FILTER RESISTOR VALUE AT WHICH A 0.1LSB CHANGE IN FULL-SCALE ERROR FROM ITS VALUE AT $R_{FILTER}=0$ IS FIRST DETECTED.

TYPICAL PERFORMANCE CHARACTERISTICS

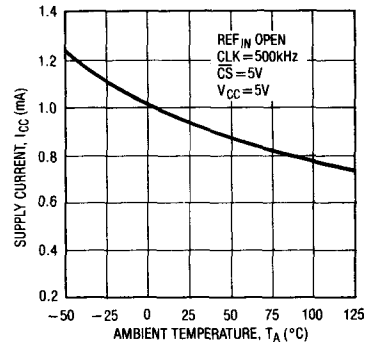
Change in Full Scale Error vs V_{CC} Supply Voltage



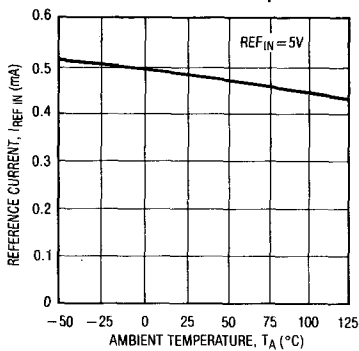
V_{CC} Supply Current vs Supply Voltage



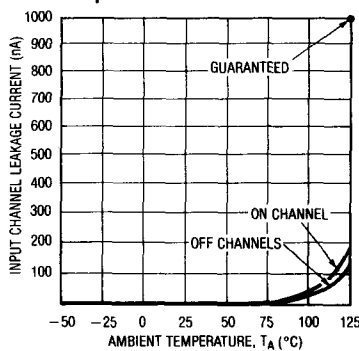
V_{CC} Supply Current vs Temperature



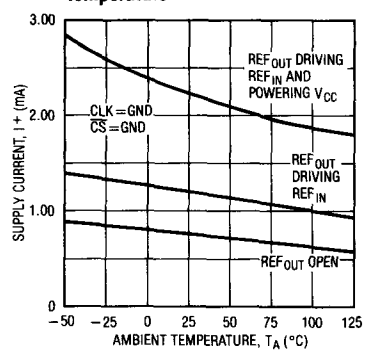
Reference Current vs Temperature



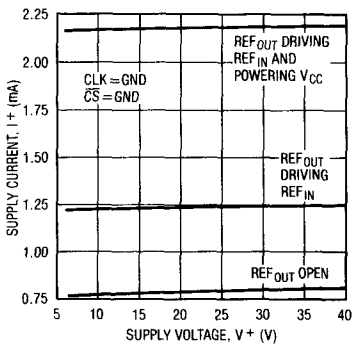
Input Channel Leakage Current vs Temperature



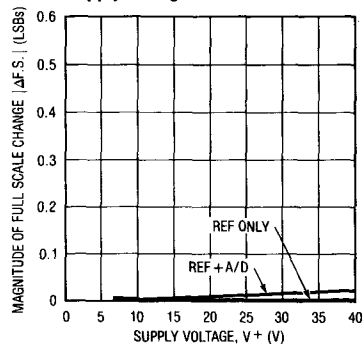
$V+$ Supply Current vs Temperature



$V+$ Supply Current vs Supply Voltage



Change in Full Scale Error vs $V+$ Supply Voltage



APPLICATIONS INFORMATION

The LTC1095 is a data acquisition component which contains the following functional blocks:

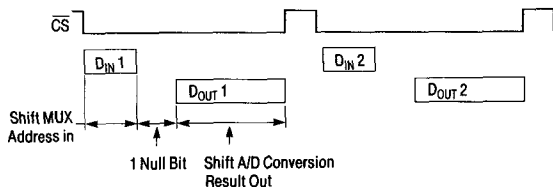
1. 10-bit successive approximation A/D converter
2. Analog multiplexer (MUX)
3. Sample and hold (S&H)
4. Synchronous, half duplex serial interface
5. Control and timing logic
6. On board reference

DIGITAL CONSIDERATIONS

1. Serial Interface

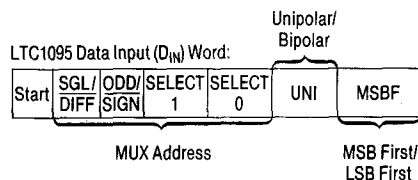
The LTC1095 communicates with microprocessors and other external circuitry via a synchronous, half duplex, four wire serial interface (see Operating Sequence). The clock (CLK) synchronizes the data transfer with each bit being transmitted on the falling CLK edge and captured on the rising CLK edge in both transmitting and receiving systems. The LTC1095 first receives input data and then transmits back the A/D conversion result (half duplex). Because of the half duplex operation, D_{IN} and D_{OUT} may be tied together allowing transmission over just 3 wires: \overline{CS} , CLK and DATA (D_{IN}/D_{OUT}).

Data transfer is initiated by a falling chip select (\overline{CS}) signal. After \overline{CS} falls the LTC1095 looks for a start bit. After the start bit is received, a 6-bit input word is shifted into the D_{IN} input which configures the LTC1095 and starts the conversion. After one null bit, the result of the conversion is output on the D_{OUT} line. At the end of the data exchange \overline{CS} should be brought high. This resets the LTC1095 in preparation for the next data exchange.



2. Input Data Word

The LTC1095 clocks data into the D_{IN} input on the rising edge of the clock. The input data word is defined as follows:



Start Bit

The first "logical one" clocked into the D_{IN} input after \overline{CS} goes low is the start bit. The start bit initiates the data transfer. The LTC1095 will ignore all leading zeros which precede this logical one. After the start bit is received, the remaining bits of the input word will be clocked in. Further inputs on the D_{IN} pin are then ignored until the next \overline{CS} cycle.

APPLICATIONS INFORMATION

Multiplexer (MUX) Address

The bits of the input word following the START bit assign the MUX configuration for the requested conversion. For a given channel selection, the converter will measure the voltage between the two channels indicated by the + and - signs in the selected row of the following tables. In single ended mode, all input channels are measured with respect to COM.

LTC1095 Channel Selection

MUX ADDRESS			DIFFERENTIAL CHANNEL SELECTION						
SGL/DIFF	ODD/SIGN	SELECT	1	0	1	2	3	4	5
0	0	0	0	0	+	-			
0	0	0	1			+	-		
0	0	1	0					+	-
0	0	1	1	NOT USED					
0	1	0	0	-	+				
0	1	0	1			-	+		
0	1	1	0					-	+
0	1	1	1	NOT USED					

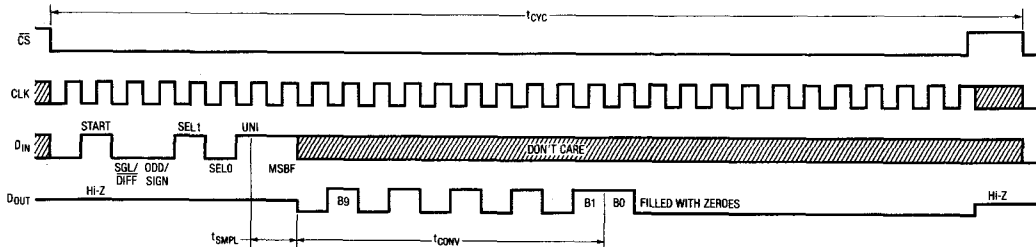
MUX ADDRESS			SINGLE ENDED CHANNEL SELECTION							
SGL/DIFF	ODD/SIGN	SELECT	1	0	1	2	3	4	5	COM
1	0	0	0	0	+					-
1	0	0	1			+				-
1	0	1	0					+		-
1	0	1	1	NOT USED						
1	1	0	0		+					-
1	1	0	1				+			-
1	1	1	0						+	-
1	1	1	1	NOT USED						

MSB First/LSB First (MSBF)

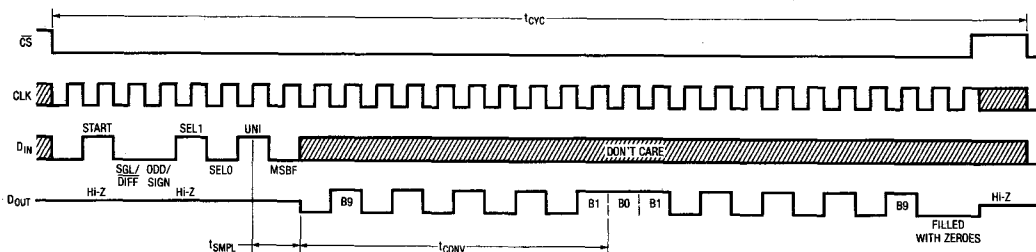
The output data of the LTC1095 is programmed for MSB first or LSB first sequence using the MSBF bit. When the MSBF bit is a logical one, data will appear on the D_{OUT} line in MSB first format. Logical zeros will be filled in indefinitely following the last data bit to accommodate longer word lengths required by some microprocessors. When the MSBF bit is a logical zero, LSB first data will follow the normal MSB first data on the D_{OUT} line. (See operating sequence).

LTC1095 Operating Sequence Example: Differential Inputs (CH4+, CH5-), Unipolar Mode

MSB First Data (MSBF = 1)



LSB First Data (MSBF = 0)



APPLICATIONS INFORMATION

Unipolar/Bipolar (UNI)

The UNI bit of the LTC1095 determines whether the conversion will be unipolar or bipolar. When UNI is a logical one, a unipolar conversion will be performed on the selected input voltage. When UNI is a logical zero, a bipolar conversion will result. The input span and code assignment for each conversion type are shown in the figures below.

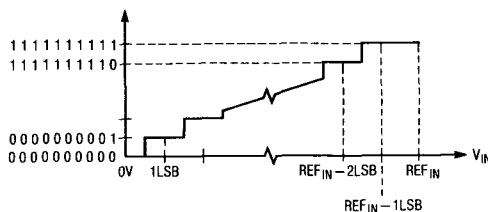
Unipolar Output Code (UNI = 1)

OUTPUT CODE	INPUT VOLTAGE	INPUT VOLTAGE (REF _{IN} = 5V)
1111111111	REF _{IN} - 1LSB	4.9951V
1111111110	REF _{IN} - 2LSB	4.9902V
⋮	⋮	⋮
⋮	⋮	⋮
0000000001	1LSB	0.0049V
0000000000	0V	0V

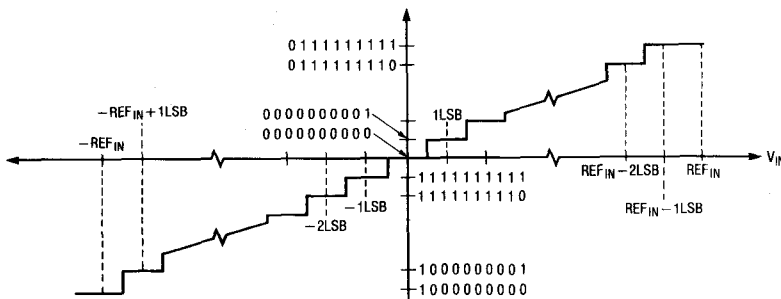
Bipolar Output Code (UNI = 0)

OUTPUT CODE	INPUT VOLTAGE	INPUT VOLTAGE (REF _{IN} = 5V)
0111111111	REF _{IN} - 1LSB	4.9902V
0111111110	REF _{IN} - 2LSB	4.9805V
⋮	⋮	⋮
⋮	⋮	⋮
0000000001	1LSB	0.0098V
0000000000	0V	0V
1111111111	-1LSB	-0.0098V
1111111110	-2LSB	-0.0195V
⋮	⋮	⋮
⋮	⋮	⋮
1000000001	-(REF _{IN}) + 1LSB	-4.9902V
1000000000	-(REF _{IN})	-5.000V

Unipolar Transfer Curve (UNI = 1)



Bipolar Transfer Curve (UNI = 0)



APPLICATIONS INFORMATION

3. Accommodating Microprocessors with Different Word Lengths

The LTC1095 will fill zeroes indefinitely after the transmitted data until \overline{CS} is brought high. At that time the D_{OUT} line is disabled. This makes interfacing easy to MPU serial ports with different transfer increments including 4 bits (e.g., COP400) and 8 bits (e.g., SPI and MICROWIRE/PLUS).

Figure 1 shows examples of LTC1095 input and output words for 4-bit and 8-bit processors. A complete data exchange can be implemented with two 4-bit MPU outputs and three inputs in 4-bit systems and one 8-bit output and two inputs in 8-bit systems. The resulting data winds up left justified in the MPU with zeroes automatically filled in the unused low order bits by the LTC1095. In section 5 another example is given using the MC68HC05C4 which positions data right justified inside the MPU.

4. Operation with D_{IN} and D_{OUT} Tied Together

The LTC1095 can be operated with D_{IN} and D_{OUT} tied together. This eliminates one of the lines required to communicate to the MPU. Data is transmitted in both directions on a single wire. The processor pin connected to this data line should be configurable as either an input or an output. The LTC1095 will take control of the data line and drive it low on the 7th falling CLK edge after the start bit is received (see Figure 2). Therefore the processor port line must be switched to an input before this happens, to avoid a conflict.

In the next section, an example is made of interfacing the LTC1095 with D_{IN} and D_{OUT} tied together to the Intel 8051 MPU.

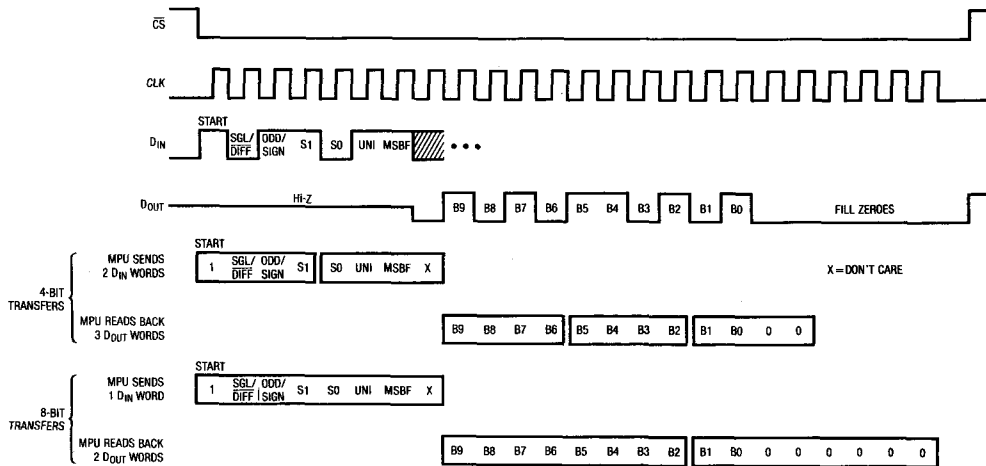


Figure 1. LTC1095 Input and Output Word Arrangements for 4-Bit and 8-Bit Serial Port Microprocessors

APPLICATIONS INFORMATION

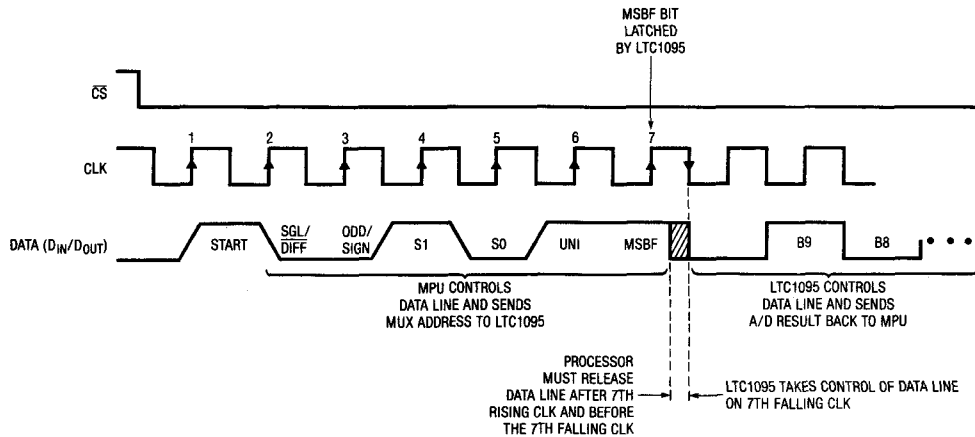


Figure 2. LTC1095 Operation with D_{IN} and D_{OUT} Tied Together

5. Microprocessor Interfaces

The LTC1095 can interface directly (without external hardware) to most popular microprocessor (MPU) synchronous serial formats (see Table 1). If an MPU without a dedicated serial port is used, then 3 or 4 of the MPU's parallel port lines can be programmed to form the serial link to the LTC1095. Included here are one serial interface example and one example showing a parallel port programmed to form the serial interface.

Motorola SPI (MC68HC05C4, MC68HC11)

The MC68HC05C4 has been chosen as an example of an MPU with a dedicated serial port. This MPU transfers data MSB first and in 8-bit increments. With three 8-bit transfers, the A/D result is read into the MPU. The first 8-bit transfer sends the start bit and the SGL/DIFF bit of the D_{IN} word to the LTC1095. The second 8-bit transfer clocks the remaining D_{IN} word bits, and B9 and B8 of the A/D conversion result. The third transfer clocks the remaining D_{OUT} bits into the μP .

ANDing the most significant byte with 03 Hex clears the 6 most significant bits. Notice how the position of the start bit in the first MPU transmit word is used to position the A/D result right justified in two memory locations.

Table 1. Microprocessors with Hardware Serial Interfaces Compatible with the LTC1095

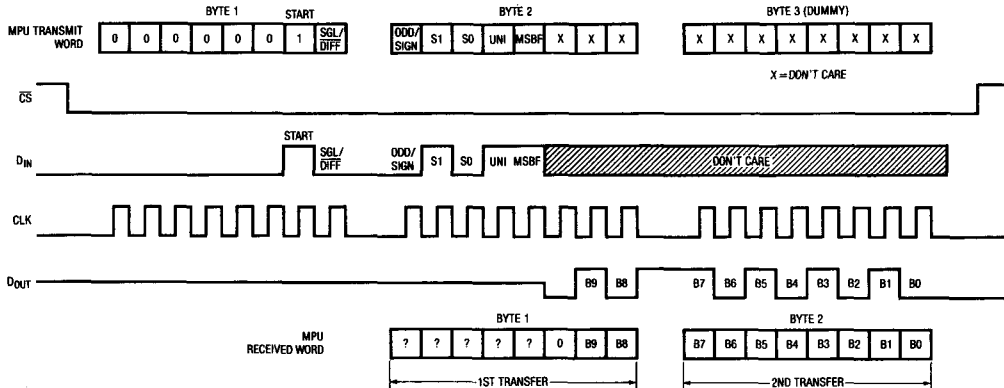
PART NUMBER	TYPE OF INTERFACE
Motorola	
MC6805S2, S3	SPI
MC68HC11	SPI
MC68HC05	SPI
RCA	
CDP68HC05	SPI
Hitachi	
HD6305	SCI Synchronous
HD63705	SCI Synchronous
HD6301	SCI Synchronous
HD63701	SCI Synchronous
HD6303	SCI Synchronous
HD64180	CSI/O
National Semiconductor	
COP400 Family	MICROWIRE†
COP800 Family	MICROWIRE/PLUS†
NS8050U	MICROWIRE/PLUS
HPC16000 Family	MICROWIRE/PLUS
Texas Instruments	
TMS7002	Serial Port
TMS7042	Serial Port
TMS70C02	Serial Port
TMS70C42	Serial Port
TMS32011*	Serial Port
TMS32020	Serial Port
TMS320C25*	Serial Port

*Requires external hardware

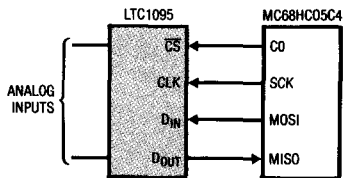
†MICROWIRE and MICROWIRE/PLUS are trademarks of National Semiconductor Corp.

APPLICATIONS INFORMATION

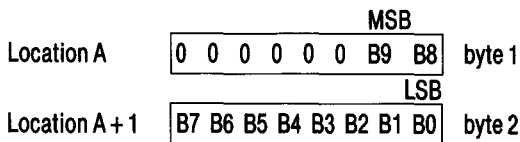
Data Exchange Between LTC1095 and MC68HC05C4



Hardware and Software Interface to Motorola MC68HC05C4 Microcontroller



D_{OUT} from LTC1095 stored in MC68HC05C4 RAM



LABEL	MNEMONIC	COMMENTS
START	BCLRn	Bit 0 Port C goes low (CS goes low)
	LDA	Load LTC1095 D _{IN} word into Acc.
	STA	Load LTC1095 D _{IN} word into SPI from Acc. Transfer begins.
	TST	Test status of SPIF
	BPL	Loop to previous instruction if not done with transfer
	LDA	Load next LTC1095 D _{IN} word into Acc.
	STA	Load LTC1095 D _{IN} word into SPI from Acc. Transfer begins.
	TST	Test status of SPIF
	BPL	Loop to previous instruction if not done with transfer
	LDA	Load contents of SPI data register into Acc. (D _{OUT} MSBs)
	STA	Start next SPI cycle
	AND	Clear 6 MSBs of first D _{OUT} word
	STA	Store in memory location A (MSBs)
	TST	Test status of SPIF
	BPL	Loop to previous instruction if not done with transfer
	BSETn	Set B0 of Port C (CS goes high)
	LDA	Load contents of SPI data register into Acc. (D _{OUT} LSBs)
	STA	Store in memory location A + 1 (LSBs)

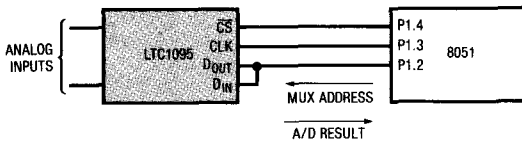
APPLICATIONS INFORMATION

Interfacing to the Parallel Port of the Intel 8051 Family

The Intel 8051 has been chosen to demonstrate the interface between the LTC1095 and parallel port microprocessors. Normally the CS, CLK and D_{IN} signals would be generated on 3 port lines and the D_{OUT} signal read on a 4th port line. This works very well. However, we will demonstrate here an interface with the D_{IN} and D_{OUT} of the LTC1095 tied together as described in section 4. This saves one wire.

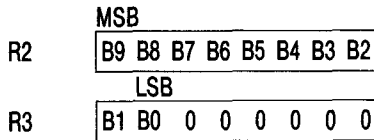
The 8051 first sends the start bit and MUX address to the LTC1095 over the data line connected to P1.2. Then P1.2 is reconfigured as an input (by writing to it a one) and the 8051 reads back the 10-bit A/D result over the same data line.

Hardware and Software Interface to 8051 Microcontroller

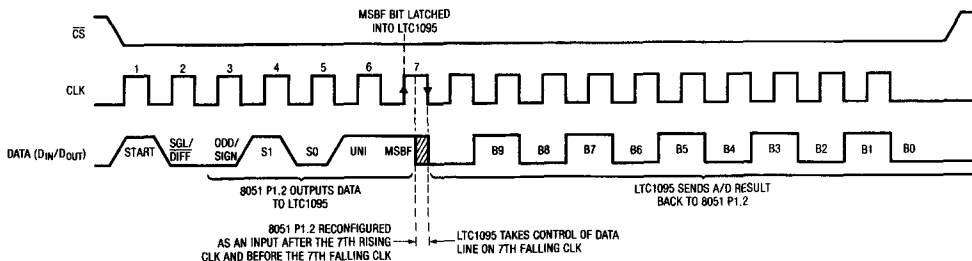


LABEL	MNEMONIC	OPERAND	COMMENTS
LOOP 1	MOV	A, #FFH	D _{IN} word for LTC1095
	SETB	P1.4	Make sure CS is high
	CLR	P1.4	CS goes low
	MOV	R4, #07	Load counter
	RLC	A	Rotate D _{IN} bit into Carry
	CLR	P1.3	CLK goes low
LOOP	MOV	P1.2, C	Output D _{IN} bit to LTC1095
	SETB	P1.3	CLK goes high
	DJNZ	R4, LOOP 1	Next bit
	MOV	P1, #04	Bit 2 becomes an input
	CLR	P1.3	CLK goes low
	MOV	R4, #09	Load counter
	MOV	C, P1.2	Read data bit into Carry
	RLC	A	Rotate data bit into Acc.
	SETB	P1.3	CLK goes high
	CLR	P1.3	CLK goes low
	DJNZ	R4, LOOP	Next bit
	MOV	R2, A	Store MSBs in R2
	MOV	C, P1.2	Read data bit into Carry
	SETB	P1.3	CLK goes high
	CLR	P1.3	CLK goes low
	CLR	A	Clear Acc.
	RLC	A	Rotate data bit from Carry to Acc.
	MOV	C, P1.2	Read data bit into Carry
RRC	A	Rotate right into Acc.	
RRC	A	Rotate right into Acc.	
MOV	R3, A	Store LSBs in R3	
SETB	P1.4	CS goes high	

D_{OUT} from LTC1095 stored in 8051 RAM



Data Exchange Between LTC1095 and 8051



APPLICATIONS INFORMATION

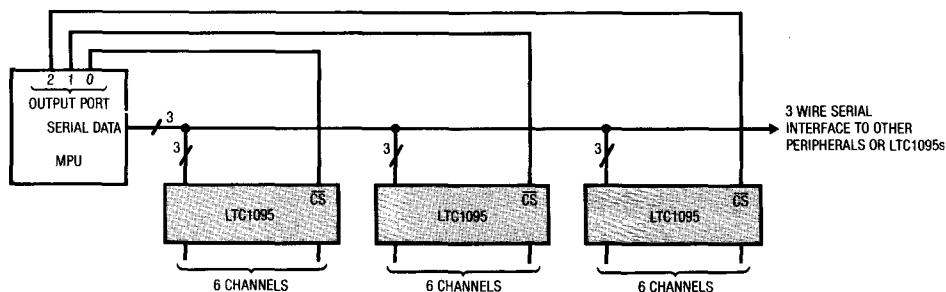


Figure 3. Several LTC1095s Sharing One 3 Wire Serial Interface

Sharing the Serial Interface

The LTC1095 can share the same 2 or 3 wire serial interface with other peripheral components or other LTC1095s (see Figure 3). In this case, the CS signals decide which LTC1095 is being addressed by the MPU.

ANALOG CONSIDERATIONS

1. Grounding

The LTC1095 should be used with an analog ground plane and single point grounding techniques.

The AGND pin should be tied directly to this ground plane.

The DGND pin of the LTC1095 can also be tied directly to this ground plane because minimal digital noise is generated within the chip itself.

The V_{CC} pin should be bypassed to the ground plane with a $4.7\mu\text{F}$ tantalum with leads as short as possible. The V^- pin should be bypassed with a $0.1\mu\text{F}$ ceramic disk. For single supply applications, V^- can be tied to the ground plane.

It is also recommended that the COM pin be tied directly to the ground plane. All analog inputs should be referenced directly to the single point ground. Digital inputs and outputs should be shielded from and/or routed away from the reference and analog circuitry.

Figure 4 shows an example of an ideal LTC1095 ground plane design for a two sided board. Of course this much ground plane will not always be possible, but users should strive to get as close to this ideal as possible.

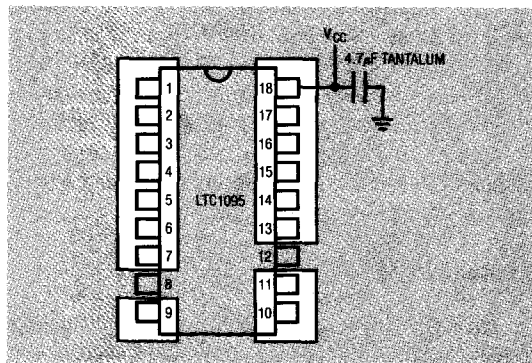


Figure 4. Example Ground Plane for the LTC1095

APPLICATIONS INFORMATION

2. Bypassing

For good performance, V_{CC} must be free of noise and ripple. Any changes in the V_{CC} voltage with respect to analog ground during a conversion cycle can induce errors or noise in the output code. V_{CC} noise and ripple can be kept below 1mV by bypassing the V_{CC} pin directly to the analog ground plane with a 4.7 μ F tantalum with leads as short as possible. Figures 5 and 6 show the effects of good and poor V_{CC} bypassing.

3. Analog Inputs

Because of the capacitive redistribution A/D conversion techniques used, the analog inputs of the LTC1095 have capacitive switching input current spikes. These current spikes settle quickly and do not cause a problem. However, if large source resistances are used or if slow settling op amps drive the inputs, care must be taken to insure that the transients caused by the current spikes settle completely before the conversion begins.

Source Resistance

The analog inputs of the LTC1095 look like a 60pF capacitor (C_{IN}) in series with a 500 Ω resistor (R_{ON}) as shown in Figure 7. C_{IN} gets switched between the selected "+" and "-" inputs once during each conversion cycle. Large external source resistances and capacitances will slow the settling of the inputs. It is important that the overall RC time constants be short enough to allow the analog inputs to completely settle within the allowed time.

"+" Input Settling

This input capacitor is switched onto the "+" input during the sample phase (t_{SMPL} , see Figure 8). The sample phase is the 1/2 CLK cycles before the conversion starts. The voltage on the "+" input must settle completely within this sample time. Minimizing R_{SOURCE}^+ and C1 will improve the input settling time. If large "+" input source re-

sistance must be used, the sample time can be increased by using a slower CLK frequency. With the minimum possible sample time of 3 μ s, $R_{SOURCE}^+ < 2k$ and $C1 < 20pF$ will provide adequate settling.

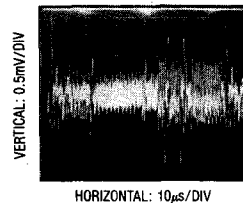


Figure 5. Poor V_{CC} Bypassing. Noise and Ripple Can Cause A/D Errors.

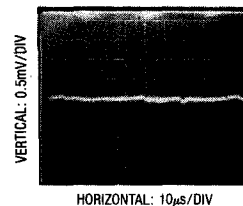


Figure 6. Good V_{CC} Bypassing Keeps Noise and Ripple On V_{CC} Below 1mV

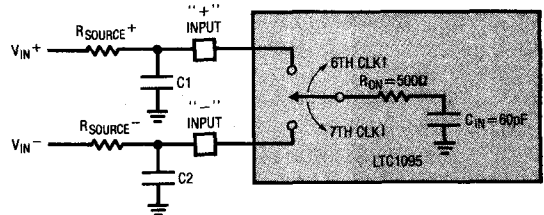


Figure 7. Analog Input Equivalent Circuit

APPLICATIONS INFORMATION

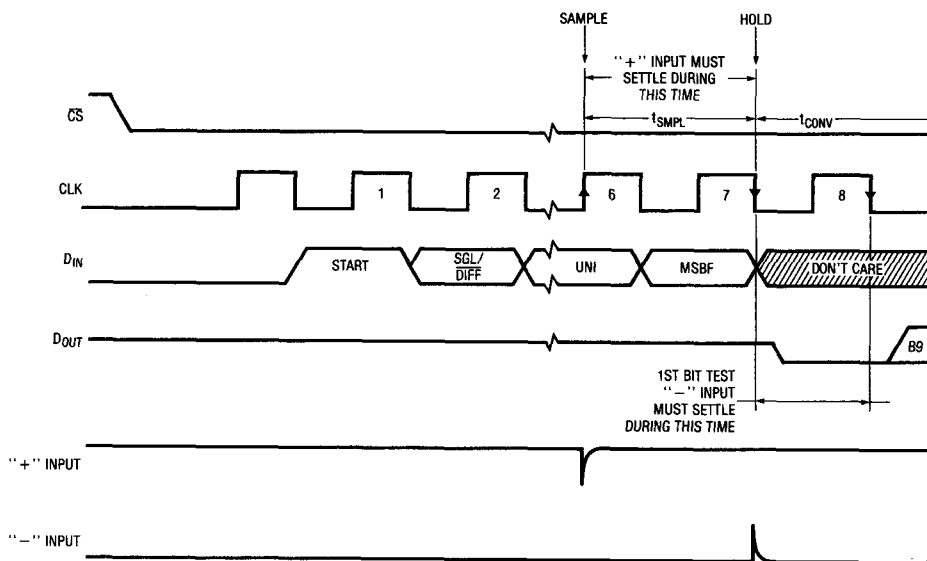


Figure 8. "+ " and "- " Input Settling Windows

"- " Input Settling

At the end of the sample phase the input capacitor switches to the "- " input and the conversion starts (see Figure 8). During the conversion, the "+ " input voltage is effectively "held" by the sample and hold and will not affect the conversion result. However, it is critical that the "- " input voltage settle completely during the first CLK cycle of the conversion time and be free of noise. Minimizing R_{SOURCE^-} and C_2 will improve settling time. If large "- " input source resistance must be used, the time allowed for settling can be extended by using a slower CLK frequency. At the maximum CLK rate of 500kHz, $R_{SOURCE^-} < 1k\Omega$ and $C_2 < 20pF$ will provide adequate settling.

Input Op Amps

When driving the analog inputs with an op amp it is important that the op amp settle within the allowed time (see Figure 8). Again, the "+ " and "- " input sampling times can be extended as described above to accommodate slower op amps. Most op amps including the LT1006 and LT1013 single supply op amps, can be made to settle well even with the minimum settling windows of $3\mu s$ ("+" input) and $2\mu s$ ("- " input) which occur at the maximum clock rate of 500kHz. Figures 9 and 10 show examples of adequate and poor op amp settling.

APPLICATIONS INFORMATION

RC Input Filtering

It is possible to filter the inputs with an RC network as shown in Figure 11. For large values of C_F (e.g., $1\mu\text{F}$), the capacitive input switching currents are averaged into a net DC current. Therefore, a filter should be chosen with a small resistor and large capacitor to prevent DC drops across the resistor. The magnitude of the DC current is approximately $I_{DC} = 60\text{pF} \times V_{IN}/t_{CYC}$ and is roughly proportional to V_{IN} . When running at the minimum cycle time of $38\mu\text{s}$, the input current equals $8\mu\text{A}$ at $V_{IN} = 5\text{V}$. In this case, a filter resistor of 50Ω will cause 0.1LSB of full-scale error. If a larger filter resistor must be used, errors can be eliminated by increasing the cycle time as shown in the typical curve of Maximum Filter Resistor vs Cycle Time.

Input Leakage Current

Input leakage currents can also create errors if the source resistance gets too large. For instance, the maximum input leakage specification of $1\mu\text{A}$ (at 125°C) flowing through a source resistance of $1\text{k}\Omega$ will cause a voltage drop of 1mV or 0.2LSB . This error will be much reduced at lower temperatures because leakage drops rapidly (see typical curve of Input Channel Leakage Current vs Temperature).

4. Sample and Hold

Single Ended Inputs

The LTC1095 provides a built-in sample and hold (S&H) function for signals acquired in the single ended mode. This sample and hold allows conversion of rapidly varying signals (see typical curve of S&H Acquisition Time vs Source Resistance). The input voltage is sampled during the t_{SMPL} time as shown in Figure 8. The sampling interval

begins as the bit preceding the MSBF bit is shifted in and continues until the falling CLK edge after the MSBF bit is received. On this falling edge, the S&H goes into hold mode and the conversion begins.

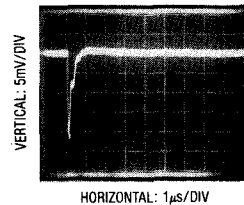


Figure 9. Adequate Settling of Op Amp Driving Analog Input

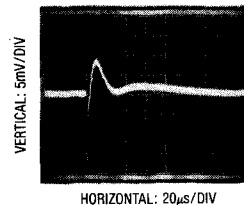


Figure 10. Poor Op Amp Settling Can Cause A/D Errors

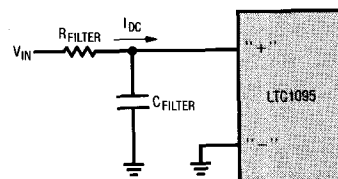


Figure 11. RC Input Filtering

APPLICATIONS INFORMATION

Differential Inputs

With differential inputs, the A/D no longer converts just a single voltage but rather the difference between two voltages. In this case, the voltage on the selected “+” input is still sampled and held and therefore may be rapidly time varying just as in single ended mode. However, the voltage on the selected “-” input must remain constant and be free of noise and ripple throughout the conversion time. Otherwise, the differencing operation may not be performed accurately. The conversion time is 10 CLK cycles. Therefore, a change in the “-” input voltage during this interval can cause conversion errors. For a sinusoidal voltage on the “-” input this error would be:

$$V_{\text{ERROR (MAX)}} = V_{\text{PEAK}} \times 2 \times \pi \times f(\text{“-”}) \times 10 / f_{\text{CLK}}$$

Where $f(\text{“-”})$ is the frequency of the “-” input voltage, V_{PEAK} is its peak amplitude and f_{CLK} is the frequency of the CLK. In most cases V_{ERROR} will not be significant. For a 60Hz signal on the “-” input to generate a 1/4LSB error (1.25mV) with the converter running at $\text{CLK} = 500\text{kHz}$, its peak value would have to be 150mV.

5. Internal Reference

The LTC1095 contains an internal precision 5V buried zener reference which is capable of supplying the full scale reference for the converter when connected as shown in Figure 15. With its 10mA output current the reference can also power the A/D and other external circuitry to provide a TTL input/TTL output system running off a single 7.2V-40V supply (see Figure 16).

6. Reference Input

The voltage on the reference input of the LTC1095 defines the voltage span of the A/D converter. The reference input looks primarily like a 10kΩ resistor to ground but will have transient capacitive switching currents due to the switched capacitor conversion technique (see Figure 12).

During each bit test of the conversion (every CLK cycle), a capacitive current spike will be generated on the reference pin by the A/D. These current spikes settle quickly and do not cause a problem. However, if slow settling circuitry is used to drive the reference input, care must be taken to ensure that transients caused by these current spikes settle completely during each bit test of the conversion.

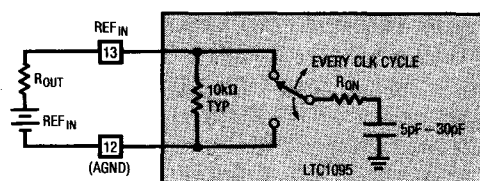


Figure 12. Reference Input Equivalent Circuit

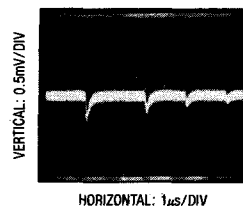


Figure 13. Adequate Reference Settling

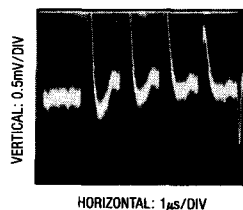


Figure 14. Poor Reference Settling Can Cause A/D Errors

APPLICATIONS INFORMATION

When driving the reference input, three things should be kept in mind:

1. The source resistance (R_{OUT}) driving the reference input should be low (less than 1Ω) to prevent DC drops caused by the 1mA maximum reference current ($I_{REF IN}$).
2. Transients on the reference input caused by the capacitive switching currents must settle completely during each bit test (each CLK cycle). Figures 13 and 14 show examples of both adequate and poor settling. Using a slower CLK will allow more time for the reference to settle. However, even at the maximum CLK rate of 500kHz most references and op amps can be made to settle within the $2\mu s$ bit time.
3. It is recommended that REF_{IN} be tied to REF_{OUT} as shown in Figure 15.

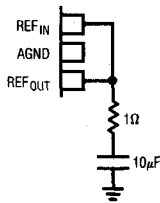


Figure 15. Suggested Circuit for REF_{IN} Tied to REF_{OUT}

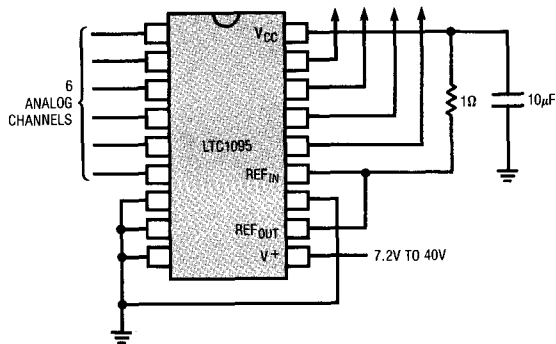


Figure 16. LTC1095 Single Supply Operation

7. Reduced Reference Operation

The LTC1095 can operate with reference voltages below 1V, by dividing down the 5V reference output voltage as shown in Figure 17.

The effective resolution of the LTC1095 will be increased by reducing the input span of the converter. The LTC1095 exhibits good linearity and gain over a wide range of reference voltages (see typical curves of Linearity and Full Scale Error vs Reference Voltage). However, care must be taken when operating at low values of $V_{REF IN}$ because of the reduced LSB step size and the resulting higher accuracy requirement placed on the converter. The following factors must be considered when operating at low $V_{REF IN}$ values.

1. Offset
2. Noise
3. Conversion speed (CLK frequency)

Offset with Reduced Reference Voltages

The offset of the LTC1095 has a larger effect on the output code when the A/D is operated with reduced reference voltage. The offset (which is typically a fixed voltage) becomes a larger fraction of an LSB as the size of the LSB is reduced. The typical curve of Unadjusted Offset Error vs Reference Voltage shows how offset in LSBs is related to reference voltage for a typical value of V_{OS} . For example, a

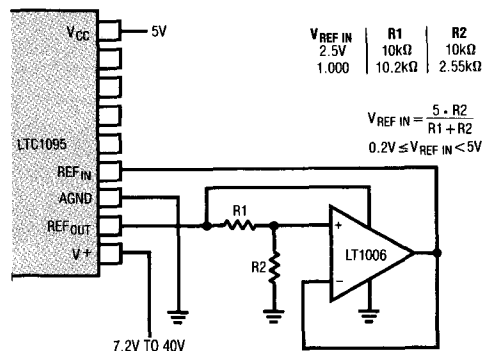


Figure 17. Operating LTC1095 on Reduced Reference Voltage

APPLICATIONS INFORMATION

V_{OS} of 0.5mV which is 0.1LSB with a 5V reference becomes 0.5LSB with a 1V reference and 2.5LSBs with a 0.2V reference. If this offset is unacceptable, it can be corrected digitally by the receiving system or by offsetting the “-” input to the LTC1095.

Noise with Reduced Reference Voltages

The total input referred noise of the LTC1095 can be reduced to approximately 200 μ V peak-to-peak using a ground plane, good bypassing, good layout techniques and minimizing noise on the reference input. This noise is insignificant with a 5V reference but will become a larger fraction of an LSB as the size of the LSB is reduced. The typical curve of Noise Error vs Reference Voltage shows the LSB contribution of this 200 μ V of noise.

For operation with a 5V reference, the 200 μ V noise is only 0.04LSB peak-to-peak. In this case, the LTC1095 noise will contribute virtually no uncertainty to the output code. However, for reduced references, the noise may cause undesirable jitter in the output code. For example, with a

1V reference, this same 200 μ V noise is 0.2LSB peak-to-peak. This will reduce the range of input voltages, over which a stable output code can be achieved, by 0.2LSB. If the reference is further reduced to 200mV, the 200 μ V noise becomes equal to one LSB and a stable code may be difficult to achieve. In this case, averaging readings may be necessary.

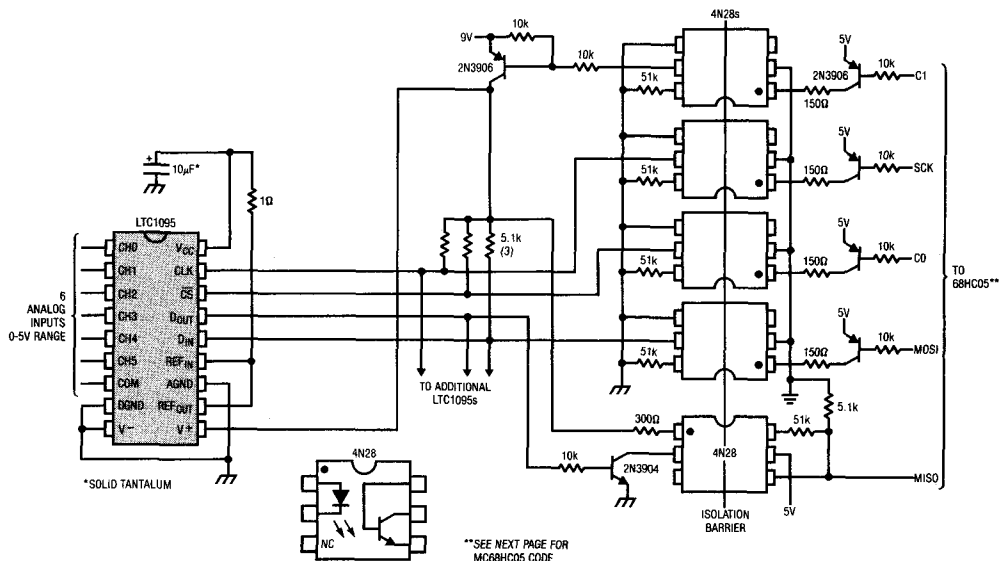
This noise data was taken in a very clean setup. Any setup induced noise (noise or ripple on: V_{CC} , REF_{IN} , V_{IN} or V^-) will add to the internal noise. The lower the reference voltage to be used, the more critical it becomes to have a clean, noise-free setup.

Conversion Speed with Reduced Reference Voltages

With reduced reference voltages, the LSB step size is reduced and the LTC1095 internal comparator overdrive is reduced. Therefore, it may be necessary to reduce the maximum CLK frequency when low reference voltages are used.

TYPICAL APPLICATIONS

Micropower, 500V Opto Isolated, Multichannel, 10-Bit Data Acquisition System



9

TYPICAL APPLICATIONS

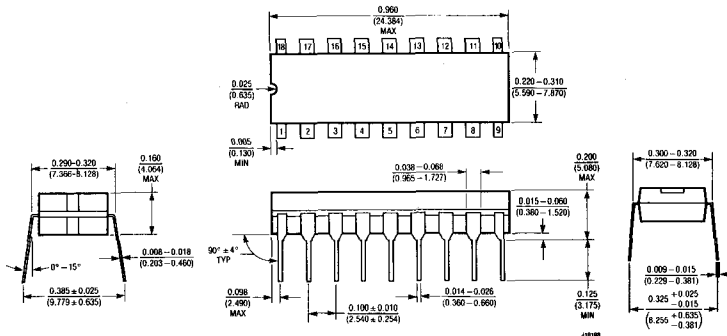
68HC05 Code Communicates with LTC1095 through Opto-Isolators

LABEL	MNEMONIC	OPERAND	COMMENTS
START	ORG	\$100	
	CLR X		Clear X register
	LDA		CH0
	STA	#\$1F	CH0 address
	LDA	\$50	CH1
	STA	#\$9F	CH1 address
	LDA	\$51	CH2
	STA	#\$3F	CH2 address
	LDA	\$52	CH3
	STA	#\$BF	CH3 address
	LDA	\$53	CH4
	STA	#\$5F	CH4 address
	LDA	\$54	CH5
	STA	#\$DF	CH5 address
	LDA	\$55	Data for SPCR
	STA	#\$53	Load data into SPCR
LDA	\$0A	Data for DDR	
STA	#\$FF	Configure PORT C DDR	
LDA	\$06	C1 (PWR OFF) goes low	
T1	BCLR	1,\$02	Load counter
	LDA	#\$FF	Decrement Acc.
T2	DECA	T1	Load counter
	BNE	T1	Decrement Acc.
T3	DECA	T2	Load counter
	BNE	T2	Decrement Acc.
	LDA	#\$FF	Load counter
	DECA	T3	Decrement Acc.
	BNE	T3	Decrement Acc.
	LDA	#\$FF	Load counter

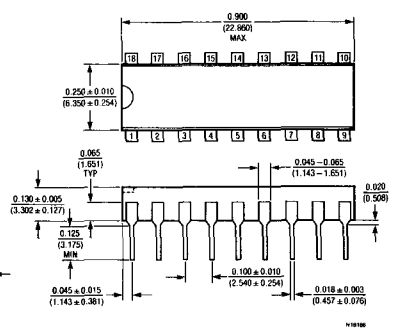
LABEL	MNEMONIC	OPERAND	COMMENTS
T4	DECA		Decrement Acc.
START1	BNE	T4	
	BCLR	0,\$02	C0 (CS) goes low
TEST2	LDA	#\$03	D _{IN} prefix start and SGL
	STA	\$0C	Start transfer
	TST	\$0B	Test if done
TEST	BPL	TEST2	If not try again
	LDA	\$50,X	Put D _{IN} word in Acc.
	STA	\$0C	Start transfer
	TST	\$0B	Test if done
SKIP	BPL	TEST	If not try again
	LDA	#0C	Load MSBs in Acc.
	STA	\$60,X	Store MSBs in \$60 + X
	LDA	#\$FF	Insure 1's output last
TEST1	STA	\$0C	Start next transfer
	TST	\$0B	Test if done
SKIP1	BPL	TEST1	If not try again
	BSET	0,\$02	C0 (CS) goes high
	LDA	\$0C	Put LSBs in Acc.
	STA	\$70,X	Put LSBs in \$70 + x
	INCX		Increment X register
	CPX	#\$06	Check if done
	BNE	START1	
	BSET	1,\$02	Set C1 (PWR OFF)
	CLR X		Reset counter
	JMP		Start next loop

PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

J Package
18-Lead Ceramic DIP



N Package
18-Lead Plastic DIP



High Speed 8-Bit A/D Converter with Built-In Sample-and-Hold

FEATURES

- Built-In Sample-and-Hold
- No Missing Codes
- No User Trims Required
- All Timing Inputs Edge Sensitive for Easy Processor Interface
- Fast Conversion Time: 2.5 μ s
- Latched Three-State Outputs
- Single 5V Operation
- No External Clock
- Overflow Output Allows Cascading
- T_C Input Allows User Adjustable Conversion Time
- 0.3" Wide 20-Pin DIP

KEY SPECIFICATIONS

- | | |
|----------------------------------|---|
| ■ Resolution | 8 Bits |
| ■ Conversion Time | 2.5 μ s (RD Mode)
2.5 μ s (WR-RD Mode) |
| ■ Slew Rate Limit (Internal S/H) | 2.5V/ μ s |
| ■ Low Power | 75mW Max |
| ■ Total Unadjusted Error | ± 1 LSB
$\pm 1/2$ LSB |
| LTC1099 | |
| LTC1099A | |

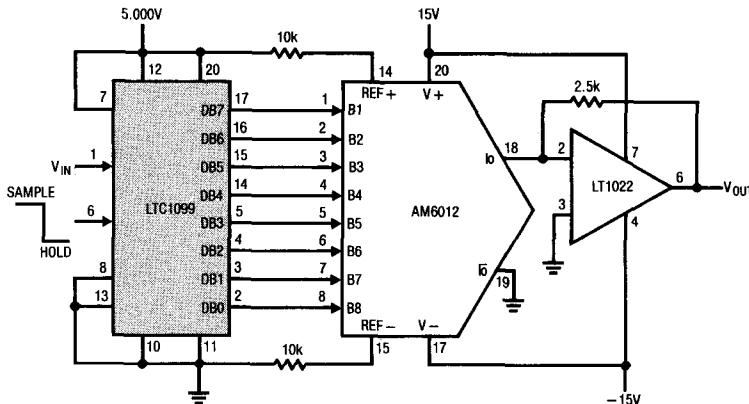
DESCRIPTION

The LTC1099 is a high speed microprocessor compatible 8-bit analog-to-digital converter (A/D). An internal sample-and-hold (S/H) allows the A/D to convert inputs up to the full Nyquist limit. With a conversion rate of 2.5 μ s this allows 156kHz 5Vp-p input signals, or slew rates as high as 2.5V/ μ s, to be digitized without the need for an external S/H.

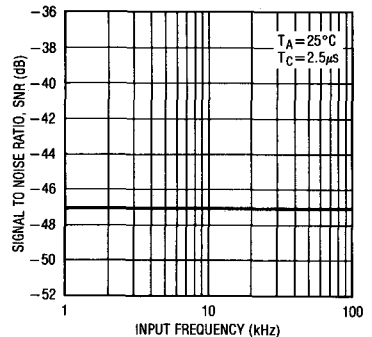
Two modes of operation, READ (RD) mode and WRITE-READ (WR-RD) mode, allow easy interface with processors. All timing is internal and edge sensitive which eliminates the need for external pulse shaping circuits. The Stand-Alone (SA) mode is convenient for those applications not involving a processor.

Data outputs are latched with three-state control to allow easy interface to a processor data bus or I/O port. An overflow output (OFL) is provided to allow cascading for higher resolution.

Infinite Hold Time Sample-and-Hold (T_{ACQ} = 240ns)



Signal to Noise Ratio (SNR) vs Input Frequency



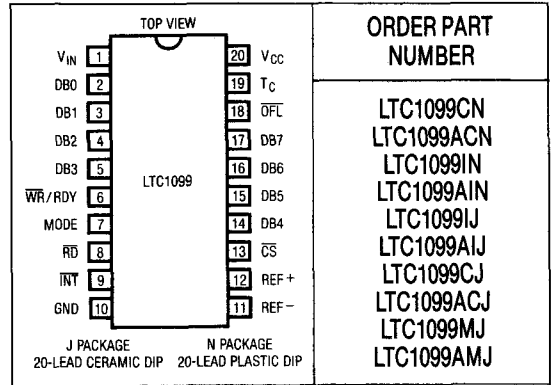
LTC1099

ABSOLUTE MAXIMUM RATINGS

(Notes 1 and 2)

Supply Voltage (V_{CC}) to GND	12V
Voltage	
Analog and Reference Inputs	-0.3V to $V_{CC} + 0.3V$
Digital Inputs	-0.3V to 12V
Digital Outputs	-0.3V to $V_{CC} + 0.3V$
Power Dissipation	500mW
Operating Temperature Range	
LTC1099C/1099AC	0°C to 70°C
LTC1099I/1099AI	-40°C to 85°C
LTC1099M/1099AM	-55°C to 125°C
Storage Temperature Range	-65°C to 150°C
Lead Temperature (Soldering, 10 sec.)	300°C

PACKAGE/ORDER INFORMATION



CONVERTER CHARACTERISTICS (Note 3)

PARAMETER	CONDITIONS	LTC1099AI/1099I LTC1099AM/1099M			LTC1099AC/1099C			UNITS	
		MIN	TYP	MAX	MIN	TYP	MAX		
Accuracy									
Total Unadjusted Error	Note 4	•							
LTC1099A		•		± 1/2			± 1/2	LSB	
LTC1099		•		± 1			± 1	LSB	
Minimum Resolution (No Missing Codes)		•	8		8			Bits	
Reference Input									
Input Resistance		•	1	3.2	6	2	3.2	4.5	kΩ
REF+ Input Voltage Range	Note 5	•	REF-		V_{CC}	REF-		V_{CC}	V
REF- Input Voltage Range	Note 5	•	GND		REF+	GND		REF+	V
Analog Input									
Input Voltage Range		•	GND		V_{CC}	GND		V_{CC}	V
Input Leakage Current	$\overline{CS} = V_{CC}, V_{IN} = V_{CC}, GND$	•			± 3			± 3	μA
Input Capacitance				60		60			pF
Sample-and-Hold									
Acquisition Time				240		240			ns
Aperature Time				110		110			ns
Tracking Rate				2.5		2.5			V/μs

DIGITAL AND DC ELECTRICAL CHARACTERISTICS (Note 3)

SYMBOL	PARAMETER	CONDITIONS	LTC1099AI/1099I LTC1099AM/1099M			LTC1099AC/1099C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V _{IH}	High Level Input Voltage	All Digital Inputs, V _{CC} = 5.25V	●	2.0			2.0		V
V _{IL}	Low Level Input Voltage	All Digital Inputs, V _{CC} = 4.75V	●		0.8		0.0001	0.8	V
I _{IH}	High Level Input Current	V _{IH} = 5V; CS, RD, Mode V _{IH} = 5V; WR	●	0.0001	1			1	μA
			●	0.0005	3		0.0005	3	μA
I _{IL}	Low Level Input Current	V _{IL} = 0V; All Digital Inputs	●	-0.0001	-1		-0.0001	-1	μA
V _{OH}	High Level Output Voltage	DB0-DB7, OFL, INT, RDY; V _{CC} = 4.75V I _{OUT} = 360μA I _{OUT} = 10μA	●	2.4	4.0 4.7		2.4	4.0 4.7	V V
V _{OL}	Low Level Output Voltage	DB0-DB7, OFL, INT, RDY; V _{CC} = 4.75V I _{OUT} = 1.8mA	●		0.4			0.4	V
I _{OZ}	High-Z Output Leakage	DB0-DB7, RDY; V _{OUT} = 5V DB0-DB7, RDY; V _{OUT} = 0V	●	0.1	3		0.1	3	μA
			●	-0.1	-3		-0.1	-3	μA
I _{SOURCE}	Output Source Current	DB0-DB7, OFL, INT, RDY; V _{OUT} = 0V	●	-11	-6		-11	-7	mA
I _{SINK}	Output Sink Current	DB0-DB7, OFL, INT, RDY; V _{OUT} = 5V	●	14	7		14	9	mA
I _{CC}	Supply Current	CS = WR = RD = V _{CC}	●	11	20		11	15	mA

AC CHARACTERISTICS (Note 3)

SYMBOL	PARAMETER	CONDITIONS	LTC1099AI/1099I LTC1099AM/1099M			LTC1099AC/1099C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
RD Mode (Figure 2) Pin 7 = GND									
t _{CRD}	Conversion Time	T _A = 25°C	●	2.3	2.5 2.8 5.0		2.3	2.5 2.8 3.75	μs μs
t _{RDY}	Delay From CS _I to RDY _I	C _L = 100pF			70			70	ns
t _{ACCO}	Delay From RD _I to Output Data Valid	C _L = 100pF			t _{CRD} + 35			t _{CRD} + 35	ns
t _{INTH}	Delay From RD _I to INT _I	C _L = 100pF			70			70	ns
t _{IH} , t _{I0H}	Delay From RD _I to High-Z State on Outputs	Test Circuit Figure 1			70			70	ns
t _P	Delay Time Between Conversions				700			700	ns
t _{ACC2}	Delay Time From RD _I to Output Data Valid				70			70	ns
WR-RD Mode (Figures 3 and 4) Pin 7 = V_{CC}									
t _{CWR}	Conversion Time	T _A = 25°C	●	2.3	2.5 2.8 5.0		2.3	2.5 2.8 3.75	μs μs
t _{ACCO}	Delay Time From WR _I to Output Data Valid	C _L = 100pF			t _{CWR} + 40			t _{CWR} + 40	ns
t _{ACC2}	Delay From RD _I to Output Data Valid	C _L = 100pF			70			70	ns
t _{INTH}	Delay From RD _I to INT _I	C _L = 100pF			70			70	ns
t _{IHWR}	Delay From WR _I to INT _I	C _L = 100pF			240			240	ns
t _{IH} , t _{I0H}	Delay From RD _I to High-Z State on Outputs	Test Circuit Figure 1			70			70	ns
t _P	Delay Time Between Conversions				700			700	ns
t _{WR}	Minimum WR Pulse Width				55			55	ns

Note 1: Absolute maximum ratings are those values beyond which the life of the device may be impaired.

Note 2: All voltages are with respect to GND (Pin 10) unless otherwise noted.

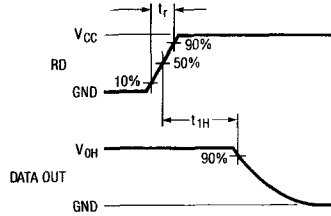
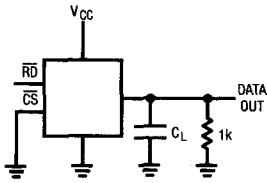
Note 3: V_{CC} = 5V, REF₊ = +5V, REF₋ = 0V and T_A = T_{MIN} to T_{MAX} unless otherwise noted. All typical values at T_A = 25°C. The ● indicates specifications which apply over the full operating temperature range.

Note 4: Total unadjusted error includes offset, gain, linearity and hold step errors.

Note 5: Reference input voltage range is guaranteed but is not tested.

TEST CIRCUITS

t_{rH}
 $t_r = 20ns, C_L = 10pF$



t_{OH}
 $t_r = 20ns, C_L = 10pF$

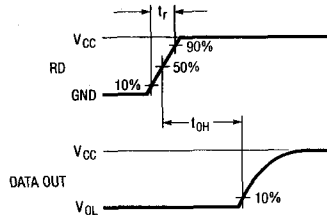
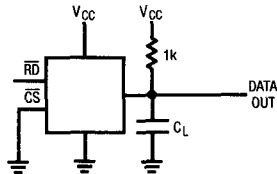


Figure 1. Three-State Test Circuit

TIMING DIAGRAMS

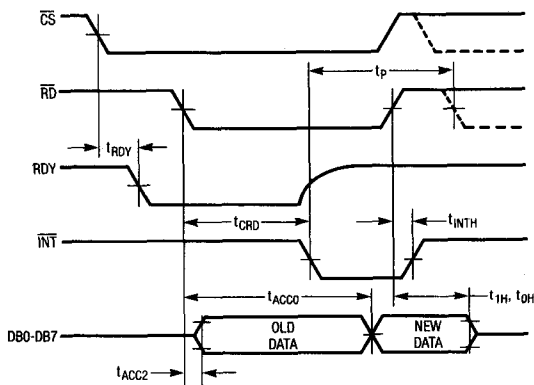


Figure 2. RD Mode (Pin 7 is GND)

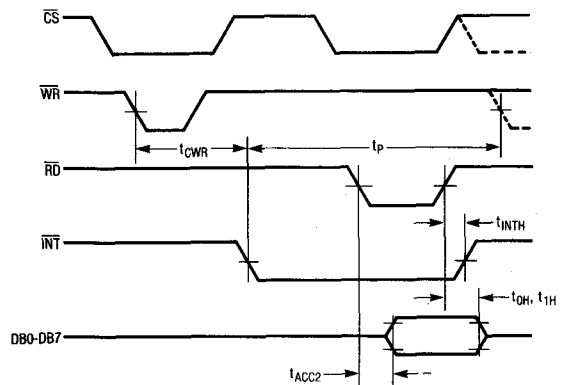


Figure 3A. WR-RD Mode (Pin 7 is HIGH and $t_{RD} > t_{CWR}$)

TIMING DIAGRAMS

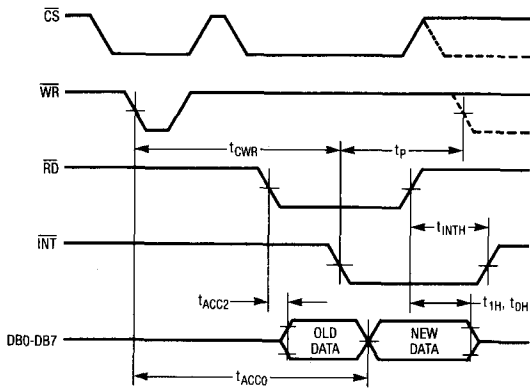


Figure 3B. WR-RD Mode (Pin 7 is HIGH and $t_{RD} < t_{CWR}$)

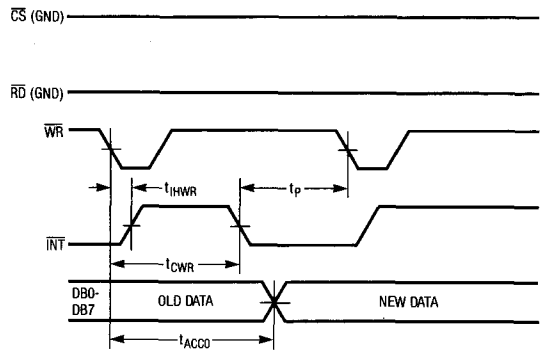


Figure 4. WR-RD Mode (Pin 7 is HIGH) Stand-Alone Operation

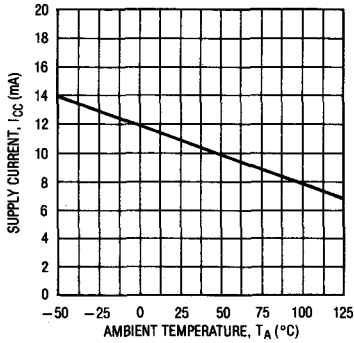
PIN FUNCTIONS

PIN #	NAME	DESCRIPTION	PIN #	NAME	DESCRIPTION
1	V_{IN}	Analog input.	9	\overline{INT}	Output that goes low when the conversion in process is complete and goes high after data is read.
2-5	DB0-DB3	Data outputs; DB0 = LSB.	10	GND	Ground connection.
6	\overline{WR}/RDY	\overline{WR}/RDY is an input when Mode = V_{CC} . Falling edge of \overline{WR} switches internal S/H to hold then starts conversion. \overline{WR}/RDY is an open drain output (active pull down) when Mode = GND. RDY goes low at start of conversion and pull down is turned off when conversion is complete. Resistive pull up is usually used in this mode.	11	REF -	Low reference potential (analog ground).
7	MODE	WR-RD when Mode = V_{CC} . RD when Mode = GND. No internal pull down.	12	REF +	High reference potential; $V_{REF} = \text{Full Scale} = (REF+) - (REF-)$.
8	\overline{RD}	A low on \overline{RD} with \overline{CS} low activates three-state outputs. With Mode = GND and \overline{CS} low, the falling edge of \overline{RD} switches internal S/H to hold and starts conversion.	13	\overline{CS}	Chip select — When high, data outputs are high impedance and all inputs are ignored.
			14-17	DB4-DB7	Data outputs; DB7 = MSB.
			18	\overline{OFL}	Overflow output — Goes low when $V_{IN} > V_{REF}$.
			19	T_C	User adjustable conversion time.
			20	V_{CC}	Positive supply; $4.75V \leq V_{CC} \leq 5.25V$.

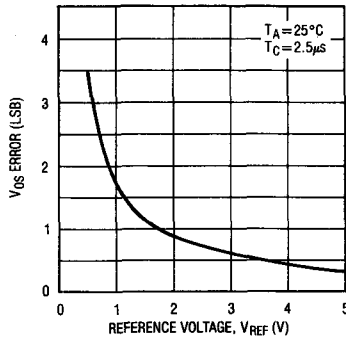
9

TYPICAL PERFORMANCE CHARACTERISTICS

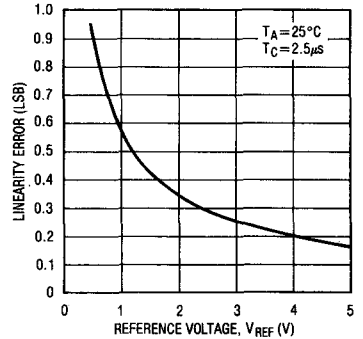
Supply Current vs Temperature



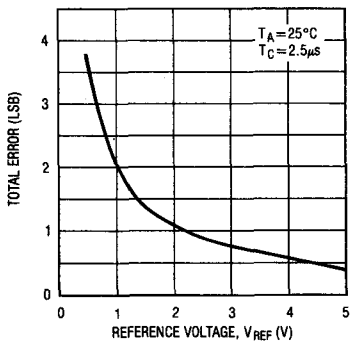
V_{OS} Error vs Reference Voltage



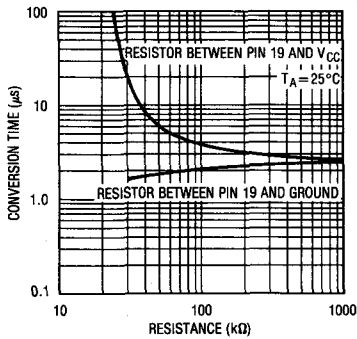
Linearity Error vs Reference Voltage



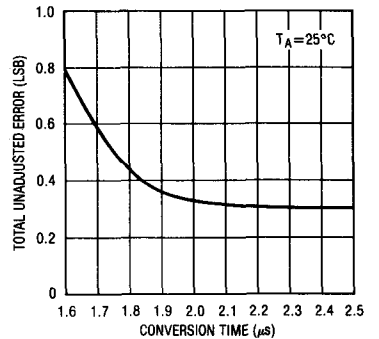
Total Error vs Reference Voltage



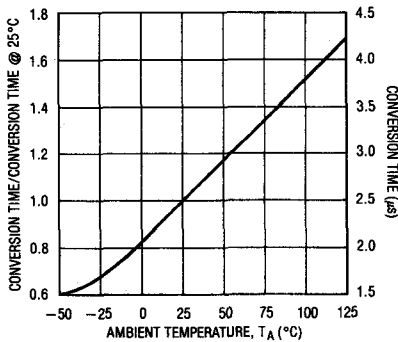
Conversion Time vs R_{EXT}



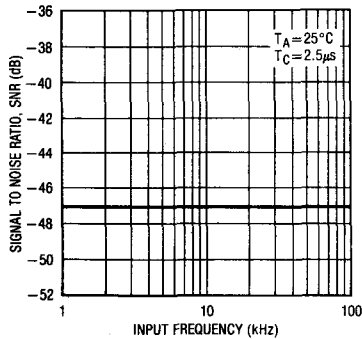
Accuracy vs Conversion Time



Conversion Time vs Temperature



Signal to Noise Ratio (SNR) vs Input Frequency



FUNCTIONAL DESCRIPTION

Figure 5 shows the functional block diagram for the LTC1099 two step flash ADC. It consists of two 4-bit flash converters, a 4-bit DAC and a differencing circuit. The conversion process proceeds as follows:

- 1) At the start of the conversion the on-board sample-and-hold switches from the sample to the hold mode. This is a true sample-and-hold with an acquisition time of 240ns, an aperture time of 110ns and a tracking rate of $2.5V/\mu s$.
- 2) The held input voltage is converted by the 4-bit MS-Flash ADC. This generates the upper or most significant 4-bits of the 8-bit output.
- 3) A 4-bit approximation, from the DAC output, is subtracted from the held input voltage.
- 4) The LS-Flash ADC converts the difference between the held input voltage and the DAC approximation. This generates the lower or least significant 4-bits of the 8-bit output. The LS-Flash reference is one sixteenth of the MS-Flash reference. This effectively multiplies the difference by 16.
- 5) Upon the completion of the LS 4-bit flash the eight output latches are updated simultaneously. At the same time the sample-and-hold is switched from the hold mode to the acquire mode in preparation for the next conversion.

The advantage of this approach is the reduction in the amount of hardware required. A full flash converter requires 255 comparators while this approach requires only 31. The price paid for this reduction in hardware is an increase in conversion time. A full flash converter requires only one comparison cycle while this approach requires two comparison cycles, hence two step flash.

This architecture is further simplified in the LTC1099 by reusing the MS-Flash hardware to do the LS-Flash. This reduces the number of comparators from 31 to 16. This is possible because the MS and LS conversions are done at different times.

To take the simple block diagram of Figure 5 and reconfigure it to reuse the MS-Flash to do the LS-Flash is conceptually simple, but from a hardware point of view is not practical. A new six input switched capacitor comparator is used to accomplish this function in a simple, although not straightforward, manner.

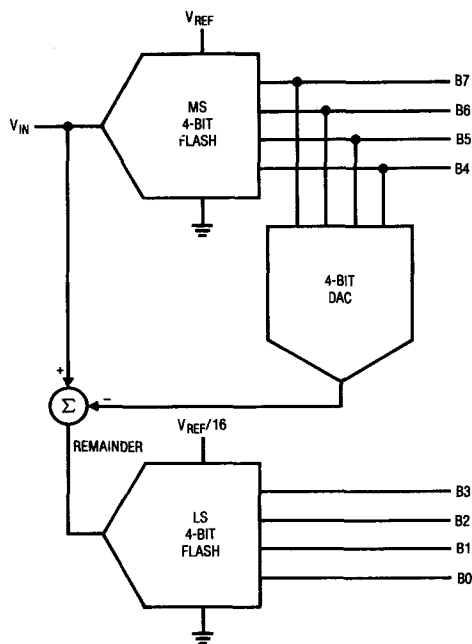


Figure 5. 8-Bit Two-Step Semiflash A/D

Figure 6 shows the six input switched capacitor comparator. Intuitively the comparator is easy to understand by noting that the common connection between the two input capacitors, C1 and C2, acts like a virtual ground. In operational amplifier circuits, current is summed at the virtual ground node. Input voltage is converted to current by the input resistors. In the switched capacitor comparator, input voltage is converted to charge by the input capacitors and these charges are summed at the virtual ground node.

FUNCTIONAL DESCRIPTION

A major advantage of this technique is that the switch-on impedance has no effect on accuracy as long as sufficient time exists to fully charge and discharge the capacitors.

During the first time period the T_+ and T_z switches are closed. This forces the common node between C_1 and C_2 to an arbitrary bias voltage. Since the capacitors subtract out this voltage it may be considered, for the sake of this discussion, to be exactly zero (i.e. virtual ground). Note also that variations in the bias voltage with time and temperature will also be rejected. In this state C_1 charges to V_{IN} . When T_z opens V_{IN} is held on C_1 .

The next step is the first comparison — the MS-Flash. T_z and T_+ are opened and T_{-1} is closed. The equation for each comparator is:

$$V_{IN} + 1/2LSB - MS_{TAP} = 0V$$

There are 16 identical comparators each tied to the tap on a 16 resistor ladder. The MS tap voltages vary from V_{REF} to $0V$ in 16 equal steps of $V_{REF}/16$.

Notice that capacitor C_2 adds $1/2LSB$ to V_{IN} . This offsets the converter transfer function by $1/2LSB$, equally distributing the $1LSB$ quantization error to $\pm 1/2LSB$.

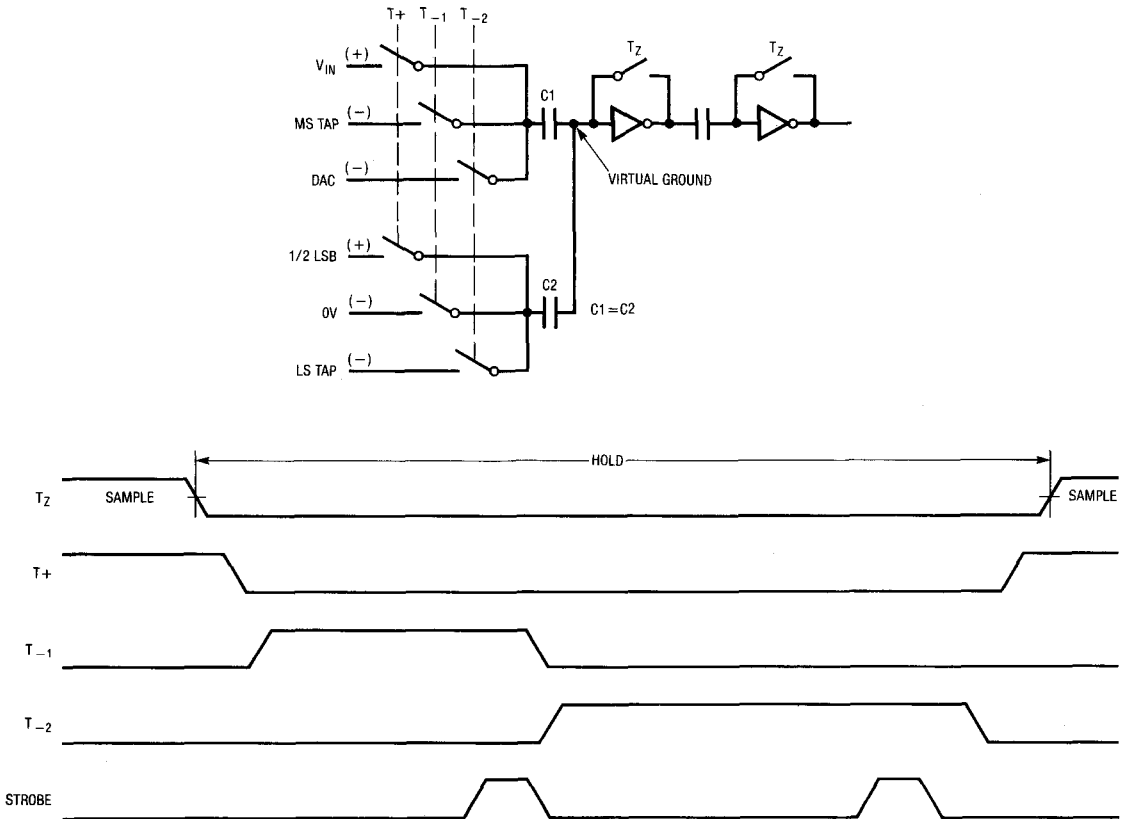


Figure 6. Six Input Switched Capacitor Comparator

FUNCTIONAL DESCRIPTION

The outputs of the 16 comparators are temporarily latched and drive the 4-bit DAC directly without need of decoding. This holds the DAC output constant for the next step — the LS conversion. The LS conversion is started when T_{-1} is opened and T_{-2} is closed. Capacitor C1 subtracts the 4-bit DAC approximation from V_{IN} and inputs the difference charge to the virtual ground node. The equation for each comparator is:

$$V_{IN} + 1/2LSB - V_{DAC} - LS_{TAP} = 0V$$

The 4-bit DAC approximation is input to all 16 comparators. The LS tap voltages are converted to charge by capacitor C2. LS taps vary from $V_{REF}/16V$ to $0V$ in 16 equal steps of $V_{REF}/256$. The comparators look at the net charge on the virtual ground node to perform the LS-Flash conversion. When this conversion is complete the 4 LSB's along with the 4 MSB's are transferred to the output latches. In this way all eight outputs will change simultaneously.

DIGITAL INTERFACE

The digital interface to the LTC1099 entails either controlling the conversion timing or reading data. There are two basic modes for controlling and reading the A/D — the WRITE-READ (WR-RD) mode and the READ (RD) mode.

WR-RD Mode (Pin 7 = High)

In the WR-RD mode a conversion sequence starts on the falling edge of \overline{WR} with \overline{CS} low (Figures 3A and 3B). This is an edge sensitive control function. The width of the \overline{WR} input is not important. All timing functions are internal to the A/D.

The first thing to happen after the falling edge of \overline{WR} is the internal S/H is switched to hold. This typically takes 110ns after \overline{WR} falls and is the aperture time of the S/H.

Next the A/D conversion takes place. The conversion time is internally set at $2.5\mu s$, but is user adjustable (see Adjusting the Conversion Time). The end of conversion is signaled by the high to low transition of \overline{INT} . The S/H is switched back to the acquire state as soon as the conversion is complete.

After the conversion is complete the 8-bit result is available on the three-state outputs. The outputs are active with \overline{RD} and \overline{CS} low. Output data is latched and, if no new conversion is initiated, is available indefinitely as long as the power is not turned off.

The WR-RD mode is also used for stand-alone operation. By tying \overline{CS} and \overline{RD} low the data outputs will be continuously active (Figure 4). The falling edge of \overline{WR} starts the conversion sequence and when done new data will appear on the outputs. All outputs will be updated simultaneously. In stand-alone operation the outputs will never be in a high impedance state.

RD Mode (Pin 7 = Low)

In the RD mode a conversion sequence is initiated by the falling edge of \overline{RD} when \overline{CS} is low (Figure 2). The S/H is switched to the hold state 110ns after the falling edge of \overline{RD} . It is switched back to the acquire state at the end of conversion.

When \overline{RD} goes low, with \overline{CS} low, the result of the previous conversion is output. This data stays there until the ongoing conversion is complete (\overline{INT} goes low). At this time the outputs are updated with new data.

As long as \overline{CS} and \overline{RD} stay low long enough, the receiving device will get the right data. Remember the receiving device reads data in on the rising edge of \overline{RD} . The RDY output facilitates making \overline{RD} long enough.

In the RD mode the \overline{WR} input becomes the RDY output. On the falling edge of \overline{RD} the RDY goes low. It is an open drain output to allow a wired OR function so it requires a pull-up resistor. At the end of conversion the active pull-down is released and RDY goes high.

DIGITAL INTERFACE

The RDY output is designed to interface to the Ready In (RDYIN) function on many popular processors. RDYIN allows these processors to work with slow memory by stretching the \overline{RD} strobe coming from the processor. \overline{RD} will remain low as long as RDY is low. In the case of the LTC1099, RDY stays low until the conversion is complete and new data is available on the outputs. This greatly simplifies the programmer's task. Each time data is required from the A/D a simple read is executed. The hardware interface makes sure the \overline{RD} strobe is long enough.

Adjusting the Conversion Time

The conversion time of the LTC1099 is internally set at $2.5\mu\text{s}$. If desired it can be adjusted by forcing a voltage on

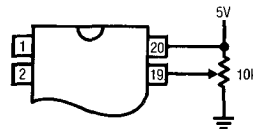


Figure 7. Adjusting the Conversion Time

Pin 19. With Pin 19 left open the conversion time runs $2.5\mu\text{s}$. A convenient way to force the voltage is with the circuit shown in Figure 7. To preset the conversion time to a fixed amount a resistor may be tied from Pin 19 to V_{CC} or GND. Tying it to V_{CC} slows down the conversion and tying it to GND will speed it up (see Typical Curves).

ANALOG INTERFACE

The inclusion of a high quality sample-and-hold (S/H) simplifies the analog interface to the LTC1099. All of the error terms normally associated with an S/H (hold step, offset, gain, and droop errors) are included in the error specifications for the A/D. This makes it easy for the designer since all the error terms need not be taken into account individually.

S/H Timing

A falling edge on the \overline{RD} or \overline{WR} input switches the S/H from acquire to hold and starts the conversion. The aperture time is the delay from the falling edge to the actual instant when the S/H switches to hold. It is typically 110ns.

As soon as a conversion is complete ($2.5\mu\text{s}$ typ.) the S/H switches back to the sample mode. Even though the acquisition time is only 240ns a new conversion cannot be started for 700ns (typ.) after a conversion is completed.

Analog Input

The input to the A/D looks like a 60pF capacitor in series with 550Ω (Figure 8).

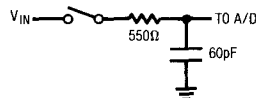


Figure 8. Equivalent Input Circuit

With this high input capacitance care must be taken when driving the inputs from a source amplifier. When the input switch closes an instantaneous capacitive load is applied to the amplifier output. This acts like an impulse into the amplifier and if it has poor phase margin the resulting ringing can cause a considerable loss of accuracy. If the amplifier is too slow the resulting settling tail will also cause a loss of accuracy. The amplifier should also have low open circuit output impedance. The LT1006 is an excellent amplifier in this regard. It also works with a single supply which fits nicely with the LTC1099.

Reference Inputs

Sixteen equal valued resistors are internally connected between REF+ and REF-. Each resistor is nominally 200Ω giving a total resistance of $3.2k\Omega$ between the reference terminals. When V_{IN} equals REF+ the output code will be all ones. When V_{IN} equals REF- the output code will be all zeros.

ANALOG INTERFACE

Although it is most common to connect REF+ to a 5V reference and REF- to ground, any voltages can be used. The only restrictions are REF+ > REF- and REF+ and REF- must be within the supply rails. As the reference voltage is reduced the A/D will eventually lose accuracy. Accuracy is quite good for references down to 1V.

Even though the reference drives a resistive ladder a lot of capacitive switching is taking place internally. For this reason driving the reference has the same characteristics as driving V_{IN} . A fast low impedance source is necessary. The reference has the additional problem of presenting a DC load to the driving source. This requires the DC as well as the AC source impedance to be low.

Good Grounding

As with any precise analog system care must be taken to follow good grounding practices when using the LTC1099. The most noise free environment is obtained by using a ground plane with GND (Pin 10) and REF- (Pin 11) tied to it. Bypass capacitors from REF+ (Pin 12) and V_{CC} (Pin 20) with short leads are also required to prevent spurious switching noise from affecting the conversion accuracy.

If a ground plane is not practical, single point grounding techniques should be used. Ground for the A/D should not be mixed in with other noisy grounds.

APPLICATIONS

Analog Multiplier

The schematic Figure 9 shows the LTC1099 configured with a DAC to form a 2 quadrant analog multiplier. An input waveform is applied to the LTC1099 where it is digitized at a 300kHz rate. The digitized signal is fed to the DAC in "flow through" mode where another signal is input to the DAC reference input. In this way the two analog signals are multiplied to produce a Double Sideband Amplitude Modulated Output. Figure 10 shows a 3kHz sine wave multiplied by a 100Hz triangle.

Note that since this is only a 2 quadrant multiplier a carrier component (the input to the LTC1099) will appear in the output spectrum. Figure 11 shows the frequency spectrum of a 42.5kHz sine wave multiplied by a 5kHz sine wave. The depth of modulation is about 30dB. Figure 12 shows a 42.375kHz sine wave multiplied by a 30.875kHz sine wave. Note that at these higher frequencies, the depth of modulation is still about 30dB. The carrier feed through is seen in Figure 12.

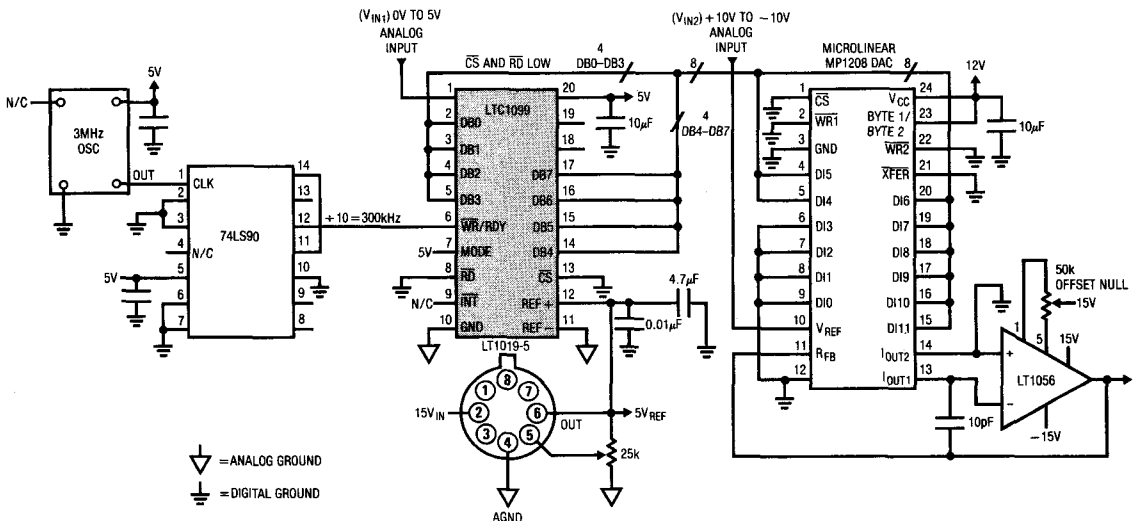


Figure 9.

ANALOG INTERFACE

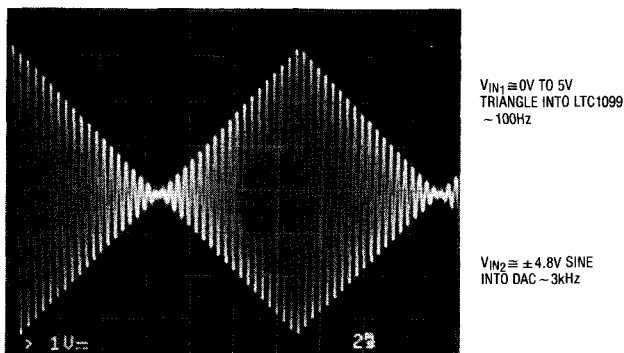


Figure 10.

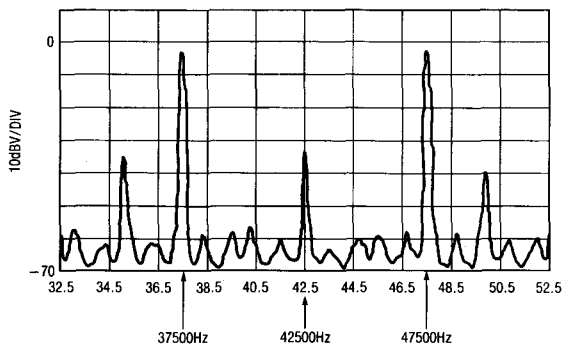


Figure 11. Two Quadrant Multiplier Output Spectrum with 0V to 4.5V at 42.5kHz into LTC1099 and $\pm 2V$ at 5kHz into DAC

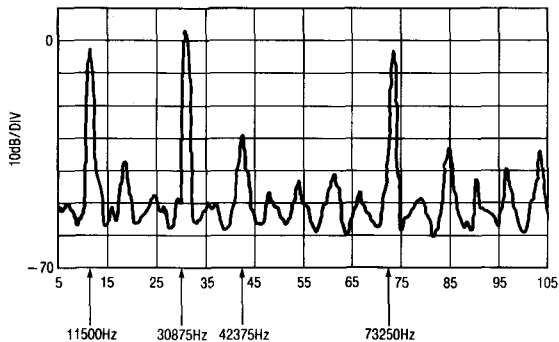
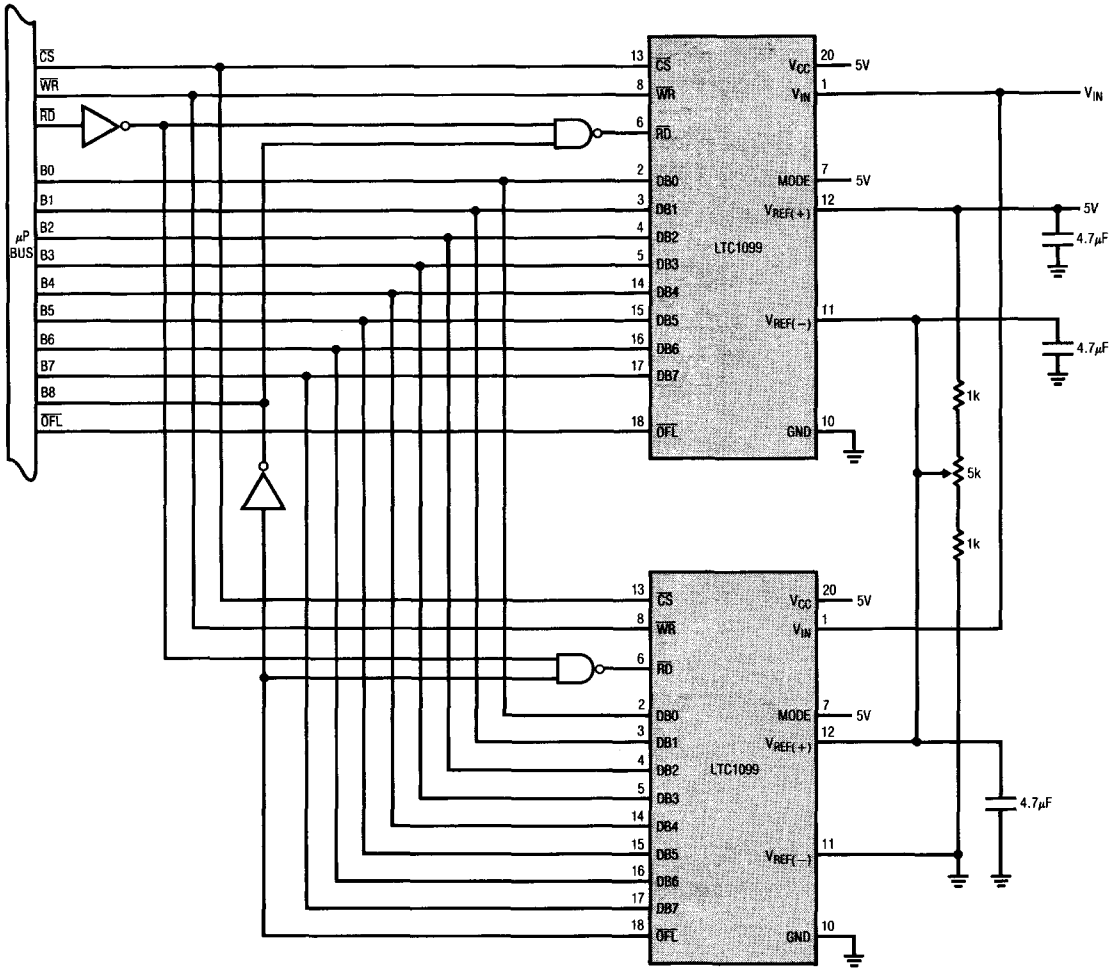


Figure 12. Two Quadrant Multiplier Output Spectrum with 0V to 4.5V at 42.375kHz into LTC1099 and $\pm 2V$ at 30.875kHz into DAC

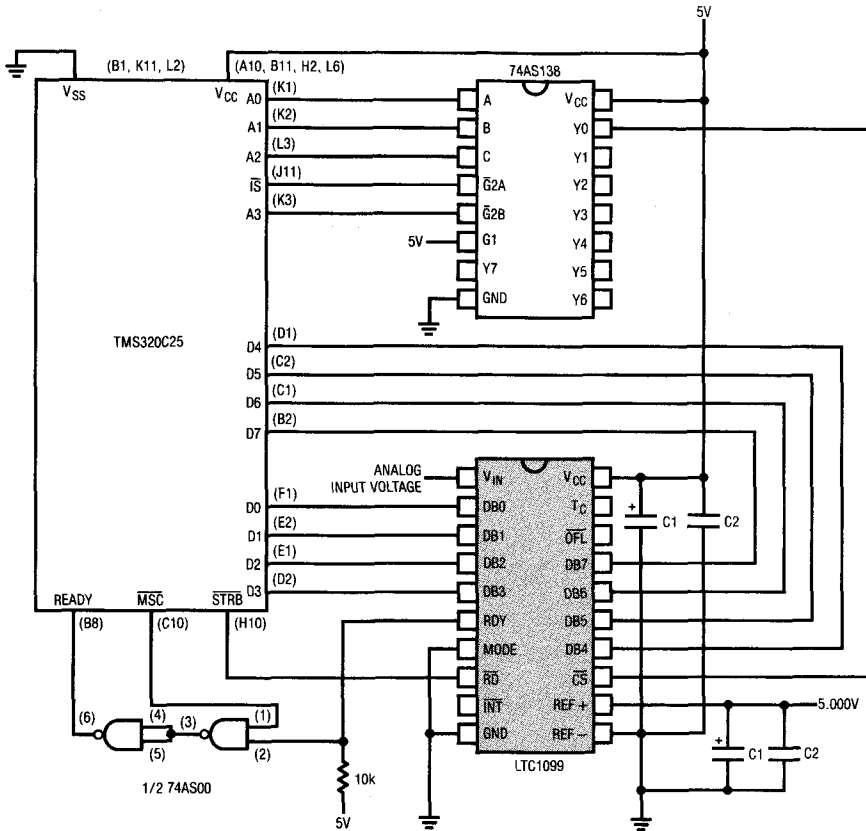
TYPICAL APPLICATIONS

Cascading for 9-Bit Resolution



TYPICAL APPLICATIONS

TMS320C25 Interface Using RD-Mode



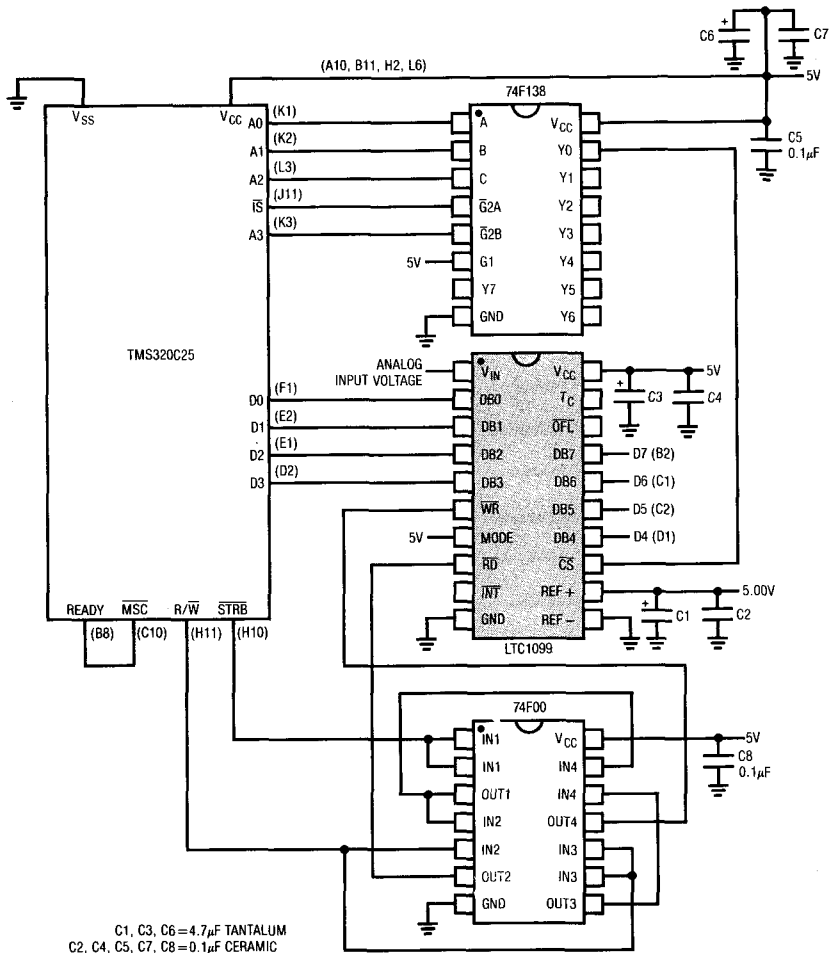
C1 = 4.7µF TANTALUM
C2 = 0.1µF CERAMIC

TMS320C25 Assembly Code for RD-Mode Interface to LTC1099

0001	0000				
0002	0032		AORG	>32	
0003	0032	CE01	DINT		Disable Interrupts
0004	0033	C800	LDPK	>00	Data Page Pointer is 0
0005	0034	8064	LOOP	IN 100,PA0	Input 1099 Data to Address 100
0006	0035	CB13	RPTK	12	Repeat Next Instruction 12 Times
0007	0036	5500	NOP		Don't Convert Again Too Soon
0008	0037	FF80	B	LOOP	Go for Another Conversion

TYPICAL APPLICATIONS

TMS320C25 Interface Using WR-RD Mode

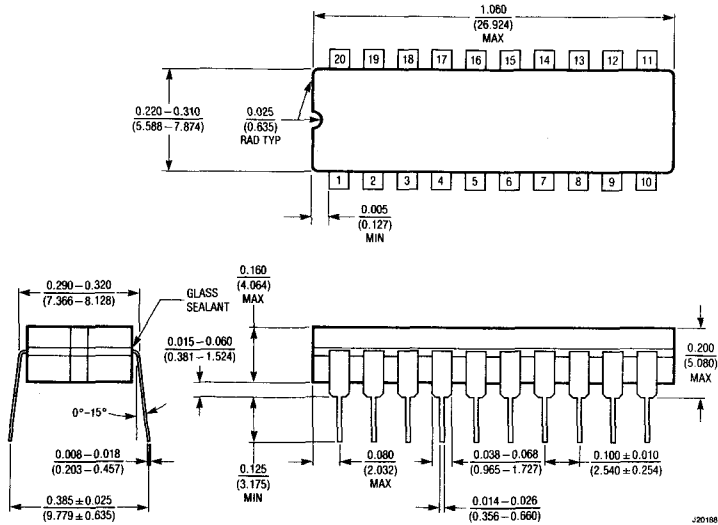


TMS320C25 Assembly Code for WR-RD-Mode Interface to LTC1099

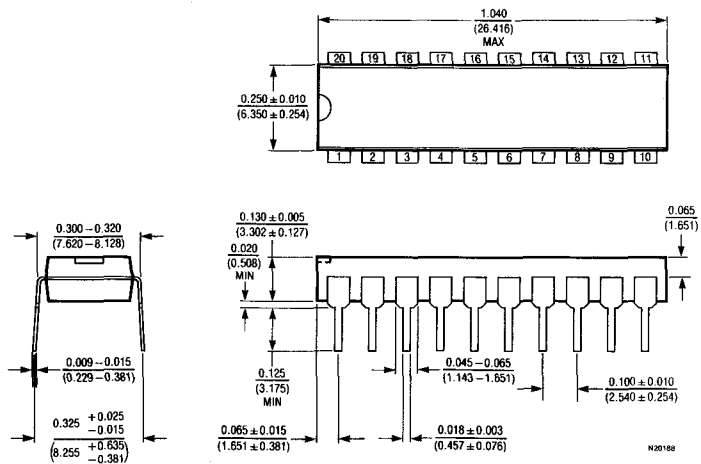
0001	0032			AORG	> 32	
0002	0032	CE01		DINT		Disable Interrupts
0003	0033	C800		LDPK	> 0	Data Page Pointer is ϕ
0004	0034	E064	LOOP	OUT	> 64.PA0	Start LTC1099 Conversion
0005	0035	CB20		RPTK	> 12	Wait for Conversion to Finish
0006	0036	5500		NOP		
0007	0037	8064		IN	> 64.PA0	Read LTC1099 Data; Store in > 64
0008	0038	FF80		B	LOOP	Do Again

PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

J Package
20-Lead Ceramic DIP



N Package
20-Lead Plastic DIP



FEATURES

- *Guaranteed* 6 μ s Max. Acquisition Time
- *Guaranteed* 0.005% Max. Gain Error
- *Guaranteed* 1mV Max. Offset Voltage
- *Guaranteed* 1mV Max. Hold Step
- Very Low Feedthrough 86dB Min.
- High Input Impedance under All Conditions
- Logic Inputs Compatible with All Logic Families

APPLICATIONS

- 12-Bit Data Acquisition Systems
- Ramp Generators
- Analog Switches
- Staircase Generators
- Sample and Difference Circuits

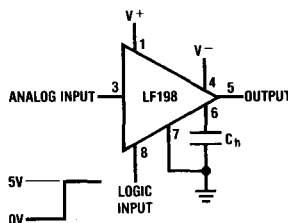
DESCRIPTION

The LF198 is a precision sample and hold amplifier which uses a combination of bipolar and junction FET transistors to provide precision, high speed, and long hold times. A typical offset voltage of 1mV and gain error of 0.002% allow this sample and hold amplifier to be used in 12-bit systems. Dynamic performance can be optimized by proper selection of the external hold capacitor. Acquisition times can be as low as 4 μ s for small capacitors while hold step and droop respectively when using larger capacitors.

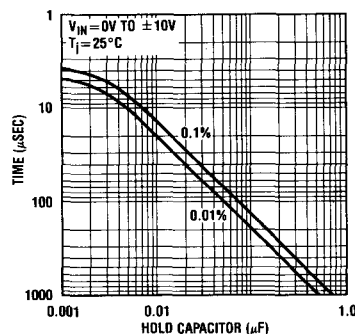
The LF198 is fixed at unity gain with 10¹⁰ Ω input impedance independent of sample / hold mode. The logic inputs are high impedance differential to allow easy interfacing to any logic family without ground loop problems. A separate offset adjust pin can be used to zero the offset voltage in either the sample or hold mode. Additionally, the hold capacitor can be driven with an external signal to provide precision level shifting or "differencing" operation. The device will operate over a wide supply voltage range from ± 5 V to ± 18 V with very little change in performance, and key parameters are specified over this full supply range.

The LF198A version offers tightened electrical specifications for key parameters.

Basic Sample and Hold



Acquisition Time



LF198A/LF398A
LF198/LF398

ABSOLUTE MAXIMUM RATINGS

Input Voltage Equal to Supply Voltage
 Logic to Logic Reference Differential Voltage (Note 2) +30V, -30V
 Output Short Circuit Duration Indefinite
 Hold Capacitor Short Circuit Duration 10 sec
 Lead Temperature (Soldering, 10 seconds) 300°C
 Supply Voltage ±18V
 Power Dissipation (Package Limitation) (Note 1) 500mW
 Operating Temperature Range
 LF198/LF198A -55°C to 125°C
 LF398/LF398A 0°C to 70°C
 Storage Temperature Range -65°C to 150°C

PACKAGE/ORDER INFORMATION

<p>TOP VIEW H PACKAGE METAL CAN</p>	ORDER PART NUMBER
	LF198AH LF198H LF398AH LF398H
<p>TOP VIEW N8 PACKAGE PLASTIC DUAL IN LINE</p>	LF398J8 LF398AN8 LF398N8

ELECTRICAL CHARACTERISTICS (Note 3)

PARAMETER	CONDITIONS	LF198A			LF398A			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage (Note 6)			0.5	1	1	2		mV
Input Bias Current (Note 6)			5	25	10	25		nA
Input Impedance				75		50		nA
Gain Error	$R_L = 10k$		10^{10}		10^{10}			Ω
Feedthrough Attenuation Ratio at 1kHz	$C_h = 0.01\mu F$	86	96		86	96		dB
Output Impedance	"HOLD" Mode		0.5	1	0.5	1		Ω
"HOLD" Step (Note 4)	$C_h = 0.01\mu F, V_{OUT} = 0$			4		6		Ω
Supply Current (Note 6)	$T_j \geq 25^\circ C$		0.25	1	0.25	1		mV
Logic and Logic Reference Input Current			4.5	5.5	4.5	6.5		mA
Leakage Current into Hold Capacitor (Note 6)	"HOLD" Mode (Note 5)		2	10	2	10		μA
Acquisition Time to 0.1%	$\Delta V_{OUT} = 10V, C_h = 1000pF$ $C_h = 0.01\mu F$		10	100	10	100		pA
Hold Capacitor Charging Current	$V_{IN} - V_{OUT} = 2V$		4	6	4	6		μs
Supply Voltage Rejection Ratio	$V_{OUT} = 0$		16	25	16	25		μs
Differential Logic Threshold		90	110		90	110		dB
		0.8	1.4	2.4	0.8	1.4	2.4	V

ELECTRICAL CHARACTERISTICS (Note 3)

PARAMETER	CONDITIONS	LF198			LF398			UNITS	
		MIN	TYP	MAX	MIN	TYP	MAX		
Input Offset Voltage (Note 6)		●		1	3		2	7	mV
					5		10		mV
Input Bias Current (Note 6)		●		5	25		10	50	nA
					75		100		nA
Input Impedance			10^{10}			10^{10}		Ω	
Gain Error	$R_L = 10k$	●		0.002	0.005		0.004	0.01	%
					0.02		0.02		%
Feedthrough Attenuation Ratio at 1kHz	$C_H = 0.01\mu F$		86	96		80	96		dB
Output Impedance	"HOLD" Mode	●		0.5	2		0.5	4	Ω
					4		6		Ω
"HOLD" Step (Note 4)	$C_H = 0.01\mu F, V_{OUT} = 0$		0.5	2.0		0.5	2.5	mV	
Supply Current (Note 6)	$T_J \geq 25^\circ C$		4.5	5.5		4.5	6.5	mA	
Logic and Logic Reference Input Current			2	10		2	10	μA	
Leakage Current into Hold Capacitor (Note 6)	"HOLD" Mode (Note 5)		30	100		30	200	μA	
Acquisition Time to 0.1%	$\Delta V_{OUT} = 10V, C_H = 1000pF$ $C_H = 0.01\mu F$		4			4		μS	
			16			16		μS	
Hold Capacitor Charging Current	$V_{IN} - V_{OUT} = 2V$		5			5		mA	
Supply Voltage Rejection Ratio	$V_{OUT} = 0$		80	110		80	110	dB	
Differential Logic Threshold			0.8	1.4	2.4	0.8	1.4	2.4	V

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: T_J max for the LF198/LF198A is $150^\circ C$; T_J max for the LF398/LF398A is $100^\circ C$.

Note 2: The logic inputs are protected to $\pm 30V$ differential as long as the voltage on both pins does not exceed the supply voltage. For proper operation, however, both logic and logic reference pins must be at least 2V below the positive supply and one of these pins must be at least 3V above the negative supply.

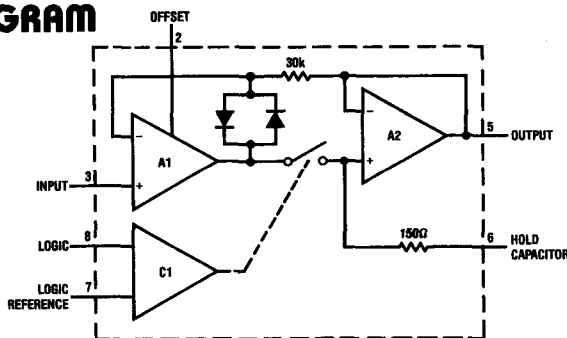
Note 3: Unless otherwise noted, $V_S = \pm 15V, T_J = 25^\circ C, -11.5V \leq V_{IN} \leq +11.5V, C_H = 0.01\mu F, R_L = 10k\Omega$ and unit is in "sample" mode. Logic reference = 0V and logic voltage = 2.5V.

Note 4: The hold step is sensitive to stray capacitance coupling between input logic signals and the hold capacitor. 1pF, for instance, will create an additional 0.5mV step with a 5V logic swing and a $0.01\mu F$ hold capacitor. Magnitude of the hold step is inversely proportional to hold capacitor value.

Note 5: Leakage current is measured at a junction temperature of $25^\circ C$. The effects of junction temperature rise due to power dissipation or elevated ambient can be calculated by doubling the $25^\circ C$ value for each $11^\circ C$ increase in chip temperature. Leakage is guaranteed over full input signal range.

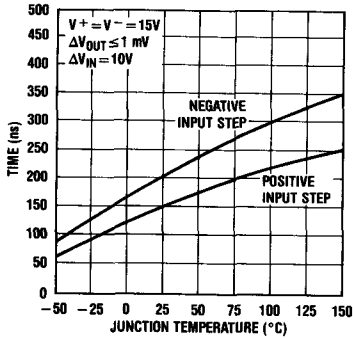
Note 6: These parameters are guaranteed over a supply voltage range of $\pm 5V$ to $\pm 18V$.

FUNCTIONAL DIAGRAM



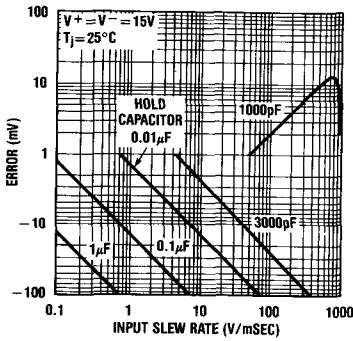
TYPICAL PERFORMANCE CHARACTERISTICS

Aperture Time*



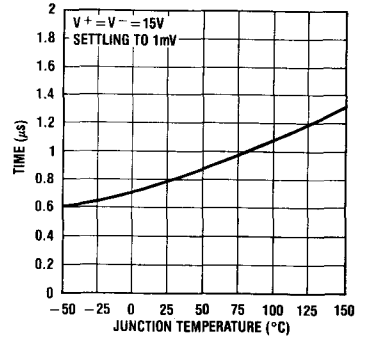
*See Definition of Terms

Dynamic Sampling Error*



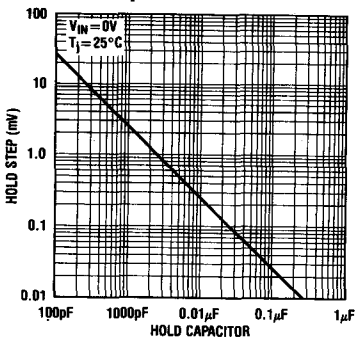
*See Definition of Terms

“Hold” Settling Time*

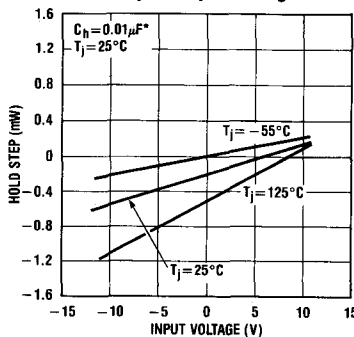


*See Definition of Terms

Hold Step

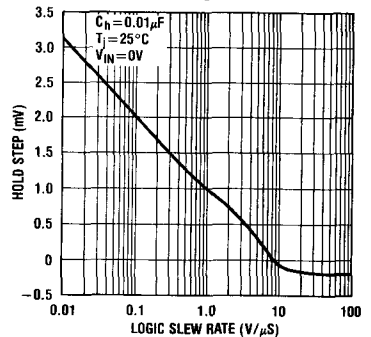


Hold Step vs Input Voltage

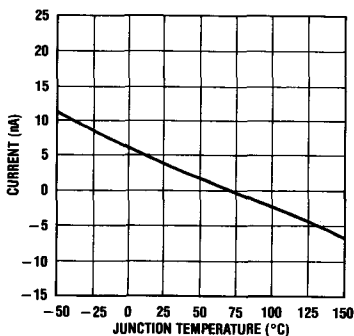


*Amplitude of hold step scales inversely with hold capacitor value

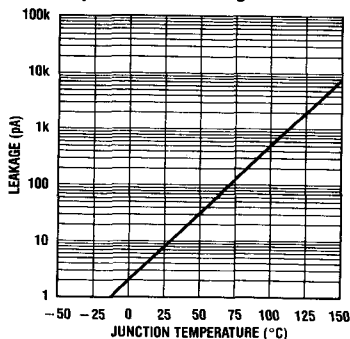
Hold Step vs Logic Slew Rate



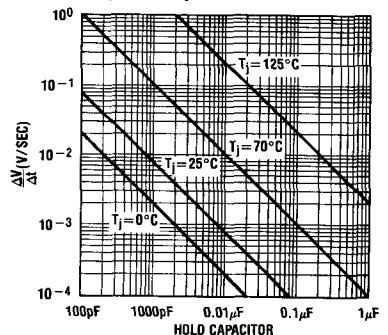
Input Bias Current



Capacitor Pin Leakage

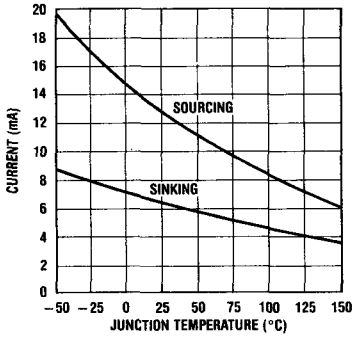


Output Droop Rate

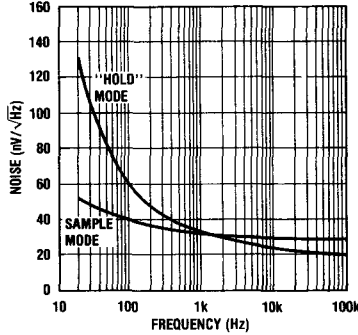


TYPICAL PERFORMANCE CHARACTERISTICS

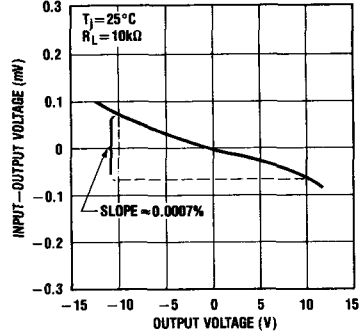
Output Short Circuit Current



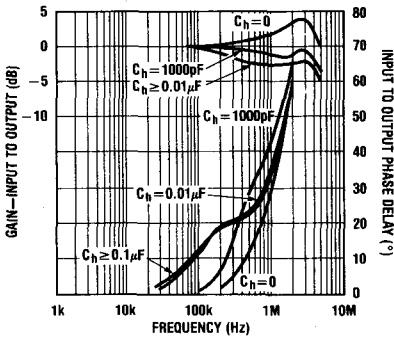
Output Noise



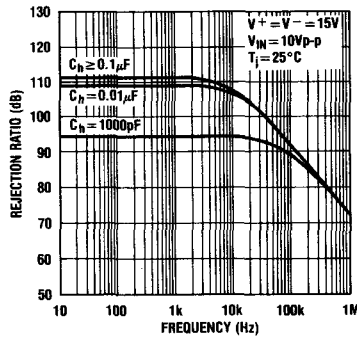
Gain Error



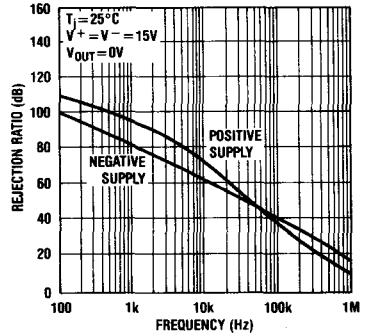
Phase and Gain (Input to Output, Small Signal)



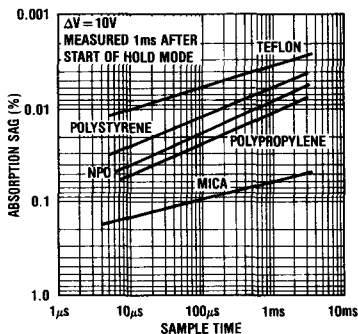
Feedthrough Rejection Ratio



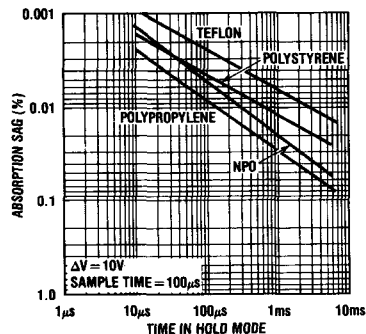
Power Supply Rejection



Capacitor Dielectric Absorption

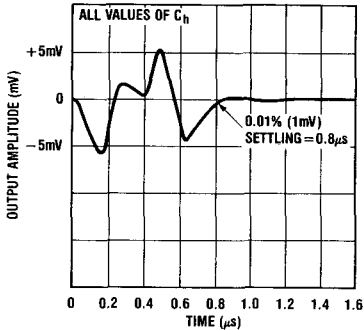


Capacitor Dielectric Absorption

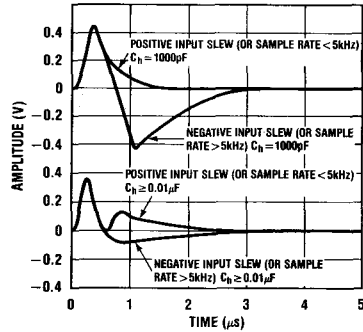


TYPICAL PERFORMANCE CHARACTERISTICS

Output Transient at Start of Hold Mode



Output Transient at Start of Sample Period



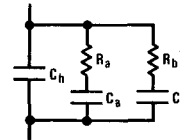
APPLICATIONS INFORMATION

Hold Capacitor

For fast sample and hold applications, the size of the hold capacitor is critical. A low value will give fast acquisition, but will also increase errors due to hold step, and droop caused by amplifier bias current. The capacitor should be made as large as possible, consistent with acquisition time and dynamic sampling error requirements. Capacitors larger than $0.1\mu\text{F}$ have an additional problem. They are generally not available in the low loss dielectrics like Teflon, Polystyrene, and NPO, at least not at a reasonable price and size. Mylar, even with its poor dielectric absorption properties, may be a reasonable choice where very long sample times are used and low droop rates are needed.

Dielectric absorption in the hold capacitor can often be the major source of error in a sample and hold. The equivalent "circuit" of a typical capacitor is shown below with parallel RC networks used to model dielectric absorption.

Typical Hold Capacitor Equivalent Circuit



$C_a, C_b = 0.01$ TO $0.1 C_h$
 R_a, R_b GENERATE TIME CONSTANTS
OF 0.1-50 MILLISECONDS WITH C_a, C_b

One can see that rapid changes in capacitor voltage will not be tracked by the internal parasitic capacitors because of the resistance in series with them. This leads to a "sag" effect in the hold capacitor after a sudden change in voltage followed by rapid switch to the hold mode. The capacitor remembers its previous state via the charge on the internal parasitic capacitance and sags

APPLICATIONS INFORMATION

back slightly toward the previous voltage. The magnitude of the sag depends on the voltage change and the time spent sampling the new voltage. Several time constants are typically evident in the sag, although some capacitors tend to exhibit a single time constant, while others show a sag that indicates a blending of many time constants. The curves labeled CAPACITOR DIELECTRIC ABSORPTION show the amount of sag found after a 10V step with sample time at the new voltage and hold time at the new voltage as variables. It is obvious that sag problems are minimized by long sample times and short hold times. This is often in conflict with basic sampling requirements, but one point should be made: if at all possible, keep the sample and hold amplifier in the "tracking", or sampling, mode as much as possible to maximize the time the hold capacitor spends near the voltage at which it will eventually "hold".

The best capacitor for sample and hold applications is Teflon. It is clearly superior with regard to dielectric absorption and operates over the full -55°C to 125°C temperature range. If size or price becomes a problem, the second choice for full temperature range operation is "NPO", or "COG" ceramic units. Some care must be used here—not all NPO capacitors use the low dielectric constant ceramic necessary for low dielectric absorption. For lower temperatures ($\leq 70^{\circ}\text{C}$), Polystyrene has traditionally been the best hold capacitor. The best units are cylindrical and fairly large—there seems to be a strong correlation between small size and poorer dielectric performance. Polypropylene has nearly the same absorption properties as polystyrene and offers 85°C operation. It also tends to be smaller. Again, stay with cylindrically wrapped units. Other standard dielectrics such as mica, glass, mylar, and ordinary ceramic are much worse with regard to dielectric absorption. Mylar is sometimes used for large values when the ratio of sample to hold time is large and extremely low droop is required.

Dynamic Sampling Error

A significant sampling error can occur in any sample and hold if the input is moving when the unit is put into the hold mode. The two major causes for this error are digital delay in switch opening and analog delay across the hold capacitor.

The switch opening delay is obvious and leads to a "held" output error of $(dv/dt) \times (T_d)$, where dv/dt is the slew rate of the input signal and T_d is switch delay. In the case of the LF198, T_d is approximately 150ns, giving a 4.5mV error when sampling the zero crossing of a 5V (peak) sine wave at 1kHz ($dv/dt = A \cdot 2\pi f = 5 \cdot 2\pi \cdot 10^3$). The analog delay is the difference between input signal and capacitor voltage. It is determined by the RC product of the hold capacitor and the effective series resistance, which in the case of the LF198 is about 150Ω . This analog delay with a $0.01\mu\text{F}$ hold capacitor is $R \cdot C = 150 \times 10^{-8} = 1.5\mu\text{s}$, or about ten times the delay of the switch. The sign of the analog delay is negative—the held output is related in time to the input voltage *before* the hold command was given. The overall dynamic sampling error is the sum of the digital and analog errors. The curve labeled *Dynamic Sampling Error* will be helpful in estimating these errors as a function of input slew rate and hold capacitor size.

Dynamic sampling error can be reduced by a factor of ten or more by inserting a delay in the logic input so that the "hold" command is delayed by an amount equal to the RC time constant of the LF198 and external hold capacitor. For a $0.01\mu\text{F}$ hold capacitor and the 150Ω resistor internal to the LF198, this is $1.5\mu\text{s}$. A simple RC network can be used in front of the logic input for delays up to $\approx 1\mu\text{s}$. Longer delays require the addition of a logic gate to speed up the rise time of the delayed signal. See LOGIC RISE TIME in this section for further details.

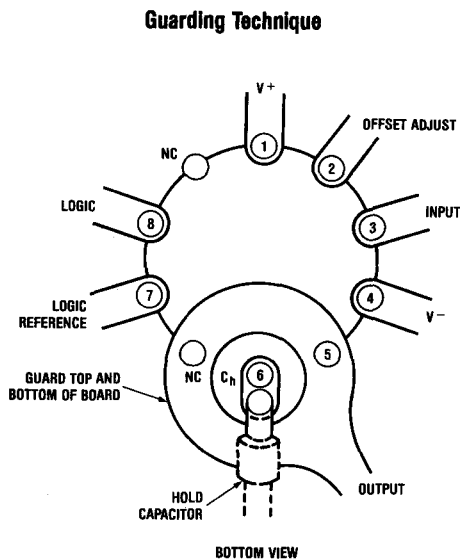
Hold Step

Hold step is the small voltage step (after settling) seen at the output of a sample and hold amplifier when it is switched from the sample mode to the hold mode with a steady DC input. Hold step is typically the result of, or can be modeled as, a fixed quantity of charge transferred to the hold capacitor as a result of the internal switching that occurs during the hold command. In the case of the LF198, that charge is about 5 picocoulombs, giving a hold step of 0.5mV for a $0.01\mu\text{F}$ hold capacitor and 5mV for a 1000pF hold capacitor. ($V = Q/C$.) Hold step is reasonably independent of logic amplitude if care is taken to minimize the stray capacitance between the logic input

9

APPLICATIONS INFORMATION

and the hold capacitor. With thoughtful layout, including the guarding technique shown below, stray capacitance should be under 0.3pF, limiting charge variations to less than 0.3 picocoulombs per volt.



Use 10-pin layout. Guard around C_H is tied to output.

Hold step varies slightly with analog input voltage (see curves). A typical unit will change at 0.4 picocoulombs per volt. This manifests itself as a gain error when the amplifier is switched to the hold mode. With a $0.01\mu\text{F}$ capacitor, the resulting gain error will be $(0.4 \text{ PC/V}) / 0.01\mu\text{F} = 0.004\%$. This gain error is in the opposite direction of DC (sample mode) gain error. At high values of hold capacitor, DC gain error will dominate and gain will be slightly below unity (0.002%). For low value capacitors ($< 0.01\mu\text{F}$), hold step induced gain error will dominate and hold mode gain will be slightly above unity. Zeroing out hold step does not change the variation of hold step with regard to input voltage.

Offset Zeroing

A sample and hold amplifier has two distinct offset voltages. The first is just the DC offset of the amplifier while in the sample or "tracking" mode. It is identical to the input offset of any operational amplifier. The second offset voltage is the sum of the DC offset plus a dynamic term called hold step. Hold step is a change in output voltage when the amplifier is switched from sample mode to hold mode, with the input held steady. This second offset is often called hold mode offset. It can be less than or much greater than the DC offset, depending on the magnitude and sign of hold step.

A fairly accurate model for hold step is a fixed charge injected into the hold capacitor by the switch turn-off circuitry. The magnitude of the charge is reasonably independent of logic input amplitude. The resulting change in hold capacitor voltage is Q/C_H . The charge, Q , is typically 5 picocoulombs, giving a 0.5mV hold step with a $0.01\mu\text{F}$ hold capacitor. Since most sample and hold amplifiers are "used," i.e., have their outputs read by an A to D converter, etc., during the hold mode, hold mode offset is arguably much more important than sample mode DC offset.

DC offset adjustment is accomplished with a 1k low TC cermet potentiometer tied to V^+ with 0.6mA flowing through it and the wiper tied to pin 2. This allows pin 2 to be moved $\pm 300\text{mV}$ around its nominal voltage (0.3V below V^+). Offset adjustment range is $\pm 9\text{mV}$, and the adjustment procedure nominally improves offset drift when the DC offset is reduced to zero. This offset method *can* be used to zero out hold mode offset, but at the expense of some induced offset drift. Each millivolt of hold step offset that is corrected by this method introduces $3.3\mu\text{V}/^\circ\text{C}$ drift. For $0.002\mu\text{F}$ or larger hold capacitors where hold step is a few millivolts or less, this is a practical solution to hold mode offset. In precision wide temperature range applications, or where C_H is less than $0.002\mu\text{F}$, a separate hold mode zeroing method should be used. The circuit shown in the application section using a logic inverter and a 5pF capacitor is recommended (DC AND AC ZEROING).

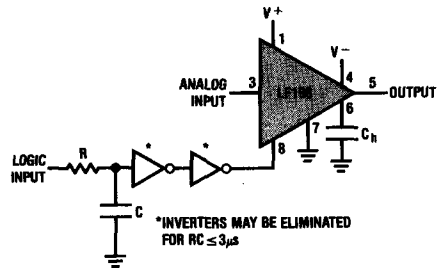
APPLICATIONS INFORMATION

Logic Fall Time

Hold step is independent of logic input fall time only for fall times faster than $10V/\mu s$. For instance, as logic fall time changes from $10V/\mu s$ to $1V/\mu s$, hold step with a $0.01\mu F$ hold capacitor will typically increase from $0.25mV$ to $1.0mV$. See the curve labeled HOLD STEP vs LOGIC SLEW RATE for further data points. If logic slew rate is not constant, use the value at the threshold point ($1.5V$ with respect to logic reference). An RC network will have a discharge slew rate of V_L/RC , where V_L is the logic threshold of the LF198. The delay generated by the network will be $RC \ln(V^+/V_L)$, where V^+ is logic amplitude. For a $1\mu s$ delay, with $5V$ logic, an RC time constant of $0.8\mu s$ is needed. This has a slew rate of $2V/\mu s$ at threshold, which will slightly degrade hold step. It is obvious that an RC delay network significantly longer than

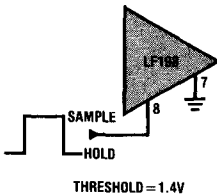
$1\mu s$ will have a large effect on hold step. If longer delays are required, they should be followed by several inverter stages or a Schmitt trigger to increase slew rate.

Adding Delay to Logic Input

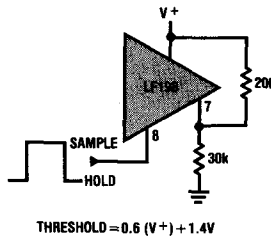


LOGIC INPUT CONFIGURATIONS*

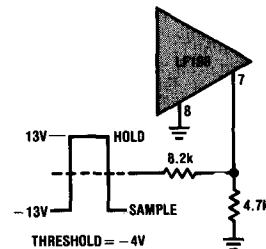
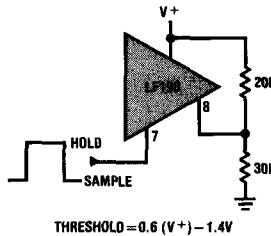
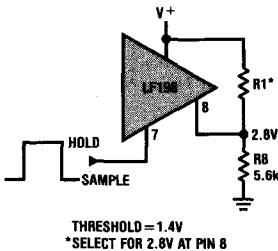
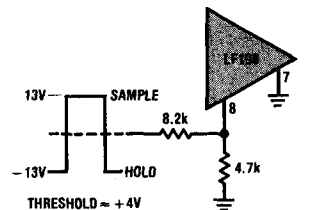
TTL and CMOS
 $3V \leq V_L$ (Hi State) $\leq 10V$



CMOS
 $7V \leq V_L$ (Hi State) $\leq 15V$



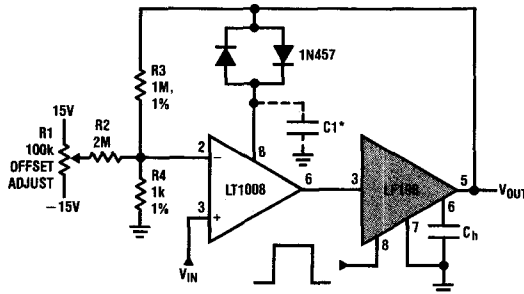
Op Amp Drive



*The logic input signal high state must be at least 2V below the positive supply voltage of the LF198.

TYPICAL APPLICATIONS

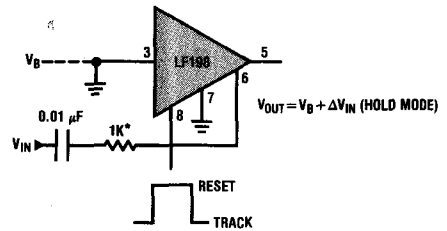
X1000 Sample and Hold



*FOR LOWER GAINS, THE LT1008 MUST BE FREQUENCY COMPENSATED

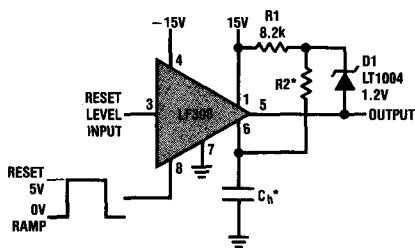
USE $\approx \frac{100}{A_v}$ pF FROM COMP 2 TO GROUND

Sample and Difference Circuit (Output Follows Input in Hold Mode and Resets to V_B in Sample Mode)



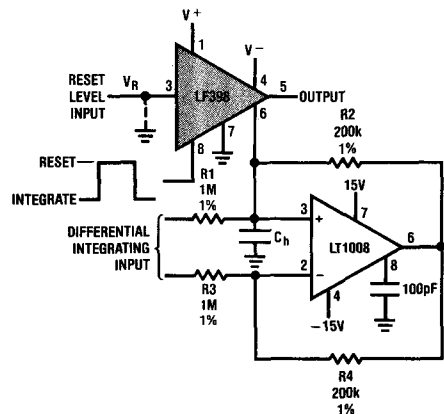
*THIS RESISTOR PROTECTS INPUT FROM SURGE CURRENTS, BUT INCREASES SAMPLE TIME. IT CAN BE ELIMINATED IF INPUT IS OTHERWISE PROTECTED.

Ramp Generator with Variable Reset Level



*SELECT FOR RAMP RATE $\frac{\Delta V}{\Delta T} = \frac{1.2V}{(R2)C_h}$
 $R \geq 10k$

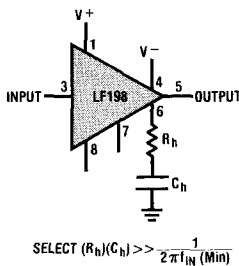
Integrator with Programmable Reset Level



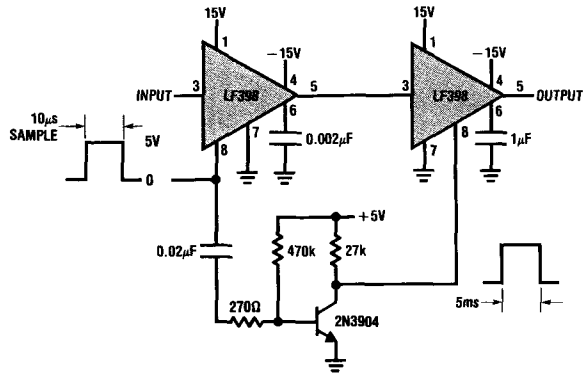
$$V_{OUT}(\text{HOLD MODE}) = \left[\frac{1}{(R1)C_h} \int_0^t V_{IN} dt \right] + [V_R]$$

TYPICAL APPLICATIONS

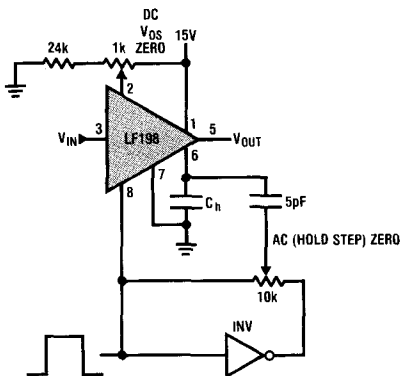
Output Holds at Average of Sampled Input



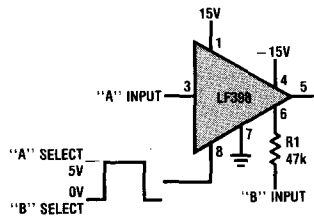
Fast Acquisition, Low Droop Sample and Hold



DC and AC Zeroing



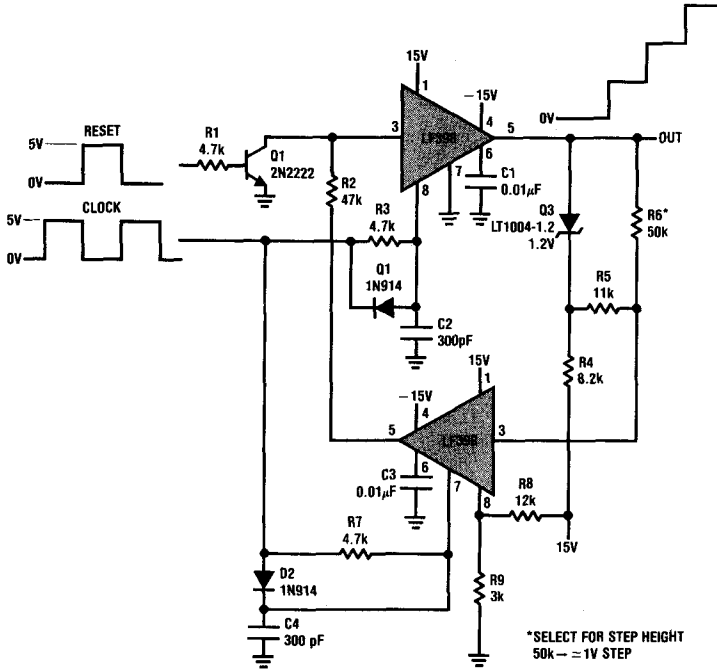
2-Channel Switch



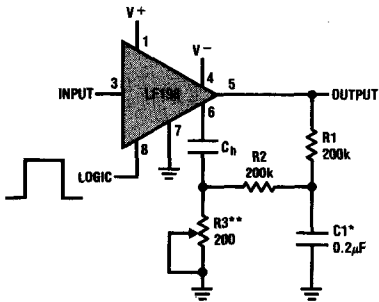
	A	B
Gain	$1 \pm 0.02\%$	$1 \pm 0.2\%$
Z _{IN}	$10^{10}\Omega$	47kΩ
BW	$\approx 1\text{MHz}$	$\approx 400\text{kHz}$
Crosstalk @ 1kHz	-90dB	-90dB
Offset	$\leq 6\text{mV}$	$\leq 75\text{mV}$

TYPICAL APPLICATIONS

Staircase Generator

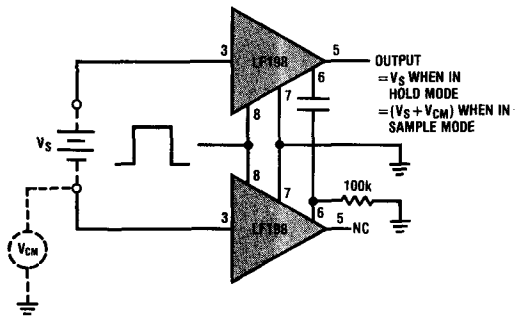


Capacitor Hysteresis Compensation



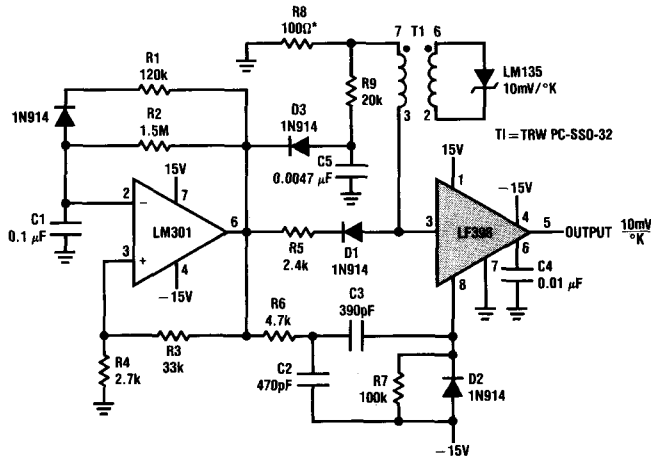
*SELECT FOR TIME CONSTANT $C1 = \frac{T}{100k}$
 **ADJUST FOR AMPLITUDE

Differential Hold



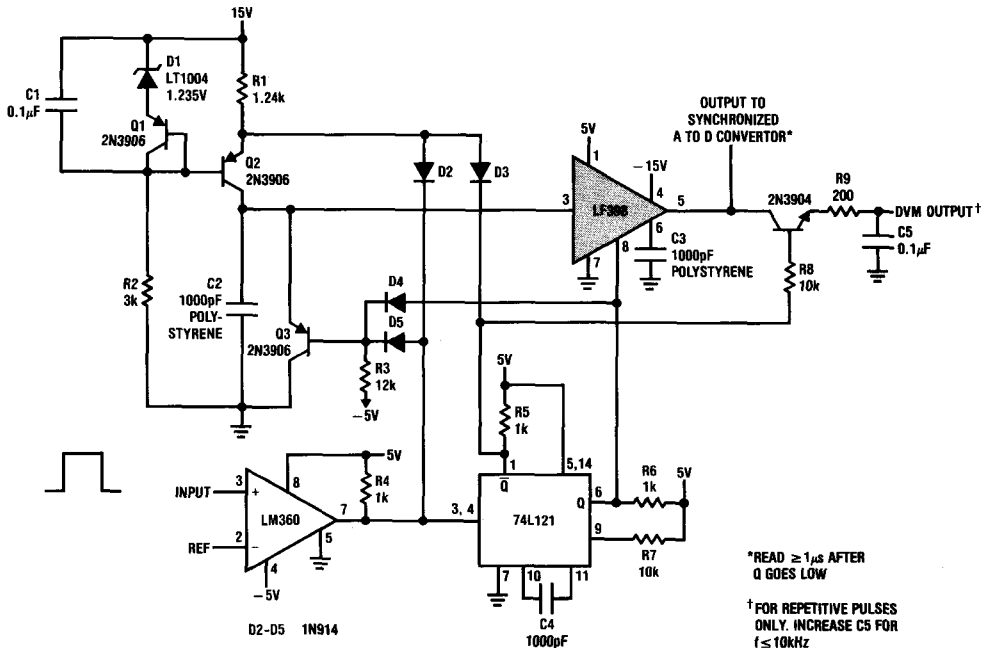
TYPICAL APPLICATIONS

Isolated Temperature Sensor



*COMPENSATES FOR TRANSFORMER RESISTANCE.
SELECT FOR FLAT OUTPUT FROM LF198 WHILE
IN SAMPLE MODE.

Pulse Width to Voltage Converter

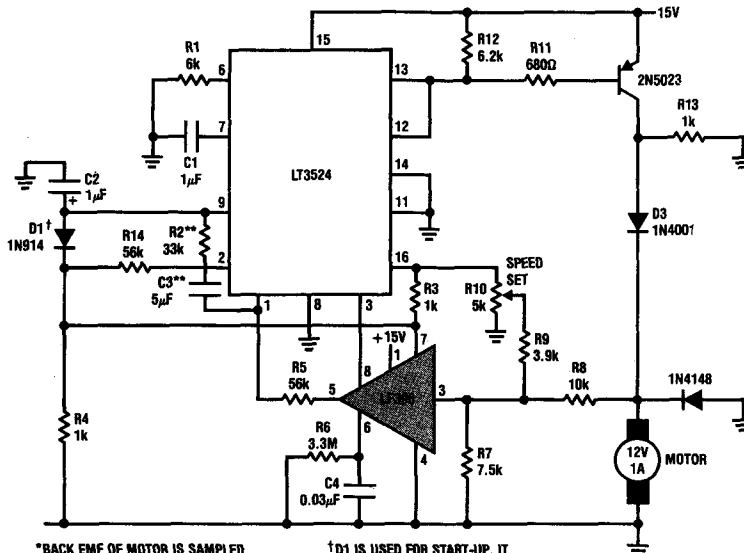


*READ $\geq 1\mu\text{s}$ AFTER
Q GOES LOW

† FOR REPETITIVE PULSES
ONLY. INCREASE C5 FOR
 $f \leq 10\text{kHz}$

TYPICAL APPLICATIONS

Motor Speed Controller Needs No Tachometer*



*BACK EMF OF MOTOR IS SAMPLED AND USED TO CONTROL SPEED.
 **SELECT FOR OPTIMUM LOOP STABILITY.
 C3 IS NON POLARIZED

†D1 IS USED FOR START-UP. IT LIMITS DUTY CYCLE TO ~75%

DEFINITION OF TERMS

Hold Step: The voltage step at the output of the amplifier when switching from sample mode to hold mode with a constant analog input voltage and a logic swing of 5V.

Acquisition Time: The time required to acquire, within a defined error, a new analog input voltage with an output change of 10V. Acquisition time includes output settling time and includes the time required for all internal nodes to settle so that the output is at the proper value when switched to the hold mode.

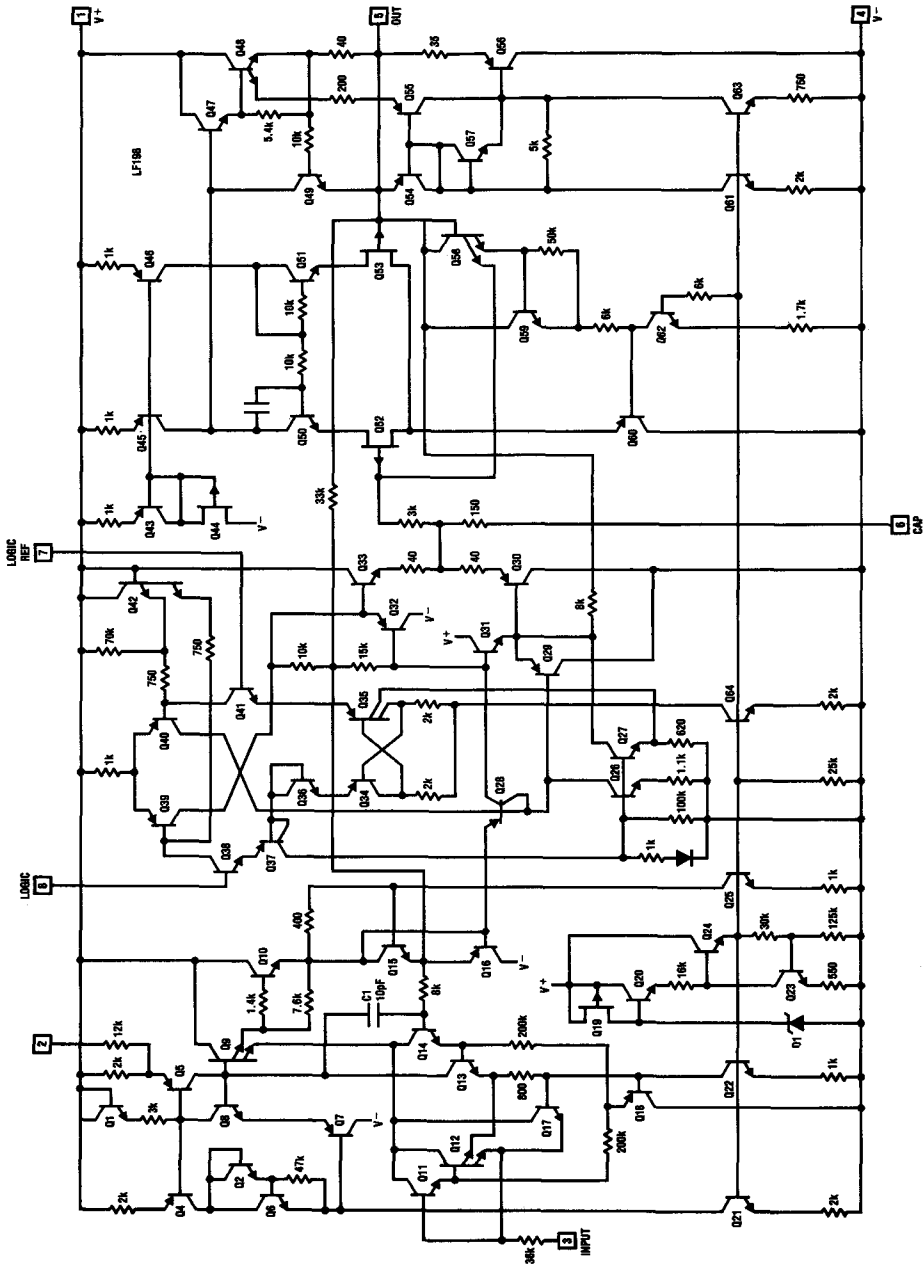
Gain Error: The ratio of output voltage swing to input voltage swing in the sample mode expressed as a percent difference.

Hold Settling Time: The time required for the output to settle within 1mV of final value after a hold command is initiated.

Dynamic Sampling Error: The error introduced into the held output voltage due to a changing analog input at the time the hold command is given. Error is expressed in mV with a given hold capacitor value and input slew rate. Note that this error term occurs even for long sample times.

Aperture Time: The delay required between "Hold" command and an input analog transition, so that the transition does not affect the held output.

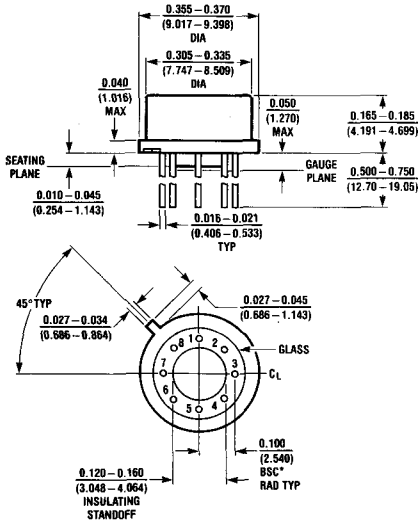
SCHEMATIC DIAGRAM



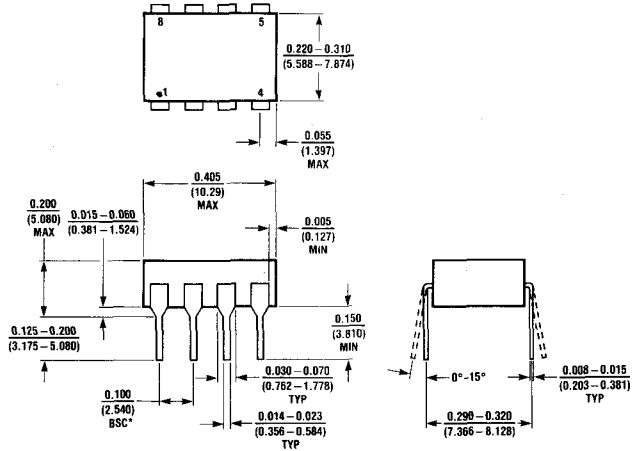
LF198A/LF398A LF198/LF398

PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

H Package Metal Can



J8 Package 8 Lead Hermetic DIP

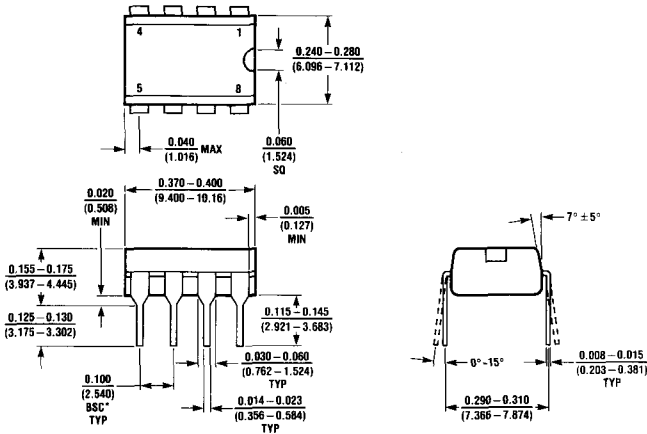


*LEADS WITHIN 0.007 OF TRUE POSITION (TP) AT GAUGE PLANE

	T _{max}	θ _{ja}	θ _{jc}
LF198/LF198A	150°C	150°C/W	45°C/W
LF398/LF398A	100°C	150°C/W	45°C/W

	T _{max}	θ _{ja}
LF398	100°C	100°C/W

N8 Package 8 Lead Plastic



*LEADS WITHIN 0.007 OF TRUE POSITION (TP) AT GAUGE PLANE

	T _{max}	θ _{ja}
LF398/LF398A	100°C	130°C/W

FEATURES

- 4 μ s Typical Acquisition Time
- *Guaranteed* 0.01% Max. Gain Error
- 2mV Typ. Offset Voltage
- 2.5mV Max. Hold Step
- Very Low Feedthrough 80dB Min.
- High Input Impedance Under All Conditions
- Logic Inputs Compatible with All Logic Families

APPLICATIONS

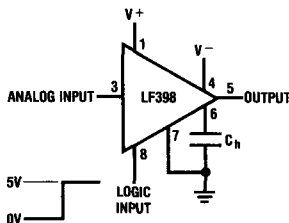
- 12-Bit Data Acquisition Systems
- Ramp Generators
- Analog Switches
- Staircase Generators
- Sample and Difference Circuits

DESCRIPTION

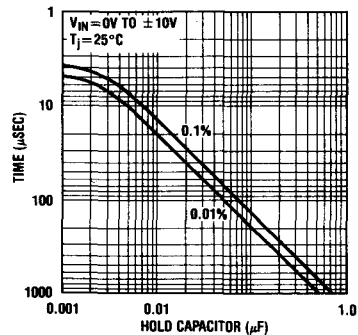
The LF398 is a precision sample and hold amplifier which uses a combination of bipolar and junction FET transistors to provide precision, high speed, and long hold times. A typical offset voltage of 2mV and gain error of 0.004% allow this sample and hold amplifier to be used in 12-bit systems. Dynamic performance can be optimized by proper selection of the external hold capacitor. Acquisition times can be as low as 4 μ s for small capacitors while hold step and droop errors can be held below 0.1mV and 30 μ V/sec respectively when using larger capacitors.

The LF398 is fixed at unity gain with 10¹⁰ Ω input impedance independent of sample/hold mode. The logic inputs are high impedance differential to allow easy interfacing to any logic family without ground loop problems. A separate offset adjust pin can be used to zero the offset voltage in either the sample or hold mode. Additionally, the hold capacitor can be driven with an external signal to provide precision level shifting or "differencing" operation. The device will operate over a wide supply voltage range from ± 5 V to ± 18 V with very little change in performance, and key parameters are specified over this full supply range.

Basic Sample and Hold



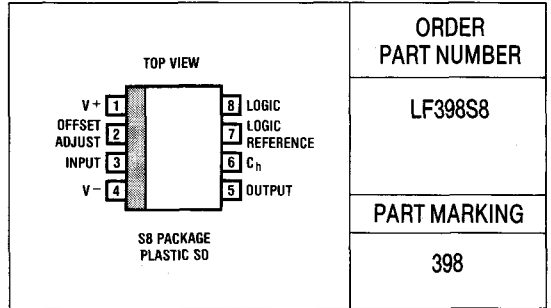
Acquisition Time



ABSOLUTE MAXIMUM RATINGS

Input Voltage Equal to Supply Voltage
 Logic to Logic Reference Differential
 Voltage (Note 2) + 30V, - 30V
 Output Short Circuit Duration Indefinite
 Hold Capacitor Short Circuit Duration 10 sec
 Lead Temperature (Soldering, 10 seconds) 300°C
 Supply Voltage ± 18V
 Power Dissipation (Package Limitation)
 (Note 1) 500mW
 Operating Temperature Range 0°C to 70°C
 Storage Temperature Range - 65°C to 150°C

PACKAGE/ORDER INFORMATION



ELECTRICAL CHARACTERISTICS (Note 3)

PARAMETER	CONDITIONS	LF398			UNITS	
		MIN	TYP	MAX		
Input Offset Voltage (Note 6)		●	2	7	mV	
Input Bias Current (Note 6)		●	10	50	nA	
Input Impedance			10 ¹⁰	100	Ω	
Gain Error	R _L = 10k	●	0.004	0.01	%	
Feedthrough Attenuation Ratio at 1kHz	C _h = 0.01μF		80	96	dB	
Output Impedance	"HOLD" Mode	●	0.5	4	Ω	
"HOLD" Step (Note 4)	C _h = 0.01μF, V _{OUT} = 0		0.5	2.5	mV	
Supply Current (Note 6)	T _i ≥ 25°C		4.5	6.5	mA	
Logic and Logic Reference Input Current			2	10	μA	
Leakage Current Into Hold Capacitor (Note 6)	"HOLD" Mode (Note 5)		30	200	pA	
Acquisition Time to 0.1%	ΔV _{OUT} = 10V, C _h = 1000pF		4		μS	
	C _h = 0.01μF		16		μS	
Hold Capacitor Charging Current	V _{IN} - V _{OUT} = 2V		5		mA	
Supply Voltage Rejection Ratio	V _{OUT} = 0		80	110	dB	
Differential Logic Threshold			0.8	1.4	2.4	V

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: T_i max for the LF398S8 is 100°C.

Note 2: The logic inputs are protected to ± 30V differential as long as the voltage on both pins does not exceed the supply voltage. For proper operation, however, both logic and logic reference pins must be at least 2V below the positive supply and one of these pins must be at least 3V above the negative supply.

Note 3: Unless otherwise noted, V_S = ± 15V, T_i = 25°C, - 11.5V ≤ V_{IN} ≤ + 11.5V, C_h = 0.01μF, R_L = 10kΩ and unit is in "sample" mode. Logic reference = 0V and logic voltage = 2.5V.

Note 4: The hold step is sensitive to stray capacitance coupling between input logic signals and the hold capacitor. 1pF, for instance, will create an additional 0.5mV step with a 5V logic swing and a 0.01μF hold capacitor. Magnitude of the hold step is inversely proportional to hold capacitor value.

Note 5: Leakage current is measured at a junction temperature of 25°C. The effects of junction temperature rise due to power dissipation or elevated ambient can be calculated by doubling the 25°C value for each 11°C increase in chip temperature. Leakage is guaranteed over full input signal range.

Note 6: These parameters are guaranteed over a supply voltage range of ± 5V to ± 18V.

SECTION 10— RS232 INTERFACE

SECTION 10—RS232/INTERFACE

INDEX	10-2
SELECTION GUIDE	10-3
PROPRIETARY PRODUCTS	
<i>LT1015, High Speed Dual Line Receiver</i>	13-6
<i>LT1030, Quad Low Power Line Driver</i>	10-5
<i>LT1030CS, Quad Low Power Line Driver</i>	10-9
<i>LT1032, Quad Low Power Line Driver</i>	10-11
<i>LT1039, RS232 Driver/Receiver with Shutdown</i>	10-19
<i>LTC1045, Programmable Micropower Hex Translator/Receiver/Driver</i>	10-27
<i>LT1080, Advanced Low Power 5V RS232 Dual Driver/Receiver</i>	10-43
<i>LT1081, Advanced Low Power 5V RS232 Dual Driver/Receiver</i>	10-43
<i>LT1080CS/LT1081CS, 5V Powered RS232 Driver/Receiver with Shutdown</i>	10-51
<i>LT1130, 5-Driver/5-Receiver RS232 Transceiver</i>	10-55
<i>LT1131, 5-Driver/4-Receiver RS232 Transceiver with Shutdown</i>	10-55
<i>LT1132, 5-Driver/3-Receiver RS232 Transceiver</i>	10-55
<i>LT1133, 3-Driver/5-Receiver RS232 Transceiver</i>	10-55
<i>LT1134, 4-Driver/4-Receiver RS232 Transceiver</i>	10-55
<i>LT1135, 5-Driver/3-Receiver RS232 Transceiver without Charge Pump</i>	10-55
<i>LT1136, 4-Driver/5-Receiver RS232 Transceiver with Shutdown</i>	10-55
<i>LT1137, 3-Driver/5-Receiver RS232 Transceiver with Shutdown</i>	10-55
<i>LT1138, 5-Driver/3-Receiver RS232 Transceiver with Shutdown</i>	10-55
<i>LT1139, 4-Driver/4-Receiver RS232 Transceiver with Shutdown</i>	10-55
<i>LT1140, 5-Driver/3-Receiver RS232 Transceiver without Charge Pump</i>	10-55
<i>LT1141, 3-Driver/5-Receiver RS232 Transceiver without Charge Pump</i>	10-55
<i>LT1180, Advanced Low Power 5V RS232 Dual Driver/Receiver with Small Capacitors</i>	10-67
<i>LT1181, Advanced Low Power 5V RS232 Dual Driver/Receiver with Small Capacitors</i>	10-67
<i>LT1280, Advanced Low Power 5V RS232 Dual Driver/Receiver</i>	10-75
<i>LT1281, Advanced Low Power 5V RS232 Dual Driver/Receiver</i>	10-75

MILITARY, COMMERCIAL AND INDUSTRIAL

PART NUMBER	DESCRIPTION	NUMBER OF DRIVERS	NUMBER OF RECEIVERS	MAXIMUM SUPPLY CURRENT	SHUTDOWN FEATURE	PACKAGES AVAILABLE	IMPORTANT FEATURES
LT1030C	Quad Micropower RS232 Line Driver	4	0	1mA	X	J, N, S	Quad RS232 Driver, Can be Strobed Off for Zero Supply Current. Supply Range from $\pm 5V$ to $\pm 15V$.
LT1032C, I, M	Quad Micropower RS232 Line Driver	4	0	1mA	X	J, N	Quad RS232 Driver. Can be Strobed Off for Zero Supply Current. Supply Range from $\pm 5V$ to $\pm 15V$.
LT1039C, I, M	Triple RS232 Driver/Receiver with Shutdown	3	3	15mA	X	J, N	Triple RS232 Driver/Receiver Includes Shutdown Feature. Bias Pin Allows One Receiver to Remain Active while the Rest of the Device is Shut Down. Rugged Bipolar Design.
LT1039C-16	Triple RS232 Driver/Receiver	3	3	15mA		J16, N16	16 Pin Version of LT1039 without Shutdown Feature. Pin-For-Pin Compatible with MC145406, Rugged Bipolar Design Less Subject to ESD Damage and Latchup.
LT1080C, I, M	+5V Powered RS232 Driver/Receiver with Shutdown	2	2	22mA	X	J, N, S	Dual RS232 Driver/Receiver with Built In $\pm 5V$ to $\pm 9V$ Power Converter. Shutdown Feature Allows Device to be Turned Off When Not Used, Saving Power.
LT1180C, I, M	+5V Powered RS232 Driver/Receiver with Shutdown	2	2	22mA	X	J, N, S	Dual RS232 Driver/Receiver with Built In $\pm 5V$ to $\pm 9V$ Power Converter. Shutdown Feature Allows Device to be Turned Off When Not Used, Saving Power. Uses smaller $0.1\mu F$ capacitors.
LT1081C, I, M	+5V Powered RS232 Driver/Receiver	2	2	22mA		J, N, S	16 Pin Version of LT1080 without Shutdown Feature. Pin-For-Pin Compatible with MAX-232, Rugged Bipolar Design Less Subject to ESD Damage and Latchup.
LT1181C, I, M	+5V Powered RS232 Driver/Receiver	2	2	22mA		J, N, S	16 Pin Version of LT1180 without Shutdown Feature. Pin-For-Pin Compatible with MAX-232, Rugged Bipolar Design Less Subject to ESD Damage and Latchup. Uses smaller $0.1\mu F$ Capacitors.
LTC1045C, M	Programmable Micropower Hex Level Translator/Receiver/Driver	0	6	4.5mA 100 μA **		J, N, S	Versatile Level Translator Performs Many Level Translation, Line Driver and Line Receiver Functions. Power Consumption is Programmable.
LT1130C, M	+5V Powered RS232 Transceiver	5	5	27mA		J, N, S	LT113X Product Family Offers Wide Array of Multiple Driver/Receiver Functions. All Devices (Except LT1135, LT1139, LT1140, LT1141) Have $\pm 5V$ to $\pm 9V$ Power Supply Converter On-Chip. All Outputs are Overload Protected and Do Not Allow Current Flow Back Into Power Supplies When Shut Down. The LT1135, LT1140 and LT1141 Do Not Have Onboard Voltage Converters and are Ideal for Low Power Applications with $\pm 12V$ Supplies Already Available. The LT1139 Has a $\pm 12V$ to $-9V$ Voltage Converter and is Suited for Low Power Applications where $\pm 12V$ and $\pm 5V$ Supplies are Available.
LT1131C, M	+5V Powered RS232 Transceiver	5	4	27mA	X	J, N, S	
LT1132C, M	+5V Powered RS232 Transceiver	5	3	27mA		J, N, S	
LT1133C, M	+5V Powered RS232 Transceiver	3	5	27mA		J, N, S	
LT1134C, M	+5V Powered RS232 Transceiver	4	4	27mA		J, N, S	
LT1135C, M	+5V Powered RS232 Transceiver	5	3	*		J, N, S	
LT1136C, M	+5V Powered RS232 Transceiver	4	5	27mA	X	J, N, S	
LT1137C, M	+5V Powered RS232 Transceiver	3	5	27mA	X	J, N, S	
LT1138C, M	+5V Powered RS232 Transceiver	5	3	27mA	X	J, N, S	
LT1139C, M	+5V Powered RS232 Transceiver	4	4	*	X	J, N, S	
LT1140C, M	+5V Powered RS232 Transceiver	5	3	*	X	J, N, S	
LT1141C, M	+5V Powered RS232 Transceiver	3	5	*	X	J, N, S	

* Not yet determined at time of printing. Will be substantially below 27mA. Consult factory for actual values.

** Programmable down to 100 μA .

REFER TO TABLE OF CONTENTS FOR REVISED DATA LOCATION

NOTES

FEATURES

- Low Operating Voltage $\pm 5V$ to $\pm 15V$
- $500\mu A$ Supply Current
- Zero Supply Current when Shut Down
- Outputs Can Be Driven $\pm 30V$
- Output "Open" when Off (3-State)
- 10mA Output Drive
- Pinout Similar to 1488*
- Output of Several Devices can be Paralleled
- Available in SO Package

APPLICATIONS

- RS232 Driver
- Micropower Interface
- Level Translator

* Check compatibility, some pins different

DESCRIPTION

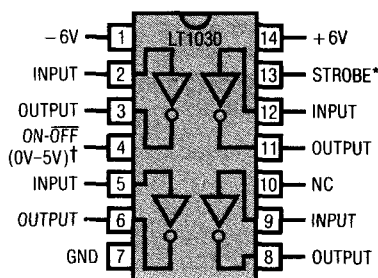
The LT1030 is an RS232 line driver that operates over a $\pm 5V$ to $\pm 15V$ range on low supply current and can be shut down to zero supply current. Outputs are fully protected from externally applied voltages of $\pm 30V$ by current limiting. Since the output swings to within 200mV of the positive supply and 1V of the negative supply, power supply needs are minimized.

A major advantage of the LT1030 is the high impedance output state when off or powered down, which allows several different drivers on the same bus.

Our RS232 product line includes other high-performance devices. The LT1039 is a triple low-power driver/receiver with shutdown that can be powered from a 5V supply. The LT1080 is a 5V powered dual driver/receiver with on-chip $\pm 9V$ power generator, and shutdown.

TYPICAL APPLICATION

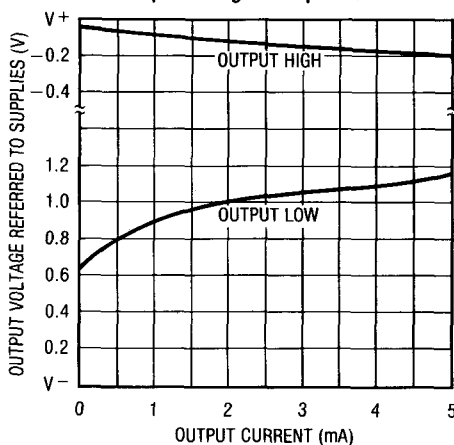
RS232 Line Driver



* NO CONNECTION NEEDED WHEN NOT USED.

† 5V = ON.

Output Swing vs Output Current



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	± 15V
Logic Input Pins	V ⁻ to 25V
On-Off Pin	GND to 12V
Output (Forced)	V ⁻ + 30V, V ⁺ - 30V
Short Circuit Duration (to ± 30V)	Indefinite
Operating Temperature Range	
LT1030C	0°C to 70°C
Guaranteed Functional by Design	- 25°C to 85°C
Storage Temperature	- 65°C to 150°C
Lead Temperature (Soldering, 10 sec)	300°C

PACKAGE/ORDER INFORMATION

J PACKAGE
14-LEAD CERAMIC DIP

S PACKAGE
14-LEAD PLASTIC S
(.150" WIDE)

N PACKAGE
14-LEAD PLASTIC DIP

ORDER PART NUMBER

LT1030CJ
LT1030CN
LT1030CS
FOR MILITARY APPLICATIONS
USE LT1032MJ

ELECTRICAL CHARACTERISTICS (Supply Voltage = ± 5V to ± 15V)

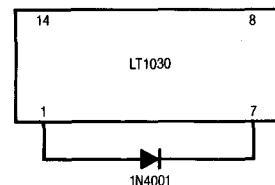
PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Current	V _{ON-OFF} ≥ 2.4V, I _{OUT} = 0, All Outputs Low	●		500	1000	μA
Power Supply Leakage Current	V _{ON-OFF} ≤ 0.4V V _{ON-OFF} ≤ 0.1V	●		10	150	μA
Output Voltage Swing	Load = 2mA	Positive	V ⁺ - 0.3V	V ⁺ - 0.1V		V
		Negative		V ⁻ + 0.9V	V ⁻ + 1.4V	V
Output Current	V _{SUPPLY} ± 5V to ± 15V		5	12		mA
Output Overload Voltage (Forced)	Operating or Shutdown	●	V ⁺ - 30V		V ⁻ + 30V	V
Output Current	Shutdown V _{OUT} = ± 30V			2	100	μA
Input Overload Voltage (Forced)	Operating or Shutdown	●	V ⁻		15	V
Logic Input Levels	Low Input (V _{OUT} = High)	●		1.4	0.8	V
	High Input (V _{OUT} = Low)	●	2	1.4		V
Logic Input Current	V _{IN} > 2.0V			2	20	μA
	V _{IN} < 0.8V			10	20	μA
On-Off Pin Current	0 ≤ V _{IN} ≤ 5V	●	- 10	30	65	μA
Slew Rate			4	15	30	V/μS

The ● denotes specifications which apply over the operating temperature range.

Note 1: 3V applied to the strobe pin will force all outputs low. Strobe pin input impedance is about 2k to ground. Leave open when not used.

PIN FUNCTIONS

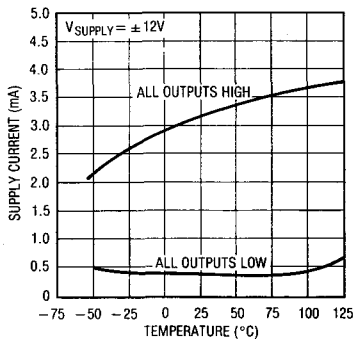
PIN	FUNCTION	COMMENT
1	Minus Supply	Operates - 2V to - 15V
2,5,9,12	Logic Input	Operates properly on TTL or CMOS levels. Output valid from (V ⁻ + 2V) ≤ V _{IN} ≤ 15V. Connect to 5V when not used.
3,6,8,11	Output	Line drive output.
4	On-Off	Shuts down entire circuit. Cannot be left open. For "normally on" operation, connect between 5V-10V.
7	Ground	Ground must be more positive than V ⁻
13	Strobe	Forces all outputs low. Drive with 3V.
14		Positive supply 5V to 15V.



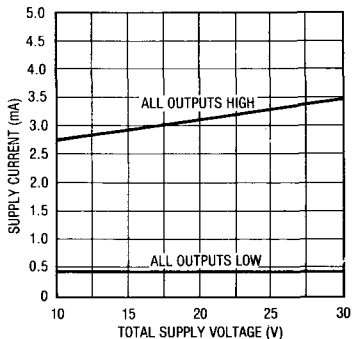
Note: As with other bipolar ICs, forward biasing the substrate diode can cause problems. The LT1030 will draw high current from V⁺ to ground if the V⁻ pin is open circuited or pulled above ground. If this is possible, connecting a diode from V⁻ to ground will prevent the high current state. Any low cost diode can be used.

TYPICAL PERFORMANCE CHARACTERISTICS

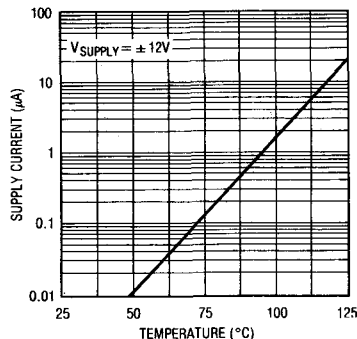
On Supply Current vs Temperature



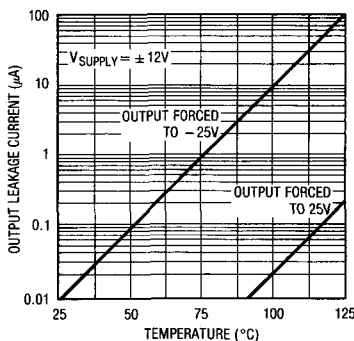
On Supply Current vs Supply Voltage



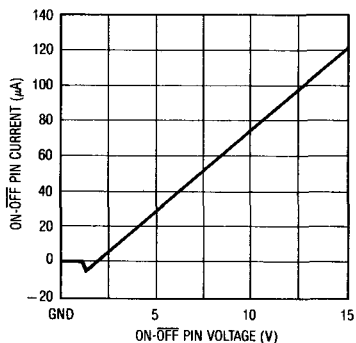
Off Supply Current vs Temperature



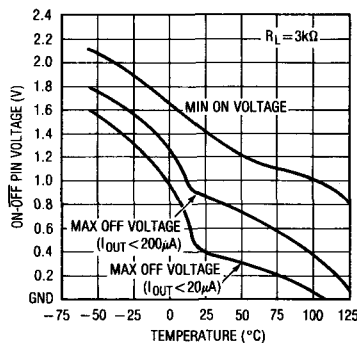
Off Output Leakage vs Temperature



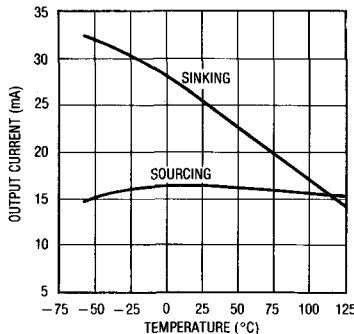
On-Off Pin Current vs Voltage



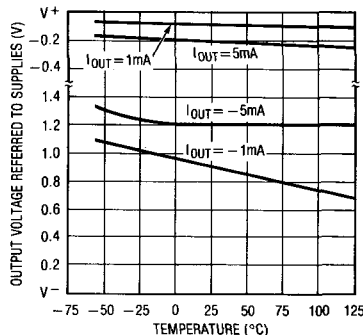
Shutdown Voltage vs Temperature



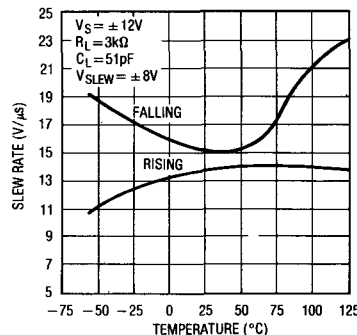
Current Limit vs Temperature



Output Swing vs Temperature



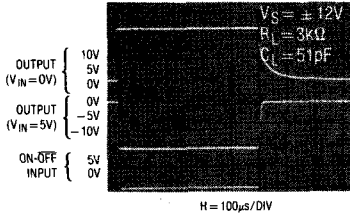
Slew Rate vs Temperature



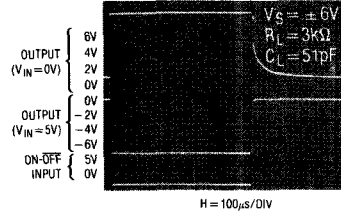
10

TYPICAL PERFORMANCE CHARACTERISTICS

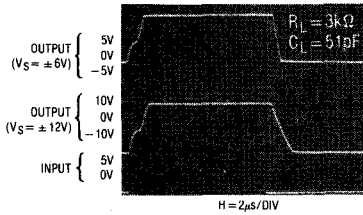
On-Off Response Time



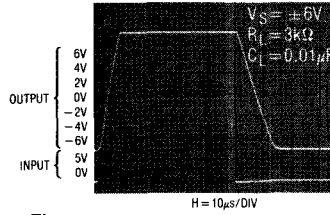
On-Off Response Time



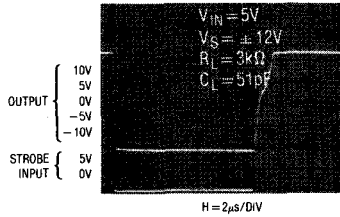
Output Waveform



Output Waveform Driving Capacitive Load

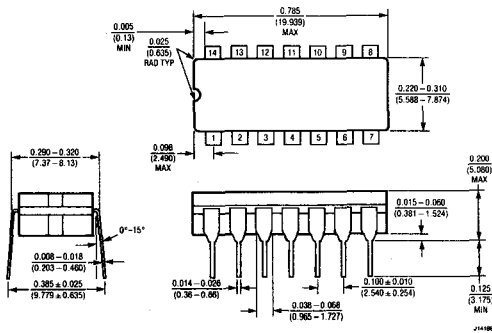


Strobe Pin Response Time



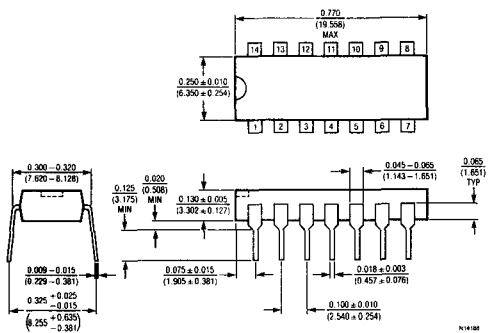
PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

J Package
14-Lead Hermetic DIP



T_{jmax}	Θ_{JA}
150°C	80°C/W

N Package
14-Lead Plastic



T_{jmax}	Θ_{JA}
110°C	130°C/W

FEATURES

- Low Operating Voltage $\pm 5V$ to $\pm 15V$
- 500 μA Supply Current
- Zero Supply Current when Shut Down
- Outputs can be Driven $\pm 30V$
- Output "Open" when Off (3-State)
- 10mA Output Drive
- Pin Compatible with 1488
- Output of Several Devices can be Paralleled

APPLICATIONS

- RS232 Driver
- Micropower Interface
- Level Translator

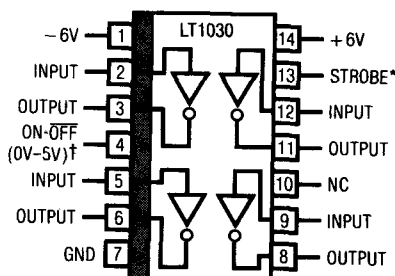
DESCRIPTION

The LT1030 is an RS232 line driver that operates over a $\pm 5V$ to $\pm 15V$ range on low supply current and can be shut down to zero supply current. Outputs are fully protected from externally applied voltages of $\pm 30V$ by current limiting. Since the output swings to within 200mV of the positive supply and 1V of the negative supply, power supply needs are minimized.

A major advantage of the LT1030 is the high impedance output state when off or powered down, which allows several different drivers on the same bus.

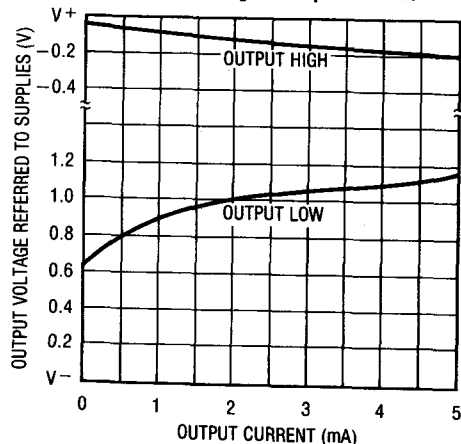
TYPICAL APPLICATION

RS232 Line Driver



*NO CONNECTION NEEDED WHEN NOT USED.
 †5V = ON.

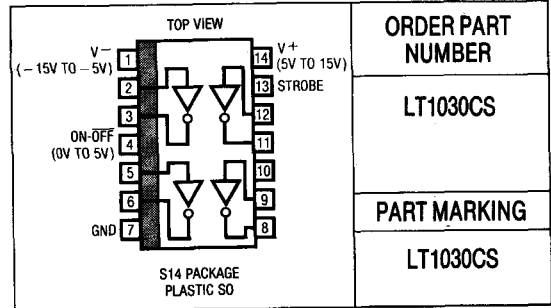
Output Swing vs Output Current



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	± 15V
Logic Input Pins	V ⁻ to 25V
On-Off Pin	GND to 12V
Output (Forced)	V ⁻ + 30V, V ⁺ - 30V
Short Circuit Duration (to ± 30V)	Indefinite
Operating Temperature Range	
LT1030C	0°C to 70°C
Guaranteed Functional by Design	-25°C to 85°C
Storage Temperature	-65°C to 150°C
Lead Temperature (Soldering, 10 sec)	300°C

PACKAGE/ORDER INFORMATION



ELECTRICAL CHARACTERISTICS (Supply Voltage = ± 5V to ± 15V)

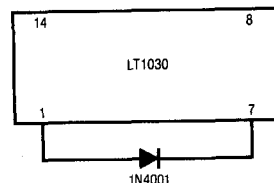
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	V _{ON-OFF} ≥ 2.4V, I _{OUT} = 0, All Outputs Low	●	500	1000	μA
Power Supply Leakage Current	V _{ON-OFF} ≤ 0.4V V _{ON-OFF} ≤ 0.1V	●	1 10	10 150	μA
Output Voltage Swing	Load = 2mA				
	Positive	V ⁺ - 0.3V	V ⁺ - 0.1V		V
	Negative		V ⁻ + 0.9V	V ⁻ + 1.4V	V
Output Current	V _{SUPPLY} ± 5V to ± 15V	5	12		mA
Output Overload Voltage (Forced)	Operating or Shutdown	●	V ⁺ - 30V	V ⁻ + 30V	V
Output Current	Shutdown V _{OUT} = ± 30V		2	100	μA
Input Overload Voltage (Forced)	Operating or Shutdown	●	V ⁻	15	V
Logic Input Levels	Low Input (V _{OUT} = High)	●	1.4	0.8	V
	High Input (V _{OUT} = Low)	●	2	1.4	V
Logic Input Current	V _{IN} > 2.0V		2	20	μA
	V _{IN} < 0.8V		10	20	μA
On-Off Pin Current	0 ≤ V _{IN} ≤ 5V	●	-10	30	μA
Slew Rate			4	15	V/μS

The ● denotes specifications which apply over the operating temperature range.

Note 1: 3V applied to the strobe pin will force all outputs low. Strobe pin input impedance is about 2k to ground. Leave open when not used.

PIN FUNCTIONS

PIN	FUNCTION	COMMENT
1	Minus Supply	Operates -2V to -15V
2,5,9,12	Logic Input	Operates properly on TTL or CMOS levels. Output valid from (V ⁻ + 2V) ≤ V _{IN} ≤ 15V. Connect to 5V when not used.
3,6,8,11	Output	Line drive output.
4	On-Off	Shuts down entire circuit. Cannot be left open. For "normally on" operation, connect between 5V-10V.
7	Ground	Ground must be more positive than V ⁻
13	Strobe	Forces all outputs low. Drive with 3V.
14		Positive supply 5V to 15V.



Note: As with other bipolar ICs, forward biasing the substrate diode can cause problems. The LT1030 will draw high current from V⁺ to ground if the V⁻ pin is open circuited or pulled above ground. If this is possible, connecting a diode from V⁻ to ground will prevent the high current state. Any low cost diode can be used.

FEATURES

- Low Operating Voltage $\pm 5V$ to $\pm 15V$
- $500\mu A$ Supply Current
- Zero Supply Current when Shut Down
- Outputs Can Be Driven $\pm 30V$
- Thermal Limiting
- Output "Open" when Off (Three-State)
- 10mA Output Drive
- Pinout Similar to 1488 (See Diagram)*

APPLICATIONS

- RS232 Driver
- Power Supply Inverter
- Micropower Interface
- Level Translator

* Check compatibility, some pins different

DESCRIPTION

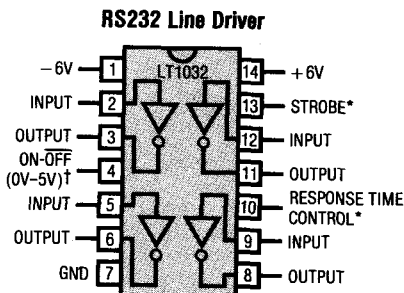
The LT1032 is a RS232 and RS423 line driver that operates over a $\pm 5V$ to $\pm 15V$ range on low supply current and can be shut down to zero supply current. Outputs are fully protected from externally applied voltages of $\pm 30V$ by both current and thermal limiting. Since the output swings to within 200mV of the positive supply and 600mV of the negative supply, power supply needs are minimized.

Also included is a strobe pin to force all outputs low independent of input or shutdown conditions. Further, slew rate can be adjusted with a resistor connected to the supply.

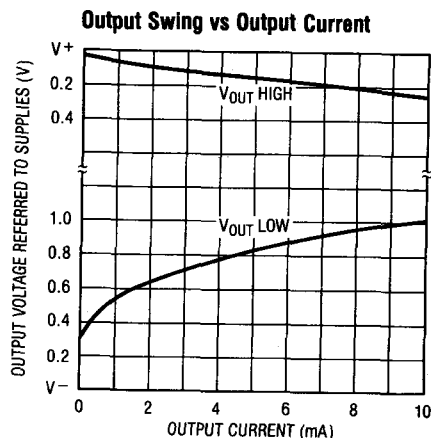
A major advantage of the LT1032 is the high impedance output state when off or powered down.

For applications requiring dual or triple RS232 driver/receiver devices, see the LT1080 (dual) or LT1039 (triple) datasheets.

TYPICAL APPLICATION



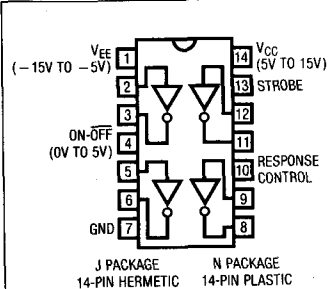
* NO CONNECTION NEEDED WHEN NOT USED.
[†] 5V = ON.



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	± 15V
Logic Input Pins	V ⁻ to 25V
On-Off Pin	GND to 15V
Output (Forced)	V ⁻ + 30V, V ⁺ - 30V
Response Pin	± 6V
Short Circuit Duration (to ± 30V)	Indefinite
Operating Temperature Range	
LT1032M	- 55°C to 125°C
LT1032C	0°C to 70°C
Guaranteed Functional by Design	- 25°C to 85°C
Lead Temperature (Soldering, 10 sec)	300°C

PACKAGE/ORDER INFORMATION



ORDER PART NUMBER

LT1032MJ
LT1032CJ
LT1032CN

ELECTRICAL CHARACTERISTICS

(Supply Voltage = ± 5V to ± 15V)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	V _{ON-OFF} ≥ 2.4V, I _{OUT} = 0, All Outputs Low	●	500	1000	μA
Power Supply Leakage Current	V _{ON-OFF} ≤ 0.4V	●	1	10	μA
	V _{ON-OFF} ≤ 0.1V, T _A = 125°C	●	10	50	μA
Output Voltage Swing	Load = 2mA	Positive	V ⁺ - 0.3V	V ⁺ - 0.1V	V
		Negative		V ⁻ + 0.7V	V ⁻ + 0.9V
Output Current	V _{SUPPLY} ± 5V to ± 15V	10	22		mA
Output Overload Voltage (Forced)	Operating or Shutdown	●	V ⁺ - 30V	V ⁻ + 30V	V
Output Current	Shutdown V _{OUT} = ± 30V		2	100	μA
Input Overload Voltage (Forced)	Operating or Shutdown	●	V ⁻	30V	V
Logic Input Levels	Low Input (V _{OUT} = High)	●		0.8	V
	High Input (V _{OUT} = Low)	●	2	1.4	V
Logic Input Current	V _{IN} > 2.0V		2	20	μA
	V _{IN} < 0.8V		10	20	μA
On-Off Pin Current	0 ≤ V _{IN} ≤ 5V	●	- 10	3	50
Slew Rate	I _{RESPONSE} = 0		4	15	30
Change in Slew Rate (Note 2)	I _{RESPONSE} = + 50μA			+ 50	%
	I _{RESPONSE} = - 50μA			- 50	%
Response Pin Leakage	V _{SUPPLY} = ± 6V, V _{ON/OFF} ≤ 0.4V, V _{RESPONSE} = ± 6V		1		μA

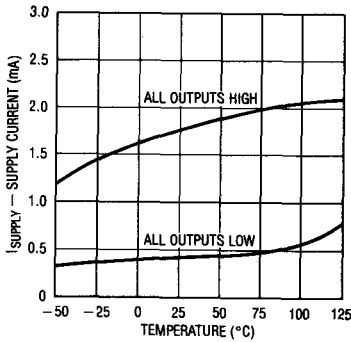
The ● denotes specifications which apply over the operating temperature range.

Note 1: 3V applied to the strobe pin will force all outputs low. Strobe pin input impedance is about 2k to ground. Leave open when not used.

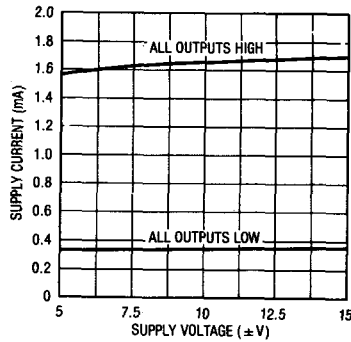
Note 2: Response can be changed by connecting a resistor to the supply. For supplies less than ± 6V this current is disconnected when shut down. Leave open when not used.

TYPICAL PERFORMANCE CHARACTERISTICS

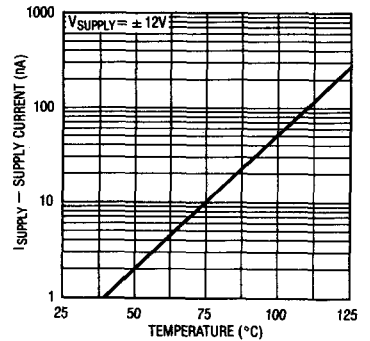
On Supply Current vs Temperature



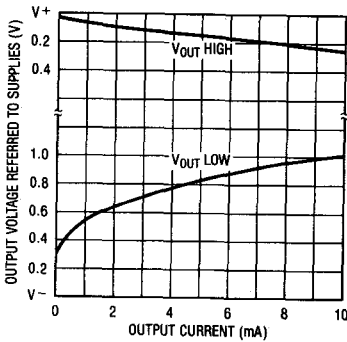
Supply Current vs Supply Voltage



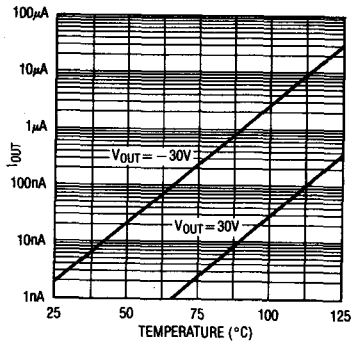
Off Supply Current vs Temperature



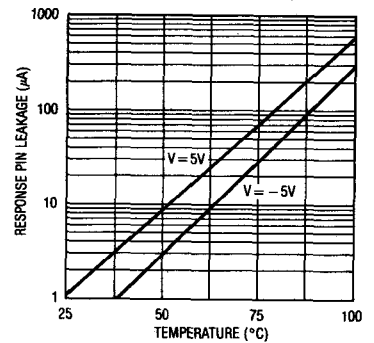
Output Swing vs Output Current



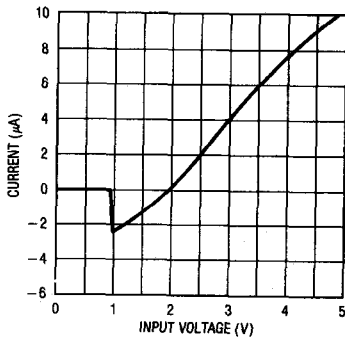
Output Leakage vs Temperature



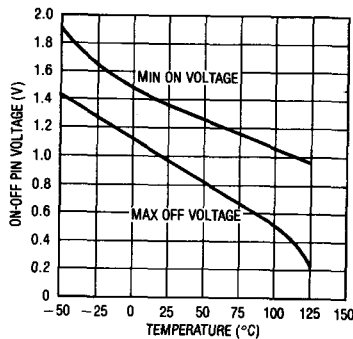
Response Pin Leakage vs Temperature (Device Off)



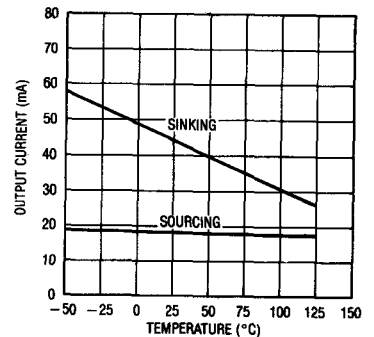
On-Off Pin Current vs Voltage



Shutdown Pin Voltage vs Temperature



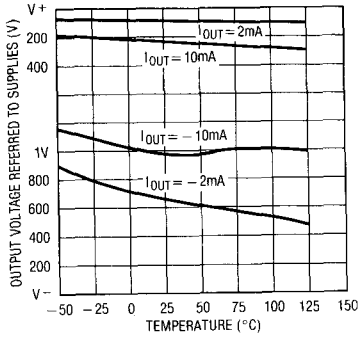
Current Limit vs Temperature



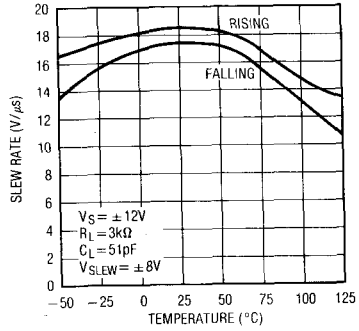
10

TYPICAL PERFORMANCE CHARACTERISTICS

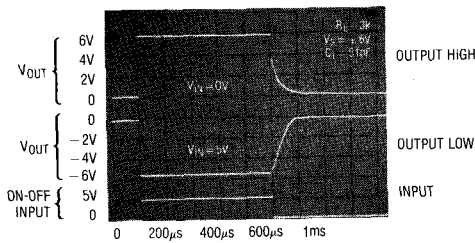
Output Swing vs Temperature



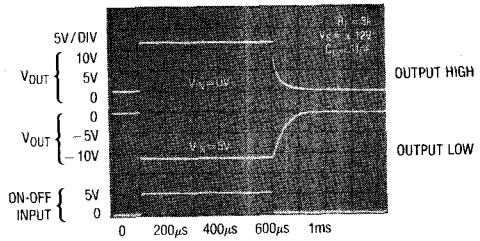
Slew Rate vs Temperature



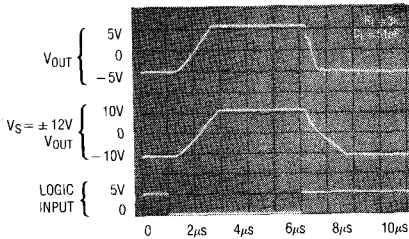
On-Off Response Time



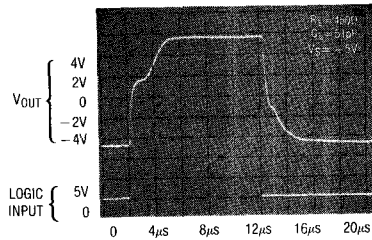
On-Off Response Time



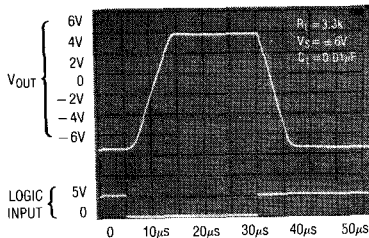
Output Waveform



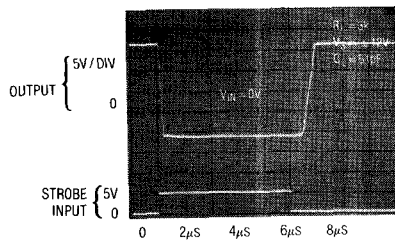
Output Waveform



Output Waveform Driving Capacitive Load



Strobe Pin Response



APPLICATIONS INFORMATION

Application Hints

The LT1032 is exceptionally easy to use when compared to older drivers. Operating supply voltage can be as low as $\pm 3V$ or as high as $\pm 15V$. Input levels are referred to ground.

The logic inputs are internally set at TTL levels. Outputs are valid for input voltages from 1V above V^- to 25V. Driving the logic inputs to V^- turns off the output stage. The "on-off" control completely turns off all supply current of the LT1032. The levels required to drive the device on or off are set by internal emitter-base voltages. Since the current into the "on-off" pin is so low, TTL or CMOS drivers have no problem controlling the device.

The strobe pin is not fully logic compatible. The impedance of the strobe pin is about $2k\Omega$ to ground. Driving the strobe pin positive forces the output stages low—even if the device is shut off. Under worst-case conditions, 3V minimum at 2mA are needed driving the strobe pin to insure strobing.

The response pin can be used to make some adjustment in slew rate. A resistor can be connected between the response pin and the power supplies to drive $50\mu A$ to $100\mu A$ into the pin. The response pin is a low impedance point operating at about 0.75V above ground. For supply voltage up to $\pm 6V$, current is turned off when the device is turned off. For higher supply voltages, a zener should be connected in series with the resistor to limit the voltage applied to the response pin to 6V. Also, for temperatures above $100^\circ C$, using the response pin is not recommended. The leakage current into the response pin at high temperatures is excessive.

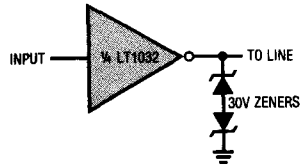
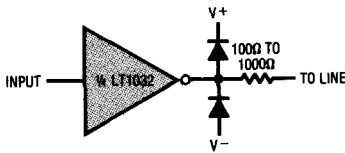
Outputs are well protected against shorts or externally applied voltage. Tested limits are $\pm 30V$, but the device can withstand external voltages up to the breakdown of the transistors (typically about 50V). The LT1032 is usually immune to ESD up to 2500V on the outputs with no damage (limit of LTC tester).

PIN FUNCTION

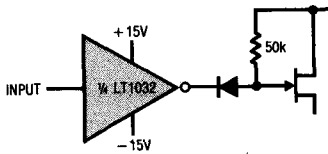
PIN	FUNCTION	COMMENT
1	Minus Supply	Operates $-2V$ to $-15V$
2,5,9,12	Logic Input	Operates properly on TTL or CMOS levels. Output valid from $(V^- + 2V) \leq V_{IN} \leq 15V$. Connect to ground when not used.
3,6,8,11	Output	Line drive output.
4	On-Off	Shuts down entire circuit. Cannot be left open. For "normally on" operation, connect to V^+ .
7	Ground	Ground must be more positive than V^-
10	Response Control	Allows limited change of slew rate. Leave open when not used.
13	Strobe	Forces all outputs low. Drive with 3V.
14	Positive Supply	Operates 5V to 15V

TYPICAL APPLICATIONS

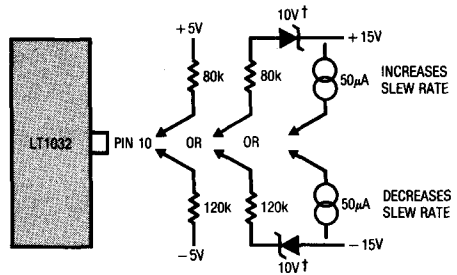
Protecting Against More than $\pm 30V$ Output Overload



FET Driver

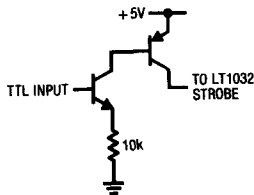


Slew Rate Adjustment*

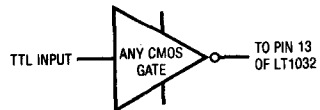


*ABOUT 4V/ μ S CHANGE
 †ZENERS PREVENT LEAKAGE DURING SHUT DOWN

TTL/CMOS Compatible Strobe

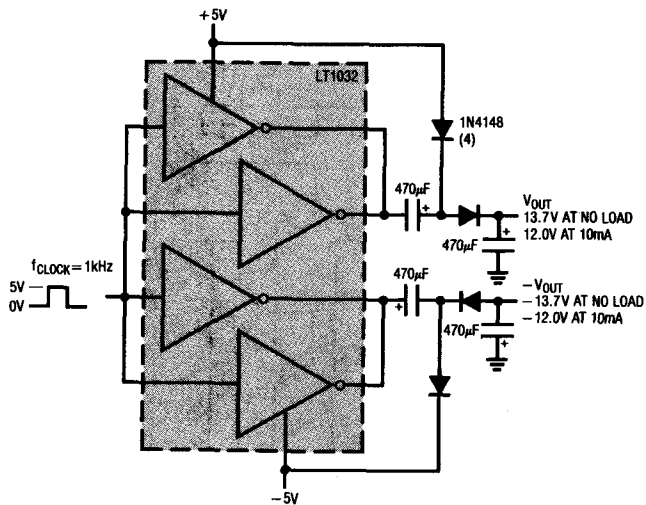


Strobing with CMOS

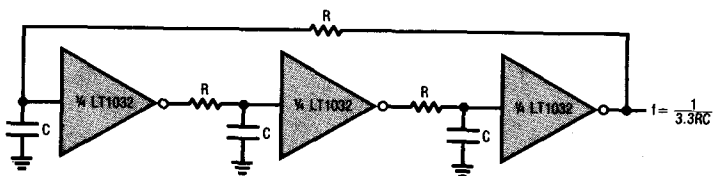


TYPICAL APPLICATIONS

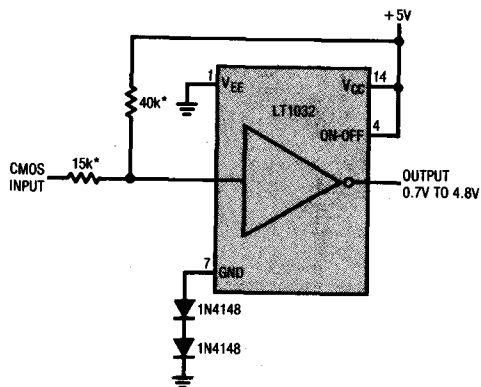
± 5V to ± 15V Voltage Multiplier



Phase Shift Oscillator

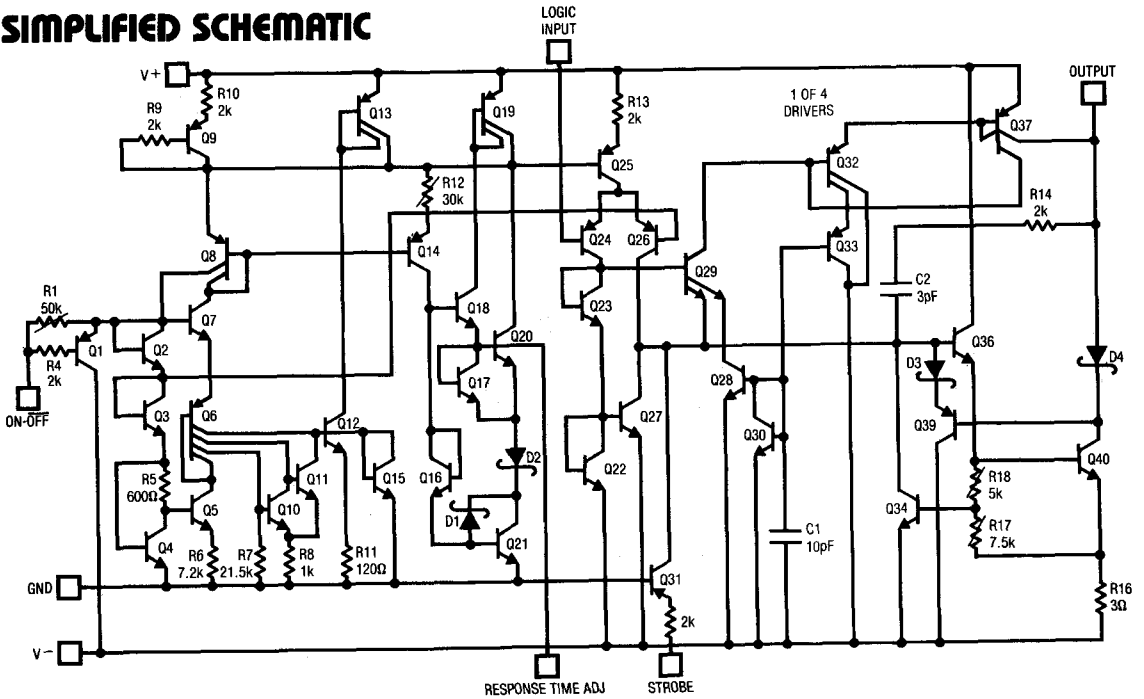


Operating from a Single 5V Supply



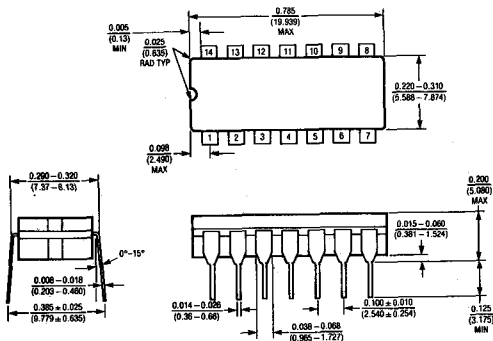
*LEVEL SHIFTING RESISTORS NEEDED FOR EACH INPUT

SIMPLIFIED SCHEMATIC

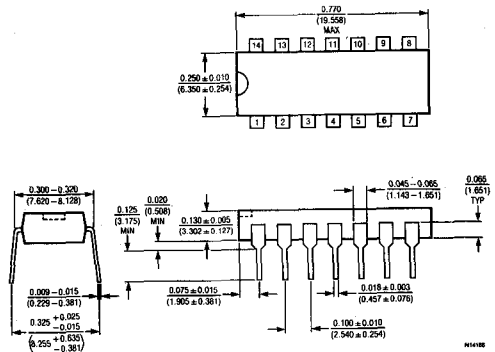


PACKAGE DESCRIPTION

**J Package
14-Lead Ceramic DIP**



**N Package
14-Lead Plastic DIP**



	T _{max}	Θ _J A	Θ _J C
LT1032MJ	150°C	100°C/W	60°C/W
LT1032CJ	85°C	100°C/W	60°C/W
LT1032CN	85°C	100°C/W	60°C/W

FEATURES

- Operates from $\pm 5V$ to $\pm 15V$ Supplies
- Fully Protected Against Overload
- Outputs can be Driven $\pm 30V$ without Damage
- Three-State Outputs; Outputs Open when Off
- Bipolar Circuit—No Latch Up
- $\pm 30V$ Input Range
- Triple Driver/Receiver
- No Supply Current in Shutdown
- $30k\Omega$ Input Impedance
- Meets All RS232 Specifications
- 16 Pin Version—Pin Compatible with MC145406
- Available in SO Package

APPLICATIONS

- RS232 Interface
- Terminals
- Modems

DESCRIPTION

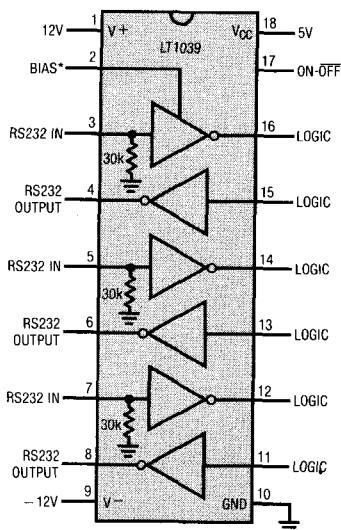
The LT1039 is a triple RS232 driver/receiver which includes SHUTDOWN. Each receiver will accept up to $\pm 30V$ input and can drive either TTL or CMOS logic. The RS232 drivers accept TTL logic inputs and output RS232 voltage levels. The outputs are fully protected against overload and can be shorted to ground or up to $\pm 30V$ without damage to the drivers. Additionally, when the system is shut down or power is off, the outputs are in a high impedance state allowing data line sharing. Bipolar circuitry makes this driver/receiver exceptionally rugged against overloads or ESD damage.

A bias pin allows one receiver to be kept on while the rest of the part is shut down.

The 1039 is also available in the 16 pin version, without shutdown or bias pin functions.

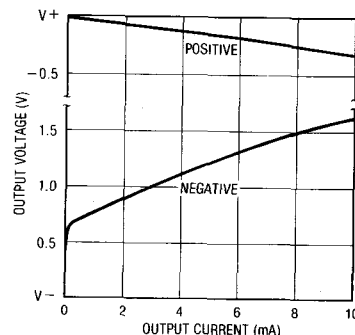
For applications requiring operation from a single 5V supply, see LT1080/81 datasheet.

TYPICAL APPLICATION



*BIAS PIN USED TO KEEP THE RECEIVER ON WHILE IN SHUTDOWN.

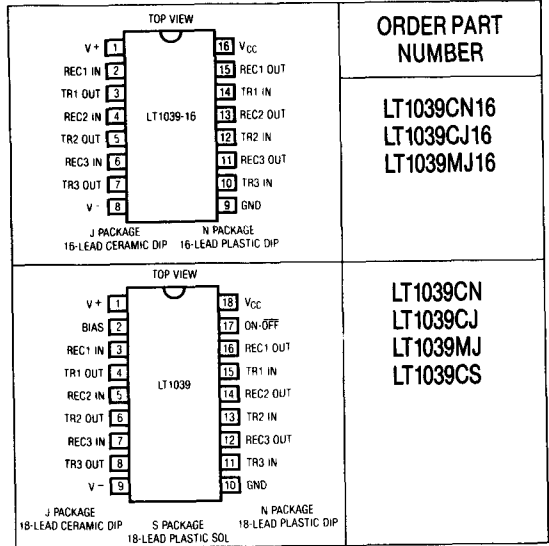
Driver Output Swing



ABSOLUTE MAXIMUM RATINGS

Supply Voltage
 Driver (V^+ , V^-) $\pm 16V$
 Receiver (V_{CC}) $7V$
 Logic Inputs V^- to $25V$
 Receiver Inputs $\pm 30V$
 On-Off Input GND to $12V$
 Driver Outputs $V^- + 30V$ to $V^+ - 30V$
 Short Circuit Duration Indefinite
 Operating Temperature Range
 LT1039M $-55^\circ C$ to $125^\circ C$
 LT1039C $0^\circ C$ to $70^\circ C$
 Guaranteed Functional by Design $-25^\circ C$ to $85^\circ C$
 Lead Temperature (Soldering, 10 sec.) $300^\circ C$

PACKAGE/ORDER INFORMATION



ORDER PART NUMBER

LT1039CN16
 LT1039CJ16
 LT1039MJ16

LT1039CN
 LT1039CJ
 LT1039MJ
 LT1039CS

ELECTRICAL CHARACTERISTICS

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	
Driver $V^+ = 12V$; $V^- = -12V$; $V_{ON-OFF} = 2.5V$						
Output Voltage Swing	Load = 3k to Ground	Positive Negative	$V^+ - 0.4$ $V^- + 1.5$	$V^+ - 0.1$ $V^- + 1$	V V	
Logic Input Voltage Levels	Input Low Level ($V_{OUT} = High$) Input High Level ($V_{OUT} = Low$)	● ●	2.0	1.4 1.4	V V	
Logic Input Current	$V_{IN} \geq 2.0V$ $V_{IN} \leq 0.8V$			1 5	20 20	μA μA
Output Short Circuit Current	Sourcing Current, $V_{OUT} = 0V$ Sinking Current, $V_{OUT} = 0V$		5 -5	15 -15	mA mA	
Output Leakage Current	SHUTDOWN (Notes 1 and 2); $V_{OUT} = \pm 18V$, $V_{IN} = 0$	●		10 (25°C)	200	μA
Supply Leakage Current	SHUTDOWN (Note 1)	●		1 (25°C)	100	μA
Slew Rate	$R_L = 3k\Omega$; $C_L = 51pF$		4	15	30	V/ μs
Supply Current	$V_{OUT} = Low$			4	8	mA
Receiver $V_{CC} = 5V$; $V_{ON-OFF} = 2.5V$						
Input Voltage Thresholds	Input Low ($V_{OUT} = High$) Input High ($V_{OUT} = Low$)	● ●	0.5	1.3 1.7	2.8	V V
Hysteresis		●	0.1	0.4	1.0	V
Input Resistance		●		30		k Ω
Output Voltage	Output Low, $I_{OUT} = -1.6mA$ Output High, $I_{OUT} = 160\mu A$	● ●	3.5	0.4 4.8	0.5	V V
Output Short Circuit Current	Sinking Current, $V_{OUT} = V_{CC}$ Sourcing Current, $V_{OUT} = 0V$ (Note 3)	● ●	-10 0.5	1		mA mA
Output Leakage Current	SHUTDOWN (Note 1); $0V \leq V_{OUT} \leq V_{CC}$, $V_{IN} = 0$	●		1	10	μA
Supply Current		●		4	7	mA

ELECTRICAL CHARACTERISTICS

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Leakage Current	SHUTDOWN (Note 1)	●		1 (25°C)	100	μA
On-Off Pin Current	$0V \leq V_{ON-OFF} \leq 5V$	●	-15		80	μA

The ● denotes specifications which apply over the operating temperature range.

Note 1: $V_{ON-OFF} = 0.4V$ for $-55^{\circ}C \leq T_A \leq 100^{\circ}C$, and $V_{ON-OFF} = 0.2V$ for $100^{\circ}C \leq T_A \leq 125^{\circ}C$. Does not apply to LT1039-16 part.

Note 2: For $T_A \geq 100^{\circ}C$, leakage current is 350μA max.

Note 3: For $T_A \leq -25^{\circ}C$, output source current is 0.4 mA.

PIN FUNCTIONS (Pin numbers listed are for 18 pin device).

V+, **V-** (Pins 1, 9): Driver supply pins. Supply current drops to zero in SHUTDOWN mode. Driver outputs are in a high impedance state when $V+$ and $V- = 0V$.

V_{CC} (Pin 18): 5V power for receivers.

GND (Pin 10): Ground pin.

TR IN (Pins 11, 13, 15): RS232 driver input pins. Inputs are TTL/CMOS compatible. Inputs should not be allowed to float. Tie unused inputs to V_{CC} .

TR OUT (Pins 4, 6, 8): Driver outputs with RS232 voltage levels. Outputs are in a high impedance state when in the SHUTDOWN mode or when power is off ($V+$ and $V- = 0V$) to allow data line sharing. Outputs are fully short circuit protected from $V- + 30V$ to $V+ - 30V$ with power on, off, or in the SHUTDOWN mode. Typical output breakdowns are greater than $\pm 45V$ and higher applied voltages will not damage the device if moderately current limited.

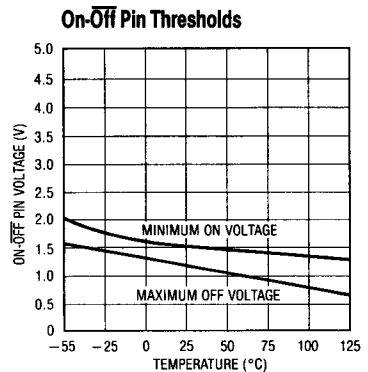
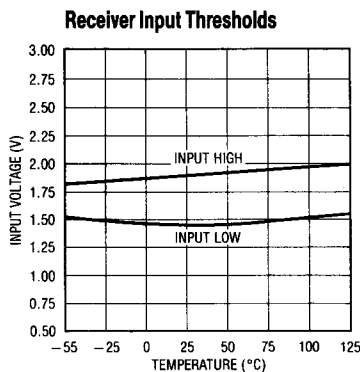
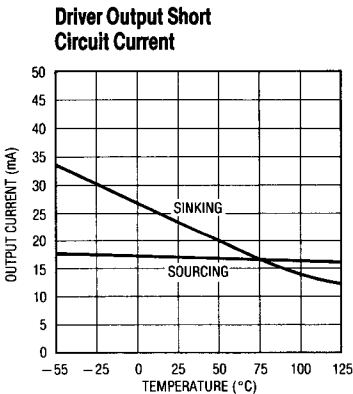
REC IN (Pins 3, 5, 7): Receiver input pins. Accepts RS232 voltage levels ($\pm 30V$) and has 0.4V of hysteresis to provide noise immunity. Input impedance is nominally 30kΩ.

REC OUT (Pins 12, 14, 16): Receiver outputs with TTL/CMOS voltage levels. Outputs are in a high impedance state when in the SHUTDOWN mode to allow data line sharing. Outputs are fully short circuit protected to ground or V_{CC} with power on, off, or in the SHUTDOWN mode.

ON-OFF (Pin 17): Controls the operation mode of the LT1039 and is TTL/CMOS compatible. A logic low puts the device in the SHUTDOWN mode which reduces input supply current to zero and places both driver and receiver outputs in a high impedance state.

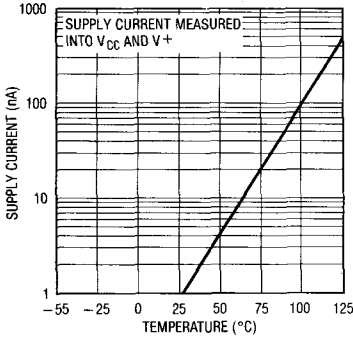
BIAS (Pin 2): Keeps receiver 1 on while the LT1039 is in the SHUTDOWN mode. Leave BIAS pin open when not in use. See Application Hints for proper use.

TYPICAL PERFORMANCE CHARACTERISTICS

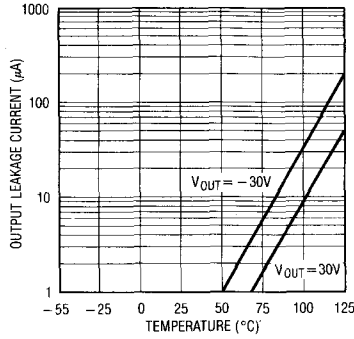


TYPICAL PERFORMANCE CHARACTERISTICS

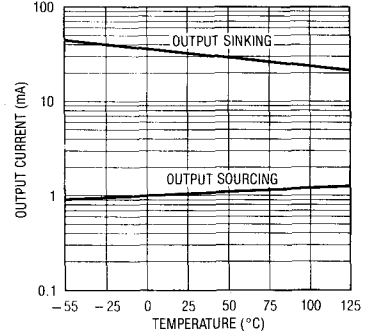
Supply Current in SHUTDOWN



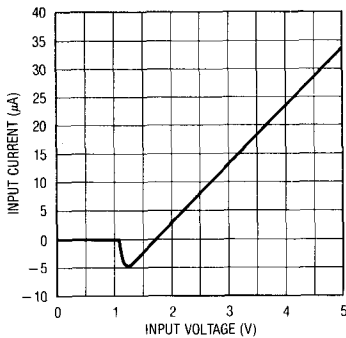
Driver Output Leakage in SHUTDOWN



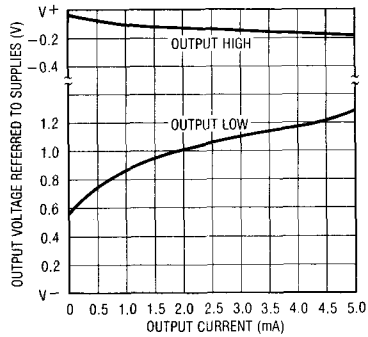
Receiver Output Short Circuit Current



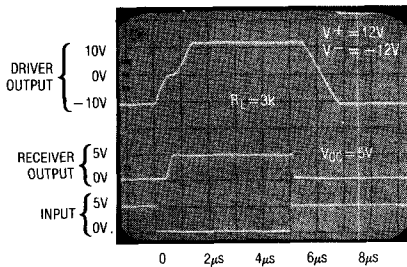
On-Off Pin Current vs Voltage



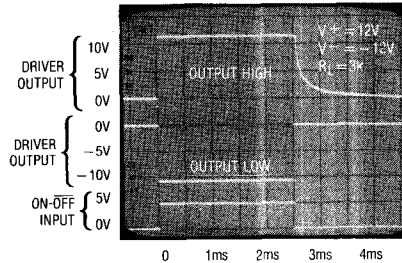
Driver Output Swing vs Current



Output Waveforms

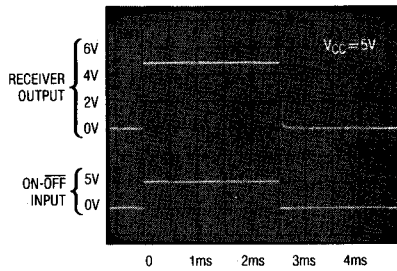


SHUTDOWN to Driver Output

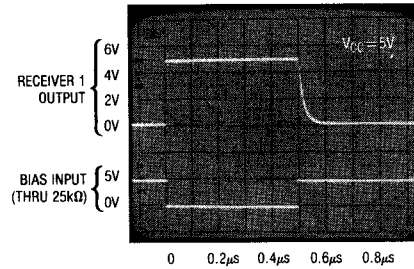


TYPICAL PERFORMANCE CHARACTERISTICS

SHUTDOWN to Receiver Output

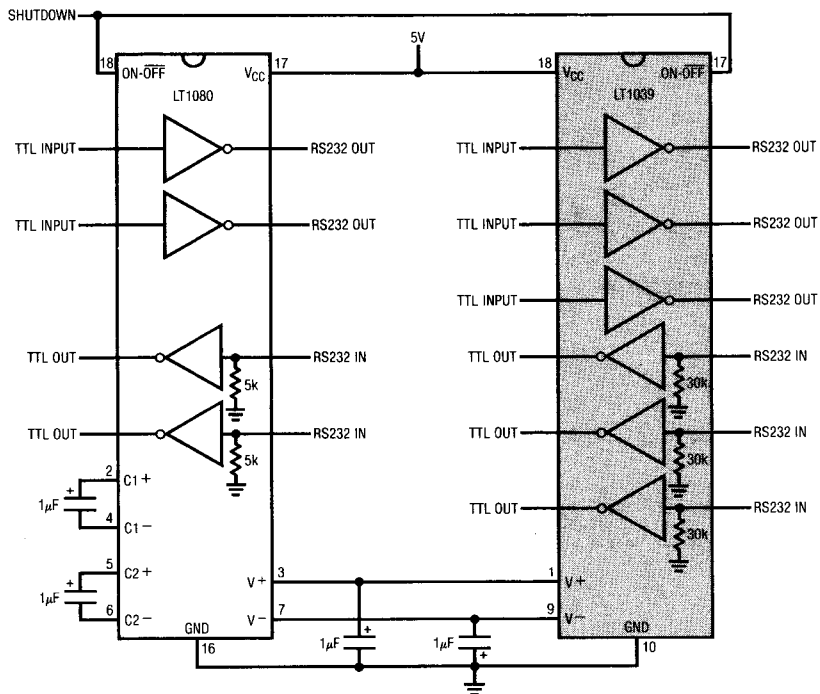


Bias Pin Response Time



TYPICAL APPLICATION

LT1080 (Driver/Receiver with Power Supply) Driving an LT1039



APPLICATION HINTS

The driver output stage of the LT1039 offers significantly improved protection over older bipolar and CMOS designs. In addition to current limiting, the driver output can be externally forced to $\pm 30V$ with no damage or excessive current flow, and will not disrupt the supplies. Some drivers have diodes connected between the outputs and the supplies, so externally applied voltages can cause excessive supply voltage to develop.

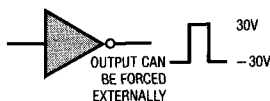
Placing the LT1039 in the SHUTDOWN mode (Pin 17 low) puts both the driver and receiver outputs in a high

impedance state. This allows data line sharing and transceiver applications.

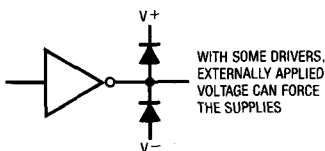
The SHUTDOWN mode also drops all supply currents (V_{CC} , V^+ , V^-) to zero for power-conscious systems.

When driving CMOS logic from a receiver that will be used in the SHUTDOWN mode and there is no other active receiver on the line, a 51k resistor can be placed from the logic input to V_{CC} to force a definite logic level when the receiver output is in a high impedance state.

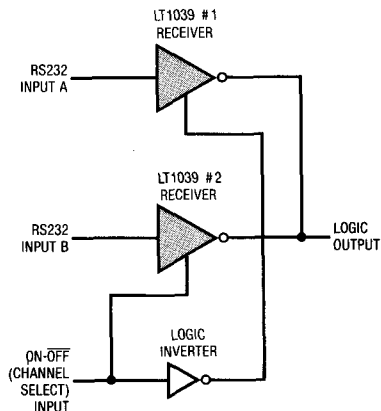
LT1039 Driver



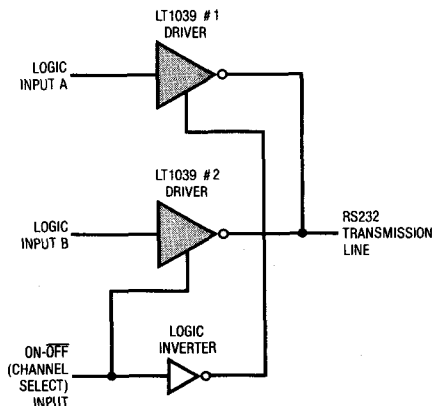
Older RS232 Drivers and Other CMOS Drivers



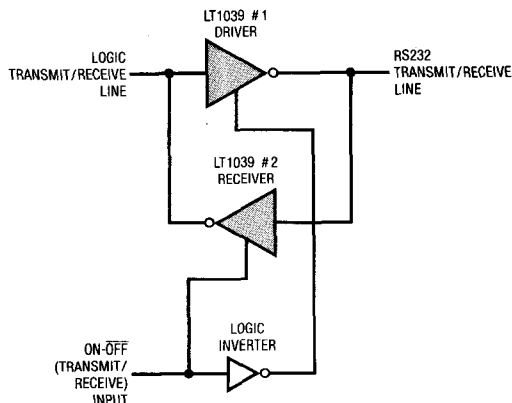
Sharing a Receiver Line



Sharing a Transmitter Line



Transceiver



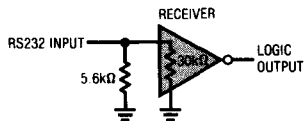
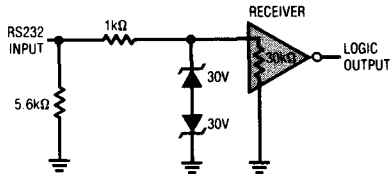
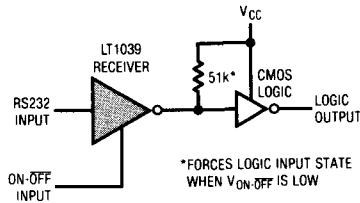
APPLICATION HINTS

To protect against receiver input overloads in excess of $\pm 30V$, a voltage clamp can be placed on the data line and still maintain RS232 compatibility.

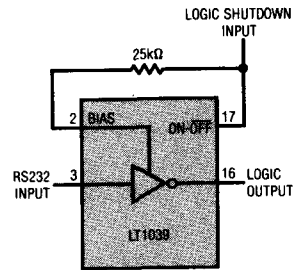
The receiver input impedance of the LT1039 is nominally $30k\Omega$. For applications requiring a $5k\Omega$ input impedance, a $5.6k\Omega$ resistor can be connected from the receiver input to ground.

Driver inputs should not be allowed to float. Any unused inputs should be tied to V_{CC} .

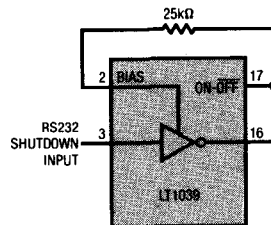
The bias pin is used to "keep alive" one receiver while in the SHUTDOWN mode (all other circuitry being inactive). This allows a system to be in SHUTDOWN and still have one active receiver for transferring data. It can also be used to make an RS232 compatible SHUTDOWN control line. Driving the bias pin low through a resistance of $24k\Omega$ to $30k\Omega$ keeps the receiver active. Do not drive the bias pin directly from a logic output without the series resistor. An unused bias pin should be left open.



Keeping Alive One Receiver while in SHUTDOWN

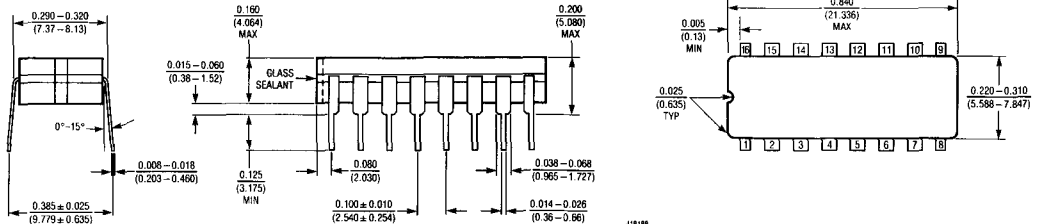


RS232 Compatible SHUTDOWN Control Line



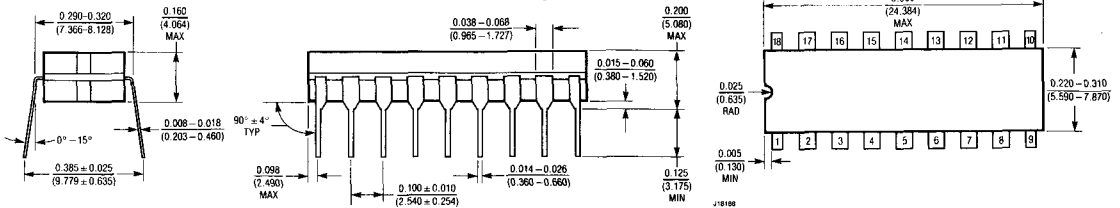
PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

J16 Package Ceramic DIP



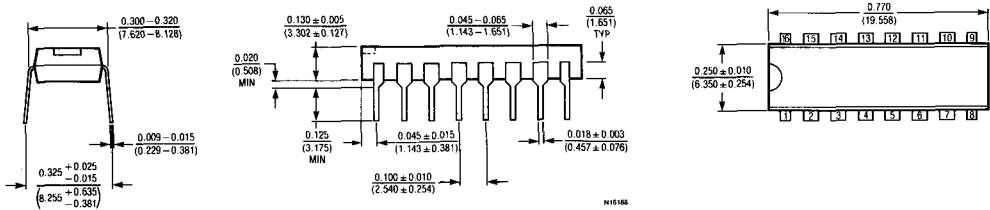
	T _{max}	θ _{ja}	θ _{jc}
LT1039MJ16	150°C	100°C/W	30°C/W
LT1039CJ16	150°C	100°C/W	30°C/W

J18 Package Ceramic DIP



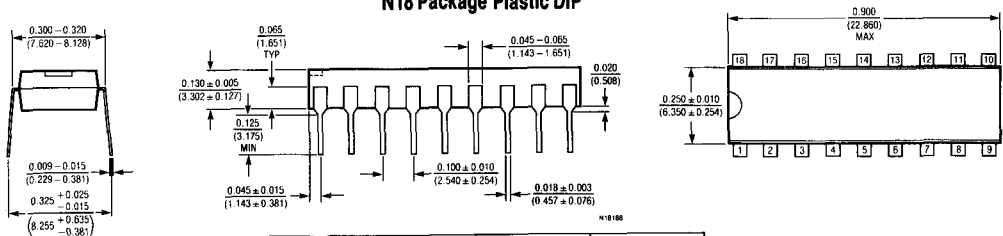
	T _{max}	θ _{ja}	θ _{jc}
LT1039MJ	150°C	100°C/W	40°C/W
LT1039CJ	150°C	100°C/W	40°C/W

N16 Package Plastic DIP



	T _{max}	θ _{ja}	θ _{jc}
LT1039CN16	85°C	140°C/W	50°C/W

N18 Package Plastic DIP



	T _{max}	θ _{ja}	θ _{jc}
LT1039CN	85°C	120°C/W	50°C/W

FEATURES

- Efficiently Translate Voltage Levels
- Internal Hysteresis for Noise Immunity
- Output Latches Included
- Three-State Outputs
- Programmable Power/Speed
- Power can be Completely Shut Off
- $\pm 50V$ on Inputs with External $100k\Omega$ Limit Resistor
- $1.2\mu s$ Response at $100\mu A$ Supply Current

APPLICATIONS

- TTL/CMOS to $\pm 5V$ Analog Switch Drive
- TTL to CMOS (3V to 15V V_{CC})
- ECL to CMOS (3V to 15V V_{CC})
- Ground Isolation Buffer
- Low Power RS232 Line Receiver

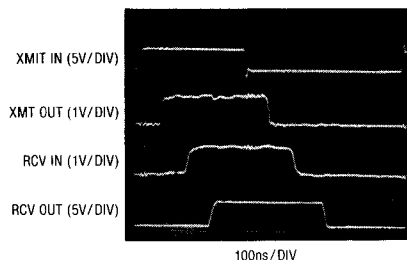
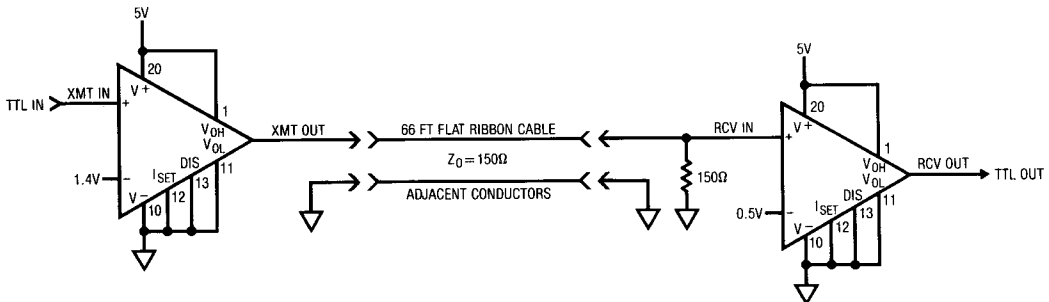
DESCRIPTION

The LTC1045 is a hex level translator manufactured using Linear Technology's enhanced LTCMOS™ silicon gate process. It consists of six high speed comparators with output latches and three-state capability. Each comparator's plus input is brought out separately. The minus inputs of comparators 1-4 are tied to V_{TRIP1} and 5-6 are tied to V_{TRIP2} .

The I_{SET} pin has several functions. When taken to V^+ the outputs are latched and power is completely shut off. Power/speed can be programmed by connecting I_{SET} to V^- through an external resistor.

LTCMOS™ is a trademark of Linear Technology Corp.

Flat Ribbon Cable Driver/Receiver



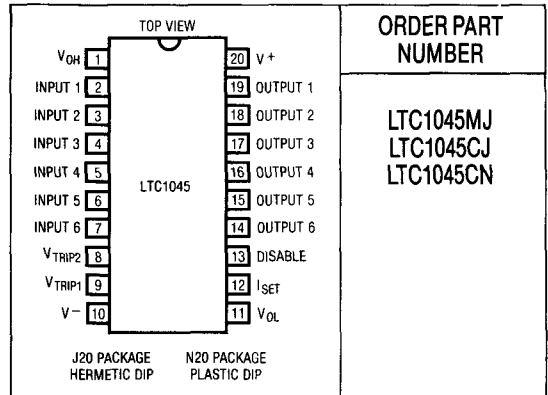
100ns / DIV

ABSOLUTE MAXIMUM RATINGS

(Notes 1 and 2)

- Total Supply Voltage (V^+ , V_{OH} to V^- , V_{OL})..... 18V
- Output High Voltage (V_{OH}) $\leq V^+$
- Input Voltage 18V to $V^- - 0.3V$
- Operating Temperature Range
 - LTC1045C..... -40°C to 85°C
 - LTC1045M -55°C to 125°C
- Storage Temperature Range -55°C to 150°C
- Lead Temperature (Soldering, 10 sec) 300°C
- Output Short Circuit Duration
 - ($V_{OH} - V_{OL} \leq 10V$)..... Continuous
- ESD (MIL-STD-883, Method 3015.1)..... 2000V

PACKAGE/ORDER INFORMATION



ORDER PART NUMBER

LTC1045MJ
LTC1045CJ
LTC1045CN

ELECTRICAL CHARACTERISTICS

(Note 3) $V^+ = V_{OH} = 5V$, $V^- = V_{OL} = 0V$, $T_A = 25^\circ\text{C}$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	LTC1045M			LTC1045C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
I_B	Input Bias Current	$V^- \leq V_{IN} \leq V^+$		± 1	1.0	± 1		0.5	nA μA
	Trip Voltage Range (Pin 8 and Pin 9)		V^-		$V^+ - 2$	V^-		$V^+ - 2$	V
I_S	V^+ to V^- Supply Current	DISABLE = V^+ , $R_{SET} = 10k$		2.5	3.5 5.0	2.5	3.5	4.5	mA mA
I_{OFF}	V^+ to V^- Supply Current in Shutdown	DISABLE = $I_{SET} = V^+$		10	5	10		1	nA μA
V_{REF}	Voltage on I_{SET} (Pin 12)	$R_{SET} = 10k$	0.5	0.9	1.4	0.6	0.9	1.25	V V
V_{OH}	TTL Output High Voltage	$I_{OUT} = -360\mu\text{A}$, $V^+ = 4.5V$	2.4	4.4		2.4	4.4		V
V_{OL}	TTL Output Low Voltage	$I_{OUT} = 1.6\text{mA}$, $V^+ = 4.5V$		0.2	0.4		0.2	0.4	V
I_{SINK}	Output Short Circuit Sink Current	$V_{IN} = V_{TRIP} - 100\text{mV}$, $V_{OUT} = V^+$	8.5 5.5	15		7.5 5.5	15		mA mA
I_{SOURCE}	Output Short Circuit Source Current	$V_{IN} = V_{TRIP} + 100\text{mV}$, $V_{OUT} = V^-$	4.5 3.2	8.0		4.0 3.2	8.0		mA mA
I_{OZ}	Three-State Leakage Current	DISABLE = V^+ $V_{OL} \leq V_{OUT} \leq V_{OH}$		0.005	1		0.005	1	μA μA
R_{OH}	Output Resistance to V_{OH}	$ I_{OUT} \leq 100\mu\text{A}$		260	400 600		260	475 600	Ω Ω
R_{OL}	Output Resistance to V_{OL}	$ I_{OUT} \leq 100\mu\text{A}$		100	150 250		100	180 250	Ω Ω
	I_{SET} Voltage for Shutdown		$V^+ - 0.5$			$V^+ - 0.5$			V
V_{IH} V_{IL}	DISABLE Input Logic Levels	$V^+ = 4.5V$, $V^- = 0V$ $V^+ = 5.5V$, $V^- = 0V$	2.0		0.8	2.0		0.8	V V
	Input Supply Differential ($V^+ - V^-$) (Note 3)		4.5		15	4.5		15	V
	Output Supply Differential ($V_{OH} - V_{OL}$) (Note 3)		3		15	3		15	V

AC ELECTRICAL CHARACTERISTICS

$V^+ = V_{OH} = 5V$, $V^- = V_{OL} = 0V$, $T_A = 25^\circ C$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	LTC1045M			LTC1045C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
t_d	Response Time	Test Circuit Figure 1 $R_{SET} = 10k, \pm 100mV$ Drive	●		200			250	ns
						350		350	
t_{SETUP}	Time Before Rising Edge of I_{SET} that Data Must be Present	Test Circuit Figure 2		80			80	ns	
t_{HOLD}	Time After Rising Edge of I_{SET} that Data Must be Present	Test Circuit Figure 2		0			0	ns	
t_{ACC}	Falling Edge of DISABLE to Logic Level (from Hi-Z State)	Test Circuit Figure 3		165			165	ns	
t_{IH}, t_{OH}	Rising Edge of DISABLE to Hi-Z State	Test Circuit Figure 3		200			200	ns	

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: Absolute Maximum Ratings are those values beyond which the life of the device may be impaired.

Note 2: The maximum differential voltage between any two power pins (V^+ , V^- , V_{OH} and V_{OL}) must not exceed 18V. The maximum recommended operating differential is 15V.

Note 3: During operation near the maximum supply voltage limit, care should be taken to avoid or suppress power supply turn-on and turn-off transients, power supply ripple, or ground noise; any of these conditions must not cause a supply differential to exceed the absolute maximum rating.

TEST CIRCUITS

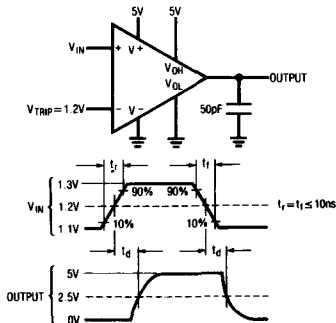


Figure 1. Response Time Test Circuit

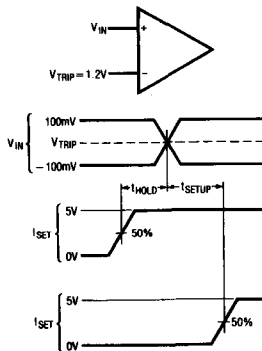


Figure 2. Latch Test Circuit

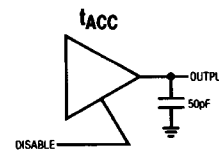
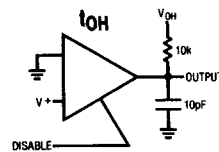
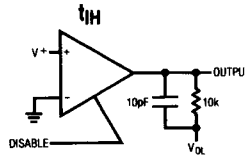
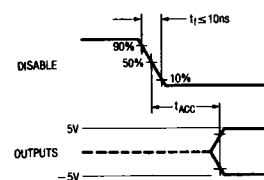
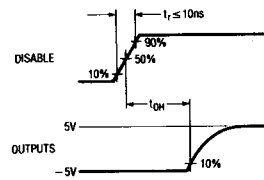
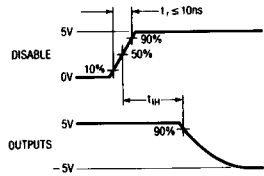
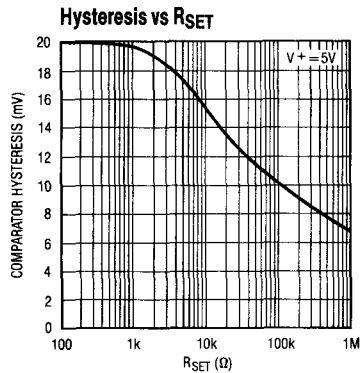
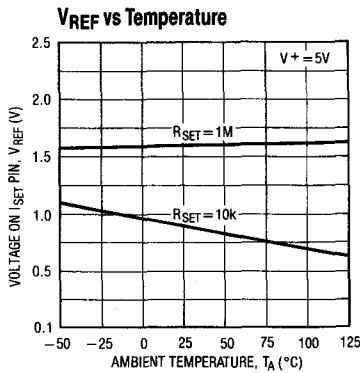
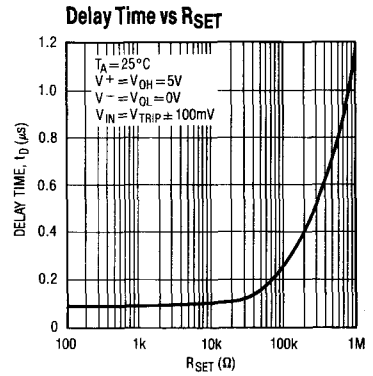
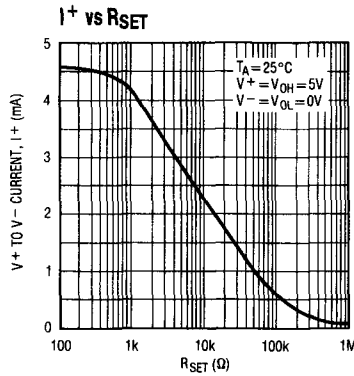
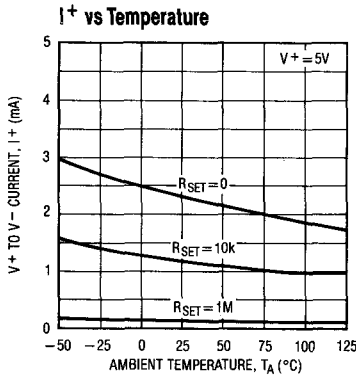


Figure 3. Three-State Output Test Circuit, Conditions: $V^+ = 5V$, $V^- = 0V$, $V_{OH} = 5V$, $V_{OL} = 0V$



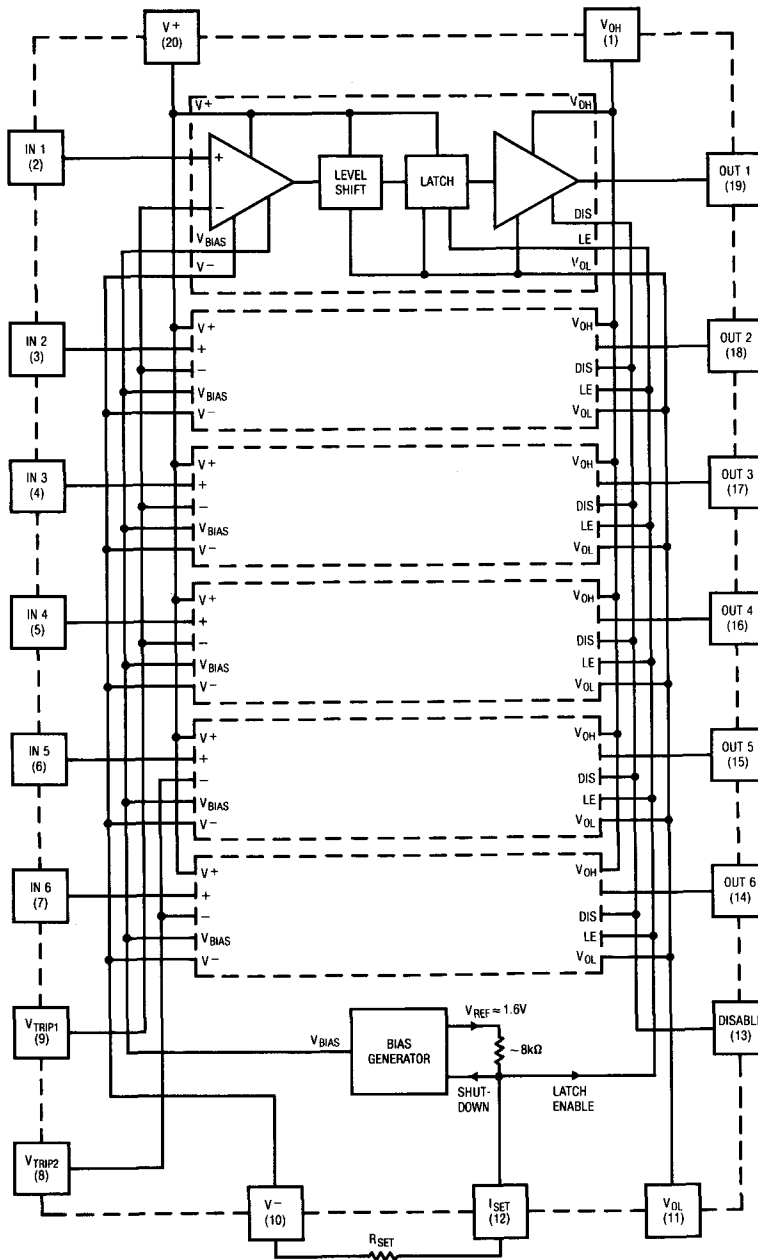
TYPICAL PERFORMANCE CHARACTERISTICS



PIN DESCRIPTION

Pin	Name	Description	Pin	Name	Description
1	VOH	High level to which the output switches	11	VOL	Comparator negative supply
2-7	INPUT	Six comparator inputs; voltage range = V- to V+ + 18V	12	ISET	This pin has three functions 1) RSET from this pin to V- sets bias current 2) When forced to V+ power is shut off completely 3) When forced to V+ outputs are latched
8	VTRIP2	Trip point for first four comparators (inputs 1-4); voltage range = V- to V+ - 2V	13	DISABLE	When high outputs are Hi-Z
9	VTRIP1	Trip point for last two comparators (inputs 5-6); voltage range = V- to V+ - 2V	14-19	OUTPUT	Six driver outputs
10	V-	Low level to which the output switches	20	V+	Comparator positive supply

BLOCK DIAGRAM



10

APPLICATIONS INFORMATION

The LTC1045 consists of six voltage translators and associated control circuitry, see Block Diagram. Each translator has a linear comparator input stage with the positive input brought out separately. The negative inputs of the first four comparators are tied in common to V_{TRIP1} and the negative inputs of the last two comparators are tied in common to V_{TRIP2} . With these inputs the switching point of the comparators can be set anywhere within the common-mode range of V^- to $V^+ - 2V$. To improve noise immunity each comparator has a small built-in hysteresis. Hysteresis varies with bias current from 7mV at low bias current to 20mV at high bias current (see typical curve of Hysteresis vs R_{SET}).

Setting the Bias Current

Unlike CMOS logic, any linear CMOS circuit must draw some quiescent current. The bias generator (Block Diagram) allows the quiescent current of the comparators to be varied. Bias current is programmed with an external resistor (see typical curve of I^+ vs R_{SET}). As the bias current is decreased, the LTC1045 slows down (see typical curve of Delay Time vs R_{SET}).

Shutting Power Off and Latching the Outputs

In addition to setting the bias current, the I_{SET} pin shuts power completely off and latches the translator outputs. To do this, the I_{SET} pin must be forced to $V^+ - 0.5V$. As shown in Figure 4, a CMOS gate or a TTL gate with a resistor pull-up does this quite nicely. Even though power is

turned off to the linear circuitry, the CMOS output logic is powered and maintains the output state. With no DC load on the output, power dissipation, for all practical purposes, is zero.

Latching the output is fast—typically 80ns from the rising edge of I_{SET} . Going from the latched to flow through state is much slower—typically 1.5 μ s from the falling edge of I_{SET} . This time is set by the comparator's power up time. During the power up time, the output can assume false states. To avoid problems, the output should not be considered valid until 2 μ s to 5 μ s after the falling edge of I_{SET} .

Putting the Outputs in Hi-Z State

A DISABLE input sets the six outputs to a high impedance state. This allows the LTC1045 to be interfaced to a data bus. When DISABLE = "1" the outputs are high impedance and when DISABLE = "0" they are active. With TTL supplies, $V^+ = 4.5V$ to 5.5V and $V^- = GND$, the DISABLE input is TTL compatible.

Power Supplies

There are four power supplies on the LTC1045: V^+ , V^- , V_{OH} and V_{OL} . They can be connected almost arbitrarily, but there are a few restrictions. A minimum differential must exist between V^+ and V^- and V_{OH} and V_{OL} . The V^+ to V^- differential must be at least 4.5V and the V_{OH} to V_{OL} differential must be at least 3.0V. Another restriction is caused by the internal parasitic diode D1 (see Figure 5).

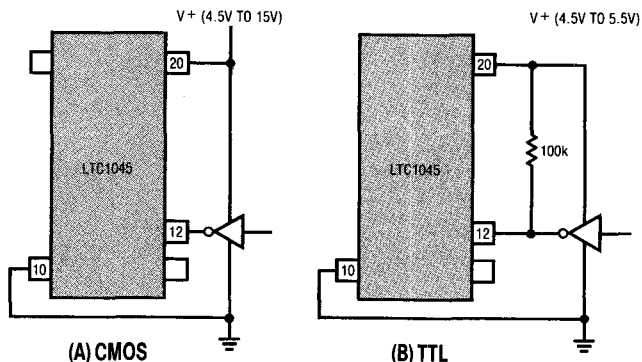


Figure 4. Driving the I_{SET} Pin with Logic

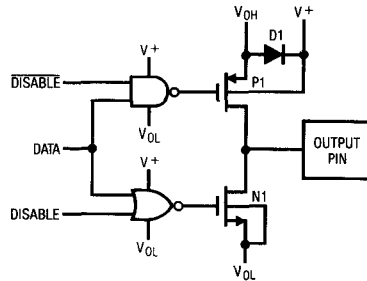


Figure 5. Output Driver

APPLICATIONS INFORMATION

Because of this diode, V_{OH} must not be greater than V^+ . Lastly the maximum voltage between any two power supply pins must not exceed 15V operating or 18V absolute maximum. For example, if $V^+ = 5V$, V^- or V_{OL} should be no more negative than $-10V$. Note that V_{OL} should not be more negative than $-10V$ even if the V_{OH} to V_{OL} differential does not exceed the 15V maximum. In this case the V^+ to V_{OL} differential sets the limit.

Input Voltage

The LTC1045 has no upper clamp diodes as do conventional CMOS circuits. This allows the inputs to exceed the V^+ supply. The inputs will break down approximately 30V above the V^- supply. If the input current is limited with 100k Ω , the input voltage can be driven to at least $\pm 50V$ with no adverse effects for any combination of allowed

power supply voltages. Output levels will be correct even under these conditions (i.e., if the input voltage is above the trip point, the output will be high and if it is below, the output will be low).

Output Drive

Output drive characteristics of the LTC1045 will vary with the power supply voltages that are chosen. Output impedance is affected by V^+ , V_{OH} and V_{OL} . V^- has no effect on output impedance. Guaranteed drive characteristics are specified in the table of electrical characteristics for $V^+ = V_{OH} = 5V$ and $V^- = V_{OL} = 0V$. Figures 6 and 7 show relative output impedance for other supply combinations. In general, output impedance is minimized if V^+ to V_{OH} is minimized and V_{OH} to V_{OL} is maximized.

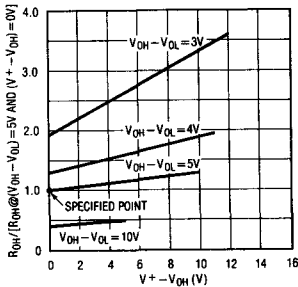


Figure 6. Relative Output Sourcing Resistance (R_{OH}) vs $V^+ - V_{OH}$

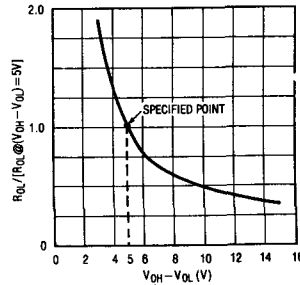
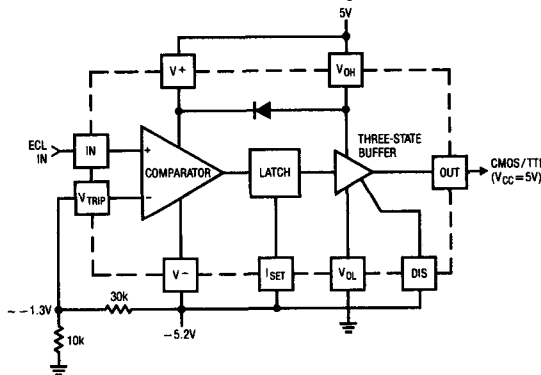


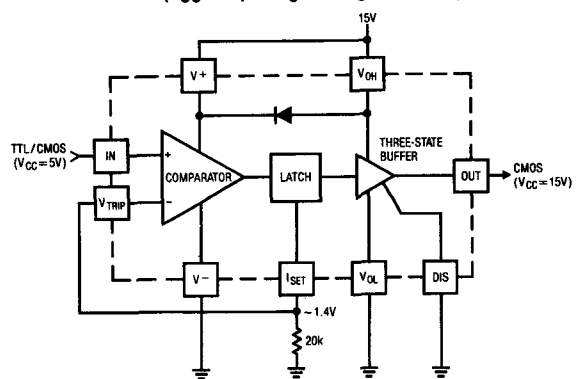
Figure 7. Relative Output Sinking Resistance (R_{OL}) vs $V_{OH} - V_{OL}$

TYPICAL APPLICATIONS

ECL to CMOS/TTL Logic

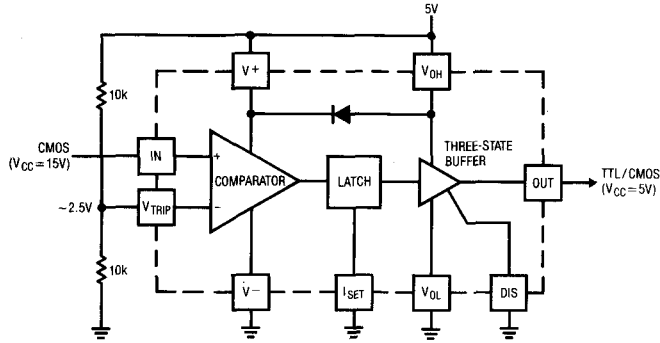


TTL/CMOS ($V_{CC} = 5V$) to High Voltage CMOS ($V_{CC} = 15V$)

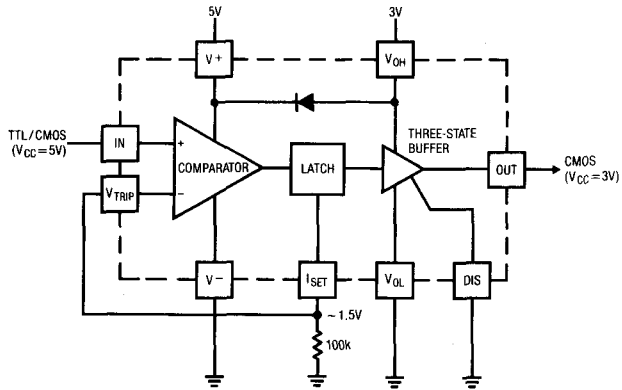


TYPICAL APPLICATIONS

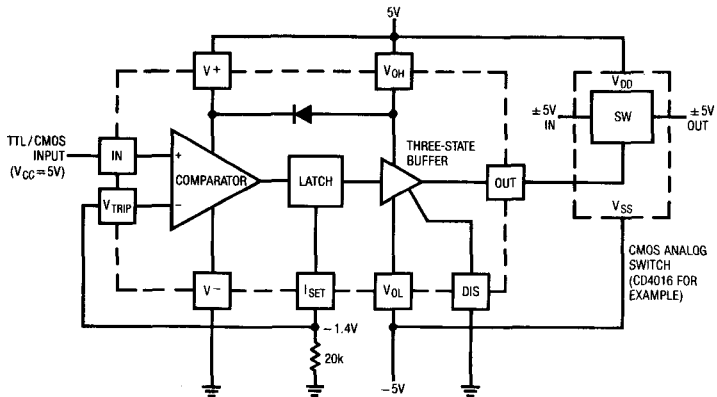
High Voltage CMOS ($V_{CC} = 15V$) to TTL/CMOS ($V_{CC} = 5V$)



TTL/CMOS ($V_{CC} = 5V$) to Low Voltage CMOS ($V_{CC} = 3V$)

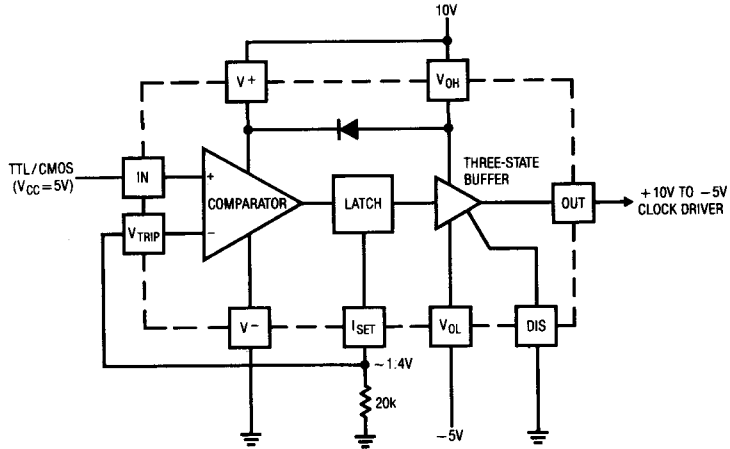


TTL/CMOS Logic Levels to $\pm 5V$ Analog Switch Driver

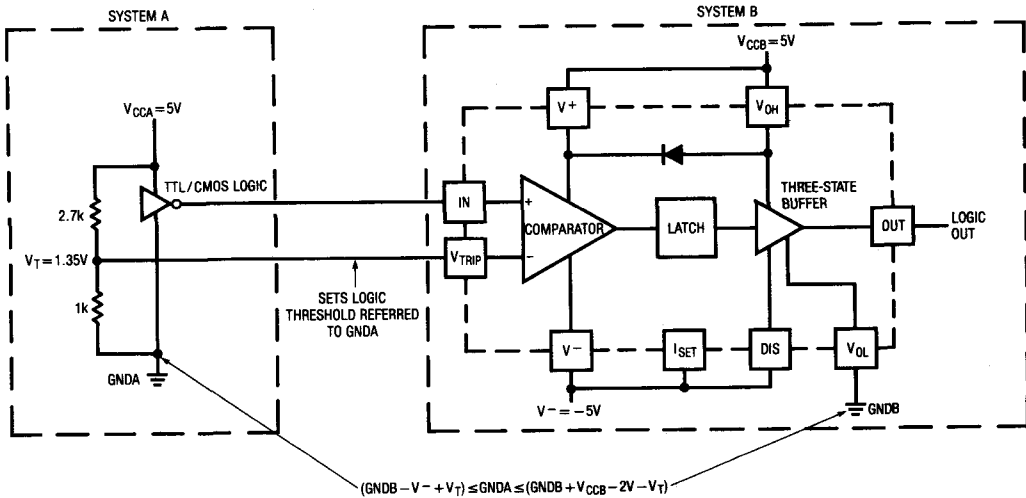


TYPICAL APPLICATIONS

TTL/CMOS ($V_{CC} = 5V$) to +10V/-5V Clock Driver

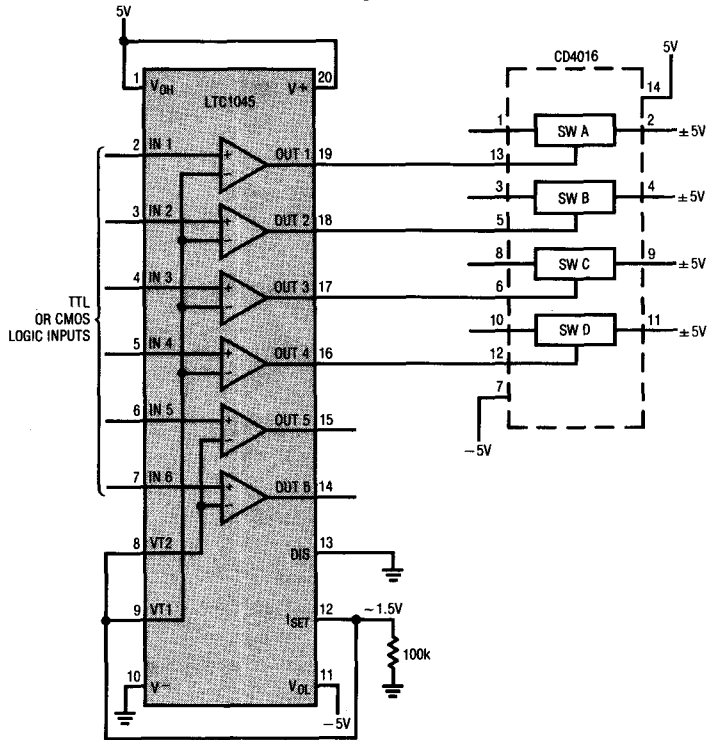


Logic Ground Isolation when Two Grounds are within LTC1045 Common-Mode Range

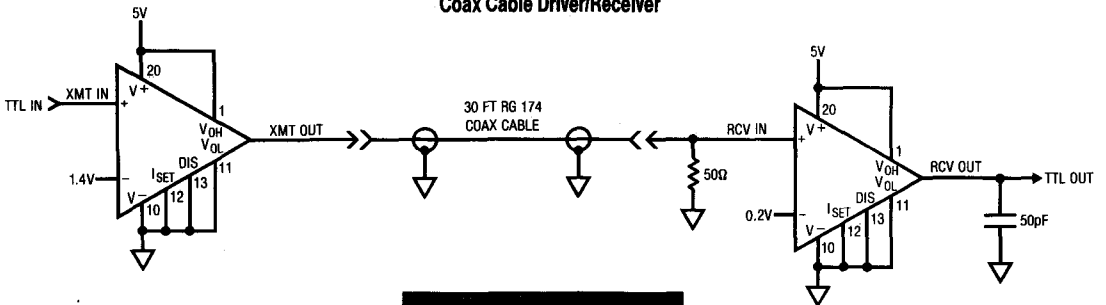


TYPICAL APPLICATIONS

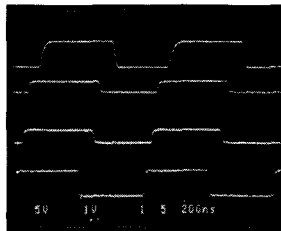
±5V Analog Switch Driver



Coax Cable Driver/Receiver



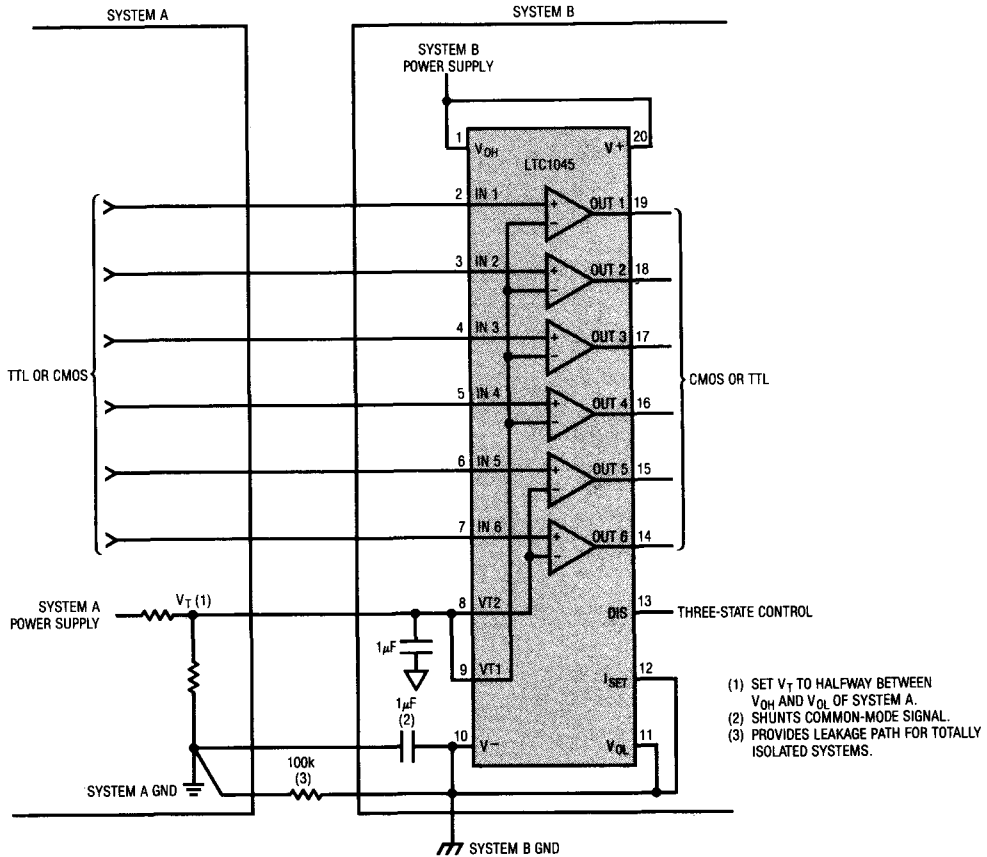
RCV OUT (5V/DIV)
 RCV IN (1V/DIV)
 XMIT OUT (1V/DIV)
 XMIT IN (5V/DIV)



200ns/DIV

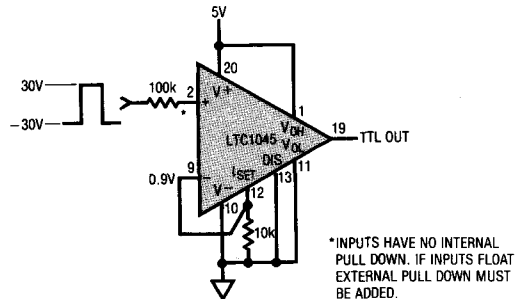
TYPICAL APPLICATIONS

Logic Systems DC Isolation



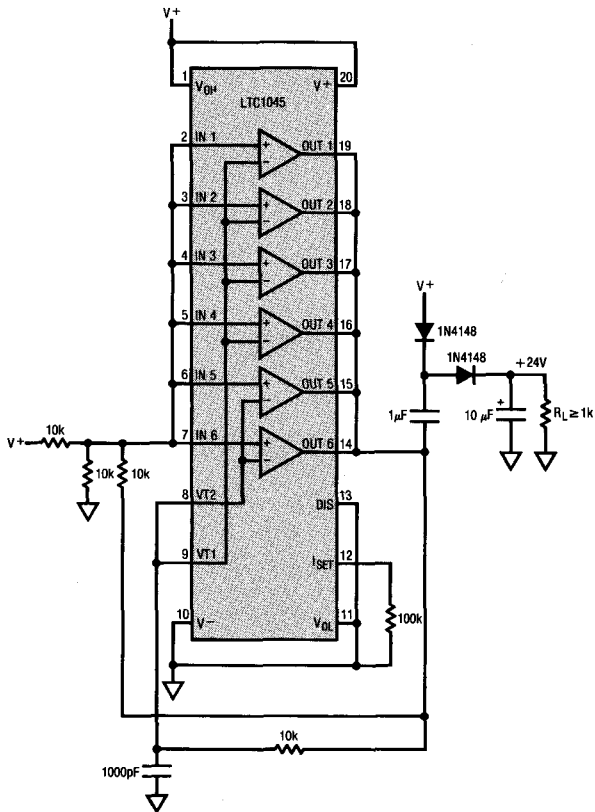
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RS232 Receiver

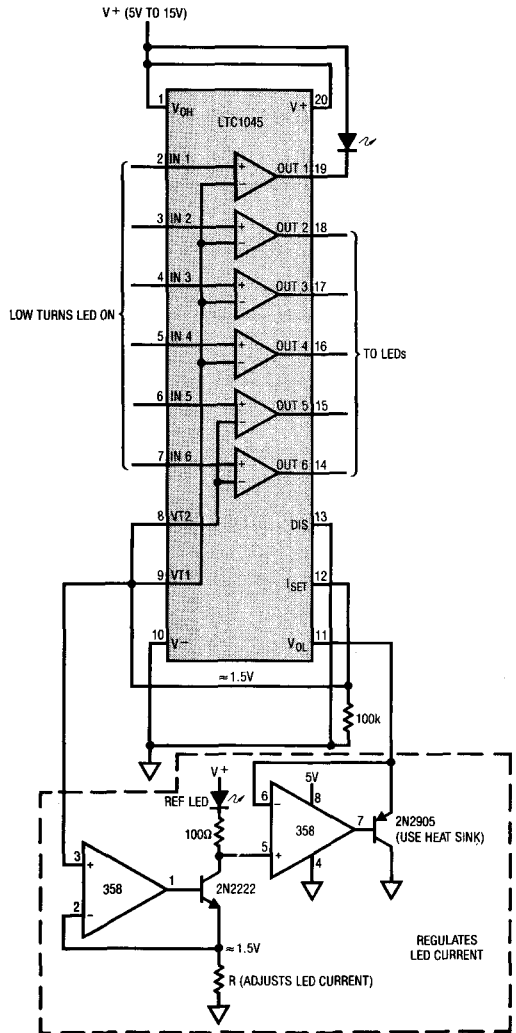


TYPICAL APPLICATIONS

24V Relay Supply from +12V/+15V Supply

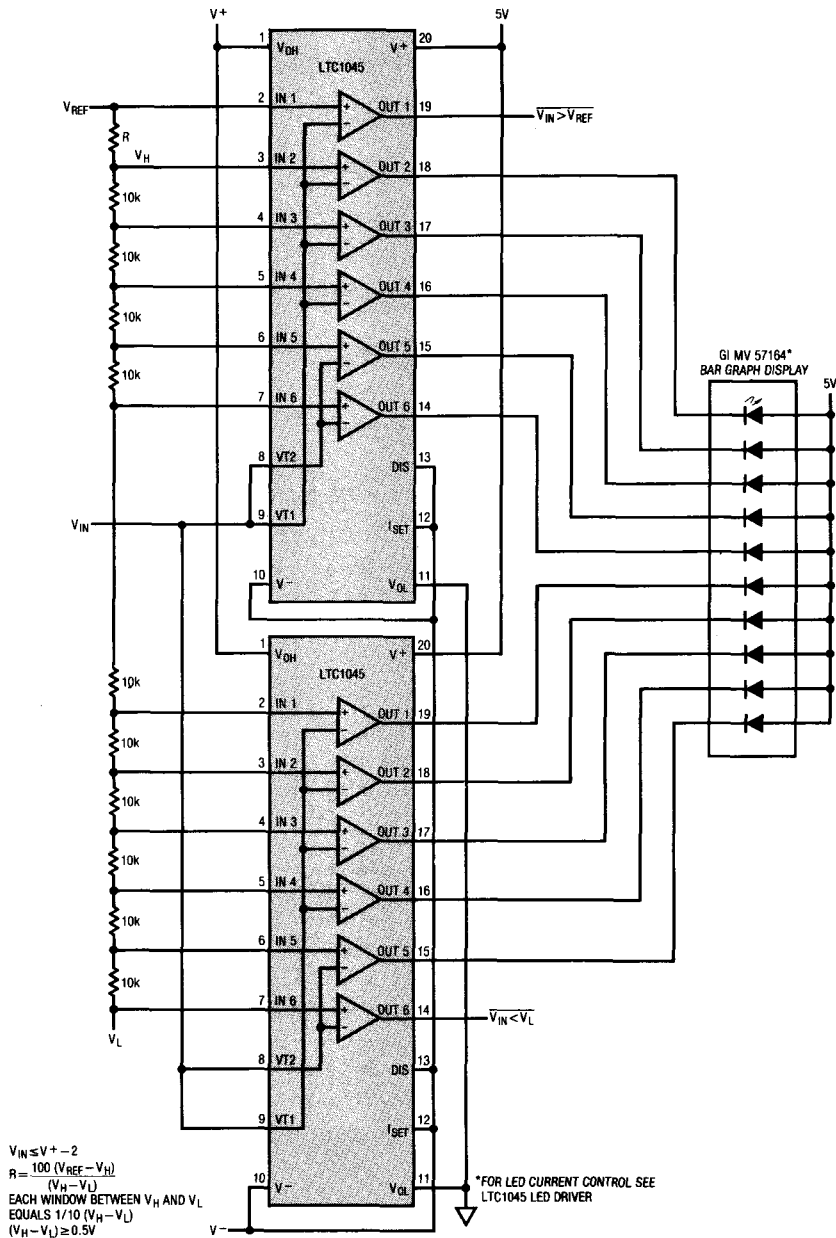


LED Driver



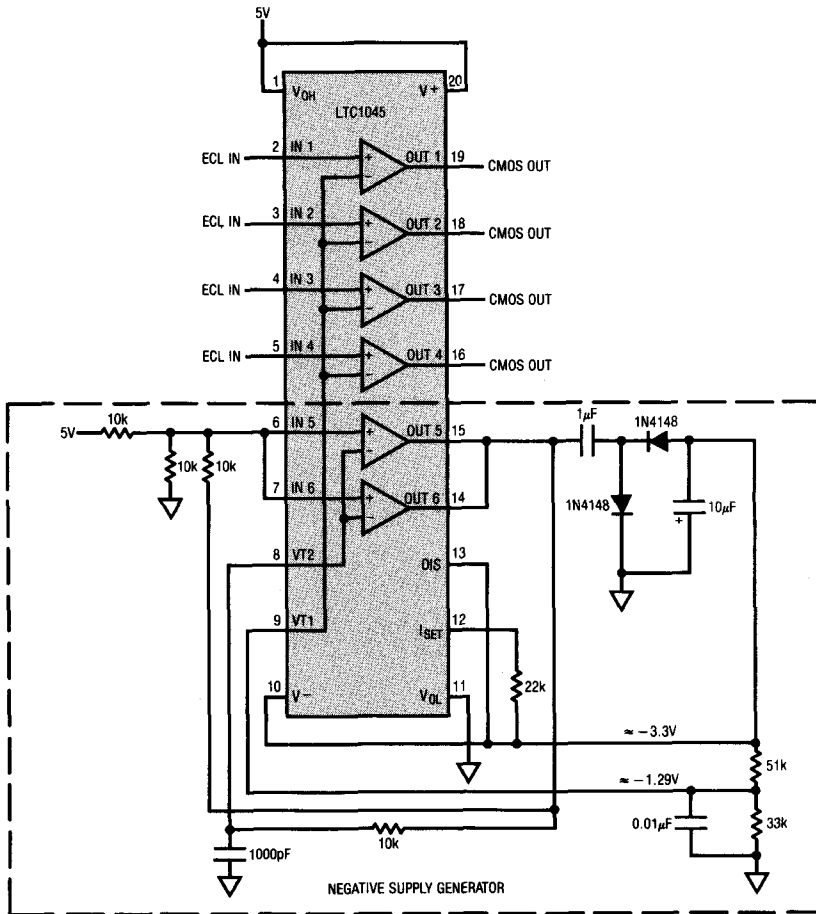
TYPICAL APPLICATIONS

Multi-Window Comparator and Display



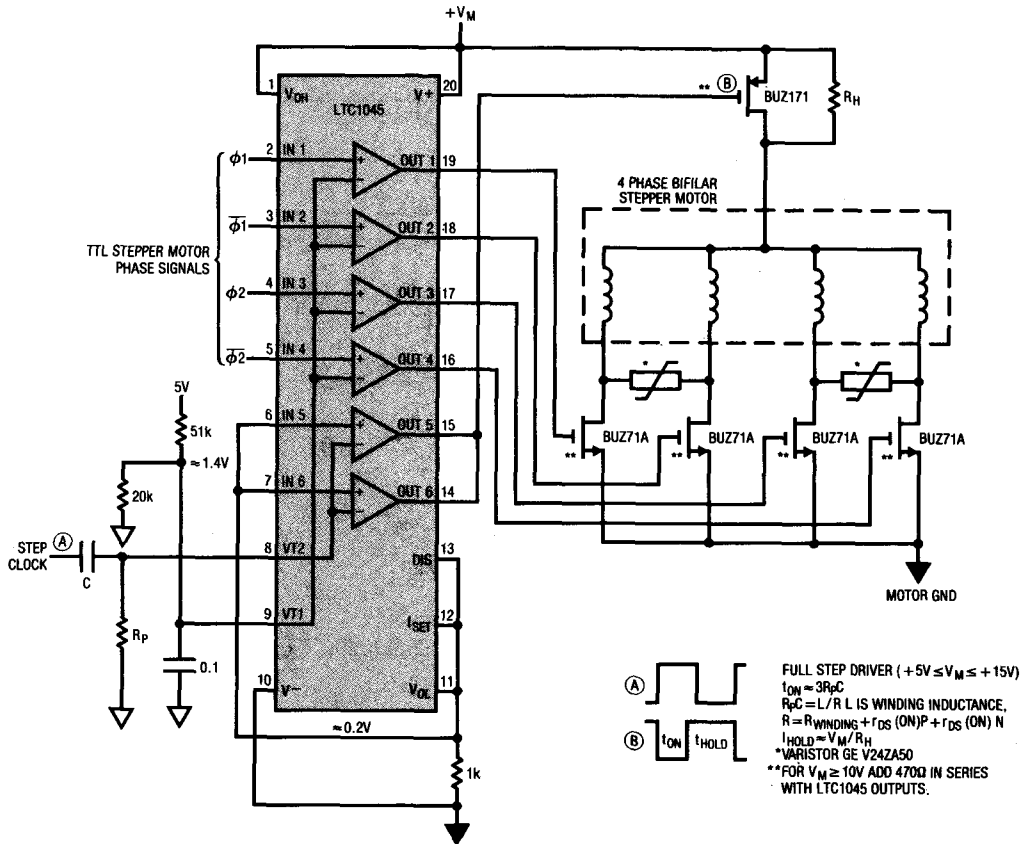
TYPICAL APPLICATIONS

ECL to CMOS from Single +5V Supply



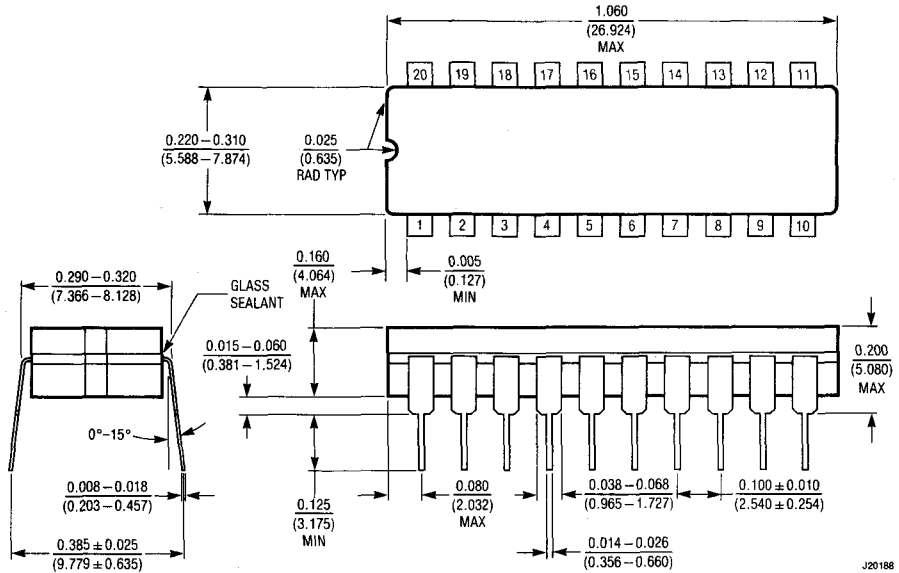
TYPICAL APPLICATIONS

Power MOSFET Driver Low Power Consumption Stepper Motor Driver



PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

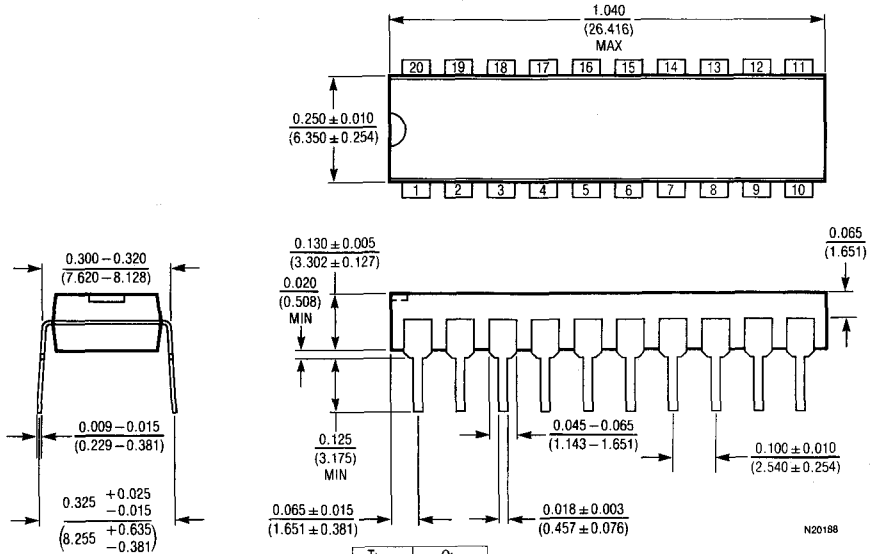
J20 Package Ceramic DIP



J20188

T _{jmax}	θ _{ja}
150°C	70°C/W

N20 Package Molded DIP



N20188

T _{jmax}	θ _{ja}
110°C	90°C/W

Advanced Low Power 5V RS232 Dual Driver/Receiver

FEATURES

- Absolutely No Latchup
- CMOS Comparable Low Power — 60mW
- **Superior to CMOS**
 - Improved Speed — Operates Over 64K Baud
 - Improved Protection — Outputs Can be Forced to $\pm 30V$ Without Damage
 - Three-State Outputs are High Impedance When Off
 - Only Needs $1\mu F$ Capacitors
- Can Power Additional RS232 Drivers — 10mA
- $1\mu A$ Supply Current in Shutdown
- Available in SO Package
- Available With or Without Shutdown

APPLICATIONS

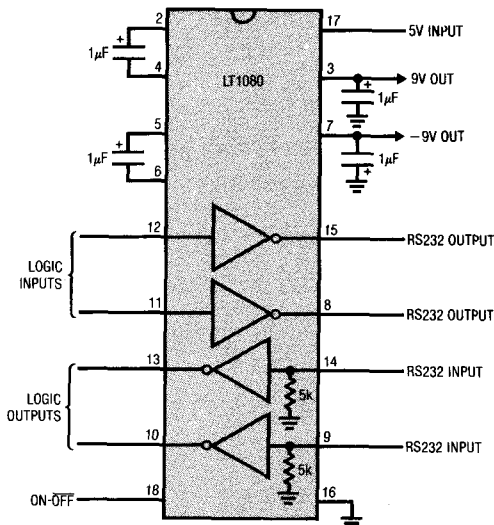
- Portable Computers
- Battery Powered RS232 Systems
- Power Supply Generator
- Terminals
- Modems

DESCRIPTION

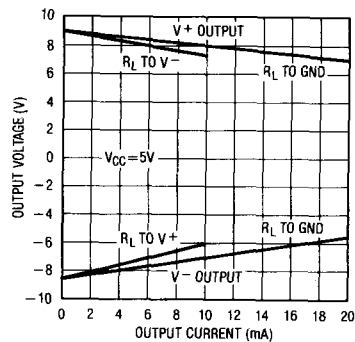
The LT1080 and LT1081 are the only dual RS232 driver/receiver with charge pump to guarantee absolutely no latchup. These interface optimized devices provide a realistic balance between CMOS levels of power dissipation and real world requirements for ruggedness. The driver outputs are fully protected against overload and can be shorted to $\pm 30V$. Unlike CMOS, the advanced architecture of the LT1080/LT1081 does not load the signal line when "shut down" or when power is off. Both the receiver and RS232 outputs are put into a high impedance state. An advanced output stage allows driving higher capacitive loads at higher speeds with exceptional ruggedness against ESD.

For applications requiring up to 5 drivers and 5 receivers with charge pump in one package see the LT1130 Series data sheet. A version of the LT1080/81, the LT1180 and LT1181 which use only $0.1\mu F$ capacitors is also available. All of Linear Technology's RS232 IC's are available in standard surface mount packages.

TYPICAL APPLICATION



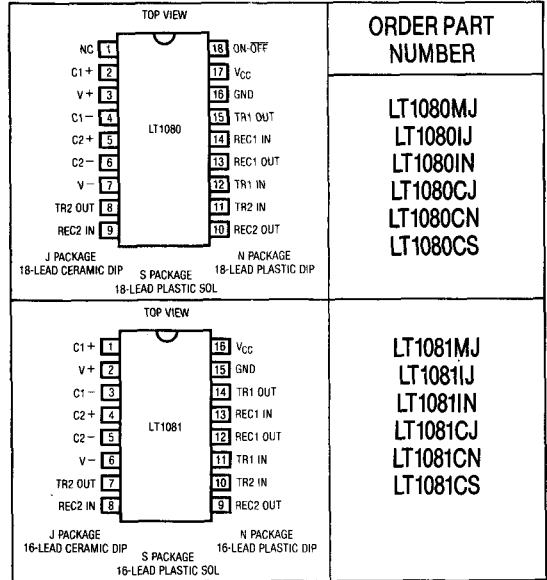
Supply Generator Outputs



ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V _{CC})	6V
V ⁺	12V
V ⁻	-12V
Input Voltage	
Driver	V ⁻ to V ⁺
Receiver	-30V to 30V
On-Off Pin	GND to 12V
Output Voltage	
Driver	V ⁻ + 30V to V ⁺ - 30V
Receiver	-0.3V to V _{CC} + 0.3V
Short Circuit Duration	
V ⁺	30 Seconds
V ⁻	30 Seconds
Driver Output	Indefinite
Receiver Output	Indefinite
Operating Temperature Range	
LT1080M/LT1081M	-55°C to 125°C
LT1080I/LT1081I	-40°C to 85°C
LT1080C/LT1081C	0°C to 70°C
Lead Temperature (Soldering, 10 sec.)	300°C

PACKAGE/ORDER INFORMATION



ELECTRICAL CHARACTERISTICS (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Driver					
Output Voltage Swing	Load = 3k to GND Both Outputs.	5.0 -5.0	7.3 -6.5		V V
Logic Input Voltage Level	Input Low Level (V _{OUT} = High) Input High Level (V _{OUT} = Low)	2.0	1.4 1.4	0.8	V V
Logic Input Current	V _{IN} ≥ 2.0V V _{IN} ≤ 0.8V		5 5	20 20	μA μA
Output Short Circuit Current	Sourcing Current, V _{OUT} = 0V Sinking Current, V _{OUT} = 0V	7 -7	12 -12		mA mA
Output Leakage Current	SHUTDOWN (Note 2), V _{OUT} = ±30V		10	100	μA
Slew Rate	R _L = 3kΩ, C _L = 51pF	4	15	30	V/μs
Receiver					
Input Voltage Thresholds	Input Low Threshold, LT1080C, LT1081C LT1080I, M/LT1081I, M	0.8 0.2	1.3 1.3		V V
	Input High Threshold, LT1080C/LT1081C LT1080I, M/LT1081I, M		1.7 1.7	2.4 3.0	V V
Hysteresis		0.1	0.4	1.0	V
Input Resistance		3	5	7	kΩ
Output Voltage	Output Low, I _{OUT} = -1.6mA		0.2	0.4	V
	Output High, I _{OUT} = 160μA (V _{CC} = 5V)	3.5	4.8		V
Output Short Circuit Current	Sinking Current, V _{OUT} = V _{CC}	-10	-20		mA
	Sourcing Current, V _{OUT} = 0V	0.6	1		mA
Output Leakage Current	SHUTDOWN (Note 2), 0V ≤ V _{OUT} ≤ V _{CC}		1	10	μA

ELECTRICAL CHARACTERISTICS (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply Generator (Note 3)					
V ⁺ Output Voltage	I _{OUT} = 0mA	8	9		V
	I _{OUT} = 10mA	7	8		V
	I _{OUT} = 15mA	6.5	7.5		V
V ⁻ Output Voltage	I _{OUT} = 0mA	-7.5	-8.5		V
	I _{OUT} = -10mA	-5.5	-6.5		V
	I _{OUT} = -15mA	-5	-6		V
Supply Current		●	12	22	mA
Supply Leakage Current (V _{CC})	SHUTDOWN (Note 2) (LT1080 Only)	●	1	100	μA
On-Off Pin Current	0V ≤ V _{ON-OFF} ≤ 5V (LT1080 Only)	●	-15	80	μA
Supply Rise Time	(Note 4) (LT1080 Only)		1		ms

The ● denotes specifications which apply over the operating temperature range (0°C ≤ T_A ≤ 70°C for commercial grade, -40°C ≤ T_A ≤ 85°C for industrial grade or -55°C ≤ T_A ≤ 125°C for military grade devices).

Note 1: These parameters apply for 4.5V ≤ V_{CC} ≤ 5.5V and V_{ON-OFF} = 3V, unless otherwise specified.

Note 2: V_{ON-OFF} = 0.4V for -55°C ≤ T_A ≤ 100°C, and V_{ON-OFF} = 0.2V for 100°C ≤ T_A ≤ 125°C. (LT1080 only)

Note 3: Unless otherwise specified, V_{CC} = 5V, external loading of V⁺ and V⁻ equals zero and the driver outputs are low (inputs high).

Note 4: Time from either SHUTDOWN high or power on until V⁺ ≥ 6V and V⁻ ≤ -6V. All external capacitors are 1μF.

PIN FUNCTIONS (Pin numbers refer to LT1080)

V_{CC} (Pin 17): Input supply pin. Supply current drops to zero in the SHUTDOWN mode.

GND (Pin 16): Ground pin.

On-Off (Pin 18): Controls the operation mode of the LT1080 and is TTL/CMOS compatible. A logic low puts the device in the SHUTDOWN mode which reduces input supply current to zero and places both driver and receiver outputs in a high impedance state. A logic high fully enables the device.

V⁺ (Pin 3): Positive supply for RS232 drivers. V⁺ ≈ 2V_{CC} - 1.5V. Requires an external capacitor (≥ 1μF) for charge storage. May be loaded (up to 15mA) for external system use. Loading does reduce V⁺ voltage (see graphs). Capacitor may be tied to ground or +5V input supply. With multiple transceiver, the V⁺ and V⁻ pins may be paralleled into common capacitors.

V⁻ (Pin 7): Negative supply for RS232 drivers. V⁻ ≈ -(2V_{CC} - 2.5V). Requires an external capacitor (≥ 1μF) for charge storage. May be loaded (up to -15mA) for external system use. Loading does reduce V⁻ voltage (see graphs). With multiple transceiver, the V⁺ and V⁻ pins may be paralleled into common capacitors.

TR1 IN; TR2 IN (Pins 12, 11): RS232 driver input pins. Inputs are TTL/CMOS compatible. Inputs should not be allowed to float. Tie unused inputs to V_{CC}.

TR1 OUT; TR2 OUT (Pins 15, 8): Driver outputs with RS232 voltage levels. Outputs are in a high impedance state when in the SHUTDOWN mode or when power is off (V_{CC} = 0V) to allow data line sharing. Outputs are fully short circuit protected from V⁻ + 30V to V⁺ - 30V with power on, off, or in the SHUTDOWN mode. Typical output breakdowns are greater than ±45V and higher applied voltages will not damage the device if moderately current limited. Shorting one output will affect output from the other.

REC1 IN; REC2 IN (Pins 14, 9): Receiver inputs. Accepts RS232 voltage levels (±30V) and has 0.4V of hysteresis to provide noise immunity. Input impedance is nominally 5kΩ.

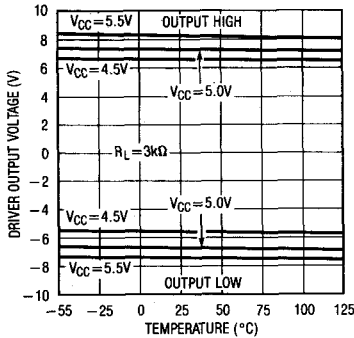
REC1 OUT; REC2 OUT (Pins 13, 10): Receiver outputs with TTL/CMOS voltage levels. Outputs are in a high impedance state when in the SHUTDOWN mode to allow data line sharing. Outputs are fully short circuit protected to ground or V_{CC} with power on, off, or in the SHUTDOWN mode.

C1 +; C1 -; C2 +; C2 - (Pins 2, 4, 5, 6): Requires an external capacitor (≥ 1μF) from C1 + to C1 - and another from C2 + to C2 -. Pin 2 can be used for connecting a second positive supply. When a separate positive supply is used, C1 can be deleted.

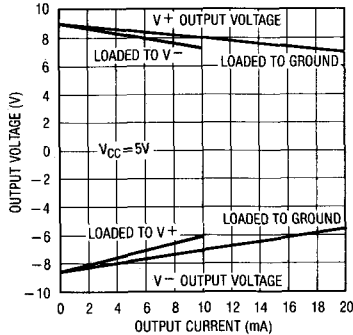
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TYPICAL PERFORMANCE CHARACTERISTICS

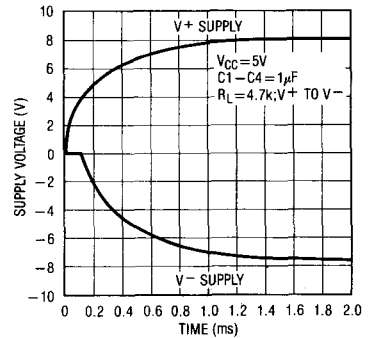
Driver Output Voltage



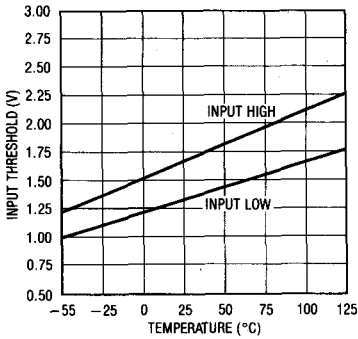
Supply Generator Outputs



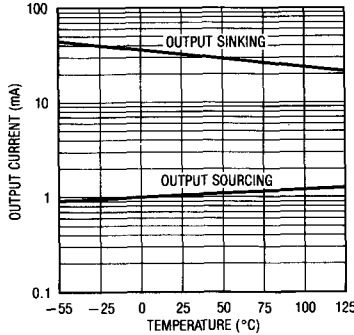
Supply Generation from Vcc or Shutdown



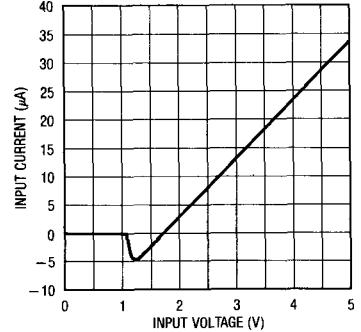
Receiver Input Thresholds



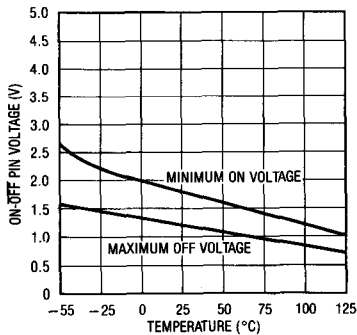
Receiver Output Short Circuit Current



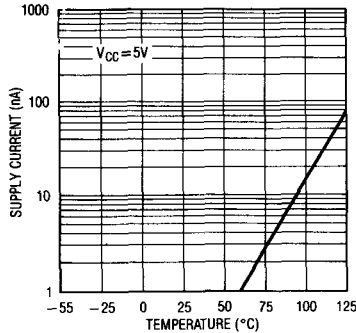
On-Off Pin Current vs Voltage



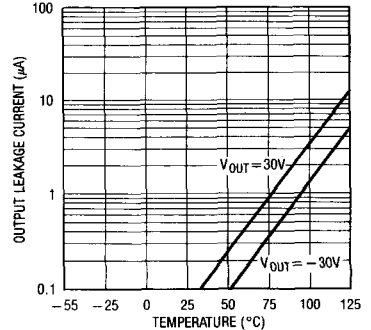
On-Off Pin Thresholds



Supply Current in Shutdown

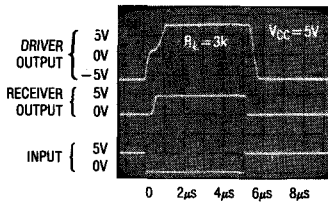


Driver Output Leakage in Shutdown

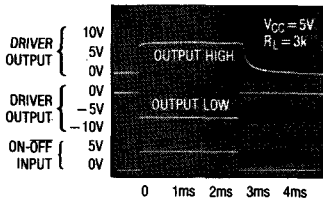


TYPICAL PERFORMANCE CHARACTERISTICS

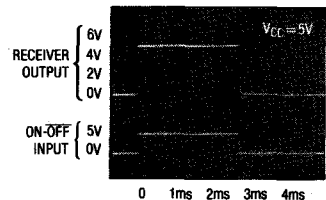
Output Waveforms



Shutdown to Driver Output

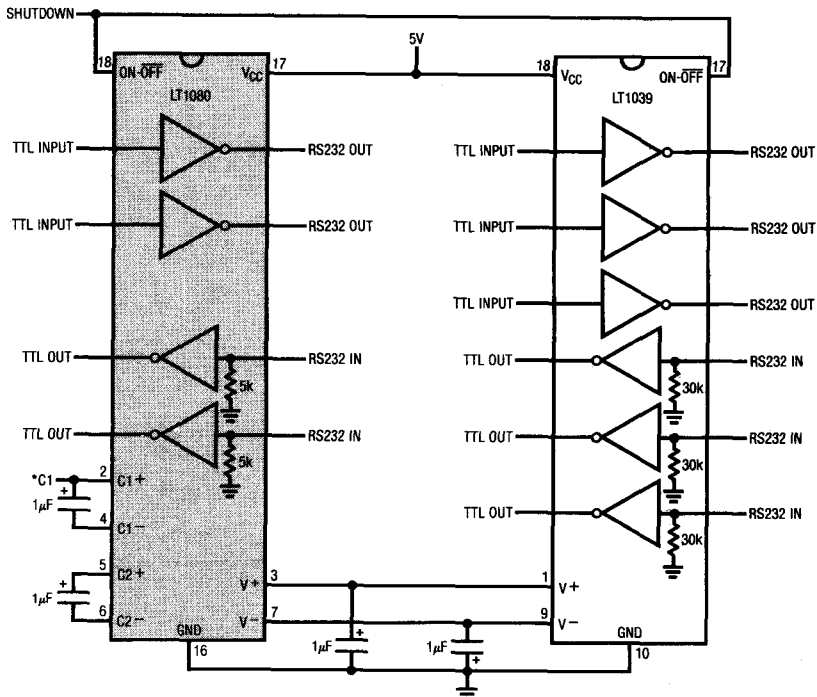


Shutdown to Receiver Output



TYPICAL APPLICATION

Supporting an LT1039 (Triple Driver/Receiver)



* IN APPLICATIONS WHERE A SEPARATE SECOND POSITIVE SUPPLY IS AVAILABLE (SUCH AS +5V AND +12V), THE +12V SUPPLY MAY BE CONNECTED TO PIN 2 AND C1 DELETED. THE POWER SUPPLY CIRCUITRY WILL THEN INVERT THE +12V SUPPLY. THE +5V SUPPLY IS STILL NEEDED TO POWER THE BIASING CIRCUITRY AND RECEIVERS.

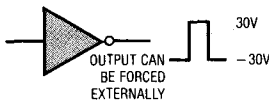
APPLICATION HINTS

The driver output stage of the LT1080 offers significantly improved protection over older bipolar and CMOS designs. In addition to current limiting, the driver output can be externally forced to $\pm 30V$ with no damage or excessive current flow, and will not disrupt the supplies. Some drivers have diodes connected between the outputs and the supplies, so externally applied voltages can cause excessive supply voltage to develop.

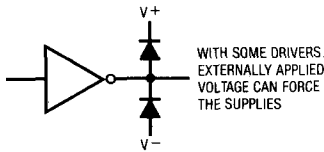
Placing the LT1080 in the SHUTDOWN mode (Pin 18 low) puts both the driver and receiver outputs in a high impedance state. This allows data line sharing and transceiver applications.

The SHUTDOWN mode also drops input supply current (V_{CC} ; Pin 17) to zero for power-conscious systems.

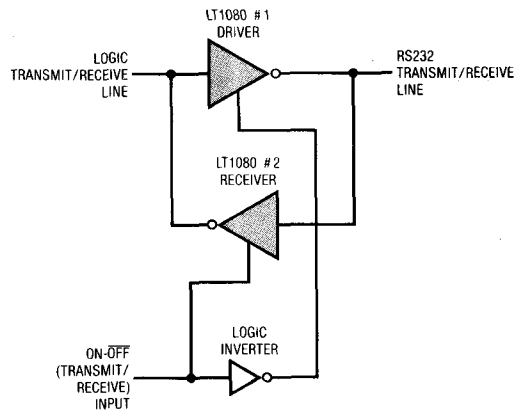
LT1080/LT1081 Driver



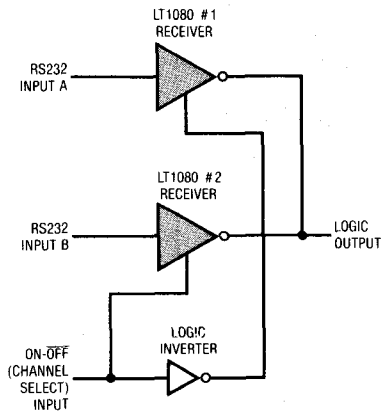
Older RS232 Drivers and CMOS Drivers



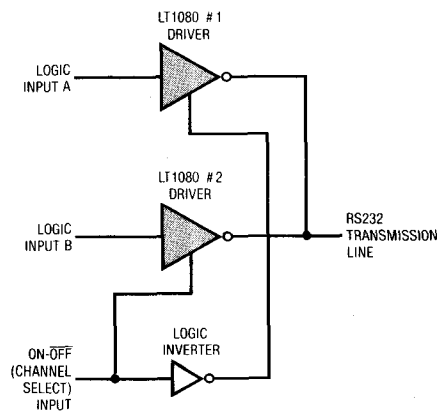
Transceiver



Sharing a Receiver Line

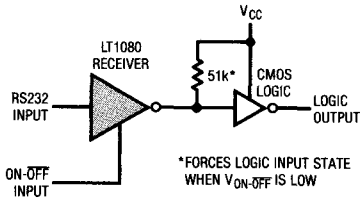


Sharing a Transmitter Line

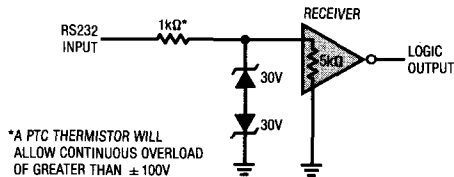


APPLICATION HINTS

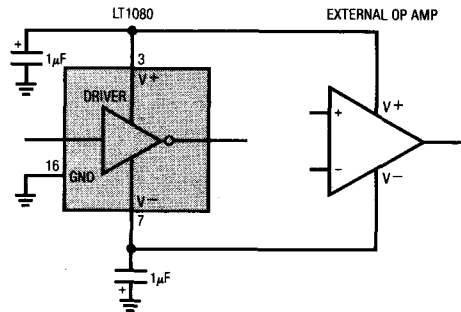
When driving CMOS logic from a receiver that will be used in the SHUTDOWN mode and there is no other active receiver on the line, a 51k resistor can be placed from the logic input to V_{CC} to force a definite logic level when the receiver output is in a high impedance state.



To protect against receiver input overloads in excess of $\pm 30V$, a voltage clamp can be placed on the data line and still maintain RS232 compatibility.

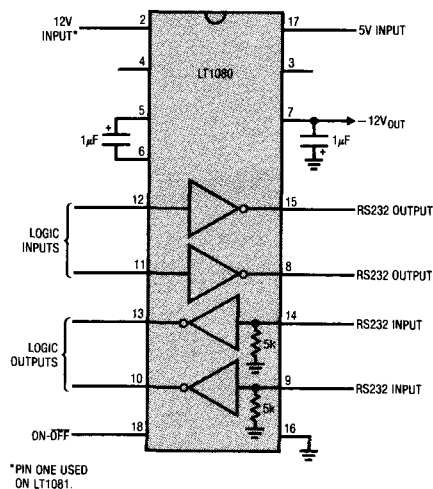


The generated driver supplies ($V+$ and $V-$) may be used to power external circuitry such as other RS232 drivers or op amps. They should be loaded with care, since excessive loading can cause the generated supply voltages to drop causing the RS232 driver output voltages to fall below RS232 requirements. See the graph "Supply Generator Outputs" for a comparison of generated supply voltage versus supply current.



TYPICAL APPLICATION

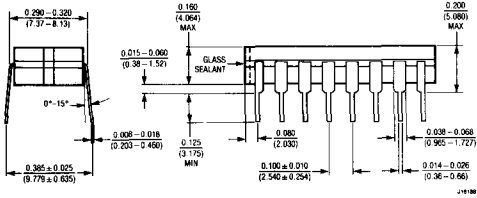
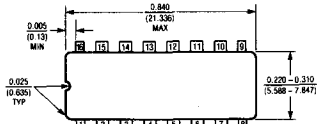
Operating with 5V and 12V



10

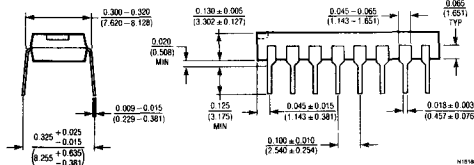
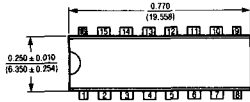
PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

J16 Package Ceramic DIP



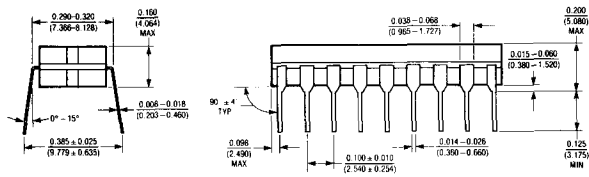
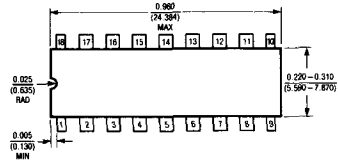
	T _{Jmax}	θ _{JA}	θ _{JC}
LT1081MJ/J	150°C	100°C/W	40°C/W
LT1081CJ	150°C	100°C/W	40°C/W

N16 Package Plastic DIP



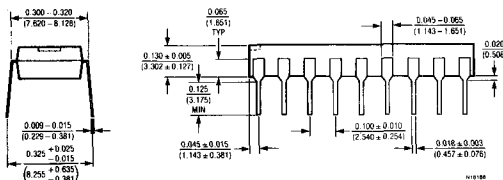
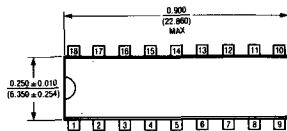
	T _{Jmax}	θ _{JA}	θ _{JC}
LT1081CN/W	125°C	120°C/W	50°C/W

J18 Package Ceramic DIP



	T _{Jmax}	θ _{JA}	θ _{JC}
LT1080MJ/J	150°C	100°C/W	40°C/W
LT1080CJ	150°C	100°C/W	40°C/W

N18 Package Plastic DIP



	T _{Jmax}	θ _{JA}	θ _{JC}
LT1080CN/W	125°C	120°C/W	50°C/W

5V Powered RS232 Driver/ Receiver with Shutdown

FEATURES

- Operates on Single 5V Power Supply
- Generates $\pm 9V$ Supplies with Only $1\mu F$ Capacitors
- Fully Protected Against Output Overloads
- RS232 Outputs can be Forced $\pm 30V$ without Damage
- Three-state Outputs are High Impedance when Off
- Bipolar Circuitry; No Latch Up
- $\pm 30V$ Receiver Input Range
- Can Power Additional RS232 Drivers such as LT1039
- No Supply Current in Shutdown
- Meets All RS232 Specifications
- 16 Pin Version without Shutdown Available

APPLICATIONS

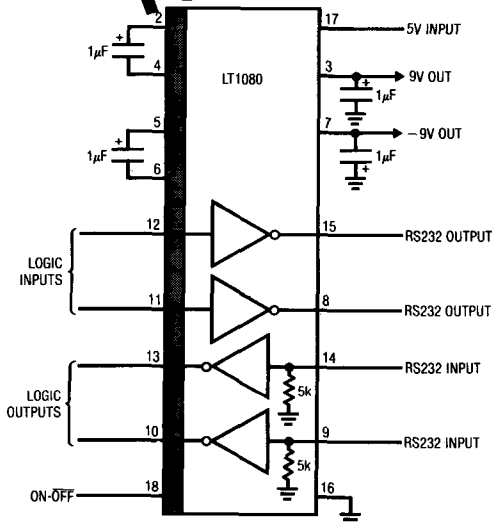
- RS232 Interface
- Battery Powered Systems
- Power Supply Generator
- Terminals
- Modems

DESCRIPTION

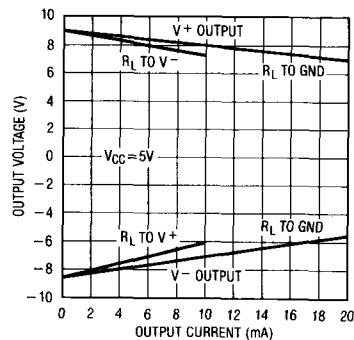
The LT1080 is a dual RS232 driver/receiver which includes a capacitive voltage generator to supply RS232 voltage levels from a single 5V supply. Each receiver will accept up to $\pm 30V$ input and can drive either TTL or CMOS logic. The RS232 drivers accept logic inputs and output RS232 voltage levels. The driver outputs are fully protected against overload and can be shorted to ground or up to $\pm 30V$ without damage. Additionally, when the system is in the SHUTDOWN mode the driver and receiver outputs are at a high impedance allowing data line sharing. Bipolar circuitry makes this driver/receiver exceptionally rugged against overload and short-circuit damage.

The power supply generator doubles the 5V input supply to $\pm 9V$, and then inverts $-9V$ to obtain $-8.5V$. Up to 15mA of external current is available to power additional RS232 drivers or other external circuitry. The SHUTDOWN mode disables the supply generators and reduces input supply current to zero. A version of the LT1080, the LT1081, is available without shutdown for 16 pin applications.

TYPICAL APPLICATION



Supply Generator Outputs



LT1080CS/LT1081CS

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC})	6V
V^+	12V
V^-	-12V
Input Voltage	
Driver	V^- to V^+
Receiver	-30V to 30V
On-Off Pin	GND to 12V
Output Voltage	
Driver	$V^- + 30V$ to $V^+ - 30V$
Receiver	-0.3V to $V_{CC} + 0.3V$
Short Circuit Duration	
V^+	30 Seconds
V^-	30 Seconds
Driver Output	Indefinite
Receiver Output	Indefinite
Operating Temperature Range	
LT1080C	0°C to 70°C
Guaranteed Functional	-25°C to 85°C
Lead Temperature (Soldering, 10 sec.)	300°C

PACKAGE/ORDER INFORMATION

<p>TOP VIEW</p> <p>S18 PACKAGE PLASTIC SOL</p>	ORDER PART NUMBER
	LT1080CS
<p>TOP VIEW</p> <p>S16 PACKAGE PLASTIC SOL</p>	ORDER PART NUMBER
	LT1081CS
	PART MARKING
	LT1080CS
	PART MARKING
	LT1081CS

ELECTRICAL CHARACTERISTICS (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Driver					
Output Voltage Swing	Load = 3k to GND Both Outputs.	5.0 -5.0	7.3 -6.5		V V
Logic Input Voltage Level	Input Low Level ($V_{OUT} = \text{High}$) Input High Level ($V_{OUT} = \text{Low}$)	2.0	1.4 1.4	0.8	V V
Logic Input Current	$V_{IN} \geq 2.0V$ $V_{IN} \leq 0.8V$		5 5	20 20	μA μA
Output Short Circuit Current	Sourcing Current, $V_{OUT} = 0V$ Sinking Current, $V_{OUT} = 0V$	7 -7	12 -12		mA mA
Output Leakage Current	SHUTDOWN (Note 2), $V_{OUT} = \pm 30V$		10	100	μA
Slew Rate	$R_L = 3k\Omega$, $C_L = 51pF$	4	15	30	V/ μs
Receiver					
Input Voltage Thresholds	Input Low Threshold, ($V_{OUT} = \text{High}$) Input High Threshold, ($V_{OUT} = \text{Low}$)	0.2	1.3 1.7	3.0	V V
Hysteresis		0.1	0.4	1.0	V
Input Resistance		3	5	7	k Ω
Output Voltage	Output Low, $I_{OUT} = -1.6mA$ Output High, $I_{OUT} = 160\mu A$ ($V_{CC} = 5V$)	3.5	0.2 4.8	0.4	V V
Output Short Circuit Current	Sinking Current, $V_{OUT} = V_{CC}$ Sourcing Current, $V_{OUT} = 0V$	-10 0.6	-20 1		mA mA
Output Leakage Current	SHUTDOWN (Note 2), $0V \leq V_{OUT} \leq V_{CC}$		1	10	μA

ELECTRICAL CHARACTERISTICS (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply Generator (Note 3)					
V ⁺ Output Voltage	I _{OUT} = 0mA	8	9		V
	I _{OUT} = 10mA	7	8		V
	I _{OUT} = 15mA	6.5	7.5		V
V ⁻ Output Voltage	I _{OUT} = 0mA	-7.5	-8.5		V
	I _{OUT} = -10mA	-5.5	-6.5		V
	I _{OUT} = -15mA	-5	-6		V
Supply Current			10	22	mA
Supply Leakage Current (V _{CC})	SHUTDOWN (Note 2) (LT1080 Only)		1	100	μA
On-Off Pin Current	0V ≤ V _{ON-OFF} ≤ 5V (LT1080 Only)	-15		80	μA
Supply Rise Time	(Note 4)		1		ms

The ● denotes specifications which apply over the operating temperature range (0°C ≤ T_A ≤ 70°C). The LT1080/LT1081 is guaranteed functional by design for -25°C ≤ T_A ≤ 85°C.

Note 1: These parameters apply for 4.5V ≤ V_{CC} ≤ 5.5V and V_{ON-OFF} = 3V, unless otherwise specified.

Note 2: V_{ON-OFF} = 0.4V. (LT1080 only)

Note 3: Unless otherwise specified, V_{CC} = 5V, external loading of V⁺ and V⁻ equals zero and the driver outputs are low (Inputs high).

Note 4: Time from either SHUTDOWN high (LT1080 only) or power on until V⁺ ≥ 6V and V⁻ ≤ -6V. All external capacitors are 1μF.

PIN FUNCTIONS

V_{CC} (Pin 17): Input supply pin. Supply current drops to zero in the SHUTDOWN mode.

GND (Pin 16): Ground pin.

On-Off (Pin 18): Controls the operation mode of the LT1080 and is TTL/CMOS compatible. A logic low puts the device in the SHUTDOWN mode which reduces input supply current to zero and places both driver and receiver outputs in a high impedance state. A logic high fully enables the device.

V⁺ (Pin 3): Positive supply for RS232 drivers. V⁺ ≈ 2V_{CC} - 1.5V. Requires an external capacitor (≥ 1μF) for charge storage. May be loaded (up to 15mA) for external system use. Loading does reduce V⁺ voltage (see graphs.)

V⁻ (Pin 7): Negative supply for RS232 drivers. V⁻ ≈ -(2V_{CC} - 2.5V). Requires an external capacitor (≥ 1μF) for charge storage. May be loaded (up to -15mA) for external system use. Loading does reduce V⁻ voltage (see graphs.)

TR1 IN; TR2 IN (Pins 12, 11): RS232 driver input pins. Inputs are TTL/CMOS compatible. Inputs should not be allowed to float. Tie unused inputs to V_{CC}.

TR1 OUT; TR2 OUT (Pins 15, 8): Driver outputs with RS232 voltage levels. Outputs are in a high impedance state when in the SHUTDOWN mode or when power is off (V_{CC} = 0V) to allow data line sharing. Outputs are fully short circuit protected from V⁻ + 30V to V⁺ - 30V with power on, off, or in the SHUTDOWN mode. Typical output breakdowns are greater than ±45V and higher applied voltages will not damage the device if moderately current limited.

REC1 IN; REC2 IN (Pins 14, 9): Receiver inputs. Accepts RS232 voltage levels (±30V) and has 0.4V of hysteresis to provide noise immunity. Input impedance is nominally 5kΩ.

REC1 OUT; REC2 OUT (Pins 13, 10): Receiver outputs with TTL/CMOS voltage levels. Outputs are in a high impedance state when in the SHUTDOWN mode to allow data line sharing. Outputs are fully short circuit protected to ground or V_{CC} with power on, off, or in the SHUTDOWN mode.

C1 +; C1 -; C2 +; C2 - (Pins 2, 4, 5, 6): No user applications. Requires an external capacitor (≥ 1μF) from C1 + to C1 - and another from C2 + to C2 -.

10

NOTES

Advanced Low Power 5V RS232 Drivers/Receivers with Charge Pump

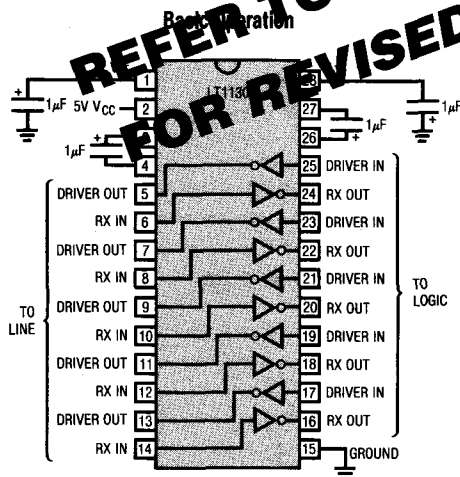
FEATURES

- Absolutely No Latchup
- CMOS Comparable Low Power — 80mW
- Operates from a **Single 5V Supply**
- **Superior to CMOS**
 - **Easy PC Layout** — Flow Through Architecture
 - Improved Speed — Operates Over 64K Baud
 - Improved Protection — Outputs Can be Forced to $\pm 30V$ Without Damage
 - Three-State Outputs are High Impedance When Off
 - Only Needs $1\mu F$ Capacitors
 - Output Overvoltage Does Not Force Current Back Into Supplies
- $1\mu A$ Supply Current in Shutdown
- Available in SO Package

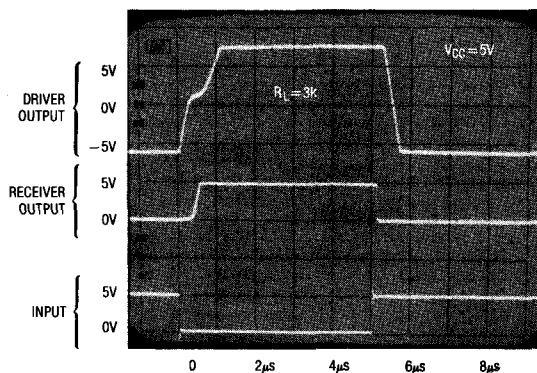
DESCRIPTION

The LT1130 Series are the only RS232 drivers/receivers with charge pump to guarantee absolutely no latchup. These interface optimized devices provide a realistic balance between CMOS levels of power dissipation and real world requirements for ruggedness. The driver outputs are fully protected against overload and can be shorted to $\pm 30V$. Unlike CMOS, the advanced architecture of the LT1130 does not load the signal line when "shut down" or when power is off. Both the receiver and RS232 outputs are put into a high impedance state. An advanced output stage allows driving higher capacitance loads at higher speeds with exceptional efficiency.

For applications requiring only 2 drivers and 2 receivers with charge pump in one package see the LT1180 Series data sheet. All of Linear Technology's RS232 IC's are available in standard surface mount packages.



Output Waveform



LT1130 5-Driver/5-Receiver RS232 Transceiver
 LT1131 5-Driver/4-Receiver RS232 Transceiver w/Shutdown
 LT1132 5-Driver/3-Receiver RS232 Transceiver
 LT1133 3-Driver/5-Receiver RS232 Transceiver
 LT1134 4-Driver/4-Receiver RS232 Transceiver
 LT1135 5-Driver/3-Receiver RS232 Transceiver w/o Charge Pump

LT1136 4-Driver/5-Receiver RS232 Transceiver w/Shutdown
 LT1137 3-Driver/5-Receiver RS232 Transceiver w/Shutdown
 LT1138 5-Driver/3-Receiver RS232 Transceiver w/Shutdown
 LT1139 4-Driver/4-Receiver RS232 Transceiver w/Shutdown
 LT1140 5-Driver/3-Receiver RS232 Transceiver w/o Charge Pump
 LT1141 3-Driver/5-Receiver RS232 Transceiver w/o Charge Pump

LT1130 Series

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V _{cc})	6V
V ⁺	13.2V
V ⁻	-13.2V
Input Voltage	
Driver	V ⁻ to V ⁺
Receiver	-30V to 30V
On-Off Pin	GND to 12V
Output Voltage	
Driver	V ⁻ + 30V to V ⁺ - 30V
Receiver	-0.3V to V _{cc} + 0.3V

Short Circuit Duration	
V ⁺	30 Seconds
V ⁻	30 Seconds
Driver Output	Indefinite
Receiver Output	Indefinite
Operating Temperature Range	
Military (LT113XM/LT114XM)	-55°C to 125°C
Industrial (LT113XI/LT114XI)	-40°C to 85°C
Commercial (LT113XC/LT114XC)	0°C to 70°C

PRODUCT SELECTION TABLE

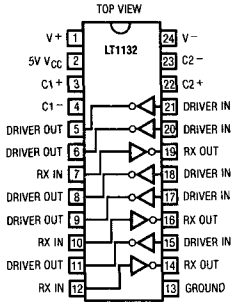
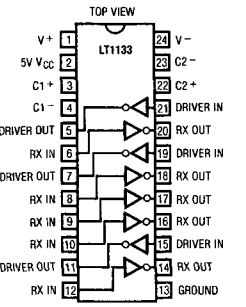
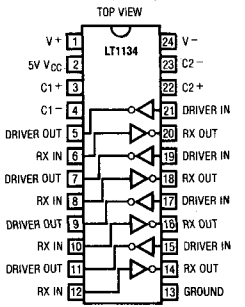
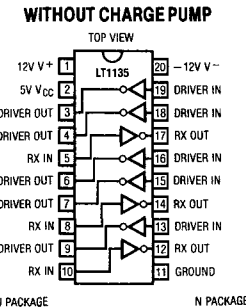
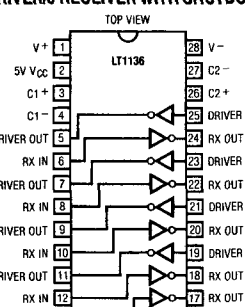
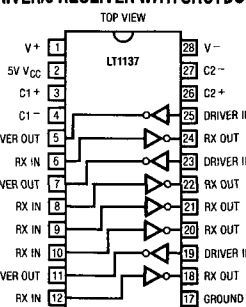
Part Number	Power Supply Voltages*	Shutdown	Drivers	Receivers	External Components
LT1130	+5	No	5	5	4 Capacitors
LT1131	+5	Yes	5	4	4 Capacitors
LT1132	+5	No	5	3	4 Capacitors
LT1133	+5	No	3	5	4 Capacitors
LT1134	+5	No	4	4	4 Capacitors
LT1135	+5, +12, -12	No	5	3	None
LT1136	+5	Yes	4	5	4 Capacitors
LT1137	+5	Yes	3	5	4 Capacitors
LT1138	+5	Yes	5	3	4 Capacitors
LT1139	+5, +12	Yes	4	4	2 Capacitors
LT1140	+5, +12, -12	Yes	5	3	None
LT1141	+5, +12, -12	Yes	3	5	None

*The LT1130, LT1131, LT1132, LT1133, LT1134, LT1136, LT1137, and LT1138 can operate with +5V and +12V supplies and two external capacitors.

PACKAGE/ORDER INFORMATION

5-DRIVER/5-RECEIVER		ORDER PART NUMBER	5-DRIVER/4-RECEIVER WITH SHUTDOWN		ORDER PART NUMBER		
		LT1130MJ LT1130CJ LT1130CN LT1130IJ LT1130IN LT1130CS			LT1131MJ LT1131CJ LT1131CN LT1131IJ LT1131IN LT1131CS		
J PACKAGE 28-LEAD CERAMIC DIP (.600" WIDE)	S PACKAGE 28-LEAD PLASTIC SOL. (.600" WIDE)		N PACKAGE 28-LEAD PLASTIC DIP (.600" WIDE)	J PACKAGE 28-LEAD CERAMIC DIP (.600" WIDE)		S PACKAGE 28-LEAD PLASTIC SOL. (.600" WIDE)	N PACKAGE 28-LEAD PLASTIC DIP (.600" WIDE)

PACKAGE/ORDER INFORMATION

<p>5-DRIVER/3-RECEIVER</p> <p>TOP VIEW</p>  <p>J PACKAGE 24-LEAD CERAMIC DIP (.300" WIDE)</p> <p>N PACKAGE 24-LEAD PLASTIC DIP (.300" WIDE)</p> <p>S PACKAGE 24-LEAD PLASTIC SOL (.300" WIDE)</p>	<p>ORDER PART NUMBER</p> <p>LT1132MJ LT1132CJ LT1132CN LT1132IJ LT1132IN LT1132CS</p>	<p>3-DRIVER/5-RECEIVER</p> <p>TOP VIEW</p>  <p>J PACKAGE 24-LEAD CERAMIC DIP (.300" WIDE)</p> <p>N PACKAGE 24-LEAD PLASTIC DIP (.300" WIDE)</p> <p>S PACKAGE 24-LEAD PLASTIC SOL (.300" WIDE)</p>	<p>ORDER PART NUMBER</p> <p>LT1133MJ LT1133CJ LT1133CN LT1133IJ LT1133IN LT1133CS</p>
<p>4-DRIVER/4-RECEIVER</p> <p>TOP VIEW</p>  <p>J PACKAGE 24-LEAD CERAMIC DIP (.300" WIDE)</p> <p>N PACKAGE 24-LEAD PLASTIC DIP (.300" WIDE)</p> <p>S PACKAGE 24-LEAD PLASTIC SOL (.300" WIDE)</p>	<p>LT1134MJ LT1134CJ LT1134CN LT1134IJ LT1134IN LT1134CS</p>	<p>5-DRIVER/3-RECEIVER WITHOUT CHARGE PUMP</p> <p>TOP VIEW</p>  <p>J PACKAGE 20-LEAD CERAMIC DIP (.300" WIDE)</p> <p>N PACKAGE 20-LEAD PLASTIC DIP (.300" WIDE)</p> <p>S PACKAGE 20-LEAD PLASTIC SOL (.300" WIDE)</p>	<p>LT1135MJ LT1135CJ LT1135CN LT1135IJ LT1135IN LT1135CS</p>
<p>4-DRIVER/5-RECEIVER WITH SHUTDOWN</p> <p>TOP VIEW</p>  <p>J PACKAGE 28-LEAD CERAMIC DIP (.600" WIDE)</p> <p>N PACKAGE 28-LEAD PLASTIC DIP (.600" WIDE)</p> <p>S PACKAGE 28-LEAD PLASTIC SOL (.600" WIDE)</p>	<p>LT1136MJ LT1136CJ LT1136CN LT1136IJ LT1136IN LT1136CS</p>	<p>3-DRIVER/5-RECEIVER WITH SHUTDOWN</p> <p>TOP VIEW</p>  <p>J PACKAGE 28-LEAD CERAMIC DIP (.600" WIDE)</p> <p>N PACKAGE 28-LEAD PLASTIC DIP (.600" WIDE)</p> <p>S PACKAGE 28-LEAD PLASTIC SOL (.600" WIDE)</p>	<p>LT1137MJ LT1137CJ LT1137CN LT1137IJ LT1137IN LT1137CS</p>

10

PACKAGE/ORDER INFORMATION

<p>5-DRIVER/3-RECEIVER WITH SHUTDOWN</p> <p>J PACKAGE 28-LEAD CERAMIC DIP (.600" WIDE)</p> <p>S PACKAGE 28-LEAD PLASTIC SOL (.600" WIDE)</p> <p>N PACKAGE 28-LEAD PLASTIC DIP (.600" WIDE)</p>	<p>ORDER PART NUMBER</p> <p>LT1138MJ LT1138CJ LT1138CN LT1138IJ LT1138IN LT1138CS</p>	<p>4-DRIVER/4-RECEIVER WITH SHUTDOWN WITH +12V AND +5V SUPPLIES</p> <p>J PACKAGE 24-LEAD CERAMIC DIP (.300" WIDE)</p> <p>S PACKAGE 24-LEAD PLASTIC SOL (.300" WIDE)</p> <p>N PACKAGE 24-LEAD PLASTIC DIP (.300" WIDE)</p>	<p>ORDER PART NUMBER</p> <p>LT1139MJ LT1139CJ LT1139CN LT1139IJ LT1139IN LT1139CS</p>
<p>5-DRIVER/3-RECEIVER WITHOUT CHARGE PUMP</p> <p>J PACKAGE 24-LEAD CERAMIC DIP (.300" WIDE)</p> <p>S PACKAGE 24-LEAD PLASTIC SOL (.300" WIDE)</p> <p>N PACKAGE 24-LEAD PLASTIC DIP (.300" WIDE)</p>	<p>LT1140MJ LT1140CJ LT1140CN LT1140IJ LT1140IN LT1140CS</p>	<p>3-DRIVER/5-RECEIVER WITHOUT CHARGE PUMP</p> <p>J PACKAGE 24-LEAD CERAMIC DIP (.300" WIDE)</p> <p>S PACKAGE 24-LEAD PLASTIC SOL (.300" WIDE)</p> <p>N PACKAGE 24-LEAD PLASTIC DIP (.300" WIDE)</p>	<p>LT1141MJ LT1141CJ LT1141CN LT1141IJ LT1141IN LT1141CS</p>

For 2-Driver/2-Receiver devices, see LT1080/81 and LT1180/81 data sheet.

ELECTRICAL CHARACTERISTICS (Note 1)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Any Driver						
Output Voltage Swing	Load = 3k to GND	Positive Negative	● ●	5.0 -5.0	7.3 -6.5	V V
Logic Input Voltage Level	Input Low Level ($V_{OUT} = \text{High}$) Input High Level ($V_{OUT} = \text{Low}$)		● ●	2.0	1.4 1.4	V V
Logic Input Current	$0.8V \leq V_{IN} \leq 2.0V$		●	5	20	μA
Output Short Circuit Current	$V_{OUT} = 0V$			12		mA
Output Leakage Current	SHUTDOWN (Note 2), $V_{OUT} = \pm 30V$ (Note 3)		●	10	100	μA
Slew Rate	$R_L = 3k\Omega$, $C_L = 51\text{pF}$			4	15	V/ μs

ELECTRICAL CHARACTERISTICS (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Any Receiver					
Input Voltage Thresholds	Input Low Threshold, ($V_{OUT} = \text{High}$) Input High Threshold, ($V_{OUT} = \text{Low}$)	0.8	1.3 1.7	2.4	V
Hysteresis		● 0.1	0.4	1.0	V
Input Resistance		3	5	7	kΩ
Output Voltage	Output Low, $I_{OUT} = -1.6\text{mA}$ Output High, $I_{OUT} = 160\mu\text{A}$ ($V_{CC} = 5\text{V}$)	● 3.5	0.2 4.8	0.4	V
Output Short Circuit Current	Sinking Current, $V_{OUT} = V_{CC}$ Sourcing Current, $V_{OUT} = 0\text{V}$	-10 0.4	-20 1		mA
Output Leakage Current	SHUTDOWN (Note 2), $0\text{V} \leq V_{OUT} \leq V_{CC}$	●	1	10	μA
Power Supply Generator					
V ⁺ Output			8		V
V ⁻ Output			-7.5		V
Supply Current			17	27	mA
Supply Leakage Current	SHUTDOWN, $-55^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$ SHUTDOWN, $0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$	●	1	100	μA
Supply Rise Time	SHUTDOWN To Turn On		2		ms
On/Off Pin Current	SHUTDOWN, $0\text{V} \leq V_{ON/OFF} \leq 5\text{V}$	●	-15	80	μA

The ● denotes the specifications which apply over the full operating temperature range. ($0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$ for commercial grade, $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ for industrial grade, and $-55^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$ for military grade).

Note 1: Testing done at $V_{CC} = 5\text{V}$ and $V_{ON/OFF} = 3\text{V}$

Note 2: $V_{ON/OFF} \leq 0.1\text{V}$

Note 3: For LT1139, 40, and 41 with 12V supplies, V_{OUT} leakage is $200\mu\text{A}$ and V_{OUT} is forced to $\pm 25\text{V}$.

PIN FUNCTIONS

V_{CC}: Input supply pin. Supply current drops to zero in the SHUTDOWN mode.

GND: Ground pin.

On/Off: Controls the operation mode of the device and is TTL/CMOS compatible. A logic low puts the device in the SHUTDOWN mode which reduces input supply current to zero and places both driver and receiver outputs in a high impedance state. A logic high fully enables the device.

V⁺: Positive supply (RS232 drivers). $V^+ \approx 2V_{CC} - 1.5\text{V}$. Requires an external capacitor ($\geq 1\mu\text{F}$) for charge storage. Capacitor may be tied to ground or +5V input supply. V⁺ voltage is short circuit proof for 30 seconds. With multiple transceivers, the V⁺ and V⁻ pins may be paralleled into common capacitors.

V⁻: Negative supply (RS232 drivers). $V^- \approx -(2V_{CC} - 2.5\text{V})$. Requires an external capacitor ($\geq 1\mu\text{F}$) for charge storage.

Loading does reduce V⁻ voltage. V⁻ is short circuit proof for 30 seconds. With multiple transceivers, the V⁺ and V⁻ pins may be paralleled into common capacitors.

DRIVER IN: RS232 driver input pins. Inputs are TTL/CMOS compatible. Inputs should not be allowed to float. Tie unused inputs to V_{CC}.

DRIVER OUT: Driver outputs with RS232 voltage levels. Outputs are in a high impedance state when in the SHUTDOWN mode or when power is off ($V_{CC} = 0\text{V}$) to allow data line sharing. Outputs are fully short circuit protected from V⁻ + 30V to V⁺ - 30V with power on, off, or in the SHUTDOWN mode. Typical output breakdowns are greater than $\pm 45\text{V}$ and higher applied voltages will not damage the device if moderately current limited. Although the outputs are protected, short circuits on one output can load the power supply generators disrupting the signal level from other outputs.

10

LT1130 Series

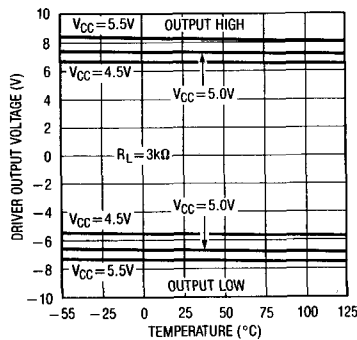
RX IN: Receiver inputs. Accepts RS232 voltage levels ($\pm 30V$) and has 0.4V of hysteresis to provide noise immunity. Input impedance is nominally 5k Ω .

RX OUT: Receiver outputs with TTL/CMOS voltage levels. Outputs are in a high impedance state when in the SHUT-DOWN mode to allow data line sharing. Outputs are fully short circuit protected to ground or V_{CC} with power on, off, or in the SHUTDOWN mode.

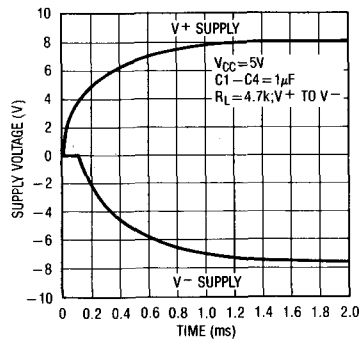
C1 +; C1 -; C2 +; C2 -: Requires an external capacitor ($\geq 1\mu F$) from C1 + to C1 - and another from C2 + to C2 -. In applications where larger positive voltages are available, such as +12V, C1 can be eliminated and the positive voltage connected directly to the C1 + terminal.

TYPICAL PERFORMANCE CHARACTERISTICS

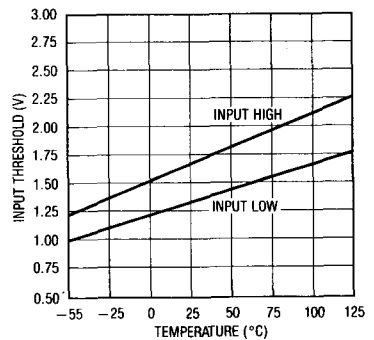
Driver Output Voltage



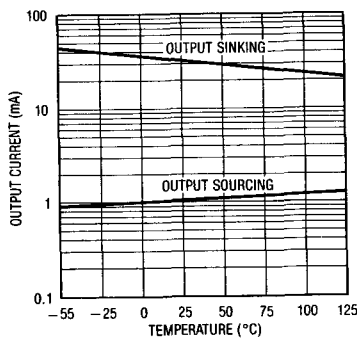
Supply Generation from V_{CC} or Shutdown



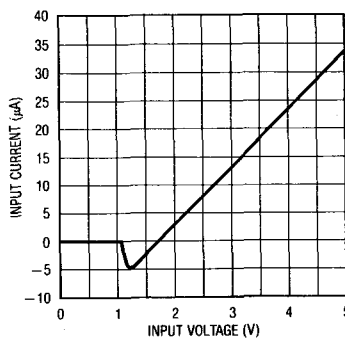
Receiver Input Thresholds



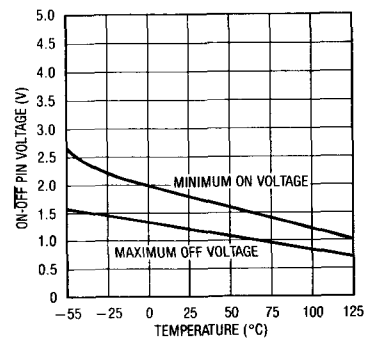
Receiver Output Short Circuit Current



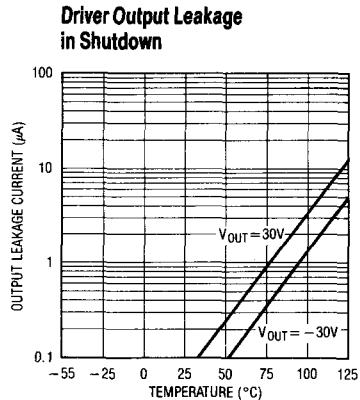
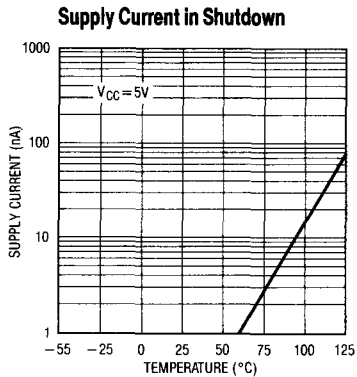
On-Off Pin Current vs Voltage



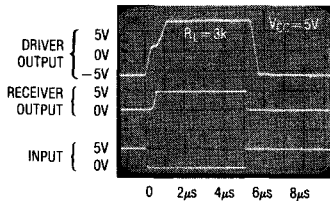
On-Off Pin Thresholds



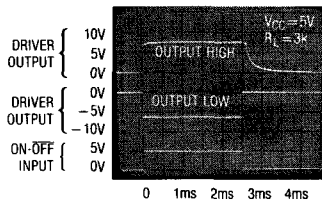
TYPICAL PERFORMANCE CHARACTERISTICS



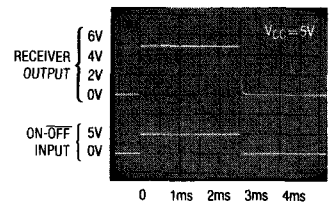
Output Waveforms



Shutdown to Driver Output



Shutdown to Receiver Output



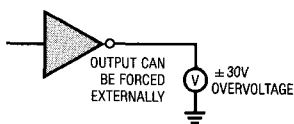
APPLICATION HINTS

The driver output stage of the LT1130 offers significantly improved protection over older bipolar and CMOS designs. In addition to current limiting, the driver output can be externally forced to $\pm 30V$ with no damage or excessive cur-

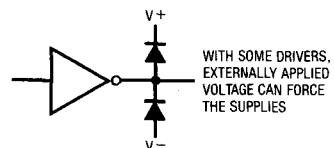
rent flow, and will not disrupt the supplies. Some drivers have diodes connected between the outputs and the supplies, so externally applied voltages can cause excessive supply voltage to develop.

10

LT1130 Driver



Older RS232 Drivers and CMOS Drivers

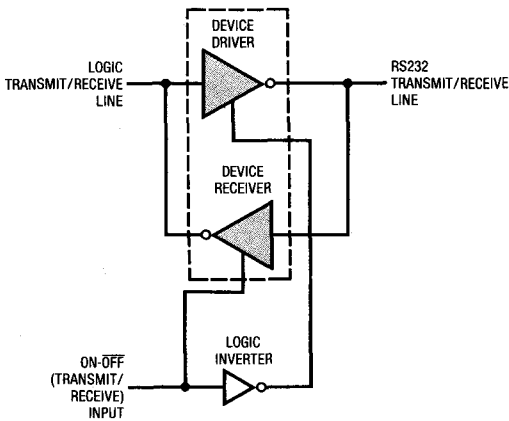


APPLICATION HINTS

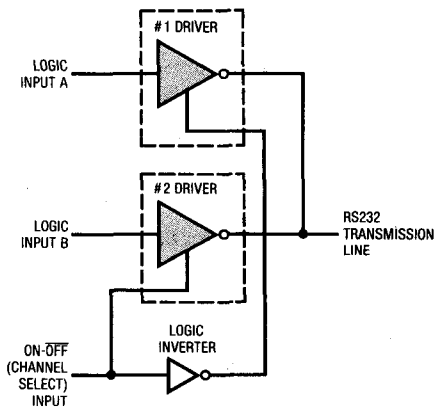
Placing the LT1130 type device in the SHUTDOWN mode puts both the driver and receiver outputs in a high impedance state. This allows data line sharing and transceiver applications.

The SHUTDOWN mode also drops input supply current to zero for power-conscious systems.

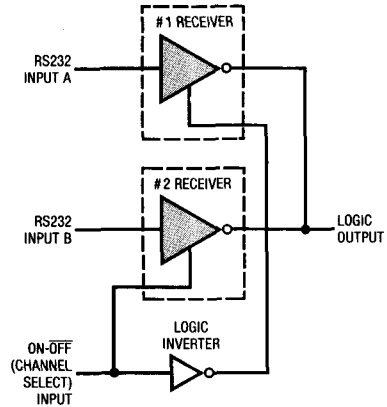
Transceiver



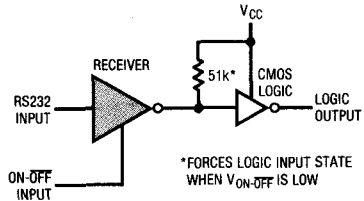
Sharing a Receiver Line



Sharing a Transmitter Line

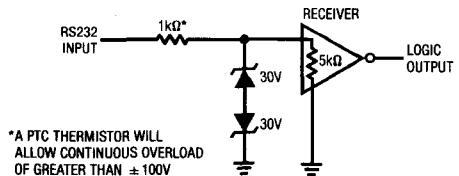


When driving CMOS logic from a receiver that will be used in the SHUTDOWN mode and there is no other active receiver on the line, a 51k resistor can be placed from the logic input to V_{CC} to force a definite logic level when the receiver output is in a high impedance state.



*FORCES LOGIC INPUT STATE WHEN V_{ON-OFF} IS LOW

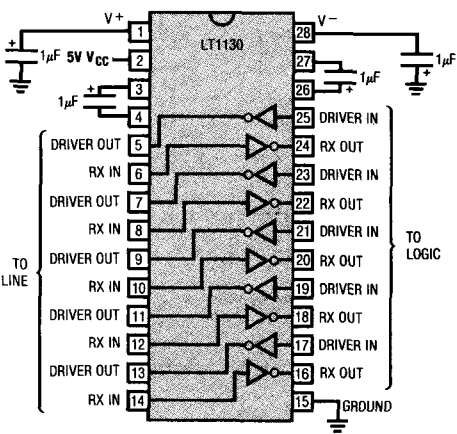
To protect against receiver input overloads in excess of $\pm 30V$, a voltage clamp can be placed on the data line and still maintain RS232 compatibility.



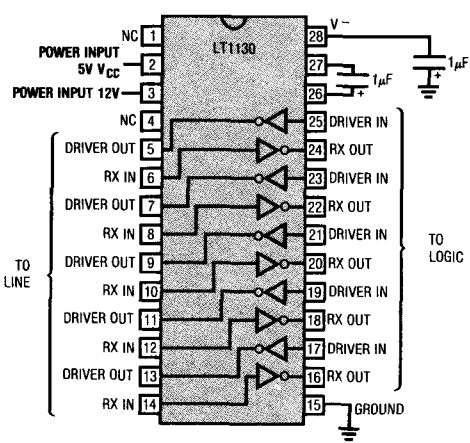
*A PTC THERMISTOR WILL ALLOW CONTINUOUS OVERLOAD OF GREATER THAN $\pm 100V$

TYPICAL APPLICATIONS

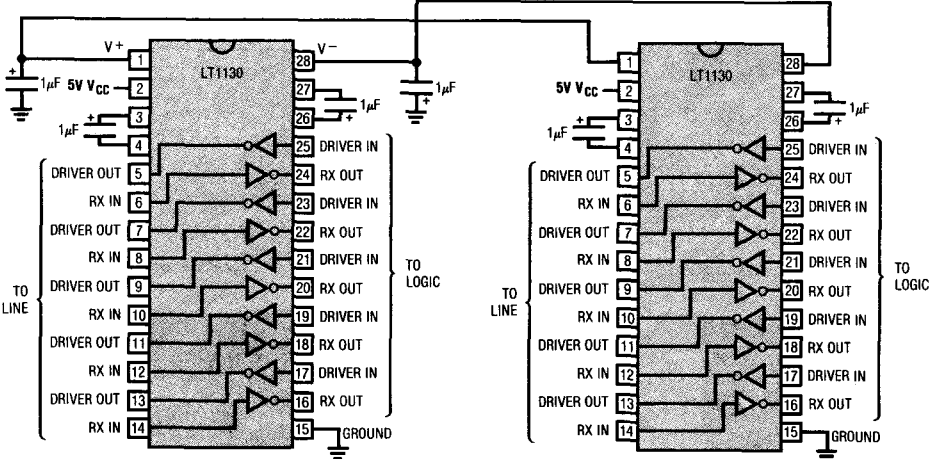
Basic Operation



Operating with +5V and +12V Supplies

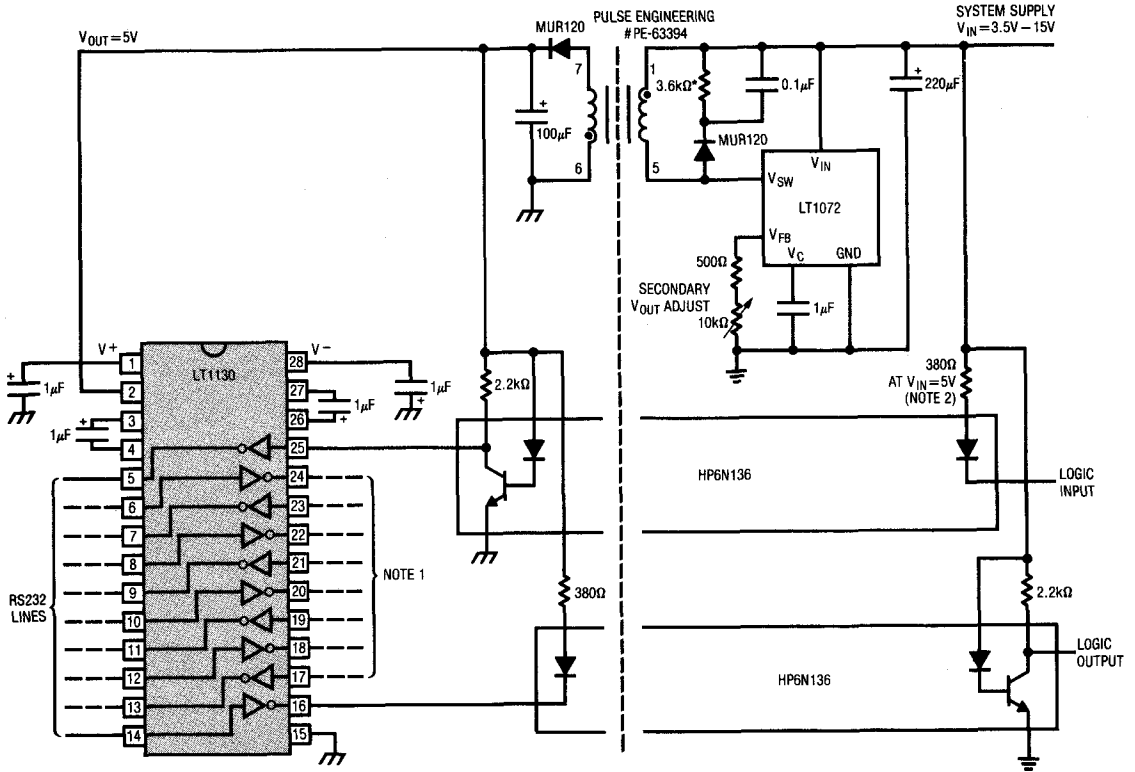


Paralleling Power Supply Generator with Common Storage Capacitors



10

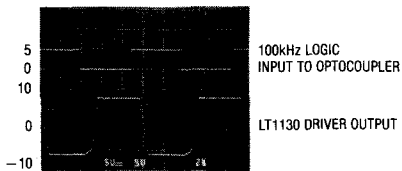
2500V Isolated 5-Driver/5-Receiver RS232 Transceiver



⏏ = SYSTEM GROUND
⏏ = FLOATING COMMON

NOTE 1: REPEAT THE OPTOCOUPLER CONNECTIONS FOR EACH LINE.
NOTE 2: SELECT FOR 10mA THROUGH LED.
*FOR IMPROVED EFFICIENCY, REPLACE THE 3.6kΩ RESISTOR WITH A 30V ZENER DIODE.

RS232 Driver Signals



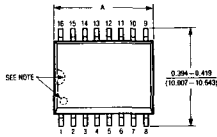
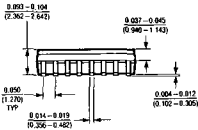
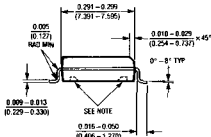
RS232 Receiver Signals



PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

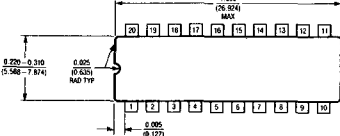
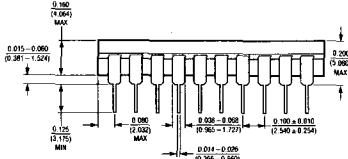
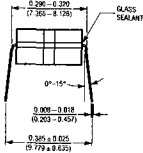
S Package
20, 24- and 28-Lead Plastic SOL
(.300" / 7.620" Wide)

NO. OF LEADS	A DIM.
18	0.215 - 0.415 (5.413 - 10.541)
18	0.432 - 0.416 (11.038 - 10.538)
20	0.450 - 0.215 (11.578 - 5.413)
24	0.450 - 0.415 (11.578 - 10.531)
28	0.730 - 0.715 (18.780 - 18.193)

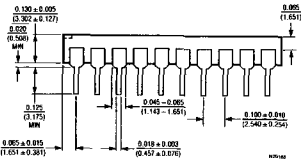
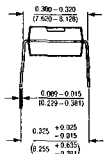


NOTE:
 PIN 1 CENTER MOTION ON TOP AND CARRIES ON THE BOTTOM OF PACKAGE ARE THE MARKING LOCATIONS. THE PART MAY BE SUPPLIED WITH OR WITHOUT ANY OF THE OPTIONS.

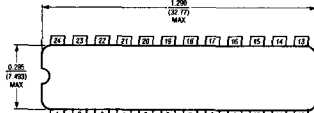
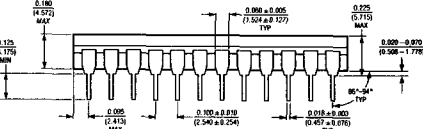
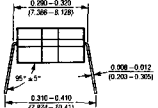
J Package
20-Lead Ceramic DIP
(.300" Wide)



N Package
20-Lead Plastic DIP
(.300" Wide)



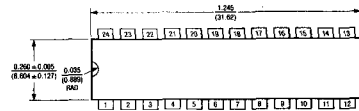
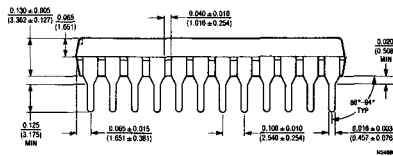
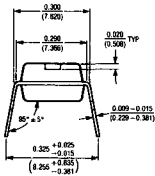
J Package
24-Lead Ceramic DIP
(.300" Wide)



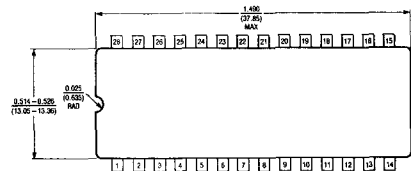
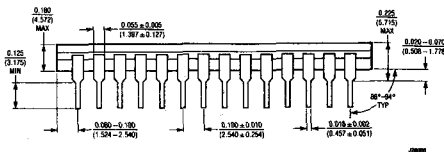
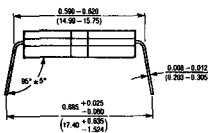
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PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

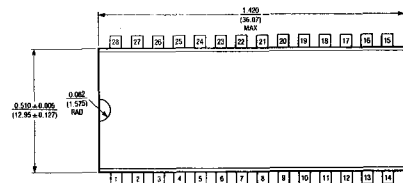
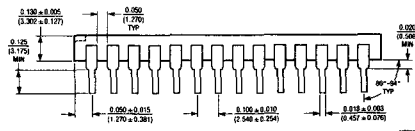
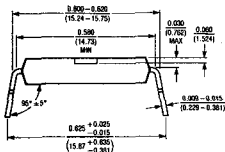
**N Package
24-Lead Plastic DIP
(.300" Wide)**



**J Package
28-Lead Ceramic DIP
(.600" Wide)**



**N Package
28-Lead Plastic DIP
(.600" Wide)**



Advanced Low Power 5V RS232 Dual Driver/Receiver with Small Capacitors

FEATURES

- 0.1 μ F Capacitors
- Absolutely No Latchup
- CMOS Comparable Low Power — 70mW
- **Superior to CMOS**
 - Improved Speed — Operates Over 64K Baud
 - Improved Protection — Outputs Can be Forced to $\pm 30V$ Without Damage
 - Three-State Outputs are High Impedance When Off
 - Smaller Board Area Required
- 1 μ A Supply Current in Shutdown
- Available in SO Package
- Available With or Without Shutdown

APPLICATIONS

- Portable Computers
- Battery Powered RS232 Systems
- Power Supply Converter
- Terminals
- Modems

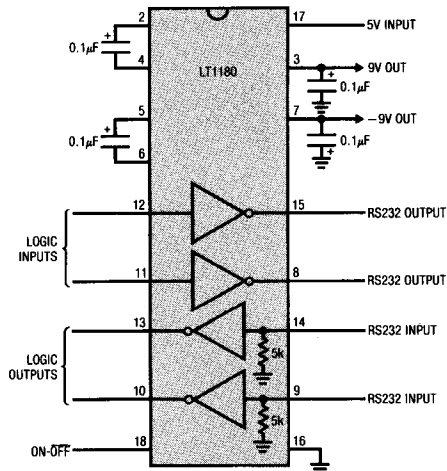
DESCRIPTION

The LT1180 and LT1181 are the only dual RS232 driver/receiver with charge pump to guarantee absolutely no latchup. Requiring only 0.1 μ F charge pump capacitors, these interface optimized devices provide a realistic balance between CMOS levels of power dissipation and real world requirements for ruggedness. Small capacitors reduce cost as well as board size. The driver outputs are fully protected against overload and can be shorted to $\pm 30V$. Unlike CMOS, the advanced architecture of the LT1180/LT1181 does not load the signal line when "shut down" or when power is off from the receiver and RS232 outputs are protected high impedance state. An advanced output structure allows driving large capacitive loads at higher speeds with exceptional ruggedness against ESD.

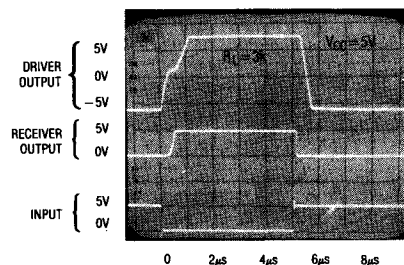
For applications requiring up to 5 drivers and 5 receivers with charge pump in one package see the LT1130 Series data sheet. A version of the LT1180/81, the LT1080 and LT1081 is available for applications requiring extra current from the charge pump to power other circuitry. All of Linear Technology's RS232 IC's are available in standard surface mount packages.

 REFER TO TABLE OF CONTENTS
 FOR REVISED DATA LOCATION

TYPICAL APPLICATION



Output Waveforms



ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC}) 6V
 V₊ 13.2V
 V₋ -13.2V
 Input Voltage
 Driver V₋ to V₊
 Receiver -30V to 30V
 On-Off Pin GND to 12V
 Output Voltage
 Driver V₋ + 30V to V₊ - 30V
 Receiver -0.3V to V_{CC} + 0.3V

Short Circuit Duration
 V₊30 Seconds
 V₋30 Seconds
 Driver Output Indefinite
 Receiver Output Indefinite
 Operating Temperature Range
 LT1180M/LT1181M -55°C to 125°C
 LT1180I/LT1181I -40°C to 85°C
 LT1180C/LT1181C 0°C to 70°C
 Lead Temperature (Soldering, 10 sec.) 300°C

PACKAGE/ORDER INFORMATION

<p>TOP VIEW</p> <p>J PACKAGE 18-LEAD CERAMIC DIP</p> <p>N PACKAGE 18-LEAD PLASTIC DIP</p>	<p>ORDER PART NUMBER</p> <p>LT1180MJ LT1180IJ LT1180IN LT1180CJ LT1180CN</p>	<p>TOP VIEW</p> <p>S PACKAGE 18-LEAD PLASTIC SOL</p>	<p>ORDER PART NUMBER</p> <p>LT1180IS LT1180CS</p>
<p>TOP VIEW</p> <p>J PACKAGE 16-LEAD CERAMIC DIP</p> <p>N PACKAGE 16-LEAD PLASTIC DIP</p>	<p>LT1181MJ LT1181IJ LT1181IN LT1181CJ LT1181CN</p>	<p>TOP VIEW</p> <p>S PACKAGE 16-LEAD PLASTIC SOL</p>	<p>LT1181IS LT1181CS</p>

ELECTRICAL CHARACTERISTICS (Note 1)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS	
Driver							
Output Voltage Swing	Load = 3k to GND Both Outputs.	Positive	5.0	7.3		V	
		Negative	-5.0	-6.5		V	
Logic Input Voltage Level	Input Low Level ($V_{OUT} = \text{High}$)	●		1.4	0.8	V	
	Input High Level ($V_{OUT} = \text{Low}$)	●	2.0	1.4		V	
Logic Input Current	$V_{IN} \geq 2.0V$	●		5	20	μA	
	$V_{IN} \leq 0.8V$	●		5	20	μA	
Output Short Circuit Current	Sourcing Current, $V_{OUT} = 0V$		7	12		mA	
	Sinking Current, $V_{OUT} = 0V$		-7	-12		mA	
Output Leakage Current	SHUTDOWN (Note 2), $V_{OUT} = \pm 30V$	●		10	100	μA	
Slew Rate	$R_L = 3k\Omega$, $C_L = 51pF$		4	15	30	V/ μs	
Receiver							
Input Voltage Thresholds	Input Low Threshold, LT1180C, LT1181C LT1180I, M/LT1181I, M	●	0.8	1.3		V	
		●	0.2	1.3		V	
	Input High Threshold, LT1180C/LT1181C LT1180I, M/LT1181I, M	●		1.7	2.4		V
		●		1.7	3.0		V
Hysteresis		0.1	0.4	1.0	V		
Input Resistance			3	5	7	k Ω	
Output Voltage	Output Low, $I_{OUT} = -1.6mA$ Output High, $I_{OUT} = 160\mu A$ ($V_{CC} = 5V$)	●		0.2	0.4	V	
		●	3.5	4.8		V	
Output Short Circuit Current	Sinking Current, $V_{OUT} = V_{CC}$		-10	-20		mA	
	Sourcing Current, $V_{OUT} = 0V$		0.6	1		mA	
Output Leakage Current	SHUTDOWN (Note 2), $0V \leq V_{OUT} \leq V_{CC}$	●		1	10	μA	
Supply Current	(Note 3) $T_A = 125^\circ C$	●		14	23	mA	
		●			30	mA	
Supply Leakage Current (V_{CC})	SHUTDOWN (Note 2) (LT1180 Only)	●		1	100	μA	
On-Off Pin Current	$0V \leq V_{ON-OFF} \leq 5V$ (LT1180 Only)	●	-15		80	μA	

The ● denotes specifications which apply over the operating temperature range ($0^\circ C \leq T_A \leq 70^\circ C$ for commercial grade, $-40^\circ C \leq T_A \leq 85^\circ C$ for industrial grade or $-55^\circ C \leq T_A \leq 125^\circ C$ for military grade devices).

Note 1: These parameters apply for $V_{ON-OFF} = 3V$, $V_{CC} = 5V$ and $C = 0.1\mu F$ unless otherwise specified.

Note 2: $V_{ON-OFF} = 0.4V$ for $-55^\circ C \leq T_A \leq 100^\circ C$, and $V_{ON-OFF} = 0.2V$ for $100^\circ C \leq T_A \leq 125^\circ C$ (LT1180 only).

Note 3: Unless otherwise specified, $V_{CC} = 5V$, external loading of V^+ and V^- equals zero and the driver outputs are low (inputs high).

PIN FUNCTIONS (Pin numbers refer to LT1180)

V_{CC} (Pin 17): Input supply pin. Supply current drops to zero in the SHUTDOWN mode.

GND (Pin 16): Ground pin.

On-Off (Pin 18): Controls the operation mode of the LT1180 and is TTL/CMOS compatible. A logic low puts the device in the SHUTDOWN mode which reduces input supply current to zero and places both driver and receiver outputs in a high impedance state. A logic high fully enables the device.

V+ (Pin 3): Positive supply for RS232 drivers. $V+ \approx 2V_{CC} - 1.5V$. Requires an external capacitor ($\geq 0.1\mu F$) for charge storage. Capacitor may be tied to ground or +5V input supply. With multiple transceivers, the V+ and V- pins may be paralleled into common capacitors.

V- (Pin 7): Negative supply for RS232 drivers. $V- \approx -(2V_{CC} - 2.5V)$. Requires an external capacitor ($\geq 0.1\mu F$) for charge storage. With multiple transceivers, the V+ and V- pins may be paralleled into common capacitors.

TR1 IN; TR2 IN (Pins 12, 11): RS232 driver input pins. Inputs are TTL/CMOS compatible. Inputs should not be allowed to float. Tie unused inputs to V_{CC}.

TR1 OUT; TR2 OUT (Pins 15, 8): Driver outputs with RS232 voltage levels. Outputs are in a high impedance state when in the SHUTDOWN mode or when power is off ($V_{CC}=0V$) to allow data line sharing. Outputs are fully short circuit protected from $V- + 30V$ to $V+ - 30V$ with power on, off, or in the SHUTDOWN mode. Typical output breakdowns are greater than $\pm 45V$ and higher applied voltages will not damage the device if moderately current limited. Shorting one output will affect output from the other.

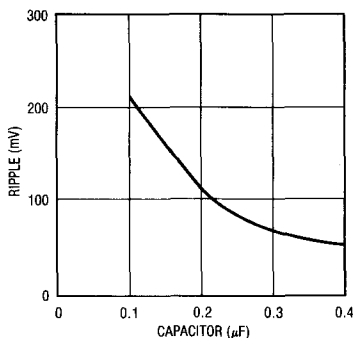
REC1 IN; REC2 IN (Pins 14, 9): Receiver inputs. Accepts RS232 voltage levels ($\pm 30V$) and has 0.4V of hysteresis to provide noise immunity. Input impedance is nominally 5k Ω .

REC1 OUT; REC2 OUT (Pins 13, 10): Receiver outputs with TTL/CMOS voltage levels. Outputs are in a high impedance state when in the SHUTDOWN mode to allow data line sharing. Outputs are fully short circuit protected to ground or V_{CC} with power on, off, or in the SHUTDOWN mode.

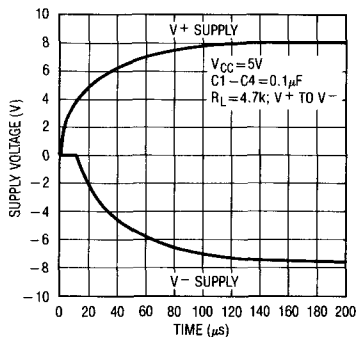
C1+; C1-; C2+; C2- (Pins 2, 4, 5, 6): Requires an external capacitor ($\geq 0.1\mu F$) from C1+ to C1- and another from C2+ to C2-. Pin 2 can be used for connecting a second positive supply. When a separate positive supply is used, C1 can be deleted.

TYPICAL PERFORMANCE CHARACTERISTICS

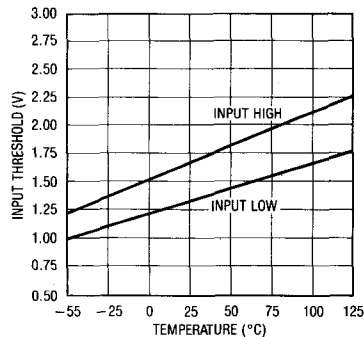
Supply Ripple vs Capacitor



Supply Generation from V_{CC} or Shutdown

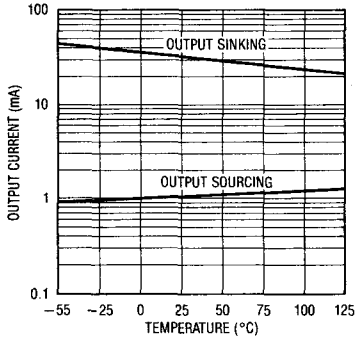


Receiver Input Thresholds

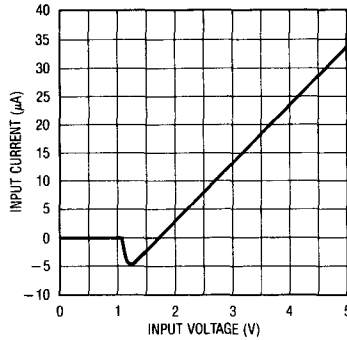


TYPICAL PERFORMANCE CHARACTERISTICS

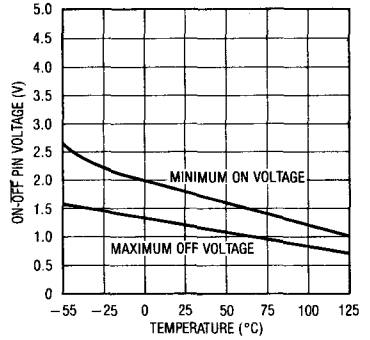
Receiver Output Short Circuit Current



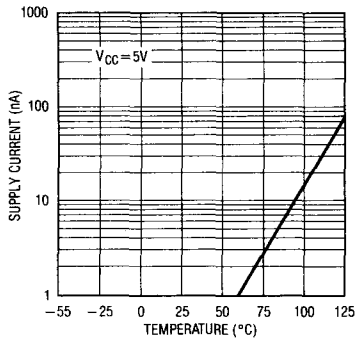
On-Off Pin Current vs Voltage



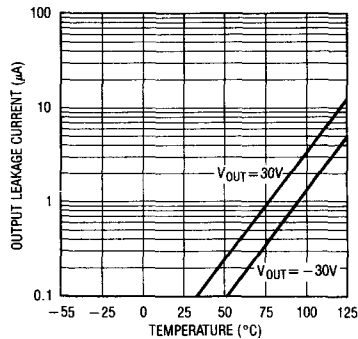
On-Off Pin Thresholds



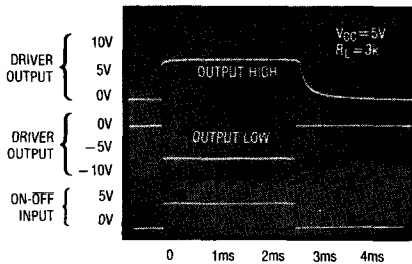
Supply Current in Shutdown



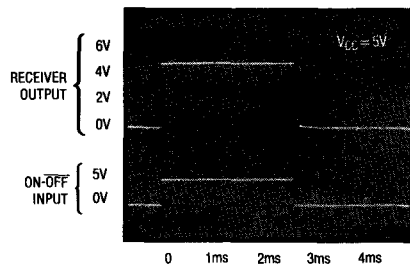
Driver Output Leakage in Shutdown



Shutdown to Driver Output



Shutdown to Receiver Output



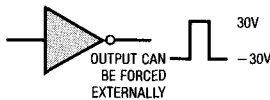
APPLICATION HINTS

The driver output stage of the LT1180 offers significantly improved protection over older bipolar and CMOS designs. In addition to current limiting, the driver output can be externally forced to $\pm 30V$ with no damage or excessive current flow, and will not disrupt the supplies. Some drivers have diodes connected between the outputs and the supplies, so externally applied voltages can cause excessive supply voltage to develop.

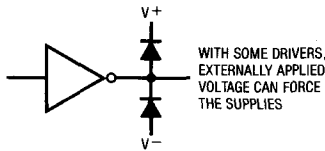
Placing the LT1180 in the SHUTDOWN mode (Pin 18 low) puts both the driver and receiver outputs in a high impedance state. This allows data line sharing and transceiver applications.

The SHUTDOWN mode also drops input supply current (V_{CC} ; Pin 17) to zero for power-conscious systems.

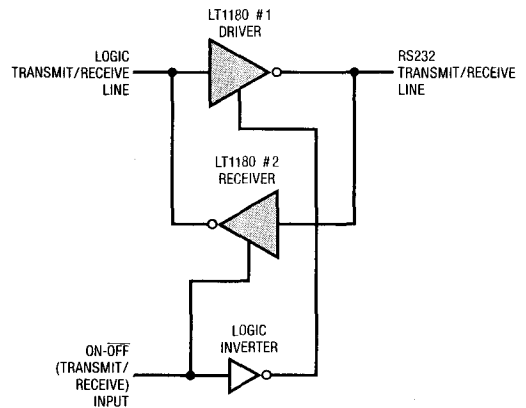
LT1180/LT1181 Driver



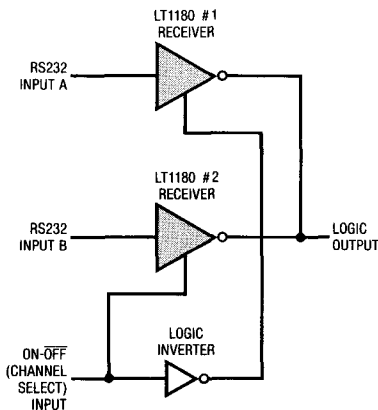
Older RS232 Drivers and CMOS Drivers



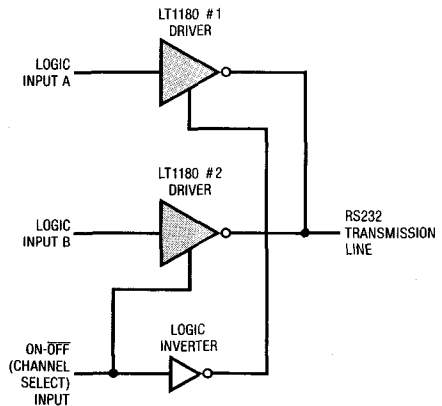
Transceiver



Sharing a Receiver Line



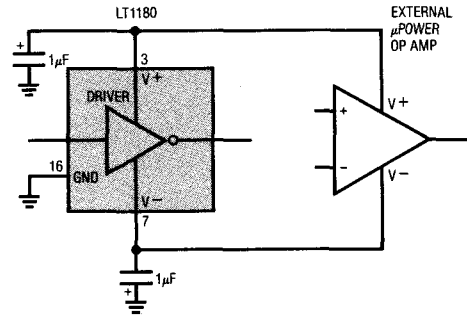
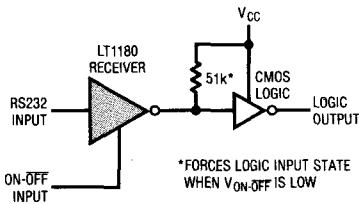
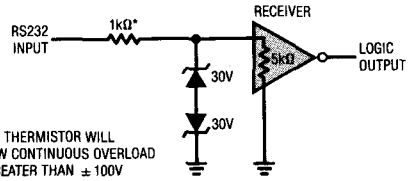
Sharing a Transmitter Line



APPLICATION HINTS

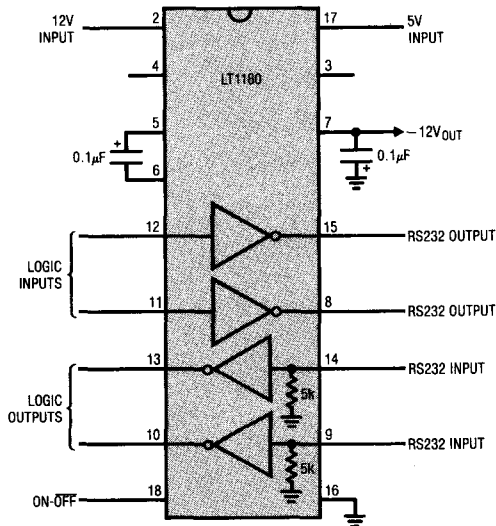
When driving CMOS logic from a receiver that will be used in the SHUTDOWN mode and there is no other active receiver on the line, a 51k resistor can be placed from the logic input to V_{CC} to force a definite logic level when the receiver output is in a high impedance state.

To protect against receiver input overloads in excess of $\pm 30V$, a voltage clamp can be placed on the data line and still maintain RS232 compatibility.



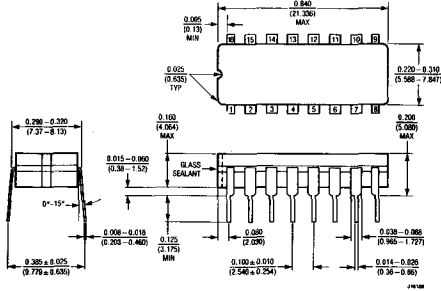
TYPICAL APPLICATION

Operating with 12V and 5V Supplies



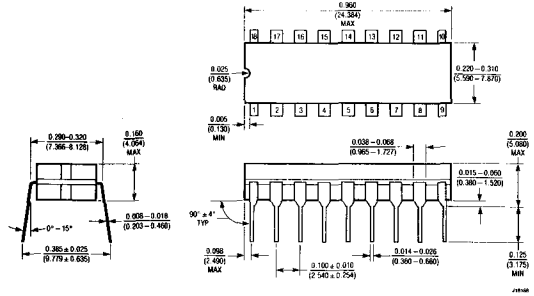
PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

J Package
16-Lead Ceramic DIP



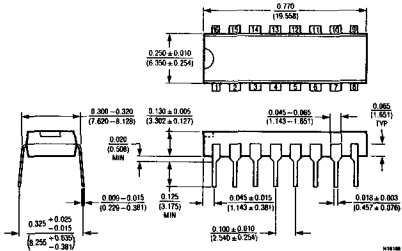
	T_{jmax}	θ_{ja}	θ_{jc}
LT1181MJ/J	150°C	100°C/W	40°C/W
LT1181CJ	150°C	100°C/W	40°C/W

J Package
18-Lead Ceramic DIP



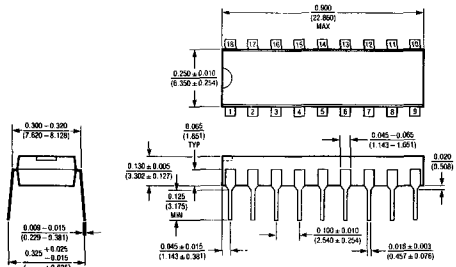
	T_{jmax}	θ_{ja}	θ_{jc}
LT1180MJ/J	150°C	100°C/W	40°C/W
LT1180CJ	150°C	100°C/W	40°C/W

N Package
16-Lead Plastic DIP



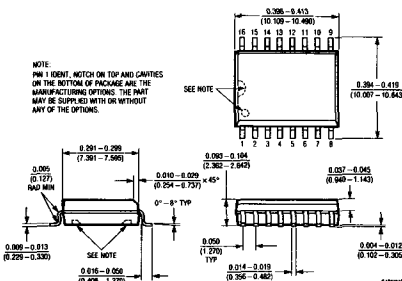
	T_{jmax}	θ_{ja}	θ_{jc}
LT1181CN/IN	125°C	120°C/W	50°C/W

N Package
18-Lead Plastic DIP

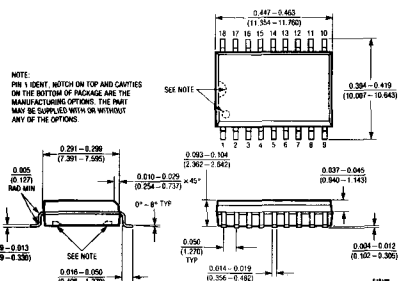


	T_{jmax}	θ_{ja}	θ_{jc}
LT1180CN/IN	125°C	120°C/W	50°C/W

S Package
16-Lead Plastic SOL



S Package
18-Lead Plastic SOL



Advanced Low Power 5V RS232 Dual Driver/Receiver

FEATURES

- 10mA Max Supply Current
- Absolutely No Latchup
- CMOS Comparable Low Power — 35mW Typ
- Superior to CMOS
 - Improved Speed — Operates Over 64K Baud
 - Improved Protection — Outputs Can be Forced to $\pm 30V$ Without Damage
 - Three-State Outputs are High Impedance When Off
 - Smaller Board Area Required
- $1\mu A$ Supply Current in Shutdown
- Available in SO Package
- Available With or Without Shutdown

APPLICATIONS

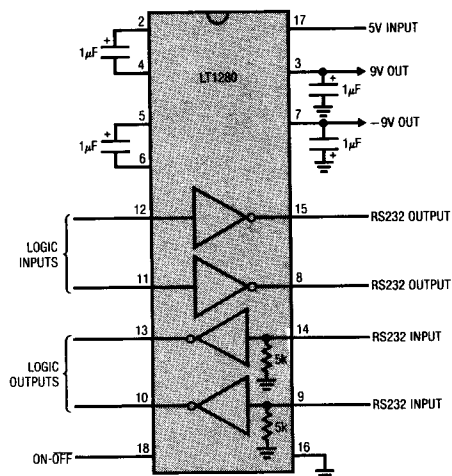
- Portable Computers
- Battery Powered RS232 Systems
- Power Supply Generators
- Terminals
- Modems

DESCRIPTION

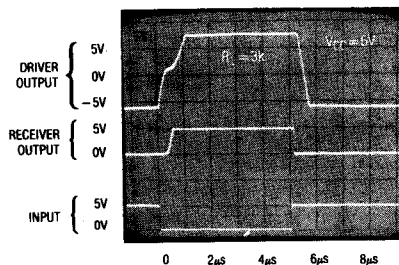
The LT1280 and LT1281 are the only dual RS232 driver/receiver with charge pump to guarantee absolutely no latchup. Requiring only $1\mu F$ charge pump capacitors, these interface optimized devices provide a realistic balance between CMOS levels of power dissipation and real world requirements for ruggedness. Small capacitors reduce cost as well as board size. The driver outputs are fully protected against overload and can be shorted to $\pm 30V$. Unlike CMOS, the advanced architecture of the LT1280/LT1281 does not load the signal line when "shut down" or when power is off. The receiver and RS232 outputs are put into a high impedance state. An advanced output stage allows driving high capacitive loads at high speeds with exceptional ruggedness against ESD.

For applications requiring up to 5 drivers and 5 receivers with charge pump in one package see the LT1130 Series data sheet. A version of the LT1280/81, the LT1180 and LT1181 is available for applications requiring small ($0.1\mu F$) capacitors. All of Linear Technology's RS232 IC's are available in standard surface mount packages.

TYPICAL APPLICATION



Output Waveforms



LT1280/LT1281

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC}) 6V
 V^+ 13.2V
 V^- -13.2V
 Input Voltage
 Driver V^- to V^+
 Receiver -30V to 30V
 On-Off Pin GND to 12V
 Output Voltage
 Driver $V^- + 30V$ to $V^+ - 30V$
 Receiver -0.3V to $V_{CC} + 0.3V$

Short Circuit Duration
 V^+ 30 Seconds
 V^- 30 Seconds
 Driver Output Indefinite
 Receiver Output Indefinite
 Operating Temperature Range
 LT1280M/LT1281M -55°C to 125°C
 LT1280I/LT1281I -40°C to 85°C
 LT1280C/LT1281C 0°C to 70°C
 Lead Temperature (Soldering, 10 sec.) 300°C

PACKAGE/ORDER INFORMATION

<p>TOP VIEW</p> <p>J PACKAGE 18-LEAD CERAMIC DIP</p> <p>N PACKAGE 18-LEAD PLASTIC DIP</p>	<p>ORDER PART NUMBER</p> <p>LT1280MJ LT1280IJ LT1280IN LT1280CJ LT1280CN</p>	<p>TOP VIEW</p> <p>S PACKAGE 18-LEAD PLASTIC SOL</p>	<p>ORDER PART NUMBER</p> <p>LT1280IS LT1280CS</p>
<p>TOP VIEW</p> <p>J PACKAGE 16-LEAD CERAMIC DIP</p> <p>N PACKAGE 16-LEAD PLASTIC DIP</p>	<p>ORDER PART NUMBER</p> <p>LT1281MJ LT1281IJ LT1281IN LT1281CJ LT1281CN</p>	<p>TOP VIEW</p> <p>S PACKAGE 16-LEAD PLASTIC SOL</p>	<p>ORDER PART NUMBER</p> <p>LT1281IS LT1281CS</p>

ELECTRICAL CHARACTERISTICS (Note 1)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Driver						
Output Voltage Swing	Load = 3k to GND Both Outputs.	Positive	5.0	7.3		V
		Negative	-5.0	-6.5		V
Logic Input Voltage Level	Input Low Level ($V_{OUT} = \text{High}$)			1.4	0.8	V
	Input High Level ($V_{OUT} = \text{Low}$)		2.0	1.4		V
Logic Input Current	$V_{IN} \geq 2.0V$			5	20	μA
	$V_{IN} \leq 0.8V$			5	20	μA
Output Short Circuit Current	Sourcing Current, $V_{OUT} = 0V$		7	12		mA
	Sinking Current, $V_{OUT} = 0V$		-7	-12		mA
Output Leakage Current	SHUTDOWN (Note 2), $V_{OUT} = \pm 30V$ (Note 4)			10	25	μA
Slew Rate	$R_L = 3k\Omega$, $C_L = 51pF$		4	15	30	V/ μs
Receiver						
Input Voltage Thresholds	Input Low Threshold, LT1280C/LT1281C LT1280I, M/LT1281I, M		0.8	1.3		V
			0.2	1.3		V
	Input High Threshold, LT1280C/LT1281C LT1280I, M/LT1281I, M			1.7	2.4	V
				1.7	3.0	V
Hysteresis		0.1	0.4	1.0	V	
Input Resistance		3	5	7	k Ω	
Output Voltage	Output Low, $I_{OUT} = -1.6mA$			0.2	0.4	V
	Output High, $I_{OUT} = 160\mu A$ ($V_{CC} = 5V$)		3.5	4.8		V
Output Short Circuit Current	Sinking Current, $V_{OUT} = V_{CC}$		-10	-20		mA
	Sourcing Current, $V_{OUT} = 0V$		0.3	0.6		mA
Output Leakage Current	SHUTDOWN (Note 2), $0V \leq V_{OUT} \leq V_{CC}$			1	10	μA
Supply Current	(Note 3)			7	10	mA
					14	mA
Supply Leakage Current (V_{CC})	SHUTDOWN (Note 2) (LT1280 Only) (Note 4)			1	25	μA
On-Off Pin Current	$0V \leq V_{ON-OFF} \leq 5V$ (LT1280 Only)			-15	80	μA

The ● denotes specifications which apply over the operating temperature range ($0^\circ C \leq T_A \leq 70^\circ C$ for commercial grade, $-40^\circ C \leq T_A \leq 85^\circ C$ for industrial grade or $-55^\circ C \leq T_A \leq 125^\circ C$ for military grade devices).

Note 1: These parameters apply for $V_{ON-OFF} = 3V$, $V_{CC} = 5V$ and $C = 1.0\mu F$ unless otherwise specified.

Note 2: $V_{ON-OFF} = 0.4V$ for $-55^\circ C \leq T_A \leq 100^\circ C$, and $V_{ON-OFF} = 0.2V$ for $100^\circ C \leq T_A \leq 125^\circ C$ (LT1280 only).

Note 3: Unless otherwise specified, $V_{CC} = 5V$, external loading of V^+ and V^- equals zero and the driver outputs are low (inputs high).

Note 4: Leakage current at $125^\circ C = 100\mu A$ max.

PIN FUNCTIONS (Pin numbers refer to LT1280)

V_{CC} (Pin 17): Input supply pin. Supply current drops to zero in the SHUTDOWN mode.

GND (Pin 16): Ground pin.

On-Off (Pin 18): Controls the operation mode of the LT1280 and is TTL/CMOS compatible. A logic low puts the device in the SHUTDOWN mode which reduces input supply current to zero and places both driver and receiver outputs in a high impedance state. A logic high fully enables the device.

V⁺ (Pin 3): Positive supply for RS232 drivers. $V^+ \approx 2V_{CC} - 1.5V$. Requires an external capacitor ($\geq 0.1\mu F$) for charge storage. Capacitor may be tied to ground or +5V input supply. With multiple transceivers, the V⁺ and V⁻ pins may be paralleled into common capacitors.

V⁻ (Pin 7): Negative supply for RS232 drivers. $V^- \approx -(2V_{CC} - 2.5V)$. Requires an external capacitor ($\geq 0.1\mu F$) for charge storage. With multiple transceivers, the V⁺ and V⁻ pins may be paralleled into common capacitors.

TR1 IN; TR2 IN (Pins 12, 11): RS232 driver input pins. Inputs are TTL/CMOS compatible. Inputs should not be allowed to float. Tie unused inputs to V_{CC}.

TR1 OUT; TR2 OUT (Pins 15, 8): Driver outputs with RS232 voltage levels. Outputs are in a high impedance state when in the SHUTDOWN mode or when power is off ($V_{CC}=0V$) to allow data line sharing. Outputs are fully short circuit protected from $V^- + 30V$ to $V^+ - 30V$ with power on, off, or in the SHUTDOWN mode. Typical output breakdowns are greater than $\pm 45V$ and higher applied voltages will not damage the device if moderately current limited. Shorting one output will affect output from the other.

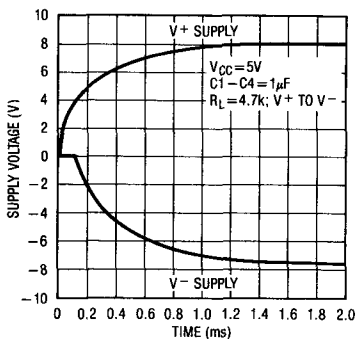
REC1 IN; REC2 IN (Pins 14, 9): Receiver inputs. Accepts RS232 voltage levels ($\pm 30V$) and has 0.4V of hysteresis to provide noise immunity. Input impedance is nominally 5k Ω .

REC1 OUT; REC2 OUT (Pins 13, 10): Receiver outputs with TTL/CMOS voltage levels. Outputs are in a high impedance state when in the SHUTDOWN mode to allow data line sharing. Outputs are fully short circuit protected to ground or V_{CC} with power on, off, or in the SHUTDOWN mode.

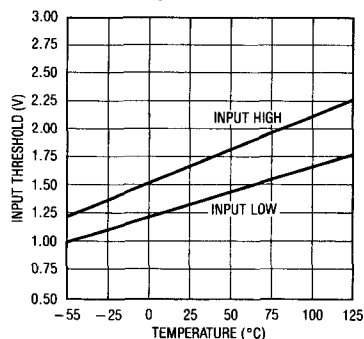
C1⁺; C1⁻; C2⁺; C2⁻ (Pins 2, 4, 5, 6): Requires an external capacitor ($\geq 0.1\mu F$) from C1⁺ to C1⁻ and another from C2⁺ to C2⁻. Pin 2 can be used for connecting a second positive supply. When a separate positive supply is used, C1 can be deleted.

TYPICAL PERFORMANCE CHARACTERISTICS

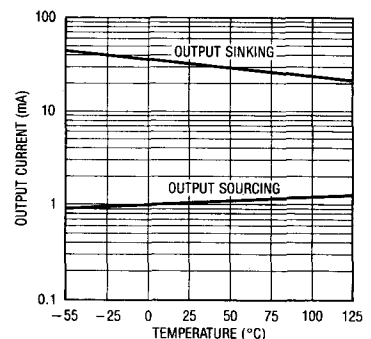
Supply Generation from V_{CC} or Shutdown



Receiver Input Thresholds

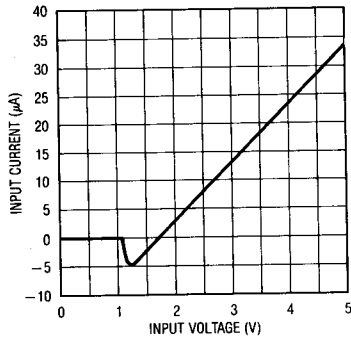


Receiver Output Short Circuit Current

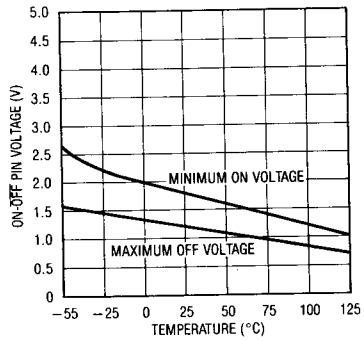


TYPICAL PERFORMANCE CHARACTERISTICS

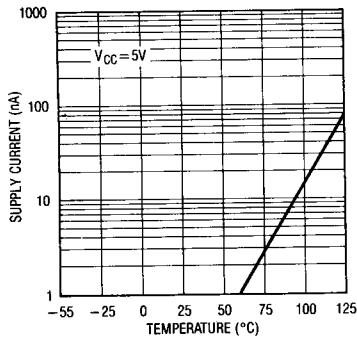
On-Off Pin Current vs Voltage



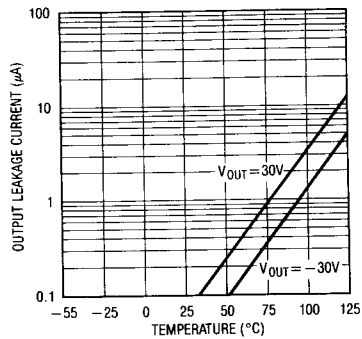
On-Off Pin Thresholds



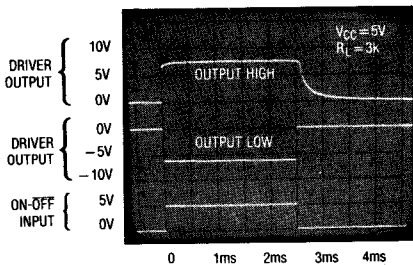
Supply Current in Shutdown



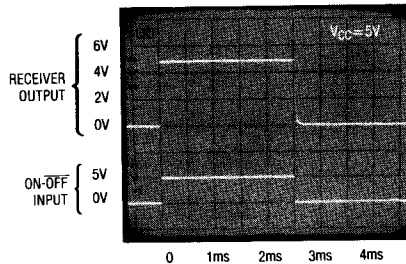
Driver Output Leakage in Shutdown



Shutdown to Driver Output



Shutdown to Receiver Output



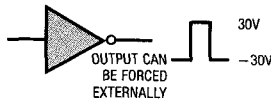
APPLICATION HINTS

The driver output stage of the LT1280 offers significantly improved protection over older bipolar and CMOS designs. In addition to current limiting, the driver output can be externally forced to $\pm 30V$ with no damage or excessive current flow, and will not disrupt the supplies. Some drivers have diodes connected between the outputs and the supplies, so externally applied voltages can cause excessive supply voltage to develop.

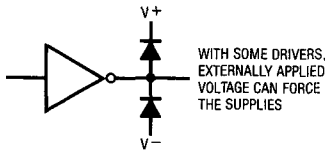
Placing the LT1280 in the SHUTDOWN mode (Pin 18 low) puts both the driver and receiver outputs in a high impedance state. This allows data line sharing and transceiver applications.

The SHUTDOWN mode also drops input supply current (V_{CC} ; Pin 17) to zero for power-conscious systems.

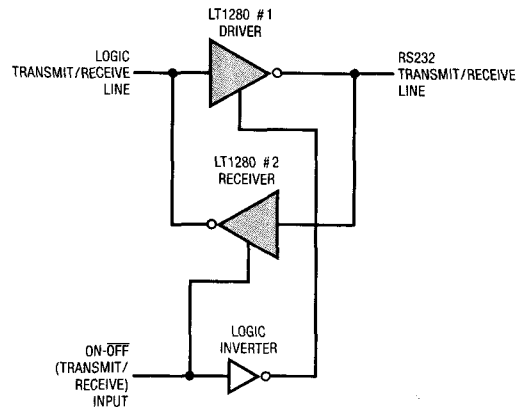
LT1280/LT1281 Driver



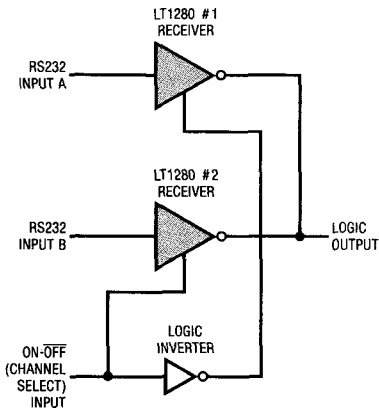
Older RS232 Drivers and CMOS Drivers



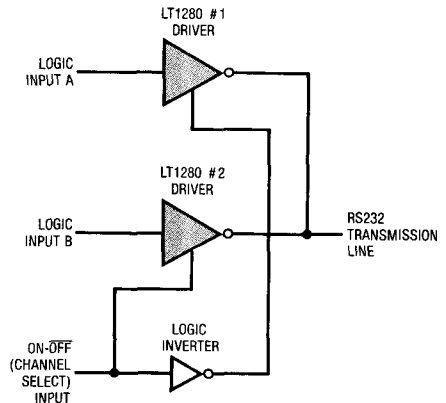
Transceiver



Sharing a Receiver Line



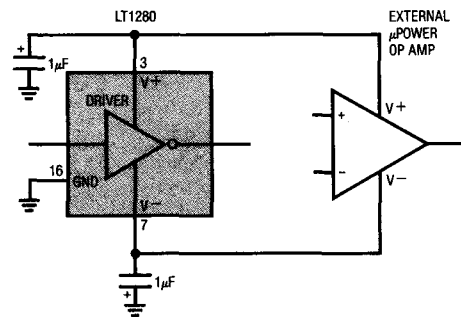
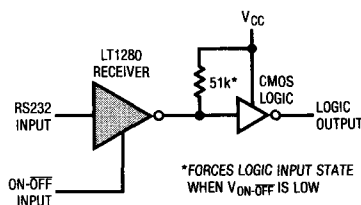
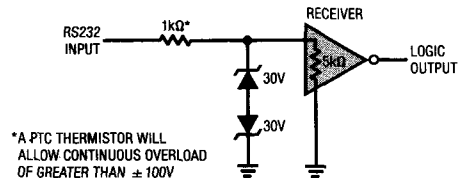
Sharing a Transmitter Line



APPLICATION HINTS

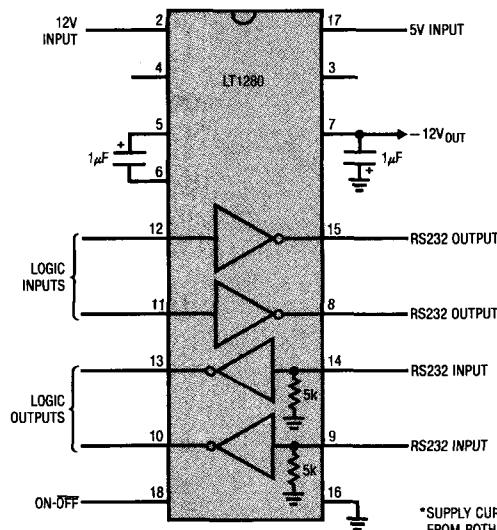
When driving CMOS logic from a receiver that will be used in the SHUTDOWN mode and there is no other active receiver on the line, a 51k resistor can be placed from the logic input to V_{CC} to force a definite logic level when the receiver output is in a high impedance state.

To protect against receiver input overloads in excess of $\pm 30V$, a voltage clamp can be placed on the data line and still maintain RS232 compatibility.



TYPICAL APPLICATION

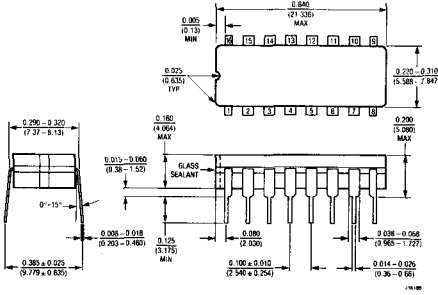
Operating with 12V and 5V Supplies*



*SUPPLY CURRENT IS SHUTDOWN FROM BOTH SUPPLIES.
 I_Q TYP = 4mA.

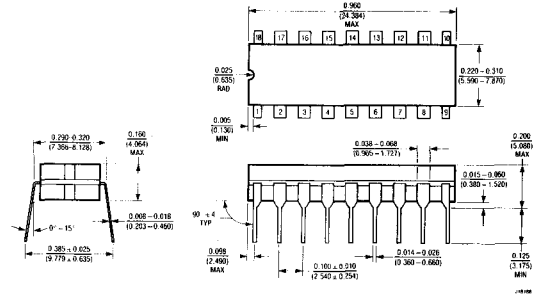
PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

J Package 16-Lead Ceramic DIP



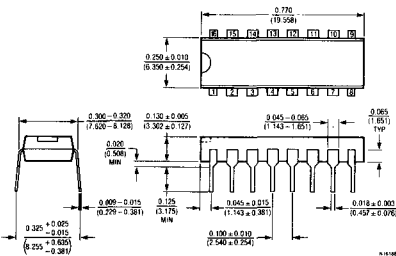
	T _{max}	θ _{ja}	θ _{jc}
LT1281MJ/J	150°C	100°C/W	40°C/W
LT1281CJ	150°C	100°C/W	40°C/W

J Package 18-Lead Ceramic DIP



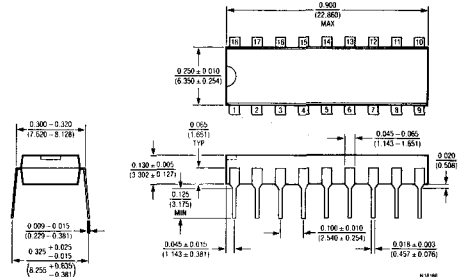
	T _{max}	θ _{ja}	θ _{jc}
LT1280MJ/J	150°C	100°C/W	40°C/W
LT1280CJ	150°C	100°C/W	40°C/W

N Package 16-Lead Plastic DIP



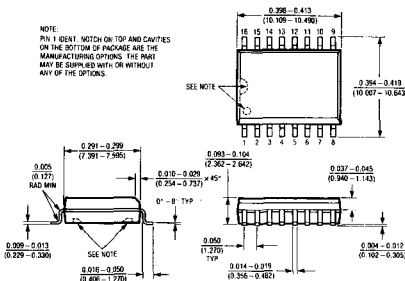
	T _{max}	θ _{ja}	θ _{jc}
LT1281CN/I/N	125°C	120°C/W	50°C/W

N Package 18-Lead Plastic DIP

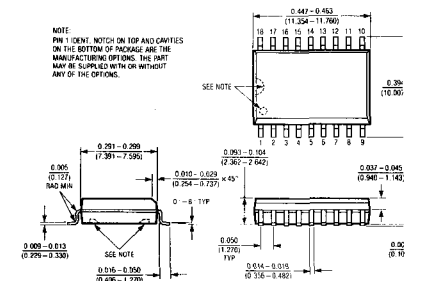


	T _{max}	θ _{ja}	θ _{jc}
LT1280CN/I/N	125°C	120°C/W	50°C/W

S Package 16-Lead Plastic SOL



S Package 18-Lead Plastic SOL



SECTION 11 — SPECIAL FUNCTION

SECTION 11—SPECIAL FUNCTION

INDEX	11-2
PROPRIETARY PRODUCTS	
<i>LTK001, Thermocouple Cold Junction Compensator and Matched Amplifier</i>	11-3
<i>LTC201, Quad CMOS SPST Low Charge Injection Analog Switch</i>	13-3
<i>LT1025, Micropower Thermocouple Cold Junction Compensator</i>	11-7
<i>LTC1043, Dual Precision Instrumentation Switched-Capacitor Building Block</i>	11-15
<i>LTC1043CS, Dual Precision Instrumentation Switched-Capacitor Building Block</i>	11-31
<i>LT1088, Wideband RMS-DC Converter Building Block</i>	11-33
<i>LT1089, High Side Switch</i>	11-45
<i>LT1188, 1.5A High Side Switch</i>	13-55

Thermocouple Cold Junction Compensator and Matched Amplifier

FEATURES

- 0.75°C Initial Accuracy (A Version)
- Extremely Low Warmup Drift
- Preset Outputs for Type E, J, K, R, S, T
- Single 5V to ±20V Operation
- 480 μ A Typical Supply Current

APPLICATIONS

- Thermocouple Cold Junction Compensation

DESCRIPTION

The LTK001 is a thermocouple amplifier supplied with a matched cold junction compensator. By separating the amplifier and compensator functions, the problem of compensator temperature rise is virtually eliminated. The compensator is a selected version of the LT1025 cold junction compensator. The amplifier, which is also available separately as LTKA0x has been specially selected for thermocouple applications. It has low supply current to minimize warmup drift, very low offset voltage (<35 μ V), high gain,

and extremely low input bias currents (<600pA) to allow high impedance input filters to be used without degrading offset voltage or drift.

Matching of the kits is accomplished by separating the compensators and amplifiers according to the polarity of their initial (room temperature) errors. This eliminates the need to sum the errors of the two components to find the worst-case error.

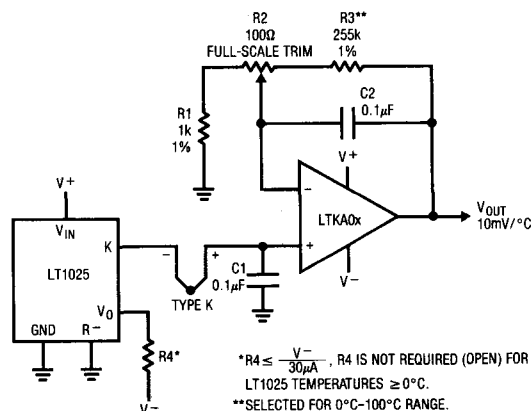
The LTK001 has direct thermocouple outputs of 60.9 μ V/°C (E), 51.7 μ V/°C (J), 40.6 μ V/°C (K, T), and 5.95 μ V/°C (R, S). It also has a 10mV/°C output which can be scaled to match any arbitrary thermocouple.

The amplifier in the LTK001 kit is available in an 8-pin plastic miniDIP for 0°C to 70°C operation and an 8-pin TO-39 metal can for -55°C to +125°C operation. The compensator is available in 8-pin plastic miniDIP for 0°C to 70°C operation and 8-pin ceramic miniDIP for -55°C to +125°C operation.

For multiple thermocouple applications using one compensator, amplifiers may be ordered separately (LTKA0x), still matched to the compensator.

For typical performance curves and applications circuits consult the LT1025 data sheet.

Type K 10mV/°C Thermometer



ABSOLUTE MAXIMUM RATINGS

Amplifier (LTKA0x)

Supply Voltage (Total V+ to V-) 40V
 Differential Input Current (Note 1)..... ± 10mA
 Common-Mode Input Voltage Equal to Supplies
 Output Short Circuit Duration Indefinite

Compensator (LT1025)

Supply Voltage (VIN to Ground Pin) 36V
 Output Voltage (Forced) 5V
 Output Short Circuit Duration Indefinite

Both Devices

Operating Temperature Range
 LTK001AMJ, LTK001MJ -55°C to 125°C
 LTK001ACN, LTK001CN 0°C to 70°C
 Storage Temperature Range -65°C to 150°C
 Lead Temperature Range (Soldering, 10 sec.) 300°C

PACKAGE/ORDER INFORMATION

<p>PLASTIC DIP COMPENSATOR (LT1025) HERMETIC DIP COMPENSATOR (LT1025)</p>	ORDER PART NUMBER
	KIT LTK001CN LTK001ACN LTK001MJ LTK001AMJ
<p>PLASTIC DIP AMPLIFIER (LTKA0x)</p>	AMPLIFIER ONLY (Note A) LTKA00CN8 LTKA01CN8
	AMPLIFIER ONLY (Note A) LTKA00MH LTKA01MH
<p>METAL CAN AMPLIFIER (LTKA0x)</p>	

Note A: The polarity of the amplifier is indicated by the 0 or 1 in the part number. An LT1025 with a 0 identifier is properly matched with an LTKA00 while an LT1025 with a 1 identifier should be used with an LTKA01.

ELECTRICAL CHARACTERISTICS — MATCHED AMPLIFIER AND COMPENSATOR TA = 25°C, VS = ± 15V (Amplifier), VS = 5V (Compensator)

PARAMETER	CONDITIONS	LTK001A			LTK001			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Total Temperature Error @ 25°C (Note 2)		Type E		0.75		2.5		°C
		Type J			0.75		2.5	°C
		Type K, T			0.86		2.5	°C
		Type R, S	(Note 11)		5.0		5.0	°C
Slope Error (Notes 3 and 8)	0°C ≤ Tj ≤ 70°C	Type E		0.05		0.09		°C/°C
		Type J		0.06		0.09	°C/°C	
		Type K, T		0.07		0.10	°C/°C	
		Type R, S		0.28		0.32	°C/°C	
Total Temperature Error at Temperature Extremes (Note 8)	0°C ≤ Tj ≤ 70°C	Type E		2.0		5		°C
		Type J		2.1		5	°C	
		Type K, T		2.6		5.2	°C	
		Type R, S	(Note 11)		16		16	°C
	-55°C ≤ Tj ≤ 125°C	Type E		6		8.5		°C
		Type J		6		8.5	°C	
		Type K, T		6.3		9	°C	
		Type R, S	(Note 11)		30		30	°C
Temperature Error Change with Supply Voltage (Note 4)			0.1		0.1		°C/V	
Supply Current			480 900		480 900		µA	

ELECTRICAL CHARACTERISTICS COMPENSATOR (LT1025) $V_S = 5V$ unless otherwise specified

PARAMETER	CONDITIONS			COMPENSATOR (LT1025)		UNITS
				MIN	TYP	
Temperature Error at 10mV/°C Output (Note 8)	$T_j = 25^\circ\text{C}$	LTK001A		0.3	0.5	°C
		LTK001		0.5	2.0	°C
	Full Temperature Span	●	See Curve on LT1025 Data Sheet			
Temperature Error at Individual Outputs (Note 9)	LTK001A	E, J, K, T		0.4	0.75	°C
		R, S		0.4	1.5	°C
	LTK001	E, J, K, T		0.8	2.4	°C
		R, S		1.2	3.5	°C
	Full Temperature Span	●	See Curve on LT1025 Data Sheet			
Supply Current	$4V \leq V_{IN} \leq 36V$ $0^\circ\text{C} \leq T_j \leq 70^\circ\text{C}$ $-55^\circ\text{C} \leq T_j \leq 125^\circ\text{C}$			80	100	μA
		●			150	μA
		●				200
Change in Supply Current	$4V \leq V_{IN} \leq 36V$			0.01	0.05	$\mu\text{A/V}$
Line Regulation (Note 10)	$4V \leq V_{IN} \leq 36V$ 10mV/°C Output	●		0.003	0.02	°C/V
Load Regulation (Note 10)	$0 \leq I_O \leq 1\text{mA}$ 10mV/°C Output	●		0.04	0.2	°C
Divider Impedance		E		2.5		k Ω
		J		2.1		k Ω
		K, T		4.4		k Ω
		R, S		3.8		k Ω

ELECTRICAL CHARACTERISTICS AMPLIFIER (LTKA0x) $V_S = \pm 15V$, $V_{CM} = 0$, $T_j = 25^\circ\text{C}$, unless otherwise specified

PARAMETER	CONDITIONS			AMPLIFIER (LTKA0x)		UNITS
				MIN	TYP	
Input Offset Voltage				10	35	μV
Input Offset Voltage Drift with Temperature	(Note 5)	●		0.3	1.5	$\mu\text{V}/^\circ\text{C}$
Input Bias Current	$0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$ $-55^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$	●		± 200	± 600	pA
		●		± 300	± 1500	pA
Input Bias Current Drift with Temperature	(Note 5)	●		1	5	pA/°C
Input Offset Current	$0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$ $-55^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$	●		± 100	± 500	pA
		●		± 200	± 700	pA
Input Offset Current Drift with Temperature	(Note 5)	●		0.6	4	pA/°C
Large Signal Voltage Gain	$R_L = 10\text{k}\Omega$	●		400	2000	V/mV
Common-Mode Rejection Ratio	$V_{CM} = \pm 13.5V$	●		106	130	dB
Power Supply Rejection Ratio	$\pm 2.5V \leq V_S \leq \pm 20V$ (Note 4)	●		106	125	dB
Common-Mode Input Voltage Range	Notes 5 and 6	Above V^-		0.75		V
		Below V^+			1.0	V
Output Voltage Swing (Notes 5 and 7)	Referred to Supplies	$I_{OUT} = 0.1\text{mA}$		0.8		V
		$I_{OUT} = 1\text{mA}$		1.1		V
Supply Current		●		400	800	μA
Supply Voltage Range	Total V^+ to V^- Voltage	●		4.5	40	V

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: The inputs of the LTKA0x amplifiers are clamped with diodes, so a differential voltage rating does not apply.

Note 2: Total temperature error is the overall error at 25°C taking into account the offset of the amplifier, the offset at the compensator 10mV/°C output, and the error in the compensator divider network. Warmup drift is not included.

Note 3: Slope error is the increase in total temperature error as ambient temperature is increased. It is guaranteed by design and by other tests, but is not tested directly.

Note 4: This is a worst-case limit assuming that any or all supply voltages change.

Note 5: Guaranteed, but not tested.

Note 6: By referring common-mode range to the supplies, the range referred to ground can be quickly calculated for any given supply voltage. With a single 5V supply, for instance, which has a worst-case low value of 4.7V, the upper common-mode limit is $4.7V - 1V = 3.7V$. The lower common-mode limit is $0V + 0.75V = 0.75V$. With $\pm 15V$ supplies, the limits would be $+14V$ and $-14.25V$, respectively. Common-mode range has a temperature sensitivity of $\approx 2mV/°C$.

Note 7: Absolute output voltage swing is calculated by subtracting the

given limits from actual supply voltage. These limits indicate the point where offset voltage has changed suddenly by $5\mu V$.

Note 8: Temperature error is defined as the deviation from the following formula:

$$V_{OUT} = \alpha(T) + \alpha\beta(T - 25°C)^2$$

α = Typical thermocouple Seebeck coefficient as follows, E = $60.9\mu V/°C$, J = $51.7\mu V/°C$, K, T = $40.6\mu V/°C$, R, S = $5.95\mu V/°C$. $\alpha = 10mV/°C$ at the 10mV output.

β = Nonlinearity coefficient built into the LT1025 to help compensate for the nonlinearities of the thermocouples. $\beta = 5.5 \times 10^{-4}$, generating $0.34°C$ bow for $25°C$ temperature change, and $1.36°C$ bow for $50°C$ change.

Note 9: Temperature error at the individual outputs is the sum of the 10mV/°C output error plus the resistor divider error.

Note 10: Line and load regulation do not take into account the effects of self-heating. Output changes due to self-heating can be calculated as follows:

$$\Delta V_{OUT}(\text{Line}) = \Delta V_{IN}(I_Q + I_{load})(150°C/W)$$

$$\Delta V_{OUT}(\text{Load}) = (\Delta I_{load})(V_{IN})(150°C/W)$$

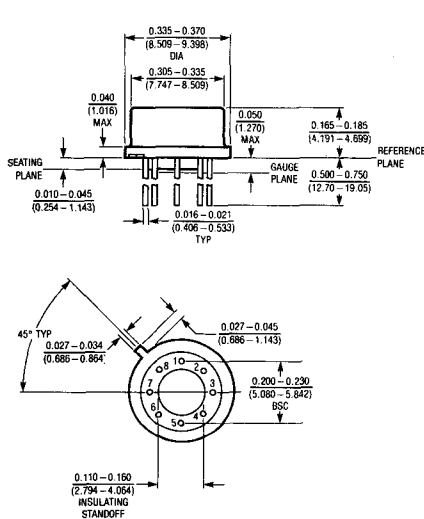
$$I_Q = \text{LT1025 supply current}$$

Load regulation is $30\mu A \leq I_Q \leq 1mA$ for $T_A \leq 0°C$.

Note 11: Larger errors with type R and S thermocouples are due mostly to $35\mu V$ offset of the amplifier. This error can be reduced to $5\mu V$ max with the LTC1050 or LTC1052 operational amplifiers.

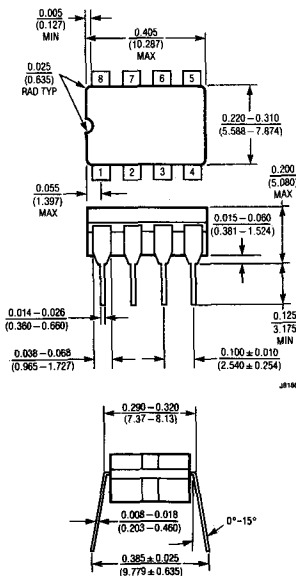
PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

H Package
8 Lead TO-5 Metal Can



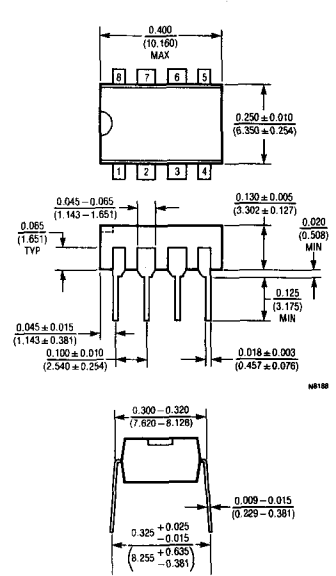
T_{JMAX}	θ_{JA}	θ_{JC}
150°C	150°C/W	45°C/W

J Package
8 Lead Hermetic DIP



T_{JMAX}	θ_{JA}
150°C	100°C/W

N Package
8 Lead Molded DIP



T_{JMAX}	θ_{JA}
100°C	130°C/W

Micropower Thermocouple Cold Junction Compensator

FEATURES

- 80 μ A Supply Current
- 4V to 36V Operation
- 0.5°C Initial Accuracy (A Version)
- Compatible with Standard Thermocouples (E, J, K, R, S, T)
- Auxiliary 10mV/°C Output

APPLICATIONS

- Thermocouple Cold Junction Compensator
- Centigrade Thermometer
- Temperature Compensation Network

DESCRIPTION

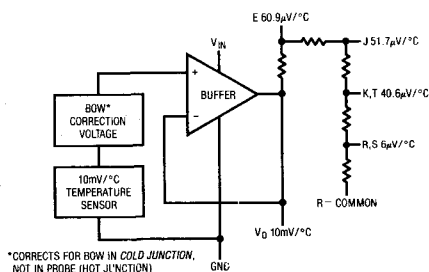
The LT1025 is a micropower thermocouple cold junction compensator for use with type E, J, K, R, S, and T thermocouples. It utilizes wafer level and post-package trimming to achieve 0.5°C initial accuracy. Special curvature correction circuitry is used to match the "bow" found in all thermocouples so that accurate cold junction compensation is maintained over a wider temperature range.

The LT1025 will operate with a supply voltage from 4V to 36V. Typical supply current is 80 μ A, resulting in less than 0.1°C internal temperature rise for supply voltages under 10V. A 10mV/°C output is available at low impedance, in addition to the direct thermocouple voltages of 60.9 μ V/°C (E), 51.7 μ V/°C (J), 40.3 μ V/°C (K, T) and 5.95 μ V/°C (R, S). All outputs are essentially independent of power supply voltage.

A special kit is available (LTK001) which contains an LT1025 and a custom tailored thermocouple amplifier. The amplifier and compensator are matched to allow a much tighter specification of temperature error than would be obtained by adding the compensator and amplifier errors on a worst-case basis. The amplifier from this kit is available separately as LTKA0x.

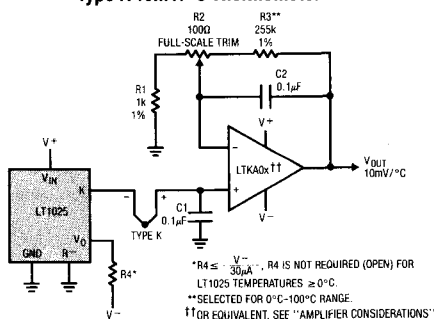
The LT1025 is available in an 8 pin plastic miniDIP for temperatures between 0°C and 70°C. A ceramic miniDIP is also available for -55°C to +125°C operation.

BLOCK DIAGRAM



TYPICAL APPLICATION

Type K 10mV/°C Thermometer



ABSOLUTE MAXIMUM RATINGS

Input Supply Voltage.....	36V
Output Voltage (Forced).....	5V
Output Short Circuit Duration.....	Indefinite
Operating Temperature Range	
LT1025AC, LT1025C.....	0°C to +70°C
LT1025AM, LT1025M.....	-55°C to +125°C
Storage Temperature Range.....	-55°C to +150°C
Lead Temperature (Soldering, 10 sec).....	300°C

PACKAGE/ORDER INFORMATION

	ORDER PART NUMBER
	LT1025AMJ8 LT1025MJ8 LT1025ACN8 LT1025CN8

ELECTRICAL CHARACTERISTICS

$V_S = 5V, T_A = 25^\circ C$, Pin 5 tied to Pin 4, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	
Temperature Error at 10mV/°C Output (Notes 3, 4)	$T_J = 25^\circ C$					
	LT1025A		0.3	0.5	°C	
	LT1025		0.5	2.0	°C	
	Full Temperature Span	●	See Curve			
Resistor Divider Accuracy (Notes 1, 3)	$V_{OUT} = 10mV/^\circ C$ LT1025A	E	60.6	60.9	61.3	$\mu V/^\circ C$
		J	51.4	51.7	52.1	$\mu V/^\circ C$
	LT1025	K, T	40.3	40.6	41.0	$\mu V/^\circ C$
		R, S	5.8	5.95	6.2	$\mu V/^\circ C$
	LT1025	E	60.4	60.9	61.6	$\mu V/^\circ C$
		J	51.2	51.7	52.3	$\mu V/^\circ C$
		K, T	40.2	40.6	41.2	$\mu V/^\circ C$
		R, S	5.75	5.95	6.3	$\mu V/^\circ C$
Supply Current	$4V \leq V_{IN} \leq 36V$ LT1025AC, LT1025C LT1025AM, LT1025M	●	50	80	100	μA
		●	50		150	μA
		●			200	μA
Line Regulation (Note 2)	$4V \leq V_{IN} \leq 36V$	●	0.003	0.02	°C/V	
Load Regulation (Note 2)	$0 \leq I_O \leq 1mA$	●	0.04	0.2	°C	
Divider Impedance	E, J, K, T, R, S		2.5			k Ω
			2.1			k Ω
			4.4			k Ω
			3.8			k Ω
Change in Supply Current	$4V \leq V_{IN} \leq 36V$		0.01	0.05	$\mu A/V$	

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: Divider accuracy is measured by applying a 10.000V signal to the output divider and measuring the individual outputs.

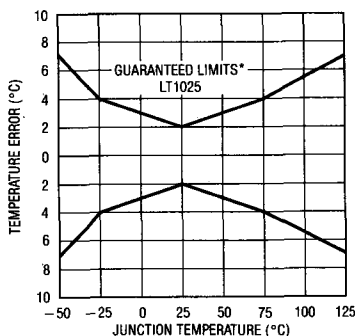
Note 2: Regulation does not include the effects of self-heating. See "Internal Temperature Rise" in Application Guide. Load regulation is $30\mu A \leq I_O \leq 1mA$ for $T_A \leq 0^\circ C$.

Note 3: To calculate total temperature error at individual thermocouple outputs, add 10mV/°C output error to the resistor divider error. Total error for type K output at 25°C with an LT1025A is $0.5^\circ C$ plus $(0.4\mu V/^\circ C)(25^\circ C) / (40.6\mu V/^\circ C) = 0.5^\circ C + 0.25^\circ C = 0.75^\circ C$.

Note 4: Temperature error is defined as the deviation from the following formula: $V_{OUT} = 10mV(T) + (10mV)(5.5 \times 10^{-4})(T - 25^\circ C)^2$. The second term is a built-in nonlinearity designed to help compensate the nonlinearity of the cold junction. This "bow" is $\approx 0.34^\circ C$ for a 25°C temperature change.

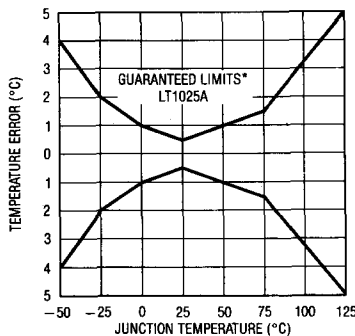
TYPICAL PERFORMANCE CHARACTERISTICS

10mV/°C Output Temperature Error LT1025



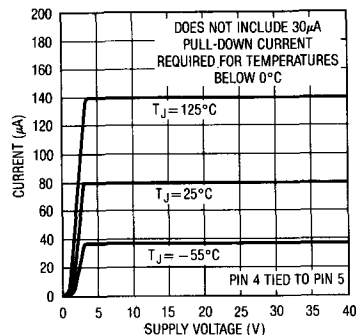
*ERROR CURVE FACTORS IN THE NONLINEARITY TERM BUILT IN TO THE LT1025. SEE THEORY OF OPERATION IN APPLICATION GUIDE SECTION.

10mV/°C Output Temperature Error LT1025A



*ERROR CURVE FACTORS IN THE NONLINEARITY TERM BUILT IN TO THE LT1025. SEE THEORY OF OPERATION IN APPLICATION GUIDE SECTION.

Supply Current



APPLICATION GUIDE

The LT1025 was designed to be extremely easy to use, but the following ideas and suggestions should be helpful in obtaining the best possible performance and versatility from this new cold junction compensator.

Theory of Operation

A thermocouple consists of two dissimilar metals joined together. A voltage (Seebeck EMF) will be generated if the two ends of the thermocouple are at different temperatures. In Figure 1, iron and constantan are joined at the temperature measuring point T₁. Two additional thermocouple junctions are formed where the iron and constantan connect to ordinary copper wire. For the purposes of this discussion it is assumed that these two junctions are at the same temperature, T₂. The Seebeck voltage, V_S, is the product of the Seebeck coefficient α, and the temperature difference, T₁ - T₂; V_S = α(T₁ - T₂). The junctions at T₂ are commonly called the cold junction because a common practice is to immerse the T₂ junction in 0°C ice/water slurry to make T₂ independent of room temperature variations. Thermocouple tables are based on a cold-junction temperature of 0°C.

To date, IC manufacturers efforts to make microminiature thermos bottles have not been totally successful. Therefore, an electronically simulated cold-junction is required for most applications. The idea is basically to add a temperature dependent voltage to V_S such that the voltage sum is the same as if the T₂ junction were at a constant 0°C instead of at room temperature. This voltage source is called a cold junction compensator. Its output is designed to be 0V at 0°C and have a slope equal to the Seebeck coefficient over the expected range of T₂ temperatures.

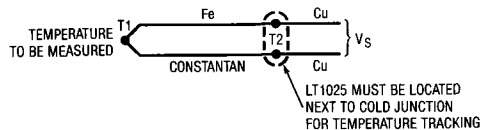


Figure 1

To operate properly, a cold junction compensator must be at exactly the same temperature as the cold junction of the thermocouple (T₂). Therefore, it is important to locate the LT1025 physically close to the cold junction with local temperature gradients minimized. If this is not possible, an extender made of matching thermocouple wire can be

used. This shifts the cold junction from the user termination to the end of the extender so that the LT1025 can be located remotely from the user termination as shown in Figure 2.

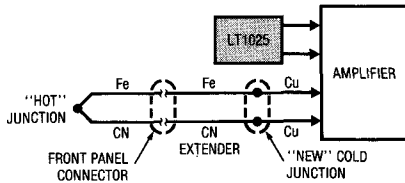


Figure 2

The four thermocouple outputs on the LT1025 are $60.9\mu\text{V}/^\circ\text{C}$ (E), $51.7\mu\text{V}/^\circ\text{C}$ (J), $40.6\mu\text{V}/^\circ\text{C}$ (K and T), and $6\mu\text{V}/^\circ\text{C}$ (R and S). These particular coefficients are chosen to match the room temperature (25°C) slope of the thermocouples. Over wide temperature ranges, however, the slope of thermocouples changes, yielding a quasi-parabolic error compared to a constant slope. The LT1025 outputs have a deliberate parabolic "bow" to help compensate for this effect. The outputs can be mathematically described as the sum of a linear term equal to room temperature slope plus a quadratic term proportional to temperature deviation from 25°C squared. The coefficient (β) of the quadratic term is a compromise value chosen to offer improvement in all the outputs.

$$V_{\text{OUT}} = \alpha T + \alpha\beta(T - 25^\circ)^2$$

$$\beta \approx 5.5 \times 10^{-4}$$

The actual β term which would be required to best compensate each thermocouple type in the temperature range of 0°C to 50°C is: E, 6.6×10^{-4} ; J, 4.8×10^{-4} ; K, 4.3×10^{-4} ; R, 1.9×10^{-3} ; S, 1.9×10^{-3} ; T, 1×10^{-3} .

The temperature error specification for the LT1025 $10\text{mV}/^\circ\text{C}$ output (shown as a graph) assumes a β of 5.5×10^{-4} . For example, an LT1025 is considered "perfect" if its $10\text{mV}/^\circ\text{C}$ output fits the equation $V_O = 10\text{mV}(T) + (10\text{mV})(5.5 \times 10^{-4})(T - 25^\circ\text{C})^2$.

Operating at Negative Temperatures

The LT1025 is designed to operate with a single positive supply. It therefore cannot deliver proper outputs for temperatures below zero unless an external pull-down resistor is added to the V_O output. This resistor can be connected to any convenient negative supply. It should be selected to sink at least $30\mu\text{A}$ of current. Suggested value for a -5V

supply is $150\text{k}\Omega$, and for a -15V supply, $470\text{k}\Omega$. Smaller resistors must be used if an external load is connected to the $10\text{mV}/^\circ\text{C}$ output. The LT1025 can source up to 1mA of current, but there is a trade-off with internal temperature rise.

Internal Temperature Rise

The LT1025 is specified for temperature accuracy assuming no internal temperature rise. At low supply voltages this rise is usually negligible ($\approx 0.05^\circ\text{C}@5\text{V}$), but at higher supply voltages or with external loads or pull-down current, internal rise could become significant. This effect can be calculated from a simple thermal formula, $\Delta T = (\Theta_{\text{JA}})(V^+)(I_Q + I_L)$, where Θ_{JA} is thermal resistance from junction to ambient, ($\approx 130^\circ\text{C}/\text{W}$), V^+ is the LT1025 supply voltage, I_Q is the LT1025 supply current ($\approx 80\mu\text{A}$), and I_L is the total load current including actual load to ground and any pull-down current needed to generate negative outputs. A sample calculation with a 15V supply and $50\mu\text{A}$ pull-down current would yield, $(130^\circ\text{C}/\text{W})(15\text{V})(80 + 50\mu\text{A}) = 0.32^\circ\text{C}$. This is a significant rise in some applications. It can be reduced by lowering supply voltage (a simple fix is to insert a 10V zener in the V_{IN} lead) or the system can be calibrated and specified after an initial warm-up period of several minutes.

Driving External Capacitance

The direct thermocouple drive pins on the LT1025 (J, K, etc.) can be loaded with as much capacitance as desired, but the $10\text{mV}/^\circ\text{C}$ output should not be loaded with more than 50pF unless external pull-down current is added, or a compensation network is used.

Thermocouple Effects in Leads

Thermocouple voltages are generated whenever dissimilar materials are joined. This includes the leads of IC packages, which may be kovar in TO-5 cans, alloy 42 or copper in dual-in-line packages, and a variety of other materials in plating finishes and solders. The net effect of these thermocouples is "zero" if all are at exactly the same temperature, but temperature gradients exist within IC packages and across PC boards whenever power is dissipated. For this reason, extreme care must be used to ensure that no temperature gradients exist in the vicinity of the thermocouple terminations, the LT1025, or the thermocouple amplifier. If a gradient cannot be eliminated, leads should be

positioned isothermally, especially the LT1025 R⁻ and appropriate output pins, the amplifier input pins, and the gain setting resistor leads. An effect to watch for is amplifier offset voltage warm-up drift caused by mismatched thermocouple materials in the wire-bond/lead system of the IC package. This effect can be as high as tens of microvolts in TO-5 cans with kovar leads. It has nothing to do with the actual offset drift specification of the amplifier and can occur in amplifiers with measured “zero” drift. Warm-up drift is directly proportional to amplifier power dissipation. It can be minimized by avoiding TO-5 cans, using low supply current amplifiers, and by using the lowest possible supply voltages. Finally, it can be accommodated by calibrating and specifying the system after a five minute warm-up period.

Reversing the Polarity of the 10mV/°C Output

The LT1025 can be made to “stand on its head” to achieve a minus 10mV/°C output point. This is done as shown in Figure 3. The normal output (V_O) is grounded and feedback is established between the ground pin and the positive supply pin by feeding both of them with currents while coupling them with a 6V zener. The ground pin will now be forced by feedback to generate -10mV/°C as long as the grounded output is supplying a net “source” current into ground. This condition is satisfied by selecting R1 such that the current through R1 (I⁻) is more than the sum of the LT1025 supply current, the maximum load current (I_L), and the minimum zener current (≈ 50μA). R2 is then selected to supply more current than I⁻.

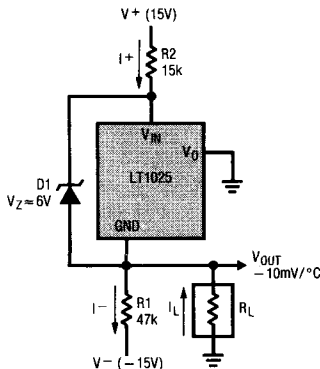


Figure 3

$$R1 = \frac{V^-}{300\mu A + I_L} \quad R2 = \frac{V^+ - V_Z (\approx 6V)}{V^- / R1 + 280\mu A}$$

For ± 15V supplies, with I_L = 20μA maximum, R1 = 47k and R2 = 15k.

Amplifier Considerations

Thermocouple amplifiers need very low offset voltage and drift, and fairly low bias current if an input filter is used. The best precision bipolar amplifiers should be used for type J, K, E, and T thermocouples which have Seebeck coefficients of 40–60μV/°C. In particularly critical applications or for R and S thermocouples (6–15μV/°C), a chopper-stabilized amplifier is required. Linear Technology offers three amplifiers specifically tailored for thermocouple applications. The LTKA0x is a bipolar design with extremely low offset (< 35μV), low drift (< 1.5μV/°C), very low bias current (< 1nA), and almost negligible warm-up drift (supply current is ≈ 400μA). It is very cost effective even when compared with “jellybean” op amps with vastly inferior specifications.

For the most demanding applications, the LTC1050 and LTC1052 CMOS chopper-stabilized amplifiers offer 5μV offset and 0.05μV/°C drift (even over the full military temperature range). Input bias current is 30pA, and gain is typically 30 million. These amplifiers should be used for R and S thermocouples, especially if no offset adjustments can be tolerated, or a large ambient temperature swing is expected.

Regardless of amplifier type, it is suggested that for best possible performance, dual-in-line (DIP) packages be used to avoid thermocouple effects in the kovar leads of TO-5 metal can packages if amplifier supply current exceeds 500μA. These leads can generate both DC and AC offset terms in the presence of thermal gradients in the package and/or external air motion.

In many situations, thermocouples are used in high noise environments, and some sort of input filter is required. (See discussion of input filters). To reject 60Hz pick-up with reasonable capacitor values, input resistors in the 10k–100k range are needed. Under these conditions, bias current for the amplifier needs to be less than 1nA to avoid offset and drift effects.

To avoid gain error, high open loop gain is necessary for single-stage thermocouple amplifiers with 10mV/°C or higher outputs. A type K amplifier, for instance, with

11

100mV/°C output, needs a *closed* loop gain of $\approx 2,500$. An ordinary op amp with a minimum open loop of 50,000 would have an initial gain error of $(2,500)/(50,000) = 5\%$! Although closed loop gain is commonly trimmed, temperature drift of open loop gain will have a very deleterious effect on output accuracy. Minimum suggested open loop gain for type E, J, K, and T thermocouples is 250,000. This gain is adequate for type R and S if output scaling is 10mV/°C or less.

Suggested Amplifier Types

THERMOCOUPLE	SUPPLY VOLTAGE		
	$\pm 15V$	$\pm 5V$	SINGLE SUPPLY
E, J, K, T	LTKA0x	LTKA0x	LTC1050
	LT1012	LT1012	LTC1052
	LT1001	LT1001	LT1006
		LTC1050	
		LTC1052	
R, S	LTKA0x	LTC1050	LTC1050
	LT1012	LTC1052	LTC1052
		LTKA0x	LT1006

Thermocouple Nonlinearities

Thermocouples are linear over relatively limited temperature spans if accuracies of better than 2°C are needed. The graph in Figure 4 shows thermocouple nonlinearity for the temperature range of 0°C–400°C. Nonlinearities can be dealt with in hardware by using offsets, breakpoints, or power series generators. Software solutions include look-up tables, power series expansions, and piece-wise approximations. For tables and power series coefficients, the reader is referred to the ASTM Publication 470A.

Hardware correction for nonlinearity can be as simple as an offset term. This is shown in Figure 5. The thermocouple shown in the figure has an increasing slope (α) with temperature. The temperature range of interest is between T_L and T_H , with a calibration point at T_M . If a simple amplifier is used and calibrated at T_M , the output will be very high at T_L and very low at T_H . Adding the proper offset term and calibrating at T1/6 or T5/6 can significantly reduce errors. The technique is as follows:

1. Calculate amplifier gain:

$$G = (SF)(T_H - T_L) / (V_H - V_L)$$

SF = Output scale factor, e.g., 10mV/°C

V_H = Thermocouple output @ T_H

V_L = Thermocouple output @ T_L

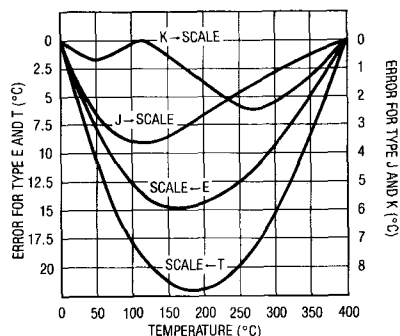


Figure 4. Thermocouple Nonlinearity, 0°C–400°C

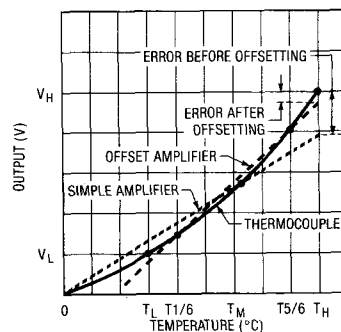


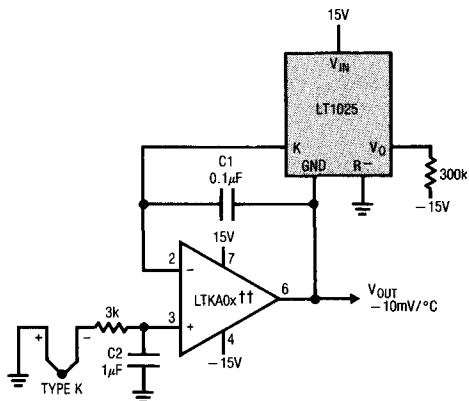
Figure 5. Offset Curve Fitting

2. Use precision resistors to set gain or calibrate gain by introducing a precision “delta” input voltage and trimming for proper “delta” output.
3. Calibrate output by adding in a true offset term which does not affect gain (by summing, etc.). Calibration may be done at any temperature either by immersing the thermocouple in a calibrated bath or by substituting a precision input voltage. The method which tends to minimize worst-case error over the whole T_L to T_H range is to calibrate at 1/6 or 5/6 of span. This may be modified if best accuracy is desired at one particular point.

Breakpoint correction for nonlinearity is more complicated than a simple offset, but a single breakpoint combined with offset will reduce errors typically by 4:1 over a simple offset technique.

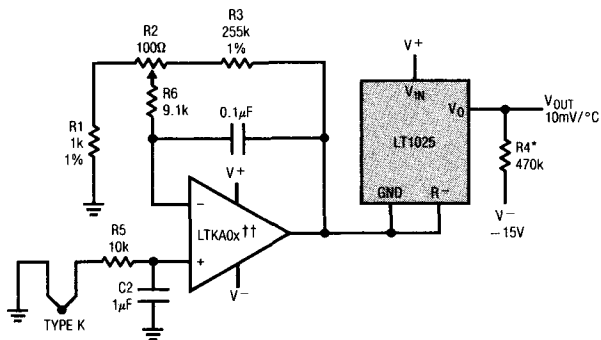
APPLICATION CIRCUITS

Eliminating Amplifier Feedback Resistors (Output Goes Negative with Increasing Temperature)



†† OR EQUIVALENT. SEE "AMPLIFIER CONSIDERATIONS"

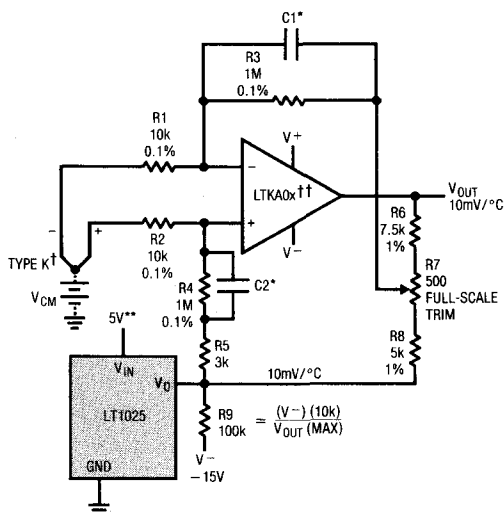
Type K Thermometer with Grounded Thermocouple



* $R4 \leq \frac{V-}{30\mu A}$ IF OUTPUT MUST SINK CURRENT, $R4$ MUST BE DECREASED APPROPRIATELY. $R4$ IS NOT REQUIRED (OPEN) FOR LT1025 TEMPERATURES $\geq 0^\circ C$ WHEN SOURCING CURRENT ONLY.

†† OR EQUIVALENT. SEE "AMPLIFIER CONSIDERATIONS"

Differential Thermocouple Amplifier



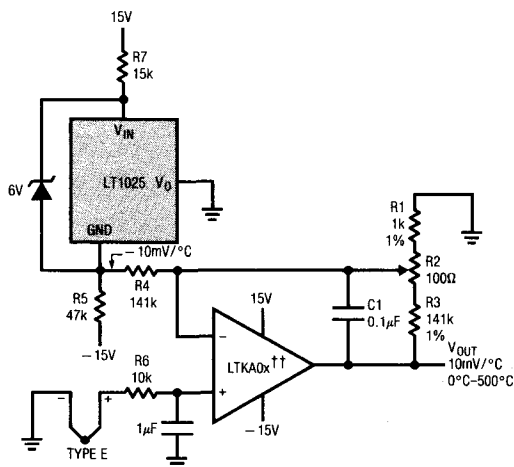
*C1 AND C2 FILTER RIPPLE AND NOISE, BUT WILL LIMIT AC COMMON-MODE REJECTION IF NOT MATCHED. SUGGESTED VALUES ARE 0.001µF TO 0.1µF.

**USE LOWEST POSSIBLE SUPPLY VOLTAGE TO MINIMIZE INTERNAL TEMPERATURE RISE.

† FOR BEST ACCURACY, THERMOCOUPLE RESISTANCE SHOULD BE LESS THAN 100Ω.

†† OR EQUIVALENT. SEE "AMPLIFIER CONSIDERATIONS"

Utilizing Negative LT1025 Drive to Accommodate Grounded Thermocouple*

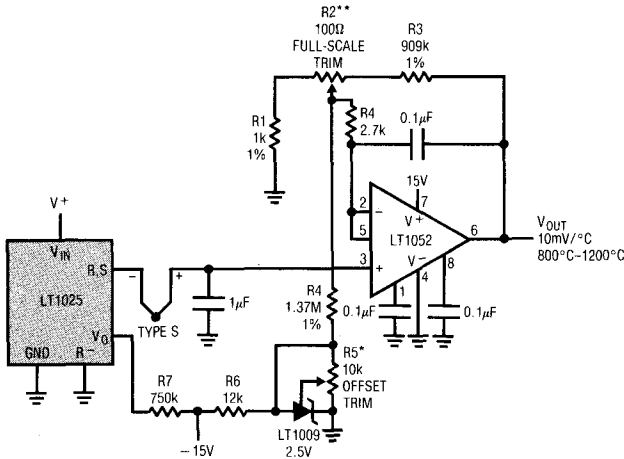


*SEE "REVERSING THE POLARITY OF THE 10mV/°C OUTPUT"

†† OR EQUIVALENT. SEE "AMPLIFIER CONSIDERATIONS"

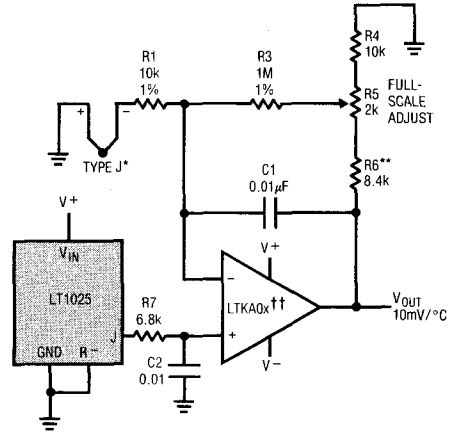
LT1025

Type S Thermocouple Amplifier with Ultra-Low Offset and Drift†



*TRIM R5 FOR $V_{OUT} = 1.669V @ V_{IN} = 0.000mV$ (+ INPUT OF AMPLIFIER GROUND)
 **TRIM R2 FOR $V_{OUT} = 9.998V @ T = 1000^{\circ}C$. OR FOR $V_{IN} @ +$ INPUT OF AMPLIFIER = $9.585mV$
 † THIS AMPLIFIER HAS A DELIBERATE OFFSET TO ALLOW OUTPUT SLOPE ($10mV/^{\circ}C$) TO BE SET INDEPENDENTLY FROM AN ARBITRARY HIGH TEMPERATURE CENTER POINT ($1000^{\circ}C$). THIS IS REQUIRED BECAUSE THE SLOPE OF TYPE "S" THERMOCOUPLES VARIES RAPIDLY WITH TEMPERATURE, INCREASING FROM $6\mu V/^{\circ}C @ 25^{\circ}C$ TO $11\mu V/^{\circ}C @ 1000^{\circ}C$. NONLINEARITY LIMITS ACCURACY TO $\approx 3^{\circ}C$ OVER THE $800^{\circ}C$ TO $1200^{\circ}C$ RANGE EVEN WITH OFFSET CORRECTION.

Grounded Thermocouple Amplifier with Positive Output



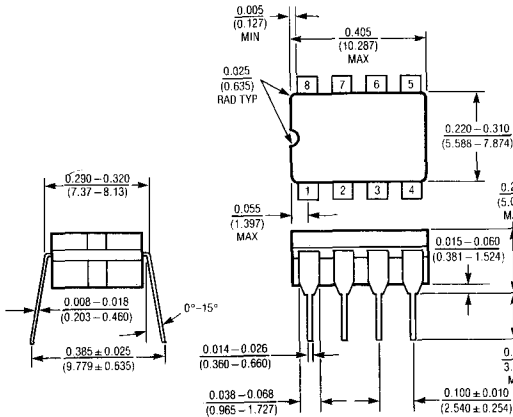
*FOR BEST ACCURACY, THERMOCOUPLE RESISTANCE SHOULD BE LESS THAN 500.

**SELECTED FOR $0^{\circ}C$ TO $200^{\circ}C$ RANGE.

†† OR EQUIVALENT. SEE "AMPLIFIER CONSIDERATIONS"

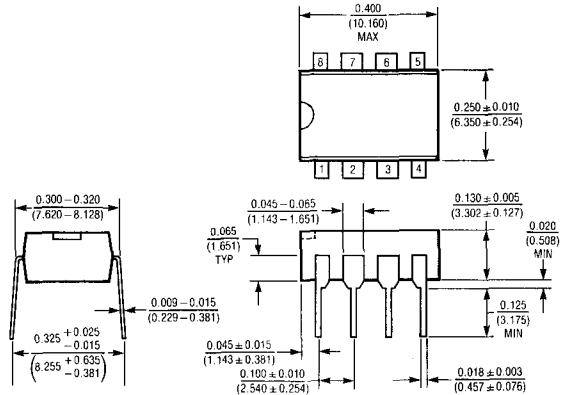
PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

J Package 8 Lead Hermetic DIP



T_J MAX	θ_{JA}
150°C	100°C/W

N Package 8 Lead Molded DIP



T_J MAX	θ_{JA}
100°C	130°C/W

Dual Precision Instrumentation Switched-Capacitor Building Block

FEATURES

- Instrumentation Front End with 120dB CMRR
- Precise, Charge-Balanced Switching
- Operates from 3V to 18V
- Internal or External Clock
- Operates up to 5MHz Clock Rate
- Low Power
- Two Independent Sections with One Clock

APPLICATIONS

- Precision Instrumentation Amplifiers
- Ultra Precision Voltage Inverters, Multipliers and Dividers
- V-F and F-V Converters
- Sample and Hold
- Switched-Capacitor Filters

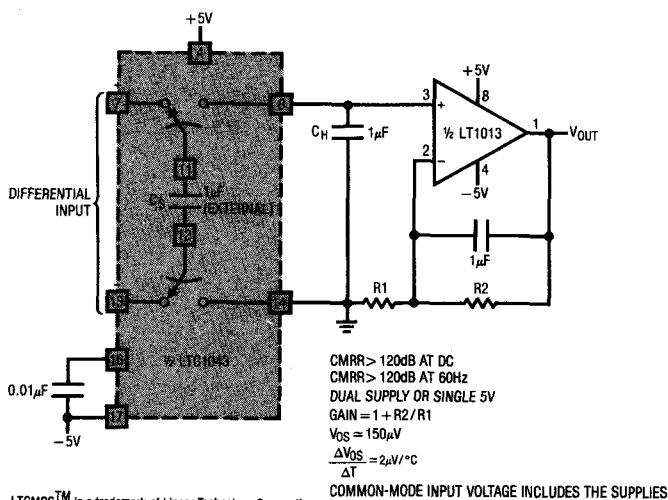
DESCRIPTION

The LTC1043 is a monolithic, charge-balanced, dual switched-capacitor instrumentation building block. A pair of switches alternately connects an external capacitor to an input voltage and then connects the charged capacitor across an output port. The internal switches have a break-before-make action. An internal clock is provided and its frequency can be adjusted with an external capacitor. The LTC1043 can also be driven with an external CMOS clock.

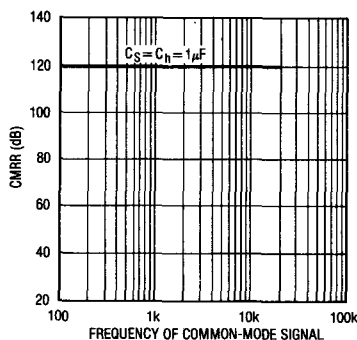
The LTC1043, when used with low clock frequencies, provides ultra precision DC functions without requiring precise external components. Such functions are differential voltage to single-ended conversion, voltage inversion, voltage multiplication and division by 2, 3, 4, 5, etc. The LTC1043 can also be used for precise V-F and F-V circuits without trimming, and it is also a building block for switched-capacitor filters, oscillators and modulators.

The LTC1043 is manufactured using Linear Technology's enhanced L^{TC}MOS™ silicon gate process.

Instrumentation Amplifier



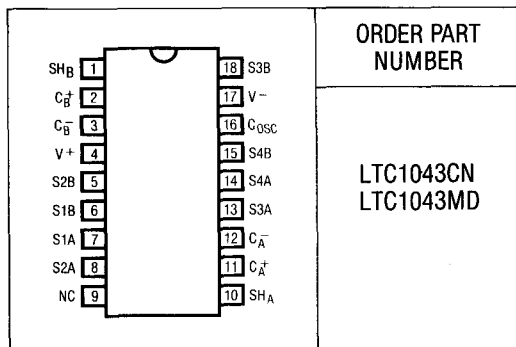
CMRR vs Frequency



ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V^+ to V^-) 18V
 Input Voltage
 at Any Pin $V^- - 0.3V \leq V_{IN} \leq V^+ + 0.3V$
 Operating Temperature Range
 LTC1043C $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$
 LTC1043M $-55^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$
 Storage Temperature Range -65°C to 150°C
 Lead Temperature (Soldering, 10 sec.) 300°C

PACKAGE/ORDER INFORMATION



ELECTRICAL CHARACTERISTICS $v^+ = 10V, v^- = 0V, T_A = 25^\circ\text{C}$ unless otherwise specified.

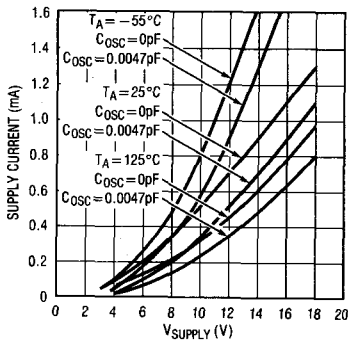
SYMBOL	PARAMETER	CONDITIONS	LTC1043M			LTC1043C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
I_S	Power Supply Current	Pin (16) Connected High or Low	●	0.25	0.4	0.25	0.4	mA	
		C_{OSC} (Pin 16 to V^-) = 100pF	●	0.4	0.65	0.4	0.65	mA	
I_I	OFF Leakage Current	Any Switch, Test Circuit 1 (Note 1)	●	6	100	6	100	pA	
			●	6	500	6		nA	
R_{ON}	ON Resistance	Test Circuit 2, $V_{IN} = 7V, I = \pm 0.5mA$ $V^+ = 10V, V^- = 0V$	●	240	400	240	400	Ω	
R_{ON}	ON Resistance	Test Circuit 2, $V_{IN} = 3.1V, I = \pm 0.5mA$ $V^+ = 5V, V^- = 0V$	●	400	700	400	700	Ω	
f_{OSC}	Internal Oscillator Frequency	C_{OSC} (Pin 16 to V^-) = 0pF		185		185		kHz	
		C_{OSC} (Pin 16 to V^-) = 100pF	●	20	34	50	20	34	50
		Test Circuit 3	●	15	75	15	75		
I_{OSC}	Pin Source or Sink Current	Pin 16 at V^+ or V^-	●	40	70	40	70	μA	
			●		100		100	μA	
	Break-Before-Make Time			25		25		ns	
	Clock to Switching Delay	C_{OSC} Pin Externally Driven		75		75		ns	
f_M	Maximum External CLK Frequency	C_{OSC} Pin Externally Driven with CMOS Levels		5		5		MHz	
CMRR	Common-Mode Rejection Ratio	$V^+ = 5V, V^- = -5V, -5V < V_{CM} < 5V, DC$ to 400Hz		120		120		dB	

The ● denotes the specifications which apply over the full operating temperature range: LTC1043M operates from $-55^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$; LTC1043C operates from $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$.

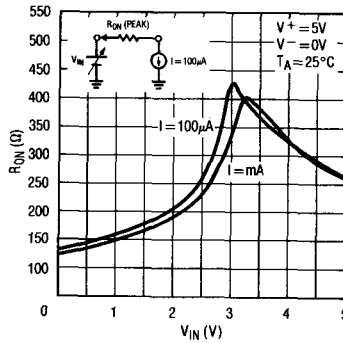
Note 1: OFF leakage current is guaranteed but not tested at 25°C .

TYPICAL PERFORMANCE CHARACTERISTICS (Test Circuits 2 through 4)

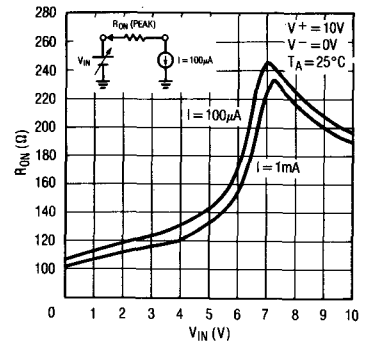
Power Supply Current vs Power Supply Voltage



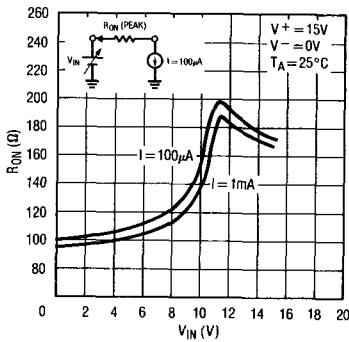
R_{ON} vs V_{IN}



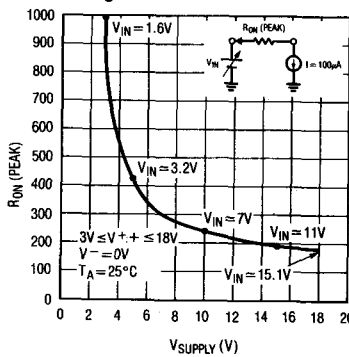
R_{ON} vs V_{IN}



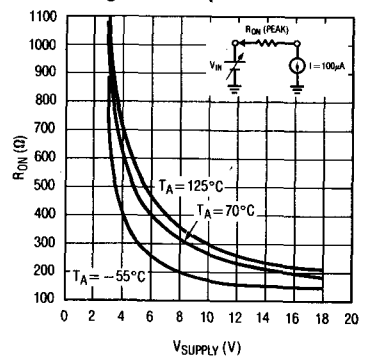
R_{ON} vs V_{IN}



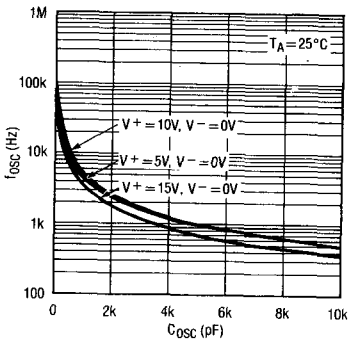
R_{ON} (Peak) vs Power Supply Voltage



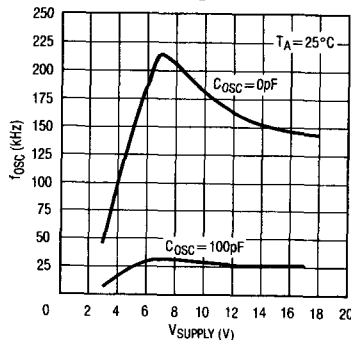
R_{ON} (Peak) vs Power Supply Voltage and Temperature



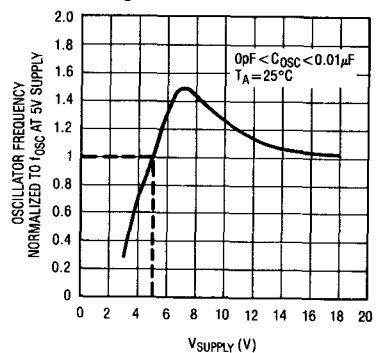
Oscillator Frequency, f_{OSC} , vs C_{OSC}



Oscillator Frequency, f_{OSC} , vs Supply Voltage

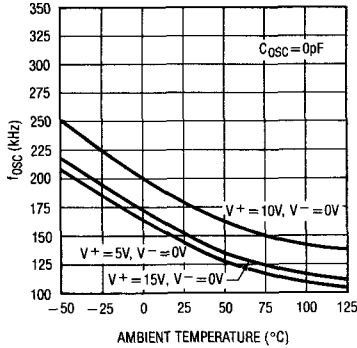


Normalized Oscillator Frequency, f_{OSC} , vs Supply Voltage

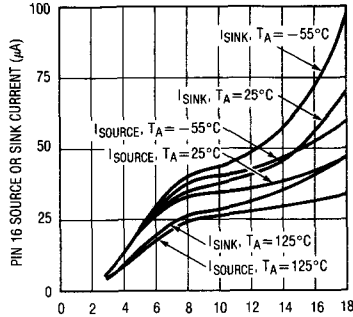


TYPICAL PERFORMANCE CHARACTERISTICS (Test Circuits 2 through 4)

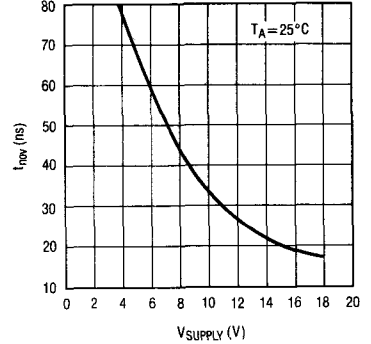
Oscillator Frequency, f_{osc} , vs Ambient Temperature, T_A



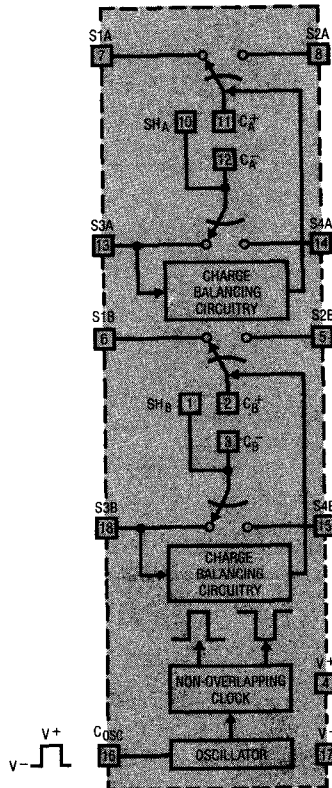
C_{osc} Pin I_{SINK} , I_{SOURCE} vs Supply Voltage



Break-Before-Make Time, t_{nov} , vs Supply Voltage



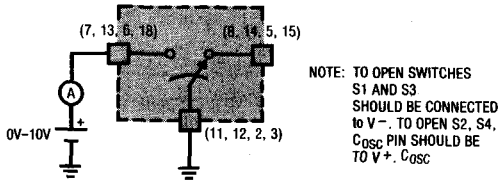
BLOCK DIAGRAM



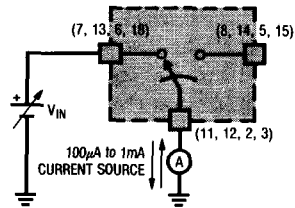
THE SWITCHES ARE TIMED AS SHOWN WITH PIN 16 HIGH

THE CHARGE BALANCING CIRCUITRY SAMPLES THE VOLTAGE AT S3 WITH RESPECT TO S4 (PIN 16 HIGH) AND INJECTS A SMALL CHARGE AT THE C+ (PIN 16 LOW). THIS BOOSTS THE CMRR WHEN THE LTC1043 IS USED AS AN INSTRUMENTATION AMPLIFIER FRONT END. FOR MINIMUM CHARGE INJECTION IN OTHER TYPES OF APPLICATIONS, S3A AND S3B SHOULD BE GROUNDDED.

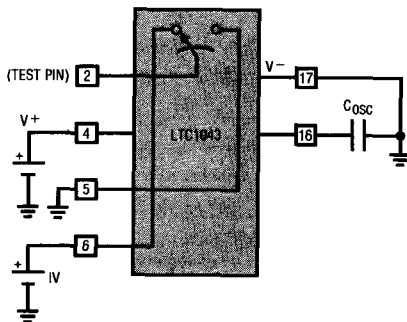
TEST CIRCUITS



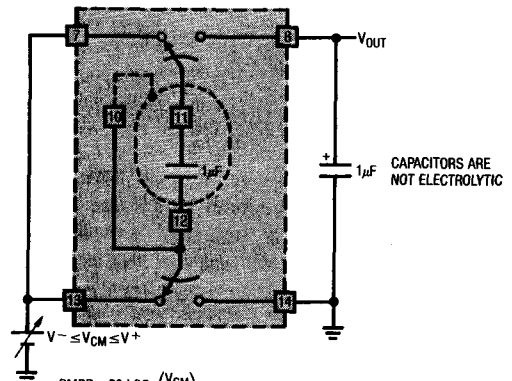
Test Circuit 1. Leakage Current Test



Test Circuit 2. R_{ON} Test



Test Circuit 3. Oscillator Frequency, f_{osc}



Test Circuit 4. CMRR Test

APPLICATIONS INFORMATION

Common-Mode Rejection Ratio (CMRR)

The LTC1043, when used as a differential to single-ended converter (Figure 1) rejects common-mode signals and preserves differential voltages. Unlike other techniques, the LTC1043's CMRR does not degrade with increasing common-mode voltage frequency. During the sampling mode, the impedance of pins 2, 3 (and 11, 12) should be reasonably balanced, otherwise, common-mode signals will appear differentially. The value of the CMRR depends on the value of the sampling and holding capacitors (C_S , C_H) and on the sampling frequency. Since the common-mode voltages are not sampled, the common-mode signal frequency can well exceed the sampling frequency without experiencing aliasing phenomena. The CMRR of Figure 1

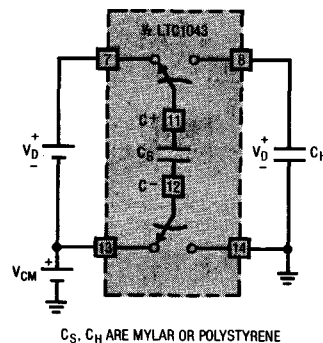


Figure 1. Differential to Single-Ended Converter

APPLICATIONS INFORMATION

is measured by shorting pins 7 and 13 and by observing, with a precision DVM, the change of the voltage across C_H with respect to an input CM voltage variation. During the sampling and holding mode, charges are being transferred and minute voltage transients will appear across the holding capacitor. Although the R_{ON} on the switches is low enough to allow fast settling, as the sampling frequency increases, the rate of charge transfer increases and the average voltage measured with a DVM across it will increase proportionally; this causes the CMRR of the sampled data system, as seen by a "continuous" instrument (DVM), to decrease, Figure 2.

Switch Charge Injection

Figure 3 shows one out of the eight switches of the LTC1043, configured as a basic sample and hold circuit. When the switch opens, a "hold step" is observed and its magnitude depends on the value of the input voltage. Figure 4 shows charge injected into the hold capacitor. For instance, a $2pC_b$ of charge injected into a $0.01\mu F$ capacitor causes a $200\mu V$ hold step. As shown in Figure 4, there is a predictable and repeatable charge injection cancellation when the input voltage is close to half the supply voltage of the LTC1043. This is a unique feature of this product, containing charge-balanced switches fabricated with a self-aligning gate CMOS process. Any switch of the LTC1043, when powered with symmetrical dual supplies, will sample and hold small signals around ground without any significant error.

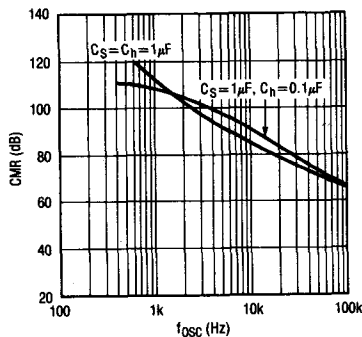


Figure 2. CMRR vs Sampling Frequency

Shielding the Sampling Capacitor for Very High CMRR

Internal or external parasitic capacitors from the C^+ pin(s) to ground affect the CMRR of the LTC1043, (Figure 1). The common-mode error due to the internal junction capacitances of the C^+ pin(s) 2 and 11 is cancelled through internal circuitry. The C^+ pin, therefore, should be used as the top plate of the sampling capacitor. The interpin capacitance between pin 2 and dummy pin 1 (11 and 10) appears in parallel with the sampling capacitor so it does not degrade the CMRR. A shield placed underneath the sampling capacitor (Figure 5) and connected to either pin 1 or 3 helps to boost the CMRR in excess of 120dB.

Excessive external parasitic capacitance between the C^- pins and ground indirectly degrades CMRR; this becomes visible especially when the LTC1043 is used with clock frequencies above 2kHz. Because of this, if a shield is used, the parasitic capacitance between the shield and circuit ground should be minimized.

It is recommended that the outer plate of the sampling capacitor be connected to the C^- pin(s).

Input Pins, SCR Sensitivity

An internal 60Ω resistor is connected in series with the input of the switches (pins 5, 6, 7, 8, 13, 14, 15, 18) and it is included in the R_{ON} specification. When the input voltage exceeds the power supply by a diode drop, current will flow into the input pin(s). The LTC1043 will not

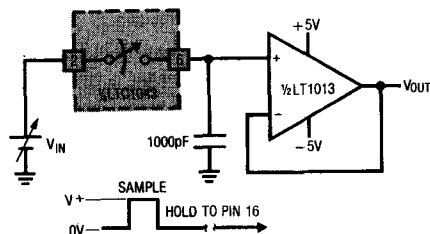


Figure 3

APPLICATIONS INFORMATION

latch until the input current reaches 2mA–3mA. The device will recover from the latch mode when the input drops 3V–4V below the voltage value which caused the latch. For instance, if an external resistor of 200Ω is connected in series with an input pin, the input can be taken 1.3V above the supply without latching the IC. The same applies for the C⁺ and C⁻ pins.

C_{osc} Pin (16), Figure 6

The C_{osc} pin can be used with an external capacitor, C_{osc}, connected from pin 16 to pin 17, to modify the internal oscillator frequency. If pin 16 is floating, the internal 24pF capacitor plus any external interpin capacitance set the oscillator frequency around 190kHz with ±5V supply. The typical performance characteristics curves provide the necessary information to set the oscillator fre-

quency for various power supply ranges. Pin 16 can also be driven with an external clock to override the internal oscillator. Although standard 7400 series CMOS gates do not guarantee CMOS levels with the current source and sink requirements of pin 16, they will in reality drive the C_{osc} pin. CMOS gates conforming to standard B series output drive have the appropriate voltage levels and more than enough output current to simultaneously drive several LTC1043 C_{osc} pins. The typical trip levels of the Schmitt trigger, Figure 6, are given below.

SUPPLY	TRIP LEVELS	
V ⁺ = 5V, V ⁻ = 0V	V _H = 3.4V	V _L = 1.35V
V ⁺ = 10V, V ⁻ = 0V	V _H = 6.5V	V _L = 2.8V
V ⁺ = 15V, V ⁻ = 0V	V _H = 9.5V	V _L = 4.1V

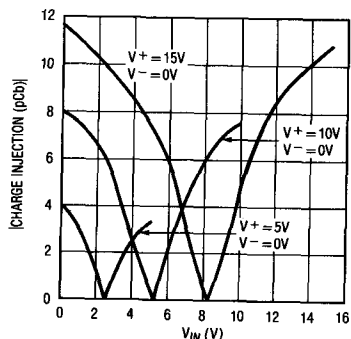


Figure 4. Individual Switch Charge Injection vs Input Voltage

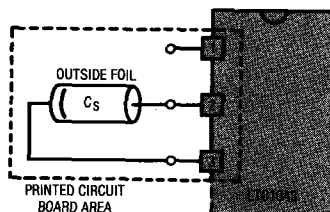
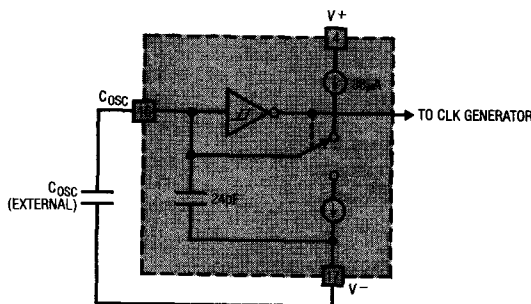


Figure 5. Printed Circuit Board Layout Showing Shielding the Sampling Capacitor

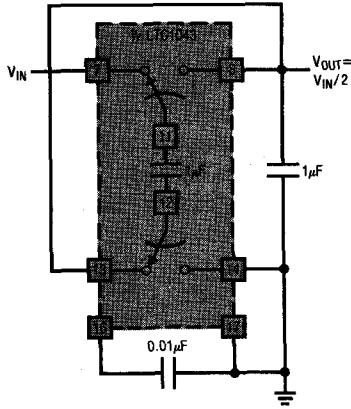


$$f_{osc} = 190\text{kHz} \times \frac{(24\text{pF})}{(24\text{pF} + C_{osc})}$$

Figure 6. Internal Oscillator

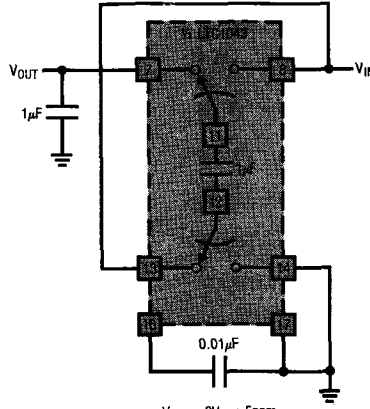
APPLICATIONS

Divide by 2



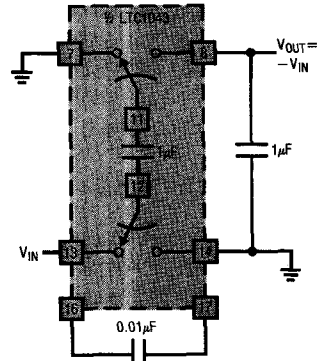
$V_{OUT} = V_{IN}/2 \pm 1\text{ppm}$
 $0 \leq V_{IN} \leq V^+$
 $3 \leq V^+ \leq 18\text{V}$

Multiply by 2



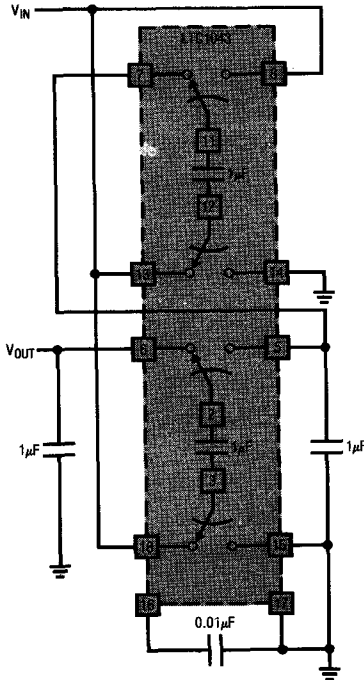
$V_{OUT} = 2V_{IN} \pm 5\text{ppm}$
 $0 \leq V_{IN} < V^+/2$
 $3 \leq V^+ \leq 18\text{V}$

Ultra Precision Voltage Inverter



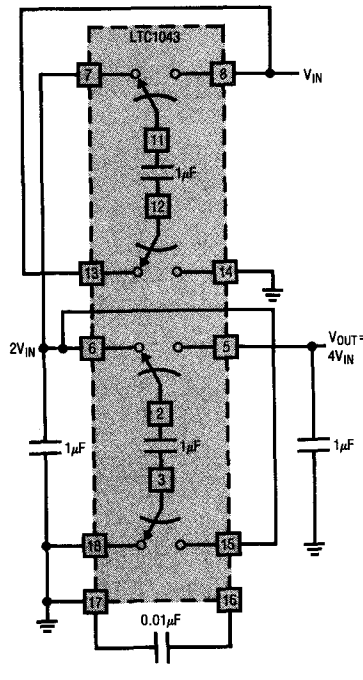
$V_{OUT} = -V_{IN} \pm 2\text{ppm}$
 $V^- < V_{IN} < V^+$
 $V^+ = +5\text{V}, V^- = -5\text{V}$

Precision Multiply by 3



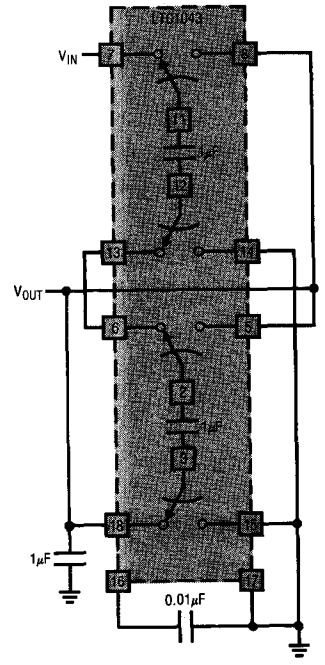
$V_{OUT} = 3V_{IN} \pm 10\text{ppm}$
 $0 < V_{IN} < V^+/3$
 $3\text{V} < V^+ < 18\text{V}$

Precision Multiply by 4



$V_{OUT} = 4V_{IN} \pm 40\text{ppm}$
 $0 \leq V_{IN} \leq V^+/4$
 $3\text{V} < V^+ < 18\text{V}$

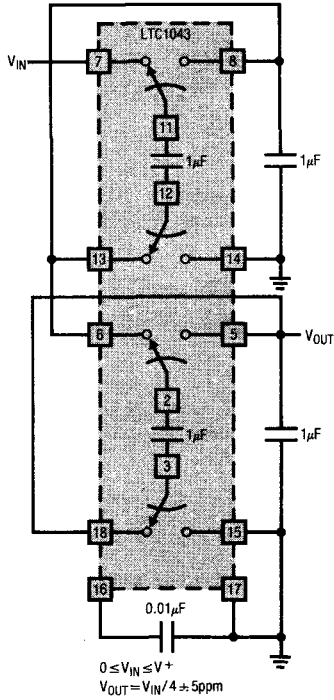
Divide by 4



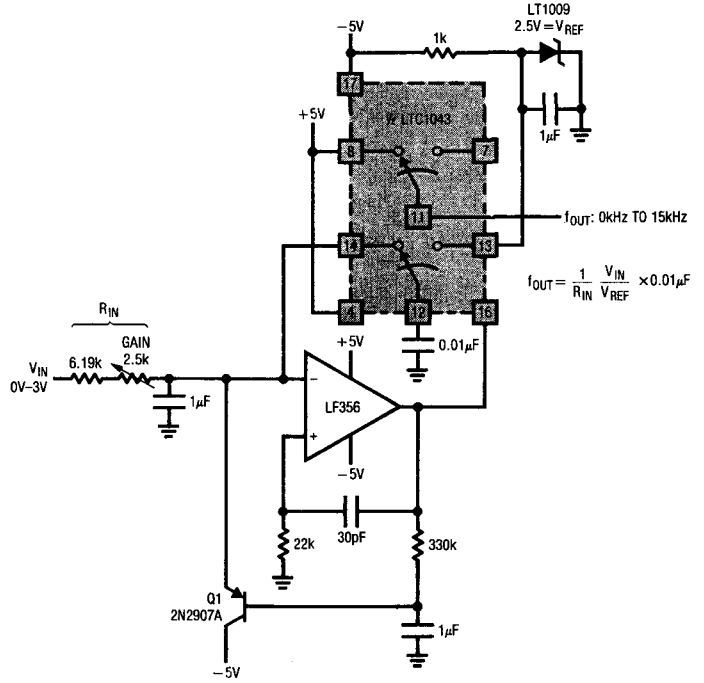
$V_{OUT} = V_{IN}/4 \pm 3\text{ppm}$
 $0 \leq V_{IN} \leq V^+$

APPLICATIONS

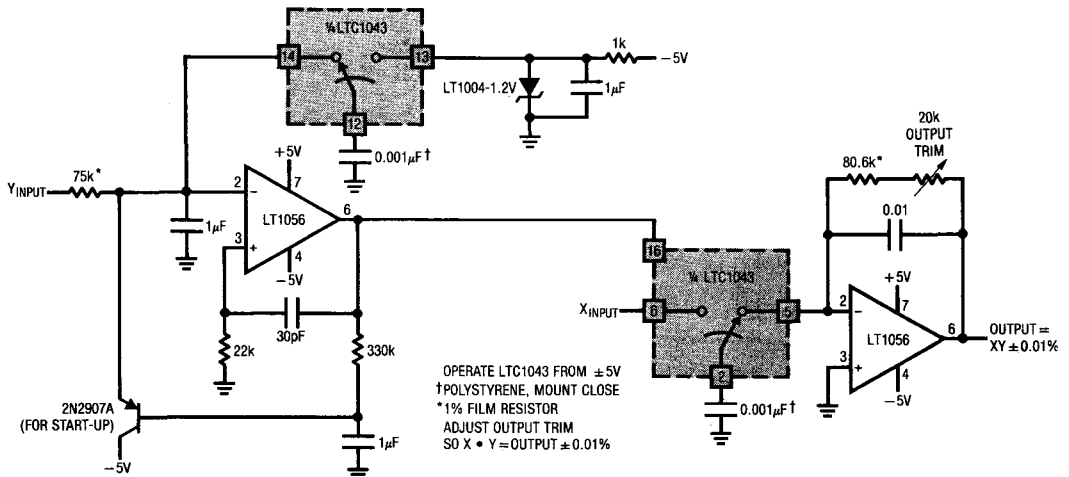
Divide by 4



0.005% V → F Converter

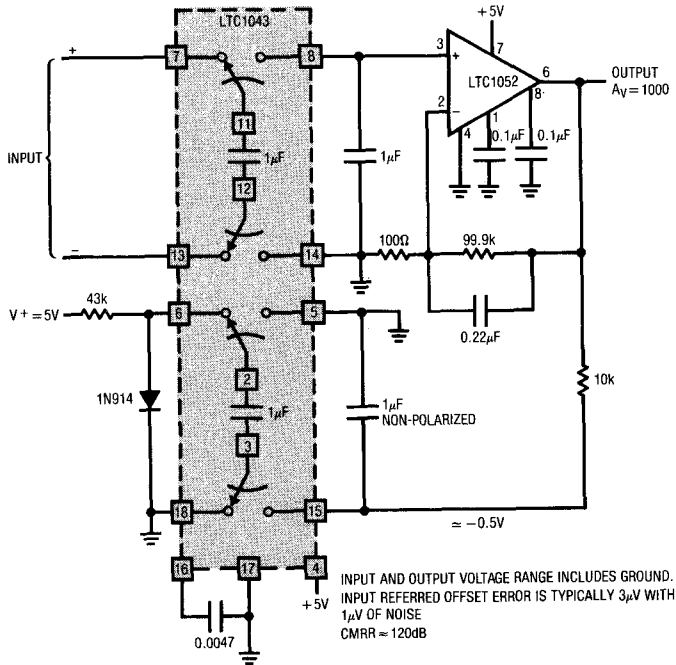


0.01% Analog Multiplier

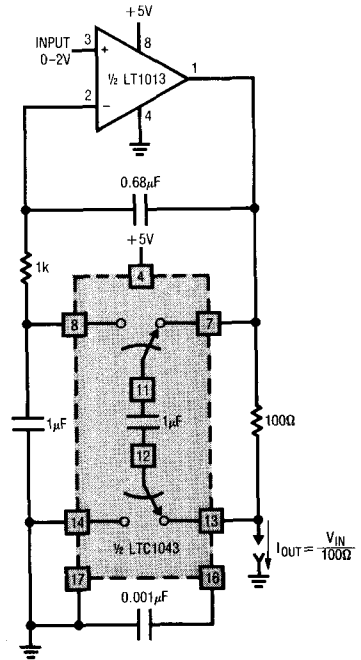


APPLICATIONS

Single 5V Supply, Ultra Precision Instrumentation Amplifier

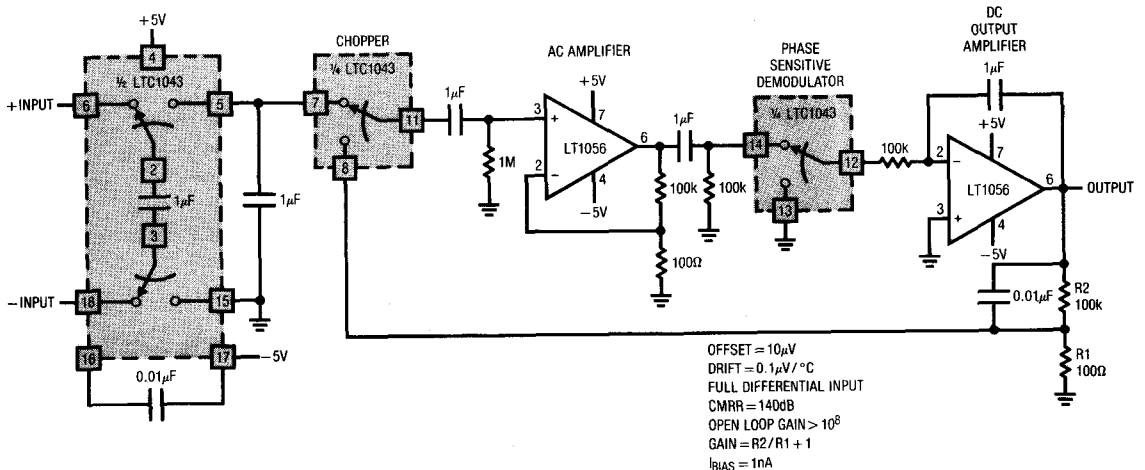


Voltage Controlled Current Source with Ground Referred Input and Output



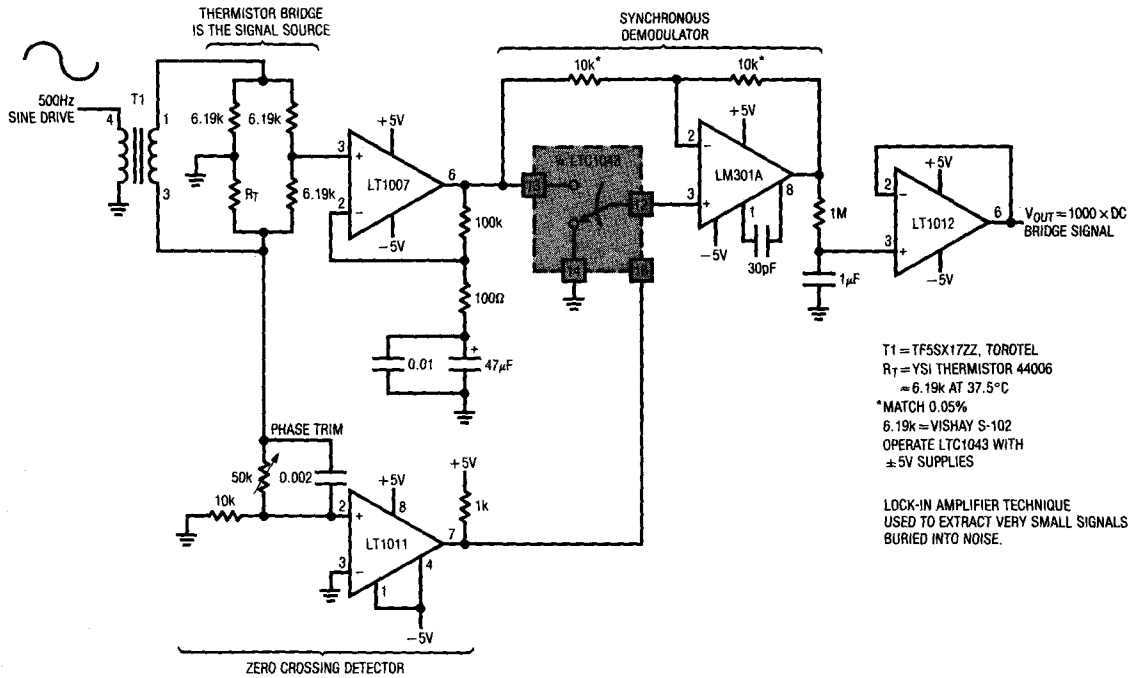
OPERATES FROM A SINGLE 5V SUPPLY

Precision Instrumentation Amplifier

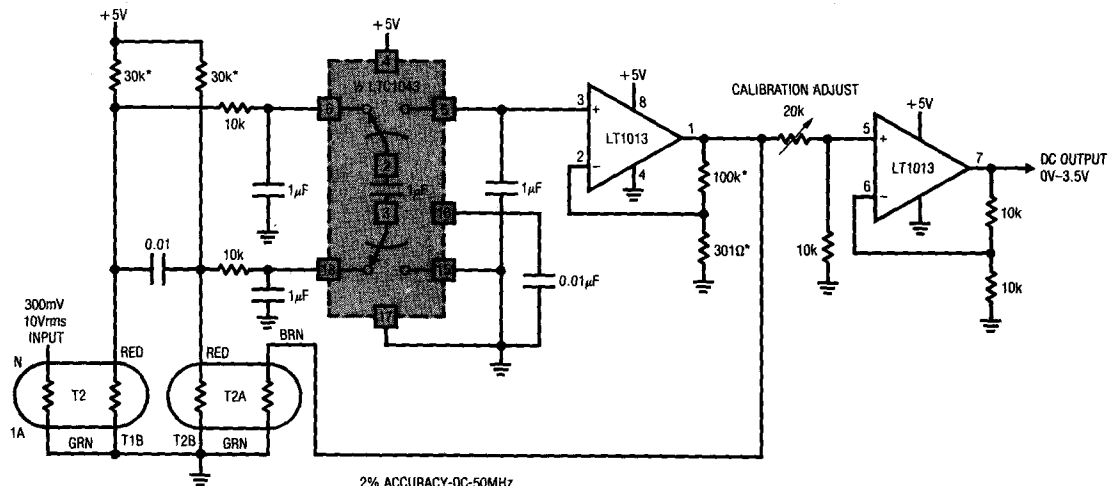


APPLICATIONS

Lock-In Amplifier (=Extremely Narrow-Band Amplifier)



50MHz Thermal rms → DC Converter

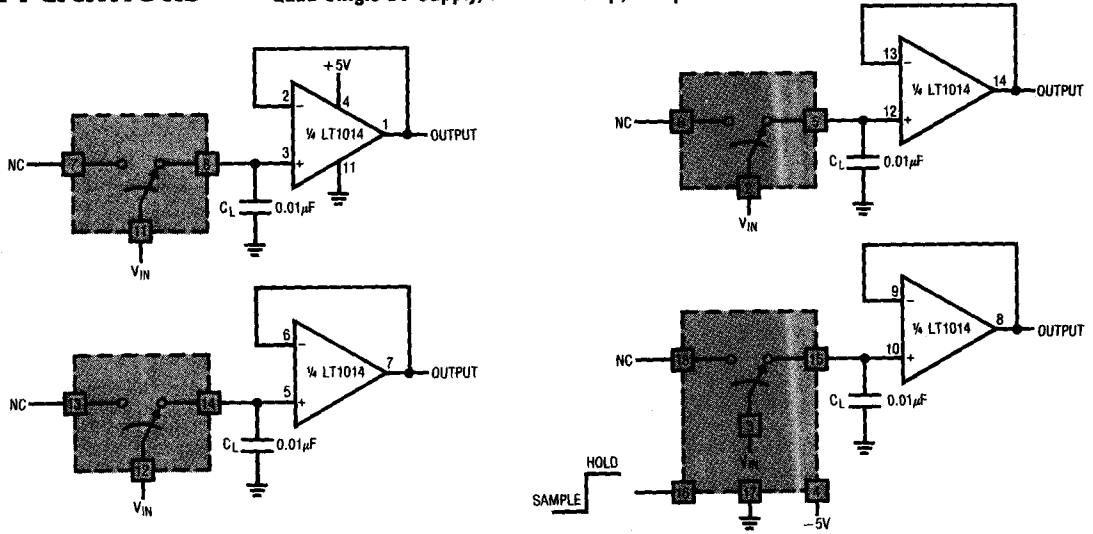


2% ACCURACY-DC-50MHz
 100:1 CREST FACTOR CAPABILITY
 T1-T2 = YELLOW SPRINGS INST. CO. THERMISTOR COMPOSITE
 ENCLOSE T1 AND T2 IN STYROFOAM

*1% RESISTOR

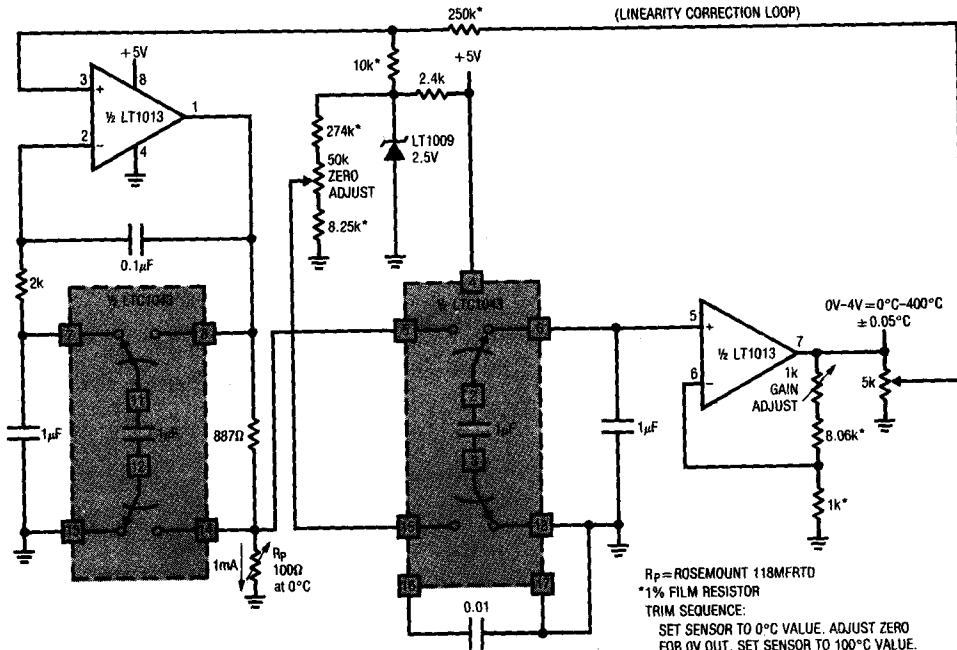
APPLICATIONS

Quad Single 5V Supply, Low Hold Step, Sample and Hold



FOR $1V \leq V_{IN} \leq 4V$, THE HOLD STEP IS $\leq 300\mu V$.
ACQUISITION TIME $\sim 8 \times R_{ON} C_H$ FOR 10-BIT ACCURACY.

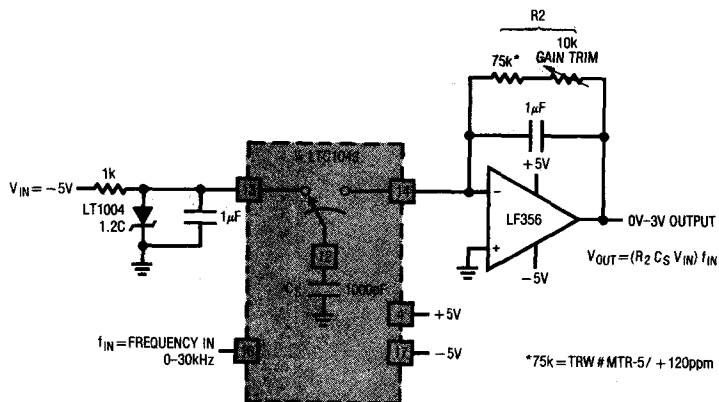
Single Supply Precision Linearized Platinum RTD Signal Conditioner



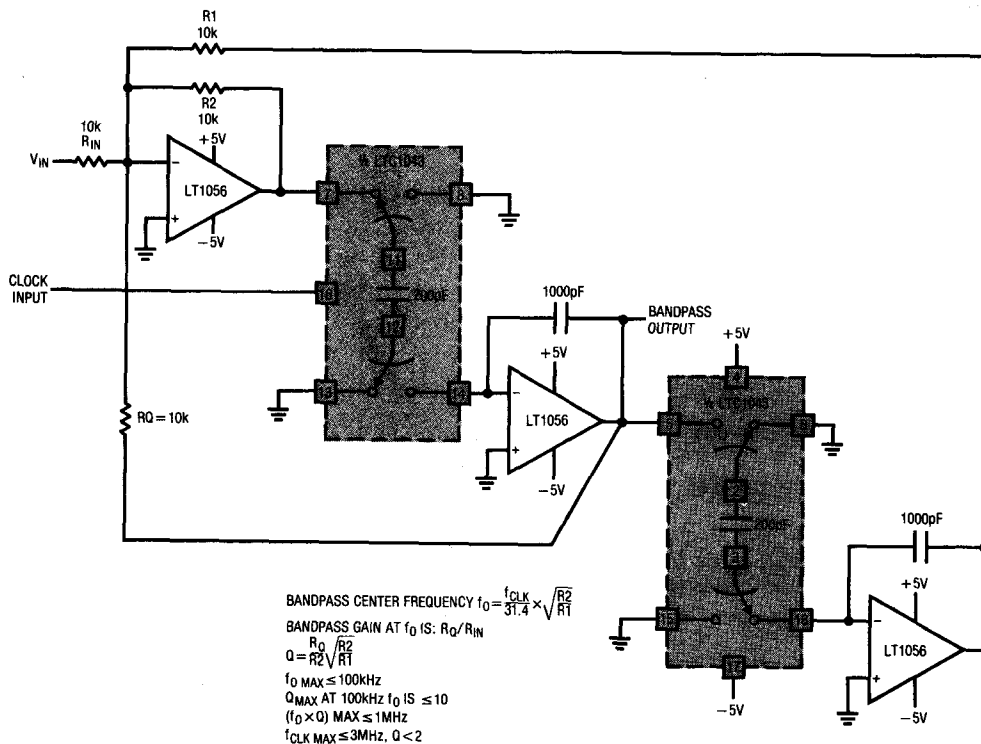
R_p = ROSEMOUNT 118MFRTD
*1% FILM RESISTOR
TRIM SEQUENCE:
SET SENSOR TO 0°C VALUE. ADJUST ZERO FOR 0V OUT. SET SENSOR TO 100°C VALUE. ADJUST GAIN FOR 1,000V OUT. SET SENSOR TO 400°C VALUE. ADJUST LINEARITY FOR 4,000V OUT. REPEAT AS REQUIRED.

APPLICATIONS

0.005% F → V Converter

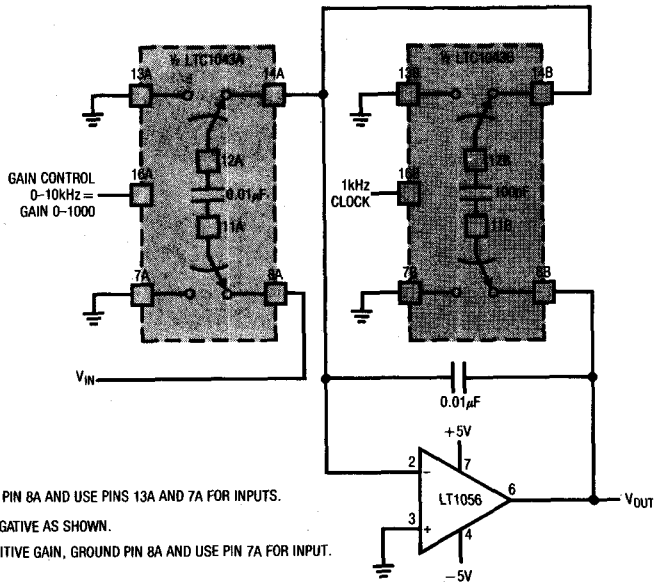


High Frequency Clock Tunable Bandpass Filter



APPLICATIONS

Frequency-Controlled Gain Amplifier

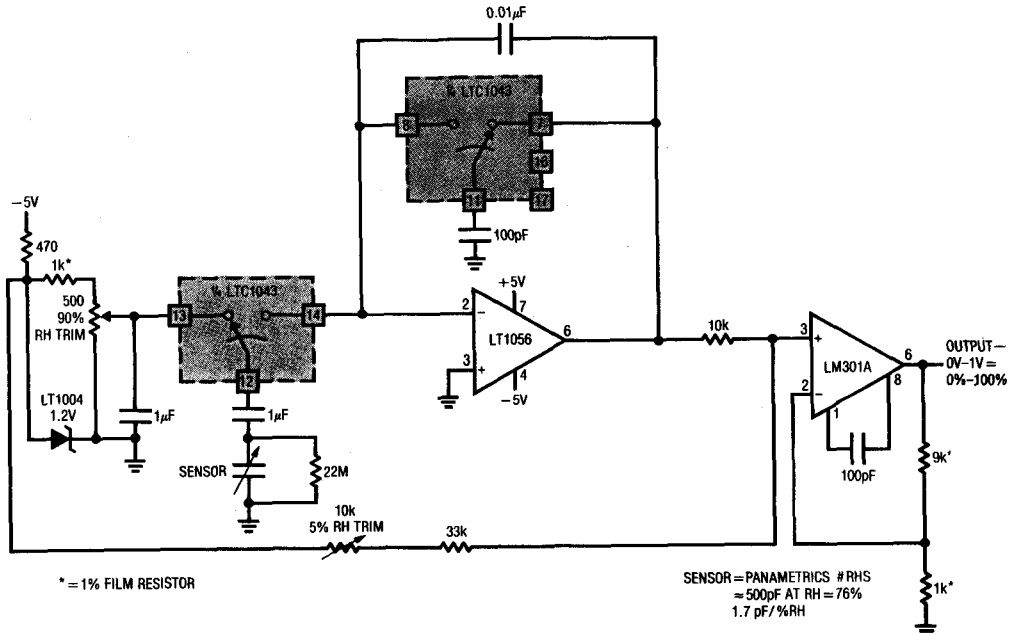


FOR DIFFERENTIAL INPUT, GROUND PIN 8A AND USE PINS 13A AND 7A FOR INPUTS.

$GAIN = \frac{f_{IN} \times 0.01\mu F}{1kHz \times 100pF}$; GAIN IS NEGATIVE AS SHOWN.

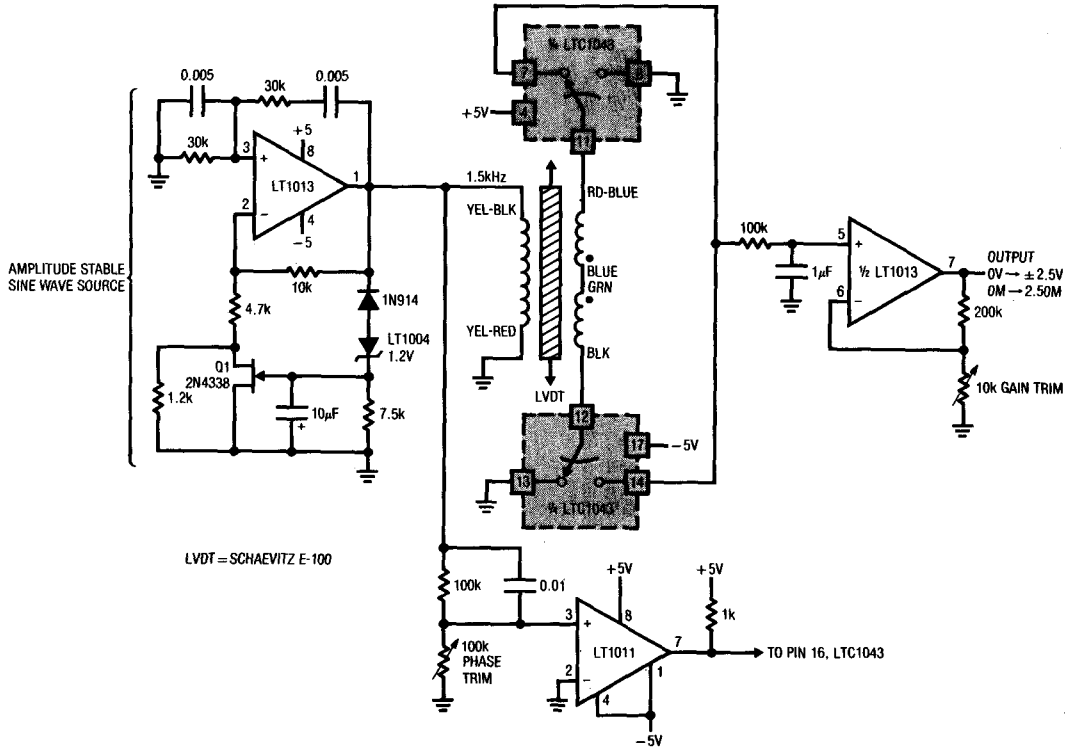
FOR SINGLE-ENDED INPUT AND POSITIVE GAIN, GROUND PIN 8A AND USE PIN 7A FOR INPUT.
USE $\pm 5V$ SUPPLIES FOR LTC1043.

Relative Humidity Sensor Signal Conditioner

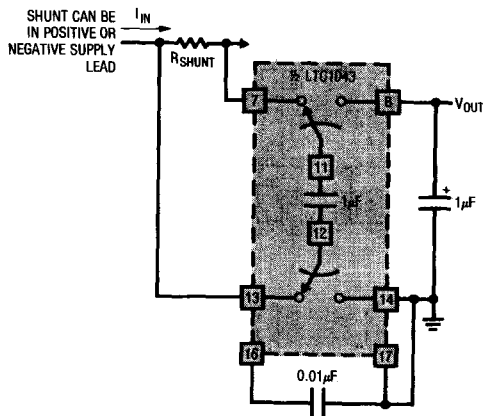


APPLICATIONS

Linear Variable Differential Transformer (LVDT), Signal Conditioner

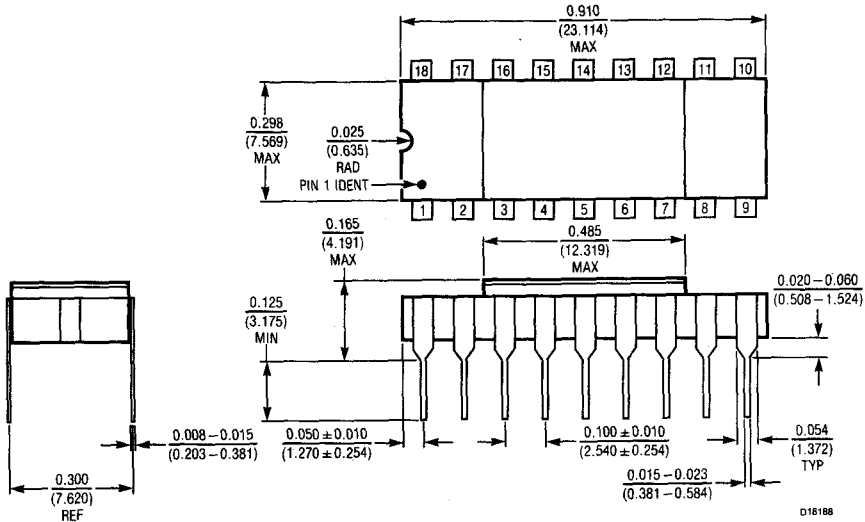


Precision Current Sensing in Supply Rails



PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

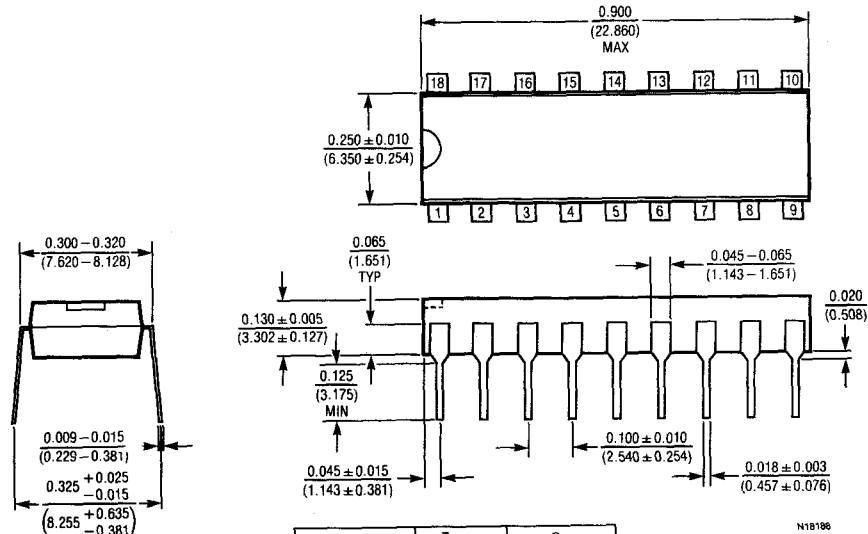
D Package
18 Lead Side Brazed



D16188

	T _{jmax}	Θ _{ja}
LTC1043MD	150°C	100°C/W
LTC1043CD	150°C	100°C/W

N Package
18 Lead Plastic DIP



N18186

	T _{jmax}	Θ _{ja}
LTC1043CN	100°C	100°C/W

Dual Precision Instrumentation Switched-Capacitor Building Block

FEATURES

- Instrumentation Front End with 120dB CMRR
- Precise, Charge-Balanced Switching
- Operates from 3V to 18V
- Internal or External Clock
- Operates up to 5MHz Clock Rate
- Low Power
- Two Independent Sections with One Clock

APPLICATIONS

- Precision Instrumentation Amplifiers
- Ultra Precision Voltage Inverters, Multipliers and Dividers
- V-F and F-V Converters
- Sample and Hold
- Switched-Capacitor Filters

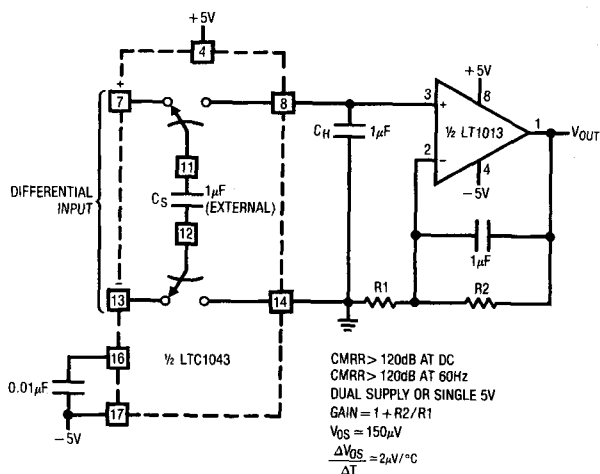
DESCRIPTION

The LTC1043 is a monolithic, charge-balanced, dual switched-capacitor instrumentation building block. A pair of switches alternately connects an external capacitor to an input voltage and then connects the charged capacitor across an output port. The internal switches provide a break-before-make action. An internal clock is provided and its frequency can be adjusted with an external capacitor. The LTC1043 can also be driven with an external CMOS clock.

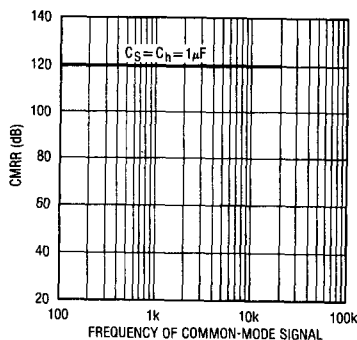
The LTC1043, when used with low clock frequencies, provides ultra precision DC functions without requiring precise external components. Such functions are differential voltage to single-ended conversion, voltage inversion, voltage multiplication and division by 2, 3, 4, 5, etc. The LTC1043 can also be used for precise V-F and F-V circuits without trimming, and it is also a building block for switched-capacitor filters, oscillators and modulators.

The LTC1043 is manufactured using Linear Technology's enhanced L^TCMOS™ silicon gate process.

Instrumentation Amplifier



CMRR vs Frequency

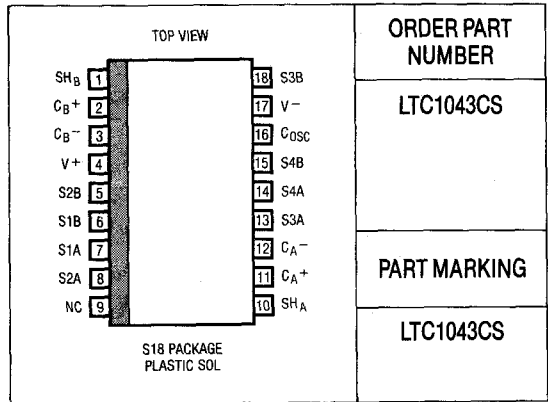


LTC1043CS

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	18V
Input Voltage at Any Pin	$-0.3V \leq V_{IN} \leq V^+ + 0.3V$
Operating Temperature Range.....	$-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$
Storage Temperature Range.....	-65°C to 150°C
Lead Temperature (Soldering, 10 sec.).....	300°C

PACKAGE/ORDER INFORMATION



ORDER PART NUMBER

LTC1043CS

PART MARKING

LTC1043CS

ELECTRICAL CHARACTERISTICS $V^+ = 10V, V^- = 0V, T_A = 25^{\circ}\text{C}$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	LTC1043C			UNITS
			MIN	TYP	MAX	
I_s	Power Supply Current	Pin 16 Connected High or Low	●	0.25	0.4	mA
		C_{osc} (Pin 16 to V^-) = 100pF	●	0.4	0.65	mA
I_l	OFF Leakage Current	Any Switch, Test Circuit 1 (Note 1)	●	6	100	pA
			●	6		nA
R_{ON}	ON Resistance	Test Circuit 2, $V_{IN} = 7V, I = \pm 0.5mA$ $V^+ = 10V, V^- = 0V$	●	240	400	Ω
R_{ON}	ON Resistance	Test Circuit 2, $V_{IN} = 3.1V, I = \pm 0.5mA$ $V^+ = 5V, V^- = 0V$	●	400	700	Ω
f_{osc}	Internal Oscillator Frequency	C_{osc} (Pin 16 to V^-) = 0pF		20	185	kHz
		C_{osc} (Pin 16 to V^-) = 100pF	●	34	50	kHz
I_{osc}	Pin Source or Sink Current	Pin 16 at V^+ or V^-	●	40	70	μA
			●		100	μA
	Break-Before-Make-Time			25		ns
	Clock to Switching Delay	C_{osc} Pin Externally Driven		75		ns
f_M	Maximum External CLK Frequency	C_{osc} Pin Externally Driven with CMOS Levels		5		MHz
CMRR	Common-Mode Rejection Ratio	$V^+ = 5V, V^- = -5V, -5V < V_{CM} < 5V, DC$ to 400Hz		120		dB

The ● denotes specifications which apply over the full operating temperature range. LTC1043 operates from $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$.

Note 1: OFF leakage current is guaranteed but not tested at 25°C .

Wideband RMS-DC Converter Building Block

FEATURES

- 300MHz 3dB Bandwidth
- 1% Accuracy DC-50MHz
- 2% to 100MHz
- Bandwidth Flat Over Input Voltage Range
- 50:1 Crest Factor
- 20:1 Dynamic Range
- 35V Peak Input
- Thermally Based Operation
- Fully Specified Thermal and Electrical Parameters
- Standard IC Packages
- Resistive Inputs

DESCRIPTION

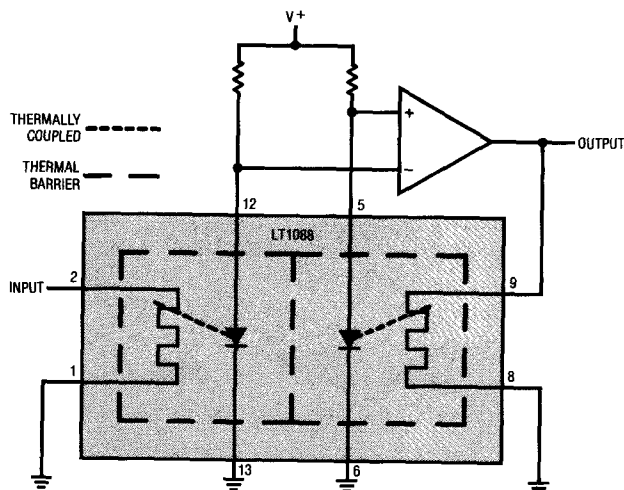
The LT1088 is a thermally based RMS-DC converter building block. It converts the input waveform to heat. Using external circuitry, the thermal signal is expressed as a DC output voltage.

LTC's proprietary thermal packaging process permits accurate thermal signal processing in a standard IC package. The thermal method provides far greater bandwidth than RMS converters based on logarithmic computing techniques. The LT1088's high voltage breakdown allows crest factor measurements of 50:1 and operation over a 20:1 input dynamic range. Resistive inputs of 50 Ω or 250 Ω accommodate drive from a wide variety of sources.

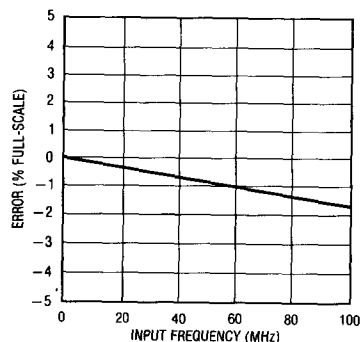
APPLICATIONS

- Wideband RMS Voltmeters
- RF Leveling Loops
- Wideband AGC
- High Crest Factor Measurements
- SCR Power Monitoring

Simplified RMS-DC Converter



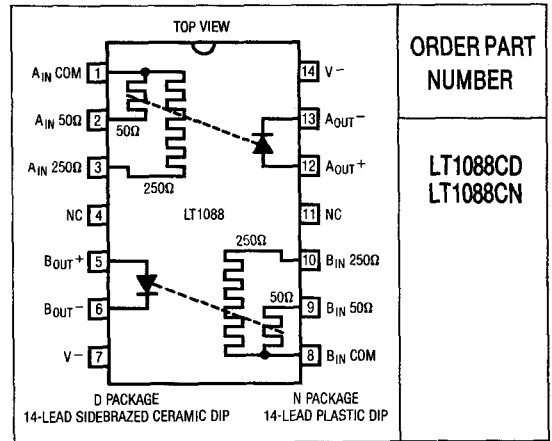
Accuracy vs Frequency (50 Ω Input)



ABSOLUTE MAXIMUM RATINGS

Voltage on Any Pin	$V^- + 40V$ to V^-
Voltage from Channel A to Channel B	100V
Reverse Diode Voltage	3.5V
Forward Diode Current	15mA
Input Power (25°C)	0.375W
Peak Input Power (30 sec)	0.435W
Derate Power at $-3mW/^\circ C$ above 25°C	
Maximum Die Temperature	150°C
Peak Die Temperature (30 sec)	175°C
Functional Temperature Range	$-55^\circ C$ to $125^\circ C$
Operating Temperature Range	$-40^\circ C$ to $85^\circ C$
Lead Temperature (Soldering, 10 sec)	300°C

PACKAGE/ORDER INFORMATION



ORDER PART NUMBER

LT1088CD
LT1088CN

ELECTRICAL CHARACTERISTICS $T_A = 25^\circ C$, unless otherwise noted (See Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS		
Input Heaters							
50Ω Input		40	50	60	Ω		
250Ω Input		200	250	300	Ω		
50Ω Temperature Coefficient		●	2000		ppm/°C		
250Ω Temperature Coefficient		●	2000		ppm/°C		
50Ω Temperature Coefficient Match	Input A to Input B	●	30	500	ppm		
250Ω Temperature Coefficient Match	Input A to Input B	●	30	500	ppm		
Resistance Matching	50Ω Inputs		2	10	%		
	250Ω Inputs		2	10	%		
250Ω to 50Ω Ratio Match		-15	0	5	%		
250Ω to 50Ω Ratio Match Temperature Coefficient		●	50		ppm/°C		
Output Diodes							
Forward Voltage	$I = 5mA$	0.6	0.7	0.8	V		
Forward Voltage Match	Out A to Out B; $I = 5mA$	●	5		mV		
Voltage Temperature Coefficient	$I = 5mA$	●	-1.6	-1.75	-1.9	mV/°C	
Thermal Characteristics							
Thermal Resistance	Either Die to Ambient	LT1088CD	●	200	300	400	°C/W
		LT1088CN	●	140	210	280	°C/W
Thermal Matching	Channel A to Channel B	●	30			°C/W	
Thermal Cross Talk	Channel A to Channel B	LT1088CD	●	2500			°C/W
		LT1088CN	●	1750			°C/W

The ● denotes specifications which apply over full operating temperature range.

Note 1: All electrical testing conducted at 25°C.

TYPICAL PERFORMANCE CHARACTERISTICS

Figure 4's Response vs Frequency—500 Input

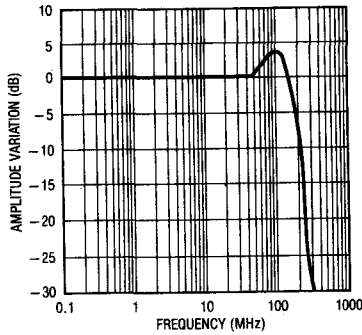
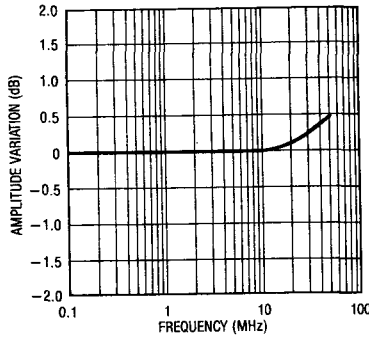
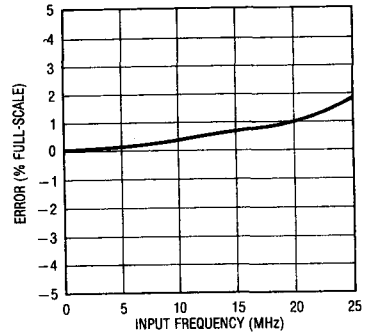


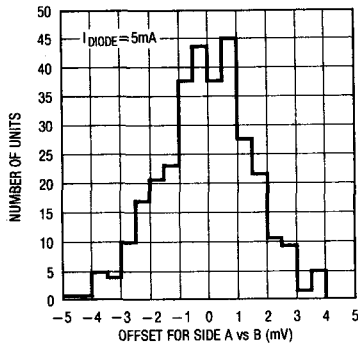
Figure 4's Response vs Frequency—2500 Input



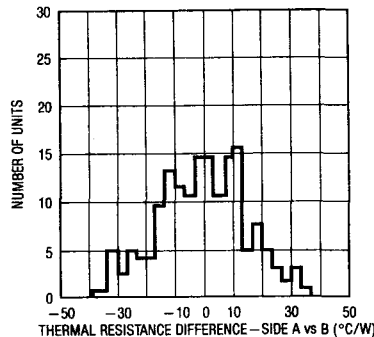
Accuracy vs Frequency for Figure 4—2500 Input



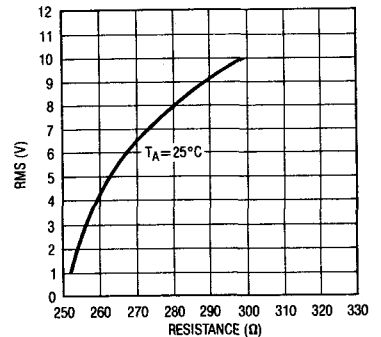
Distribution of Diode Offset Voltage



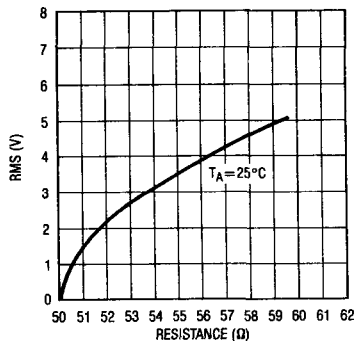
Distribution of Thermal Resistance



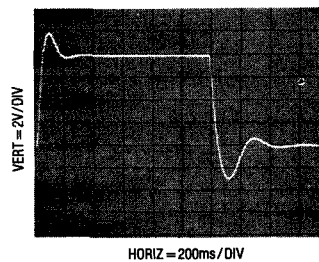
Heater Resistance vs RMS Volts—2500 Heater



Heater Resistance vs RMS Volts—500 Heater



Figures 4's Settling Time (LT1088CD)



APPLICATIONS INFORMATION

Pin Functions

A_{IN} 50Ω, B_{IN} 50Ω, A_{IN} 250Ω, B_{IN} 250Ω (Pins 2, 9, 3, 10): Heater input pins. Input and servo amplifier are connected to these pins. Since the LT1088 is symmetrical, either channel A or B may be used as the input. For higher input impedance, the 50Ω and 250Ω heaters may be series connected. No heater pin may be below V⁻ or more than 40V above V⁻. Maximum heater dissipation must not exceed the absolute maximum ratings.

A_{IN} COM, B_{IN} COM (Pins 1, 8): Common point for the 50Ω and 250Ω input heaters, usually tied to ground.

A_{OUT}⁺, B_{OUT}⁺ (Pins 12, 5): High side of the temperature sensing diodes. Normally they are driven at 5mA from the positive supply. No diode pin may be below V⁻ or more than 40V above V⁻.

A_{OUT}⁻, B_{OUT}⁻ (Pins 13, 6): Low side of the temperature sensing diodes. These pins are normally tied to ground. No diode pin may be below V⁻ or more than 40V above V⁻.

V⁻ (Pins 7, 14): These pins must be the most negative potential of the circuit, usually tied to ground.

Parasitic Diodes

As with all bipolar ICs the LT1088 contains parasitic diodes which must not be forward biased. The parasitic diodes, marked with asterisks, appear in Figure 1. The

dashed lines indicate that all points of the heaters are parasitically diode connected to V⁻.

Thermal Considerations

Because the LT1088's operation depends on thermal symmetry, it is sensitive to external temperature gradients. This is particularly the case for small inputs, which cause the device to run very close to ambient temperature. The device should be mounted in an area which is isothermal and free of drafts. Power generating components should be kept away from the LT1088 and particular caution taken in fan cooled equipment. Under normal conditions no thermal baffle or enclosure is required. Under no circumstances should a heat sink be used.

Heater Protection

Most LT1088 failures will be caused by excessive heater drive. Input power (25°C) is specified at 375mW with 30 second excursions to 435mW permitted. These figures are derated by -3mW/°C above 25°C. Figure 2 plots safe operating limits for input duty cycle vs input voltage. Accidental heater overdrives can damage or destroy the LT1088. In situations where overdrive may occur, some form of heater protection should be employed. Suggested circuits appear in the applications section.

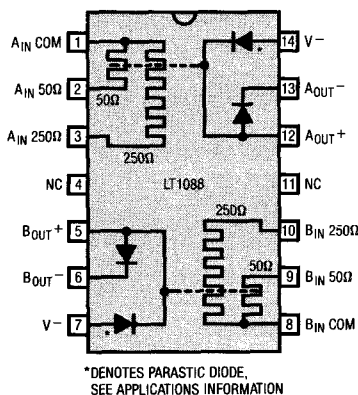


Figure 1

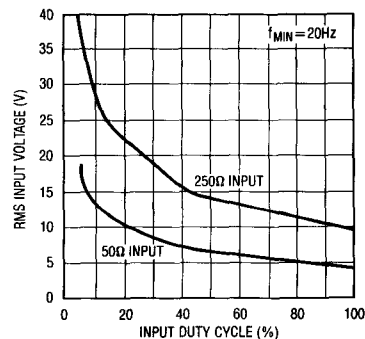


Figure 2. Safe Operating Limits

APPLICATIONS INFORMATION

Filtering

The LT1088's thermal time constant provides effective low pass filtering. Low frequency cut-off is set by servo loop time constants. For the 3300pF value given in the basic RMS-DC application, the circuit begins to follow the input below about 50Hz. Normally, this is not a problem, because the LT1088's primary application will be at high frequency. Lower frequency operation is obtainable by increasing the 3300pF value, although settling time will increase proportionally.

Crest Factor

Crest factor is defined as the ratio of peak input voltage to RMS value. Crest factor performance is set by IC breakdown limits and the usable low input power range. Breakdown limits are a function of processing. The usable low input power range is a basic signal-to-noise conflict. Low input power produces small amounts of signal. This makes accurate, stable discrimination between desired inputs and ambient thermal phenomena uncertain and noisy. These constraints set crest factor at 50:1 for the 50 Ω input and 40:1 for the 250 Ω input.

Layout

At frequencies above 10MHz, input connections require care. Parasitic inductance builds quickly in wire runs, so

the LT1088's input heater lead should be *directly* connected to the source to be measured. It is also wise to shield the input line from the rest of the circuit. The heater common should be returned *directly* to a ground plane. An additional precaution is to mount the 0.01 μ F bypass capacitors right at the LT1088 package. These units minimize the effects of RF pick-up by the temperature sensing diodes.

Accuracy

Amplitude measurement at high frequency to significant accuracy is difficult because of parasitic effects. At frequencies much above 5MHz, small parasitic capacitive and inductive terms become important. The accuracy figures quoted for the applications circuits were taken against certified standards utilizing direct and transfer techniques. Thermal transfer standards (Fluke Model 540B with A-55 converters) certified to 50MHz were used as references. The data above 50MHz was also taken with these references, although the individual units used had not been certified at these frequencies. The accuracy of units of this type which have been certified is normally inside the tolerances listed, so there is good probability the data is valid.

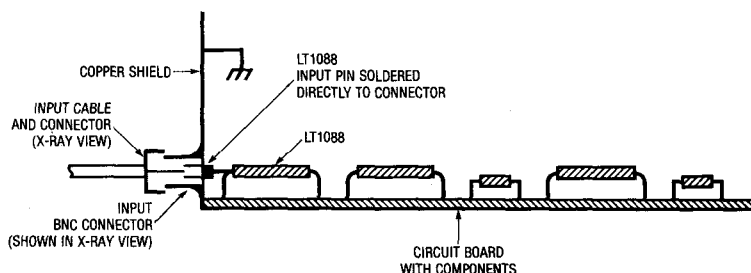


Figure 3. Typical Evaluation Layout

APPLICATIONS INFORMATION

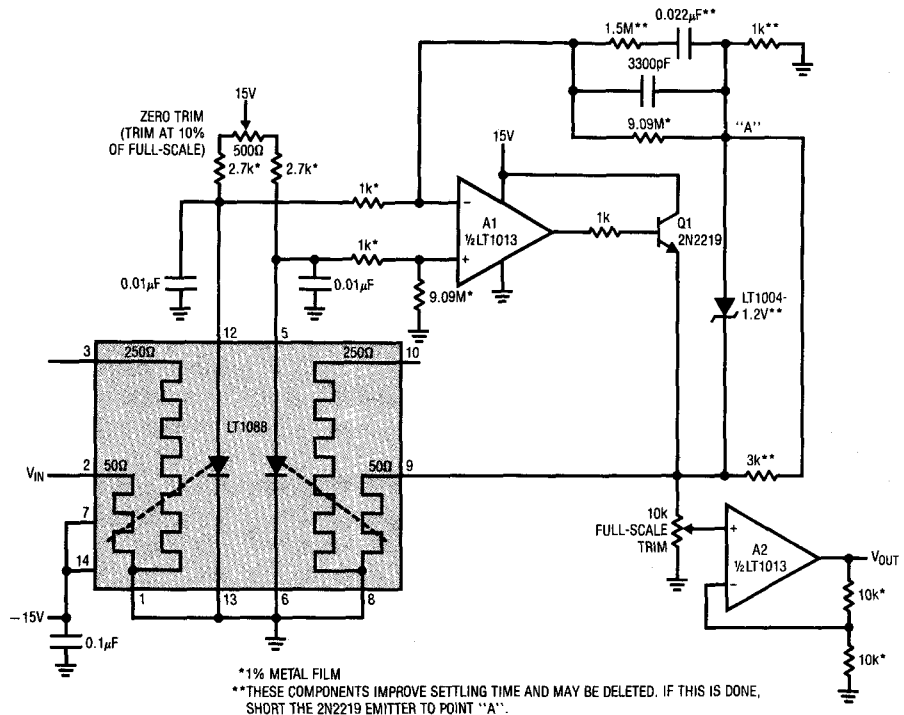


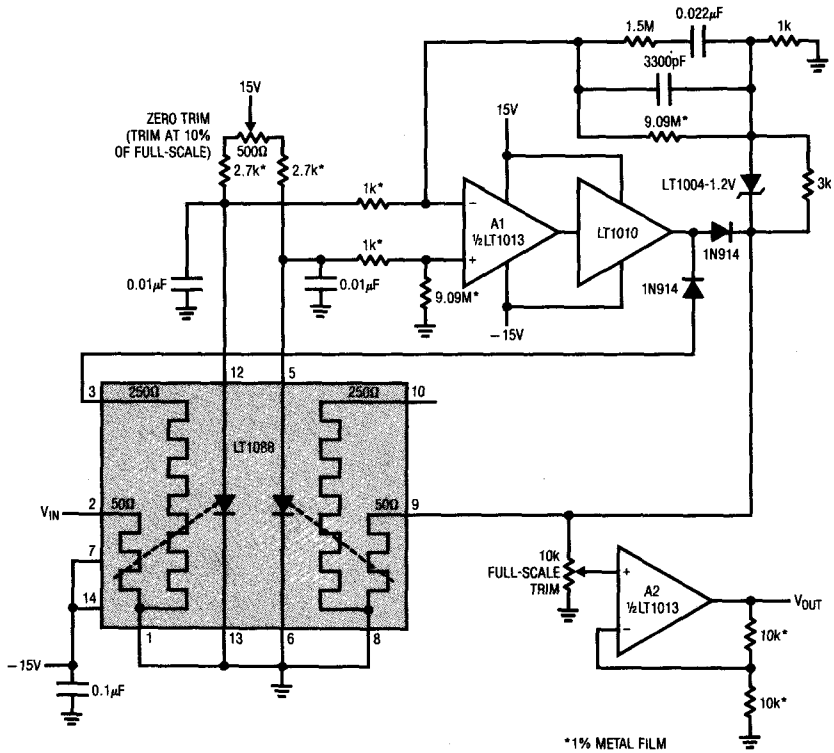
Figure 4. Basic RMS-DC Converter

Figure 4's Typical Specifications

Accuracy:	Crest Factor:
50Ω Input	50Ω Input 50:1
DC to 50MHz 1% FS	250Ω Input 40:1
DC to 100MHz 2% FS	3dB Bandwidth 300MHz
250Ω Input	Full-Scale Settling Time (1%) 500ms (LT1088CD)
DC to 20MHz 1% FS 710ms (LT1088CN)
Temperature Effect on Accuracy 100ppm/°C	Input Voltage Range (25°C)
Dynamic Range 20:1 (LT1088CD)/14:1 (LT1088CN)	50Ω Input 4.25V
	250Ω Input 9.5V

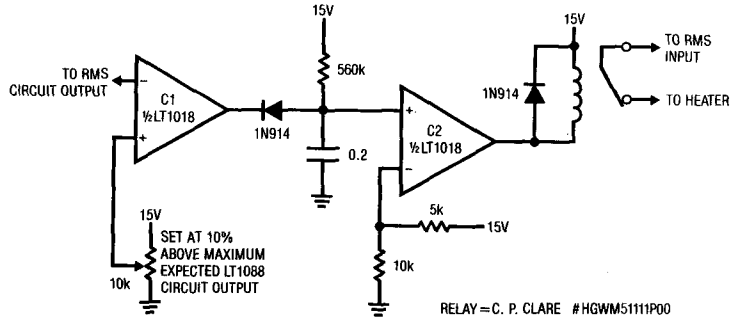
APPLICATIONS

Fast Settling RMS-DC Converter

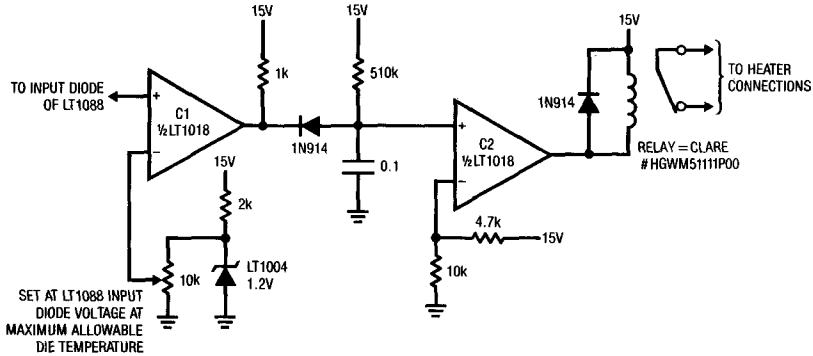


APPLICATIONS

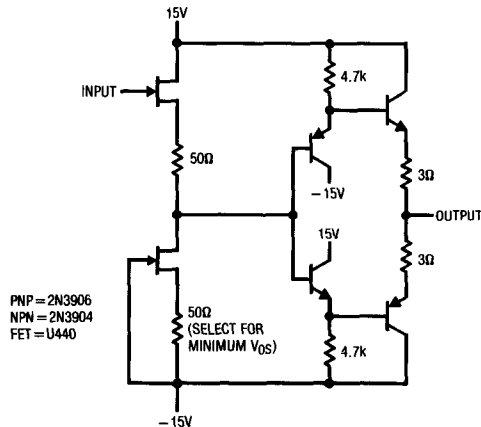
Servo-Sensed Heater Protection Circuit ($\approx 50\text{ms}$ Response)



Diode Sensed Heater Protection Circuit ($\approx 15\text{ms}$ Response)

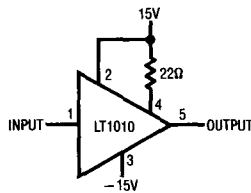


Discrete Input Buffer for the LT1088

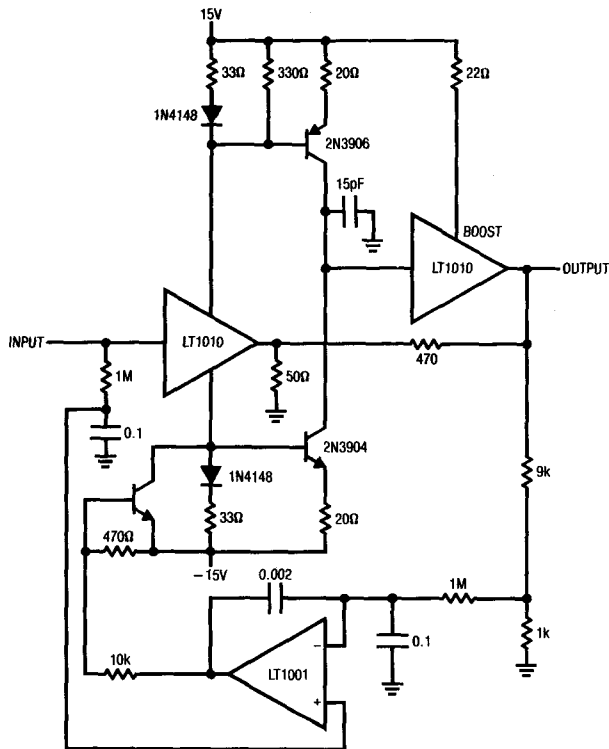


APPLICATIONS

LT1010 Buffer†



LT1010 Buffer with Gain of 10†

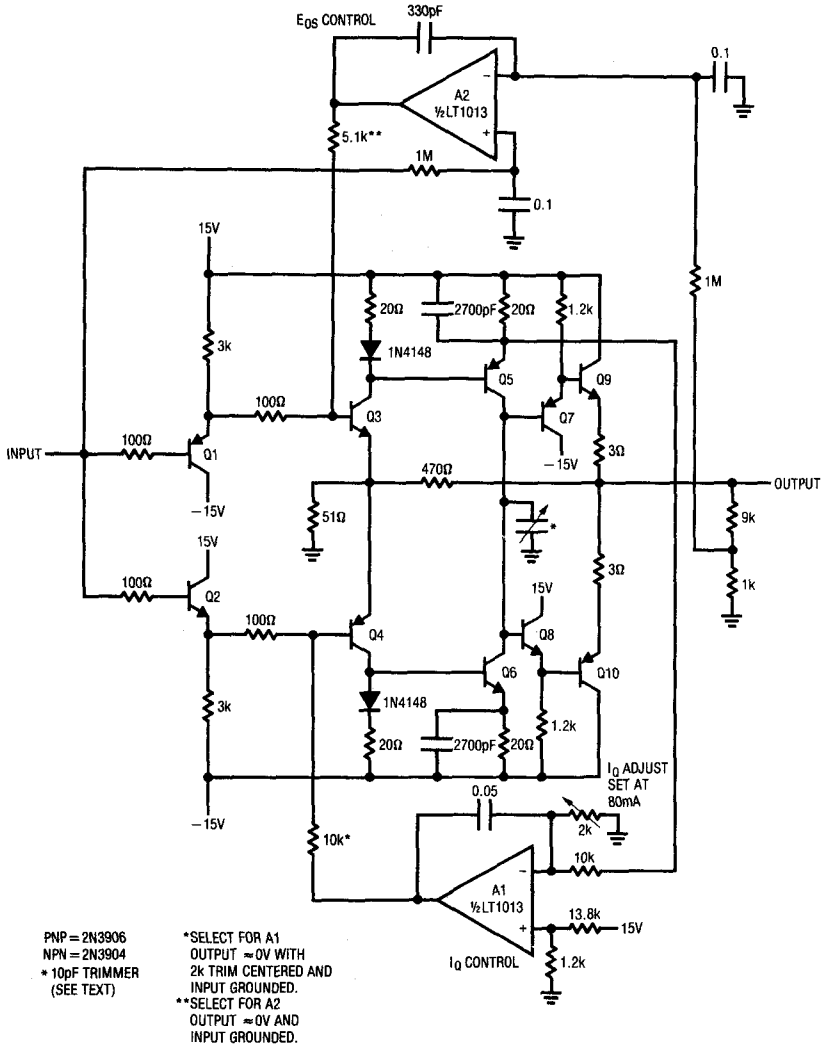


11

† See Summary of Buffer Characteristics table for buffer speed.

APPLICATIONS

Wideband Discrete Buffer with Gain = 10†



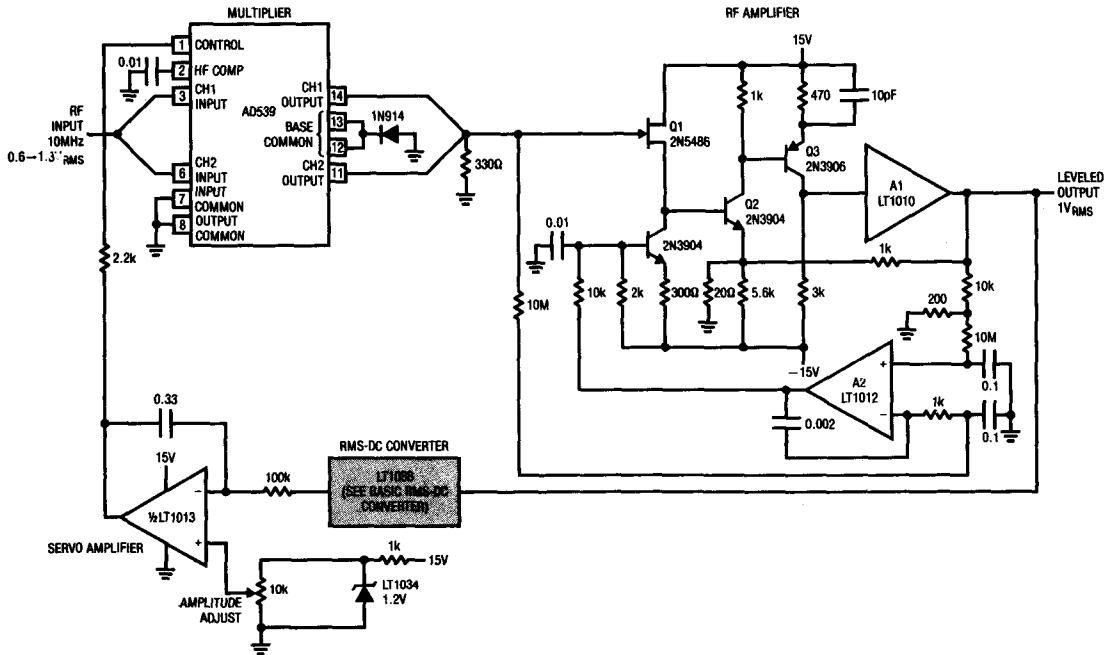
† See Summary of Buffer Characteristics table for buffer speed.

APPLICATIONS

Summary of Buffer Characteristics

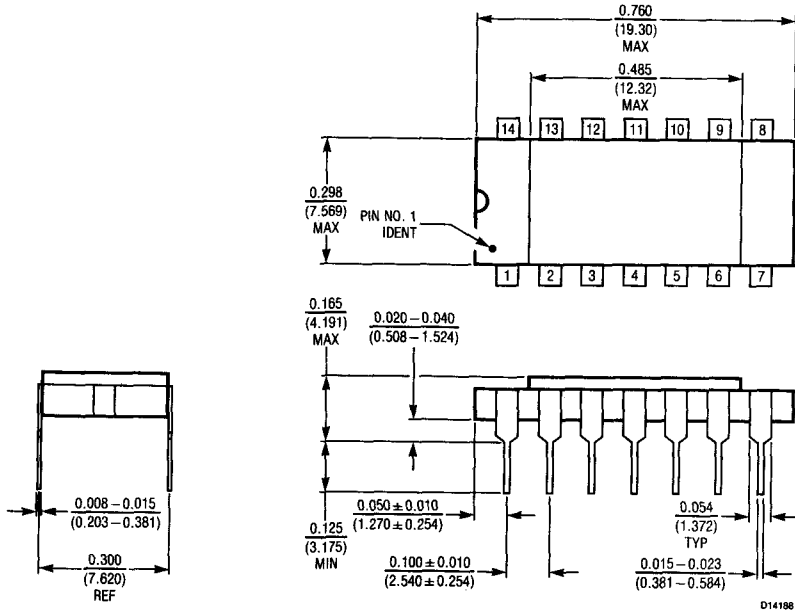
Type of Buffer	Slew Rate	1% Error Bandwidth	
		250 Ω Load ($\pm 10V_{out}$)	50 Ω Load ($\pm 5V_{out}$)
Discrete—A = 10	3000V/ μ s	25MHz	32MHz
LT1010 Based—A = 10	100V/ μ s	0.75MHz	2MHz
Discrete—A = 1	2000V/ μ s	15MHz	25MHz
LT1010 Based—A = 1	100V/ μ s	0.75MHz	2MHz

RF Leveling Loop

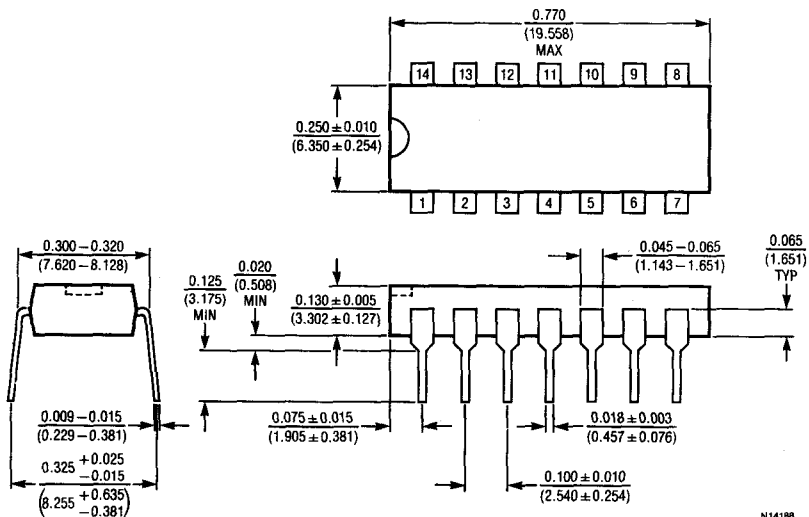


PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

D Package
14-Lead Sidebrazed Ceramic DIP



N Package
14-Lead Plastic DIP



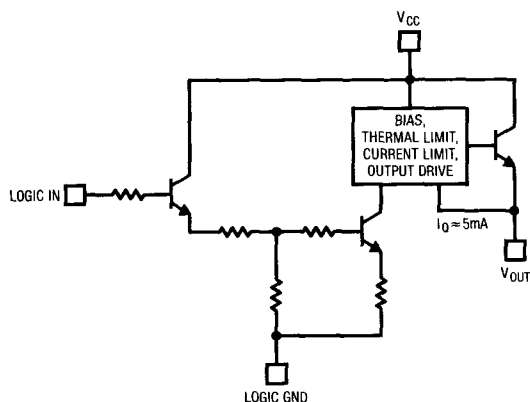
FEATURES

- 7.5A Switch Capability
- Low Series Drop ($< 1.5V @ 7.5A$)
- Logic Input (Positive or Negative Logic)
- Current Limited
- Thermal Overload
- 5mA Quiescent Current
- 10 μ s Risetime

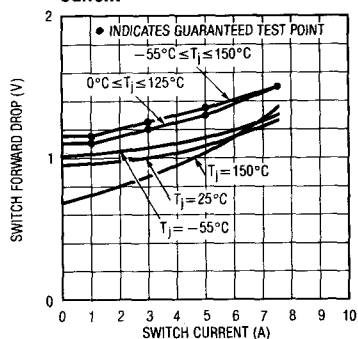
DESCRIPTION

The LT1089 is a logic driven, high current, high side switch utilizing bipolar technology. The device is capable of driving loads up to 7.5A with a low series drop of only 1.5V, and the series drop is specified over the full range of switch currents. The device has internal current limiting and thermal overload protection. The input logic is designed so that the output can drive loads referenced either above or below the device ground pin. Either positive or negative logic can be used to drive the input. The device is available in both TO-3 metal can and TO-220 plastic packages.

BLOCK DIAGRAM

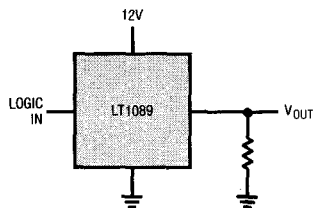


LT1089 Switch Voltage vs Output Current

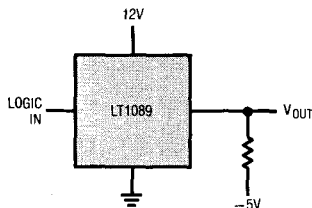


TYPICAL APPLICATIONS

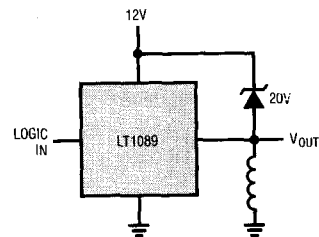
Driving Ground Referred Loads



Driving Negative Referred Loads



Driving Inductive Loads



ABSOLUTE MAXIMUM RATINGS*

Switch Voltage ($V_{CC} - V_{OUT}$)	30V
Logic Input Voltage ($V_{IN} - GND$)	15V
Logic Input Voltage Range (V_{IN})	$(V_{CC} - 30V) < V_{IN} < V_{CC}$
Ground Pin Voltage Range (GND)	$(V_{CC} - 30V) < GND < V_{CC}$
Operating Junction Temperature Range	
" M " Grades	-55°C to 150°C
" C " Grades	0°C to 125°C
Storage Temperature Range	-65°C to 150°C
Lead Temperature (Soldering, 10 sec.)	300°C

MAXIMUM OPERATING SPECIFICATIONS*

Switch Voltage ($V_{CC} - V_{OUT}$)	20V
Logic Input Voltage ($V_{IN} - GND$)	5V
Logic Input Voltage Range (V_{IN})	$(V_{CC} - 20V) < V_{IN} < V_{CC}$
Ground Pin Voltage Range (GND)	$(V_{CC} - 20V) < GND < V_{CC}$

*Note: Absolute maximum ratings are those voltages that the device is rated to withstand on a transient basis without damage. Maximum operating specifications are the maximum recommended operating voltages. The device is fully specified up to the maximum operating specifications. For voltages greater than the maximum operating specifications some device parameters may exceed the data sheet limits.

PACKAGE/ORDER INFORMATION

<p>BOTTOM VIEW V_{IN} NC CASE IS V_{OUT} 1 2 4 3 LOGIC IN GND K PACKAGE 4-LEAD TO-3 METAL CAN</p>	ORDER PART NUMBER	<p>FRONT VIEW 5 LOGIC IN 4 V_{IN} 3 V_{OUT} 2 GND 1 NC T PACKAGE 5-LEAD TO-220</p>	ORDER PART NUMBER
	LT1089MK LT1089CK		LT1089CT

ELECTRICAL CHARACTERISTICS

PARAMETER	CONDITIONS (NOTE 1)	MIN	TYP	MAX	UNITS
Output Saturation Voltage	$I_{SWITCH} = 7.5A, (V_{IN} - GND) = 5V$ $4V < (V_{CC} - GND) < 20V$	•	1.3	1.5	V
Input Voltage ($V_{IN} - GND$)	Switch ON, (Note 2) $4V < (V_{CC} - GND) < 20V$	•	2.4	1.5	V
	Switch OFF, (Note 3) $4V < (V_{CC} - GND) < 20V$	•	1.5	0.8	V
		•			
Input Current	Switch ON, ($V_{IN} - GND$) = 5V	•	-20	-100	μA
	Switch OFF, ($V_{IN} - GND$) = 0V	•	0	± 5	μA
		•			
Ground Pin Current	Switch ON, ($V_{IN} - GND$) = 5V	•	3.5	5.0	mA
	Switch OFF, ($V_{IN} - GND$) = 0V	•	0	± 20	μA
		•			
Output Current	Switch OFF, ($V_{IN} - GND$) = 0V	•	5	10	mA
Current Limit	Switch ON, ($V_{IN} - GND$) = 5V $(V_{CC} - V_{OUT}) = 5V$	•	8.0	9.5	A
	$(V_{CC} - V_{OUT}) = 20V$	•	0.5	1.0	1.5
Turn-On Delay		•	1	10	μS
Turn-Off Delay		•	5	20	μS
Output Risetime	$R_{LOAD} = 4\Omega$	•	10	25	μS
		•			

ELECTRICAL CHARACTERISTICS

PARAMETER	CONDITIONS (NOTE 1)	MIN	TYP	MAX	UNITS
Output Faltime	$R_{LOAD} = 4\Omega$ (Note 4)	•	10	25	μS μS
Thermal Resistance	K Package T Package			1.6 2.0	$^{\circ}C/W$ $^{\circ}C/W$

The • denotes the specifications which apply over the full operating temperature range.

Note 1: Unless otherwise specified, $(V_{CC} - GND) = 20V$ and the output load is referred to the ground pin (GND) of the device. Positive current values are defined to flow out of the device.

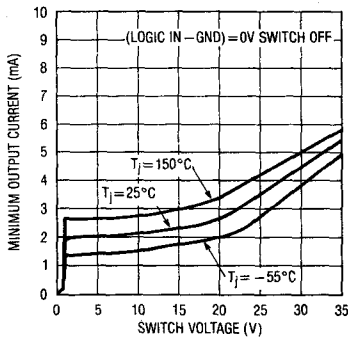
Note 2: For input voltages greater than 2.4V the device is guaranteed to be turned on. 1.5V is the typical threshold at 25°C.

Note 3: For input voltages less than 0.8V, the device is guaranteed to be in an off state. 1.5V is the typical switch threshold at 25°C.

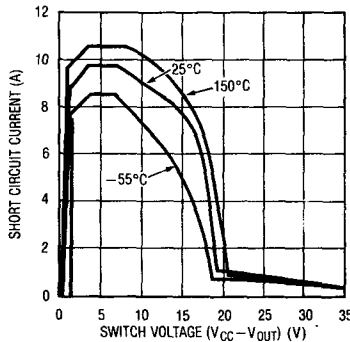
Note 4: For reactive loads such as large capacitors, the output falltime will be determined by the load.

TYPICAL PERFORMANCE CHARACTERISTICS

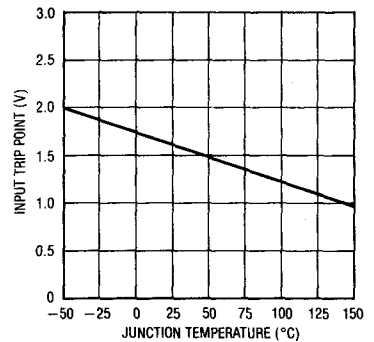
Minimum Output Current



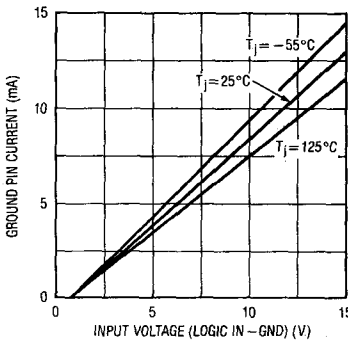
Short Circuit Current



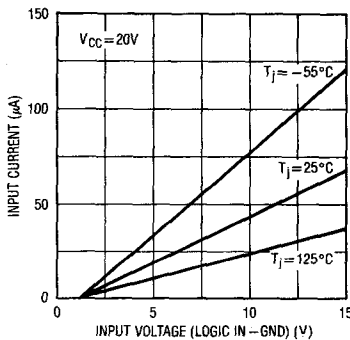
Input Trip Voltage (Logic In - GND)



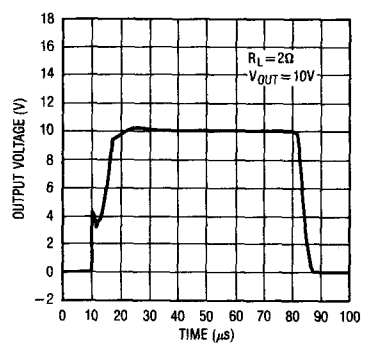
Ground Pin Current



Logic Input Current



Rise and Fall Times



APPLICATION HINTS

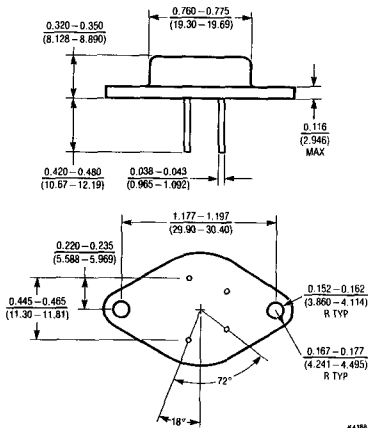
The logic and ground pins function as a differential logic input with a common-mode range of V_{CC} to $V_{CC} - 20V$ and a differential threshold voltage ($V_{LOGIC} - GND$) of 1.5V. Note that if either Logic In or GND are left open the switch remains inactive.

The LT1089 must be protected against overvoltage at turn-off when driving inductive loads. The inductive flyback voltage can easily exceed the maximum operating switch voltage ($V_{CC} - V_{OUT}$) of 20V, potentially damaging the switch. The solution is to clamp the switch voltage to 20V or less with a zener diode. Remember that the switch can handle 7.5A and the zener may be required to handle the same amount of current.

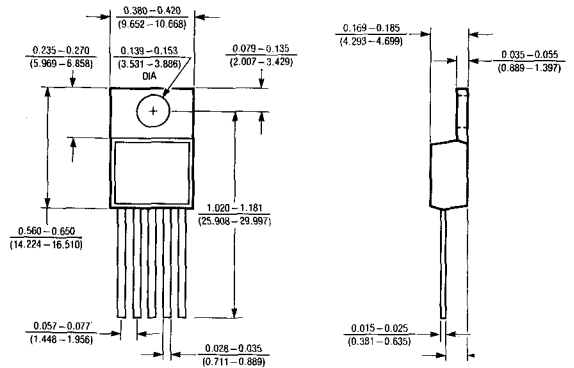
Care must be exercised when operating near the maximum switch voltage. A high current or capacitive load may trip the current limit circuit at turn-on, thereby adversely affecting the risetime of V_{OUT} . The risetime is then governed by the current limit divided by the load capacitance, while the falltime is a function of the complex load. In addition, at switch voltages greater than 18V the switch current must be less than 0.5A or the device output will not pull up. Check the short circuit current characteristics for more detailed information.

PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

K Package
4-Lead TO-3 Metal Can



T Package
5-Lead TO-220



SECTION 12— MILITARY PRODUCTS

**REFER TO TABLE OF CONTENTS
FOR REVISED DATA LOCATION**

SECTION 12—MILITARY PRODUCTS

INDEX	12-2
MIL/JAN Products	12-3
Standard Military Drawings	12-4
Hi-Rel	12-4
MIL-STD-883 Product	12-4
MIL-M-38510 Class B Flow	12-6
MIL-M-38510 Class S Flow	12-7
Military Sampling Plan	12-8
MIL-STD-883 Test Methods	12-9
Military Parts List	12-13

NOTE

Military product datasheets are available from your local LTC Sales Representative, or by calling LTC Communications at (800) 637-5545.

LINEAR TECHNOLOGY MILJAN PRODUCTS

Linear Technology Corporation offers a comprehensive selection of precision voltage references, operational amplifiers, voltage regulators, comparators, and CMOS circuits designed specifically to serve the rigorous requirements of the military marketplace.

The company's specification system and quality procedures and policies were set up from the beginning to meet the exacting demands of MIL-Q-9858 (Quality Program Requirements), MIL-I-45208 (Inspection System Requirements), MIL-M-38510 (General Specification For Microcircuits) and MIL-STD-883 (Test Methods and Procedures For Microelectronics).

Compliance to these specifications is a statutory requirement for all employees at Linear Technology. The programs now in place that serve the varied requirements for ground, sea, air, and space applications include:

- JAN S
- JAN B
- Standard Military Drawings (SMD)
- Hi-Rel (SCD)
- 883

Linear Technology JAN

At the end of 1969, the Solid State Applications Branch of the Rome Air Development Center (RADC) issued the first copy of MIL-M-38510. This general specification for microcircuits established the procedures that a manufacturer must follow to have his products listed on the Qualified Parts List (QPL).

One major problem faced by defense contractors using semiconductor devices was the inability to interchange devices caused by a proliferation of non-standard electrical specifications. The 38510 (JAN) program addressed this problem by publishing detailed electrical specifications (slash sheets) for each component to be listed on the QPL.

JAN devices are completely processed in the United States or its territories and all wafer fabrication, wafer sort, assembly, testing, and conformance testing are performed onshore.

In early 1985, Linear Technology Corporation joined the ranks of the eighteen existing QPL suppliers. Of these eight-

een, only a handful of suppliers participate in the linear military JAN market. Linear Technology believes its analog design experience and manufacturing strength can contribute significantly to this market.

In August 1984, Linear Technology Corporation was visited by a team of DESC (Defense Electronics and Supply Center) personnel. This team spent almost four days on their audit and at the end of the visit they awarded the company "Class B Line Certification." *This was a first for any company to receive this distinction on a first audit!* In November 1987, Linear Technology Corporation was audited by a team from DESC, Naval Weapons Support Center and Aerospace Corporation and was awarded "Class S Line Certification."

Linear Technology's first QPL listing was achieved in February, 1985, one year after the company made JAN Class B a corporate goal. Other companies have typically taken 2 to 3 years to achieve this status. The line certification and QPL approvals were awarded to MIL-38510 and MIL-STD-883 Rev. C specifications.

Linear Technology's policy of providing JAN Class B linear components supports the United States Government's position of standardization to decrease the number of active part types maintained by DESC. This number is currently in excess of 70,000 for all types of components (contrasted to approximately 5,000 industry standard components). Standardization will clearly decrease costs and assist in the maintenance of military weapon systems and equipment now in the field. Linear Technology Corporation has over 40 products listed on the Class B Qualified Parts List (Part 1), products qualified on the Class S Qualified Parts List (Parts 1 and 2), and we have an active and aggressive program to further expand our offering of JAN products.

**EXAMPLES OF LINEAR TECHNOLOGY
 MILITARY PROGRAM PARTICIPATION**

AMRAAM	SPARROW	PERSHING II
PHOENIX	HARPOON	MINUTEMAN
PHALANX	HARM	B-1B
F-15	COPPERHEAD	B-52
F-16	GPS	TOW
F-18	HTTB	MAVERICK
DRAGON	SEAHAWK	ACTS
STD. MISSILE	FLEET SATCOM	M-1 TANK

MILITARY PRODUCTS

Linear Technology Standard Military Drawings

DESC drawings were initiated in 1976 to standardize the electrical requirements for full temperature-tested military components. These DESC drawings (or minispecs) were initially issued for low power Schottky devices (54LS) used by defense subcontractors on the Air Force's F16. The program accomplished standardization of testing, without the delays associated with the qualification process for JAN components.

The DESC drawing was viewed as a preliminary specification prior to JAN approval, and it ranks second in the order of purchasing hierarchy to JAN. This order is defined in Requirement 64 of MIL-STD-454. If a JAN part is available, it is still preferred, however, there are many types of devices where the volume is such that the cost of a full JAN qualification may not be justified, but where a need exists for electrical standardization.

CMOS and analog circuits were added to the DESC Drawing Program in 1977, 1978 and 1979, but widespread acceptance of these parts was not achieved. Today with more emphasis being placed on standardization, the interest level in DESC drawings has accelerated. This category of product can be built offshore with 883-level processing and the electrical parameters are tested specifically to the DESC drawing.

To provide parts to a DESC drawing, a manufacturer has to have at least one part on the 38510 Qualified Parts List. He must also provide DESC with a certificate of compliance agreeing to the tests and conditions listed on the drawing.

In 1986 a new program named Standard Military Drawings (SMDs) was launched by DESC. This replaced the previous DESC Drawing Program. This new program is aimed directly at standardizing electrical requirements with the objective to decrease the time required to issue a military drawing. To achieve this, we have set up a computer link-up with the DESC Standardized Mil Drawing Group. A flowchart showing the preparation of Mil drawings is shown in Figure 1. Linear Technology is actively supporting this new Mil Drawing program and we are working closely with DESC and OEMs to participate in this government plan toward a greater level of standardization in military specifications.

Linear Technology has over 80 devices listed on DESC and Mil drawings, and we are actively supporting these stand-

ardization programs by having parts available off the shelf from Linear Technology Corporation and from distribution outlets.

Linear Technology Hi-Rel

Linear Technology Corporation recognizes the need for source controlled drawings (SCD's) and the company's DESC-certified line is well equipped to handle these requirements for space and hi-rel applications. The company has a comprehensive review procedure and emphasis is placed on compliance to test methods and procedures. Over 4,000 specifications have been reviewed to date with fast feedback to our customers.

Linear Technology has serviced source controlled drawing orders including "S" level specifications with a variety of source inspection and conformance test requirements. Each source controlled drawing requires dedicated flows, software and hardware, and as a result, certain minimum requirements have to be fulfilled. Linear Technology's Product Marketing group can provide you with more details on a case-by-case basis.

Linear Technology MIL-STD-883 Product

The semiconductor industry 883 designation on military semiconductor components established a defacto standard in response to a significant demand from the military defense contractors. The Government recognized the existence of 883 components in the recent revisions of MIL-STD-883C and MIL-M-38510, and the requirements for compliant 883 components are now defined very specifically in these documents.

MIL-STD-883 is a test procedures and methods document and the last major revision (Rev. C) became effective on June 1, 1984. This document is revised periodically and defines the conditions for two categories of product, Class B and Class S. Class B is intended for applications where maintenance is difficult or expensive and where reliability is vital. Class S is intended for space and critical applications where replacement is extremely difficult or impossible and where reliability is imperative. The Class B PDA (Percent Defective Allowable) was tightened from 10% to 5% following

burn-in and the Group A electrical sampling plans (LTPD levels) also were tightened. In addition, a critical paragraph was added to MIL-STD-883 to alleviate any misinterpretation; a factor that had previously created vastly different 883 programs throughout the semiconductor industry.

On December 31, 1984, another key clause was added to MIL-STD-883 Rev. C, "paragraph 1.2.1." This states that if a manufacturer advertises, certifies, or marks parts as compliant with MIL-STD-883 those parts must meet all of the provisions of MIL-STD-883, a practice consistent with "Truth in Advertising".

According to the Defense Electronics Supply Center (a branch of the Defense Department's Logistics Agency), the intent of paragraph 1.2.1 was to link MIL-STD-883 with the controls and details contained in MIL-M-38510.

Linear Technology Corporation can state unequivocally that all of its 883 products are in full compliance with the new

MIL-STD-883 Rev. C requirements. We have over 275 versions of our 883 products listed in our current catalog, including operational amplifiers, voltage regulators, voltage references, comparators, and our advanced line of proprietary CMOS circuits.

All products manufactured by Linear Technology are designed to meet the full requirements of the military, from -55°C to 125°C.

Military Market Commitment

Linear Technology Corporation is a focused, dedicated company servicing the needs of the linear military marketplace. We are shipping to the top U.S. defense electronics contractors who have qualified and approved our products. Linear Technology Corporation is committed to being the best and most proficient high quality supplier of analog military components.

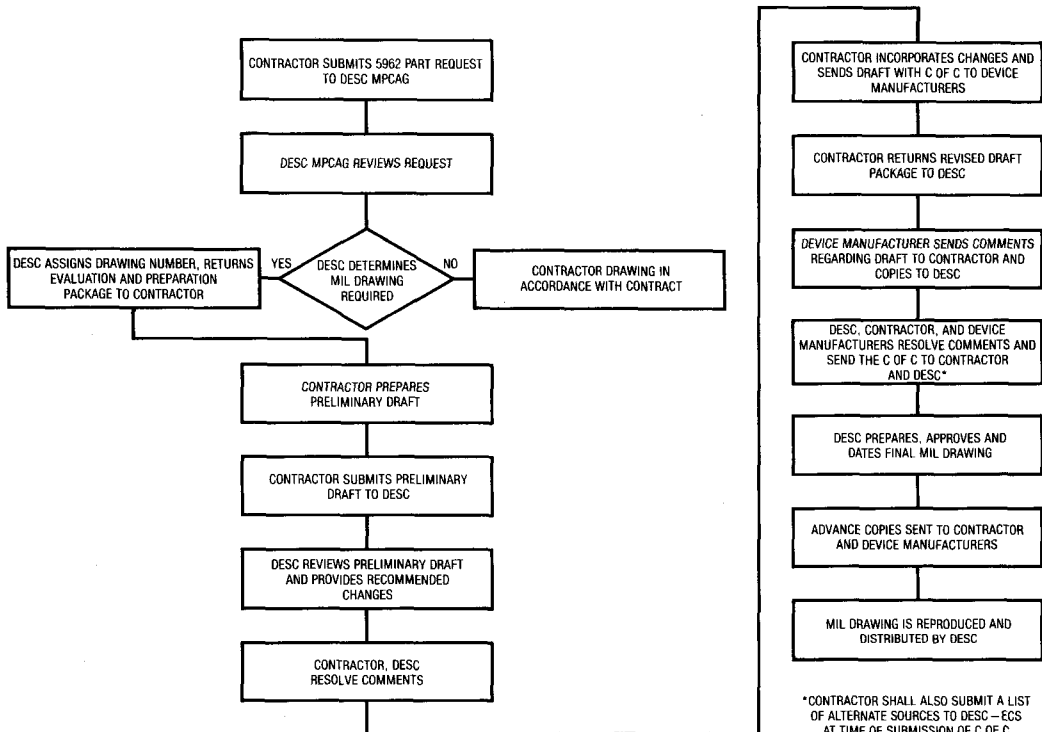
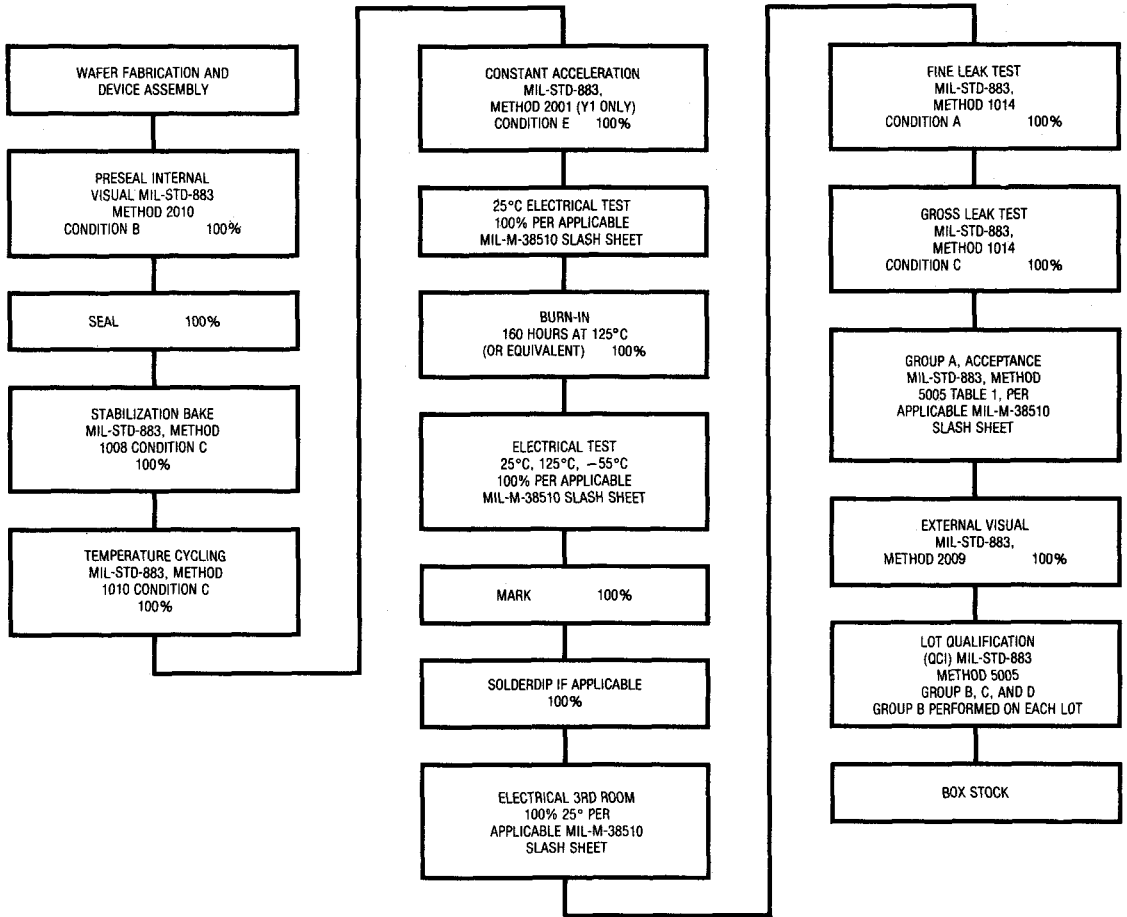


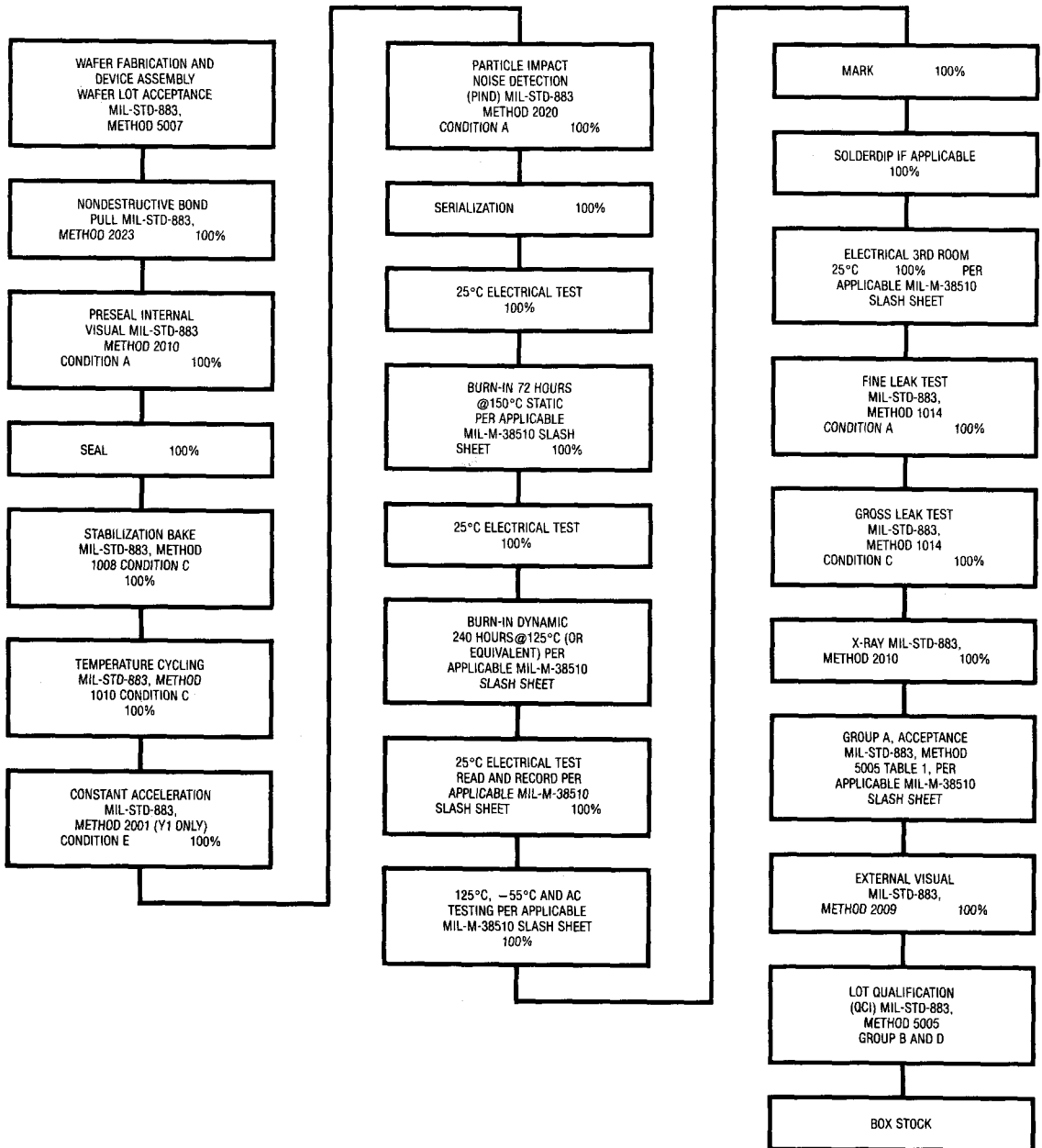
Figure 1. Mil Drawing Preparation Flowchart.

MILITARY PRODUCTS

MIL-M-38510 CLASS B FLOW



MIL-M-38510 CLASS S FLOW



12

MILITARY PRODUCTS

LINEAR TECHNOLOGY 883 GROUP A SAMPLING PLAN

TEST	CONDITION	883C	
		SAMPLE SIZE	LTPD
DC Parametric	$T_A = 25^\circ\text{C}$	116	2.0%
DC Parametric	$T_A = -55^\circ\text{C}$ $+ 125^\circ\text{C}$	116	2.0%
AC Parametric	$T_A = 25^\circ\text{C}$	116	2.0%

883 CERTIFICATE OF CONFORMANCE—LEVEL B

LTC Part Number _____

Lot Traceability No. _____

Purchase Order No. _____

Customer Name _____ P/N _____ Qty _____

Date Code _____ Shipper # _____ Traveller Lot # _____

Group A = _____ Group B = _____ Group C = _____ Group D = _____

Group A Re-Inspection Data, If Applicable _____

QUALITY ASSURANCE INSPECTOR	
DATE	SIGNATURE

LINEAR TECHNOLOGY CORPORATION HEREBY DECLARES THAT THE COMPONENTS SPECIFIED ON THE ABOVE PURCHASE ORDER COMPLY WITH YOUR SPECIFICATIONS AND REQUIREMENTS OF MIL-STD 883 REV C. ALL SUPPORTING DOCUMENTATION AND RECORDS ARE RETAINED ON FILE BY LTC AND ARE AVAILABLE FOR INSPECTION. THE MAJOR ELEMENTS OF THE 883C PROGRAM ARE SHOWN BELOW.

Operation	Screening Procedure MIL-STD-883C Method 5004
Internal Visual	Method 2010, Condition B
Stabilization Bake	Method 1008, Condition C
Temperature Cycling	Method 1010, Condition C, 10 cycles - 65°C to 150°C
Constant Acceleration	Method 2001, Condition E, 30K G's Y1 axis (TO-3 PKG at 20K G's)
Fine Leak	Method 1014, Condition A
Gross Leak	Method 1014, Condition C
Burn-in	Method 1015, 160 hrs at 125°C (or equivalent)
Final Electrical	+ 25°C DC (per LTC Data Sheet) PDA = 5%
	+ 125°C or 150°C DC
	- 55°C DC
	+ 25°C AC
QA Acceptance	Method 5005 Group A (sample/lot)
Quality Conformance	Group B (sample/lot)
	Group C (sample every 3 months/Generic Group)
	Group D (sample every 6 months/Package Type)
External Visual	Method 2009

EXAMPLE

NOTE: Each operation is performed on a 100% basis unless otherwise stated.

FORM. NO. 00-03-6072

LINEAR TECHNOLOGY CORPORATION
1630 McCarthy Blvd.
Milpitas, CA 95035-7487

12

MILITARY PRODUCTS

LINEAR TECHNOLOGY CORPORATION
 1630 McCarthy Blvd.
 Milpitas, CA 95035-7487

GROUP A DATA Mil-Std 883, METHOD 5005

LTC P/N: _____ LOT #: _____
 GENERIC TYPE: _____ PKG: _____ DATE CODE: _____
 ASSEMBLY LOC: _____

	LTPD	ACC #	S/S	# FAILED	DATE TEST	OPER NUMBER
SUBGROUP 1 Static test at 25°C	2%					
SUBGROUP 2 Static tests at maximum rated operating temperature	2%					
SUBGROUP 3 Static tests at minimum rated operating temperature	2%					
SUBGROUP 4 Dynamic tests at 25°C	2%					
SUBGROUP 5 Dynamic tests at maximum rated operating temperature	2%					
SUBGROUP 6 Dynamic tests at minimum rated operating temperature	2%					
SUBGROUP 7 Functional tests at 25°C	SAME AS SUBGROUP #1					
SUBGROUP 8 Functional tests at maximum and minimum operating temperature	SAME AS SUBGROUPS 2 & 3					
SUBGROUP 9 Switching tests at 25°C	2%					
SUBGROUP 10 Switching tests at maximum rated operating temperature	2%					
SUBGROUP 11 Switching tests at minimum rated operating temperature	2%					

EXAMPLE

QA APPROVAL: _____ DATE: _____

FORM No. 00-03-6037

MILITARY PRODUCTS

LINEAR TECHNOLOGY CORPORATION
1630 McCarthy Blvd.
Milpitas, CA 95035-7487

GROUP B DATA Mil-Std 883, METHOD 5005

LTC P/N: _____ LOT #: _____
 GENERIC TYPE: _____ PKG: _____ DATE CODE: _____
 ASSEMBLY LOC: _____

TEST	METHOD	CONDITION	LTPD	ACC #	S/S	# FAILED	DATE TESTED	OPER #
SUBGROUP 1 Physical Dimensions	2016			0	2			
SUBGROUP 2 Resistance to Solvents	2015			0	4			
SUBGROUP 3 Solderability	2003	Soldering Temp. of 245 ± 5°C	10	0				
SUBGROUP 4 Internal Visual/Mechanical	2014	design and construction requirements		0	1			
SUBGROUP 5 Bond Strength	2011	C or D	15	0				
SUBGROUP 7 Fine Leak Gross Leak	1014		5	0				

QA APPROVAL: _____ DATE: _____

FORM No. 00-03-6006

LINEAR TECHNOLOGY CORPORATION
1630 McCarthy Blvd.
Milpitas, CA 95035-7487

GROUP C DATA Mil-Std 883, METHOD 5005

LTC P/N: _____ LOT # _____
 GENERIC TYPE: _____ PKG: _____ DATE CODE: _____
 CT. GROUP: _____

TEST	METHOD	CONDITION	LTPD	ACC #	S/S	# FAILED	DATE TESTED	OPER #
SUBGROUP 1 Steady State Life Test	1005	T _A = 125°C (1000 Hours or Equiv.)	5	0	45			
Electrical Endpoints								
SUBGROUP 2 Temperature Cycling Constant Acceleration Fine Leak Gross Leak Visual Examination	1010 2001 1014 1014 1010/ 1011	C E Y1 only	15	0	15			
Electrical Endpoints	Test #							

QA APPROVAL: _____ DATE: _____

FORM No. 00-03-6007

MILITARY PRODUCTS

LINEAR TECHNOLOGY CORPORATION
 1630 McCarthy Blvd.
 Milpitas, CA 95035-7487

GROUP D DATA Mil-Std 883, METHOD 5005

LTC P/N: _____ LOT #: _____
 GENERIC TYPE: _____ PKG: _____ DATE CODE: _____
 ASSEMBLY LOC: _____

TEST	METHOD	CONDITION	LTPD	ACC #	S/S	# FAILED	DATE TESTED	OPER #
SUBGROUP 1 Physical Dimensions	2016		15	0	15			
SUBGROUP 2 Lead Integrity	2004	B2 (lead fatigue)	15	0	15			
Fine Leak	1014							
Gross Leak	1014							
SUBGROUP 3 Thermal Shock Temperature Cycle Moisture Resistance Fine Leak Gross Leak Visual Examination Electrical Endpoints	1011 1010 1004 1014 1014 1004/ 1010	B 15 cycles C 100 cycles Test #	15	0	15			
SUBGROUP 4 Mechanical Shock Vibration Variables- Frequency Constant Acceleration Fine Leak Gross Leak Visual Examination Electrical Endpoints	2002 2007 2001 1014 1014 1010/ 1011	B A E Y1 only Test #	15	0	15			
SUBGROUP 5 Salt Atmosphere Fine Leak Gross Leak Visual Examination	1009 1014 1014 1009	A Visual Criteria	15	0	15			
SUBGROUP 6 Internal Water-Vapor	1018	5000ppm		0	3			
SUBGROUP 7 Adhesion of Lead Finish	2025		15	0	15			
SUBGROUP 8 Lid Torque	2024	Glass Frit Seal only		0	5			

EXAMPLE

QA APPROVAL: _____ DATE: _____

FORM No. 00-03-6008

MILITARY PARTS LIST

JAN S QPLT	JM38510/10103SHA (LM101AW) JM38510/10104SCA (LM108AJ)** JM38510/10104SHA (LM108AW) JM38510/10104SPA (LM108AJ8) JM38510/10107SPA (LM118J8) JM38510/11404SGA (LF155AH) JM38510/11404SGC (LF155AH) JM38510/11405SGA (LF156AH)	JM38510/11405SGC (LF156AH) JM38510/11803SXA (LM137H) JM38510/11803SXC (LM137H) JM38510/11804SYA (LM137K) JM38510/12501SGA (LF198H) JM38510/13501SGA (OP07AH) JM38510/13501SGC (OP07AH) JM38510/13501SPA (OP07AJ8)	JM38510/13502SGA (OP07H) JM38510/13502SGC (OP07H) JM38510/13502SPA (OP07J8) JM38510/13503SGA (OP27AH) JM38510/13503SGC (OP27AH) JM38510/13503SPA (OP27AJ8)	
JAN B QPLT	JM38510/10103BGA (LM101AH) JM38510/10104BCA (LM108AJ) JM38510/10104BGA (LM108AH) JM38510/10104BGC (LM108AH) JM38510/10104BGA (LM108AJ8) JM38510/10106BEA (LH2108AD) JM38510/10107BGA (LM118H) JM38510/10107BGC (LM118H) JM38510/10107BPA (LM118J8) JM38510/11401BGA (LF155H) JM38510/11401BGC (LF155H) JM38510/11402BGA (LF156H) JM38510/11402BGC (LF156H)	JM38510/11402BPA (LF156J8) JM38510/11404BGA (LF155AH) JM38510/11404BGC (LF155AH) JM38510/11405BGA (LF156AH) JM38510/11405BGC (LF156AH) JM38510/11405BPA (LF156AJ8) JM38510/11703BXA (LM117H) JM38510/11703BXC (LM117H) JM38510/11704BYA (LM117K) JM38510/11706BYA (LM138K) JM38510/11803BXA (LM137H) JM38510/11803BXC (LM137H) JM38510/11804BYA (LM137K)	JM38510/12501BGA (LF198H) JM38510/12501BGC (LF198H) JM38510/13501BGA (OP07AH) JM38510/13501BGC (OP07AH) JM38510/13501BPA (OP07AJ8) JM38510/13502BGA (OP07H) JM38510/13502BGC (OP07H) JM38510/13502BPA (OP07J8) JM38510/13503BGA (OP27AH) JM38510/13503BGC (OP27AH) JM38510/13503BPA (OP27AJ8)	
DESC Drawings**†	7703401XA (LM117H) 7703401XC (LM117H) 7703401YA (LM117K) 7703402XA (LM117HVVH) 7703402XC (LM117HVVH) 7703402YA (LM117HVK) 7703403XA (LM137H) 7703403XC (LM137H) 7703403YA (LM137K) 7703404XA (LM137HVVH) 7703404XC (LM137HVVH) 7703404YA (LM137HVK)	7703405XX (LT117AH) 7703405YX (LT117AK) 7703406XX (LT137AH) 7703406YX (LT137AK) 7703407XX (LT117AHVH) 7703407YX (LT117AHVK) 7703408XX (LT137AHVH) 7703408YX (LT137AHVK) 7802801EA (SG1524J) 8203601GX (OP07AH) 8203601PX (OP07AJ8) 8203602GX (OP07H)	8203602PX (OP07J8) 8418001XA (LM136AH-2.5) 8418001XC (LM136AH-2.5) 8551401GX (REF02AH) 8551401PX (REF02AJ8) 8551501VX (LT1526J) 8601401CA (LM119J) 8601401IA (LM119H) 8601401HA (LM119W) 8601402CA (LT119AJ) 8601402IA (LT119AH)	
Standard Military Drawings (SMD)†	5962-8680601EA (LT1846J) 5962-8684501IX (LT1016MH) 5962-8684501PX (LT1016MJ8) 5962-8686101XX (LT580SH) 5962-8686102XX (LT580TH) 5962-8688201XA (LH0070-0H) 5962-8688201XC (LH0070-0H) 5962-8688202XA (LH0070-1H) 5962-8688202XC (LH0070-1H) 5962-8688203XA (LH0070-2H) 5962-8688203XC (LH0070-2H) 5962-8688701CA (OP227AJ) 5962-8757801GA (LT1007AMH) 5962-8757801PA (LT1007AMJ8) 5962-8759401XC (LM185H-1.2)	5962-8759402XX (LM185H-2.5) 5962-8760401GX (LM10H) 5962-8766601VX (LT1080MJ) 5962-8766602EX (LT1081MJ) 5962-8767501XX (LM150K) 5962-8767502XX (LT150AK) 5962-8773801GA (LT1001MH) 5962-8773801PA (LT1001MJ8) 5962-8774101XX (LT1033MK) 5962-8777501YX (LM123K) 5962-8853701GA (OP37AH) 5962-8853701PA (OP37AJ8) 5962-8853703GA (OP37CH) 5962-8853703PA (OP37CJ8) 5962-8856201XX (LT1010MH)	5962-8856201YX (LT1010MK) 5962-8859701XA (LT1004MH-1.2) 5962-8859702XA (LT1004MH-2.5) 5962-8860001GX (LT1021BM-10) 5962-8860002GX (LT1021CM-10) 5962-8860003GX (LT1021DM-10) 5962-8864101RA (LTC1060AMJ) 5962-8864601XA (LT1085MK) 5962-8864701GA (LT1021BMH-7) 5962-8864702GA (LT1021DMH-7) 5962-8876201GA (LT1021BMH-5) 5962-8876202GA (LT1021CMH-5) 5962-8876203GA (LT1021DMH-5)	
883 Operational Amplifiers	LF155AH/883 LF155H/883 LF156AH/883 LF156H/883 LF412AMH/883 LF412MH/883 LF412AMJ8/883 LF412MJ8/883 LH0070-0H/883 LH0070-1H/883 LH0070-2H/883 LH2108AD/883 LH2108D/883	LM10H/883 LM10J8/883 LM101AH/883 LM101AJ8/883 LM107H/883 LM107J8/883 LM108AH/883 LM108H/883 LM108AJ8/883 LM108J8/883 LM108H/883 LM118H/883 LM118J8/883 LT118AH/883	LT118AJ8/883 LT1001AMH/883 LT1001AMJ8/883 LT1001MH/883 LT1001MJ8/883 LT1002AMJ8/883 LT1002MJ8/883 LT1006MH/883 LT1006MJ8/883 LT1006AMH/883 LT1006AMJ8/883 LT1007AMH/883 LT1007AMJ8/883	LT1007MH/883 LT1007MJ8/883 LT1008MH/883 LT1012MD/883 LT1012MH/883 LT1013AMH/883 LT1013AMJ8/883 LT1013MH/883 LT1013MJ8/883 LT1014AMJ8/883 LT1014MJ8/883 LT1022AMH/883 LT1022MH/883

MILITARY PRODUCTS

883 Operational Amplifiers (Continued)	LT1023MH/883	LT1057AMJ8/883	LTC1052MJ8/883	OP-27CH/883	
	LT1023MJ8/883	LT1057MH/883	OP-05AH/883	OP-27CJ8/883	
	LT1024AMD/883	LT1057MJ8/883	OP-05AJ8/883	OP-37AH/883	
	LT1024MD/883	LT1058AMJ/883	OP-05H/883	OP-37AJ8/883	
	LT1028AMH/883	LT1058MJ/883	OP-05J8/883	OP-37CH/883	
	LT1028AMJ8/883	LT1078AM/883	OP-07AH/883	OP-37CJ8/883	
	LT1028MH/883	LT1078AMJ8/883	OP-07AJ8/883	OP-215AH/883	
	LT1028MJ8/883	LT1078MH/883	OP-07H/883	OP-215AJ8/883	
	LT1037AMH/883	LT1078MJ8/883	OP-07J8/883	OP-215CH/883	
	LT1037AMJ8/883	LT1079AMJ/883	OP-15AH/883	OP-215CJ8/883	
	LT1037MH/883	LT1079MJ/883	OP-15BH/883	OP-227AJ/883	
	LT1037MJ8/883	LTC1050AMH/883	OP-15CH/883	OP-227CJ/883	
	LT1055AMH/883	LTC1050AMJ8/883	OP-16AH/883	OP-237AJ/883	
	LT1055MH/883	LTC1050MH/883	OP-16BH/883	OP237CJ/883	
	LT1056AMH/883	LTC1050MJ8/883	OP-16CH/883		
	LT1056MH/883	LTC1052MH/883	OP-27AH/883		
	LT1057AMH/883	LTC1052MJ/883	OP-27AJ8/883		
	883 Regulators	LM117H/883	LM150K/883	LT138AK/883	LT1083MK-5/883
		LM117HVH/883	LT117AH/883	LT150AK/883	LT1083MK-12/883
		LM117HVK/883	LT117AHVH/883	LT1003MK/883	LT1084MK-5/883
LM117K/883		LT117AHVK/883	LT1005MK/883	LT1084MK-12/883	
LM123K/883		LT117AK/883	LT1020MJ/883	LT1085MK-5/883	
LM137H/883		LT123AK/883	LT1033MK/883	LT1085MK-12/883	
LM137HVH/883		LT137AH/883	LT1035MK/883	LT1086MK-5/883	
LM137HVK/883		LT137AHVH/883	LT1036MK/883	LT1086MK-12/883	
LM137K/883		LT137AHVK/883	LT1036MK/883	LT1086MK/883	
LM138K/883		LT137AK/883	LT1054MJ8/883		
883 References		LM129AH/883	LT580TH/883	LT1021CMH-5/883	LT1034BMH/883
		LM129BH/883	LT580UH/883	LT1021DMH-5/883	LT1034MH/883
		LM129CH/883	LT581SH/883	LT1021BMH-7/883	REF-01AH/883
		LM134H/883	LT581TH/883	LT1021DMH-7/883	REF-01AJ8/883
	LM136AH-2.5/883	LT1004MH-1.2/883	LT1021BMH-10/883	REF-01H/883	
	LM136H-2.5/883	LT1004MH-2.5/883	LT1021CMH-10/883	REF-01J8/883	
	LM185H-1.2/883	LT1009MH/883	LT1021DMH-10/883	REF-02AH/883	
	LM185H-2.5/883	LT1019MH-2.5/883	LT1029AMH/883	REF-02AJ8/883	
	LM199AH/883	LT1019MH-4.5/883	LT1029MH/883	REF-02H/883	
	LM199AH-20/883	LT1019MH-5.0/883	LT1031BMH/883	REF-02J8/883	
	LM199H/883	LT1019MH-10/883	LT1031CMH/883		
	LT580SH/883	LT1021BMH-5/883	LT1031DMH/883		
	883 Comparators	LM111H/883	LT119AH/883	LT1011MH/883	LT1018MH/883
		LM111J8/883	LT119AJ/883	LT1011MJ8/883	LT1018MJ8/883
LM119H/883		LT685MH/883	LT1016MH/883	LTC1040MJ/883	
LM119J/883		LT685MJ/883	LT1016MJ8/883	LTC1042MJ/883	
LT111AH/883		LT1011AMH/883	LT1017MH/883		
LT111AJ8/883		LT1011AMJ8/883	LT1017MJ8/883		
883 Switched-Mode Control Circuits	LT1070MK/883	LT1524J/883	LT1527AJ/883	SG1524J/883	
	LT1070HVMK/883	LT1525AJ/883	LT1846J/883	SG1525AJ/883	
	LT1071MK/883	LT1526J/883	LT1847J/883	SG1527AJ/883	
	LT1071HVMK/883				
883 Interface	LT1032MJ/883	LT1081MJ/883			
	LT1039MJ/883	LTC1045MJ/883			
	LT1080MJ/883				
Other 883	LF198AH/883	LTC1041MJ8/883	LT1054MH/883	LTC1060MJ/883	
	LF198H/883	LTC1043MD/883	LTC1059AMJ/883	LTC1061AMJ/883	
	LT1010MH/883	LTC1044MH/883	LTC1059MJ/883	LTC1061MJ/883	
	LT1010MK/883	LTC1044MJ8/883	LTC1060AMJ/883		

† Parts may be ordered using an "X" lead finish suffix. These parts will be supplied with either gold plate or solder-dip finish at Linear Technology Corporation's discretion.

* Certain parts may be ordered with "C" lead finish suffix (gold plate). Consult factory for pricing and availability.

** Bold face entries indicate new additions.

SECTION 13— NEW PRODUCTS

**REFER TO TABLE OF CONTENTS
FOR REVISED DATA LOCATION**

SECTION 13—NEW PRODUCTS

INDEX	13-2
PROPRIETARY PRODUCTS	
<i>LTC201, Quad CMOS SPST Low Charge Injection Analog Switch</i>	13-3
<i>LT1015, High Speed Dual Line Receiver</i>	13-6
<i>LT1027, Precision 5V Reference</i>	13-8
<i>LTC1049, Low Power Chopper Stabilized Op Amp with Internal Capacitors</i>	13-10
<i>LTC1051, Dual Precision Chopper Stabilized Op Amp with Internal Capacitors</i>	13-13
<i>LTC1064-2, Low Noise, High Frequency 8th Order Butterworth Lowpass Filter</i>	13-15
<i>LTC1064-3, Low Noise, High Frequency 8th Order Linear Phase Lowpass Filter</i>	13-19
<i>LTC1064-4, Low Noise, 8th Order, Clock Sweepable Cauer Lowpass Filter</i>	13-20
<i>LT1074, Switching Regulator</i>	13-21
<i>LT1077, Micropower, Single Supply, Precision Op Amp</i>	13-27
<i>LT1087, Adjustable Low Dropout Regulator with Kelvin-Sense Inputs</i>	13-28
<i>LTC1100, Precision, Single Supply, Instrumentation Amplifier (Fixed Gain = 100)</i>	13-35
<i>LT1101, Precision, Micropower, Single Supply Instrumentation Amplifier (Fixed Gain = 10 or 100)</i>	13-36
<i>LT1102, High Speed, Precision, JFET Input Instrumentation Amplifier (Fixed Gain = 10 or 100)</i>	13-48
<i>LTC1150, ±15V Chopper Stabilized Op Amp with Internal Capacitors</i>	13-49
<i>LT1188, 1.5A High Side Switch</i>	13-55
<i>LTC1290, Single Chip 12-Bit Data Acquisition System</i>	13-62
<i>LTC1291, 1-Channel, 12-Bit Serial I/O Data Acquisition System</i>	13-70
<i>LTC1292, 2-Channel, 12-Bit Serial I/O Data Acquisition System</i>	13-70
<i>LTC1293, 6-Channel, 12-Bit Serial I/O Data Acquisition System</i>	13-70
<i>LTC1294, 8-Channel, 12-Bit Serial I/O Data Acquisition System</i>	13-70
<i>LT1431, Programmable Reference</i>	13-72

NOTE

Final datasheets for products in this section are at various stages of completion as this catalog is being published. If you require a final datasheet for your application, please contact your local LTC Sales Representative, or call LTC Communications at (800) 637-5545, for availability.



Quad CMOS SPST

Low Charge Injection Analog Switch

May 1989

FEATURES

- Single 5V or ±15V Supply Operation
- Lower Charge Injection Than Standard DG201A
- Low R_{ON}
- Low Power Dissipation
- Low Leakage
- Guaranteed Break Before Make
- Latch Resistant Design
- TTL/CMOS Compatible
- Second Source for DG201A

DESCRIPTION

The LTC201 is a monolithic CMOS device consisting of four switches which are independently controlled. The switches have low on resistance and a very high off resistance. A break before make characteristic is inherent in these switches to prevent the shorting of two channels. With a supply voltage of ±15V the signal range is ±15V. The switches have special charge compensation circuitry which greatly reduces charge injection compared to the standard DG201A.

KEY SPECIFICATIONS

- R_{ON}
- Signal Range
- Leakage Current
- Supply Current
- Charge Injection

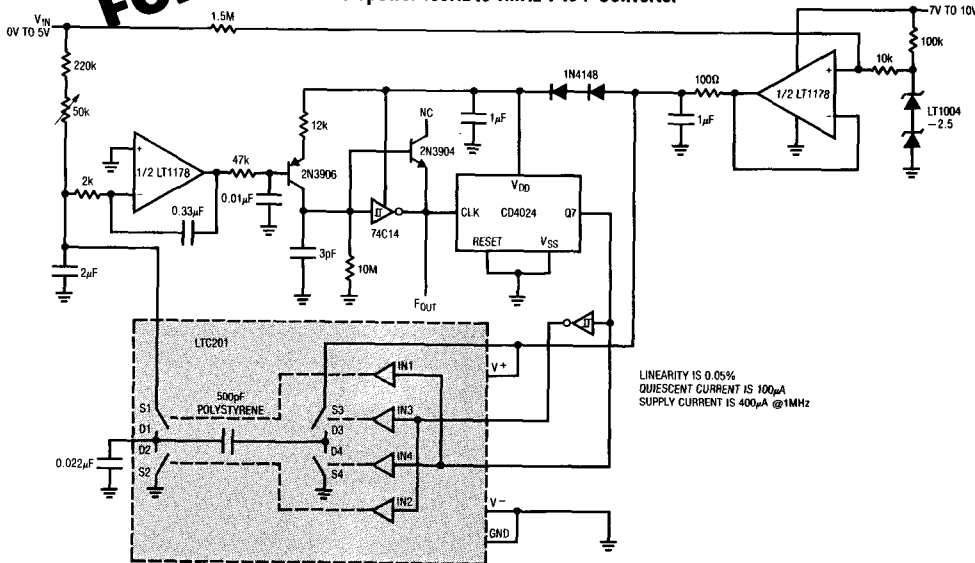
The LTC201 is designed for applications such as programmable gain amplifiers, analog multiplexers, precision charge switching and remote switching.

REFER TO TABLE OF CONTENTS FOR REVISED DATA LOCATION

60Ω
±15V
100μA
50°C

TYPICAL APPLICATION

Micropower 100Hz to 1MHz V-to-F Converter



LTC201

ABSOLUTE MAXIMUM RATINGS

(Note 1)

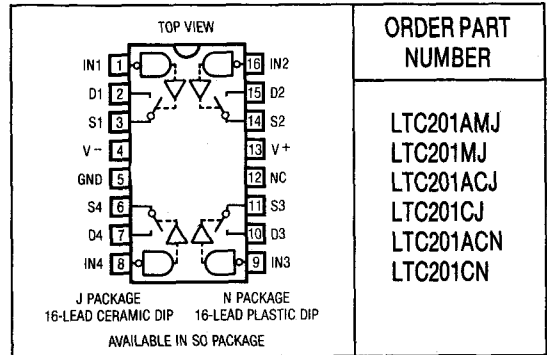
Voltages Referenced to V-

V+	44V
GND	25V
Digital Inputs, S, D (Note 3)	-2V to (V+ + 2V) or 20mA, Whichever Occurs First

Current

Any Input Except S or D	30mA
Continuous S or D	20mA
Peak S or D (Pulsed at 1ms, 10% Duty Cycle Max)	70mA
Power Dissipation (Plastic)	500mW
Power Dissipation (Ceramic)	900mW
Operating Temperature Range	
LTC201AC, LTC201C	0°C to 70°C
LTC201AM, LTC201M	-55°C to 125°C
Storage Temperature Range	-65°C to 150°C
Lead Temperature (Soldering, 10 sec.)	300°C

PACKAGE/ORDER INFORMATION



ORDER PART NUMBER

LTC201AMJ
LTC201MJ
LTC201ACJ
LTC201CJ
LTC201ACN
LTC201CN

DIGITAL AND DC ELECTRICAL CHARACTERISTICS (Note 2)

PARAMETER	CONDITIONS	LTC201A			LTC201			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Analog Signal Range		●		± 15		± 15		V
R _{ON}	-10V < V _S < 10V, I _D = 1mA	T _{MAX}		175		200		Ω
		25°C		60	120	75	160	
		T _{MIN}			120		160	
ΔR _{ON} vs V _S			20		20			%
ΔR _{ON} vs Temperature			0.5		0.5			%/°C
R _{ON} Match	V _S = 0V, I _D = 1mA		10		10			%
Off Input Leakage I _S (OFF)	V _O = ± 14V, V _S = ± 14V	●	0.5	100	0.5	100		nA
Off Output Leakage I _D (OFF)		●	0.5	100	0.5	100		
On Channel Leakage I _D (ON)		●	0.5	200	0.5	200		
Input High Voltage V _{INH}		●	2.4		2.4			V
Input Low Voltage V _{INL}		●		0.8		0.8		
Input High or Low Current I _{INH} and I _{INL}		●		1		1		μA
C _S (OFF)			5		5			pF
C _D (OFF)			12		12			
C _D , C _S (ON)			30		30			
I ⁺	All Channels On or Off V _{IN} = 0V or 2.4V	●	30	100	30	100		μA
I ⁻		●	0.1	10	0.1	10		

AC ELECTRICAL CHARACTERISTICS (Note 3)

PARAMETER	CONDITIONS	LTC201A			LTC201			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
T_{ON}	$V_S = 2V, R_L = 1k\Omega, C_L = 35pF$			600			600	ns
T_{OFF}				450			450	
Off Isolation	$V_S = 2Vp-p, R_L = 1k\Omega$ $f = 100kHz$		75			75		dB
Crosstalk			90			90		
Charge Injection Q_{INJ}	$R_S = 0\Omega, C_L = 1000pF, V_S = 0$		5			8		pC
Total Harmonic Distortion THD	$V_S = 2Vp-p, R_L = 10k\Omega$		0.01			0.01		%

The ● denotes the specifications which apply over full operating temperature range.

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: Signals on S, D, or I_N exceeding V^+ or V^- will be clamped by internal diodes. Limit forward diode current to maximum current rating.

Note 3: $V^+ = 15V, V^- = -15V$ unless otherwise noted.

FEATURES

- 10ns Response Time
- 2ns Setup Time for Latch
- Operates on Single 5V Supply
- Dual Function in 8-Pin Package
- No Input Slew Rate Requirement
- Latch Function Included On Chip
- True Differential Inputs

APPLICATIONS

- High Speed Differential Line Receiver
- Pulse Height/Width Discriminator
- Timing and Delay Generators
- Analog to Digital Interface

DESCRIPTION

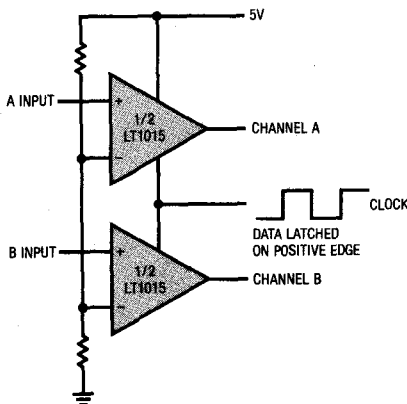
The LT1015 is a dual high speed comparator intended for line receiver and other general purpose fast comparator functions. It has 10ns response time, true differential inputs, TTL outputs, and operates from a single 5V supply. A unique output stage design virtually eliminates power supply glitching during transitions. This greatly reduces instability and crosstalk problems in multiple line applications. No minimum input slew rates are required as in previous TTL output comparators.

The LT1015 has a true latch pin for latching output data. Setup time is 2ns, allowing the comparators to capture data much faster than the actual flowthrough response time. 8-pin DIP and ceramic packages allow high packing density.

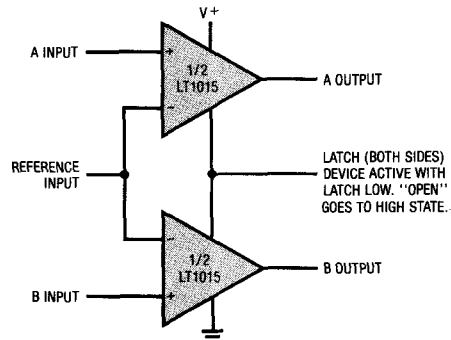
REFER TO TABLE OF CONTENTS
FOR REVISED DATA LOCATION

TYPICAL APPLICATION

2 Channel 20MHz Clocked Line Receiver



BLOCK DIAGRAM

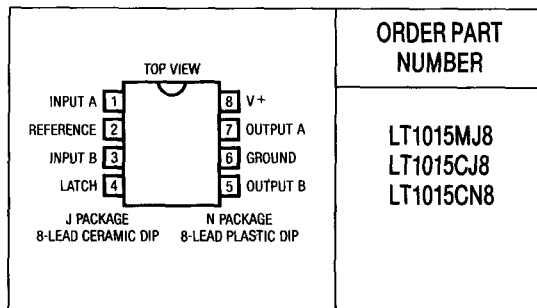


ABSOLUTE MAXIMUM RATINGS

Supply Voltage	7V
Differential Input Voltage.....	5V
Input Voltage Positive	Supply + 0.5V
Negative	- 1V
Input Current (Forced) Positive	20mA
Latch Pin Voltage.....	Supply + 1V
Output Current (Continuous).....	± 20mA
Operating Temperature Range	
LT1015M	- 55°C to 125°C*
LT1015C	0°C to 70°C
Storage Temperature Range	- 65°C to 150°C
Lead Temperature (Soldering, 10 sec.)	300°C

*Air flow must be provided for $T_A > 100^\circ\text{C}$.

PACKAGE/ORDER INFORMATION



ELECTRICAL CHARACTERISTICS

$V^+ = 4.6\text{V}$ to 5.4V , $V_{\text{LATCH}} = 0\text{V}$, Common Mode Input Voltage = 2.5V , $T_j = 25^\circ\text{C}$, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage (Note 1)	$V_{\text{CM}} = 1.25\text{V}$ to $(V^+ - 1.5\text{V})$	●	1	20	mV
Input Bias Current	$\Delta V_{\text{IN}} = 0\text{V}$ (Note 2)	●	15	30	μA
Reference Input Current	$\Delta V_{\text{IN}} = 0\text{V}$ (Note 2)	●	30	60	μA
Voltage Gain (Note 3)	$V_{\text{OUT}} = 0.5\text{V}$ to 2.5V Load = 1 TTL Gate	●	1000	2500	V/V
Common Mode Input Range (Note 5)	Minimum Input	●		1.0	V
	Maximum Input	●	$V^+ - 1.5$	$V^+ - 1.0$	V
Output High Voltage	$I_{\text{OUT}} = 4\text{mA}$	●	2.5		V
Output Low Voltage	$I_{\text{SINK}} = 4\text{mA}$	●	0.3	0.5	V
Supply Current	$V^+ = 5\text{V}$	●	55	70	mA
Latch Pin High Input Voltage	Device Latched	●		2	V
Latch Pin Low Input Voltage	Device Active	●	0.8		V
Latch Pin Current		●		1	mA
Propagation Delay	$\Delta V_{\text{IN}} \geq 20\text{mV}$ (Note 4)	●	7	10	ns
	$0^\circ\text{C} \leq T_j \leq 100^\circ\text{C}$ $-55^\circ\text{C} \leq T_j \leq 150^\circ\text{C}$	●	7	10	16
Latch Setup Time				2	ns

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: Input offset voltage is the maximum required to drive the output to a low state of 0.5V and a high state of 2.5V.

Note 2: Input currents are measured by applying a large positive differential input voltage. The resulting input current is divided by two to obtain input current at $\Delta V_{\text{IN}} = 0\text{V}$.

Note 3: Voltage gain is guaranteed by design, but not tested.

Note 4: Propagation delay is 100% tested in production with a large overdrive. The limit is guard banded to account for the slight increase ($\approx 500\text{ps}$) at 20mV overdrive.

Note 5: Common mode input range is the voltage range over which the differential input offset voltage is less than 20mV. If both inputs remain inside this common mode range, propagation delay will be unaffected. It will also be normal if the signal input is below the 1.25V lower limit when the input transition begins. An increase in propagation delay of up to 10ns may occur if the signal input is above the upper common mode limit when the transition begins. Sine wave inputs may not be affected when the peak exceeds the common mode range if the signal is inside the common mode range for 10ns before threshold is reached.

FEATURES

- Very Low Drift — 2 ppm/°C Max Slope
- Pin-Compatible with LT1021-5, REF-02
- Factory-Trimmed to $5.000V \pm 1mV @ 25^\circ C$
- Output Sinks or Sources 10mA
- Excellent Transient Response Suitable for A-to-D Reference Inputs
- Noise Reduction Pin
- Excellent Long Term Stability
- Low Noise

APPLICATIONS

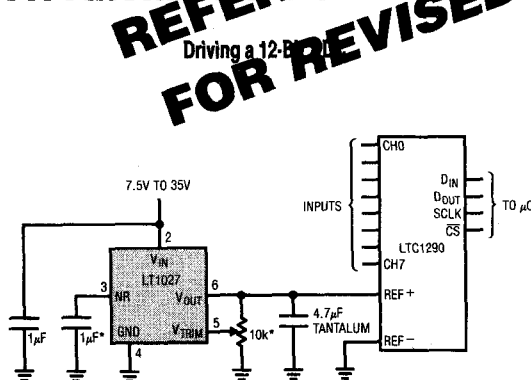
- A-to-D and D-to-A Conversion
- Digital Voltmeters
- Reference Standard
- Precision Current Source

DESCRIPTION

The LT1027 is a precision reference with extra-low drift, low noise, excellent line and load regulation and low output impedance at high frequency. This device is intended for use in 12- to 16-bit A-to-D and D-to-A systems where demanding accuracy requirements must be met without the use of power-hungry heated-substrate references. The fast-settling output recovers quickly from load transients such as those presented by A-to-D converter reference inputs. The LT1027 represents the next major advance in low-drift, high-accuracy voltage references.

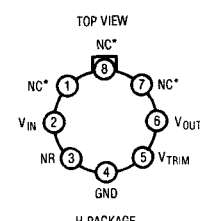
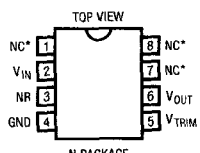
The LT1027 reference is based on LTC's proprietary advanced sub-surface emitter bipolar process which eliminates noise and stability problems associated with surface mounted devices.

TYPICAL APPLICATION



*NOISE REDUCTION CAP AND TRIM POTENTIOMETER OPTIONAL.

PACKAGE/ORDER INFORMATION

TOP VIEW	ORDER PART NUMBER
 <p>H PACKAGE 8-LEAD TO-5 METAL CAN</p> <p>*CONNECTED INTERNALLY. DO NOT CONNECT EXTERNAL CIRCUITRY TO THESE PINS.</p>	LT1027BMH LT1027CMH LT1027BCH LT1027CCH
 <p>N PACKAGE 8-LEAD PLASTIC DIP</p> <p>*CONNECTED INTERNALLY. DO NOT CONNECT EXTERNAL CIRCUITRY TO THESE PINS.</p>	LT1027BCN LT1027CCN

ABSOLUTE MAXIMUM RATINGS

Input Voltage	40V	Operating Temperature Range	
Input-Output Voltage Differential	35V	LT1027M	-55°C to 125°C
Output to Ground Voltage	7V	LT1027C	0°C to 70°C
Trim to Ground Voltage		Storage Temperature Range	
Positive	Equal to V_{OUT}	All Devices	-65°C to 150°C
Negative	-3V	Lead Temperature (Soldering, 10 sec.)	300°C
Output Short Circuit Duration			
$V_{IN} = 35V$	10 sec.		
$V_{IN} < 20V$	Indefinite		

ELECTRICAL CHARACTERISTICS $V_{IN} = 10V, I_{OUT} = 0, T_A = 25^\circ C$ unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage			5.000		V
Output Voltage Accuracy	$T_A = 25^\circ C$		± 0.02		%
Output Voltage Temperature Coefficient			2		ppm/°C
Settling Time (0.01%)	$I_{OUT} = 10mA$		2		μs
Line Regulation	$10V < V_{IN} < 40V$		4		ppm/V
Load Regulation (Source)	$0 < I_{OUT} < 10mA$		10		ppm/mA
Load Regulation (Sink)	$0 > I_{OUT} > -10mA$		25		ppm/mA
Supply Current			2		mA
Output Trim Range	$0 > V_{TRIM} > V_{OUT}$		± 50		mV

APPLICATIONS INFORMATION

Transient Response

When a 10mA load step is applied to the LT1027 output, the reference will settle to 0.01% in under 2 μs . For faster transient response under no DC load or while sourcing current, a 4.7 μF (or greater) tantalum capacitor connected between V_{OUT} and ground is recommended. This will reduce the settling time to under 500ns. Electrolytic capacitors are not advisable as the series resistance of these type units will degrade the response. If the LT1027 is to be used as a current sink, a bypass cap is not recommended. For driving capacitive-type ADCs, the 4.7 μF cap will give optimum performance, although it is not required.

Trimming Output Voltage

The LT1027 has a trim pin for adjusting output voltage. The impedance of this pin is about 20k Ω with an open circuit voltage of 2.5V. A $\pm 50mV$ trim range is obtainable by tying the trim pin to the wiper of a 10k potentiometer connected between V_{OUT} and ground. Trimming the output voltage will not affect the TC of the device.

Noise Reduction

A 1 μF capacitor between the NR (noise reduction) pin (3) and ground will reduce the noise of the LT1027 from 2.5 μV_{RMS} to 1.5 μV_{RMS} in a 0.1Hz to 1kHz bandwidth. The pin should be left open if not used. Open circuit voltage on the NR pin is 4.4V. This point goes to the internal amplifier input and is gained up to 5.000V. Do not put any DC load on this pin.

Low Power Chopper Stabilized Operational Amplifier with Internal Capacitors

April 1989

FEATURES

- Low Supply Current 200 μ A
- No External Components Required
- Maximum Offset Voltage 10 μ V
- Maximum Offset Voltage Drift 0.1 μ V/ $^{\circ}$ C
- Single Supply Operation 4.75V to 16V
- Input Common Mode Range Includes Ground
- Output Swings to Ground
- Typical Overload Recovery Time 25ms

APPLICATIONS

- 4mA–20mA Current Loops
- Thermocouple Amplifiers
- Electronic Scales
- Medical Instrumentation
- Strain Gauge Amplifiers
- High Resolution Data Acquisition

DESCRIPTION

The LTC1049 is a high performance low power chopper stabilized operational amplifier. The two sample-and-hold capacitors usually required externally by other chopper stabilized amplifiers are integrated on the chip. Further, the LTC1049 offers superior DC and AC performance with a nominal supply current of only 200 μ A.

The LTC1049 has an offset voltage of 5 μ V, with drift of 0.01 μ V/ $^{\circ}$ C, 0.1Hz to 10Hz input noise voltage is 3 μ Vp-p and typical voltage gain is 100dB. The slew rate is 0.8V/ μ s with the gain bandwidth product of 0.8MHz.

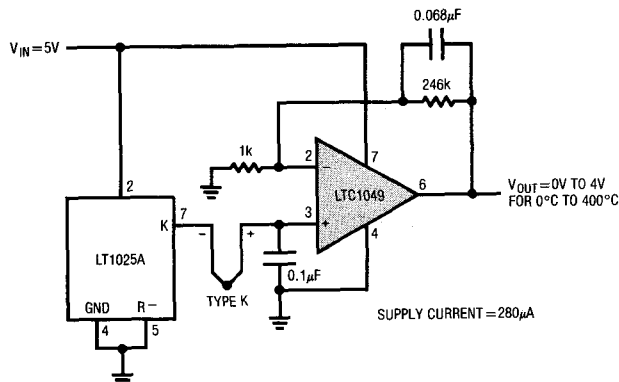
Overload recovery times from positive and negative saturation conditions are 6ms and 25ms respectively, a very significant improvement over chopper amplifiers using external capacitors.

The LTC1049 is available in standard 8-pin metal can, plastic and ceramic dual in line packages as well as an 8-pin SO package. The LTC1049 can be a plug-in replacement for most standard op amps with improved performance.

 REFER TO TABLE OF CONTENTS
 FOR REVISED DATA LOCATION

TYPICAL APPLICATION

Single Supply Thermocouple Amplifier

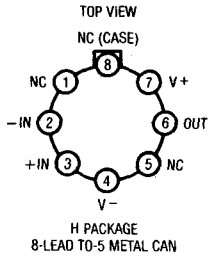
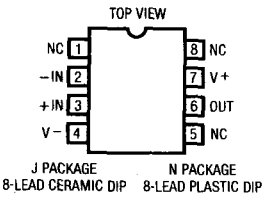
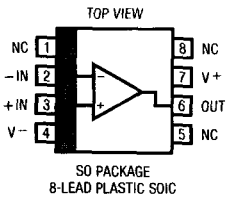


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Total Supply Voltage (V^+ to V^-)	18V
Input Voltage ($V^+ + 0.3V$) to ($V^- - 0.3V$)	
Output Short Circuit Duration	Indefinite
Operating Temperature Range	
LTC1049M	-55°C to 125°C
LTC1049C	-40°C to 85°C
Storage Temperature Range	-65°C to 150°C
Lead Temperature (Soldering, 10 sec.)	300°C

PACKAGE/ORDER INFORMATION

 <p>TOP VIEW NC (CASE) H PACKAGE 8-LEAD TO-5 METAL CAN</p>	<p>ORDER PART NUMBER</p> <p>LTC1049MH LTC1049CH</p>
 <p>TOP VIEW J PACKAGE 8-LEAD CERAMIC DIP N PACKAGE 8-LEAD PLASTIC DIP</p>	<p>LTC1049MJ8 LTC1049CJ8 LTC1049CN8</p>
 <p>TOP VIEW SO PACKAGE 8-LEAD PLASTIC SOIC</p>	<p>LTC1049CS8</p>

ELECTRICAL CHARACTERISTICS

$V_S = \pm 5V$, $T_A =$ operating temperature range, unless otherwise specified.

PARAMETER	CONDITIONS	LTC1049M			LTC1049C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$T_A = 25^\circ\text{C}$ (Note 3)		± 2	± 10		± 2	± 10	μV
Average Input Offset Drift	(Note 3)	●	± 0.02	± 0.1		± 0.02	± 0.1	$\mu\text{V}/^\circ\text{C}$
Long Term Offset Voltage Drift			50			50		nV/mo
Input Offset Current	$T_A = 25^\circ\text{C}$	●	± 30	± 60 ± 150		± 30	± 100 ± 150	pA pA
Input Bias Current	$T_A = 25^\circ\text{C}$	●	± 15	± 30 ± 800		± 15	± 50 ± 150	pA pA
Input Noise Voltage	0.1Hz to 10Hz		3.0			3.0		$\mu\text{Vp-p}$
	0.1Hz to 1Hz		1.0			1.0		$\mu\text{Vp-p}$
Input Noise Current	$f = 10\text{Hz}$ (Note 4)		2.0			2.0		$\text{fA}/\sqrt{\text{Hz}}$
Common Mode Rejection Ratio	$V_{CM} = V^-$ to 2.7V	●	115	130		110	130	dB
Power Supply Rejection Ratio	$V_S = \pm 2.375\text{V}$ to $\pm 8\text{V}$	●	115	130		110	130	dB
Large Signal Voltage Gain	$R_L = 100\text{k}\Omega$, $V_{OUT} = \pm 4.9\text{V}$	●	130	160		130	160	dB

ELECTRICAL CHARACTERISTICS

$V_S = \pm 5V$, T_A = operating temperature range, unless otherwise specified.

PARAMETER	CONDITIONS	LTC1049M			LTC1049C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Maximum Output Voltage Swing	$R_L = 10k\Omega$ $T_A = 25^\circ C$		-4.9/ +4.2			-4.9/ +4.2		V
		●	-4.6/ +3.2			-4.6/ +3.2		V
	$R_L = 100k\Omega$	●	± 4.9	± 4.97		± 4.9	± 4.97	V
Slew Rate	$R_L = 10k\Omega$, $C_L = 50pF$		0.8			0.8		V/ μs
Gain Bandwidth Product			0.8			0.8		MHz
Supply Current	No Load $T_A = 25^\circ C$		200	270		200	300	μA
		●		400			450	μA
Internal Sampling Frequency			700			700		Hz

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: Absolute Maximum Ratings are those values beyond which the life of the device may be impaired.

Note 2: Connecting any terminal to voltages greater than V^+ or less than V^- may cause destructive latch up. It is recommended that no sources operating from external supplies be applied prior to power-up of the LTC1049.

Note 3: These parameters are guaranteed by design. Thermocouple effects preclude measurement of these voltage levels in high speed automatic test systems. V_{OS} is measured to a limit determined by test equipment capability.

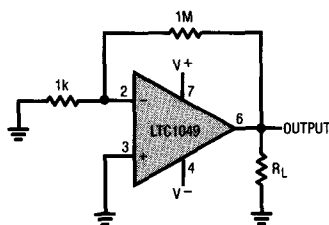
Note 4: Current Noise is calculated from the formula:

$$I_N = \sqrt{2q \cdot 1b}$$

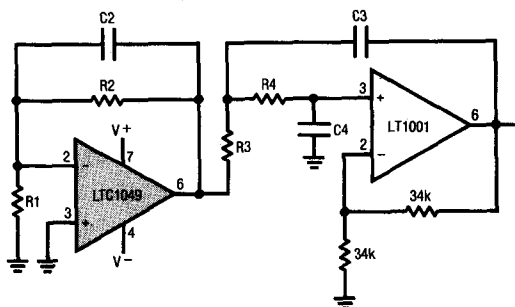
where $q = 1.6 \times 10^{-19}$ Coulomb.

TEST CIRCUITS

Electrical Characteristics Test Circuit



DC to 10Hz and DC to 1Hz Noise Test Circuit



BANDWIDTH	R1	R2	R3	R4	C2	C3	C4
10Hz	16.2 Ω	162k	16.2k	16.2 Ω	0.1 μF	1.0 μF	1.0 μF
1Hz	16.2 Ω	162k	162k	162k	1.0 μF	1.0 μF	1.0 μF

Dual Precision Chopper Stabilized Operational Amplifier With Internal Capacitors

May 1989

FEATURES

- Dual Low Cost Precision Op Amp
- No External Components Required
- Maximum Offset Voltage $5\mu\text{V}$
- Maximum Offset Voltage Drift $0.05\mu\text{V}/^\circ\text{C}$
- Low Noise $1.5\mu\text{V}_{\text{p-p}}$ (0.1Hz to 10Hz)
- Minimum Voltage Gain, 120dB
- Minimum PSRR, 120dB
- Minimum CMRR, 114dB
- Low Supply Current 1mA/Op Amp
- Single Supply Operation 4.75V to 16V
- Input Common Mode Range Includes Ground
- Output Swings to Ground
- Typical Overload Recovery Time 3ms
- Pin Compatible with Industry Standard Dual Op Amps

APPLICATIONS

- Thermocouple Amplifier
- Electronic Test Equipment
- Medical Instrumentation
- Strain Gauge Amplifier
- High Resolution Data Acquisition
- DC Accurate R, C Active Filters

DESCRIPTION

The LTC1051 is a high performance, low cost dual chopper stabilized operational amplifier. The unique achievement of the LTC1051 is that it integrates on chip the sample-and-hold capacitors usually required externally by other chopper amplifiers. Further, the LTC1051 offers better combined overall DC and AC performance than is available from other chopper stabilized amplifiers with or without internal sample/hold capacitors.

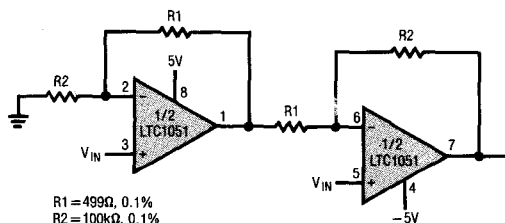
The LTC1051 has an offset voltage of $0.5\mu\text{V}$, drift of $0.01\mu\text{V}/^\circ\text{C}$, DC to 10Hz input noise voltage of $1.5\mu\text{V}_{\text{p-p}}$ and a typical voltage gain of 140dB. The slew rate of $4\text{V}/\mu\text{s}$ and a 0.5MHz bandwidth product are achieved with only 1mA of supply current per op amp.

Overload recovery times from positive and negative saturation conditions are 1.5ms and 3ms respectively, about 100 or more times improvement over chopper amplifiers using external capacitors.

The LTC1051 is available in standard plastic and ceramic dual in line packages as well as a 16-pin SOL package. The LTC1051 can be a plug in replacement for most standard dual op amps with improved performance.

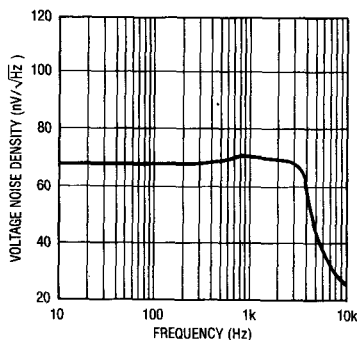
TYPICAL APPLICATION

High Performance Low Cost Instrumentation Amplifier



$R1 = 499\Omega$, 0.1%
 $R2 = 100\text{k}\Omega$, 0.1%
 GAIN = 201
 MEASURED CMRR $\sim 120\text{dB}$ AT DC
 MEASURED INPUT V_{OS} $3\mu\text{V}$
 MEASURED INPUT NOISE $2\mu\text{V}_{\text{p-p}}$ (DC - 10Hz)

LTC1051 Noise Spectrum



LTC1051

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V+ to V-)	18V
Input Voltage	(V+ + 0.3V) to (V- - 0.3V)
Output Short Circuit Duration	Indefinite
Operating Temperature Range	
LTC1051M	-55°C to 125°C
LTC1051C	-40°C to 85°C
Storage Temperature Range	-65°C to 150°C
Lead Temperature (Soldering, 10 sec.)	300°C

PACKAGE/ORDER INFORMATION

<p>J PACKAGE 8-LEAD CERAMIC DIP</p> <p>N PACKAGE 8-LEAD PLASTIC DIP</p>	ORDER PART NUMBER LTC1051MJ8 LTC1051CJ8 LTC1051CN8
<p>SO PACKAGE 16-LEAD PLASTIC SOIC</p>	LTC1051CS

ELECTRICAL CHARACTERISTICS

$V_S = \pm 5V$, $T_A =$ operating temperature range unless otherwise specified.

PARAMETER	CONDITIONS	LTC1051			UNITS
		MIN	TYP	MAX	
Input Offset Voltage	$T_A = 25^\circ\text{C}$		± 0.5	± 5	μV
Average Input Offset Drift		●	± 0.0	± 0.05	$\mu\text{V}/^\circ\text{C}$
Long Term Offset Drift			50		nV/√Mo
Input Bias Current	$T_A = 25^\circ\text{C}$ LTC1051C LTC1051M	●	± 15	± 65 ± 125 ± 450	pA
Input Offset Current	$T_A = 25^\circ\text{C}$	●	± 30	± 125 ± 175	pA
Input Noise Voltage	$R_S = 100\Omega$, DC to 10Hz $R_S = 100\Omega$, DC to 1Hz		1.5 0.4		μV_{pp} μV_{pp}
Input Noise Current	$f = 10\text{Hz}$		2.2		fA/√Hz
Common Mode Rejection Ratio, CMRR	$V_{CM} = V- \text{ to } +2.7V$, $T_A = 25^\circ\text{C}$	●	114 110	130	dB dB
Differential CMRR			114		dB
Power Supply Rejection Ratio	$V_S = \pm 2.375V \text{ to } \pm 8V$	●	120	140	dB
Large Signal Voltage Gain	$R_L = 10k\Omega$, $V_{OUT} = \pm 4V$	●	120	160	dB
Maximum Output Voltage Swing	$R_L = 10k\Omega$ $R_L = 100k\Omega$	●	± 4.7	± 4.85 ± 4.95	V V
Slew Rate	$R_L = 10k\Omega$, $C_L = 50pF$		4		V/μs
Gain Bandwidth Product			2.5		MHz
Supply Current	No Load, $T_A = 25^\circ\text{C}$	●	2	3.25 4.5	mA mA
Internal Sampling Frequency			3		kHz

$V_S = 5V$, GND, $T_A =$ operating temperature range unless otherwise specified.

PARAMETER	CONDITIONS	LTC1051			UNITS
		MIN	TYP	MAX	
Input Offset Voltage	$T_A = 25^\circ\text{C}$		± 0.5	± 5	μV
Input Offset Drift			± 0.01	± 0.05	$\mu\text{V}/^\circ\text{C}$
Input Bias Current	$T_A = 25^\circ\text{C}$		± 10	± 50	pA
Input Offset Current	$T_A = 25^\circ\text{C}$		± 20	± 80	pA
Input Noise Voltage	DC to 10Hz		1.8		μV_{pp}
Supply Current	No Load, $T_A = 25^\circ\text{C}$	●	1	2	mA

The ● denotes the specifications which apply over the full operating temperature range.

Low Noise, High Frequency, 8th Order Butterworth Lowpass Filter

May 1989

FEATURES

- 8th Order Filter in a 14-Pin Package
- 140kHz Maximum Corner Frequency
- No External Components
- 50:1 and 100:1 Clock to Cutoff Frequency Ratio
- 80 μ V_{RMS} Total Wideband Noise
- 0.03% THD or Better
- Operates from $\pm 2.37V$ to $\pm 8V$ Power Supplies

APPLICATIONS

- Antialiasing Filters
- Smoothing Filters
- Tracking High Frequency Lowpass Filters

DESCRIPTION

The LTC1064-2 is a monolithic 8th order lowpass butterworth filter, which provides a maximally flat passband. The attenuation slope is $-48dB/octave$ and the maximum attenuation is in excess of 80dB. An external TTL or CMOS clock programs the filter's cutoff frequency. The clock to cutoff frequency ratio is 100:1 (pin 10 at negative supply) or 50:1 (pin 10 at V⁺). The maximum cutoff frequency is 140kHz. No external components are needed.

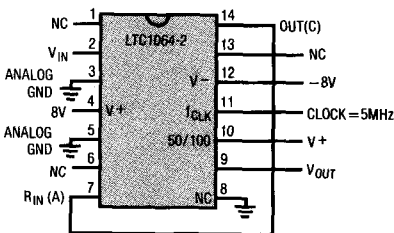
The LTC1064-2 features low wideband noise and low harmonic distortion even for input voltages up to 3V_{RMS}. In fact the LTC1064-2's overall performance competes with equivalent multi-op amp RC active realizations. The LTC1064-2 is available in a 14-pin DIP or 16-pin surface mounted SOL package. The LTC1064-2 is fabricated using LTC's enhanced analog CMOS Si-gate process.

The LTC1064-2 is pin compatible with the LTC1064-1.

REFER TO TABLE OF CONTENTS
FOR REVISED DATA LOCATION

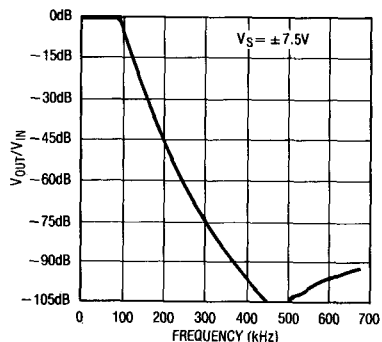
TYPICAL APPLICATION

8th Order Clock Sweepable
Lowpass Butterworth Filter



NOTE: THE POWER SUPPLIES SHOULD BE BYPASSED BY A 0.1 μ F CAPACITOR CLOSE TO THE PACKAGE. THE NC PINS 1, 6, 8, AND 13 SHOULD BE PREFERABLY GROUNDED.

Measured Frequency Response



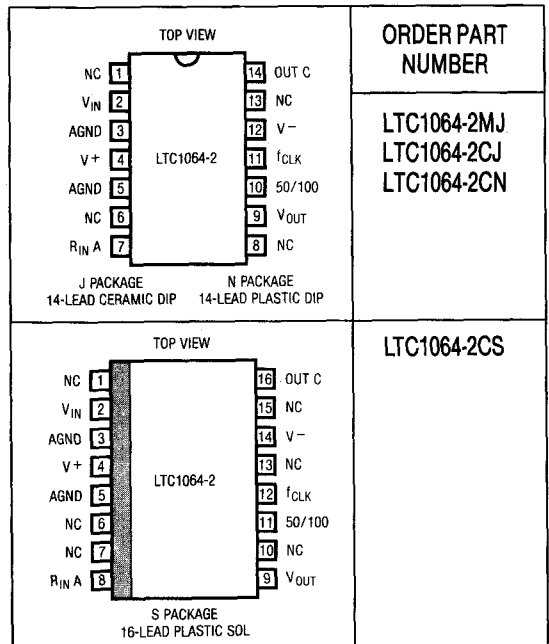
13

LTC1064-2

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V^+ to V^-)	16.5V
Power Dissipation	400mW
Storage Temperature Range	-65°C to 150°C
Lead Temperature (Soldering, 10 sec.)	300°C
Operating Temperature Range	
LTC1064-2M	-55°C to 125°C
LTC1064-2C	-40°C to 85°C

PACKAGE/ORDER INFORMATION



ORDER PART NUMBER

LTC1064-2MJ
LTC1064-2CJ
LTC1064-2CN

LTC1064-2CS

ELECTRICAL CHARACTERISTICS

$V_S = \pm 7.5V$, 100:1, $f_{CLK} = 2MHz$, $R_1 = 10k\Omega$, $T_A = 25^\circ$, TTL clock input level, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Passband Gain (Note 1)	Referenced to 0dB, 1Hz to 1kHz	-0.5		0.15	dB
Gain TempCo			0.0002		dB/°C
-3dB Frequency	100:1		20		kHz
	50:1		40		kHz
Gain at -3dB Frequency	Referenced to 0dB, $f_{IN} = 20kHz$		-3	-2.75	dB
Stopband Attenuation	At $1.5f_{-3dB}$, 50:1, $f_{IN} = 60kHz$	24	27		dB
Stopband Attenuation	At $2f_{-3dB}$, 100:1, $f_{IN} = 40kHz$	-46	47		dB
Stopband Attenuation	At $3f_{-3dB}$, 100:1, $f_{IN} = 60kHz$		74		dB
Stopband Attenuation	At $4f_{-3dB}$, 100:1, $f_{IN} = 80kHz$		90		dB
Input Frequency Range	100:1	0		$< f_{CLK}/2$	kHz
	50:1	0		$< f_{CLK}$	kHz
Output Voltage Swing and Operating Input Voltage Range	$V_S = \pm 2.37V$	-1.0		1.0	V
	$V_S = \pm 5V$	-3.1		3.2	V
	$V_S = \pm 7.5V$	-5.0		5.2	V
Total Harmonic Distortion	$V_S = \pm 5V$, Input = $1V_{RMS}$ at 1kHz		0.015		%
	$V_S = \pm 7.5V$, Input = $3V_{RMS}$ at 1kHz		0.03		%
Wideband Noise	$V_S = \pm 5V$, Input = GND 1Hz-1.99MHz		80		μV_{RMS}
	$V_S = \pm 7.5V$, Input = GND 1Hz-1.99MHz		90		μV_{RMS}
Output DC Offset (Note 1)	$V_S = \pm 7.5V$		± 30	± 125	mV
Output DC Offset TempCo	$V_S = \pm 5V$		-90		$\mu V/^\circ C$

ELECTRICAL CHARACTERISTICS

$V_S = \pm 7.5V$, 100:1, $f_{CLK} = 2MHz$, $R_1 = 10k\Omega$, $T_A = 25^\circ C$, TTL clock input level, unless otherwise specified.

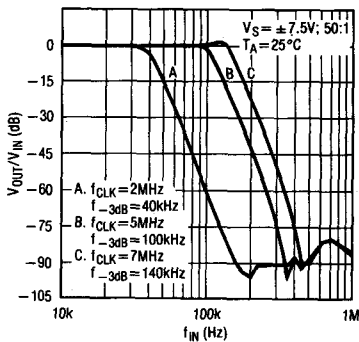
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Impedance		10	20		k Ω
Output Impedance	$f_{OUT} = 10kHz$		2		Ω
Output Short Circuit Current	Source/Sink		3/1		mA
Clock Feedthrough			200		μV_{RMS}
Maximum Clock Frequency	50% Duty Cycle, $V_S = \pm 5V$			5	MHz
	50% Duty Cycle, $T_A = 25^\circ C$, $V_S = \pm 7.5V$			7	MHz
Power Supply Current	$V_S = \pm 2.37V$, $f_{CLK} = 1MHz$	●		16	mA
		●	12	18	mA
	$V_S = \pm 5V$, $f_{CLK} = 1MHz$	●		22	mA
		●	16	20	mA
Power Supply Voltage Range		●	± 2.37	± 8	V

The ● denotes the specifications which apply over the full operating temperature range.

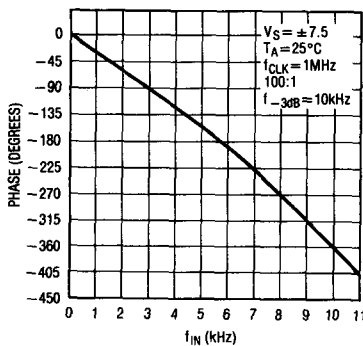
Note 1: For tighter specifications contact LTC Marketing.

TYPICAL PERFORMANCE CHARACTERISTICS

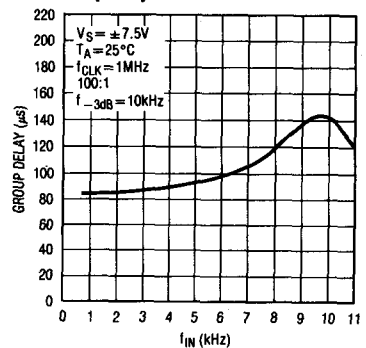
Graph 1. Amplitude Response



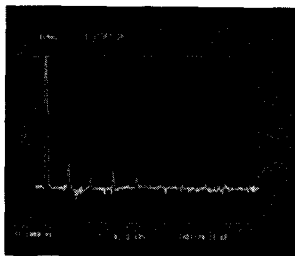
Graph 2. Phase Response



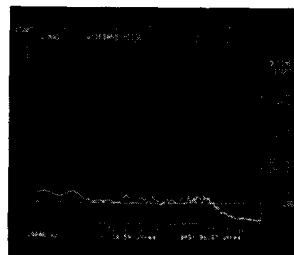
Graph 3. Group Delay vs Frequency



Graph 4. Total Harmonic Distortion = 0.03%,
Input = $3V_{RMS}$ at 1kHz, $V_S = \pm 7.5V$,
 $f_{CLK} = 1MHz$, 100:1 $f_{-3dB} = 10kHz$

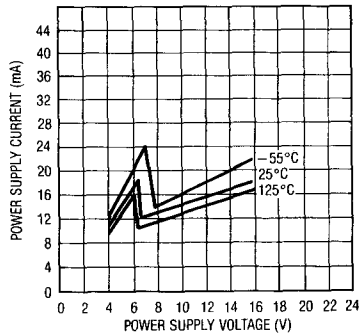


Graph 5. Wideband Noise = $87\mu V_{RMS}$,
 $V_S = \pm 7.5V$, $f_{CLK} = 2MHz$, 100:1
 $f_{-3dB} = 20kHz$

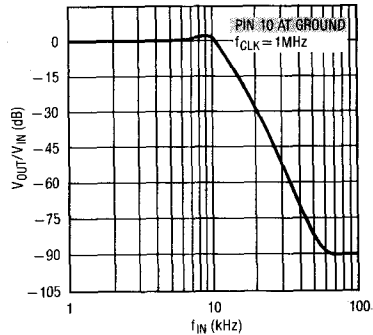


TYPICAL PERFORMANCE CHARACTERISTICS

Graph 6. Power Supply vs Current



Graph 7. Amplitude Response with Pin 10 at Ground



PIN DESCRIPTION

The power supply pins (4, 12), clock pin (11), input/output pins (2, 9) and analog ground pins (3, 5) are fully discussed in the LTC1064-1 datasheet.

The “no connection” pins (1, 6, 8, 13) should be preferably grounded, especially when high cutoff frequencies are sought.

When the 50/100 pin (10) is connected to V^+ , the $f_{CLK}/f - 3dB$ ratio is equal to 50. When pin 10 is at V^- , the $f_{CLK}/f - 3dB$ ratio equals 100. When pin 10 is grounded (or floated), the passband of the filter loses its flatness, Graph 7, and its amplitude response does not approximate a Butterworth filter.

Low Noise, High Frequency, 8th Order Linear Phase Lowpass Filter

March 1989

FEATURES

- 8th Order Filter in a 14-Pin Package
- 100kHz Maximum Corner Frequency
- No External Components
- 75:1 and 150:1 Clock to Cutoff Frequency Ratio
- $80\mu\text{VRMS}$ Total Wideband Noise
- 0.005% THD or Better
- Operates from $\pm 2.37\text{V}$ to $\pm 8\text{V}$ Power Supplies
- Low Total Output DC Offset

APPLICATIONS

- Antialiasing Filters
- Smoothing Filters
- Tracking High Frequency Lowpass Filter

DESCRIPTION

The LTC1064-3 is a monolithic 8th order lowpass Bessel filter, which provides a linear phase response over its entire passband. An external TTL or CMOS clock programs the filter's cutoff frequency. The clock to cutoff frequency ratio is 75:1 (pin 10 at V^+) or 150:1 (pin 10 at V^-). The maximum cutoff frequency is 100kHz. No external components are needed.

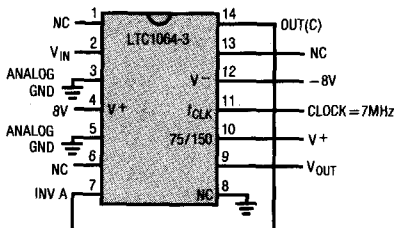
The LTC1064-3 features low wideband noise and low harmonic distortion even for input voltages up to $3V_{\text{RMS}}$. In fact the LTC1064-3's dynamic performance competes with equivalent 10-op amp RC active realizations. The LTC1064-3 is available in a 14-pin DIP or 16-pin surface mounted SOIC package. The LTC1064-3 is fabricated using LTC's standard analog CMOS Si-gate process.

The LTC1064-3 is pin compatible with the LTC1064-1, -2, and -4.

REFER TO TABLE OF CONTENTS
FOR REVISED DATA LOCATION

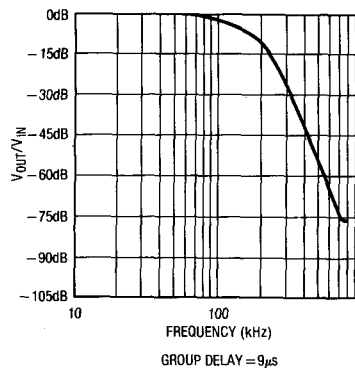
TYPICAL APPLICATION

8th Order Clock Sweeplable
Lowpass Bessel Filter



NOTE: THE POWER SUPPLIES SHOULD BE BYPASSED BY A $0.1\mu\text{F}$ OR BETTER CAPACITOR CLOSE TO THE PACKAGE. THE CONNECTION BETWEEN PINS 7 AND 14 SHOULD BE MADE UNDER THE I.C. PACKAGE.

Measured Frequency Response



Low Noise, 8th Order, Clock Sweepable Cauer Lowpass Filter

February 1989

FEATURES

- 8th Order Filter in a 14-Pin Package
- 80dB or More Stopband Attenuation
- 50:1 and 100:1 Clock to Center Ratio
- $130\mu V_{RMS}$ Total Wideband Noise
- 0.03% THD or Better
- 100kHz Maximum Cutoff Frequency
- Operates up to $\pm 8V$ Power Supplies
- Input Frequency Range up to 50 Times the Filter Cutoff Frequency

APPLICATIONS

- Antialiasing Filters
- Telecom Filters
- Sinewave Generators

DESCRIPTION

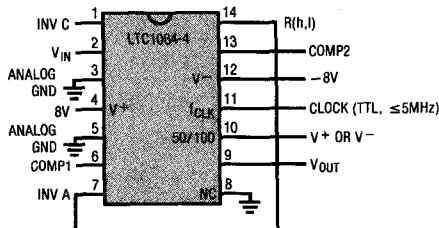
The LTC1064-4 is an 8th order, clock sweepable Cauer low-pass switched capacitor filter. An external TTL or CMOS clock programs the value of the filter's cutoff frequency. With pin 10 at V^+ , the clock to cutoff frequency ratio is 50:1; the passband ripple is $\pm 0.1dB$ and the stopband attenuation is 80dB at $2 \times f_{CUTOFF}$. Cutoff frequencies up to 100kHz can be achieved. When pin 10 is at V^- , the filter has a transitional Butterworth-Cauer response with a clock to $-3dB$ frequency ratio of 100:1. The stopband attenuation of 92dB is 20 times the cutoff frequency.

The LTC1064-4 features low noise and low harmonic distortion even when input voltages up to $3V_{RMS}$ are applied. The LTC1064-4's overall performance competes with equivalent multi-op amp RC active realizations. The LTC1064-4 is compatible with the LTC1064-1, LTC1064-2, and LTC1064-3.

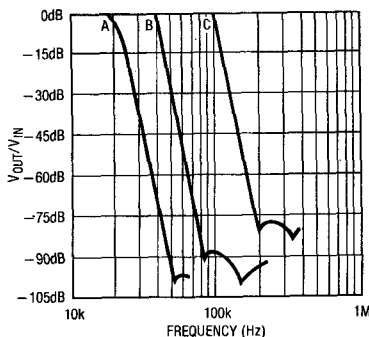
The LTC1064-4 is manufactured using Linear Technology's enhanced LTCMOS™ silicon gate process.

REFER TO TABLE OF CONTENTS FOR REVISED DATA LOCATION

TYPICAL APPLICATION

8th Order Clock Sweepable Lowpass Elliptic Filter


NOTE: THE POWER SUPPLIES SHOULD BE BYPASSED BY A $0.1\mu F$ CAPACITOR CLOSE TO THE PACKAGE. BYPASSING PIN 10 WITH A $0.1\mu F$ DISC CERAMIC CAPACITOR IMPROVES CLOCK FEEDTHROUGH. FOR CUTOFF FREQUENCY ABOVE 40kHz, USE $27pF$ - $5pF$ COMPENSATION CAPACITORS BETWEEN PINS 13 AND 1 AND 6 AND 7. THE CONNECTION BETWEEN PINS 7 AND 14 SHOULD BE PHYSICALLY DONE UNDER THE PACKAGE.

Measured Frequency Response


CURVE A: $f_{CLK}=2MHz$, 100:1
 CURVE B: $f_{CLK}=2MHz$, 50:1
 CURVE C: $f_{CLK}=5MHz$, 50:1
 $C_{COMP1}=18pF$
 $C_{COMP2}=24pF$

FEATURES

- 5A On-Board Switch
- Up to 200kHz Switching Frequency
- Greatly Improved Dynamic Behavior
- Available in Low Cost 5-Lead Packages
- Only 7mA Quiescent Current
- Programmable Current Limit
- Operates Up to 60V Input
- Includes Output Voltage Monitor
- Micropower Shutdown Mode

APPLICATIONS

- 5A Buck Converter with Output Voltage Range of 2.5V to 50V
- Tapped Inductor Buck Converter with 10A Output at 5V
- Positive-to-Negative Converter, 4.5V to 50V Input, -3.5V to -40V Output
- Negative Boost Converter, -4.5V to -40V Input, -8V to -50V Output
- Multiple Output Buck Converters
- Single or Multiple Output Flyback or Forward Converter

DESCRIPTION

The LT1074 is a 5A monolithic bipolar switching regulator which requires only a few external parts for normal operation. The power switch, all oscillator and control circuitry, all current limit components, and an output monitor are included on the chip. The topology is a classic positive "buck" configuration but several design innovations allow this device to be used as a positive to negative converter,

a negative boost converter, and as a flyback or forward converter. The switch output is specified to swing 40V below ground. This feature permits the LT1074 to use a tapped inductor in the buck mode, with output currents up to 10A using no external switch transistor.

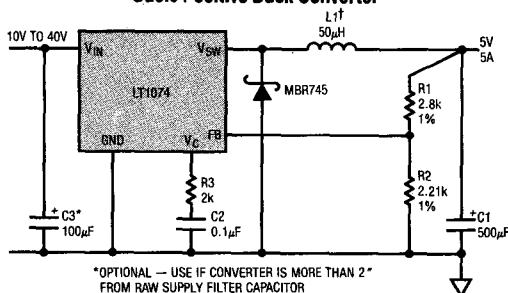
The LT1074 uses a true analog multiplier in the feedback loop. This makes the device respond nearly instantaneously to input voltage fluctuations and makes loop gain independent of input voltage. As a result, dynamic behavior of the regulator is significantly improved over previous voltage mode designs without the complexity and noise sensitivity of current mode approaches.

On-chip pulse by pulse current limiting makes the LT1074 nearly bust-proof for output overloads or shorts, and avoids surge damage to external components. The input voltage range as a buck converter is 8V to 60V, but a self-boot feature allows the device to operate with input voltages as low as 4.5V in the inverting and boost applications.

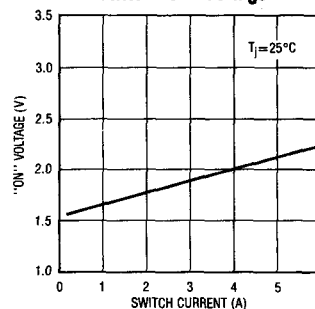
The LT1074 is available in low cost 5-lead TO-220 or TO-3 packages with frequency pre-set at 100kHz and current limit at 7A. An 11-pin single-in-line package (SIP) is also available which allows switching frequency to be increased to 200kHz and current limit to be adjusted down to zero. In addition, full micropower shutdown can be programmed as well as external current sensing, and soft start. An output monitor "status" pin can be used as a microprocessor reset, and a complementary output pin will allow implementation of ultra-high-efficiency designs.

TYPICAL APPLICATION

Basic Positive Buck Converter



Switch "On" Voltage



ABSOLUTE MAXIMUM RATINGS

Input Voltage	
LT1074	45V
LT1074HV	64V
Switch Voltage with Respect to Input Voltage	
LT1074	64V
LT1074HV	75V
Switch Voltage with Respect to Ground Pin	
LT1074	35V
LT1074HV	45V
Feedback Pin Voltage	-2V, +10V
Shutdown Pin Voltage	40V
Status Pin Voltage	30V
(Current Must Be Limited to 5mA When Status Pin Switches "On")	
Complementary Output Voltage	40V
(Current Must Be Limited to 15mA When Output Switches "On")	
I _{LIM} Pin Voltage (Forced)	4.5V
ExtLim Pin Voltage	V _{IN} - 2V to V _{IN} + 0.4V
Freq Pin Voltage	5.5V
Maximum Operating Ambient Temperature Range	
LT1074C, LT1074HVC	0°C to 70°C
LT1074M, LT1074HVM	-55°C to 125°C
Maximum Operating Junction Temperature Range	
LT1074C, LT1074HVC	0°C to 100°C
LT1074M, LT1074HVM	-55°C to 150°C
Maximum Storage Temperature	-65°C to 150°C
Lead Temperature (Soldering, 10 sec)	300°C

PACKAGE/ORDER INFORMATION

<p>BOTTOM VIEW</p> <p>K PACKAGE 4-LEAD TO-3 METAL CAN</p>	<p>ORDER PART NUMBER</p> <p>LT1074MK LT1074HVMK LT1074CK LT1074HVCK</p>
<p>FRONT VIEW</p> <p>T PACKAGE 5-LEAD TO-220</p> <p>LEADS ARE FORMED STANDARD FOR STRAIGHT LEADS, ORDER FLOW 06</p>	<p>LT1074CT LT1074HVCT</p>
<p>FRONT VIEW</p> <p>V PACKAGE 11-LEAD SIP</p> <p>CASE IS CONNECTED TO GROUND LEADS ARE FORMED.</p>	<p>LT1074CV LT1074HVCV</p>

ELECTRICAL CHARACTERISTICS $T_J = 25^\circ\text{C}$, $V_{IN} = 25\text{V}$, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Switch "On" Voltage (Note 1)	$I_{SW} = 1\text{A}$, $T_J \geq 0^\circ\text{C}$				1.8	V
	$I_{SW} = 1\text{A}$, $T_J < 0^\circ\text{C}$				2.0	V
	$I_{SW} = 5\text{A}$, $T_J \geq 0^\circ\text{C}$				2.3	V
	$I_{SW} = 5\text{A}$, $T_J < 0^\circ\text{C}$				2.5	V
Switch "Off" Leakage	(Note 6, 7)			1	300	μA
Supply Current	$V_{FB} = 2.5\text{V}$, $V_{IN} \leq V_{MAX}$ (Note 2, 7)			7	9	mA
Minimum Supply Voltage	Normal Mode	●		7.3	8	V
	Startup Mode	●		3.5	4.5	V
Switch Current Limit	I_{LIM} Open	●	5	6.5	8.5	A
	$R_{LIM} = 14\text{k}$ (Note 5)			5		A
	$R_{LIM} = 8.4\text{k}$ (Note 5)			3		A
Switching Frequency		●	90	100	110	kHz
	$V_{FB} = 0\text{V}$ through $2\text{k}\Omega$		85	20	125	kHz
Error Amplifier Voltage Gain	$1\text{V} \leq V_C \leq 4\text{V}$			2000		V/V
Error Amplifier Transconductance				4000		μmho
Feedback Pin Bias Current	$V_{FB} = V_{REF}$	●		0.5	2	μA
Reference Voltage	$V_C = 2\text{V}$	●	2.155	2.21	2.265	V
Reference Voltage Tolerance	All Conditions of Input Voltage, Output Voltage, Temperature and Load Current	●		± 0.5	± 1.5	%
				± 1	± 2.5	%
Error Amplifier Source and Sink Current	Source ($V_{FB} = 2\text{V}$)			140		μA
	Sink ($V_{FB} = 2.5\text{V}$)			800		μA
V_C Voltage at 0% Duty Cycle				1.6		V
	Over Temperature	●		-4		$\text{mV}/^\circ\text{C}$
Multiplier Reference Voltage				20		V
Reference Voltage Line Regulation	$8\text{V} \leq V_{IN} \leq V_{MAX}$ (Note 7)			0.005	0.02	$\%/V$
Switching Frequency Line Regulation	$8\text{V} \leq V_{IN} \leq V_{MAX}$ (Note 7)			0.05		$\%/V$
Shutdown Pin Current	$V_{SH} = 5\text{V}$	●	5	10	20	μA
	$V_{SH} \leq V_{THRESHOLD} (= 2.5\text{V})$	●			50	μA
Shutdown Thresholds	Switch Duty Cycle = 0	●	2.15	2.35	2.55	V
	Fully Shut Down	●	0.2	0.3	0.5	V
Status Window	As a Percent of Feedback Voltage	●	4	± 5	6	%
Status High Level	$I_{STATUS} = 0$	●	3.5	4.0	5.0	V
Status Low Level	$I_{STATUS} = 1.6\text{mA}$	●		0.25	0.4	V
Status Delay Time				9		μs
Status Minimum Width				25		μs
Freq Pin Voltage	$R_{FREQ} = 15\text{k}$			1.7		V
COMOUT Saturation Voltage	$I_{SINK} = 10\text{mA}$			0.7		V
COMOUT Leakage	$V_{COMOUT} = 20\text{V}$	●			1	μA

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: To calculate maximum switch "on" voltage at currents between 1A and 5A, a linear interpolation may be used.

Note 2: A feedback pin voltage (V_{FB}) of 2.5V forces the V_C pin to its low clamp level and the switch duty cycle to zero. This approximates the zero load condition where duty cycle approaches zero.

Note 3: Total voltage from V_{IN} pin to ground pin must be $\geq 8\text{V}$ after startup for proper regulation.

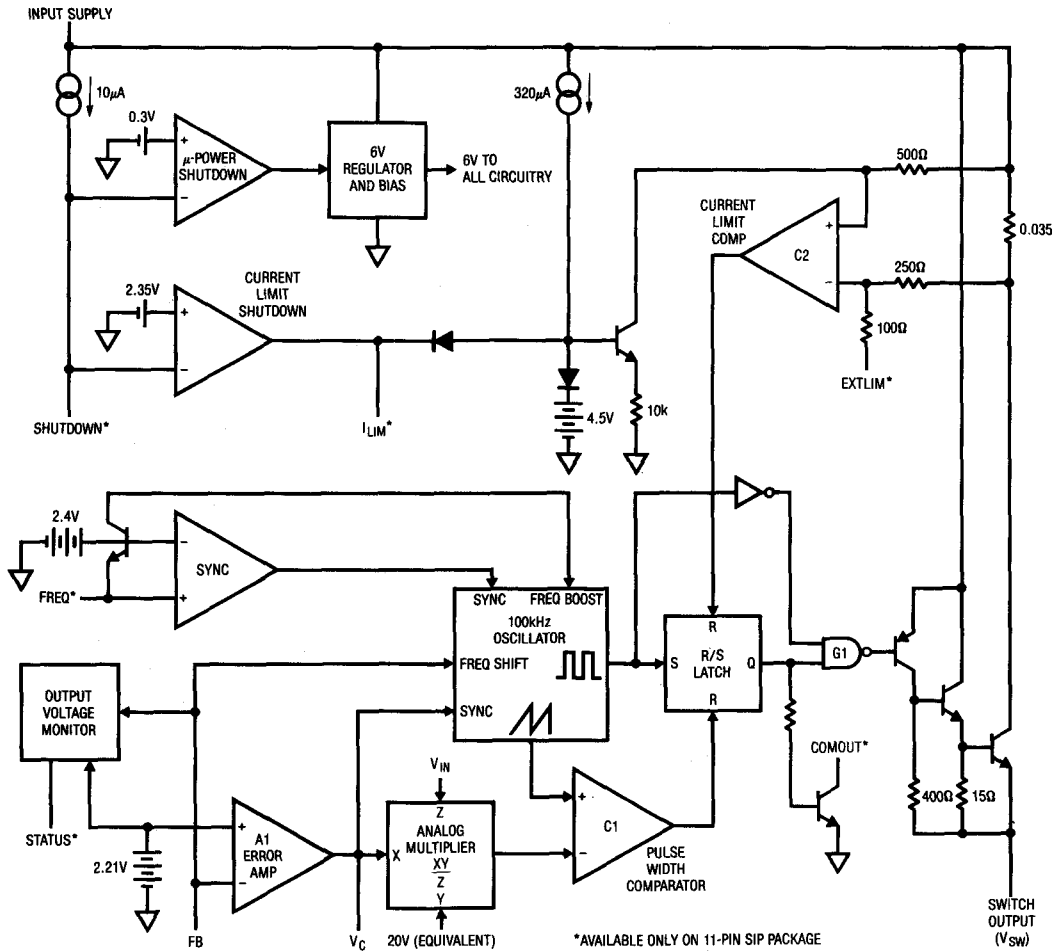
Note 4: Switch frequency is internally scaled down when the feedback pin voltage is less than 0.6V to avoid extremely short switch on times. During testing, V_{FB} is adjusted to give a minimum switch on time of $1\mu\text{s}$.

Note 5: This design center value may change slightly on the final data-sheet.

Note 6: Switch off leakage is measured with $V_{IN} = V_{MAX}$ and $V_{SW} = 0\text{V}$.

Note 7: $V_{MAX} = 40\text{V}$ for the LT1074 and 60V for the LT1074HV.

BLOCK DIAGRAM



BLOCK DIAGRAM DESCRIPTION

A switch cycle in the LT1074 is initiated by the oscillator setting the R/S latch. The pulse that sets the latch also locks out the switch via gate G1. The effective width of this pulse is approximately 700ns, which sets the maximum switch duty cycle to approximately 93% at 100kHz switching frequency. The switch is turned off by comparator C1, which resets the latch. C1 has a sawtooth waveform as one input and the output of an analog multiplier as the other input. The multiplier output is the product of an internal reference voltage, and the output of the error amplifier, A1, divided by the regulator input voltage. In standard buck regulators, this means that the output voltage of A1 required to keep a constant regulated output is independent of regulator input voltage. This greatly improves line transient response, and makes loop gain independent of input voltage. The error amplifier is a transconductance type with a G_M at null of approximately 400 μ mho. Slew current going positive is 140 microamps, while negative slew current is about 800 microamps. This asymmetry helps prevent overshoot on startup. Overall loop frequency compensation is accomplished with a series RC network from V_C to ground.

Switch current is continuously monitored by C2, which resets the R/S latch to turn the switch off if an overcurrent condition occurs. The time required for detection and switch turn off is approximately 600ns, so minimum switch "on" time in current limit is 600ns. Under dead shorted output conditions, switch duty cycle may have to be as low as 2% to maintain control of output current. This would require switch on time of 200ns at 100kHz switching frequency, so frequency is reduced at very low output voltages by feeding the FB signal into the oscillator and creating a linear frequency downshift when the FB signal drops below 1V. Current trip level is set by the voltage on the I_{LM} pin which is driven by an internal 320 microamp current source. When this pin is left open, it self-clamps at about 4.5V and sets current limit at 6.5A. In the 11-pin package an external resistor can be connected from the I_{LM} pin to ground to set a lower current limit. A capacitor in parallel with this resistor will soft-start the current limit. A slight offset in C2 guarantees that when the I_{LM} pin is pulled to within 200mV of ground, C2 output will stay high and force switch duty cycle to zero.

An output voltage monitor is included on the chip. Its output is available only on the 11-pin version. The monitor output goes low when the voltage on the FB pin is more than 5% above or below the normal regulated value. This pin can be used to "hold off" load functions until the regulator output is normal or it can be used as a microprocessor reset.

The "Freq" pin is used to raise switching frequency, and to synchronize the oscillator to an external signal. A resistor to ground will raise frequency. A 3V-5V pulse coupled through a diode will synchronize the internal oscillator from 110% to 160% of its normal frequency. The pulse should be 300ns wide. Synchronizing can also be done with the 5-lead LT1074 by pulling the V_C pin to ground for 300ns with a transistor. This has only a slight effect on regulated output voltage if the series resistor in the frequency compensation network is at least 1k Ω .

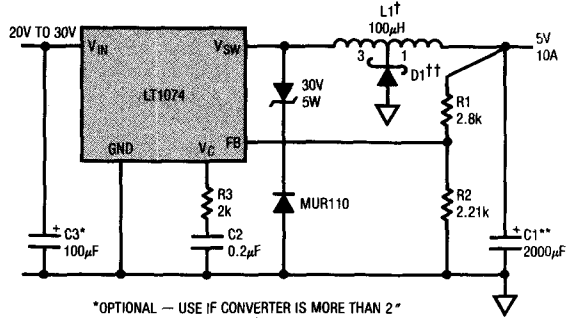
The "Shutdown" pin is used to force switch duty cycle to zero by pulling the I_{LM} pin low, or to completely shut down the regulator. Threshold for the former is approximately 2.35V, and for complete shutdown, approximately 0.3V. Total supply current in shutdown is about 100 microamps. A 10 microamp pull-up current forces the shutdown pin high when left open. A capacitor can be used to generate delayed startup. A resistor divider will program "undervoltage lockout" if the divider voltage is set at 2.35V when the input is at the desired trip point.

The "Comout" pin is an open collector switch whose voltage is the complement of the switch output (V_{SW}). In addition, the falling edge of Comout is slightly time-shifted to avoid overlap with V_{SW} . Comout is used to drive external MOSFETs in certain multiple-output and very high efficiency applications.

The switch used in the LT1074 is a Darlington NPN driven by a saturated PNP. Special patented circuitry is used to drive the PNP on and off very quickly even from the saturation state. This particular switch arrangement has no "isolation tubs" connected to the switch output, which can therefore swing to 40V below ground.

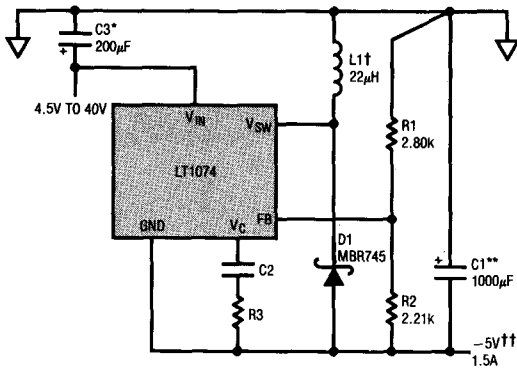
TYPICAL APPLICATIONS

Tapped Inductor Buck Converter



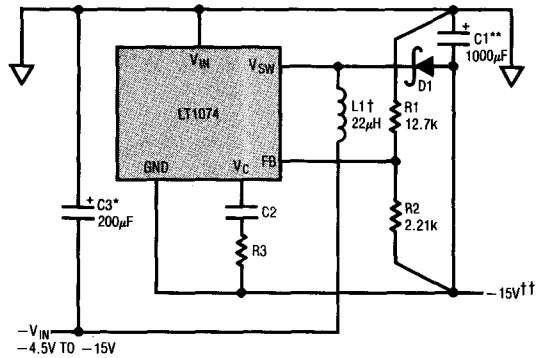
*OPTIONAL — USE IF CONVERTER IS MORE THAN 2" FROM RAW SUPPLY FILTER CAPACITOR
 **TAPPED INDUCTOR TOPOLOGY HAS A SQUARE WAVE COMPONENT OF OUTPUT RIPPLE. A 5µH, 200µF OUTPUT FILTER CAN BE ADDED.
 †TAPPED AT 3:1; PULSE ENGINEERING, INC. #PE-65282
 ††MOTOROLA MBR1N5828

Positive to Negative Converter



*OPTIONAL — USE IF CONVERTER IS MORE THAN 2" FROM RAW SUPPLY FILTER CAPACITOR
 **LOWER OUTPUT RIPPLE CAN BE OBTAINED BY PARALLELING SEVERAL LOWER VALUE CAPACITORS. AN OUTPUT FILTER OF 5µH, 100µF WILL GIVE 20:1 RIPPLE ATTENUATION WITH AN ESR OF 0.1Ω ON THE 100µF CAPACITOR.
 †PULSE ENGINEERING, INC. #PE-51590
 ††MAXIMUM OUTPUT CURRENT IS 1.5A AT VIN=5V, 3A AT VIN=15V, AND 3.5A AT VIN=30V

Negative Boost Converter



*OPTIONAL — USE IF CONVERTER IS MORE THAN 2" FROM RAW SUPPLY FILTER CAPACITOR
 **USE PARALLEL UNITS OF LOWER VALUE FOR LOWER RIPPLE, OR ADD AN OUTPUT FILTER. 5µH AND 100µF WITH ESR=0.1Ω WILL GIVE 20:1 RIPPLE ATTENUATION.
 †PULSE ENGINEERING, INC. #PE-51590
 ††MAXIMUM OUTPUT CURRENT IS 0.8A AT VIN=-5V, 1.7A AT VIN=-8V, AND 2.7A AT VIN=-12V. OUTPUT SHORTS ARE NOT ALLOWED ON A BOOST CONVERTER BECAUSE L1 AND D1 WOULD SHORT THE INPUT SUPPLY.

FEATURES

- 60 μ A Max Supply Current
- 40 μ V Max Offset Voltage
- 350pA Max Offset Current
- 0.5 μ Vp-p 0.1Hz to 10Hz Voltage Noise
- 2.5pAp-p 0.1Hz to 10Hz Current Noise
- 0.4 μ V/ $^{\circ}$ C Offset Voltage Drift
- 250kHz Gain-Bandwidth-Product
- 0.12V/ μ s Slew Rate
- Single Supply Operation
 - Input Voltage Range Includes Ground
 - Output Swings to Ground while Sinking Current
 - No Pull-Down Resistors are Needed
- Output Sources and Sinks 5mA Load Current

APPLICATIONS

- Replaces OP-07, OP-77, AD-77, LT1001, LT1012 at 10 to 60 Times the Power
- Battery or Solar Powered Systems
- 4mA to 20mA Current Loads
- Two Terminal Current Source
- Megaohm Source Resistance Difference Amplifier

DESCRIPTION

The LT1077 is a micropower precision operational amplifier optimized for single supply operation at 5V. \pm 15V specifications are also provided.

Micropower performance of competing devices is achieved at the expense of seriously degrading precision, noise, speed, and output drive specifications. The LT1077 reduces supply current without sacrificing other parameters. The offset voltage achieved is the lowest of any micropower op amp. Offset current, voltage and current noise, slew rate and gain-bandwidth product are all 10 to ten times better than on previous micropower op amps.

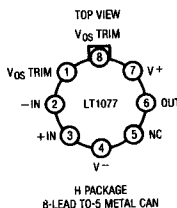
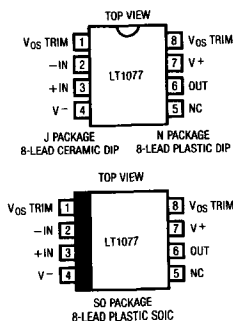
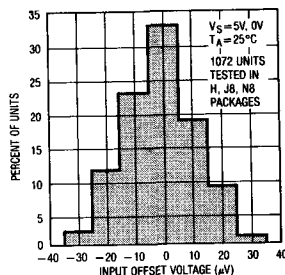
The 1/f corner of the voltage noise spectrum is at 0.7Hz. This results in low frequency (10 to 100Hz) noise performance which can only be found on devices with an order of magnitude higher supply current.

The LT1077 is completely plug-in compatible (including nulling) with all industry standard precision op amps. Thus, it can replace these precision op amps in many applications without sacrificing performance, yet with significant power savings.

The LT1077 can be operated from one lithium cell or two Ni-Cad batteries. The input range goes below ground. The all-NPN output stage swings to ground while sinking current—no pull-down resistors are needed.

For dual and quad op amps with similar specifications please see the LT1078/LT1079 datasheet.

REFER TO TABLE OF CONTENTS FOR REVISED DATA LOCATION

PACKAGE INFORMATION

Distribution of Input Offset Voltage


Adjustable Low Dropout Regulator with Kelvin-Sense Inputs

June 1989

FEATURES

- Five Terminal Adjustable
- Separate Sense Inputs Allow True Kelvin Sensing
- Easily Parallelable
- Operates Down to 1V Dropout
- Guaranteed Dropout Voltage at Multiple Current Levels
- 0.05% Line Regulation
- 0.1% Load Regulation at the Sense Point

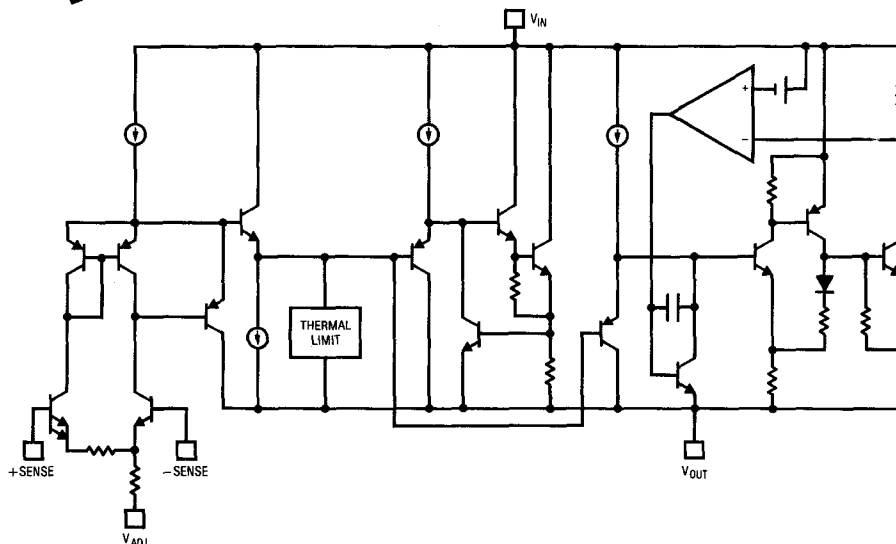
DESCRIPTION

The LT1087 is a variation of the LT1084 Adjustable Low Dropout 3 Terminal Regulator. The sense points of the internal reference/error amp are brought out to allow added flexibility. These sense points can be used in several ways.

They can be used for true Kelvin sensing of the output voltage at a remotely located load. They can be used to force the devices to share current equally when more than one device is wired in parallel, allowing the user to easily build higher current modules. This device is designed to provide 5A of output current. All internal circuitry is designed to operate down to 1V input to output differential and the dropout voltage is fully specified as a function of load current. On-chip trimming adjusts the reference voltage to 1%. Current limit is also trimmed, minimizing the stress on both the regulator and power source circuitry under overload conditions. A $10\mu\text{F}$ output capacitor is required on these devices; however, this is usually included in most regulator designs.

Unlike LNP regulators, where up to 10% of the output current is wasted as quiescent current, the LT1087 quiescent current flows into the load, increasing efficiency.

SIMPLIFIED SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

Power Dissipation Internally Limited

Input to Output Voltage Differential

“M” Grade 35V

“C” Grade 30V

Differential Voltage Between Sense Pins
($V_{+SENSE} - V_{-SENSE}$) 4V

Sense Pin Voltage

Range ($V_{OUT}^* - 1V$) $\leq V_{\pm SENSE} \leq (V_{OUT}^* + 0.4V)$

Operating Junction Temperature Range

“M” Grade

Control Section -55°C to 150°C

Power Transistor -55°C to 200°C

“C” Grade

Control Section 0°C to 125°C

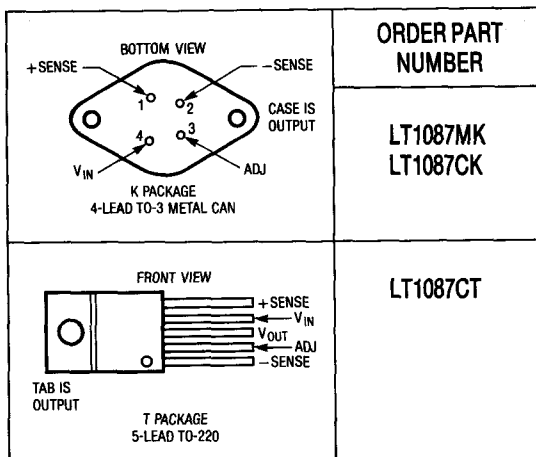
Power Transistor 0°C to 150°C

Storage Temperature -65°C to 150°C

Lead Temperature (Soldering, 10 sec) 300°C

* V_{OUT} is referring to the regulator output pin voltage.

PACKAGE/ORDER INFORMATION



ORDER PART NUMBER

LT1087MK
LT1087CK

LT1087CT

PRECONDITIONING

100% Thermal Limit Burn-In

ELECTRICAL CHARACTERISTICS (See Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Reference Voltage	$I_{OUT} = 10mA, T_j = 25^\circ C,$ $(V_{IN} - V_{OUT}) = 3V$ (K Package Only) $10mA \leq I_{OUT} \leq 5A$ $1.5V \leq (V_{IN} - V_{OUT}) \leq 25V$	1.238	1.250	1.262	V
		1.225	1.250	1.270	V
Line Regulation	$I_{LOAD} = 10mA, 1.5V \leq (V_{IN} - V_{OUT}) \leq 15V, T_j = 25^\circ C$		0.015	0.2	%
			0.035	0.2	%
	M Grade $15V \leq (V_{IN} - V_{OUT}) \leq 35V$		0.05	0.5	%
	C Grade $15V \leq (V_{IN} - V_{OUT}) \leq 30V$ (Notes 1, 2)		0.05	0.5	%
Load Regulation	$(V_{IN} - V_{OUT}) = 3V$ $10mA \leq I_{OUT} \leq 5A$ $T_j = 25^\circ C$ (Notes 1, 2)		0.1	0.3	%
			0.2	0.4	%
Dropout Voltage	$\Delta V_{REF} = 1\%, I_{OUT} = 5A,$ (Note 4)		1.3	1.5	V
Common Mode Range of Sense Pins ΔV_{REF}	$(V_{OUT} - 1V) \leq V_{+SENSE} \leq V_{OUT}$		0.4		mV
Differential Gain of Sense Pins $\Delta V_{REF} / \Delta V_{SENSE}$	$V_{+SENSE} = V_{OUT}$ $V_{-SENSE} = (V_{OUT} - 40mV)$		11		V/V
Sense Pin Bias Current			0.3		μA
Minimum Load Current	$(V_{IN} - V_{OUT}) = 25V$		5	10	mA
Thermal Regulation	$T_A = 25^\circ C, 30ms$ pulse		0.003	0.015	%/W

13

ELECTRICAL CHARACTERISTICS (See Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Ripple Rejection	$f = 120\text{Hz}$ $C_{ADJ} = 25\mu\text{F}$, $C_{OUT} = 25\mu\text{F}$ Tantalum $I_{OUT} = 5\text{A}$, $(V_{IN} - V_{OUT}) = 3\text{V}$	60	75		dB
Adjust Pin Current	$T_j = 25^\circ\text{C}$		55	120	μA
Adjust Pin Current Change	$10\text{mA} \leq I_{OUT} \leq 5\text{A}$ $1.5\text{V} \leq (V_{IN} - V_{OUT}) \leq 25\text{V}$		0.2	5	μA
Temperature Stability			0.5		%
Long Term Stability	$T_A = 125^\circ\text{C}$, 1000 Hrs.		0.3	1	%
RMS Output Noise (% of V_{OUT})	$T_A = 25^\circ\text{C}$ $10\text{Hz} \leq f \leq 10\text{kHz}$		0.003		%
Thermal Resistance Junction to Case	K Package: Control Circuitry/Power Transistor T Package: Control Circuitry/Power Transistor			0.75/2.3 0.65/2.7	$^\circ\text{C/W}$

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: See thermal regulation specifications for changes in output voltage due to heating effects. Load and line regulation are measured at a constant junction temperature by low duty cycle pulse testing. Unless otherwise specified, + Sense, - Sense and V_{OUT} are tied together at the package.

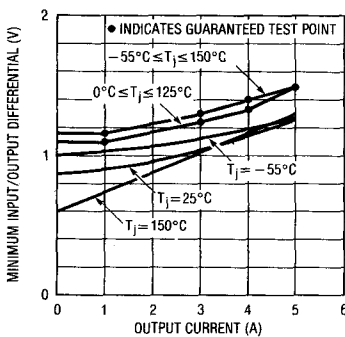
Note 2: Line and load regulation are guaranteed up to the maximum power dissipation (45W for the LT1087K, 30W for the LT1087T). Power dissipation is determined by the input/output differential and the output current. Guaranteed maximum power dissipation will not be available over the full input/output voltage range.

Note 3: Load regulation is defined to be the change in output voltage at the sense point. The sense point is defined to be the point at which the sense pins, output, and the top of the resistive divider that sets the output voltage are tied together. The voltage drop from the output pin of the device to the sense point must be $< 1\text{V}$.

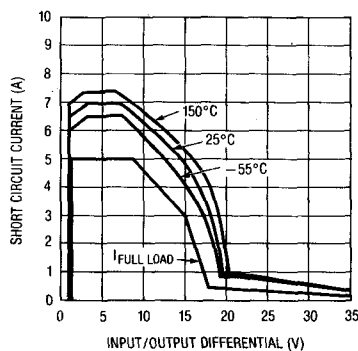
Note 4: Dropout voltage is specified over the full output current range of the device. Test points and limits are shown on the Dropout Voltage curve. Dropout voltage is defined to be the voltage from input to output and is tested with the sense pins tied to the output pin.

TYPICAL PERFORMANCE CHARACTERISTICS

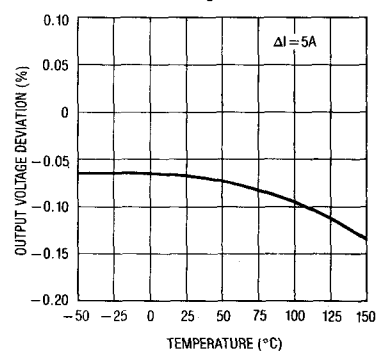
LT1087 Dropout Voltage



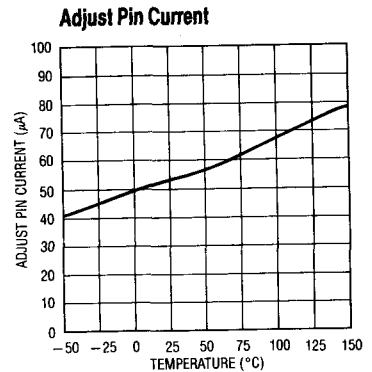
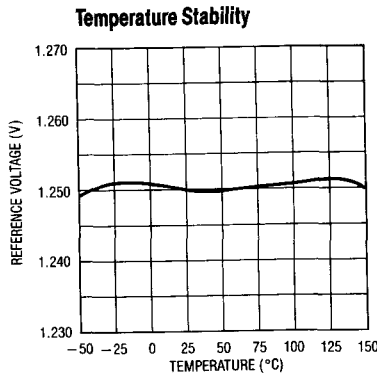
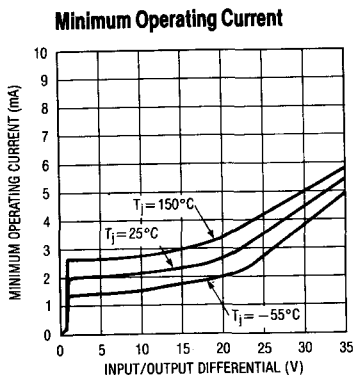
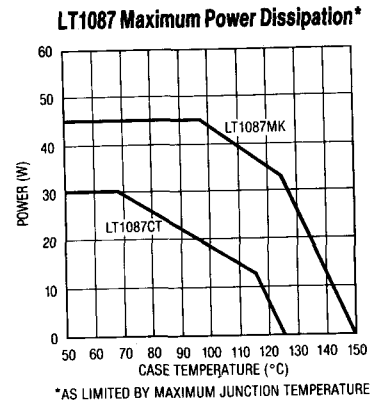
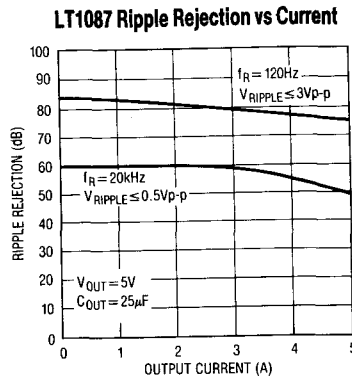
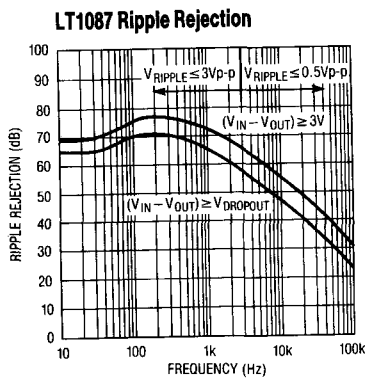
LT1087 Short Circuit Current



LT1087 Load Regulation



TYPICAL PERFORMANCE CHARACTERISTICS



APPLICATION HINTS

The LT1087 is an adjustable voltage regulator with Kelvin sense inputs. These inputs can be used to fully Kelvin sense a remote load so that the regulation at the load is nearly perfect. The sense inputs can also be used in a 2-wire configuration to compensate for voltage drops in long output leads eliminating the two extra wires needed for full Kelvin sensing.

This regulator is easy to use and has all the protection features that are expected in high performance voltage regulators. They are short circuit protected, have safe area

protection as well as thermal shutdown to turn-off the regulator should the temperature exceed about 165°C.

Sense Inputs

In a three terminal regulator the sense inputs are terminated at the output pin of the device (normally the case for adjustable regulators). This means that regulation will be best at the case of the device. Any wire resistance between the regulator and the actual load will degrade the regulation, especially at high currents. This five pin configuration allows the user to select the point where regulation will be optimized.

APPLICATION HINTS

The sense pins can be used in two basic configurations. They can be used to make a remote Kelvin sensed output, or they can be used as a differential amplifier to simply compensate for a long wire run.

For full Kelvin sensing of the output, the sense pins are tied together, then connected through a 1k resistor to the top of the R1/R2 divider that sets the output voltage. The 1k resistor is necessary to prevent high currents from flowing into the sense pins under fault conditions and will cause no significant error in the output voltage. The top and bottom of the R1/R2 divider are then tied to the points in the circuit where optimum regulation is desired. These connections must be made separate from the wires that carry the main load current. See the Remote Kelvin Sensed Output Circuit in the Typical Applications Section. At light load currents the voltage drop down the output lead will be small and the sense pins will be at approximately the same voltage as the output pin. For heavy load currents the output pin will be driven positive with respect to the sense pins by the value of the voltage drop across the output leads and the voltage at the sense points will be regulated. The output is allowed to go 1V above the sense pins in this configuration. For output pin voltages greater than 1V above the sense pins some degradation in regulation will occur. Since the output is allowed to go positive with respect to the sense pins by 1V and assuming that both the power lead to the load and the ground return are approximately equal, this configuration allows the user to have almost perfect regulation at the sense point with 2V of drop in the wire leads between the regulator and the load. Note that the input voltage to the regulator must provide enough headroom to the regulator to allow this to happen. The input voltage must be greater than the total of the regulated output voltage plus the wire drops plus the dropout voltage of the regulator ($\approx 1.5V$ for LT1087 at 5A).

If the user does not want to run the extra two wires required for full Kelvin sensing, a second method can be used to compensate for wire drops. The sense inputs can be considered to be the inputs to a differential amplifier

with a gain of 11 when the + Sense pin is positive with respect to the - Sense pin. Pulling the - Sense pin negative with respect to the + Sense pin (with the + Sense pin tied to the output) by 10mV will cause the reference voltage, nominally 1.25V, to increase by 110mV to 1.36V. The output of the regulator would then increase by the factor

$$\left[\Delta V_{REF} \left(1 + \frac{R2}{R1} \right) \right].$$

See the Remote Load Regulation Compensation Circuit in the Typical Applications. In this manner sensing across a small part of the output leads can compensate for the entire length. The maximum differential input voltage over which the differential gain holds true is 60mV at 25°C, and this voltage is proportional to absolute temperature. For most circuits the differential input voltage should be less than 40mV. Exceeding this small differential voltage will not damage the device until the differential exceeds 5V. Regulation, however, will be degraded. Assuming a maximum differential input voltage of 40mV and an output voltage of 5V, and using the formula from the Remote Load Regulation Compensation Circuit, this configuration can compensate out 1.76V of wire drop. For higher output voltages larger wire drops can be compensated out. As in the previous circuit the input voltage to the regulator must provide enough headroom for this to happen.

Output Voltage

The LT1087 develops and tries to maintain a 1.25V reference voltage between its sense pins and its adjust pin (see Figure 1). By placing a resistor between the device's sense point (the end of R3) and its adjust pin, a constant current is caused to flow through R1 and down through R2 to set the overall output voltage. Normally R1 is chosen so that the current flowing through it is equal to the specified minimum load current of 10mA. Because I_{ADJ} is very small and constant when compared with the current through R1, it represents a small error and can usually be ignored.

APPLICATION HINTS

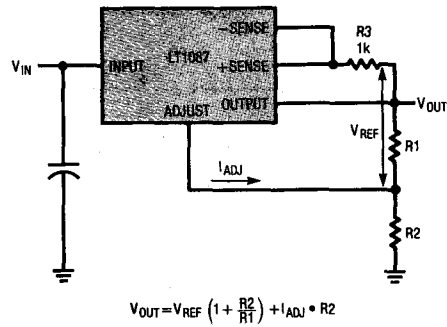
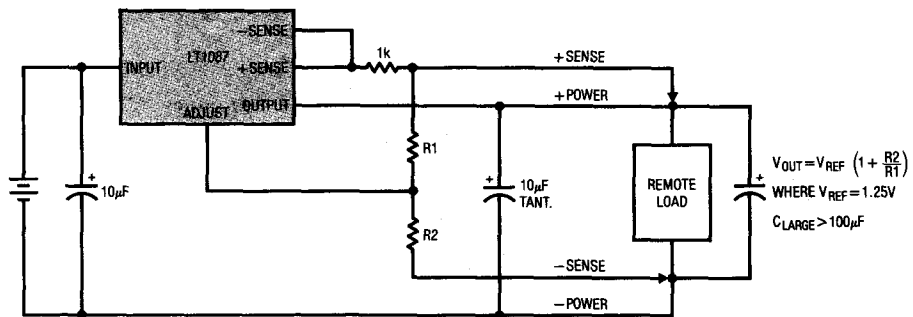


Figure 1. Standard Connection

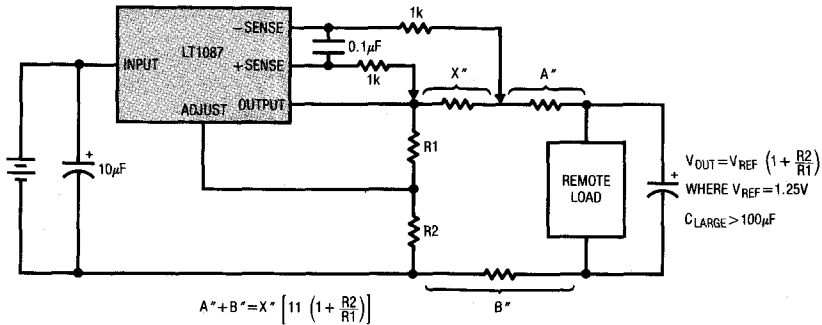
TYPICAL APPLICATIONS

Remote Kelvin Sensed Output (4-Wire)



TYPICAL APPLICATIONS

Remote Load Regulation Compensation (2-Wire)

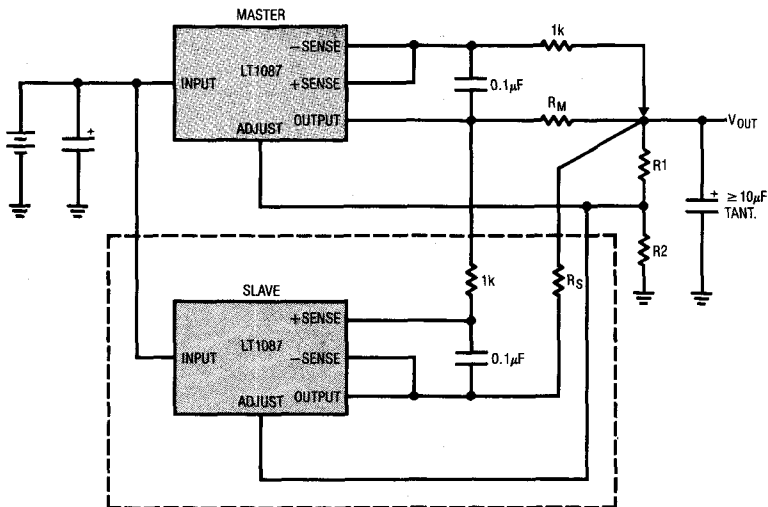


EXAMPLE: IF THE LOAD MUST BE LOCATED 10 FT. (120") FROM THE REGULATOR AND V_{OUT} IS 5V THEN $(A'' + B'') = 24.0''$ $R_1 = 120\Omega$, $R_2 = 360\Omega$

$$X'' = \frac{(A'' + B'')}{\left[11 \left(1 + \frac{R_2}{R_1} \right) \right]} \rightarrow X'' = 5.2''$$

BY CONNECTING THE - SENSE PIN 5.2" FURTHER DOWN THE OUTPUT WIRE THAN THE + SENSE PIN THE LOAD REGULATION CAUSED BY 20" OF WIRE CAN BE COMPENSATED OUT.

Paralleling Devices for Higher Current



FOR PARALLELING MORE THAN TWO DEVICES — DUPLICATE SLAVE SECTION

MINIMUM LOAD CURRENT = (10mA) (# OF DEVICES IN PARALLEL)
 R1, R2 NETWORK CAN BE USED AS THE MINIMUM LOAD

$R_M = 8m\Omega = 10''$ OF #20 A.W.G. SOLID WIRE (COPPER)
 $R_S = 7.3m\Omega = 9.1''$ OF #20 A.W.G. SOLID WIRE (COPPER)

R_M AND R_S SHOULD BE NON-INDUCTIVE. THIS IS EASILY ACCOMPLISHED BY FOLDING THE WIRE BACK UPON ITSELF SO THAT THE FIELDS GENERATED, BY CURRENT FLOWING IN THE WIRE, CANCEL.

Precision, Single Supply,
 Instrumentation Amplifier
 (Fixed Gain = 100)

June 1989

FEATURES

- Offset Voltage $2\mu\text{V}$
- Offset Voltage Drift $20\text{nV}/^\circ\text{C}$
- Bias Current 25pA
- Offset Current 10pA
- Gain Non-Linearity 8ppm
- Gain Error 0.03%
- CMRR 110dB
- $0.1\text{Hz}-10\text{Hz}$ Noise $2\mu\text{Vp-p}$
- Single 5V Supply Operation
- 8-Pin MiniDIP

APPLICATIONS

- Strain Gauge Amplifier
- Thermocouple Amplifier
- Differential to Single Ended Converter

DESCRIPTION

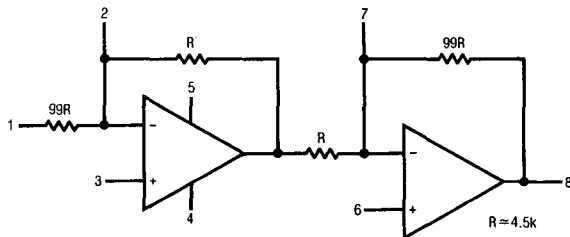
The LTC1100 is a high precision instrumentation amplifier using chopper stabilization techniques to achieve outstanding DC performance. The input DC offset is typically $2\mu\text{V}$ while the DC offset drift is $20\text{nV}/^\circ\text{C}$; a very low bias current of 25pA is also achieved.

The LTC1100 is self contained, that is, it achieves a differential gain of 100 without an external gain setting resistor or trim pot. Its gain linearity is 8ppm and the gain drift is $1\text{ppm}/^\circ\text{C}$. The LTC1100 operates from a single 5V supply up to $\pm 8\text{V}$. The output signal typically swings 150mV from its power supply rails.

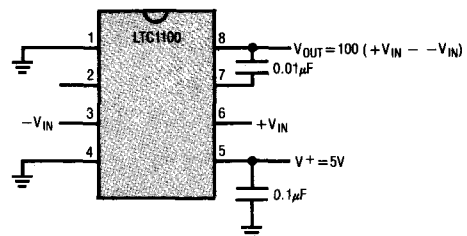
An optional external capacitor can be added from pin 7 to pin 8 to tailor the device's 20kHz bandwidth and to eliminate any unwanted noise pickup.

The LTC1100 is manufactured using Linear Technology's enhanced LTCMOSTM silicon gate process.

 REFER TO TABLE OF CONTENTS
 FOR REVISED DATA LOCATION

BLOCK DIAGRAM

TYPICAL APPLICATION

Single 5V Supply, DC Instrumentation Amplifier



Precision, Micropower, Single Supply Instrumentation Amplifier (Fixed Gain =10 or 100)

April 1989

FEATURES

- Gain Error 0.04% Max
- Gain Non-Linearity 0.0008% (8ppm) Max
- Gain Drift 4ppm/°C Max
- Supply Current 105µA Max
- Offset Voltage 160µV Max
- Offset Voltage Drift 0.4µV/°C Typ
- Offset Current 600pA Max
- CMRR, G = 100 100dB Min
- 0.1Hz to 10Hz Noise 0.9µVp-p Typ
2.3pAp-p Typ
250kHz Min
- Gain Bandwidth Product
- Single or Dual Supply Operation

APPLICATIONS

- Differential Signal Amplification in Presence of Common-Mode Voltage
- Micropower Bridge or Sensor Amplifier
 - Thermistors
 - Strain Gauges
 - Thermistors
- Differential Voltage to Current Converter
- Transformer Coupled Amplifier
- 4mA-20mA Bridge Transmitter

DESCRIPTION

The LT1101 establishes the following milestones:

- (1) It is the first micropower instrumentation amplifier,
- (2) It is the first single supply instrumentation amplifier,
- (3) It is the first instrumentation amplifier to feature fixed gains of 10 and/or 100 in low cost, space-saving 8-lead packages.

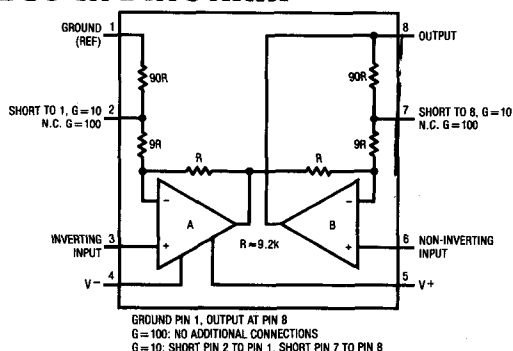
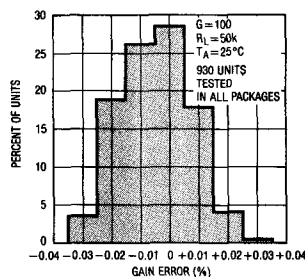
The LT1101 is completely self-contained: no external gain setting resistor is required. The LT1101 combines its micropower operation (75µA supply current) with a gain error of 0.008%, gain linearity of 3ppm, gain drift of 1ppm/°C. The output is guaranteed to drive a 2k load to ±10V with excellent gain accuracy.

Other precision specifications are also outstanding: 50µV input offset voltage, 10pA input offset current, and low drift (0.4µV/°C and 0.7pA/°C). In addition, unlike other instrumentation amplifiers, there is no output offset voltage contribution to total error.

A full set of specifications are provided with ±15V dual supplies and for single 5V supply operation. The LT1101 can be operated from a single lithium cell or two Ni-Cad batteries. Battery voltage can drop as low as 1.8V, yet the LT1101 still maintains its gain accuracy. In single supply applications, both input and output voltages swing to within a few millivolts of ground. The output sinks current while swinging to ground — no external, power consuming pull down resistors are needed.

 REFER TO TABLE OF CONTENTS
 FOR REVISED DATA LOCATION

BLOCK DIAGRAM


Gain Error Distribution


ABSOLUTE MAXIMUM RATINGS

- Supply Voltage $\pm 22V$
- Differential Input Voltage $\pm 36V$
- Input Voltage Equal to Positive Supply Voltage
..... 10V Below Negative Supply Voltage
- Output Short Circuit Duration Indefinite
- Operating Temperature Range
LT1101AM/LT1101M -55°C to 125°C
LT1101Ai/LT1101I -40°C to 85°C
LT1101AC/LT1101C 0°C to 70°C
- Storage Temperature Range
All Grades -65°C to 150°C
- Lead Temperature (Soldering, 10 sec.) 300°C

PACKAGE/ORDER INFORMATION

<p>TOP VIEW H PACKAGE 8-LEAD TO-5 METAL CAN</p>	<p>ORDER PART NUMBER</p> <p>LT1101AMH LT1101MH LT1101ACH LT1101CH</p>
	<p>TOP VIEW N PACKAGE 8-LEAD PLASTIC DIP J PACKAGE 8-LEAD CERAMIC DIP</p>

ELECTRICAL CHARACTERISTICS

$V_S = 5V, 0V, V_{CM} = 0.1V, V_{REF(PIN 1)} = 0.1V, G = 10$ or $100, T_A = 25^\circ C$, unless otherwise noted (Note 3).

SYMBOL	PARAMETER	CONDITIONS	LT1101AM/AI/AC			LT1101M/I/C			UNITS	
			MIN	TYP	MAX	MIN	TYP	MAX		
G_E	Gain Error	$G = 100, V_O = 0.1V$ to $3.5V, R_L = 50k$ $G = 10, V_O = 0.1V$ to $3.5V, R_L = 50k$	0.010	0.050		0.011	0.075		%	
G_{NL}	Gain Non-Linearity	$G = 100, R_L = 50k$ $G = 10, R_L = 50k$ (Note 1)	20 3	60 7		20 3	75 8		ppm ppm	
V_{OS}	Input Offset Voltage		50	160		60	220		μV	
I_{OS}	Input Offset Current		0.13	0.60		0.15	0.90		nA	
I_B	Input Bias Current		6	8		6	10		nA	
I_S	Supply Current		75	105		78	120		μA	
CMRR	Common-Mode Rejection Ratio	1k Source Imbalance $G = 100, V_{CM} = 0.07V$ to $3.4V$ $G = 10, V_{CM} = 0.07V$ to $3.1V$	95 84	106 100		92 82	105 99		dB dB	
	Minimum Supply Voltage	(Note 4)	1.8	2.3		1.8	2.3		V	
V_O	Maximum Output Voltage Swing	Output High, 50k to GND	4.1	4.3		4.1	4.3		V	
		Output High, 2k to GND	3.5	3.9		3.5	3.9		V	
		Output Low, $V_{REF} = 0$, No Load		3.3	6		3.3	6		mV
		Output Low, $V_{REF} = 0$, 2k to GND		0.5	1		0.5	1		mV
		Output Low, $V_{REF} = 0, I_{SINK} = 100\mu A$		90	130		90	130		mV
BW	Bandwidth	$G = 100$ (Note 1)	2.0	3.0		2.0	3.0		kHz	
		$G = 10$ (Note 1)	22	33		22	33		kHz	
SR	Slew Rate	(Note 1)	0.04	0.07		0.04	0.07		$V/\mu s$	

ELECTRICAL CHARACTERISTICS

$V_S = \pm 15V$, $V_{CM} = 0V$, $T_A = 25^\circ C$, Gain = 10 or 100, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1101AM/AI/AC			LT1101M/I/C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
G_E	Gain Error	$G = 100$, $V_O = \pm 10V$, $R_L = 50k$		0.008	0.040		0.009	0.060	%
		$G = 100$, $V_O = \pm 10V$, $R_L = 2k$		0.011	0.055		0.012	0.070	%
		$G = 10$, $V_O = \pm 10V$, $R_L = 50k$ or $2k$		0.008	0.040		0.009	0.060	%
G_{NL}	Gain Non-Linearity	$G = 100$, $R_L = 50k$		7	16		8	20	ppm
		$G = 100$, $R_L = 2k$		24	45		25	60	ppm
		$G = 10$, $R_L = 50k$ or $2k$		3	8		3	9	ppm
V_{OS}	Input Offset Voltage			50	160		60	220	μV
I_{OS}	Input Offset Current			0.13	0.60		0.15	0.90	nA
I_B	Input Bias Current			6	8		6	10	nA
	Input Resistance Common-Mode Differential Mode	(Note 1) (Note 1)	4 7	7 12		3 5	7 12		G Ω G Ω
e_n	Input Noise Voltage	0.1Hz to 10Hz (Note 2)		0.9	1.8		0.9		μV_{p-p}
	Input Noise Voltage Density	$f_o = 10Hz$ (Note 2) $f_o = 1000Hz$ (Note 2)		45 43	64 54		45 43		nV/ \sqrt{Hz} nV/ \sqrt{Hz}
i_n	Input Noise Current	0.1Hz to 10Hz (Note 2)		2.3	4.0		2.3		pA $\cdot p$
	Input Noise Current Density	$f_o = 10Hz$ (Note 2) $f_o = 1000Hz$		0.06 0.02	0.10		0.06 0.02		pA/ \sqrt{Hz} pA/ \sqrt{Hz}
	Input Voltage Range	$G = 100$	+13.0	+13.8		+13.0	+13.8		V
			-14.4	-14.7		-14.4	-14.7		V
		$G = 10$	+11.5	+12.5		+11.5	+12.5		V
			-13.0	-13.3		-13.0	-13.3		V
CMRR	Common-Mode Rejection Ratio	1k Source Imbalance							
		$G = 100$, Over CM Range $G = 10$, Over CM Range	100 84	112 100		98 82	112 99		dB dB
PSRR	Power Supply Rejection Ratio	$V_S = +2.2V$, $-0.1V$ to $\pm 18V$	102	114		100	114		dB
I_S	Supply Current			92	130		94	150	μA
V_O	Maximum Output Voltage Swing	$R_L = 50k$ $R_L = 2k$	± 13.0	± 14.2		± 13.0	± 14.2		V
			± 11.0	± 13.2		± 11.0	± 13.2		V
BW	Bandwidth	$G = 100$ (Note 1) $G = 10$ (Note 1)	2.3	3.5		2.3	3.5		kHz
			25	37		25	37		kHz
SR	Slew Rate		0.06	0.10		0.06	0.10		V/ μs

Note 1: This parameter is not tested. It is guaranteed by design and by inference from other tests.

Note 2: This parameter is tested on a sample basis only.

Note 3: These test conditions are equivalent to $V_S = 4.9V$, $-0.1V$, $V_{CM} = 0V$, $V_{REF(PIN 1)} = 0V$.

Note 4: Minimum supply voltage is guaranteed by the power supply rejection test. The LT1101 actually works at 1.8V supply with minimal degradation in performance.

ELECTRICAL CHARACTERISTICS

$V_S = \pm 15V$, $V_{CM} = 0V$, Gain = 10 or 100, $-55^\circ C \leq T_A \leq 125^\circ C$ for AM/M grades, $-40^\circ C \leq T_A \leq 85^\circ C$ for AI/I grades, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1101AM/AI			LT1101MI			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
G_E	Gain Error	$G = 100, V_O = \pm 10V, R_L = 50k$		0.024	0.070		0.026	0.100	%
		$G = 100, V_O = \pm 10V, R_L = 5k$		0.030	0.100		0.035	0.130	%
		$G = 10, V_O = \pm 10V, R_L = 50k \text{ or } 5k$		0.015	0.070		0.018	0.100	%
TCG_E	Gain Error Drift (Note 1)	$G = 100, R_L = 50k$		2	4		2	5	ppm/ $^\circ C$
		$G = 100, R_L = 5k$		2	7		2	8	ppm/ $^\circ C$
		$G = 10, R_L = 50k \text{ or } 5k$		1	4		1	5	ppm/ $^\circ C$
G_{NL}	Gain Non-Linearity	$G = 100, R_L = 50k$		24	70		26	90	ppm
		$G = 100, R_L = 5k$		70	300		75	500	ppm
		$G = 10, R_L = 50k$		4	13		5	15	ppm
		$G = 10, R_L = 5k$		10	40		12	60	ppm
V_{OS}	Input Offset Voltage		90	350		110	500	μV	
$\Delta V_{OS}/\Delta T$	Input Offset Voltage Drift	(Note 1)		0.4	2.0		0.5	2.8	$\mu V/^\circ C$
I_{OS}	Input Offset Current			0.16	0.80		0.19	1.30	nA
$\Delta I_{OS}/\Delta T$	Input Offset Current Drift	(Note 1)		0.5	4.0		0.8	7.0	pA/ $^\circ C$
I_B	Input Bias Current			7	10		7	12	nA
$\Delta I_B/\Delta T$	Input Bias Current Drift	(Note 1)		10	25		10	30	pA/ $^\circ C$
CMRR	Common-Mode Rejection Ratio	$G = 100, V_{CM} = -14.4V \text{ to } 13V$	96	111		94	111		dB
		$G = 10, V_{CM} = -13V \text{ to } 11.5V$	80	99		78	98		dB
PSRR	Power Supply Rejection Ratio	$V_S = +3.0, -0.1V \text{ to } \pm 18V$	98	110		94	110		dB
I_S	Supply Current			105	165		108	190	μA
V_O	Maximum Output Voltage Swing	$R_L = 50k$	± 12.5	± 14.0		± 12.5	± 14.0		V
		$R_L = 5k$	± 11.0	± 13.5		± 11.0	± 13.5		V

ELECTRICAL CHARACTERISTICS

$V_S = \pm 15V$, $V_{CM} = 0V$, Gain = 10 or 100, $0^\circ C \leq T_A \leq 70^\circ C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1101AC			LT1101C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
G_E	Gain Error	$G = 100, V_O = \pm 10V, R_L = 50k$		0.012	0.055		0.014	0.080	%
		$G = 100, V_O = \pm 10V, R_L = 2k$		0.018	0.085		0.020	0.100	%
		$G = 10, V_O = \pm 10V, R_L = 50k \text{ or } 2k$		0.009	0.055		0.010	0.080	%
TCG_E	Gain Error Drift (Note 1)	$G = 100, R_L = 50k$		1	4		1	5	ppm/ $^\circ C$
		$G = 100, R_L = 2k$		2	7		2	9	ppm/ $^\circ C$
		$G = 10, R_L = 50k \text{ or } 2k$		1	4		1	5	ppm/ $^\circ C$
G_{NL}	Gain Non-Linearity	$G = 100, R_L = 50k$		9	25		10	35	ppm
		$G = 100, R_L = 2k$		33	75		36	100	ppm
		$G = 10, R_L = 50k \text{ or } 2k$		4	10		4	11	ppm
V_{OS}	Input Offset Voltage		70	250		85	350	μV	
$\Delta V_{OS}/\Delta T$	Input Offset Voltage Drift	(Note 1)		0.4	2.0		0.5	2.8	$\mu V/^\circ C$
I_{OS}	Input Offset Current			0.14	0.70		0.17	1.10	nA
$\Delta I_{OS}/\Delta T$	Input Offset Current Drift	(Note 1)		0.5	4.0		0.8	7.0	pA/ $^\circ C$
I_B	Input Bias Current			6	9		6	11	nA
$\Delta I_B/\Delta T$	Input Bias Current Drift	(Note 1)		10	25		10	30	pA/ $^\circ C$
CMRR	Common-Mode Rejection Ratio	$G = 100, V_{CM} = -14.4V \text{ to } 13V$	98	112		96	112		dB
		$G = 10, V_{CM} = -13V \text{ to } 11.5V$	82	100		80	99		dB
PSRR	Power Supply Rejection Ratio	$V_S = 2.5, -0.1V \text{ to } \pm 18V$	100	112		97	112		dB
I_S	Supply Current			98	148		100	170	μA
V_O	Maximum Output Voltage Swing	$R_L = 50k$	± 12.5	± 14.1		± 12.5	± 14.1		V
		$R_L = 2k$	± 10.5	± 13.0		± 10.5	± 13.0		V

ELECTRICAL CHARACTERISTICS

$V_S = 5V, 0V, V_{CM} = 0.1V, V_{REF(PIN 1)} = 0.1V, \text{Gain} = 10 \text{ or } 100, -55^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$ for AM/M grades, $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$ for All grades, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1101AM/Al			LT1101M/I			UNITS	
			MIN	TYP	MAX	MIN	TYP	MAX		
G_E	Gain Error	$G = 100, V_O = 0.1V \text{ to } 3.5V, R_L = 50k$ $G = 10, V_{CM} = 0.15V, R_L = 50k$		0.026	0.080		0.028	0.120	%	
				0.011	0.070		0.014	0.100	%	
TCG_E	Gain Error Drift	$R_L = 50k$ (Note 1)	1	4		1	5	ppm/°C		
G_{NL}	Gain Non-Linearity	$G = 100, R_L = 50k$ $G = 10, R_L = 50k$ (Note 1)		45	110		48	140	ppm	
				4	13		5	15	ppm	
V_{OS}	Input Offset Voltage		90	350		110	500	μV		
$\Delta V_{OS}/\Delta T$	Input Offset Voltage Drift	(Note 1)	0.4	2.0		0.5	2.8	$\mu V/^\circ\text{C}$		
I_{OS}	Input Offset Current		0.16	0.80		0.19	1.30	nA		
$\Delta I_{OS}/\Delta T$	Input Offset Current Drift	(Note 1)	0.5	4.0		0.8	7.0	pA/°C		
I_B	Input Bias Current		7	10		7	12	nA		
$\Delta I_B/\Delta T$	Input Bias Current Drift	(Note 1)	10	25		10	30	pA/°C		
CMRR	Common-Mode Rejection Ratio	$G = 100, V_{CM} = 0.1V \text{ to } 3.2V$ $G = 10, V_{CM} = 0.1V \text{ to } 2.9V, V_{REF} = 0.15V$	91	105		88	104		dB	
			80	98		77	97		dB	
I_S	Supply Current		88	135		92	160	μA		
V_O	Maximum Output Voltage Swing	Output High, 50k to GND Output High, 2k to GND Output Low, $V_{REF} = 0$, No Load Output Low, $V_{REF} = 0$, 2k to GND Output Low, $V_{REF} = 0$, $I_{SINK} = 100\mu A$	3.8	4.1		3.8	4.1		V	
			3.0	3.7		3.0	3.7		V	
				4.5	8		4.5	8		mV
				0.7	1.5		0.7	1.5		mV
				125	170		125	170		mV

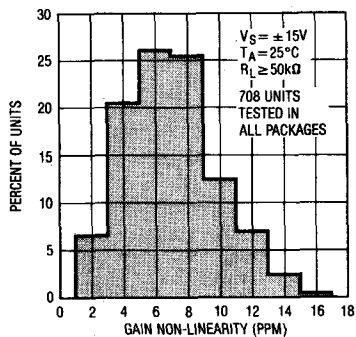
ELECTRICAL CHARACTERISTICS

$V_S = 5V, 0V, V_{CM} = 0.1V, V_{REF(PIN 1)} = 0.1V, \text{Gain} = 10 \text{ or } 100, 0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$, unless otherwise noted.

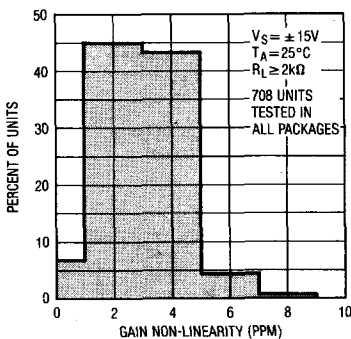
SYMBOL	PARAMETER	CONDITIONS	LT1101AC			LT1101C			UNITS	
			MIN	TYP	MAX	MIN	TYP	MAX		
G_E	Gain Error	$G = 100, V_O = 0.1V \text{ to } 3.5V, R_L = 50k$ $G = 10, V_{CM} = 0.15V, R_L = 50k$		0.017	0.065		0.018	0.095	%	
				0.010	0.060		0.012	0.080	%	
TCG_E	Gain Error Drift	$R_L = 50k$ (Note 1)	1	4		1	5	ppm/°C		
G_{NL}	Gain Non-Linearity	$G = 100, R_L = 50k$ $G = 10, R_L = 50k$ (Note 1)		25	80		25	100	ppm	
				4	10		4	11	ppm	
V_{OS}	Input Offset Voltage		70	250		85	350	μV		
$\Delta V_{OS}/\Delta T$	Input Offset Voltage Drift	(Note 1)	0.4	2.0		0.5	2.8	$\mu V/^\circ\text{C}$		
I_{OS}	Input Offset Current		0.14	0.70		0.17	1.10	nA		
$\Delta I_{OS}/\Delta T$	Input Offset Current Drift	(Note 1)	0.5	4.0		0.8	7.0	pA/°C		
I_B	Input Bias Current		6	9		6	11	nA		
$\Delta I_B/\Delta T$	Input Bias Current Drift	(Note 1)	10	25		10	30	pA/°C		
CMRR	Common-Mode Rejection Ratio	$G = 100, V_{CM} = 0.07V \text{ to } 3.3V$ $G = 10, V_{CM} = 0.07V \text{ to } 3.0V, V_{REF} = 0.15V$	93	105		90	104		dB	
			82	99		80	98		dB	
I_S	Supply Current		80	120		85	145	μA		
V_O	Maximum Output Voltage Swing	Output High, 50k to GND Output High, 2k to GND Output Low, $V_{REF} = 0$, No Load Output Low, $V_{REF} = 0$, 2k to GND Output Low, $V_{REF} = 0$, $I_{SINK} = 100\mu A$	4.0	4.2		4.0	4.2		V	
			3.3	3.8		3.3	3.8		V	
				4	7		4	7		mV
				0.6	1.2		0.6	1.2		mV
				100	150		100	150		mV

TYPICAL PERFORMANCE CHARACTERISTICS

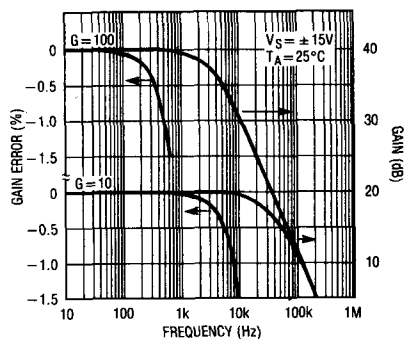
Gain = 100 Non-Linearity Distribution



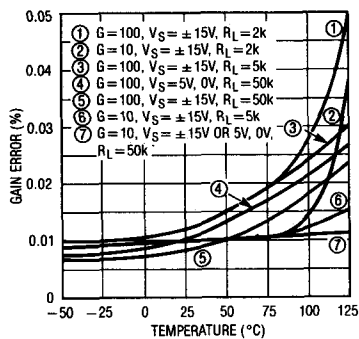
Gain = 10 Non-Linearity Distribution



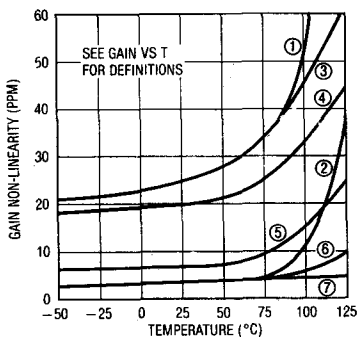
Gain vs Frequency



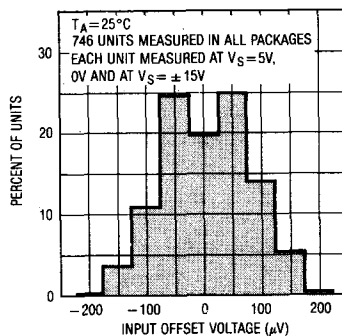
Gain Error Over Temperature



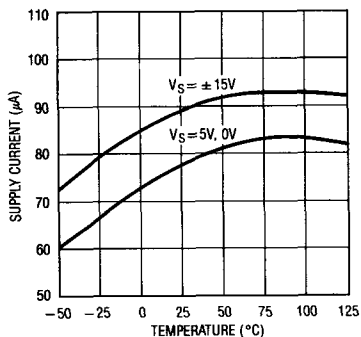
Gain Non-Linearity Over Temperature



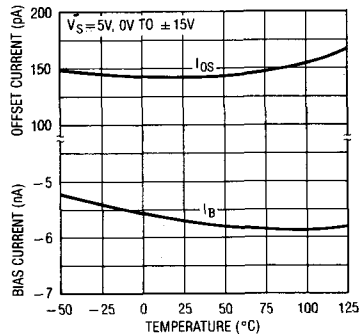
Input Offset Voltage Distribution



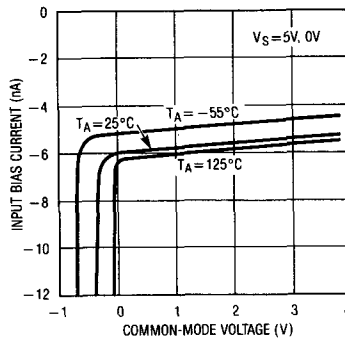
Supply Current vs Temperature



Input Bias and Offset Currents vs Temperature

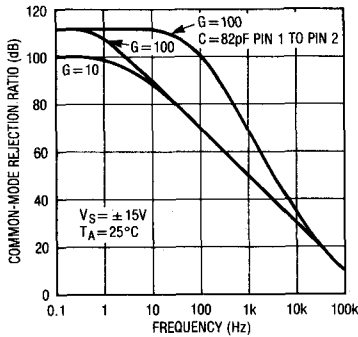


Input Bias Current vs Common-Mode Voltage

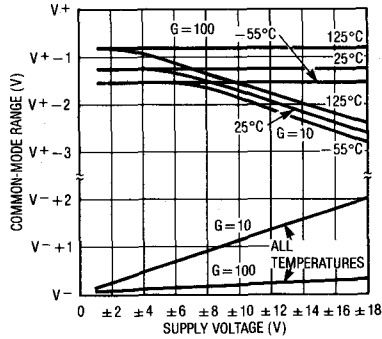


TYPICAL PERFORMANCE CHARACTERISTICS

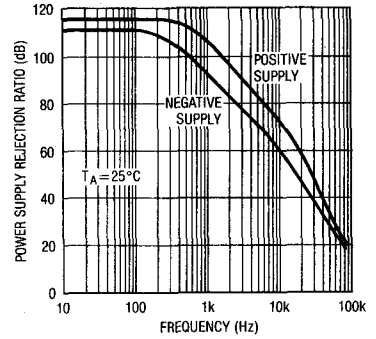
Common-Mode Rejection Ratio vs Frequency



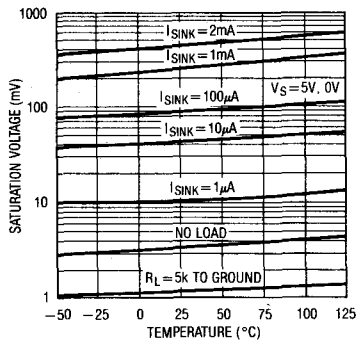
Common-Mode Range vs Supply Voltage



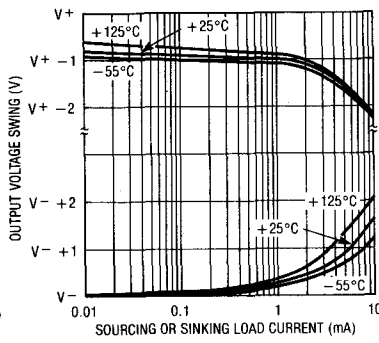
Power Supply Rejection Ratio vs Frequency



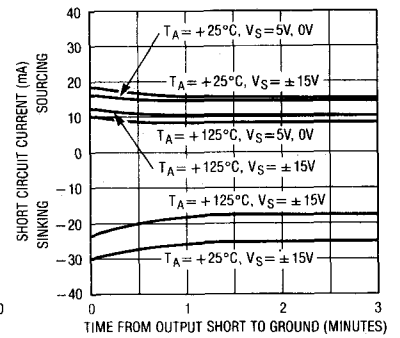
Output Saturation vs Temperature vs Sink Current



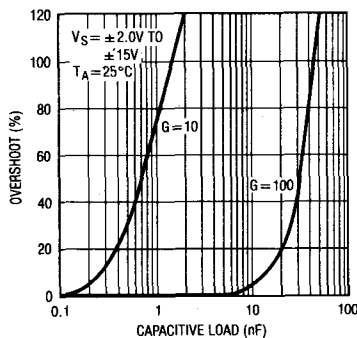
Output Voltage Swing vs Load Current



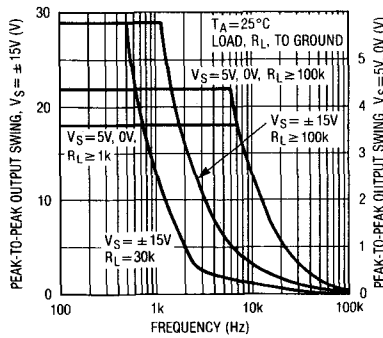
Short Circuit Current vs Time



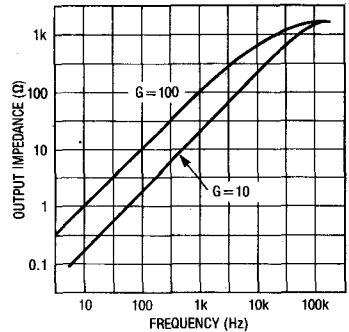
Capacitive Load Handling



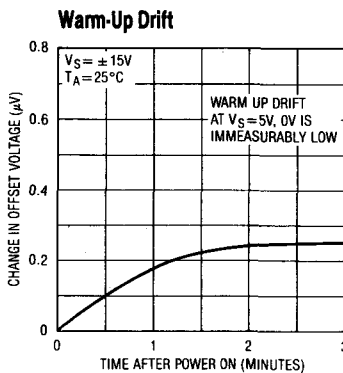
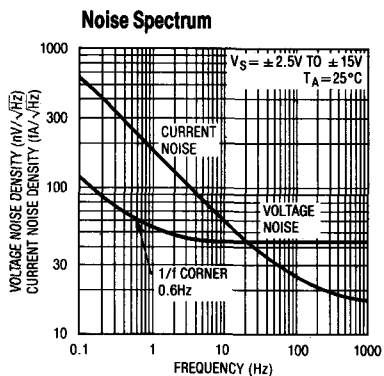
Undistorted Output Swing vs Frequency



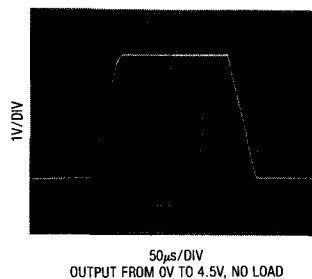
Output Impedance vs Frequency



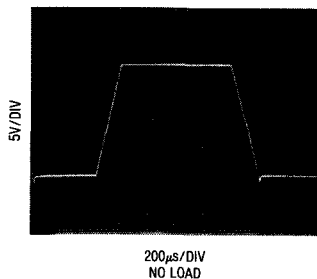
TYPICAL PERFORMANCE CHARACTERISTICS



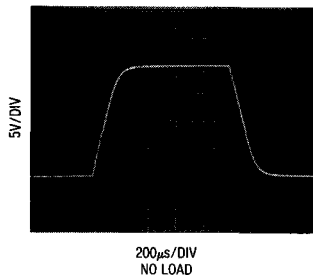
Large Signal Transient Response
 $G = 10, V_S = 5V, 0V$



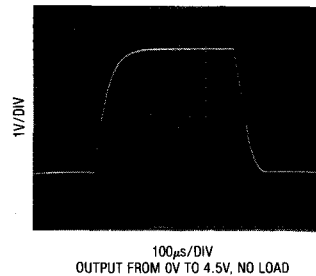
Large Signal Transient Response
 $G = 10, V_S = \pm 15V$



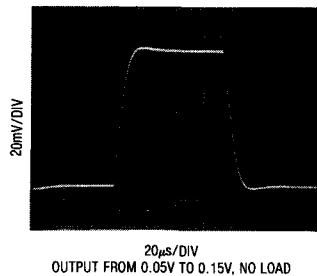
Large Signal Transient Response
 $G = 100, V_S = \pm 15V$



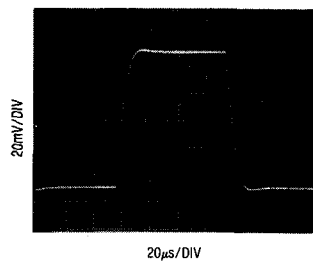
Large Signal Transient Response
 $G = 100, V_S = 5V, 0V$



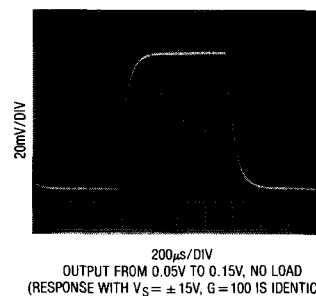
Small Signal Transient Response
 $G = 10, V_S = 5V, 0V$



Small Signal Transient Response
 $G = 10, V_S = \pm 15V$

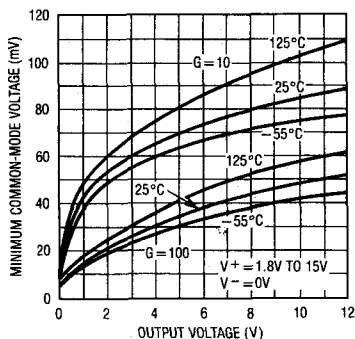


Small Signal Transient Response
 $G = 100, V_S = 5V, 0V$

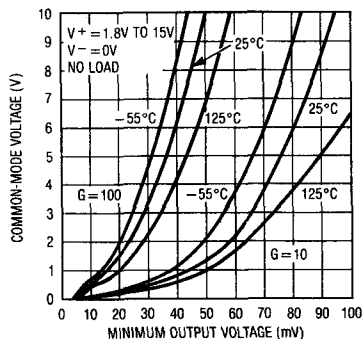


TYPICAL PERFORMANCE CHARACTERISTICS

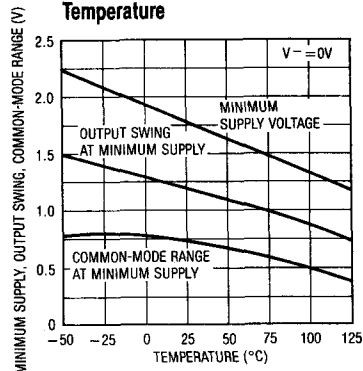
Single Supply: Minimum Common-Mode Voltage vs Output Voltage



Single Supply: Minimum Output Voltage vs Common-Mode Voltage



Minimum Supply Voltage vs Temperature



APPLICATIONS INFORMATION

Single Supply Applications

The LT1101 is the first instrumentation amplifier which is fully specified for single supply operation, i.e. when the negative supply is 0V. Both the input common-mode range and the output swing are within a few millivolts of ground.

Probably the most common application for instrumentation amplifiers is amplifying a differential signal from a transducer or sensor resistance bridge. All competitive instrumentation amplifiers have a minimum required common-mode voltage which is 3V to 5V above the negative supply. This means that the voltage across the bridge has to be 6V to 10V or dual supplies have to be used, i.e. micropower, single battery usage is not attainable on competitive devices.

The minimum output voltage obtainable on the LT1101 is a function of the input common-mode voltage. When the common-mode voltage is high and the output is low, current will flow from the output of amplifier A into the output of amplifier B. See the Minimum Output Voltage vs Common-Mode Voltage plot.

Similarly, the Minimum Common-Mode Voltage vs Output Voltage plot specifies the expected common-mode range.

When the output is high and input common-mode is low, the output of amplifier A has to sink current coming from the output of amplifier B. Since amplifier A is effectively in unity gain, its input is limited by its output.

Common-Mode Rejection vs Frequency

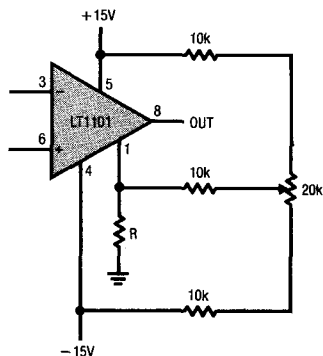
The common-mode rejection ratio (CMRR) of the LT1101 starts to roll off at a relatively low frequency. However, as shown on the CMRR vs Frequency plot, CMRR can be enhanced significantly by connecting an 82pF capacitor between pins 1 and 2. This improvement is only available in the gain 100 configuration, and it is in excess of 30dB at 60Hz.

Offset Nulling

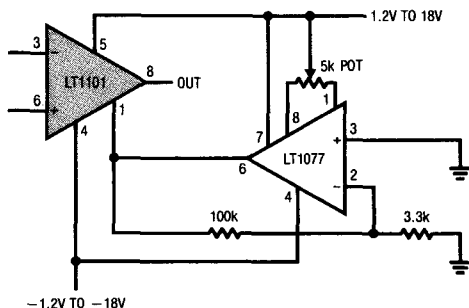
The LT1101 is not equipped with dedicated offset null terminals. In many bridge transducer or sensor applications, calibrating the bridge simultaneously eliminates the instrumentation amplifier's offset as a source of error. For example, in the Micropower Remote Temperature Sensor Application shown, one adjustment removes the offset errors due to the temperature sensor, voltage reference and the LT1101.

APPLICATIONS INFORMATION

A simple resistive offset adjust procedure is shown below. If $R = 5\Omega$ for $G = 10$, and $R = 50\Omega$ for $G = 100$ then the effect of R on gain error is approximately 0.006%. Unfortunately, about $450\mu A$ has to flow through R to bias the reference terminal (pin 1) and to null out the worst-case offset voltage. The total current through the resistor network can exceed 1mA, and the micropower advantage of the LT1101 is lost.



Another offset adjust scheme uses the LT1077 micropower op amp to drive the reference pin 1. Gain error and common-mode rejection are unaffected, the total current increase is $45\mu A$. The offset of the LT1077 is trimmed and amplified to match and cancel the offset voltage of the LT1101. Output offset null range is $\pm 25mV$.



Gains Between 10 and 100

Gains between 10 and 100 can be achieved by connecting two equal resistors ($= R_x$) between pins 1 and 2 and pins 7 and 8.

$$\text{Gain} = 10 + \frac{R_x}{R + R_x/90}$$

The nominal value of R is $9.2k\Omega$. The usefulness of this method is limited by the fact that R is not controlled to better than $\pm 10\%$ absolute accuracy in production. However, on any specific unit $90R$ can be measured between pins 1 and 2.

Input Protection

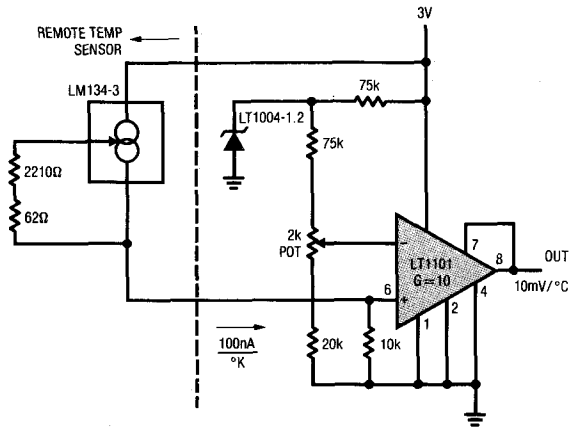
Instrumentation amplifiers are often used in harsh environments where overload conditions can occur. The LT1101 employs PNP input transistors, consequently the differential input voltage can be $\pm 30V$ (with $\pm 15V$ supplies, $\pm 36V$ with $\pm 18V$ supplies) without an increase in input bias current. Competitive instrumentation amplifiers have NPN inputs which are protected by back to back diodes. When the differential input voltage exceeds $\pm 1.3V$ on these competitive devices, input current increases to the milliampere level; more than $\pm 10V$ differential voltage can cause permanent damage.

When the LT1101's inputs are pulled above the positive supply, the inputs will clamp a diode voltage above the positive supply. No damage will occur if the input current is limited to 20mA.

500Ω resistors in series with the inputs protect the LT1101 when the inputs are pulled as much as 10V below the negative supply.

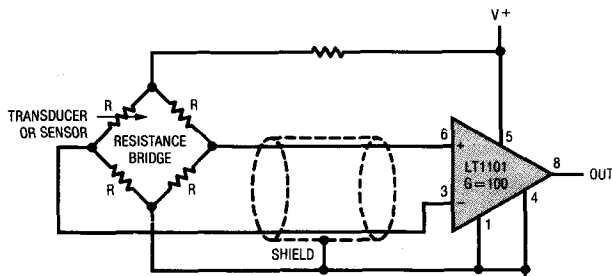
APPLICATIONS INFORMATION

Micropower, Battery Operated, Remote Temperature Sensor



TRIM OUTPUT TO 250mV AT 25°C
 TEMPERATURE RANGE = 2.5°C TO 150°C
 ACCURACY = ± 0.5°C

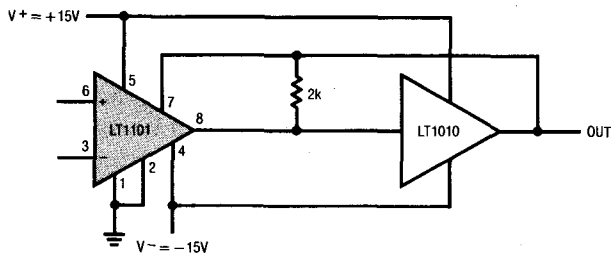
Differential Voltage Amplification from a Resistance Bridge



MINIMUM VOLTAGE ACROSS BRIDGE = 20mV
 MINIMUM SUPPLY VOLTAGE = 1.8V

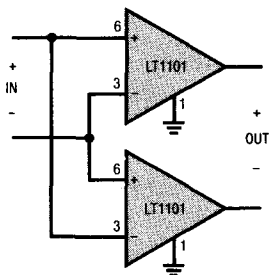
APPLICATIONS INFORMATION

Instrumentation Amplifier with $\pm 150\text{mA}$ Output Current



GAIN = 10, DEGRADED BY 0.01% DUE TO LT1010
 OUTPUT = $\pm 10\text{V}$ INTO 75Ω (TO 1.5kHz)
 DRIVES ANY CAPACITIVE LOAD
 SINGLE SUPPLY APPLICATION ($V+ = 5\text{V}$, $V- = 0\text{V}$):
 $V_{\text{OUT MIN}} = 120\text{mV}$, $V_{\text{OUT MAX}} = 3.4\text{V}$

Differential Input — Differential Output Instrumentation Amplifier



GAIN = 200, AS SHOWN
 GAIN = 20, SHORT PIN 1 TO PIN 2, PIN 7 TO PIN 8
 ON BOTH DEVICES
 GAIN = 110, SHORT PIN 1 TO PIN 2, PIN 7 TO PIN 8
 ON ONE DEVICE, NOT ON THE OTHER

High Speed, Precision, JFET Input Instrumentation Amplifier (Fixed Gain = 10 or 100)

May 1989

FEATURES

- Settling Time (0.01%) $3\mu\text{s}$
- Slew Rate $25\text{V}/\mu\text{s}$
- Gain-Bandwidth Product 30MHz
- Gain Error 0.05% Max
- Gain Drift $5\text{ppm}/^\circ\text{C}$
- Gain Non-Linearity 10ppm Max
- Offset Voltage (Input + Output) $500\mu\text{V}$ Max
- Drift with Temperature $2.5\mu\text{V}/^\circ\text{C}$
- Input Bias Current 50pA Max
- Input Offset Current 40pA Max
- Drift with Temperature (to 70°C) $1\text{pA}/^\circ\text{C}$
- Common-Mode Rejection Ratio 100dB
- $G = 10$ 100dB
- $G = 10$ 100dB

DESCRIPTION

The LT1102 is the first fast FET input instrumentation amplifier offered in the low cost, space saving 8-pin packages. Fixed gains of 10 and 100 are provided with excellent gain accuracy (0.015%) and non-linearity (2ppm). No external gain setting resistor is required.

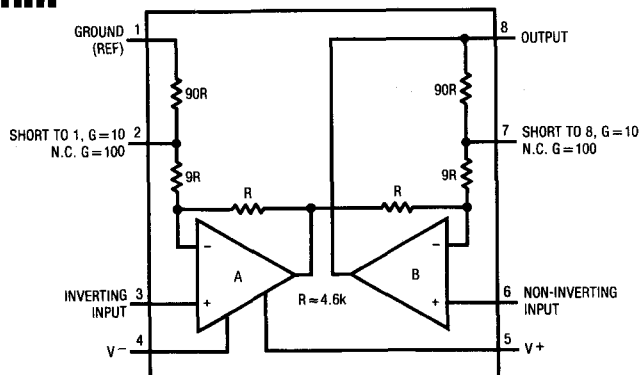
The fastest slew rate of any instrumentation amplifier is combined with impressive precision specifications: less than 10pA input bias and offset currents, 200 μV offset voltage. Unlike other FET input instrumentation amplifiers, on the LT1102 there is no input offset voltage contribution to total error and input bias currents do not double with every 10 $^\circ\text{C}$ rise in temperature. In fact, at 70°C ambient temperature the input bias current is only 50pA.

APPLICATIONS

- Fast Settling Amplifier for Signal Processing
- Multiplexed Input Data Acquisition Systems
- High Source Impedance Signal Amplification from High Resistance Bridges, Capacitance Sensors, Photodetector Sensors
- Bridge Amplifier with $<1\text{Hz}$ Lowpass Filtering

REFER TO TABLE OF CONTENTS FOR REVISED DATA LOCATION

BLOCK DIAGRAM



GROUND PIN 1, OUTPUT AT PIN 8
 G = 100: NO ADDITIONAL CONNECTIONS
 G = 10: SHORT PIN 2 TO PIN 1, SHORT PIN 7 TO PIN 8

±15V Chopper Stabilized Operational Amplifier with Internal Capacitors

June 1989

FEATURES

- High Voltage Operation, ±18V
- No External Components Required
- Maximum Offset Voltage 5 μ V
- Maximum Offset Voltage Drift 0.05 μ V/°C
- Low Noise, 1.8 μ Vp-p (0.1Hz to 10Hz)
- Minimum Voltage Gain 140dB
- Minimum PSRR 130dB
- Minimum CMRR 120dB
- Low Supply Current 0.8mA
- Single Supply Operation 4.75V to 36V
- Input Common Mode Range Includes Ground
- 200 μ A Supply Current with Pin 1 Grounded
- Typical Overload Recovery Time 20ms

DESCRIPTION

The LTC1150 is a high-voltage, high-performance chopper stabilized operational amplifier. The two sample-and-hold capacitors usually required externally by other chopper amplifiers are integrated on-chip. Further, the LTC's proprietary high-voltage CMOS structures allow the LTC1150 to operate at up to 36V total supply voltage.

The LTC1150 has an offset voltage of 0.5 μ V, drift of 0.01 μ V/°C, 0.1Hz to 10Hz input noise voltage of 1.8 μ Vp-p and a typical voltage gain of 180dB. The slew rate of 3V/ μ s and a gain bandwidth product of 2.5MHz are achieved with 0.8mA of supply current. Overload recovery times from positive and negative saturation conditions are 3ms and 20ms, respectively.

APPLICATIONS

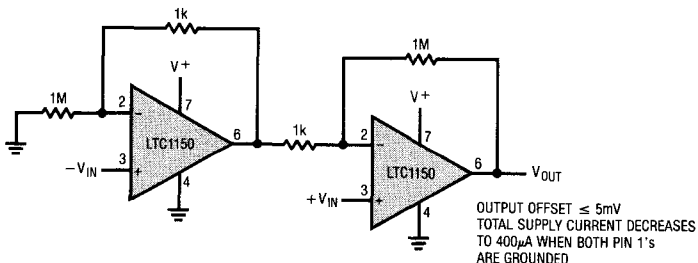
- Strain Gauge Amplifiers
- Electronic Scales
- Medical Instrumentation
- Thermocouple Amplifiers
- High Resolution Data Acquisition

In applications demanding low power consumption, pin 1 can be used to program the supply current. Pin 5 is an optional AC-coupled clock input, useful for synchronization.

The LTC1150 is available in standard 8-pin metal can, plastic and ceramic dual in line packages as well as an 8-pin SO8 package. The LTC1150 can be a plug-in replacement for most standard bipolar op amps with significant improvement in DC performance.

TYPICAL APPLICATION

Single Supply Instrumentation Amplifier



LTC1150

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Total Supply Voltage (V^+ to V^-)	36V	Operating Temperature Range	
Input Voltage	($V^+ + 0.3V$) to ($V^- - 0.3V$)	LTC1150M	-55°C to 125°C
Output Short Circuit Duration	Indefinite	LTC1150C	-40°C to 85°C
Burn-In Voltage	30V	Storage Temperature Range	-65°C to 150°C
		Lead Temperature (Soldering, 10 sec.)	300°C

PACKAGE/ORDER INFORMATION

<p>TOP VIEW CLOCK OUT</p> <p>H PACKAGE 8-LEAD TO-5 METAL CAN</p>	<p>ORDER PART NUMBER</p> <p>LTC1150MH LTC1150CH</p>	<p>TOP VIEW</p> <p>J PACKAGE 14-LEAD CERAMIC DIP</p> <p>N PACKAGE 14-LEAD PLASTIC DIP</p>	<p>ORDER PART NUMBER</p> <p>LTC1150MJ LTC1150CJ LTC1150CN</p>
<p>TOP VIEW</p> <p>J PACKAGE 8-LEAD CERAMIC DIP</p> <p>N PACKAGE 8-LEAD PLASTIC DIP</p>	<p>ORDER PART NUMBER</p> <p>LTC1150MJ8 LTC1150CJ8 LTC1150CN8</p>	<p>TOP VIEW</p> <p>SO PACKAGE 8-LEAD PLASTIC SOIC</p>	<p>ORDER PART NUMBER</p> <p>LTC1150CS8</p>

ELECTRICAL CHARACTERISTICS

$V_S = \pm 15V$, Pin 1 = Open, T_A = Operating Temperature Range, Unless Otherwise Specified.

PARAMETER	CONDITIONS	LTC1150M			LTC1150C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$T_A = 25^\circ\text{C}$ (Note 3)		± 0.5	± 5	± 0.5	± 5		μV
Average Input Offset Drift	(Note 3)	●	± 0.01	± 0.05	± 0.01	± 0.05		$\mu\text{V}/^\circ\text{C}$
Long Term Offset Voltage Drift			50		50			nV/mo
Input Offset Current	$T_A = 25^\circ\text{C}$	●	± 20	± 60 ± 150	± 20	± 100 ± 150		pA pA
Input Bias Current	$T_A = 25^\circ\text{C}$	●	± 10	± 30 ± 800	± 10	± 50 ± 100		pA pA
Input Noise Voltage	$R_S = 100\Omega$, 0.1Hz to 10Hz, TC2		1.8		1.8			$\mu\text{V}/\text{p}$
	$R_S = 100\Omega$, 0.1Hz to 1Hz, TC2		0.6		0.6			$\mu\text{V}/\text{p}$
Input Noise Current	$f = 10\text{Hz}$ (Note 4)		2.5		2.5			$\text{fA}/\sqrt{\text{Hz}}$
Common Mode Rejection Ratio	$V_{CM} = V^-$ to 12V	●	120		115			dB

ELECTRICAL CHARACTERISTICS

$V_S = \pm 15V$, Pin 1 = Open, T_A = Operating Temperature Range, Unless Otherwise Specified.

PARAMETER	CONDITIONS		LTC1150M			LTC1150C			UNITS	
			MIN	TYP	MAX	MIN	TYP	MAX		
Power Supply Rejection Ratio	$V_S = \pm 2.375V$ to $\pm 16V$	●	130	145		125	145		dB	
Large Signal Voltage Gain	$R_L = 10k\Omega$, $V_{OUT} = \pm 10V$	●	140	180		140	180		dB	
Maximum Output Voltage Swing	$R_L = 10k\Omega$ $T_A = 25^\circ C$		± 13.8	± 14.5		± 13.8	± 14.5		V	
			± 11.3			± 12.3			V	
				± 14.95		± 14.95			V	
Slew Rate	$R_L = 10k\Omega$, $C_L = 50pF$			3		3			V/ μs	
Gain Bandwidth Product				2.5		2.5			MHz	
Supply Current	No Load	$T_A = 25^\circ C$		0.8	1.2		0.8	1.2		mA
	No Load, Pin 1 = V-	$T_A = 25^\circ C$		0.2			0.2			mA
	No Load		●		1.8			1.8		mA
Internal Sampling Frequency				550		550			Hz	

ELECTRICAL CHARACTERISTICS

$V_S = 5V$, Pin 1 = Open, T_A = Operating Temperature Range, Unless Otherwise Specified.

PARAMETER	CONDITIONS		LTC1150M			LTC1150C			UNITS	
			MIN	TYP	MAX	MIN	TYP	MAX		
Input Offset Voltage	$T_A = 25^\circ C$ (Note 3)			± 0.5	± 5		± 0.5	± 5	μV	
Average Input Offset Drift	(Note 3)	●		± 0.01	± 0.05		± 0.01	± 0.05	$\mu V/^\circ C$	
Long Term Offset Voltage Drift				50			50		nV/ \sqrt{mo}	
Input Offset Current	$T_A = 25^\circ C$	●		± 10	± 30 ± 100		± 10	± 60 ± 100	pA	
Input Bias Current	$T_A = 25^\circ C$	●		± 5	± 15 ± 400		± 5	± 30 ± 100	pA	
Input Noise Voltage	$R_S = 100\Omega$, 0.1Hz to 10Hz, TC2			2.0			2.0		$\mu Vp-p$	
	$R_S = 100\Omega$, 0.1Hz to 1Hz, TC2			0.7			0.7		$\mu Vp-p$	
Input Noise Current	$f = 10Hz$ (Note 4)			1.3			1.3		fA/ \sqrt{Hz}	
Common Mode Rejection Ratio	$V_{CM} = 0V$ to $2.7V$	●		110			110		dB	
Power Supply Rejection Ratio	$V_S = \pm 2.375V$ to $\pm 16V$	●		130	145		125	145	dB	
Large Signal Voltage Gain	$R_L = 10k\Omega$, $V_{OUT} = 0.3V$ to $4.5V$	●		130	180		130	180	dB	
Maximum Output Voltage Swing	$R_L = 10k\Omega$			$0.15 - 4.85$			$0.15 - 4.85$		V	
	$R_L = 100k\Omega$			$0.02 - 4.97$			$0.02 - 4.97$		V	
Slew Rate	$R_L = 10k\Omega$, $C_L = 50pF$			1.5			1.5		V/ μs	
Gain Bandwidth Product				1.8			1.8		MHz	
Supply Current	No Load	$T_A = 25^\circ C$		0.4	0.65		0.4	0.65		mA
			●			0.95			0.95	
Internal Sampling Frequency				300			300		Hz	

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: Absolute Maximum Ratings are those values beyond which life of the device may be impaired.

Note 2: Connecting any terminal to voltages greater than $V+$ or less than $V-$ may cause destructive latch-up. It is recommended that no sources operating from external supplies be applied prior to power-up of the LTC1150.

Note 3: These parameters are guaranteed by design. Thermocouple effects preclude measurement of these voltage levels in high-speed automatic test systems. V_{OS} is measured to a limit determined by test equipment capability.

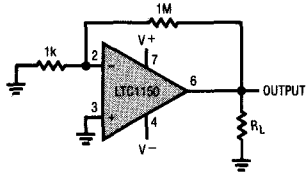
Note 4: Current Noise is calculated from the formula:

$$I_N = \sqrt{2q \cdot 1b}$$

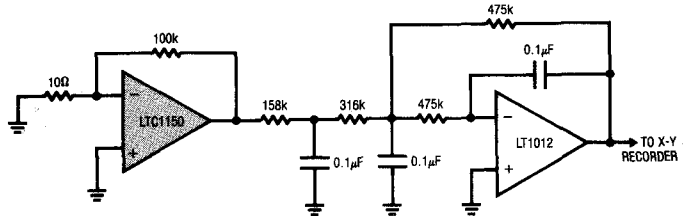
where $q = 1.6 \times 10^{-19}$ Coulomb.

TEST CIRCUITS

Offset Voltage Test Circuit



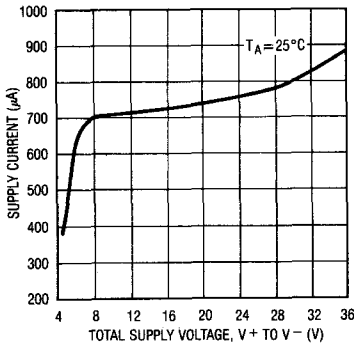
DC-10Hz Noise Test Circuit



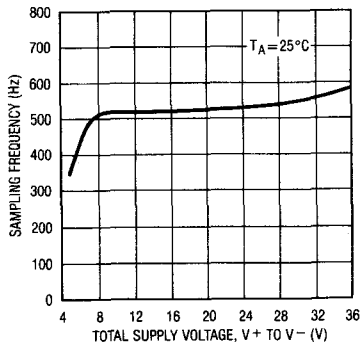
FOR 1Hz NOISE BW INCREASE ALL THE CAPACITORS BY A FACTOR OF 10.

TYPICAL PERFORMANCE CHARACTERISTICS

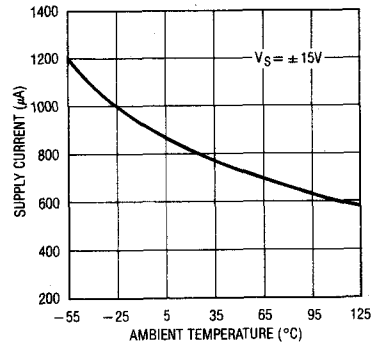
Supply Current vs Supply Voltage



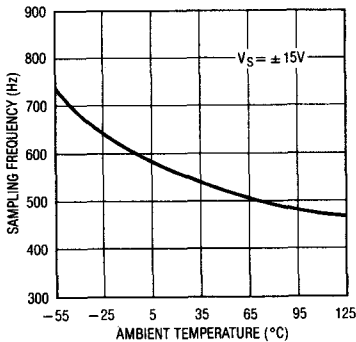
Sampling Frequency vs Supply Voltage



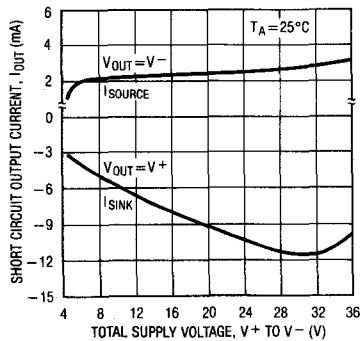
Supply Current vs Temperature



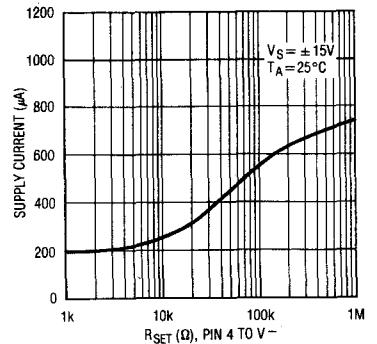
Sampling Frequency vs Temperature



Output Short Circuit Current vs Supply Voltage

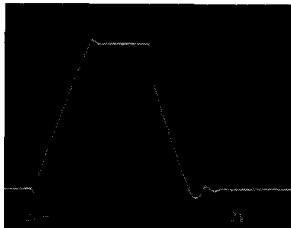


Supply Current vs RSET



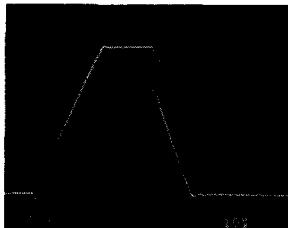
TYPICAL PERFORMANCE CHARACTERISTICS

Large Signal Transient Response



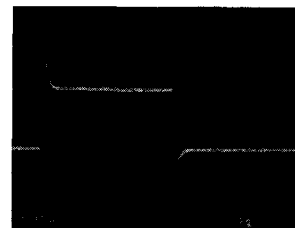
$V_S = \pm 15V$, $A_V = 1$, $C_L = 100pF$, $R_L = 10k\Omega$

Large Signal Transient Response,
Pin 1 = V^-



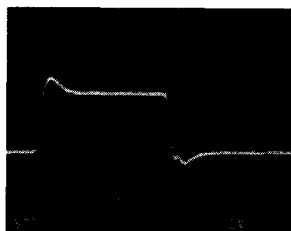
$V_S = \pm 15V$, $A_V = 1$, $C_L = 100pF$, PIN 1 = V^-

Small Signal Transient Response



$V_S = \pm 15V$, $A_V = 1$, $C_L = 100pF$, $R_L = 10k\Omega$

Small Signal Transient Response,
Pin 1 = V^-



$V_S = \pm 15V$, $A_V = 1$, $C_L = 100pF$,
 $R_L = 10k\Omega$, PIN 1 = V^-

PIN DESCRIPTION

1) 8-PIN PACKAGES

Pin 1 - Supply Current Programming Pin. The circuit supply current can be programmed through pin 1. When pin 1 is left open in normal operation the supply current is 800 μ A. Supply current can be reduced by connecting a resistor between pin 1 and pin 4, the negative supply pin. The supply current, as a function of the resistor value, is shown in typical performance curves.

Pin 2 - Inverting Input.

Pin 3 - Non-Inverting Input.

Pin 4 - Negative Supply.

Pin 5 - Optional External Clock Input. The LTC1150 has an internal oscillator to control the circuit operation of the amplifier. When an external clock is desirable it can be applied to pin 5. The applied clock is AC-coupled to the internal circuitry to simplified interface requirements. The amplitude of clock input signal needs to be greater than 2V and the voltage level has to be within the supply voltage range. Duty cycle is not critical. The internal chopping frequency is the external clock frequency divided by four. When frequency of the external clock falls below 100Hz (internal chopping at 25Hz), internal oscillator takes over and the circuit chops at 550Hz.

Pin 6 - Output.

Pin 7 - Positive Supply.

PIN DESCRIPTION

Pin 8 - Clock Output Pin. The signal coming out of this pin is at the internal oscillator frequency of about 2.2kHz (four times the chopping frequency) and has voltage levels at $V_H = +V_S$ and $V_L = +V_S - 4.6V$. If the circuit is driven by an external clock, pin 8 is pulled up to $+V_S$.

2) 14-PIN PACKAGES

Pin 1 - Supply Current Programming Pin. Function same as in 8-pin packages.

Pin 4 - Inverting Input.

Pin 5 - Non-Inverting Input.

Pin 7 - Negative Supply.

Pin 10 - Output.

Pin 11 - Positive Supply.

Pin 12 - Clock Output Pin. Signal frequency is that of the chopping frequency. The voltage level swings between $+V_S$ and $+V_S - 4.6V$.

Pin 13 - External Clock Input. With pin 14 tied to the $-V_S$ supply, an external clock can be applied to pin 13 with the threshold 2.2V below the $+V_S$ supply. Chopping frequency of the circuit is the input clock frequency divided by four. With no external connection, pin 14 is pulled up to $+V_S$ supply and the internal oscillator controls the circuit operation. A switching signal of the oscillator frequency (2.2kHz) appears on pin 13.

Pin 14 - Internal/External Clock Selection Pin. Refer to description of pin 13.

FEATURES

- 1.5A Bipolar Switch
- Controlled Output Slew Rate ($2V/\mu s$) to Limit R.F.I. Generation
- 60V Load Dump Capability with Inductive Kickback
- Internal Negative Voltage Clamp for Inductive Loads
- 500 μA Standby Current
- Logic Input — TTL Levels
- Low Input Bias Current (20 μA)
- Status Output
- Short Circuit Detection and Shutoff
- Open Circuit Detection
- Overtemp Detection and Shutoff

APPLICATIONS

- Solenoid Driver
- Relay Driver
- Motor Driver

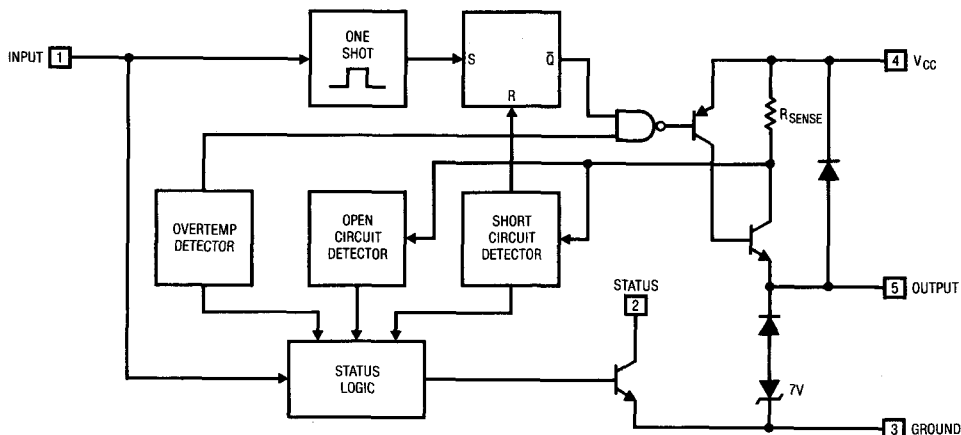
REFER TO TABLE OF CONTENTS FOR REVISED DATA LOCATION

DESCRIPTION

The LT1188 is a monolithic high side switch employing bipolar technology. The device is designed to operate in harsh environments such as those encountered in the automotive industry. The device incorporates an internal clamp diode to clamp the negative voltage spikes generated by inductive loads such as solenoids and is capable of withstanding load dumps of 60V on the supply pin while clamping such spikes. Standby current is only 500 μA and ground pin current, when driving a 1A load, is only 5mA.

The device's input logic levels are designed to be compatible with standard TTL levels, drawing only 20 μA in the on state. A status pin is provided to inform the user of the condition of the output load as well as the switch. The status pin will change state for shorted as well as open loads and will also indicate when the device is above normal operating temperature. The device protects itself against short circuited loads by limiting output current and then shutting itself off after a specified time if the short remains. The device protects itself against overtemperature by shutting itself off. Overtemperature shutoff occurs at a temperature above where the status pin overtemp indication occurs, allowing the user time to recognize and possibly correct the problem before drive to the load is removed.

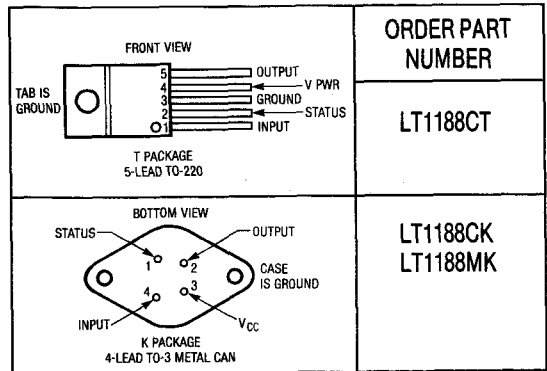
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	30V
Supply Voltage (Transient 200ms)	60V
Logic Input Voltage	30V
Operating Temperature Range	
LT1188M	-55°C to 125°C
LT1188C	0°C to 70°C
Junction Temperature Range	
LT1188M	-55°C to 175°C
LT1188C	0°C to 100°C
Storage Temperature	-65°C to 150°C
Lead Temperature (Soldering, 10 sec)	300°C

PACKAGE/ORDER INFORMATION



ELECTRICAL CHARACTERISTICS (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	
Switch Voltage Loss ($V_{CC}-V_{OUT}$, Switch On)	$I_{OUT} = 1.0A, 5V \leq V_{CC} \leq 30V$	●	1.0	1.2	V	
	$I_{OUT} = 1.5A, 5V \leq V_{CC} \leq 30V$	●	1.2	1.4	V	
Output Leakage Current	$V_{CC} = 30V, V_{OUT} = 0V, V_{IN} = 0V$	●	5	150	μA	
High Level Input Voltage	$5V \leq V_{CC} \leq 30V, I_{OUT} = 1.5A, (Note\ 2)$	●	2.0		V	
Low Level Input Voltage	$5V \leq V_{CC} \leq 30V, I_{OUT} = 0.0A, (Note\ 3)$	●		0.8	V	
High Level Input Current	$5V \leq V_{CC} \leq 30V, V_{IN} = 2.0V$	●	5	20	60	μA
Low Level Input Current	$5V \leq V_{CC} \leq 30V, V_{IN} = 0.4V$	●	0	1		μA
Status Pin Saturation Voltage	$5V \leq V_{CC} \leq 30V, I_{STATUS} = 1mA$	●	0.2	0.4	V	
Status Leakage Current	$V_{CC} = 30V, V_{STAT} = 5.5V$	●		1	μA	
Standby Current	$V_{IN} = 0.4V, R_L = \infty, V_{CC} = 30V$ Status = High	●	500	650	μA	
		●	550	750	μA	
Ground Pin Current	$V_{CC} = 30V, I_{OUT} = 1.5A$	●	9	15	mA	
Clamp Voltage	$I_{CLAMP} = 1.0A, (Note\ 4)$	●	8	10	V	
	$I_{CLAMP} = 1.5A, (Note\ 4)$	●	9	12	V	
Turn-On Delay	(Note 5)	●		30	μs	
Turn-Off Delay	(Note 6)	●		30	μs	
Output Slew Rate	$V_{CC} = 17V, R_L = 16\Omega$ Output Rising	●	0.5	1.2	5.0	V/ μs
		●	0.5	2.0	5.0	V/ μs
Short Circuit Current	$V_{CC}-V_{OUT} = 7V$	●	2.0	3.5	A	
		●		2.5	4.7	A
	$V_{CC}-V_{OUT} = 17V$	●	1.5	4.0	A	
		●		1.5	3.0	A

ELECTRICAL CHARACTERISTICS (Note 1)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Short Circuit Sense Time (t_{SC})	$V_{CC} = 30V$	●	20	50	110	μS
Status Reset Time (t_R)	$V_{CC} = 30V$	●	350	600	950	μS
Open Circuit Current Trip Level		●	18	40	75	mA
Overtemp Detection Point				150		$^{\circ}C$
Thermal Resistance	Junction to Case (Note 7)				4.0	$^{\circ}C/W$

Note 1: The ● denotes specifications which apply over the full operating temperature range.

Note 2: 2.0V is the minimum input voltage guaranteed to turn the device on. For input voltages greater than 2.0V the output voltage is guaranteed to be turned on.

Note 3: 0.8V is the maximum input voltage guaranteed to turn the device off. For input voltages less than 0.8V the device is guaranteed to be turned off.

Note 4: The negative voltage clamp is designed for intermittent operation such as clamping the reverse voltage spike caused by an inductive load. Clamp duration should be less than 100ms.

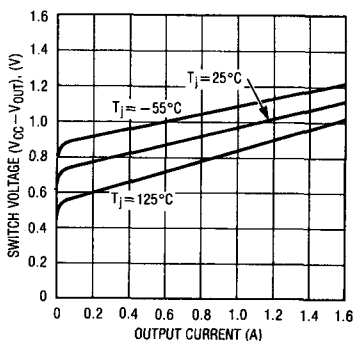
Note 5: Turn on delay time is defined to be the time from the rising edge of the input signal to the time that the output voltage is equal to 2V.

Note 6: Turn off delay time is defined to be the time from the falling edge of the input signal to the time that the output drops by 2V.

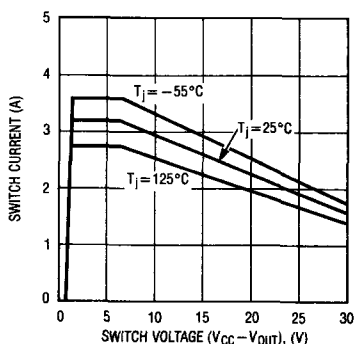
Note 7: Thermal resistance is from the junction of the switch transistor to the back of the case directly below the switch transistor. The device will be centered in the package and proper mounting techniques are required in order to have good thermal conduction away from this area of the package.

TYPICAL PERFORMANCE CHARACTERISTICS

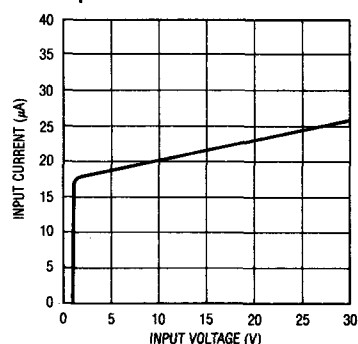
Switch Voltage Loss



Short Circuit Current

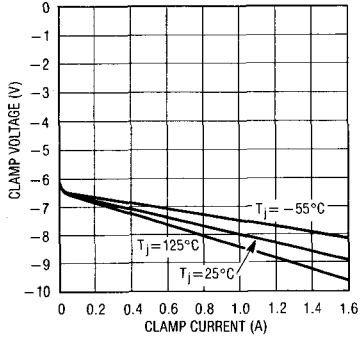


Input Current

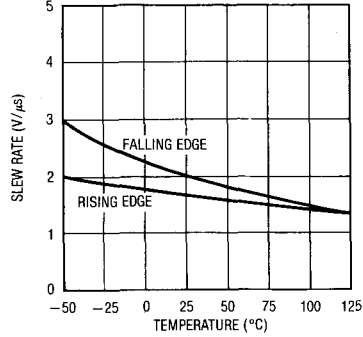


TYPICAL PERFORMANCE CHARACTERISTICS

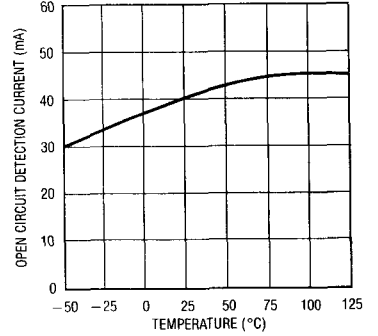
Clamp Voltage



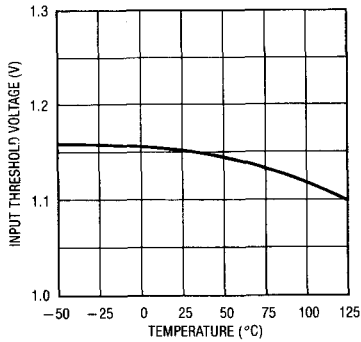
Slew Rate



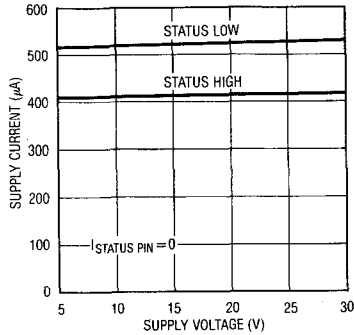
Open Circuit Detection Current



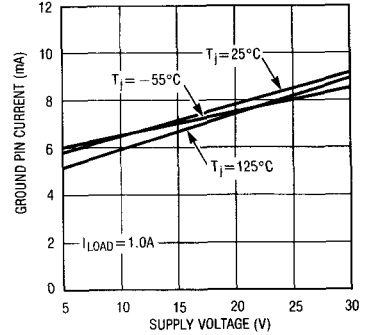
Input Threshold Voltage



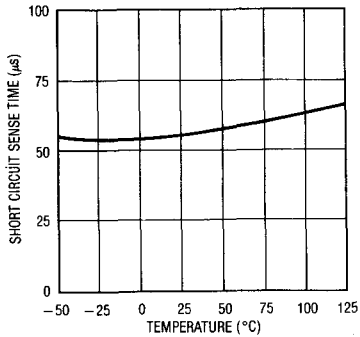
Supply Current (Switch Off)



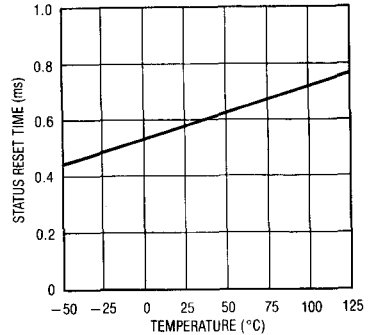
Ground Pin Current (Switch On)



Short Circuit Sense Time



Status Reset Time



PIN FUNCTIONS

Output: As can be seen from the block diagram the output of the device is the emitter of an NPN power transistor which can source current from the supply. The slew rate of the output, both rising and falling, is controlled to minimize the generation of RFI. In the negative direction the output pin is clamped to ground with a combination diode/zener clamp. This clamp is designed to clamp the flyback voltage spike of an inductive load such as a solenoid. This clamp is designed for intermittent operation. The duration of the flyback spike should be less than 100ms. This allows a wide range of inductive loads. In the positive direction the output pin is clamped to the supply with a diode.

Ground: The ground pin of the device must be connected for the device to turn on. For an open ground pin the device will be in an off state.

Input: The input pin of the device must be driven above the input voltage threshold for the device to turn on. The input voltage threshold is designed to be compatible with standard TTL levels, while the input impedance is high. Input current above the threshold is typically 20 μ A. For an open input pin the device will remain in an off state. The input

logic requires a minimum input voltage slew rate of 3V/ms. This is several orders of magnitude slower than any logic family currently in use and should not normally cause any problems.

Status: The status output is the collector of a grounded emitter NPN transistor whose base is internally driven by the status logic. A logic low indicates a fault condition (see Truth Table). This output requires an external pull-up resistor that should be chosen so that the current into the status pin, when the status pin is pulled low, is < 1mA. The breakdown voltage of this NPN collector is equal to that of the output switch.

Diagnostic Truth Table

	Input	Output	Status
Normal Operation	L	L	H
	H	H	H
Open Load	L	X	H
	H	H	L
Shorted Load	L	L	L
	H	L	L
Thermal Overload	L	L	H
	H	L	L

STATUS FUNCTIONS

Open Circuit Fault: The status output will be pulled low if the output current drops below the open circuit current threshold (typically 40mA). The open circuit detector is only active during the time that the switch is on (input high), and will only affect the status output during that time. For open circuit faults the status output will not latch low. The status line will be low only as long as the fault condition exists.

Short Circuit Fault: For short circuit faults lasting longer than the short circuit sense time ($\approx 60\mu$ s), two things will occur; the output switch will be latched off and the status output will be latched low. The output will remain off until the input is recycled. The status output will remain low until both the short is removed and the input is recycled, and will be reset high after the status reset time ($\approx 500\mu$ s) has elapsed. For continuous shorts the output will turn on, for the short circuit sense time, each time the input is cycled

and the status output will remain latched low. The current at which the short circuit detector activates is a function of the supply voltage as can be seen by looking at the short circuit current curve in the typical performance characteristics.

Thermal Fault: Thermal faults can occur for two reasons, heating from external sources or heating due to power dissipation in the switch itself. The device will act similarly for both cases. Thermal faults will only affect the status output during the time that the switch is on (input high). Thermal faults will cause the status output to latch low for the duration of an input cycle. The status output will be reset on the falling edge of the input waveform. There are two levels of thermal overload. At $\approx 150^\circ\text{C}$ junction temperature the thermal sensing circuitry will latch the status output low, and the output will remain on (as long as the input is high). At $\approx 165^\circ\text{C}$ the thermal sensing circuitry will

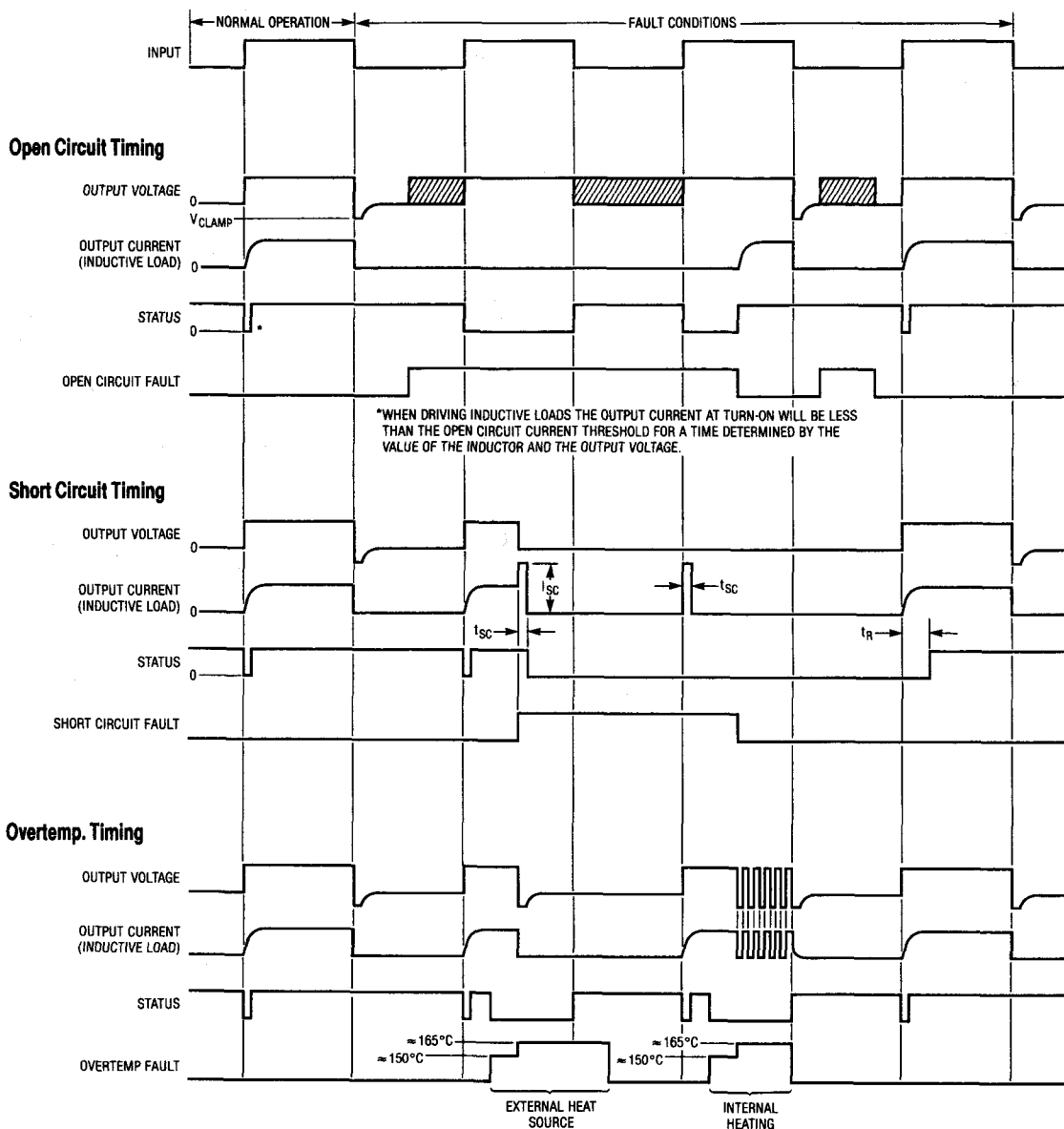
STATUS FUNCTIONS

turn the output off. If the junction temperature drops back below $\approx 165^{\circ}\text{C}$ the output will turn back on. This means that if the thermal fault is caused by an external source the output will stay off as long as the temperature is held above $\approx 165^{\circ}\text{C}$. If the thermal fault is caused by internal power dissipation, the device will cycle on and off to maintain the junction temperature near 165°C . The status output gives a fault indication at a temperature below the actual shutdown temperature to allow the user time to sense and possibly correct the fault condition before the switch takes action to protect itself.

Load Dump: For transient supply voltages greater than 35V or for transient switch voltages greater than 35V, a separate clamp network will turn the output off. This is necessary to keep the switch within its safe operating area and also to prevent the device from passing the high

voltage transient on to the load. To guarantee survival of the switch for load dump type transients the risetime of the supply voltage, at the supply pin of the device, should be limited to $< 1\text{V}/\mu\text{s}$. This is to allow the device time to turn off between when the supply voltage reaches 35V and when the supply voltage reaches 50V so that the device is turned off well below its BVCEO voltage. If the device is bypassed closely, the series inductance and resistance of the supply leads along with the supply bypass capacitor will form an RLC filter and will limit the risetime. The slew rate limiting circuitry will be disabled during this transient turn off time. The output will remain off until the supply voltage drops back below 35V. During the time that the output is turned off by this clamp network the open circuit detector will still be active and will set the status pin low until the output comes back on and the output current is greater than the open circuit current.

TIMING DIAGRAM



FEATURES

- Software Programmable Features
 - Unipolar/Bipolar Conversions
 - 4 Differential/8 Single Ended Inputs
 - MSB or LSB First Data Sequence
 - Variable Data Word Length
 - Power Shutdown
- Built-In Sample and Hold
- Single Supply 5V, 10V or $\pm 5V$ Operation
- Built-In Sample and Hold for Single Ended Inputs
- Direct 4 Wire Interface to Most MPU Serial Ports and all MPU Parallel Ports
- 50kHz Maximum Throughput Rate

KEY SPECIFICATIONS

- Resolution 12 Bits
- Fast Conversion Time 13.6 μ s, T_{amb}
- Low Supply Current 5.0mA

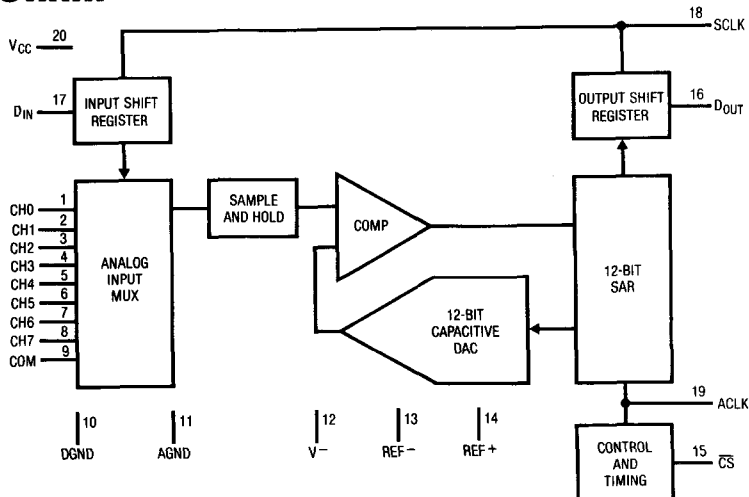
DESCRIPTION

The LTC1290 is a data acquisition component which contains a serial I/O successive approximation A/D converter. It uses LTCMOST[™] switched capacitor technology to perform either 12-bit unipolar, or 11-bit plus sign bipolar A/D conversions. The 8 channel input multiplexer can be configured for either single ended or differential inputs (or combinations thereof). An on-chip sample and hold is included for all single ended input channels. When the LTC1290 is idle it can be powered down in applications where low power consumption is desired.

The serial I/O is designed to be compatible with industry standard full duplex serial interfaces. It allows either MSB or LSB first data sequence. It automatically provides 2's complement output coding in the bipolar mode. The output data word can be programmed for a length of 8, 12 or 16-bits. This allows easy interface to shift registers and a variety of processors.

LTCMOS is a trademark of Linear Technology Corporation.

BLOCK DIAGRAM

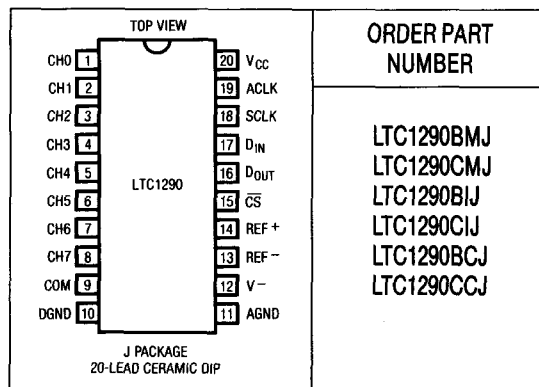


ABSOLUTE MAXIMUM RATINGS

(Notes 1 and 2)

Supply Voltage (V_{CC}) to GND or V^-	12V
Negative Supply Voltage (V^-)	-6V to GND
Voltage	
Analog and Reference Inputs .. (V^-)	-0.3V to $V_{CC} + 0.3V$
Digital Inputs	-0.3V to 12V
Digital Outputs	-0.3V to $V_{CC} + 0.3V$
Power Dissipation	500mW
Operating Temperature Range	
LTC1290BC, LTC1290CC	0°C to 70°C
LTC1290BI, LTC1290CI	-40°C to 85°C
LTC1290BM, LTC1290CM	-55°C to 125°C
Storage Temperature Range	-65°C to 150°C
Lead Temperature (Soldering, 10 sec.)	300°C

PACKAGE/ORDER INFORMATION



ORDER PART NUMBER

- LTC1290BMJ
- LTC1290CMJ
- LTC1290BIJ
- LTC1290CIJ
- LTC1290BCJ
- LTC1290CCJ

CONVERTER AND MULTIPLEXER CHARACTERISTICS (Note 3)

PARAMETER	CONDITIONS	LTC1290B		LTC1290C		UNITS	
		MIN	TYP	MAX	MIN		MAX
Offset Error	(Notes 4 and 5)	●		± 1.5		± 1.5	LSB
Linearity Error	(Notes 4 and 5)	●		± 0.5		± 0.5	LSB
Gain Error	(Notes 4 and 5)	●		± 0.5		± 1.0	LSB
Total Unadjusted Error	$V_{REF} = 5.000V$ (Notes 4 and 6)	●		± 2.5		± 3.0	LSB
Analog and REF Input Range	(Note 7)			$(V^-) - 0.05V$ to $V_{CC} + 0.05V$			V
On Channel Leakage Current (Note 8)	On Channel = 5V Off Channel = 0V	●		± 1		± 1	μA
	On Channel = 0V Off Channel = 5V	●		± 1		± 1	μA
Off Channel Leakage Current (Note 8)	On Channel = 5V Off Channel = 0V	●		± 1		± 1	μA
	On Channel = 0V Off Channel = 5V	●		± 1		± 1	μA

AC CHARACTERISTICS (Note 3)

SYMBOL	PARAMETER	CONDITIONS	LTC1290B LTC1290C			UNITS
			MIN	TYP	MAX	
f_{SCLK}	Shift Clock Frequency		0		2.0	MHz
f_{ACLK}	A/D Clock Frequency		● f_{SCLK}		4.0	MHz
t_{ACC}	Delay Time from \overline{CS} ↓ to D_{OUT} Data Valid	(Note 9)		2		ACLK Cycles
t_{SMPL}	Analog Input Sample Time	See Operating Sequence		7		SCLK Cycles
t_{CONV}	Conversion Time	See Operating Sequence		52		ACLK Cycles
t_{CYC}	Total Cycle Time	See Operating Sequence		12 SCLK + 56 ACLK		Cycles
t_{dDO}	Delay Time, SCLK ↓ to D_{OUT} Data Valid	See Parameter Measurement Section	●	130		ns
t_{dis}	Delay Time, \overline{CS} ↓ to D_{OUT} Hi-Z	See Parameter Measurement Section	●	70		ns
t_{en}	Delay Time, 2nd ACLK ↓ to D_{OUT} Enabled	See Parameter Measurement Section	●	130		ns
t_{hCS}	Hold Time, \overline{CS} After SCLK ↓			0		ns
t_{hDI}	Hold Time, D_{IN} After SCLK ↓					ns
t_{hDO}	Time Output Data Remains Valid After SCLK ↓					ns
t_f	D_{OUT} Fall Time	See Parameter Measurement Section	●	65		ns
t_r	D_{OUT} Rise Time	See Parameter Measurement Section	●	25		ns
t_{suDI}	Setup Time, D_{IN} Stable Before SCLK ↓					ns
t_{suCS}	Setup Time, \overline{CS} ↓ Before Clocking in First Address Bit	(Note 9)		2		ACLK Cycles
t_{WHCS}	\overline{CS} High Time During Conversion			52		ACLK Cycles
C_{IN}	Input Capacitance	Analog Inputs On Channel Off Channel				pF
		Digital Inputs				pF

Note 1: Absolute maximum ratings are those values beyond which the life of a device may be impaired.

Note 2: All voltage values are with respect to ground with DGND, AGND, and REF⁻ wired together (unless otherwise noted).

Note 3: $V_{CC} = 5V$, $V_{REF+} = 5V$, $V_{REF-} = 0V$, $V^- = 0V$ for unipolar mode and $-5V$ for bipolar mode, ACLK = 4.0MHz unless otherwise specified. The ● indicates specs which apply over the full operating temperature range; all other limits and typicals $T_A = 25^\circ C$.

Note 4: These specs apply for both unipolar and bipolar modes. In bipolar mode, one LSB is equal to the bipolar input span ($2V_{REF}$) divided by 4096. For example, when $V_{REF} = 5V$, 1LSB (bipolar) = $2(5V)/4096 = 2.44mV$.

Note 5: Linearity error is specified between the actual end points of the A/D transfer curve.

Note 6: Total unadjusted error includes offset, full scale, linearity, multiplexer and hold step errors.

Note 7: Two on-chip diodes are tied to each reference and analog input which will conduct for reference or analog input voltages one diode drop below V^- or one diode drop above V_{CC} . Be careful during testing at low V_{CC} levels (4.5V), as high level reference or analog inputs (5V) can cause this input diode to conduct, especially at elevated temperatures, and cause errors for inputs near full scale. This spec allows 50mV forward bias of either diode. This means that as long as the reference or analog input does not exceed the supply voltage by more than 50mV, the output code will be correct. To achieve an absolute 0V to 5V input voltage range will therefore require a minimum supply voltage of 4.950V over initial tolerance, temperature variations and loading.

Note 8: Channel leakage current is measured after the channel selection.

Note 9: To minimize errors caused by noise at the chip select input, the internal circuitry waits for two ACLK falling edge after a chip select falling edge is detected before responding to control input signals. Therefore, no attempt should be made to clock an address in or data out until the minimum chip select setup time has elapsed.

DIGITAL AND DC ELECTRICAL CHARACTERISTICS (Note 3)

SYMBOL	PARAMETER	CONDITIONS	LTC1290B LTC1290C			UNITS
			MIN	TYP	MAX	
V_{IH}	High Level Input Voltage	$V_{CC} = 5.25V$	●	2.0		V
V_{IL}	Low Level Input Voltage	$V_{CC} = 4.75V$	●		0.8	V
I_{IH}	High Level Input Current	$V_{IN} = V_{CC}$	●		2.5	μA
I_{IL}	Low Level Input Current	$V_{IN} = 0V$	●		-2.5	μA
V_{OH}	High Level Output Voltage	$V_{CC} = 4.75V, I_O = 10\mu A$ $I_O = 360\mu A$	●	2.4	4.7 4.0	V V
V_{OL}	Low Level Output Voltage	$V_{CC} = 4.75V, I_O = 1.6mA$	●		0.4	V
I_{OZ}	Hi-Z Output Leakage	$V_{OUT} = V_{CC}, CS \text{ High}$ $V_{OUT} = 0V, CS \text{ High}$	● ●		3 -3	μA μA
I_{SOURCE}	Output Source Current	$V_{OUT} = 0V$		-10		mA
I_{SINK}	Output Sink Current	$V_{OUT} = V_{CC}$		10		mA
I_{CC}	Positive Supply Current	$CS \text{ High}$ $CS \text{ High, Power Shutdown}$	● ●	5.0 0.005		mA mA
I^-	Negative Supply Current	$CS \text{ High}$	●	1	50	μA

PIN FUNCTIONS

#	PIN	FUNCTION	DESCRIPTION
1-8	CH0-CH7	Analog Inputs	The analog inputs must be free of noise with respect to AGND.
9	COM	Common	The common pin defines the zero reference point for all single ended inputs. It must be free of noise and is usually tied to the analog ground plane.
10	DGND	Digital Ground	This is the ground for the internal logic. Tie to the ground plane.
11	AGND	Analog Ground	AGND should be tied directly to the analog ground plane.
12	V^-	Negative Supply	Tie V^- to most negative potential in the circuit. (Ground in single supply applications.)
13, 14	REF ⁻ , REF ⁺	Reference Inputs	The reference inputs must be kept free of noise with respect to AGND.
15	CS	Chip Select Input	A logic low on this input enables data transfer.
16	D _{OUT}	Digital Data Output	The A/D conversion result is shifted out of this output.
17	D _{IN}	Data Input	The A/D configuration word is shifted into this input.
18	SCLK	Shift Clock	This clock synchronizes the serial data transfer.
19	ACLK	A/D Conversion Clock	This clock controls the A/D conversion process.
20	V _{CC}	Positive Supply	This supply must be kept free of noise and ripple by bypassing directly to the analog ground plane.

APPLICATIONS INFORMATION

The LTC1290 is a data acquisition component which contains the following functional blocks:

- 12-bit successive approximation capacitive A/D converter
- Analog multiplexer (MUX)
- Sample and hold (S/H)
- Synchronous, full duplex serial interface
- Control and timing logic

DIGITAL CONSIDERATIONS

Serial Interface

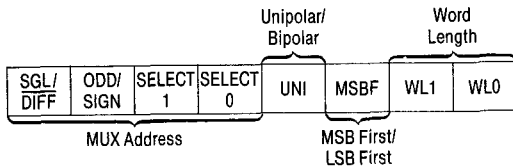
The LTC1290 communicates with microprocessors and other external circuitry via a synchronous, full duplex, four wire serial interface (see Operating Sequence). The shift clock (SCLK) synchronizes the data transfer with each bit being transmitted on the falling SCLK edge and captured on the rising SCLK edge in both transmitting and receiving systems. The data is transmitted and received simultaneously (full duplex).

APPLICATIONS INFORMATION

Data transfer is initiated by a falling chip select (\overline{CS}) signal. After the falling \overline{CS} is recognized, an 8-bit input word is shifted into the D_{IN} input which configures the LTC1290 for the next conversion. Simultaneously, the result of the previous conversion is output on the D_{OUT} line. At the end of the data exchange the requested conversion begins and \overline{CS} should be brought high. After t_{CONV} , the conversion is complete and the results will be available on the next data transfer cycle.

Input Data Word

The LTC1290 eight bit data word is clocked into the D_{IN} input on the first eight rising SCLK edges after chip select is recognized. Further inputs on the D_{IN} pin are then ignored until the next \overline{CS} cycle. The eight bits of the input word are defined as follows:



MUX Address

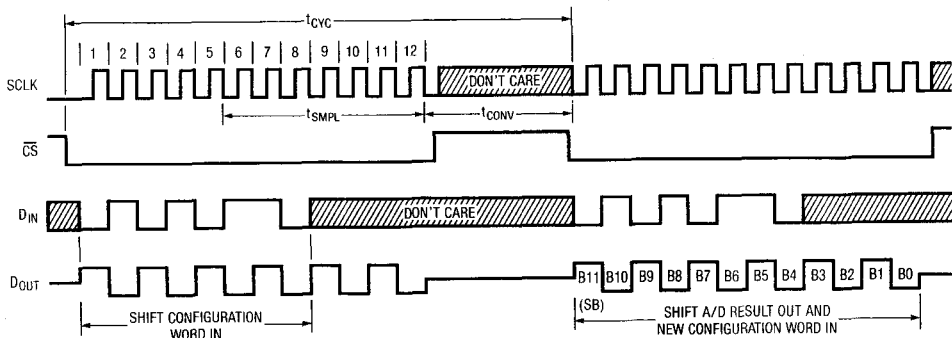
The first four bits of the input word assign the MUX configuration for the requested conversion. For a given channel selection, the converter will measure the voltage between the two channels indicated by the + and - signs

in the selected row of the following table. Note that in differential mode ($SGL/DIFF = 0$) measurements are limited to four adjacent input pairs with either polarity. In single ended mode, all input channels are measured with respect to COM.

MUX ADDRESS			DIFFERENTIAL CHANNEL SELECTION									
SGL/DIFF	ODD/SIGN	SELECT	1	0	0	1	2	3	4	5	6	7
0	0	0	0	0	+	-						
0	0	0	1			+	-					
0	0	1	0					+	-			
0	0	1	1								+	-
0	1	0	0	-	+							
0	1	0	1			-	+					
0	1	1	0						-	+		
0	1	1	1								-	+

MUX ADDRESS			SINGLE ENDED CHANNEL SELECTION										
SGL/DIFF	ODD/SIGN	SELECT	1	0	0	1	2	3	4	5	6	7	COM
1	0	0	0	0	+								-
1	0	0	1			+							-
1	0	1	0					+					-
1	0	1	1								+		-
1	1	0	0		+								-
1	1	0	1				+						-
1	1	1	0						+				-
1	1	1	1									+	-

Operating Sequence
(Example: Differential Inputs (CH3-CH2), Bipolar, MSB First and 12-Bit Word Length)



APPLICATIONS INFORMATION

Unipolar/Bipolar (UNI)

The fifth input bit (UNI) determines whether the conversion will be unipolar or bipolar. When UNI is a logical one, a unipolar conversion will be performed on the selected input voltage. When UNI is a logical zero, a bipolar conversion will result. The input span and code assignment for each conversion type are shown in the figures below.

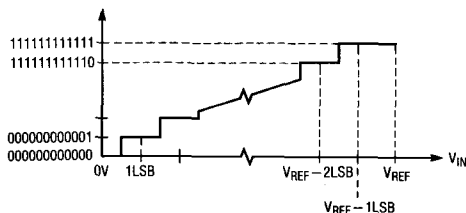
Unipolar Output Code (UNI = 1)

OUTPUT CODE	INPUT VOLTAGE	INPUT VOLTAGE ($V_{REF} = 5V$)
111111111111	$V_{REF} - 1LSB$	4.9988V
111111111110	$V_{REF} - 2LSB$	4.9976V
⋮	⋮	⋮
000000000001	1LSB	0.0012V
000000000000	0V	0V

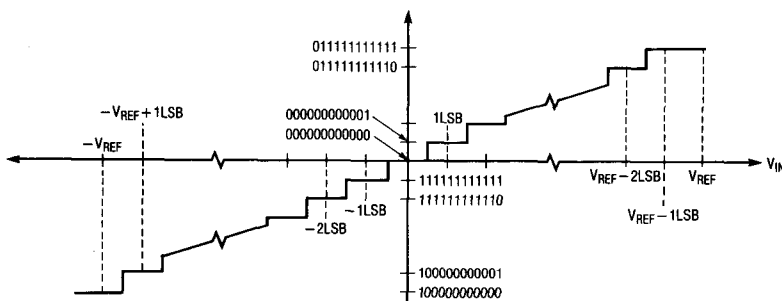
Bipolar Output Code (UNI = 0)

OUTPUT CODE	INPUT VOLTAGE	INPUT VOLTAGE ($V_{REF} = 5V$)
011111111111	$V_{REF} - 1LSB$	4.9976V
011111111110	$V_{REF} - 2LSB$	4.9851V
⋮	⋮	⋮
000000000001	1LSB	0.0024V
000000000000	0V	0V
111111111111	-1LSB	-0.0024V
111111111110	-2LSB	-0.0048V
⋮	⋮	⋮
100000000001	$-(V_{REF}) + 1LSB$	-4.9976V
100000000000	$-(V_{REF})$	-5.0000V

Unipolar Transfer Curve (UNI = 1)



Bipolar Transfer Curve (UNI = 0)



APPLICATIONS INFORMATION

MSB First/LSB First Format (MSBF)

The output data of the LTC1290 is programmed for MSB first or LSB first sequence using the MSBF bit. For MSBF first output data the input word clocked to the LTC1290 should always contain a logical one in the sixth bit location (MSBF bit). Likewise for LSB first output data the input word clocked to the LTC1290 should always contain a zero in the MSBF bit location. The MSBF bit affects only the order of the output data word. The order of the input word is unaffected by this bit.

MSBF	OUTPUT FORMAT
0	LSB First
1	MSB First

Word Length (WL1, WL0) and Power Shutdown

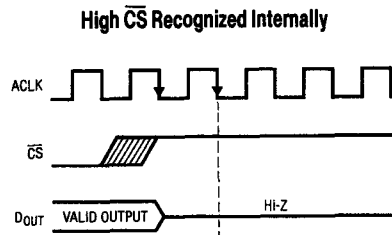
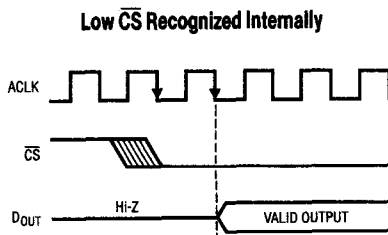
The last two bits of the input word (WL1 and WL0) program the output data word length and the power shutdown feature of the LTC1290. Word lengths of 8, 12 or 16-bits can be selected according to the following table. The WL1 and WL0 bits in a given D_{IN} word control the length of the present, not the next, D_{OUT} word. WL1 and WL0 are never "don't cares" and must be set for the correct D_{OUT} word length even when a "dummy" D_{IN} word is sent. On any

transfer cycle, the word length should be made equal to the number of SCLK cycles sent by the MPU. Power down will occur when $WL1 = 0$ and $WL0 = 1$ is selected. The previous conversion result will be clocked out as a 10-bit word so a "dummy" conversion is required before powering down the LTC1290. Conversions are resumed once \overline{CS} goes low or an SCLK is applied, if \overline{CS} is already low.

WL1	WL0	OUTPUT WORD LENGTH
0	0	8-Bits
0	1	Power Shutdown
1	0	12-Bits
1	1	16-Bits

Deglitcher

A deglitching circuit has been added to the Chip Select input of the LTC1290 to minimize the effects of errors caused by noise on that input. This circuit ignores changes in state on the \overline{CS} input that are shorter in duration than one ACLK cycle. After a change of state on the \overline{CS} input, the LTC1290 waits for two falling edge of the ACLK before recognizing a valid chip select. One indication of \overline{CS} recognition is the D_{OUT} line becoming active (leaving the Hi-Z state). Note that the deglitching applies to both the rising and falling \overline{CS} edges.



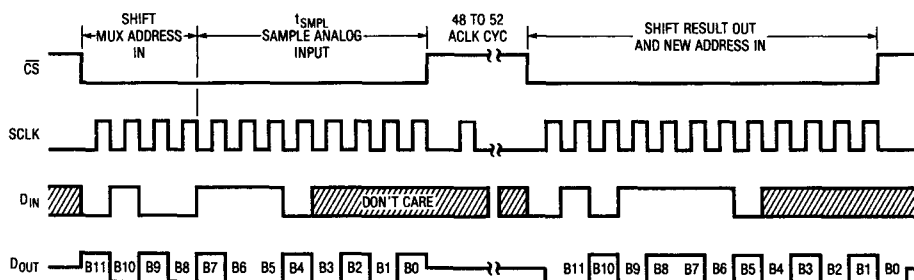
APPLICATIONS INFORMATION

\overline{CS} Low During Conversion

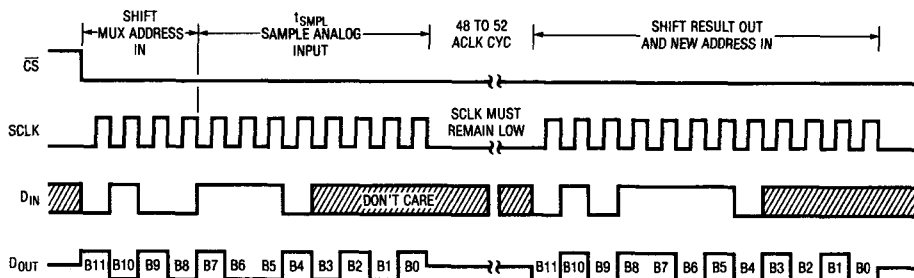
In the normal mode of operation, \overline{CS} is brought high during the conversion time. The serial port ignores any SCLK activity while \overline{CS} is high. The LTC1290 will also operate with \overline{CS} low during the conversion. In this mode, SCLK

must remain low during the conversion as shown in the following figure. After the conversion is complete, the D_{OUT} line will become active with the first output bit. Then the data transfer can begin as normal.

\overline{CS} High During Conversion



\overline{CS} Low During Conversion



1, 2, 6 and 8 Channel, 12-Bit Serial I/O Data Acquisition Systems

May 1989

FEATURES

- Programmable Features
 - Unipolar/Bipolar Conversions
 - Differential/Single Ended Multiplexer Configurations
- Sample and Hold
- Single Supply 5V, 10V or $\pm 5V$ Operation
- Direct 3 or 4 Wire Interface to Most MPU Serial Ports and All MPU Parallel I/O Ports
- Analog Inputs Common-Mode to Supply Rails
- Resolution
- Fast Conversion Time
- Low Supply Current LTC1291/2/3/4

 12 Bits
 13 μ s
 5mA Typ

12-bit, switched capacitor, successive approximation A/D core, these devices include software configurable analog multiplexers and bipolar and unipolar conversion modes as well as on chip sample and hold. On-chip serial ports allow efficient data transfer to a wide range of microprocessors and microcontrollers. These circuits can provide a complete data acquisition system in ratiometric applications or can be used with an external reference in others.

The high impedance analog inputs and the ability to operate with reduced static allow direct connection to sensors and transducers in many applications, eliminating the need for gain stages.

An efficient serial port communicates without external hardware to most MPU serial ports and all MPU parallel I/O ports allowing eight channels of data to be transmitted over as few as 3 wires. This, coupled with power shutdown (LTC1291/3/4), makes remote location possible and facilitates transmitting data through isolation barriers.

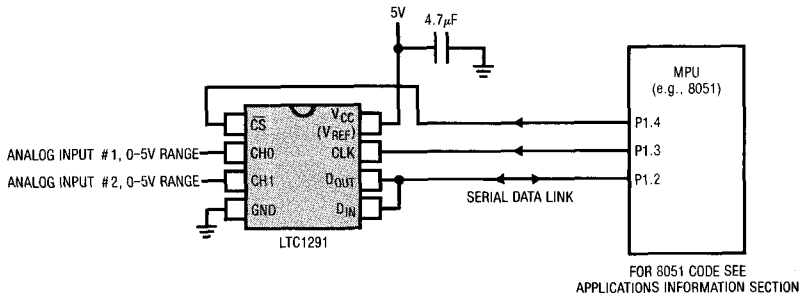
Temperature drift of offset, linearity, and full scale error are all extremely low allowing all grades to be specified with linearity errors of ± 0.5 LSB maximum over temperature.

DESCRIPTION

The LTC1291/2/3/4 12-bit data acquisition systems are designed to provide a complete function, excellent accuracy and ease of use when digitizing analog data from a wide variety of signal sources and transducers. Built around a

 REFER TO TABLE OF CONTENTS
 FOR REVISED DATA LOCATION

TYPICAL APPLICATION

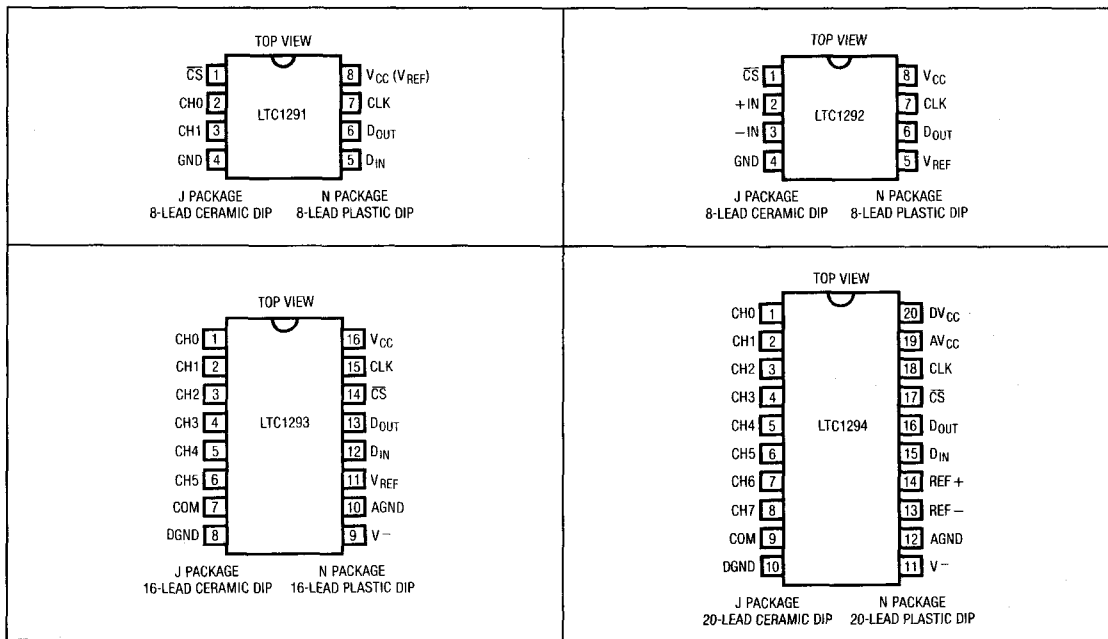


ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC}) to GND or V^- 12V
 Negative Supply Voltage (V^-) -6V to GND
 Voltage
 Analog Reference and LTC1291/2 \overline{CS}
 Inputs (V^-) -0.3V to $V_{CC} + 0.3V$
 Digital Inputs (except LTC1291/2 \overline{CS}) -0.3V to 12V
 Digital Outputs -0.3V to $V_{CC} + 0.3V$

Power Dissipation 500mW
 Operating Temperature Range
 LTC1291-4BC, LTC1291-4CC 0°C to 70°C
 LTC1291-4BI, LTC1291-4CI -40°C to 85°C
 LTC1291-4BM, LTC1291-4CM -55°C to 125°C
 Storage Temperature Range -65°C to 150°C
 Lead Temperature (Soldering, 10 sec.) 300°C

PACKAGE INFORMATION



PRODUCT GUIDE

PART NUMBER	# CHANNELS	CONVERSION MODES		REDUCED SPAN CAPABILITY (SEPARATE V_{REF})	$\pm 5V$ CAPABILITY	
		UNIPOLAR	BIPOLAR			
LTC1291	2	•				Pin for pin 12-bit upgrade of ADC0832
LTC1292	1	•		•		Pin for pin 12-bit upgrade of ADC0831
LTC1293	6	•	•	•	•	
LTC1294	8	•	•	•	•	

FEATURES

- *Guaranteed* 0.4% Initial Voltage Tolerance
- 0.1 Ω Dynamic Output Impedance
- Fast Turn-On
- Sink Current Capability, 1mA to 100mA
- Low Output Noise Voltage

APPLICATIONS

- Linear Regulators
- Adjustable Power Supplies
- Switching Power Supplies

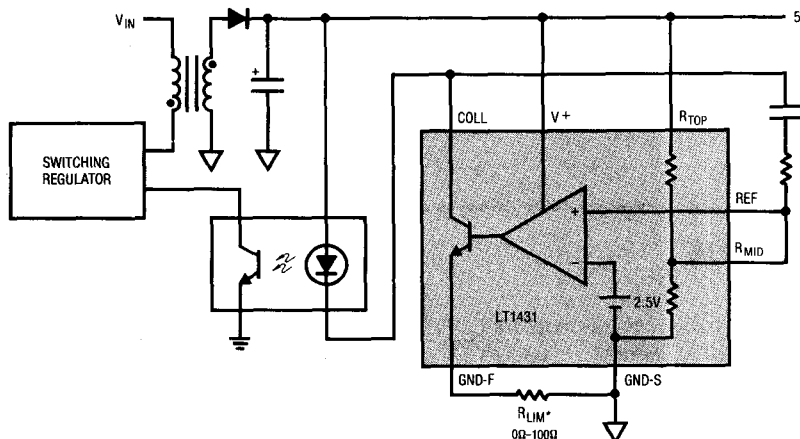
DESCRIPTION

The LT1431 is an adjustable shunt voltage regulator with 100mA sink capability, 0.4% initial reference voltage tolerance, and 1% temperature stability. On-chip divider resistors allow the LT1431 to be configured as a 5V shunt regulator with 1% initial voltage tolerance and requiring no additional external components. By adding two external resistors, the output voltage may be set to any value between 2.5V and 36V. The nominal internal current limit of 100mA may be decreased by including one external resistor.

REFER TO TABLE OF CONTENTS
FOR REVISED DATA LOCATION

TYPICAL APPLICATION

Isolated 5V Regulator



*COLLECTOR CURRENT LIMIT $\approx 600\text{mV}/(R_{LIM} + 20\Omega)$, WITH $A_{TC} OF \approx -0.3\%/^{\circ}\text{C}$

ABSOLUTE MAXIMUM RATINGS

V^+ , $V_{COLLECTOR}$	36V	
V_{COMP} , R_{TOP} , R_{MID} , V_{REF}	6V	
GND-F - GND-S	0.7V	
Ambient Temperature Range		
LT1431M	-55°C to 125°C	
LT1431C	0°C to 70°C	
Junction Temperature Range		
LT1431M	-55°C to 150°C	
LT1431C	0°C to 100°C	
Storage Temperature Range		-65°C to 150°C
Lead Temperature (Soldering, 10 sec.)		300°C

PACKAGE/ORDER INFORMATION

<p>J PACKAGE 8-LEAD CERAMIC DIP</p> <p>N PACKAGE 8-LEAD PLASTIC DIP</p>	ORDER PART NUMBER
	LT1431MJ8 LT1431CN8
<p>Z PACKAGE 3-LEAD TO-92 PLASTIC</p>	LT1431CZ

ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $I_K = 10\text{mA}$, unless otherwise specified (Note 1).

SYMBOL	PARAMETER	CONDITIONS	LT1431M			LT1431C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{REF}	Reference Voltage	$V_{KA} = 5\text{V}$, $I_K = 2\text{mA}$, (Note 2)	2490	2500	2510	2490	2500	2510	mV
			2465		2535	2480		2520	mV
$\Delta V_{REF}/\Delta T$	Reference Drift	$V_{KA} = 5\text{V}$, $I_K = 2\text{mA}$	●	50		30			ppm/°C
$\frac{\Delta V_{REF}}{\Delta V_{KA}}$	Voltage Ratio, Reference to Cathode	$I_K = 2\text{mA}$, $V_{KA} = 3\text{V}$ to 36V	●	0.2	0.5	0.2	0.5		mV/V
$ I_{REF} $	Reference Input Current	$V_{KA} = 5\text{V}$, $T_A = 25^\circ\text{C}$	●	0.2	1	0.2	1	1.2	μA
					1.5				μA
I_{MIN}	Minimum Operating Current	$V_{KA} = V_{REF}$ to 36V		0.6	1	0.6	1		mA
$ I_{OFF} $	Off-State Cathode Current	$V_{KA} = 36\text{V}$, $V_{REF} = 0\text{V}$	●		1		1		μA
					5		2		μA
$ I_{LEAK} $	Off-State Collector Leakage Current	$V_{COLL} = 36\text{V}$, $V^+ = 5\text{V}$, $V_{REF} = 2.4\text{V}$	●		1		1		μA
					5		2		μA
$ Z_{KA} $	Dynamic Impedance	$V_{KA} = V_{REF}$, $I_K = 1\text{mA}$ to 100mA , $f \leq 1\text{kHz}$			0.1		0.1		Ω
I_{LIM}	Collector Current Limit	$V_{KA} = V_{REF}$	●	100	360	100	260		mA

The ● denotes specifications which apply over the full operating temperature range.

Note 1: V_{KA} is the cathode voltage of the LT1431CZ and corresponds to V^+ of the LT1431. I_K is the cathode current of the LT1431CZ and corresponds to $(V^+) + I_{COLLECTOR}$ of the LT1431.

Note 2: The LT1431 has bias current cancellation which is effective only for $V_{KA} \geq 3\text{V}$. A slight ($\approx 2\text{mV}$) shift in reference voltage occurs when V_{KA} drops below 3V . For this reason, these tests are not performed at $V_{KA} = V_{REF}$.

Extended Temperature Range Linear ICs (200°C)

Linear Technology now offers a number of its high performance products fully characterized, tested, and with specification limits guaranteed over an extended operating temperature range of from -55°C to +200°C.

The list of extended temperature range products being offered by Linear Technology continues to grow. At the time this catalog was printed, the company offered for sale the following products.

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Op Amps:

LT1001XH Precision Op Amp
LT1007XH Low Noise, High Speed Precision Op Amp
LM101AXH Uncompensated General Purpose Op Amp
LM118XH High Slew Rate Op Amp

Precision References:

LM129XH 6.9V Precision Voltage Reference

Comparators:

LM111XH General Purpose Comparator
LM119XH High Speed Dual Comparator




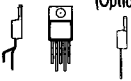

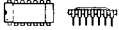




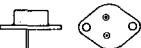
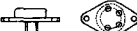



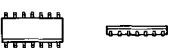
Complete specifications on Linear Technology's 200°C product offerings can be obtained from your local LTC sales representative or directly from the factory.

SECTION 14— PACKAGE DIMENSIONS

**REFER TO TABLE OF CONTENTS
FOR REVISED DATA LOCATION**

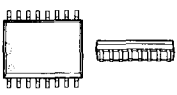
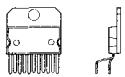
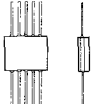
SECTION 14—PACKAGE DIMENSIONS

INDEX	14-2
Package Cross Reference	14-3
Package Dimensions	14-5

		LTC	NSC	SIG	FSC	MOT	TI	SG	AMD	RAYTH	PMI
	Plastic DIP 8 Lead	N-8	N N-8	N	T	P1	P	M	P-8	P, NB	P
	Plastic DIP 14, 16, 18, 20, 24, and 28 Lead	N	N N-14	N	P	P2	N NE NG	N	P-14 P-16	P, N	P
	TO-220 3 Lead	T	T	—	U	T	KC	P	—	—	—
	(Optional) TO-220 5 Lead	T	T	—	U	—	—	P	—	—	—
	Side Brazed Hermetic DIP 8 Lead	D-8	D	I	D	L	—	—	D-8	—	—
	Side Brazed Hermetic DIP 14, 16, 18 and 20 Lead	D	D	I	D	L	—	—	D-14 D-16 D-18	—	YB QB XB
	TO-92 3 Lead	Z	Z	—	W	—	—	—	—	—	—
	TO-5, TO-39, TO-96 TO-99, TO-100 and TO-101	H	—	—	H	—	—	T	H	T H	H J K
	Ceramic DIP 8 Lead	—	J-8	F	R	U	JG	Y	D-8	DE	Z
	Ceramic DIP 14, 16, 18, 20, 24, and 28 Lead	J	J J-14	F	D	L	J	J	D-14 D-16	DB DC J	Y Q X
	TO-3 (Steel) 2 Lead	K	K Steel	—	K	K	—	K	—	—	—
	(Aluminum)	—	K	—	K	K	—	—	—	—	—
	TO-3 4 Lead	K	K	—	K	—	—	K	—	—	—
	TO-46 3, 4 Lead	H	H	—	—	—	—	T	—	—	H J K
	TO-52 3 Lead										
	TO-3P 3 Lead	P	—	—	—	—	—	—	—	—	—
	Plastic SO 8 Lead	S-8	M	D	—	D	D	—	—	—	—
	Plastic SO 14, 16 Lead	S	M	D	—	D	D	—	—	—	—

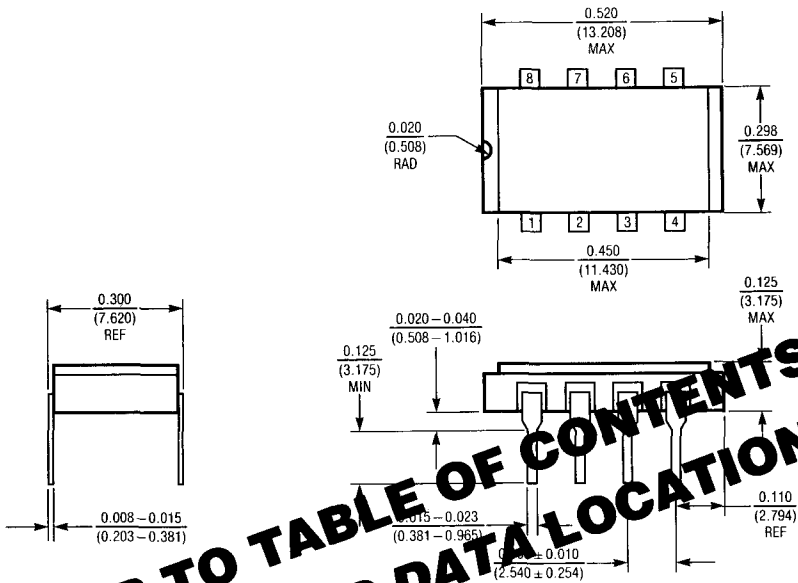
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FOR REVISED DATA LOCATION**

PACKAGE CROSS REFERENCE

		LTC	NSC	SIG	FSC	MOT	TI	SG	AMD	RAYTH	PMI
	Plastic SOL 16, 18, 20, 24, 28 Lead	S	M	D	—	D	D	—	—	—	—
	Plastic SIP 11 Lead	V	—	—	—	—	—	—	—	—	—
	10-Lead Cerpac	W	W	H	F	F	W	F	FM	—	RC
	PROPRIETARY DEVICE PREFIXES	LT LTC	LF LH LP MF LM	NE SE	μA	MC	TL	SG	AM	RM RC	OP REF CMP

**REFER TO TABLE OF CONTENTS
FOR REVISED DATA LOCATION**

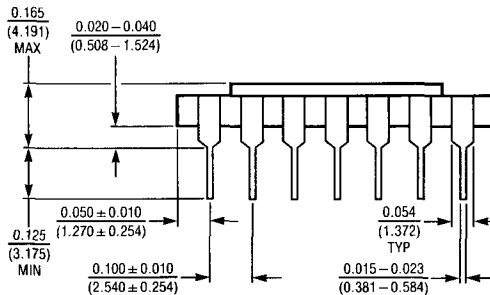
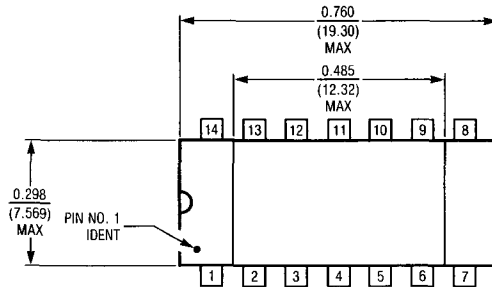
**D Package
8 Lead Sidebrazed**



06186

**REFER TO TABLE OF CONTENTS
FOR REVISED DATA LOCATION**

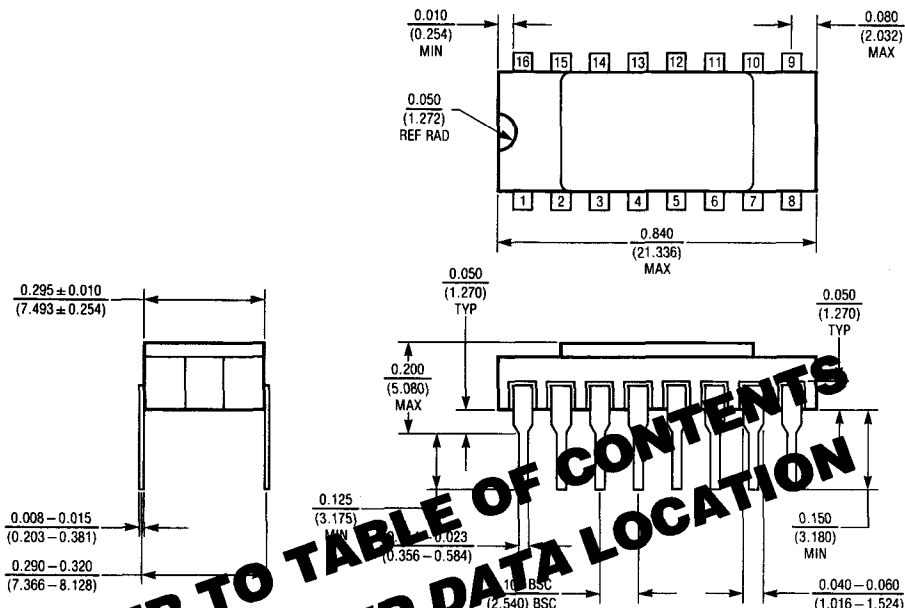
**D Package
14 Lead Sidebrazed**



D14188

PACKAGE DIMENSIONS

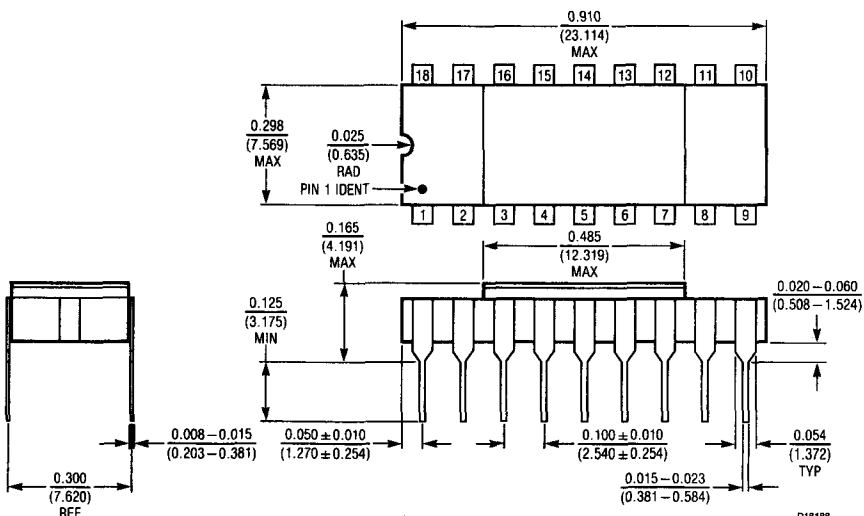
D Package 16 Lead Sidebraced



D16188

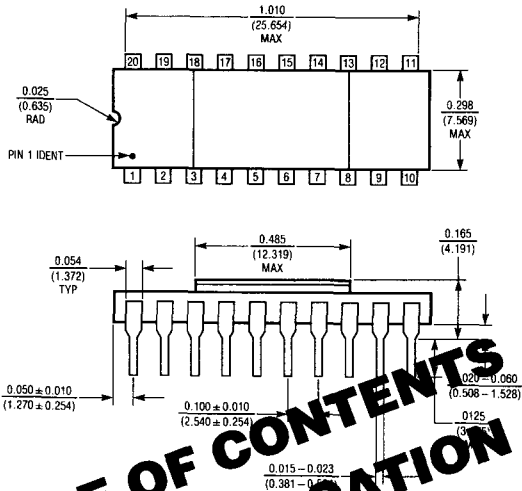
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FOR REVISED DATA LOCATION**

D Package 18 Lead Sidebraced



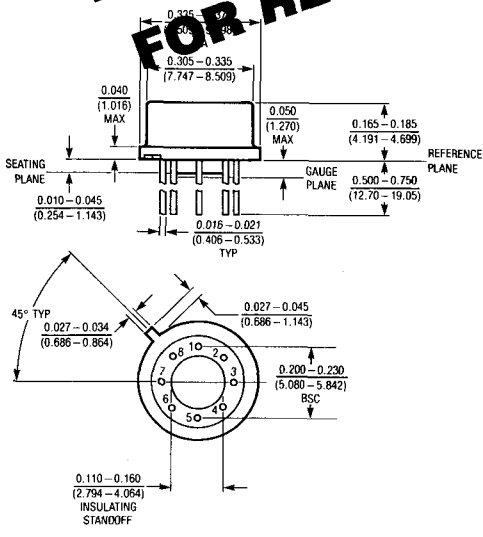
D16188

D Package 20 Lead Sidebraced



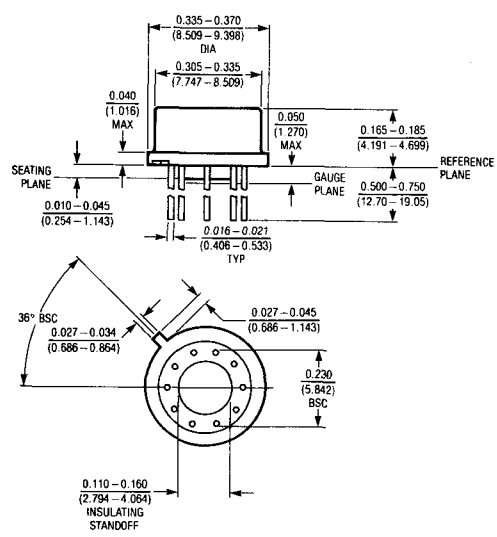
REFER TO TABLE OF CONTENTS
FOR REVISED DATA LOCATION

G Package 8 Lead TO-5 Metal Can



NOTE: LEAD DIAMETER IS UNCONTROLLED BETWEEN THE REFERENCE PLANE AND SEATING PLANE.

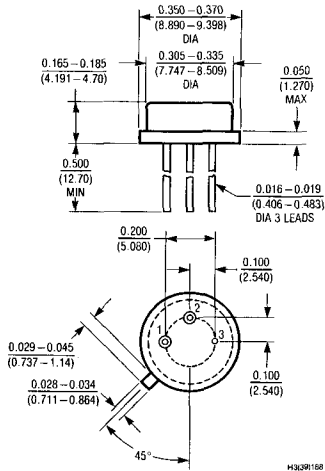
H Package 10 Lead TO-5 Metal Can



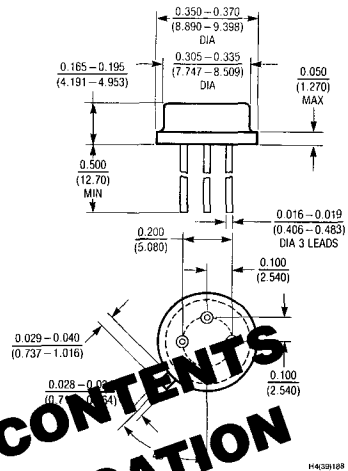
NOTE:
1. LEAD DIAMETER IS UNCONTROLLED BETWEEN THE REFERENCE PLANE AND SEATING PLANE.

PACKAGE DIMENSIONS

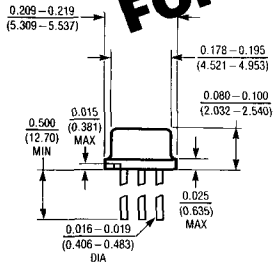
**H Package
3 Lead TO-39 Metal Can**



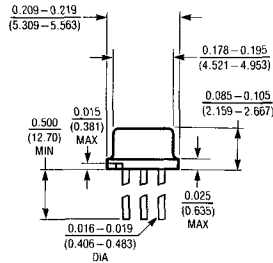
**H Package
4 Lead TO-39 Metal Can**



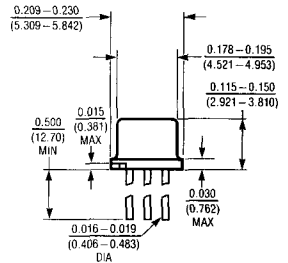
**H Package
3 Lead TO-46 Metal Can**



**H Package
4 Lead TO-46 Metal Can**

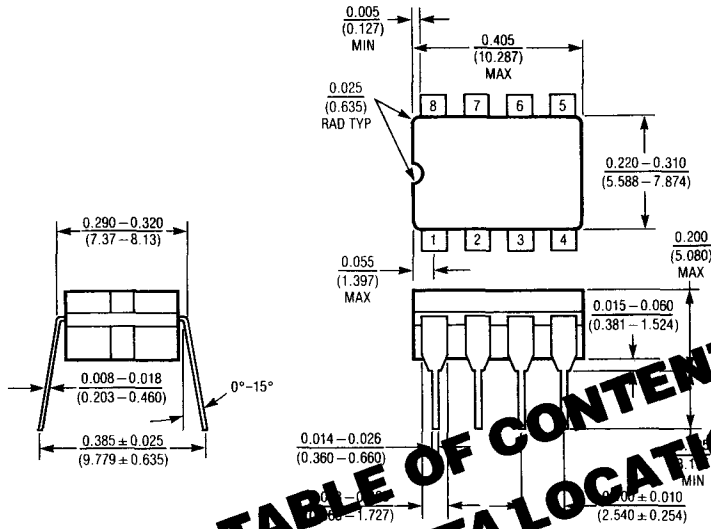


**H Package
3-Lead TO-52 Metal Can**



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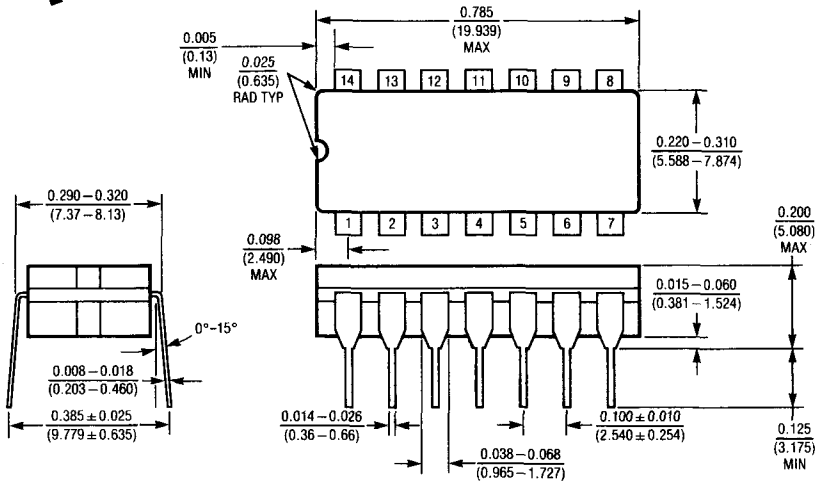
**J Package
8 Lead Cerdip**



J8188

**REFER TO TABLE OF CONTENTS
FOR REVISED DATA LOCATION**

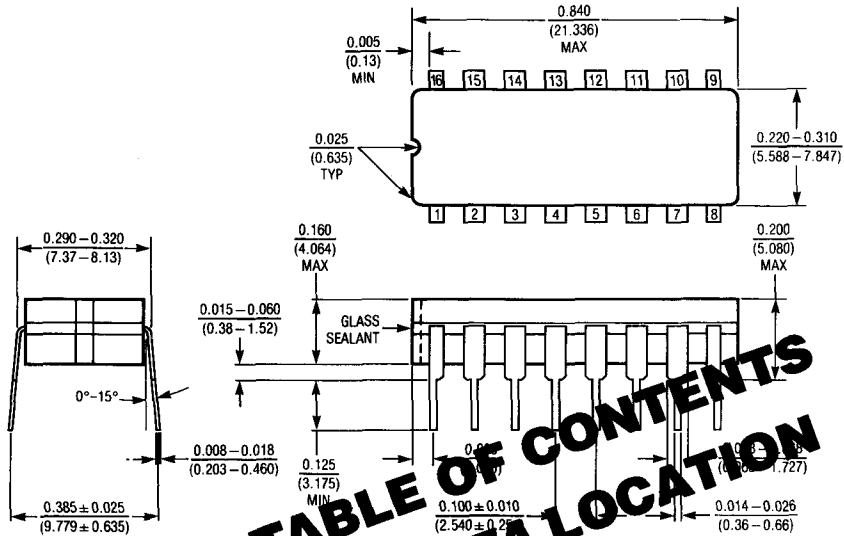
**J Package
14 Lead Cerdip**



J14180

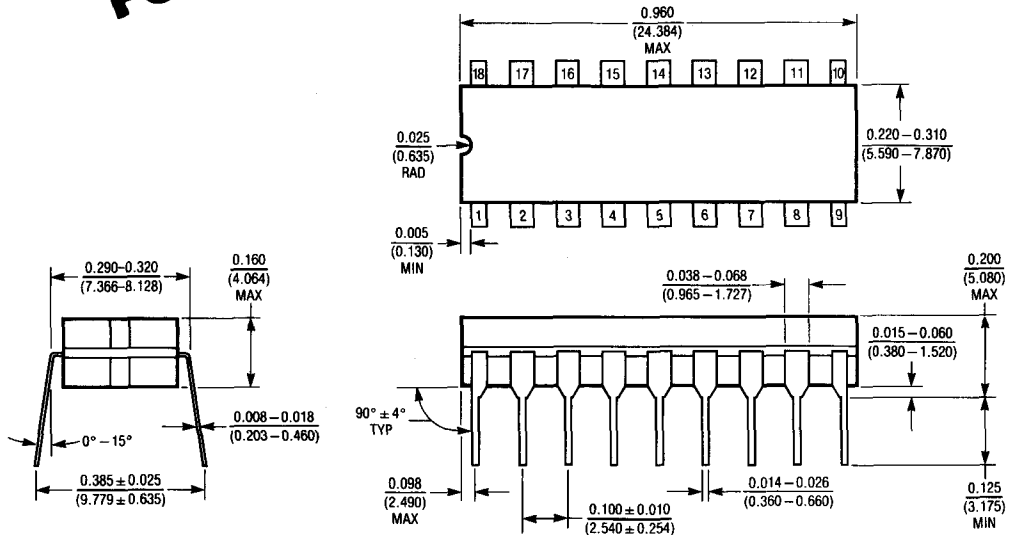
PACKAGE DIMENSIONS

**J Package
16 Lead Cerdip**

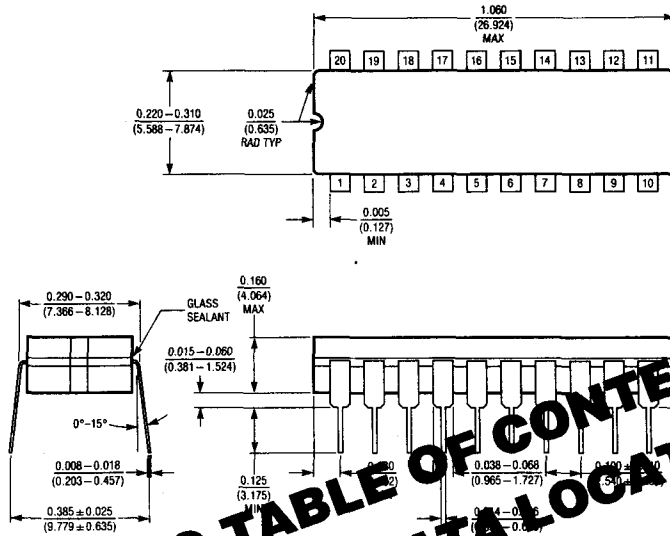


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**J Package
18 Lead Cerdip**

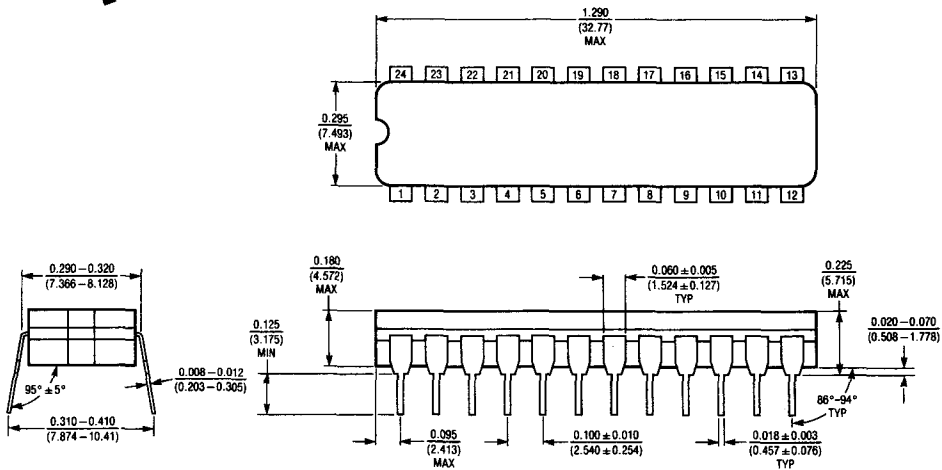


J Package
20 Lead Cerdip



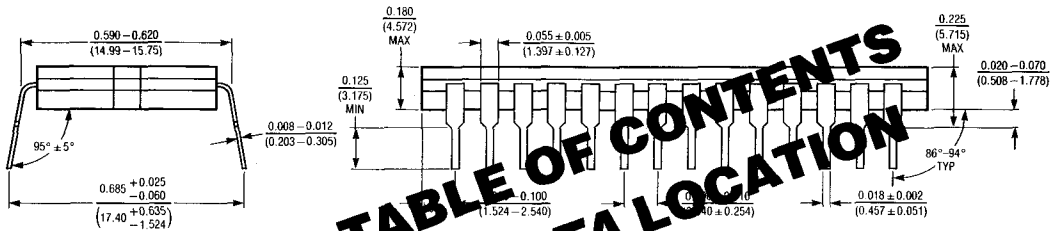
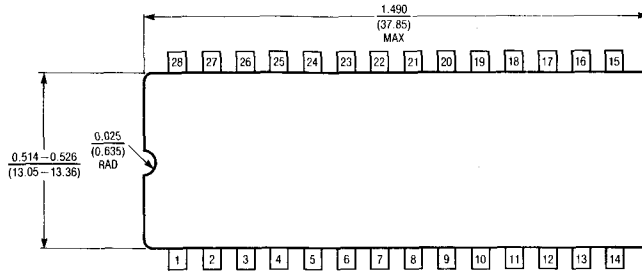
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FOR REVISED DATA LOCATION**

J Package
24 Lead Cerdip



PACKAGE DIMENSIONS

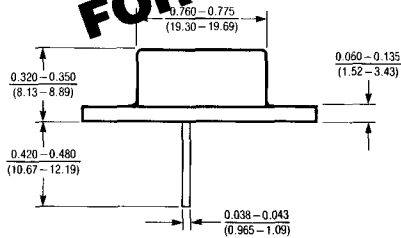
J Package
28 Lead Cerdip



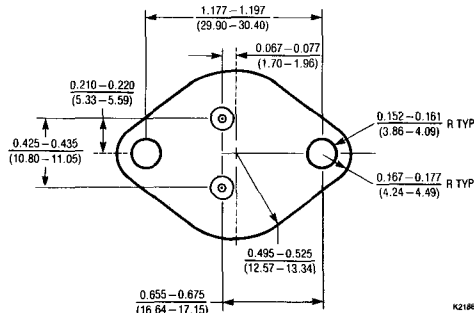
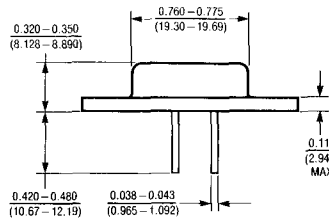
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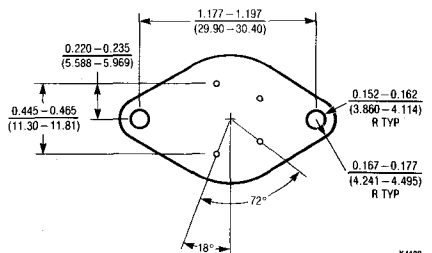
K Package
2 Lead TO-3 Metal Can



K Package
4 Lead TO-3 Metal Can

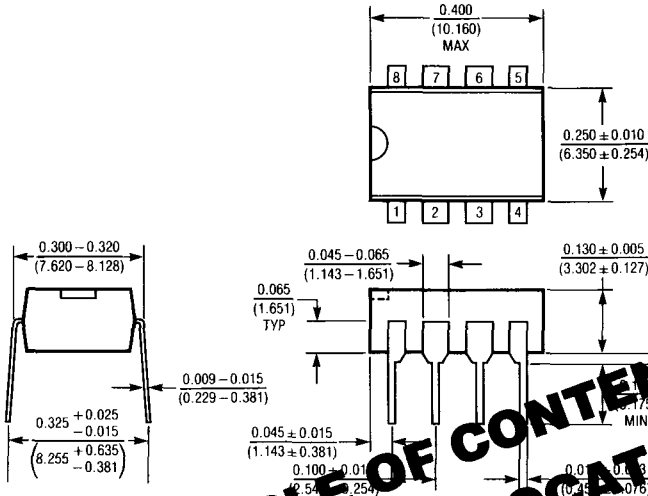


K2188



K4188

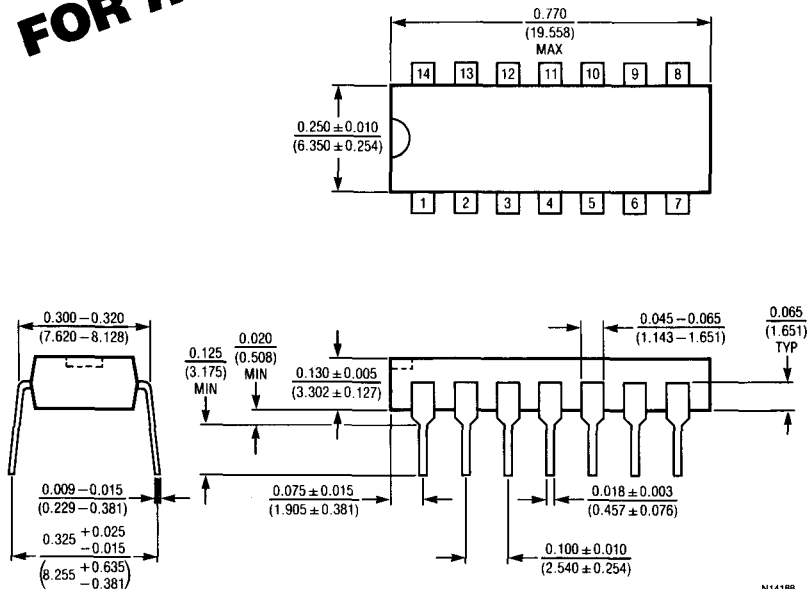
N Package
8 Lead Molded DIP



N8186

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FOR REVISED DATA LOCATION**

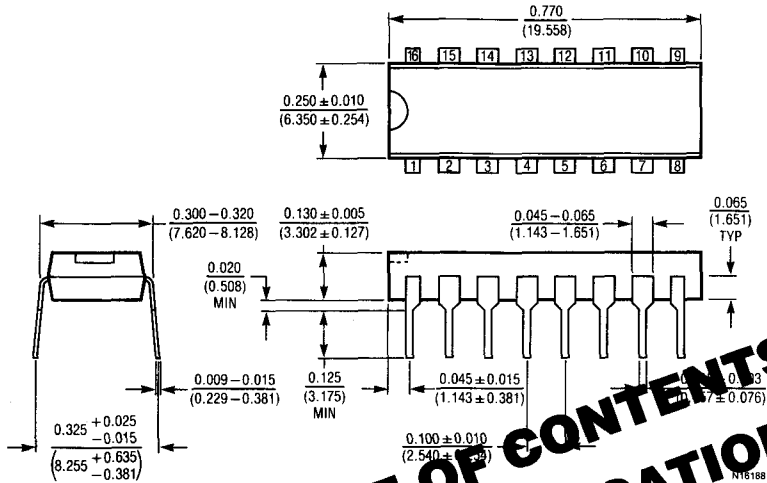
N Package
14 Lead Molded DIP



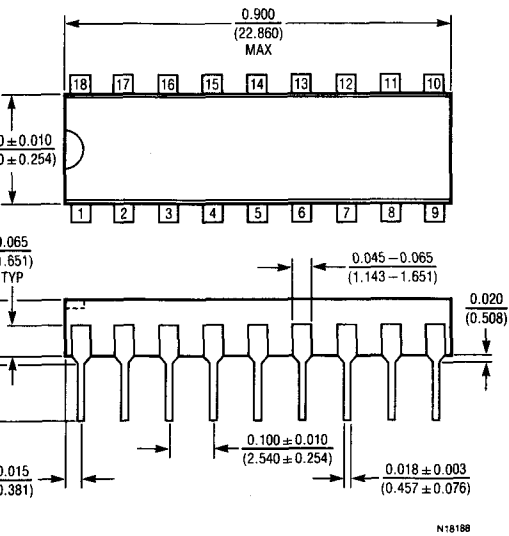
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PACKAGE DIMENSIONS

N Package 16 Lead Molded DIP

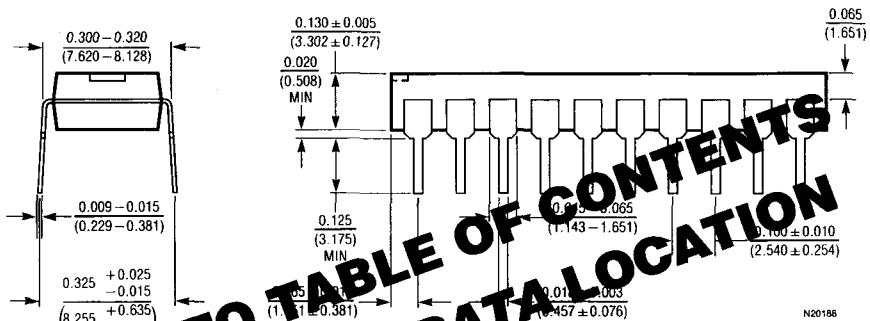
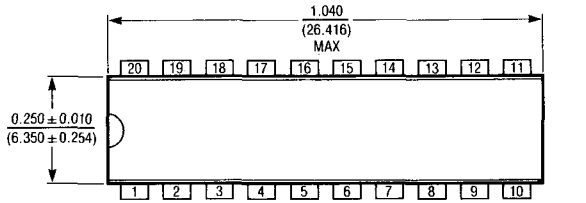


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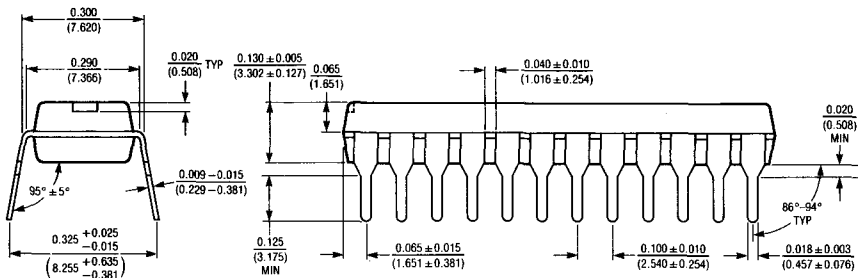
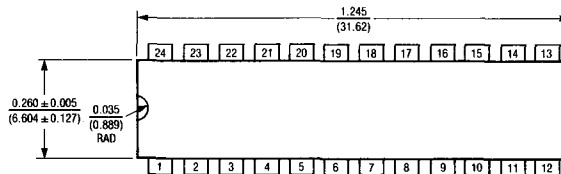
PACKAGE DIMENSIONS

N Package
20 Lead Molded DIP



N20188

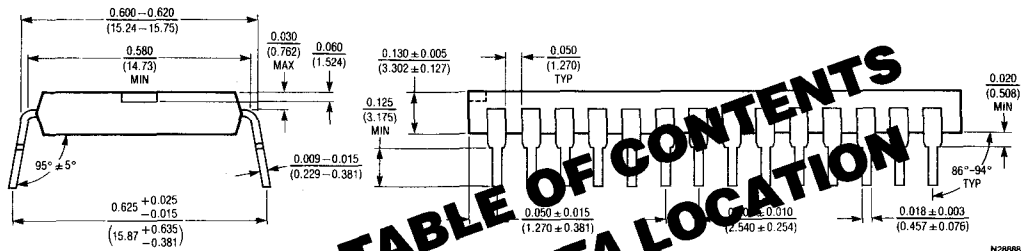
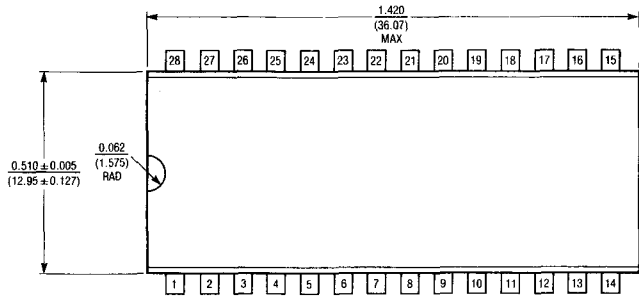
N Package
24 Lead Molded DIP



N24888

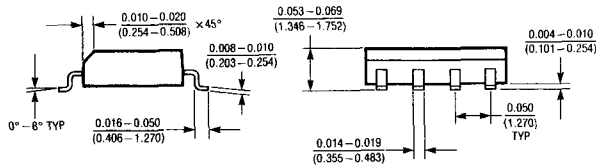
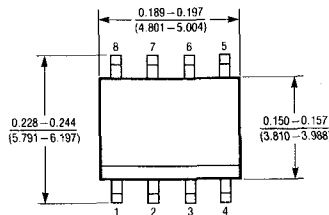
PACKAGE DIMENSIONS

N Package 28 Lead Molded DIP



**REFER TO TABLE OF CONTENTS
FOR REVISED DATA LOCATION**

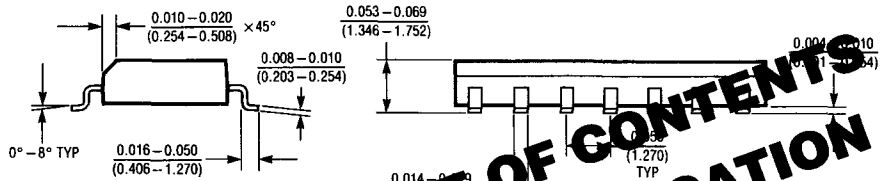
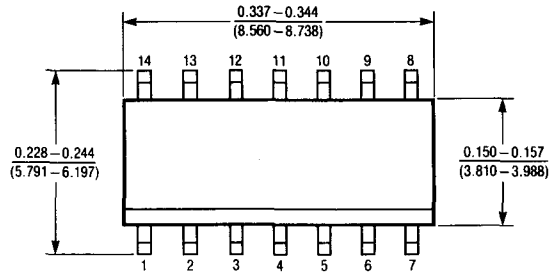
SO Package 8 Lead Small Outline



- NOTES:
1. PKG MATERIAL: PLASTIC
2. LEAD MATERIAL: A-42, TIN PLATED

58188

SO Package
14 Lead Small Outline

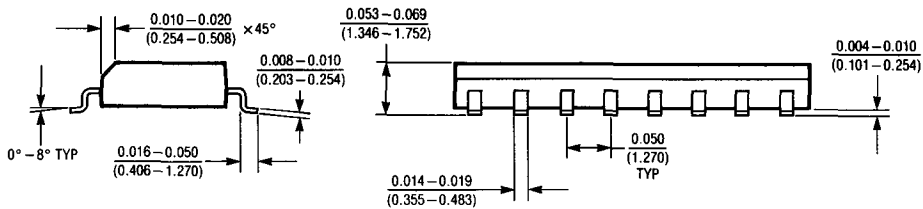
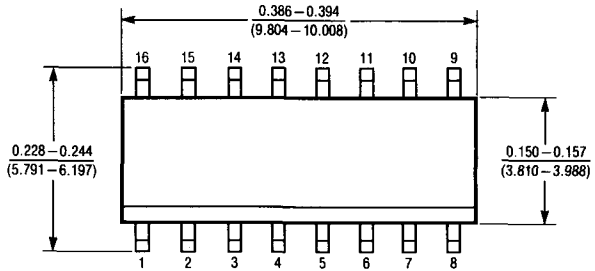


**REFER TO TABLE OF CONTENTS
FOR REVISED DATA LOCATION**

1. PKG MATERIAL: PLASTIC
2. LEAD MATERIAL: A-42, TIN PLATED

S14188

SO Package
16 Lead Small Outline

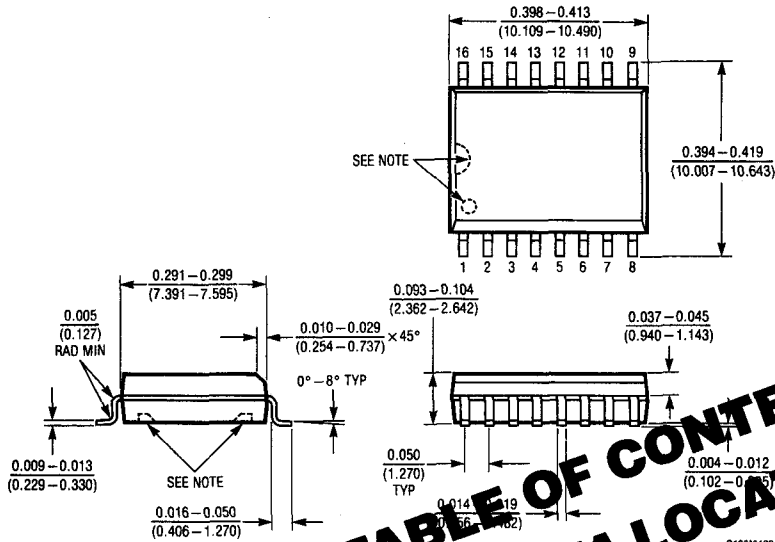


- NOTES:
1. PKG MATERIAL: PLASTIC
2. LEAD MATERIAL: A-42, TIN PLATED

S16188

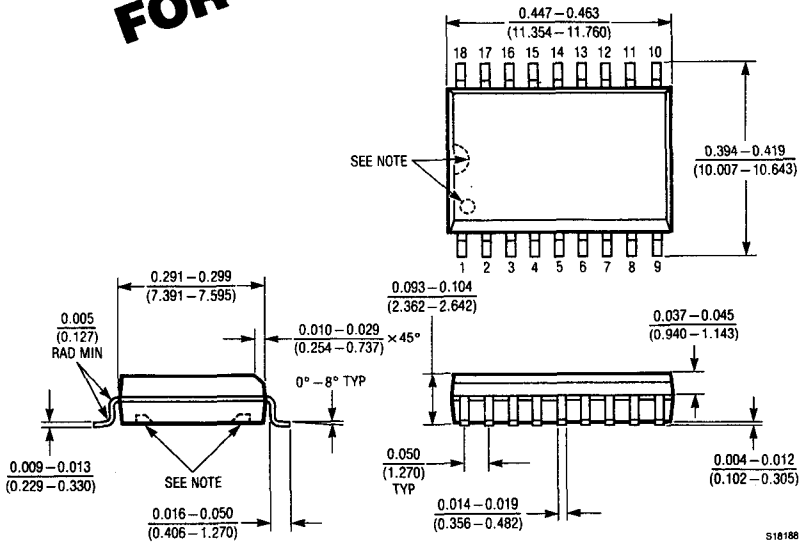
PACKAGE DIMENSIONS

SOL Package
16 Lead Small Outline (Wide)



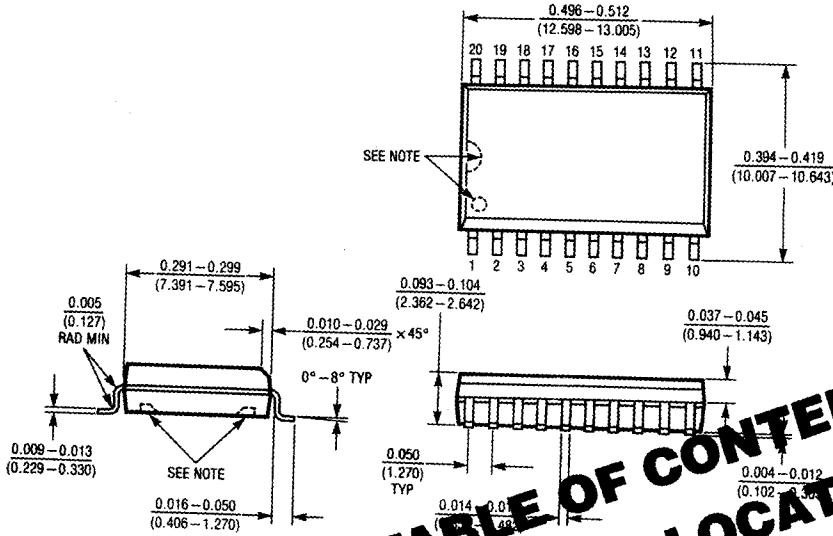
REFER TO TABLE OF CONTENTS FOR REVISED DATA LOCATION

SOL Package
18 Lead Small Outline (Wide)



PACKAGE DIMENSIONS

SOL Package 20 Lead Small Outline (Wide)

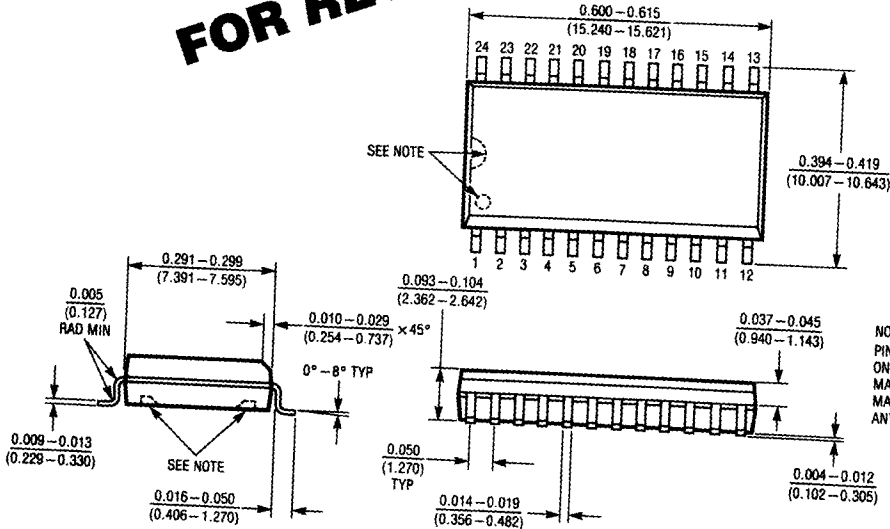


NOTE:
PIN 1 IDENT. NOTCH ON TOP AND CAVITIES ON THE BOTTOM OF PACKAGE ARE THE MANUFACTURING OPTIONS. THE PART MAY BE SUPPLIED WITH OR WITHOUT ANY OF THE OPTIONS.

S20188

REFER TO TABLE OF CONTENTS FOR REVISED DATA LOCATION

SO Package 24 Lead Small Outline (Wide)

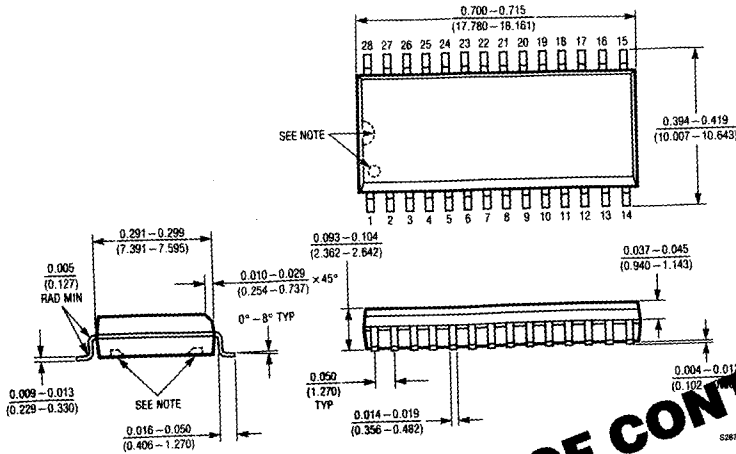


NOTE:
PIN 1 IDENT. NOTCH ON THE BOTTOM OF PACKAGE ARE THE MANUFACTURING OPTIONS. THE PART MAY BE SUPPLIED WITH OR WITHOUT ANY OF THE OPTIONS.

S24789

PACKAGE DIMENSIONS

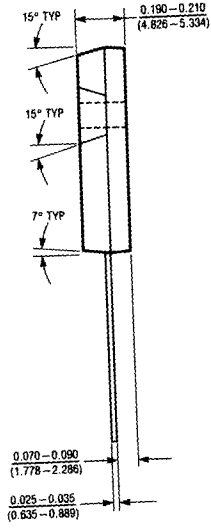
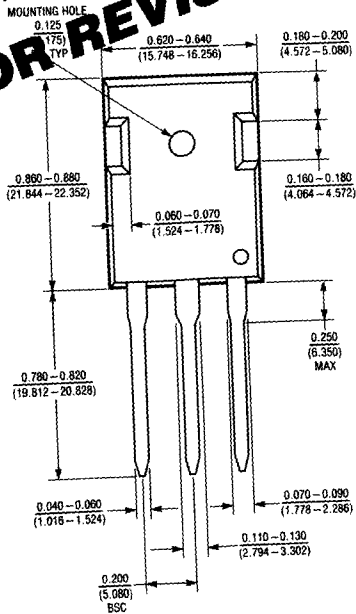
SOL Package 28 Lead Small Outline (Wide)



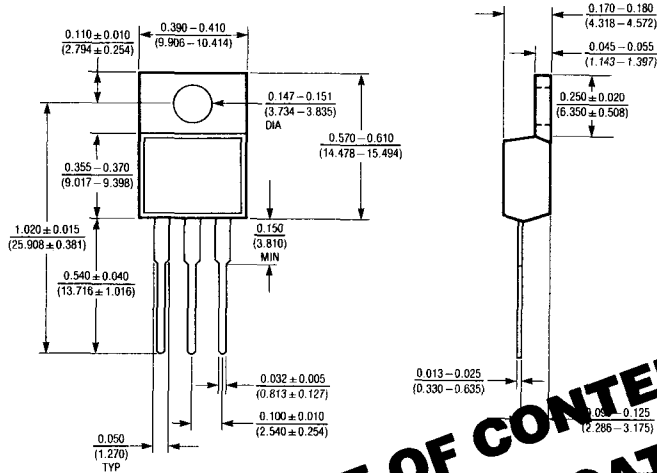
NOTE:
DIMENSIONS ON TOP AND CAVITIES
OF PACKAGE ARE THE
MANUFACTURING OPTIONS. THE PART
MAY BE SUPPLIED WITH OR WITHOUT
ANY OF THE OPTIONS.

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FOR REVISED DATA LOCATION**

P Package
Lead 247

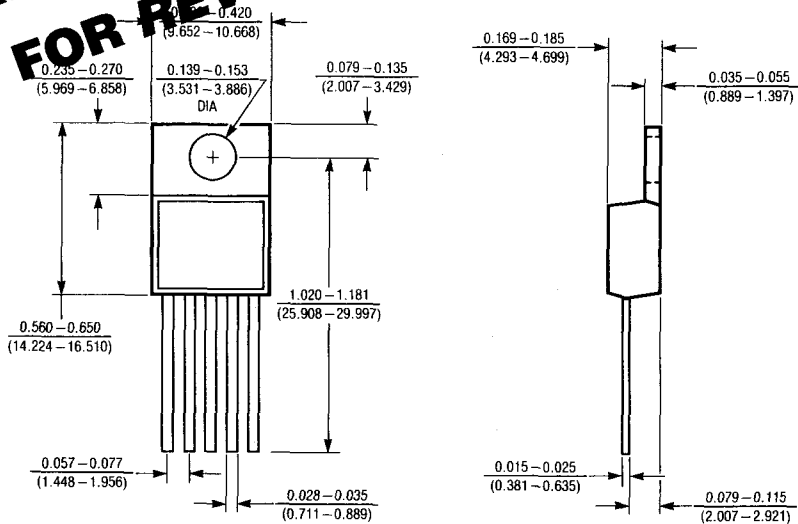


T Package
3-Lead TO-220



**REFER TO TABLE OF CONTENTS
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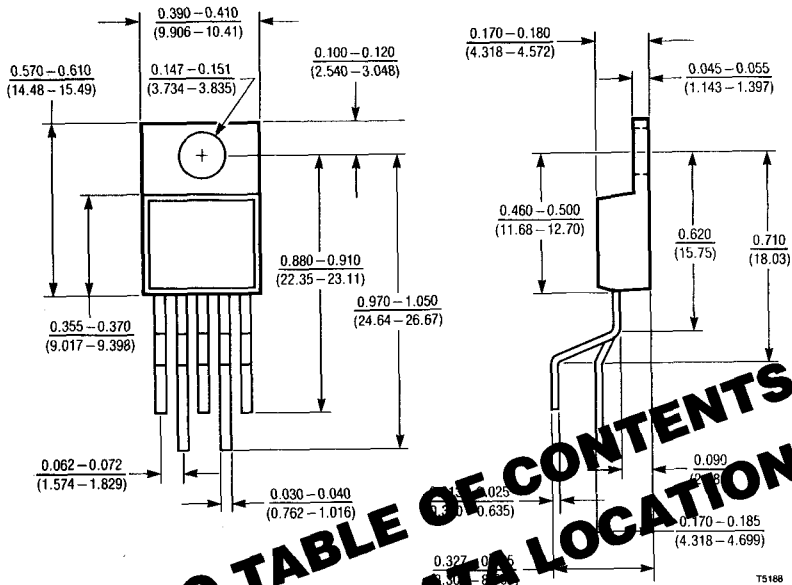
T Package
3-Lead TO-220 (Straight Lead)



T5(6)269

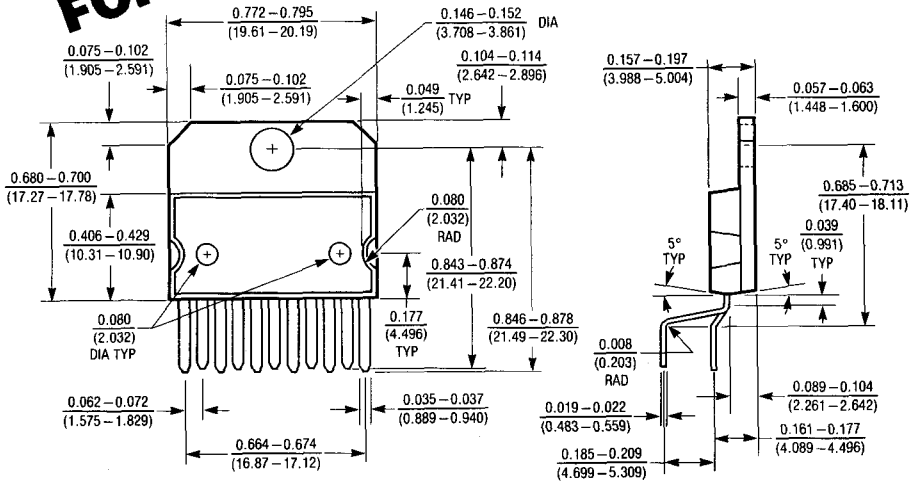
PACKAGE DIMENSIONS

T Package
5 Lead TO-220



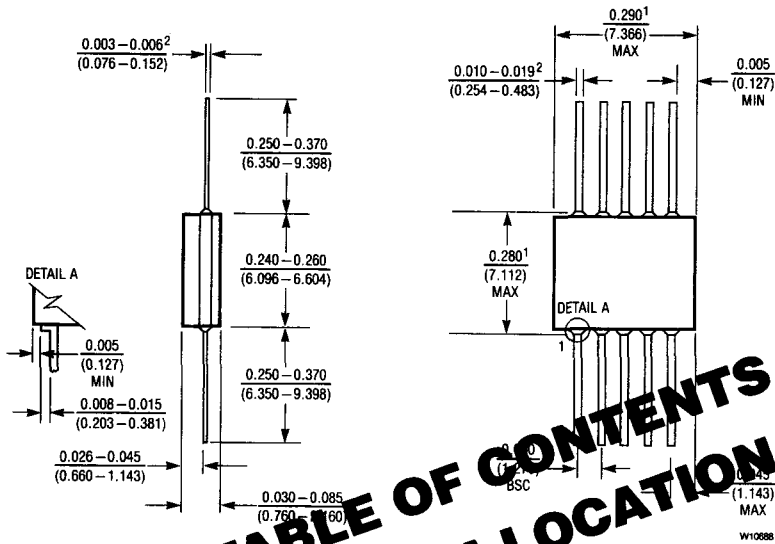
**REFER TO TABLE OF CONTENTS
FOR REVISED DATA LOCATION**

V Package
11 Lead Molded SIP



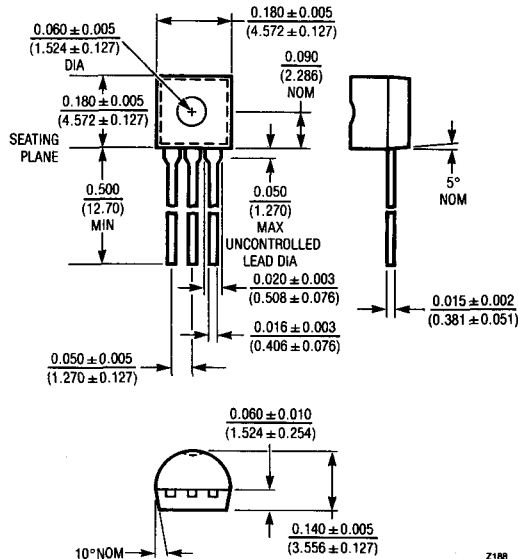
PACKAGE DIMENSIONS

W Package 10 Lead Flatpack (Cerpak)



**REFER TO TABLE OF CONTENTS
FOR REVISED DATA LOCATION**

Z Package 3-Lead TO-92



NOTES

SECTION 15— APPENDICES

**REFER TO TABLE OF CONTENTS
FOR REVISED DATA LOCATION**

SECTION 15—APPENDICES

INDEX	15-2
Introduction to Quality and Reliability Assurance Programs	15-3
Reliability Assurance Program	15-5
Quality Assurance Program	15-13
R-Flow	15-21
ESD Protection Program	15-23
Surface Mount Products	15-35
Surface Mount Parts List	15-43
Dice Products	15-45
Application Notes Index	15-47

Quality and Reliability Assurance Programs

Linear Technology Corporation has a wide ranging program integrating vendor participation, design engineering, and manufacturing to produce the most reliable and highest quality linear integrated circuits available on the market. Our modern manufacturing facility in Milpitas, California is DESC Class S and Class B line certified and we have successfully completed over 70 major OEM quality system surveys to MIL-Q-9858 and MIL-I-45208 including achieving several major customer quality awards. Our Quality and Reliability Assurance Programs are summarized below:

- **Wafer Fabrication**—A modern class 100 area, modular clean room construction with full environmental monitors. Emphasis is placed on statistical quality control, CV plots, SEM monitors and on our proprietary dual layer passivation system.
- **Assembly & End of Line**—Incoming inspection of all materials and piece-parts, line surveillance and process control monitors.
- **Testing**—Incoming inspection and acceptance of all off-shore lots prior to release to test. Ultra modern LTX testers, multipass testing with closed loop binning to reduce outgoing electrical defective levels. Many “beyond data sheet” tests and full temperature QA lot buy-offs are performed as standard processing.
- **Traceability**—A backside or side mark is placed on all units, where space permits, to give information on a unit-by-unit basis tracing back to the wafer fab lot, assembly, end of line (e.o.l.) and test lots. We consider traceability to be essential for good engineering control and additional insurance for our customers. The information provided exceeds the seal week traceability control required by MIL-STD-883.
- **ESD (Electro Static Discharge)**—A full program is in place from design through manufacturing. Products are fully characterized to MIL-STD-883C (Method 3015) and strict controls on handling and packaging are observed.
- **Training and Certification**—Operator training has been established for all operations and certification is performed on a 6 monthly basis.
- **Major Change Control**—Major change controls are in place to notify our customers in accordance with MIL-M-38510, LTC internal specifications, or specific customer specifications as required.
- **Quality Assurance**—Full monitoring and reporting of quality data with emphasis on statistical process control charts. Refer to our Quality Assurance Program.
- **Failure Analysis and Reporting**—A formal program exists to record, analyze and take appropriate corrective action on all returns. A report is generated and sent to the customer stating our findings and action.
- **Reliability Flows**—Linear Technology reliability flows include Class S and Class B JAN-38510, Standard Military Drawings (SMD), DESC Drawings, 883 (to the new Rev. C) R-Flow, and Hi-Rel (Source Controlled Drawings). In addition, specialized processing such as SEM, PIND and other tests can be performed as required.
- **Reliability Monitor**—LTC has a unique reliability structure built into each wafer that is used to obtain rapid feedback on reliability. This data is obtained in less than 1 week, versus 40 weeks for a typical reliability audit. See the LTC Reliability Program for more details.
- **Reliability Audit**—Data is gathered on a monthly basis for selected package/product combinations. This data is summarized each quarter and published in a Data Pak showing Operating Life, 85/85, Autoclave, Temperature Cycle, Thermal Shock, 883 Group C, and 883 Group D summary data. Copies of Data Pak summaries are available by writing or calling Linear Technology, 1630 McCarthy Blvd., Milpitas, CA 95035, (408) 942-0810.

NOTES

Introduction

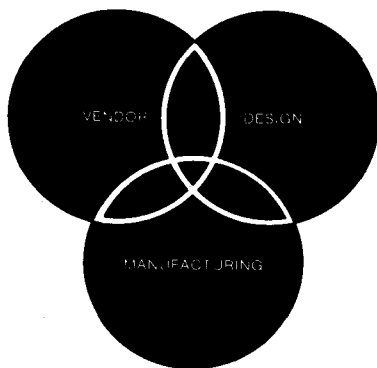
In the early 1960's the study of reliability was mainly the province of mathematicians and statisticians. In the late 1960's and throughout the 1970's it was realized that an understanding of the physical phenomena was necessary to identify the various failure mechanisms and considerable progress was made in this area. Sophisticated diagnostic techniques were devised and this knowledge complemented the earlier theoretical work to form a very sound foundation.

At Linear Technology Corporation we have a firm appreciation for the impact of Reliability on our products and we have made every effort to integrate this knowledge into our device designs and manufacturing processes. We believe that "LINEAR" should be "THE MOST RELIABLE COMPONENTS" and it is our intention to supply "TOMORROW'S RELIABILITY—TODAY"!

All areas that impact reliability have received considerable attention and achieving our goal of "THE NUMBER ONE" Reliability Supplier of Analog Circuits has impacted the DESIGN, FABRICATION, PACKAGING AND TESTING of our products.

"RELIABILITY" requires a total systems approach involving all parties; from the raw material vendor, to the designer, to manufacturing.

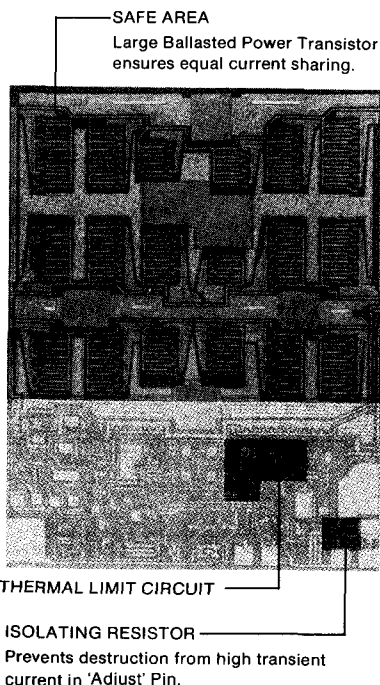
Cooperative Interface



Design

At the DESIGN stage the reliability of the circuit is heavily dependent on layout considerations. The thickness and width of the metallization has been defined to minimize the current density and avoid electromigration problems at elevated temperatures. The routing of the metal pattern is designed to eliminate potential inversion, or leakage failures and guard ring structures are used where appropriate. The positions of the bonding pads are carefully selected to optimize device performance and also to fit easily into a variety of packages without creating potential bond loop problems that could result in shorted wires. In all of our voltage regulators, thermal limiting is included in the circuitry to shut down the device if the temperature exceeds a threshold value. Additional insurance is provided by employing short circuit current protection to safeguard catastrophic failure. The philosophy of incorporating fault tolerant designs with innovative circuit concepts is a fundamental design rule at Linear Technology

5 Amp Positive Adjustable Regulator



RELIABILITY ASSURANCE PROGRAM

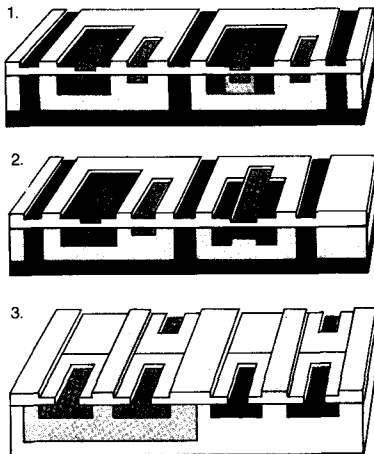
Corporation. The design rules used by Linear Technology are conservative to avoid compromising reliability, and safe operation regions are chosen to prolong device life in the field. Input protection is provided and the ability of our devices to withstand transient voltage spikes is better than average. We focus on reducing lead count of our device designs since there is generally a strong correlation between the number of leads in a package and the mean time between failures for a device. The thermal layout of our circuits is also a major consideration to minimize parameter drift and optimize performance. The designs at Linear Technology Corporation cover a diverse technological base ranging from Bipolar to CMOS. In the case of CMOS, design techniques are used to minimize SCR and latch-up phenomena. Many integrated circuit designs are susceptible to electrostatic discharge effects (ESD) and electrical overstress (EOS) with generally catastrophic results. In the designs at Linear Technology Corporation, care is taken to ensure that a high degree of protection is built into our products to minimize this effect.

Prior to release, new devices are thoroughly characterized and subjected to rigorous mechanical and electrical stress testing to exercise all facets of the design, process, and package combination. Linear Technology Corporation has an active in-house ESD (Electrostatic Discharge) program to prevent yield loss and the potential weakening on devices.

Wafer Fabrication

In the WAFER FABRICATION area the key to a reliable process is consistency and repeatability. Linear Technology has a brand new ultramodern wafer fabrication facility and wafer handling has been kept to a minimum. Cassette to cassette transfer is used extensively and proximity mode aligners are utilized in masking to significantly reduce photomasking defects. Microprocessor controlled furnaces are used to eliminate the impact of operator error.

Diverse Range of Processes

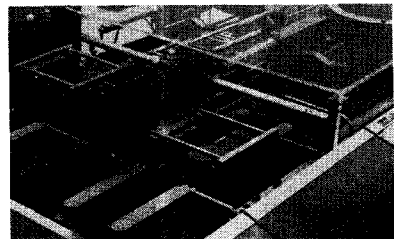


1. Super Beta Structure
2. Bi-fet Structure
3. Silicon Gate CMOS Structure

Cassette to Cassette Transfer



Canon Proximity Aligner



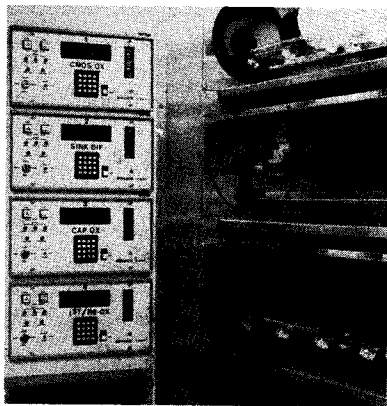
Stringent incoming inspection checks are made on the raw silicon wafers and masks used in the process. Environmental monitoring of the gases, clean air, particle count, deionized water, and furnace temperature and flows are done on a routine basis to avoid any sudden changes that could impact device reliability.

Quality Control checks at various points in the process ensure consistency and control charting is used extensively throughout the fabrication area. The quality of the oxide is checked regularly using C-V plots to check for contamination and surface state anomalies and processes are not operational until minimum requirements are met. Each wafer contains diagnostic structures in addition to the device structures and these test vehicles are used to investigate and detect potential yield and reliability hazards in advance. Scanning electron microscope pictures are taken periodically to check the integrity of the metallization system. Emphasis is given to the early detection of step coverage or misalignment problems. A proprietary passivation system has been developed that will enable

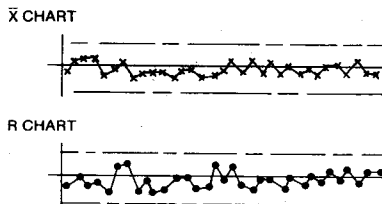
our die to operate in a variety of plastic packages and the nature of this unique multilayer system will make the die virtually impervious to the packaging medium.

The strategy of Linear Technology in developing its process is to make the chip as impervious as possible to moisture and ionic contaminants. This approach assures reliable operation even in marginal environments. The Linear Technology process offers several layers of protection. 1) Extensive CV monitoring of all diffusion tubes and deposition systems assure underlying oxides with low levels of positive ionic contamination. Phosphorous gettering ties up these ions in an inactive state. 2) A proprietary deposited oxide gives conformal coverage of metal and oxide steps, and is free of cracks. 3) A plasma nitride overcoat protects the die from external ionic contamination during handling, testing and assembly. The dual nitride/oxide layer is completely free of cracks and pinholes which enhance corrosion protection against moisture contamination.

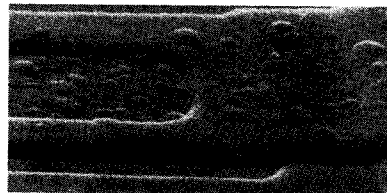
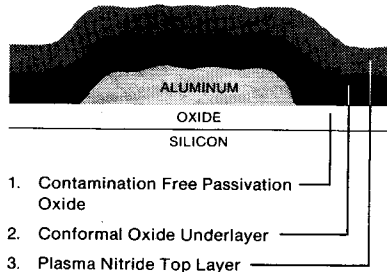
Microprocessor Controlled Furnaces



Control Chart



Passivation Process



RELIABILITY ASSURANCE PROGRAM

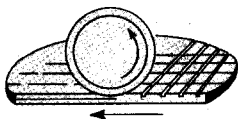
Packaging

The impact of new equipment, techniques and materials have had a tremendous impact on device reliability. In the area of wafer scribing, sawing of the wafers has decreased device chipping and cracking significantly. The handling of dice at second optical inspection and die attach is now mainly automated, removing the need to use tweezers and the resultant damage due to this operation. Automated lead bonding machines have produced tremendous gains in productivity but as importantly more consistent lead bonds have resulted from this new innovation. Die attach materials have improved and modern low temperature glass ceramic seals have dramatically increased product reliability. At Linear Technology we are using the latest state-of-the-art assembly equipment and materials. Our epoxy material has the lowest sodium and chlorine content of any molding compound available and the data on operating life, power cycling and pressure pot is outstanding. Compossibility between the different package elements, such as the molding compound and lead frame,

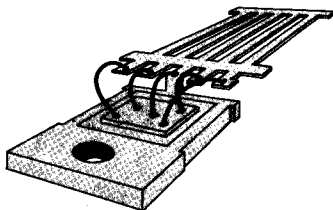
are carefully researched and selected particularly on our surface mount packages to achieve the highest reliability after board soldering. All materials are inspected to better than industry standards prior to use and strict QC checks are performed on-line to assure control and conformance to specifications. At LTC traceability to a fabrication lot is considered to be of primary importance. On all packages where space allows a side mark or a backside mark is used to give this key information. We are able to track the country of origin, assembly location, die type, wafer fab lot, exact seal date and also identify non standard processing if required on a special flow. This unique benefit is offered as a standard feature at no additional cost and adds immensely to the level of control and traceability on Linear Technology products.

Mil-Standard 883 Method 2010 Condition B or equivalent visual criteria are applied to all Linear Technology products and a thorough inspection of all lots received from our assembly operations in Southeast Asia is performed prior to testing. A system of effective and rapid communications exist between our operation in Milpitas, California and Southeast Asia to analyze and correct any assembly or process related problems before the product is shipped to the customer. Precautions are taken throughout the assembly process to minimize the impact of ESD (Electrostatic Discharge) on our devices.

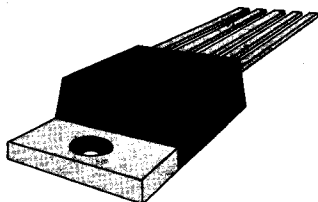
Wafer Saw



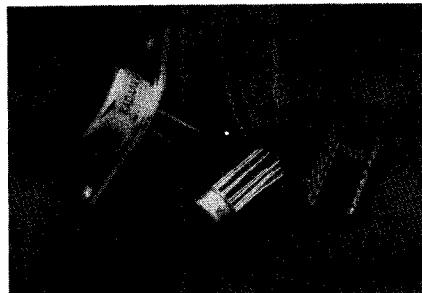
Die Attached and Wire Bonded Unit



Encapsulated and Finished Unit



Side/Backside Mark on Unit

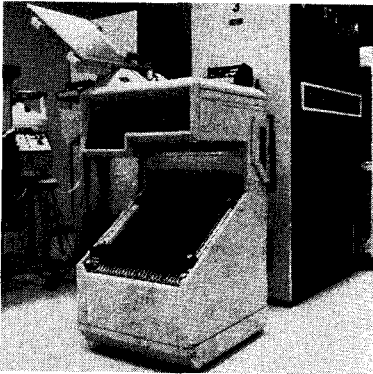


Test

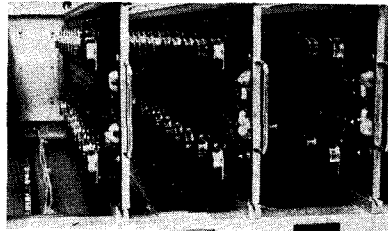
The testing of analog circuits is a science in its own right and requires very special technical skills to overcome the challenges that are presented. At Linear Technology we have invested in the very latest "state-of-the-art" computer controlled testers and our device designs exercise the limits of these excellent testers. All Military 883 products receive a 150°C or a 125°C burn-in prior to test and full temperature testing is performed. Regulator products are put on "rack burn-in" and the devices are exercised in the thermal shutdown mode prior to testing. This pretest burn-in contributes to the removal of infant mortality failures and enhances product reliability. Other tests check the thermal regulation and verify the integrity of the die attach as the presence of voids under the die for a regulator affects device performance adversely. Often, tests additional to the data sheet tests are added to a test flow to detect potential flaws that could impact reliability.

At Linear Technology we believe that the thorough and complete testing of our components is an essential element in our plan to provide 'premier' reliable products. Precautions are taken throughout test to safeguard our devices from the insidious effects of ESD (Electrostatic Discharge). As an example, all chip capacitors are pre-stressed with voltages (in excess of the device maximum voltage ratings) to induce failure in substandard lots.

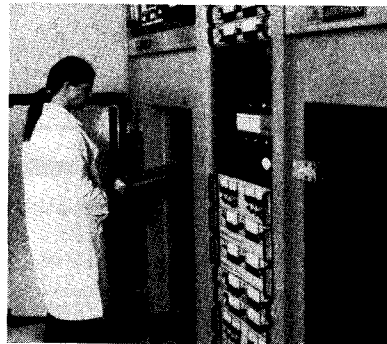
LTX/LINEAR Tester with Environmental Handler



Rack 'Burn-in' of TO-3 Regulators



Burn-in Operation



RELIABILITY ASSURANCE PROGRAM

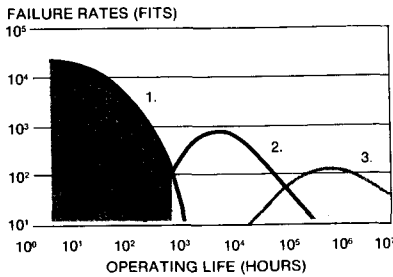
Reliability Flow

Reliability failure rate can be broken out into three main categories: 1) Infant Mortality, 2) Freak Failures and 3) Long Term Failures. Short term burn-in screening as described in the previous section address the first category—infant mortality. The long term failures represent a significant number of hours in terms of the mean time between failures and so the major area of concern is a sufficient pre-screen conditioning to eliminate the bulk of the infant mortality and freak failures.

These early life failures impact customer warranty costs and reputation severely and the replacement costs are

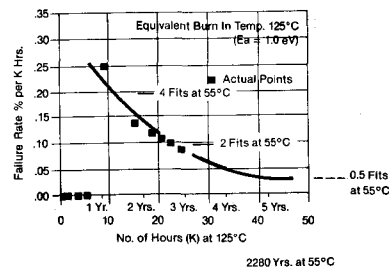
clearly several orders of magnitude greater than the initial component costs. The Linear Technology 883 program addresses this requirement and offers a cost effective in-house flow. The flow is defined in our MIL-STD 883 brochure and the essential elements of the program include visual inspection at second and third optical inspection to Condition B (Mil-Standard 883, Method 2010, temperature cycling from -65°C to 150°C , constant acceleration, fine and gross leak, followed by a 125°C burn-in for 160 hours or equivalent. Assuming an active energy of 1.0ev, this burn-in is equivalent to 80,000 hours or approximately 9 years at a normal operating temperature of around 55°C .

Typical Representation of IC Lot Failure Rates at 50°C Operation

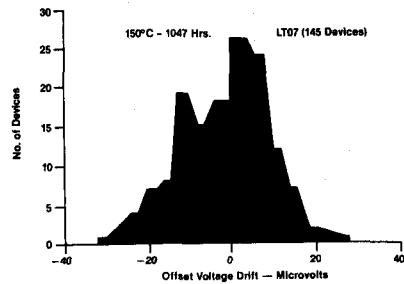


1. Infant mortality population which could be 0.5% of the lot. Its mean life could be as low as 50 hrs.
2. The freak population could represent up to 5% of the lot. Its mean life could be 5 yrs.
3. Main population whose mean life could be hundreds of years.
4. The dramatic impact on total lot reliability that is achieved by weeding out early failures via 100% burn-in.

Failure Rate vs Time—LT07H



Operating Life Drift Data



Wafer Fab Reliability Audit

As an additional reliability control, Linear Technology has innovated a periodic reliability audit of the wafer fab process, using a specifically designed reliability structure which is stepped into all wafers.

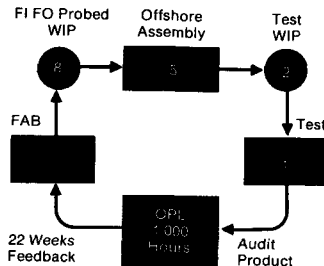
This structure is optimized to accelerate, under temperature and bias, the two most common failure mechanisms in linear circuits, namely mobile positive ions and surface charged-induced inversions. The three-terminal structure is scribed from a run and assembled in a hermetic package. These devices are burned-in for a predetermined temperature and time. The same structure becomes sensitive to either failure mechanism depending upon the bias scheme used during burn-in. A limit is defined for the leakage current change during burn-in; a failure indicates a

wafer fab problem which will be addressed by the process engineering group. The use of a test pattern allows any device to be monitored and also gives faster unambiguous feedback than is normally achieved by performing reliability testing on assembled product. Reliability data is generated in less than one week giving immediate feedback on device reliability. The standard industry monitoring schemes typically take a minimum of 22 weeks to obtain this feedback and it is not uncommon for the cycle time to be up to 40 weeks before fab is alerted of a problem.

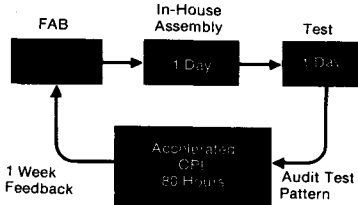
Linear Technology utilizes this new control technique in addition to the conventional reliability audit on randomly pulled finished product.

Process Reliability Monitor

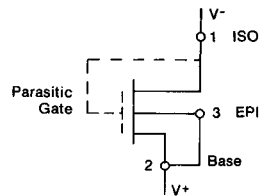
STANDARD INDUSTRY RELIABILITY AUDIT



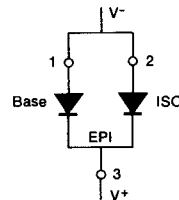
ACCELERATED FAB RELIABILITY AUDIT



FIELD CHANNEL MONITOR



SODIUM MONITOR



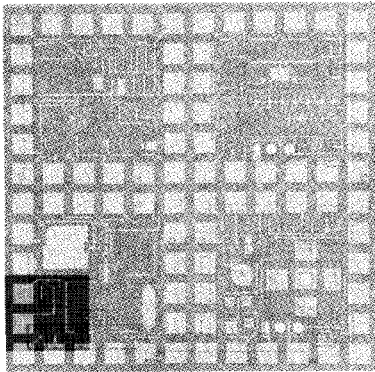
RELIABILITY ASSURANCE PROGRAM

Conclusion

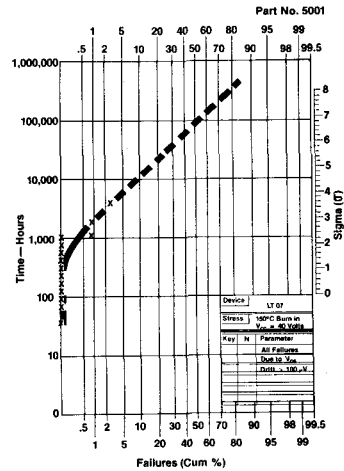
At Linear Technology Corporation we are addressing reliability and quality with the same priority to produce the best possible product in the analog world. We believe that the combination of our extensive design skills, and exciting innovations in the wafer fabrication process, coupled with the most modern assembly techniques, has produced the "MOST RELIABLE" linear products available in the market today. Our standard product flows include thermal

limit rack burn-in (for all regulators) and 150°C or 125°C burn-in for Military 883 products to significantly reduce the infant mortality failures. In addition, our 883 flow is designed to further enhance product reliability. We fully realize that the cost of failure in the field is many orders of magnitude more than the initial component cost. By purchasing Linear Technology Corporation's products, worthwhile insurance can be gained.

Reliability Test Structure



LT07H—Mean Time Between Failures



At Linear Technology Corporation our overriding commitment is to achieve Excellence in Quality, Reliability and Service (QRS) and total customer satisfaction. We interpret the word "excellence" to mean delivering products that consistently exceed all the requirements and expectations of our customers. The commitment to QRS extends from the President to every employee, from design to product qualification, and from manufacturing to shipping. To meet this commitment, Linear Technology has established a comprehensive program called "Quality for the Nineties."

This program is divided into four separate, but highly interrelated programs, namely Quality Environment, Total Quality Control (TQC), Vendor Participation, and Focus for the Nineties.

Quality Environment

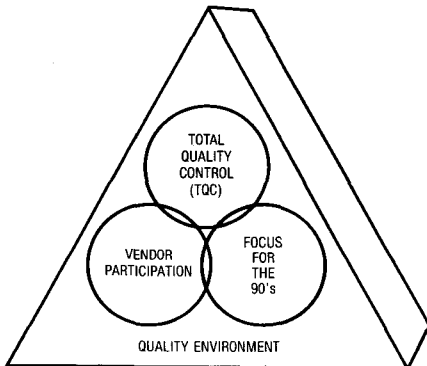
This first program, Quality Environment, serves as the building block for three other programs. It entails establishing an environment that is conducive to the participation of each and every employee in helping to build quality into our products. This program encourages every employee to identify any quality problem and participate in recommending solutions.

A comprehensive operator training and certification program has been established that covers every area of manufacturing from incoming raw material inspection, wafer fabrication, assembly, and test to shipping. Emphasis is placed on compliance with specifications, performance to quality goals, electrostatic discharge damage (ESD) awareness and controls, encouraging operators to think quality and recommend quality improvement ideas.

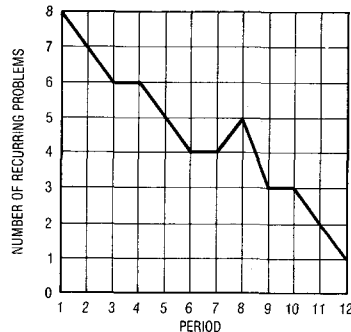
To ensure compliance with specifications, a Quality Audit Team performs a systems audit of key manufacturing areas and suppliers at periodic intervals. Compliance with process specifications and the detailed programs of the Corporate Quality Assurance Policy are verified, and discrepancies reported for quick resolution with special emphasis to eliminate recurring problems. The performance of each area is then rated, providing a strong incentive for each area to excel.

With the philosophy that each department, starting from incoming raw materials, is considered a customer of the preceding department, every effort is made by working closely together to meet or exceed our end-customer requirements and goals.

Quality for the '90's



Systems Quality Audit-Tracking Recurring Problems



QUALITY ASSURANCE PROGRAM

Total Quality Control (TQC)

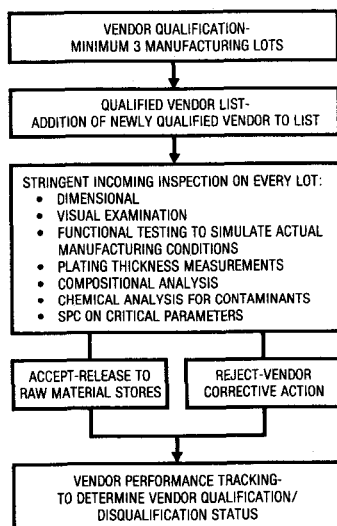
The second program starts with the incorporation of innovative, but conservative, design and layout rules to achieve the best performance without sacrificing quality and reliability. During the design and development cycle, Design, Product, Package, Manufacturing, Quality and Reliability Engineering groups participate in design reviews to ensure that all program aspects are covered; ranging from product performance objectives to ensuring reproducibility and repeatability in wafer fabrication and assembly. Special emphasis is placed on devising input protection circuitry to minimize susceptibility to voltage spikes and ESD, optimizing thermal layout to minimize parametric drift, and optimizing bond pad layout to maximize assembly and electrical test yields, at the same time allowing the die to be assembled in a wide selection of packages.

Once the design is approved, a stringent manufacturing qualification test plan is conducted on the initial engineering runs. The test plan is selected to bring out any weaknesses in the design and any manufacturability problems, and includes reliability stress tests such as high temperature operational life and high temperature humidity bias 85°C/85% RH for plastic packages, and MIL-STD-883C

method 5005 qualification testing for hermetic packages. Product performance on these tests must be equal to or better than similar products within the same generic group to be considered qualified. Major design, package, material and process changes are also subjected to these same stringent qualification requirements. In addition to achieving the required reliability performance, an engineering change must also achieve manufacturing yield and quality performance levels equal to or better than the original product to be considered qualified.

In manufacturing, process controls start with vendor qualification on raw material piece parts. A Qualified Vendor List is maintained and performance of each vendor is continuously monitored on a Vendor Rating Program. A dimensional, visual, functional and, where applicable, compositional analysis is performed on each direct raw material lot. Automated state-of-the-art wafer fabrication, assembly and test equipment, cassette-to-cassette handling in wafer fabrication and automated handling in assembly are utilized, where possible, to maintain manufacturing consistency and quality. Only fully trained and certified operators are allowed to work on production material.

Raw Material Controls



SEM Monitor of Metallization Quality



QUALITY ASSURANCE PROGRAM

Stringent process controls, typically beyond industry standards, are established for each critical manufacturing step in wafer fabrication, wafer test, assembly, package finishing, mark and pack and shipping as depicted in the Quality Control Flow Diagram. The process controls include monitors of critical assembly processes at a minimum frequency of four times per shift, and lot acceptance inspection for operations requiring 100% production inspection. Initial die inspection and pre-seal visual inspection are performed per MIL-STD-883 Method 2010 Test Condition B. Statistical quality control techniques are employed in optimizing process parameters, and monitoring process performance through the use of control charts with action limits and upper and lower control limits, and in parametric distribution analysis at electrical test.

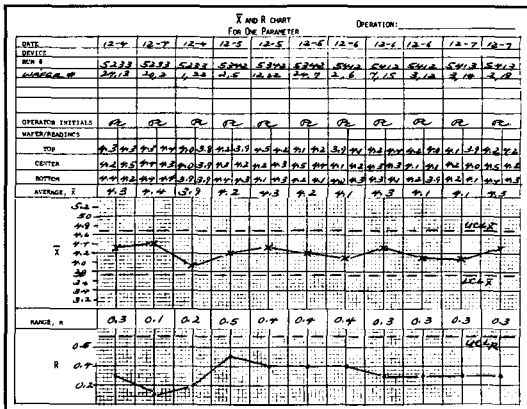
Electrical quality is guaranteed by conservative guardbanding on production test programs of a minimum of three machine guardbands, by using state-of-the-art test equipment and 0.04% AQL for lot acceptance testing at 25°C for all military and commercial lots. Additional tests, like rack burn-in, beyond the data sheet specifications on regulator products are performed by exercising the parts in a thermal shutdown mode. These tests are incorporated into the test flow to improve reliability and weed out infant mortality failures. Visual and mechanical quality is optimized by minimizing handling of parts in assembly, test and end of line operations. Lead finish processes have been selected that minimize solderability problems and all lots are subjected to

a stringent major visual/mechanical inspection. Administrative errors due to mixed and wrong parts are minimized by strictly adhering to a one lot per station policy, and double checking orders at order entry and shipping. Before shipment of a lot to the customer each lot is inspected to ensure that it meets internal and customer specifications and purchase order requirements. The level of attention paid to each unit is demonstrated by the fact that each unit is traceable to the wafer fabrication lot number via a side or back mark on both 883 and commercial products on all packages, except where there is a physical constraint.

Through the use of automated equipment, strict process controls (utilizing proven statistical quality control techniques), periodic systems and quality audits (conducted by the Quality Audit Team), stringent facilities and environmental controls and monitors, Linear Technology is able to ensure quality is built into the product and to guarantee a consistently high quality level.

The manufacturing quality controls are complimented by a reliability audit program designed to weed out design, fabrication, packaging and assembly deficiencies. Additionally, controls are supported by a comprehensive failure analysis and corrective action program designed to provide timely feedback of findings to all operating groups for resolution. The analysis of customer returns, and corrective action taken, completes the closed loop of our Total Quality Control program.

\bar{X} and R Control Chart for One Variable

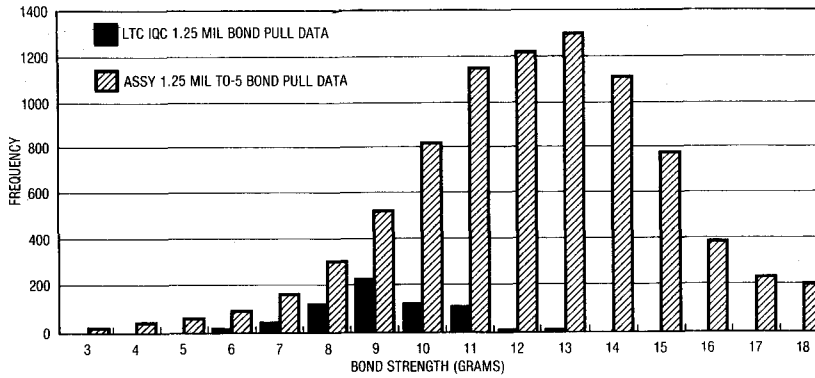


Military and Commercial Products Share the Same Stringent Inspections and Controls

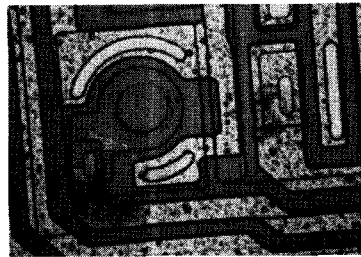
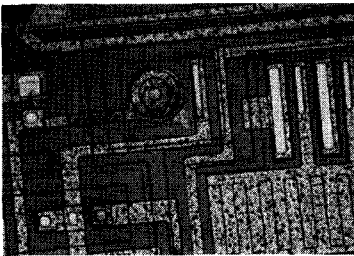
- WAFER FABRICATION PROCESS CONTROLS & CLASS 100 PROCESSING.
- REGULAR SEM MONITORS.
- DICE INSPECTION PER MIL-STD-883C METHOD. 2010 TEST CONDITION B.
- PRE-SEAL VISUAL INSPECTION PER MIL-STD-883C METHOD 2010. TEST CONDITION B.
- DIE SHEAR TEST PER MIL-STD-883C METHOD 2019.
- BOND PULL TEST PER MIL-STD-883C METHOD 2011.
- SOLDERABILITY TEST PER MIL-STD-883C METHOD 2003.
- MARK PERMANENCY TEST PER MIL-STD-883C METHOD 2015.
- HERMETICITY TESTING PER MIL-STD-883C METHOD 1014.
- QA ELECTRICAL TEST TO 0.04% AQL AT 25°C, AND TEMPERATURE TESTING.
- EXTERNAL VISUAL PER MIL-STD-883C METHOD 2009.

QUALITY ASSURANCE PROGRAM

Bond Strength Histogram



Failure Analysis Photomicrographs



QUALITY ASSURANCE PROGRAM

Vendor Participation

The requirements of high quality raw materials for integrated circuit manufacture range from ppb (parts per billion) impurity levels for electronic grade chemicals to ppm (parts per million) defective levels for lead frame packaging materials. It is not only essential, but critical for the semiconductor manufacturer to work closely with their vendors to attain the high quality levels needed in raw materials. At Linear Technology, a program has been established and implemented to allow vendor participation in formulating specifications and establishing percentage defective and lot rejection rate goals. This vendor participation ensures that the direct and raw material quality levels received are consistent with our manufacturing and end-product quality goals. Clearly, achieving optimum quality product requires the use of the best possible materials available and with continuous communication and feedback from our vendors to improve in this key area.

Focus For the 90's

The following key quality improvements programs have been established to meet the quality requirements of the 90's.

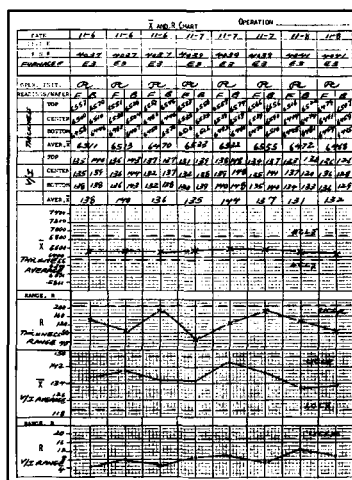
PPM Goals

As demand for quality semiconductor components becomes increasingly more stringent, the percentage goals from the 1970's have given way to ppm goals in the 1980's. At Linear Technology, ppm quality goals are established for every major operation, from incoming inspection to customer returns. Performance to goals is reviewed quarterly and, where goals are not met, quality improvement programs are defined and implemented. Quality goals are updated and tightened on an annual basis, and quality programs are redefined to achieve the new goals established. One of the early benefits of this program is demonstrated by the excellent average outgoing electrical quality (AOQ).

Statistical Process Control (SPC)

The increased reliance on automated manufacturing and test equipment underlines the need for strict process control techniques. SPC is a valuable tool and, at Linear Technology, we realize the importance of these methods. Engineering analysis is performed regularly, using SPC techniques to establish the process capability. Control charts showing \bar{X} and R points are tracked to ensure the process is within normal limits and action and shutdown limits are established for critical operations. The process capability of key processes are calculated using the C_{pk} process capability index on an ongoing basis to ensure a program for continuous quality improvement.

\bar{X} and R Control Chart for Two Variables



QUALITY ASSURANCE PROGRAM

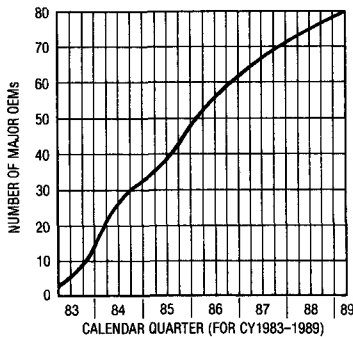
ESD Control

A comprehensive ESD control program has been established which encompasses design, handling, testing, storage, and final packaging for shipment. The program includes the use of grounded table tops, floor mats, wrist straps and heel straps, topical antistatic treatment of floor coverings, banning of static bearing materials from the manufacturing environment, ionizers, and use of conductive or antistatic materials for handling and final packaging. Areas where ESD control must be enforced are designated as ESD Protected areas. ESD awareness training programs help to increase the operator's awareness for successful implementation of this program. Every effort is made to stamp out this silent chip killer. The benefits of this program are improved quality and reliability to the customer.

Customer Ship-To-Stock Program

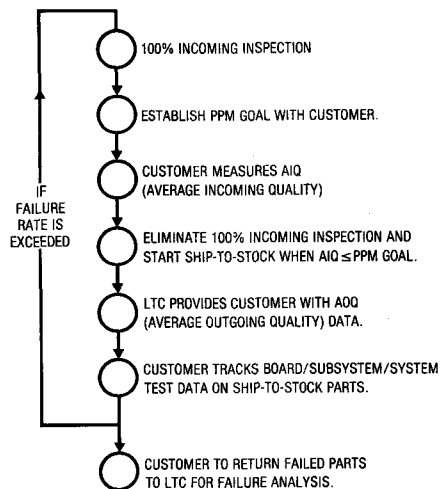
Linear Technology is working hand-in-hand with customers to supply consistently high quality-level products to help achieve a ship-to-stock program by eliminating the need to do an incoming inspection. We recognize the benefits to our customers of a ship-to-stock program, namely savings in the need to purchase and maintain incoming test equipment, savings in the need to maintain a safety stock in case of incoming lot rejections, and reduction in board failures and re-work costs because of higher component quality.

Quality System Surveys MIL-Q-9858 and MIL-I-45208 Approval



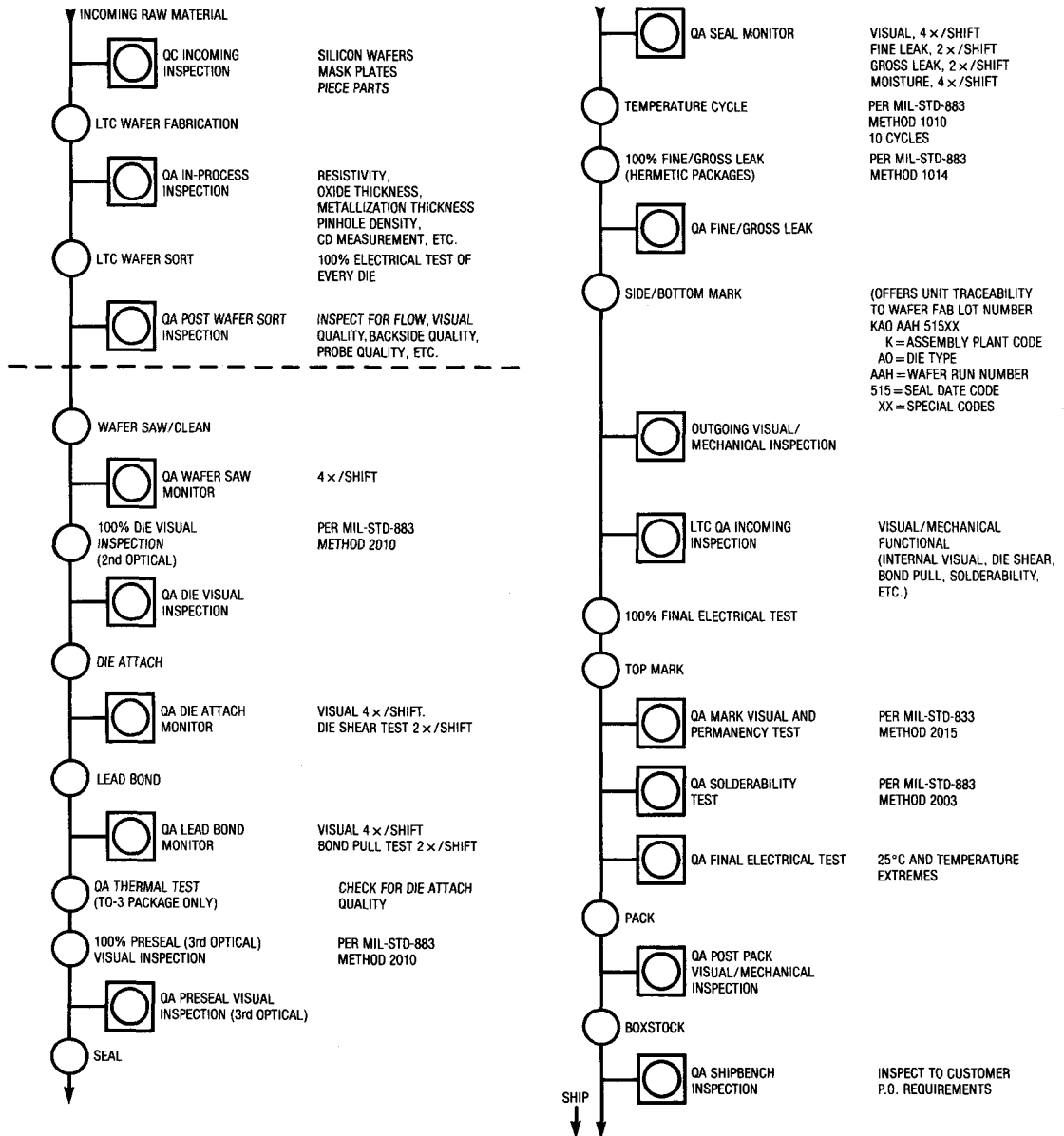
Based on the foregoing quality programs, Linear Technology Corporation is positioned to continuously improve our product quality and exceed the demands of our customers in the 80's and beyond.

Ship-To-Stock Program Flow



QUALITY ASSURANCE PROGRAM

Quality Control Flow Diagram



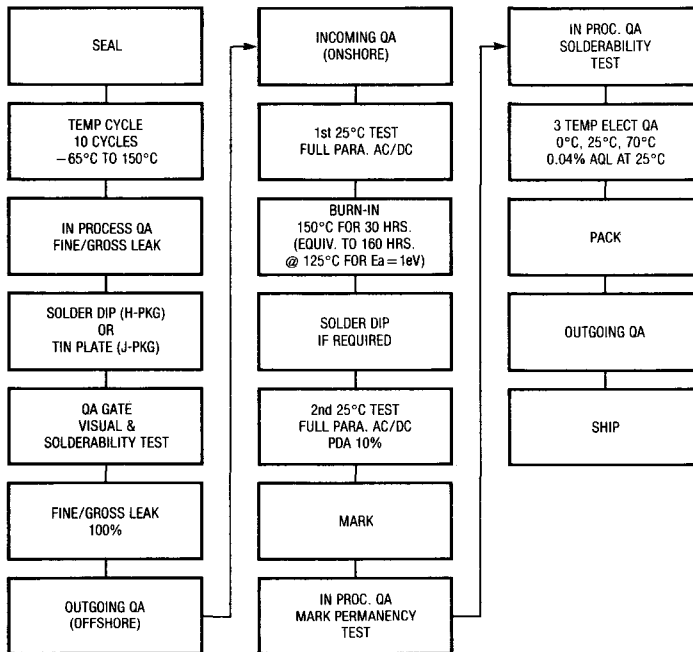
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Linear Technology R-Flow

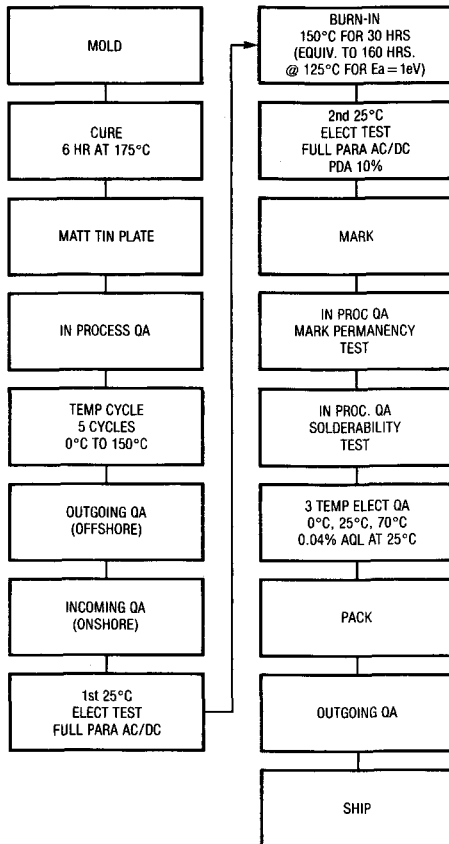
Reliability has been a key focal point at Linear Technology Corporation since our inception in 1981. Our standard product reliability is monitored closely and we have generated an extensive reliability data base for both hermetic and plastic devices. This data is published on a quarterly basis and we are seeing very low reliability failure rates in the under 1 FIT range at 55°C.*

In response to customer requests, we have added an even higher level of reliability screening for commercial hermetic and plastic components. LTC's R-Flow adds an equivalent 160 hours 125°C burn-in to the standard commercial process flow. Following burn-in, a 100% room temperature test is performed and a 10% PDA (Percent Defective Allowed) is applied. This PDA limit affords an additional level of insurance on a lot-by-lot basis and prevents the occasional disparate lot from being shipped for critical applications. The additional room temperature insertion also decreases the probability of any electrical defectives in the R-Flow lot.

*Note: 1 FIT = 1 failure in 10⁹ device hours.

R-Flow for TO-5 and CERDIP Packages


R-Flow for Plastic Dual-In-Line Packages



Introduction

As integrated circuit technologies achieve higher speed, smaller geometries, lower power and lower voltage, there is a trend toward greater ESD (Electrostatic Discharge Damage) susceptibility. State-of-the-art CMOS ICs can be susceptible to as little as 50V, a static level that is way below the 500V to 15,000V commonly found in an ESD unprotected work environment. As these state-of-the-art ICs get designed into systems, the ESD susceptibility of system hardware also increases proportionately. Industry estimates of losses due to ESD are in the range of a few billion dollars annually.

It has now become increasingly more important for all semiconductor manufacturers and users of semiconductor and other electronic components to fully understand the nature of ESD, the sources of ESD, and its impact on quality and reliability, to effectively deal with this *silent chip killer*.

Linear Technology Corporation has successfully undertaken a simple but effective ESD Protection Program as part of an overall program designed to enhance product quality and reliability. Described in this section are the keypoints of this program.

The objective is to provide increased ESD awareness by showing the sources of ESD in the work environment, and to recommend keypoints for the successful implementation of an ESD program on a company-wide basis.

The end result of a successful ESD program would be the reduction of line failures, final inspection failures and field failures, improved manufacturing yields, improved product quality and reliability and lower warranty costs. We hope that this will help to convince the reader that an ESD Protection Program must be an integral part of every electronic company's product quality and reliability program.

Key Elements of a Successful ESD Protection Program

Recent improvements in failure analysis techniques to correctly identify ESD failures together with an increase in ESD related information from technical publications,

EOS/ESD symposiums and vendors have significantly helped to increase ESD awareness.

The ESD Protection Program at Linear Technology Corporation was successfully launched in 1983 when production of ICs was first started. A constant upgrading of the program is still underway. During the ongoing efforts to improve product quality and reliability, previously unrecognized ESD related problems have been brought to light and corrected.

An effective ESD Protection Program must start at product design, and encompass all manufacturing and handling steps up to and including field service and repair. Our design goal is to achieve an ESD susceptibility level of 2,000V or greater.

Since the sources of static in any work environment are similar, key elements of the program successfully implemented at Linear Technology Corporation can also be applied to all users of electronic components. Where these key elements apply, static controls generic to an electronic systems manufacturer are included.

The key elements of a successful ESD Protection Program include:

1. Understanding static electricity.
2. Understanding ESD related failure mechanisms.
3. ESD sensitivity (ESD) testing.
4. Establishing an ESD task force to outline the requirements of the program, sell the program to management, implement the program, review progress against milestones, and follow-up to ensure the program is continuously improved and upgraded. Selecting an ESD coordinator to interface with all departments affected.
5. Conducting a facility evaluation to help identify the sources of ESD and establish static control measures.
6. Setting up an audit program.
7. Selection of ESD protective materials and equipment.
8. Establish a training and ESD awareness program.

ESD PROTECTION PROGRAM

What is Static Electricity?

Lightning and sparks from a metallic doorknob during a dry month are examples of static electricity. The magnitude of a static charge is dependent on many variables, among them the size, shape, material composition, surface characteristics and humidity. There are basically three primary static generators, namely triboelectric, inductive and capacitive charging.

Triboelectric Charging

The most common static generator is triboelectric charging. It is caused when two materials (one or both of which are insulators) come in contact and are suddenly separated or rubbed together, creating an imbalance of electrons on the materials and thus static charge.

Some materials readily give up electrons whereas others tend to accumulate excess electrons. The Triboelectric Series lists materials in descending order from positive to negative charging due to this triboelectric effect. A sample triboelectric series is shown here. A material that is higher on the list, e.g., a human body, will become positively charged when rubbed with a material, e.g., polyester, that is lower on the list, due to the transfer of electrons from the human body to the polyester material.

Triboelectric Series

Human Body	
Positive +	Glass
	Mica
	Nylon
	Wool
	Fur
	Silk
	Aluminum
	Paper
	Cotton
	Steel
	Wood
	Hard Rubber
	Orlon
	Polyester
	Polyethylene
	PVC (Vinyl)
	Teflon
Negative -	

Inductive Charging

Static can also be caused by induction, where a charged surface induces polarization on a nearby material. If there is a path to ground for the induced charge, an ESD event may take place immediately. An example of an induced charge is when the plastic portion of a molded IC package acquires a charge either through triboelectric charging or other means, produces an electrostatic field and induces a charge on the conductive leads of the device. When the device leads are grounded, a short duration damaging static pulse can take place.

Capacitive Charging

The capacitance of a charged body relative in position to another body also has an effect on the static field. To see that this is true, one need only look at the equation $Q = CV$ (charge equals capacitance times voltage). If the charge is constant, voltage increases as capacitance decreases to maintain equilibrium. As capacitance decreases the voltage will increase until discharge occurs via an arc. A low voltage on a body with a high capacitance to ground can become a damaging voltage when the body moves away from the ground plane. For example a 100V charge on a common plastic bag lying on a bench may increase to a few thousand volts when picked up by an operator, due to a decrease in capacitance.

These sources of static can be found almost anywhere in an unprotected work environment, on personnel wearing synthetic clothing and smocks, on equipment with painted or anodized surfaces, and on materials such as carpets, waxed vinyl floors, and ungrounded work surfaces.

Understanding the Failure Mechanisms

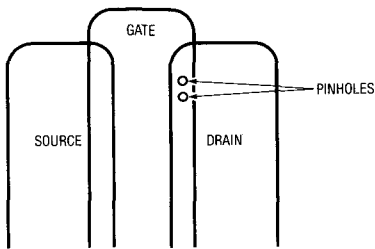
In the past, analysis of electrical failures to pinpoint ESD as a cause was often difficult. But with a better understanding of failure mechanisms and their causes, and the use of more sophisticated techniques like scanning electron microscopy (SEM), pinpointing ESD failures can now be part of a routine failure analysis.

Parametric or functional failure of bipolar and MOS ICs can occur as a result of ESD.

The primary ESD failure mechanisms include:

1. Dielectric Breakdown: This is a predominant failure mechanism on MOS devices when the voltage across the oxide exceeds the dielectric breakdown strength. This failure mechanism is basically voltage dependent where the voltage must be high enough to cause dielectric breakdown. As such, the thinner the oxide, the higher the susceptibility to ESD. MOS device failures are characterized by resistive shorts from the input to V_{DD} or V_{SS} .

**MOS Transistor Structure
Showing ESD Included Pinholes at Gate Oxide**



This failure mechanism can also be found on bipolar ICs which have metallization runs over active semiconductor regions separated by a thin oxide. Device failures are characterized by resistive or high leakage paths.

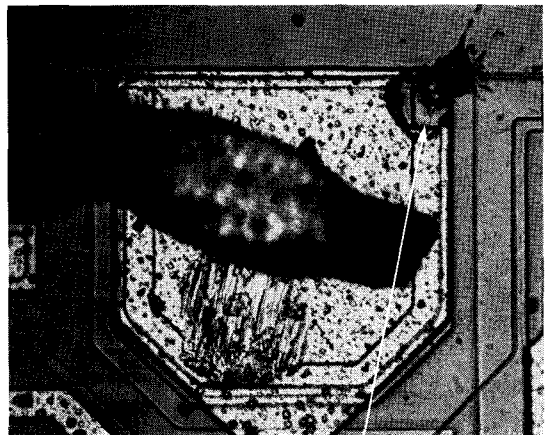
2. Thermal Runaway (Second Breakdown): This failure mechanism results in junction melting when the melting temperature of silicon (1415°C) is reached. This is basically a power dependent failure mechanism, namely the ESD pulse shape, duration and energy can produce power levels resulting in localized heating and eventually junction melting, even though the voltage level is below that required to cause dielectric breakdown. Second breakdown of the emitter-base junction of a NPN transistor is a common ESD related failure mode on bipolar ICs, since the highest current density occurs on the smallest current carrying area which is typically the emitter-base junction. Low current gain (h_{FE}) is a very sensitive indicator of emitter-base junction damage on bipolar linear ICs.

3. Metallization Melting: When junction melting and a short occurs, localized melting of the metallization can occur if there is enough energy in the ESD pulse. This is frequently a secondary failure mechanism, following a short resulting from one of the other failure modes.

4. Parametric Degradation: On precision, high speed ICs (e.g., bipolar operational amplifiers with a typical input bias current of 10pA and low input offset voltage of typically $50\mu\text{V}$) ESD can cause device degradation, besides functional failures. This can impact electrical performance and adversely affect device reliability.

This degradation in device parametric performance is far more difficult to pinpoint as an ESD related failure mode. It is also the least understood among the failure modes. The extent of this degradation is dependent on the number of ESD pulses and the level of damage sustained. The first ESD pulse may not cause an IC to fail the electrical datasheet limits, but with each subsequent ESD pulse, the parametric performance can degrade to the point where the device no longer meets the datasheet limits.

There is a great deal of current research focused on ESD induced latent failures, and there now appears to be more evidence of this type of failure mechanism.



RESISTIVE SHORT ON A
METALLIZATION STRIP OVER
A THIN OXIDE N^+ REGION
ON A BIPOLAR IC

ESD PROTECTION PROGRAM

ESD Failure Analysis Program

ESD defect identification must be an integral part of a failure analysis program. The key objectives are to help identify the ESD failure mechanism, isolate the cause for failure, and implement corrective action to prevent recurrence. All devices suspected of being damaged by ESD after initial electrical verification, should be failure analyzed.

An ESD failure analysis program is outlined below.

1. Initial electrical test verification.
2. Review device history to determine if there are any similar failures in the past. Review ESD sensitivity data if available.
3. Investigate conditions in any area that can potentially cause ESD damage. Common potential problem areas include:
 - Proper grounding procedures not being followed (e.g., conductive table/floor mats not grounded, personnel not wearing wrist strap, etc.)
 - Improper handling (e.g., handling devices at a non-ESD protected station)
 - Transporting devices in unapproved containers (e.g., in common plastic bags/tubes/tote boxes)
 - Changes in procedures or operation
 - Changes in equipment
 - Design deficiencies
4. Failure analysis sequence:
 - Bench testing and curve tracer analysis
 - Pin-to-pin analysis
 - Internal visual (10x to 1000x)
 - Liquid crystal hot spot detection
 - Scanning electron microscopy (SEM), secondary ion mass spectrometry (SIMS), energy dispersive X-ray analysis (EDX), scanning auger microprobe (SAM)
 - Plasma/chemical etching
 - Special fault decoration
 - Micro-sectioning
 - Documentation

An excellent failure analysis manual is published by the Rome Air Development Center titled "Failure Analysis Techniques—A Procedural Guide".

5. Duplication of failure by stressing identical devices. The same or similar electrical failure mode is a good indicator of an ESD induced failure mode.
6. Implement corrective action to prevent recurrence. Corrective action may include:
 - Component, board, sub-system or system level redesign
 - Improve ESD controls
 - Improve part handling
 - Improve ESD awareness
 - Improve compliance with ESD protection procedures
 - Increase audit frequencies
 - Improve packaging materials and procedures

Corrective action taken by the end user should include a thorough review of electrical and mechanical packaging designs. In addition the end user should consult with the IC manufacturer on their findings, request failure analysis of suspected ESD failures if needed and require the IC manufacturer to take appropriate corrective action on any confirmed ESD failure.

ESD Sensitivity (ESDS) Testing

ESDS testing is crucial in helping the IC designer and the end user evaluate the ESD susceptibility of a particular device. At Linear Technology Corporation, ESDS testing is incorporated into the failure analysis program and is performed on each device as part of the product characterization program. The ESDS testing is also part of new product qualification. Linear Technology performs this ESDS testing according to MIL-STD-883C, Method 3015.

The ESDS testing provides immediate feedback to the IC designer on any weakness found in the design and permits design correction before product release. The ESDS data collected is also used as baseline data to evaluate the effect of any future design changes on the ESDS testing performance, and to help ensure that the final packaging methods meet MIL-M-38510F requirements. Devices which are classified as Category A devices, susceptible to 2000V or less, on this ESDS testing are top marked with an equilateral triangle per MIL-M-38510F requirements.

Since people are considered to be a prime source of ESD, the ESDS test circuit is based on a human ESD model. A 15000 Ω resistor and a 100pF capacitor are used in the test circuit. Human capacitance is typically 50pF to 250pF, with the majority of people at 100pF or less, and human resistance ranges from 10000 Ω to 50000 Ω . Five combinations of input, output, V⁺ and V⁻ pins are tested. An ESD failure is defined as a voltage level which causes sufficient damage to the device such that it no longer meets the electrical datasheet limits.

After initial ESDS testing, it is important that ESDS test monitoring be performed periodically on devices from various lots to determine lot-to-lot variation. The VZAP-1 report titled "Electrostatic Discharge (ESD) Susceptibility of Electronic Devices" published by the Reliability Analysis Center, Rome Air Development Center, contains a wealth of information on ESDS testing data on devices of different process technologies from many manufacturers. The data in this report clearly indicates a large lot-to-lot variation relating to ESD susceptibility on the same device.

Design for ESD Protection

ESD protection designs employed on Linear Technology Corporation devices include:

1. Input clamp diodes
2. Input series resistors to limit ESD current in conjunction with clamp diodes
3. Keeping critical junctions out of reverse breakdown, or physically enlarging it
4. Eliminating metallization runs over thin oxide regions when they are tied directly to external pins

ESD Task Force

An ESD task force should consist of members from each affected department to do the foundation work, sell the program to management, and implement the program with the following objectives:

1. Develop, approve and implement an ESD control specification covering all aspects of design, ESD protected materials and equipment, and manufacturing

2. Raise the level of ESD awareness
3. Develop a training and certification program
4. Work with all departments on any ESD questions or problems
5. Develop a program to educate and assist sales offices, distributors and customers to minimize ESD
6. Review and qualify new ESD protective materials and equipment, and keep specifications and training program updated
7. Measure the cost-to-benefit ratio of the program

Facilities Evaluation

The ESD task force should be responsible for facility evaluation. This evaluation should be guided by the ESD coordinator. The ESD coordinator should be chosen for strong knowledge of ESD controls, and for the ability to effectively interface with all affected departments. The primary objective of the task force is to pinpoint areas that represent sources of static electricity and potential yield losses due to ESD.

A representative, preferably the engineering or production manager, from each of the key manufacturing areas should be represented on this task force. At Linear Technology Corporation this effort is headed by the Quality Assurance Manager and the Package Engineering Manager. The balance of the ESD task force members are the Test Engineering, Product Engineering, and Production Managers.

The only equipment needed for this survey is a field static meter which measures static up to a level of 50kV. Both nuclear and electronic type static meters are available from manufacturers like 3M, Simco, Wescorp and Scientific Enterprises.

Regardless of area classification, all manufacturing areas can be broken down into the following categories for evaluation purposes.

ESD PROTECTION PROGRAM

1. Personnel

Personnel represents one of the largest sources of static, from the type of clothing, smocks and shoes that they wear (for example, polyester or nylon smocks).

2. The Environment

The environment includes the room humidity and floors. Relative humidity plays a major part in determining the level of static generated. For example, at 10-20% RH a person walking across a carpeted floor can develop 35kV versus 1.5kV when the relative humidity is increased to 70%-80%. Therefore the humidity level must be controlled and should not be allowed to fluctuate over a broad range.

Floors also represent one of the greatest contributors of static generation on personnel, moving carts or equipment because of movement across its surface. Carpeted and waxed vinyl floors are prime static generators.

3. Work Surfaces

Painted or vinyl covered table tops, vinyl covered chairs, conveyor belts, racks, carts and shelving are also static generators.

4. Equipment

Anodized surfaces, plexiglass covers, ungrounded solder guns, plastic solder suckers, heat guns and blowers are also static generators.

5. Materials

Look out for common plastic work holders, foam, common plastic tote boxes and packaging containers.

Examples of typical static levels are shown in the table below.

	RELATIVE HUMIDITY	
	10%-20%	70%-80%
Walking across a carpeted floor	35kV	1.5kV
Walking across a vinyl floor	12kV	0.3kV
Picking up a common plastic bag	15kV	0.5kV
Sliding plastic box over bench/conveyor	15kV	2.0kV
Ungrounded solder sucker	8kV	1.0kV
Plastic cabinets	8kV	1.0kV

This ESD survey should include all direct and support manufacturing areas where semiconductor and other electronic components are handled, and should be extended to cover distribution and field sales offices, and field service centers. Once the facility evaluation is completed, the results are reviewed by the ESD task force, and controls are selected to combat each potential ESD problem area.

The ESD Protection Program

The degree of static control should be determined by the most static sensitive device or assembly in the operation. Top management support and implementing the same basic controls in all areas with no double standards will help to ensure success.

The basic concept of complete static protection is the prevention of static buildup, the removal of any already existing charges, and the protection of electronic components from induced fields. The first and foremost line of defense is the personnel wrist strap together with grounded conductive or static dissipative table tops, and conductive heel straps and grounded conductive or static dissipative floor mats.

To increase ESD awareness at Linear Technology Corporation, all ESD Protection Areas are marked by an identifying label shown below. This label alerts all personnel that ESD protection procedures are enforced in the area.

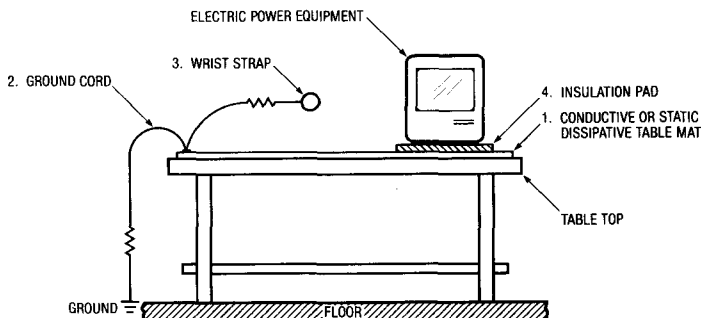


ESD Protected Workstation

Examples of ESD Protected Workstations are shown in Figures 1 and 2.

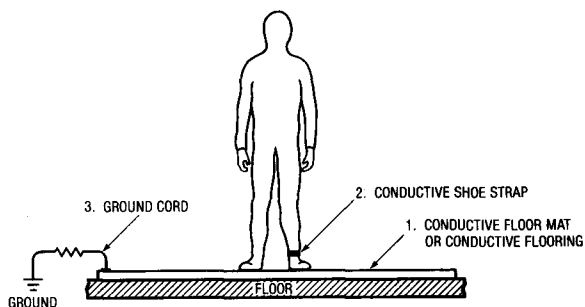
Option 1 (Figure 1): All electronic components, sub-assemblies and assemblies must be handled at an ESD Protected Workstation only. The figure illustrates an ESD Protected Workstation consisting of a static dissipative table mat grounded to earth or electrical ground through a 1MΩ series resistor, with the requirement that the operator wears a grounded insulated conductive wrist strap with a

1MΩ series resistor. This 1MΩ series resistor protects the operator from electrical shock, should the operator come in contact with a potentially lethal voltage. Option 1 should be used where the operator does not require a large degree of freedom, e.g., during product inspection, component soldering, board repair, etc.



- MATERIALS:**
1. 1/16" THICK CONDUCTIVE OR STATIC DISSIPATIVE TABLE MAT WITH SURFACE RESISTIVITY OF $\leq 10^8\Omega$ PER SQUARE.
 2. INSULATED CONDUCTIVE GROUND CORD WITH A SERIES RESISTOR OF 1/2W MINIMUM, $1M\Omega \pm 10\%$, AND 18AWG OR LARGER INSULATED WIRE.
 3. INSULATED CONDUCTIVE WRIST STRAP WITH 1/4W MINIMUM, $1M\Omega \pm 10\%$, AND 20AWG OR LARGER INSULATED WIRE. THE CURRENT LIMITING $1M\Omega$ RESISTOR MUST BE LOCATED RIGHT NEXT TO THE WRIST TO PREVENT THE POSSIBILITY OF SHUNTING THE RESISTOR.
 4. POWER TEST EQUIPMENT MUST BE CHASSIS GROUNDED VIA A THREE-PRONG PLUG, AND PLACED ON AN INSULATION PAD MADE OF FORMICA, FIBERGLASS OR EQUIVALENT MATERIAL.

Figure 1



- MATERIALS:**
1. OPTIONAL 1/8" THICK CONDUCTIVE OR STATIC DISSIPATIVE MAT OR CONDUCTIVE FLOORING (e.g., CONDUCTIVE FLOOR TILES) WITH A SURFACE RESISTIVITY OF $\leq 10^8\Omega$ PER SQUARE.
 2. CONDUCTIVE SHOE STRAP WITH A SURFACE RESISTIVITY OF $< 10^5\Omega$ PER SQUARE.
 3. INSULATED CONDUCTIVE GROUND CORD WITH A SERIES RESISTOR OF 1/2W MINIMUM, $1M\Omega \pm 10\%$, AND 18AWG OR LARGER INSULATED WIRE.

Figure 2

ESD PROTECTION PROGRAM

Option 2 (Figure 2): Shows an alternate installation method for an ESD Protected Workstation. It consists of a conductive or static dissipative floor mat grounded to earth or electrical ground through a 1M Ω series resistor with the operator wearing a conductive shoe strap. This installation is typically used where the operator needs freedom of movement over a large area, e.g., environmental chamber loading and unloading, electrical testing, etc. To be effective the conductive shoe strap must be attached to the wearer's shoe to maximize contact between the strap and the conductive floor.

Option 3: Utilizes the same conductive or static dissipative floor mat installation as Option 2 with the exception that the operator is grounded via a wrist strap through the equipment ground instead of a conductive shoe strap. It is utilized where an operator is working with a piece of free-standing equipment and does not require a great deal of freedom of movement.

Handling

At Linear Technology Corporation all products are handled, transported and staged in volume conductive tote boxes. This offers maximum protection to the components from triboelectrically generated and inductive static charges. The rule is under no circumstances should components be removed from their approved containers except at an ESD protected workstation.

Final Packaging

Only antistatic and conductive final packaging containers (for example, antistatic or conductive dip tubes, volume conductive carbon loaded plastic bags or metallic film laminate bags, foil lined boxes) are used. Filler (dunnage) material used should be antistatic, non-corrosive, and should not crumble, flake, powder, shred or be of fibrous construction. Conductive packing materials are preferred since they not only prevent buildup of triboelectric charge, but also provide shielding from external fields.

Other ESD Preventative Measures

- Where possible, ban all static bearing materials, e.g., common plastics, styrofoam from the work environment.
- Use only synthetic material smocks with 1% to 2% interwoven steel.

- Ensure all electronic and electro-mechanical equipment is chassis grounded, including conveyor belts, vapor degreasers and baskets, solder pots, etc.
- Tips of hand soldering irons are to be grounded.
- All parts of hand tools (e.g., solder suckers, pliers, etc.) which can be expected to come in contact with electronic components are to be made of conductive material and grounded.
- Conductive shorting bars are to be installed on all terminations for PC boards with electronic components during assembly, loading, inspecting, repairing, soldering, storing and transporting.
- All PC boards with electronic components are not to be handled by their circuitry, connector points or connector pins.
- High velocity air movement is to be delivered through a static neutralizer.
- Air ionizers are to be employed in neutralizing static buildup on insulators if they have to be used or as an extra precautionary measure for extremely sensitive assemblies.
- Do not slide electronic components over a surface.

Air ionizers come in three basic types: nuclear, AC and pulsed DC. These ionizers can neutralize static charges on non-conductive materials by supplying the materials with a stream of both positive and negative ions.

The advantage of the AC or pulsed DC type air ionizer is that there is no recurring annual replacement cost. The disadvantages are: it emits ozone which can damage rubber in equipment; EMI (Electro Magnetic Interference); and an imbalance in the stream of ions if not properly maintained, therefore necessitating frequent preventive maintenance.

The advantages of the nuclear type air ionizer are low maintenance, no ozone, no EMI and no imbalance problems. The disadvantages are that it requires careful handling because of the radioactive source, and the annual recurring cost to replace the radioactive source.

The selection of air ionizers must be done with care with awareness of the above limitations. The squirrel cage ionized air blower has been proven to produce a significantly more even distribution of ion patterns than does a conventional fan blower design.

Maintenance

ESD protective floor and table coverings must be properly maintained. Do not wax over them. Cleaners must not degrade their electrical properties. Vacuum to remove loose particles, followed by a wet mop with a solution of mild detergent and hot water.

Periodic Audits

At Linear Technology Corporation periodic audits are conducted to check on the following at least once a month, unless otherwise noted.

- Compliance with ESD control procedures.
- Ensure that the conductive ground cord connection is intact by measuring the series resistance to ground with an ohmmeter.
- Ensure that wrist straps are still functional by measuring the resistance from the person to ground. The ground lead of the ohmmeter is connected to the ground connection of the wrist strap, and the positive lead is connected to a stainless steel electrode (one inch in diameter, and three inches long #304 stainless steel) which is held by the person. This test method not only checks the resistance of the series resistor, but also resistance through the ground cord and also any contact resistance between the wrist strap and the person's skin. This test procedure is required when wrist straps with an elastic nylon band with interwoven metallic strands are used, since the metallic strands breakdown with prolonged use. This monitor frequency may be shortened depending on audit results.

- Measure the surface resistivity of conductive or static dissipative table tops once every 6 months using ASTM-F-150-72, ASTM-D-257 or ASTM-D-991 test methods as appropriate.

Materials Selection and Specification

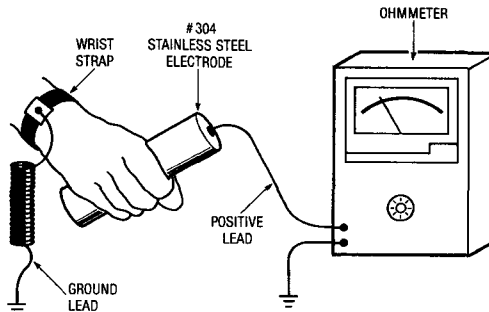
Based on the tremendous amount of ESD protective materials available, it is important that materials are selected based on a stringent qualification. Once the materials have been selected and specifications defined, a material procurement specification needs to be initiated that defines the materials and quality requirements to the vendor. One of the major pitfalls is to procure material in haste, e.g., a wrist strap, only to find out it does not perform reliably.

The SOAR-1 report titled "ESD Protective Material and Equipment: A Critical Review" published by the Rome Air Development Center is an excellent reference on the various types of ESD protective materials available.

At Linear Technology Corporation a minimum of three manufacturing lots from a potential vendor are subjected to qualification testing per the requirements of the material procurement specification for ESD protective materials. The vendor is considered qualified only when all three lots are found to be acceptable. Once vendors have been qualified, all incoming ESD protective materials are subjected to a stringent incoming inspection.

The following table summarizes a sample material and test specification for ESD protective materials.

Wrist Strap Resistance Test Set-Up



ESD PROTECTION PROGRAM

MATERIAL	PROPERTIES/DESCRIPTION	TEST METHODS
Wrist Strap	<ul style="list-style-type: none"> Insulated coil cord with a $1M\Omega \pm 10\%$, $\frac{1}{4}W$ minimum series resistor molded into snap fastener (at wrist end), and an elastic wrist band with inner metallic filaments and insulative exterior. 	Measure series resistance with ohmmeter. Apply normal tug to both ends of strap and remeasure series resistance. Resistance must be between 0.8 to 1.2M Ω .
Conductive or Static Dissipative Table and Floor Coverings, Conductive Tote Boxes, Conductive Shoe Straps	<ul style="list-style-type: none"> Must not shed particles Must not support bacterial or fungal growth Conductive: surface resistivity $< 10^9 \Omega/\text{square}$. Static Dissipative: surface resistivity $> 10^5$ and $< 10^9 \Omega/\text{square}$. 	Test per ASTM-F-150-72, ASTM-D-257, ASTM-D-991 (for surface resistivity $< 10^8 \Omega/\text{square}$).
Conductive Foam	<ul style="list-style-type: none"> Shall not contain more than 30ppm C1, K, Na when a quantitative chemical analysis is performed Must not support bacterial or fungal growth 	With devices inserted into the foam, the foam must not cause lead corrosion after a 24 hour 85°C/85% RH temperature/humidity storage.
Antistatic and Conductive Dip Tubes	<ul style="list-style-type: none"> Must not exhibit an oily-like film 	Must meet an Electrostatic Decay test per Federal Test Method Standard 101 Test Method 4046. Material charged to 5000V must be discharged to 1% of its initial value (50V) in 2 seconds after a 24 hour conditioning at 15% relative humidity.
Antistatic and Conductive Bags	<ul style="list-style-type: none"> Antistatic bags must meet MIL-B-81705 type 2 Conductive bags must meet MIL-B-117 and sealing requirements of MIL-B-81705 Must not support bacterial or fungal growth 	Test method for antistatic bags same as for antistatic/conductive dip tubes. Test method for conductive bags same as for conductive table/floor coverings.
Static Eliminators/Ionized Air Blowers	<ul style="list-style-type: none"> Ozone level: 0.1ppm maximum for 8 hour exposure Noise: 60dB maximum EMI: non-detectable when measured 6 inches away 	Voltage Decay test: A non-conductive sheet of material charged to 5kV must be discharged to 1% of its initial value (50V) in 2 seconds at a distance of 2 feet from the ionizer or larger distance if application calls for a larger distance.

Training and Certification Program

The training program should be developed to increase ESD awareness and to assist all personnel in complying with the ESD control specification. The program should include:

1. A discussion on "What is Static Electricity?"
2. How ESD affects ICs
3. Estimated cost of ESD related losses
4. Materials and equipment for controlling static
5. The importance of wearing the wrist strap
6. The importance of an audit program
7. Encourage floor personnel to feedback any ESD potential areas to the ESD task force

ESD training should be incorporated into the personnel training and certification program. At Linear Technology Corporation only fully trained and certified personnel are allowed to do actual production work. To help increase

ESD awareness, it is often a good idea to show ESD awareness films and video tapes which are available from a variety of sources (Reference 3 provides a list of films and video tapes). Personnel are retrained and recertified at a minimum frequency of once per year.

Measuring the Benefits

Where possible, the benefits of an ESD Protection Program should be tracked and quantified. The two yardsticks used at Linear Technology Corporation are final test yields and QA electrical average outgoing quality (AOQ). Since the implementation of this program, there has been a significant improvement in final test yields especially on static sensitive CMOS devices. With the elimination of ESD as a potential failure cause, the electrical AOQ has averaged well under 100ppm for all products combined. Improvements such as this help to provide positive feedback to manufacturing and support personnel on the importance of an ESD Protection Program, and also help to ensure its continuing success.

References

1. DOD-STD-1686 Electrostatic Discharge Control Program for Electrical and Electronic Parts, Assemblies and Equipment.
2. DOD-HDBK-263 Electrostatic Discharge Control Handbook for Electrical and Electronic Parts, Assemblies and Equipment.
3. SOAR-1 State-of-the-Art Report ESD Protective Materials and Equipment: A Critical Review, published by the Rome Air Development Center.
4. VZAP-1 Electrostatic Discharge (ESD) Susceptibility of Electronic Devices published by the Rome Air Development Center.
5. EOS-1, EOS-2, etc. Electrical Overstress/Electrostatic Discharge Symposium Proceedings 1979 to current year.
6. MIL-STD-883C Test Methods and Procedures For Microelectronics
7. MIL-M-38510F Microcircuits, General Specification for
8. MIL-M-55565A Microcircuits, Packaging of
9. MIL-M-81705B Barrier Materials, Flexible, Electrostatic—Free, Heat Sealable
10. FED-STD-101 Preservation, Packaging and Packing Materials Test Procedures; Test Methods. 4046: Electrostatic Properties of

NOTES

Introduction

Linear Technology Corporation was founded in 1981 to address the growing demand for high performance and superior quality linear integrated circuits.

Today, Linear Technology has successfully established a leadership position by introducing and supplying leading edge products in each of the industry's basic functional groups—op amps, comparators, voltage regulators, references, switched-capacitor filters, interface, data conversion, and a variety of special function CMOS devices, in all major package styles.

Early on, Linear Technology made the commitment to provide advanced technology, *surface mount packaging*. This makes Linear Technology the first company to offer true precision and high performance linear devices across the full range of functional categories, plus many of the popular second-source devices in JEDEC Standard SO-8, 14, 16 and SOL-16, 18 and 20 pin packages.

Support for Linear Technology's surface mount devices includes service for tape and reel, anti-static rails, quality and reliability data, and datasheets on each product.

Linear Technology intends to address customer demand for surface mount devices where technology and die sizes permit, making the combination of small package size and high performance linear devices readily available to our users.

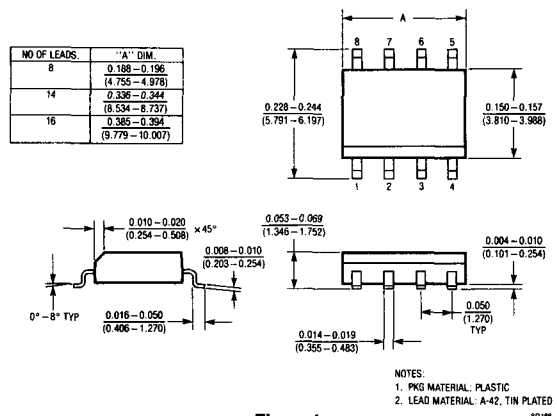
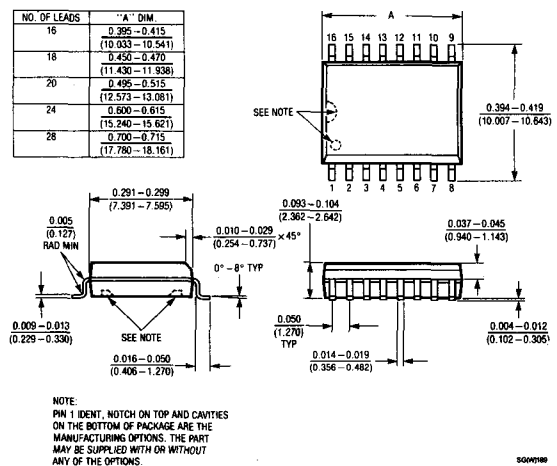
This section contains information summarizing Linear Technology's capabilities and services for surface mount packaged products, as well as specific device datasheets.

Package Descriptions

Linear Technology's SO packages conform to Standard JEDEC SOIC outlines. Figure 1 represents the 8, 14 and 16-lead narrow (150 mil width) SO packages. The 300 mil width large cavity SOL package is pictured in Figure 2.

In some instances, an LTC product available in an 8-pin standard DIP package is offered in a 16-pin SOL package. This covers the situation where the die is too large to be

accommodated by the smaller SO-8 package. Although it is preferable for an SO-8 device to have the same pin-out as the standard 8-pin dual-in-line version, some devices necessitate a rotation of the die to fit in the SO-8 package. Please refer to the applicable SO device datasheet, or consult with the factory to verify exact pinouts for each device.


Figure 1

Figure 2

SURFACE MOUNT PRODUCTS

Electrical Specifications

Wherever possible, electrical specifications for an SO device are the same as the plastic molded equivalent. Exceptions to this are identified by the omission of the standard product electrical grade designator from the part number. For example:

—LT1013DS8 has the same electrical specifications as LT1013DN8, since the “D” is common to both product numbers.

—LT1012S8 has one or more different electrical specifications than LT1012CN8, as the “C” is missing from this product designator suffix.

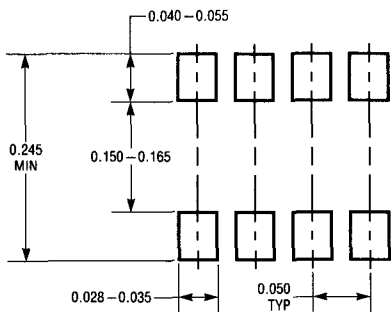
Please consult the appropriate SO package datasheet for complete electrical specifications.

Marking

Because of the limited space available for part marking on some SO packages, abbreviated marking codes are used to identify the device. These codes, if used, are identified in the individual SO package datasheets.

Recommended Solder Pads

SO-8, SO-14, SO-16



SOL-16, SOL-18, SOL-20

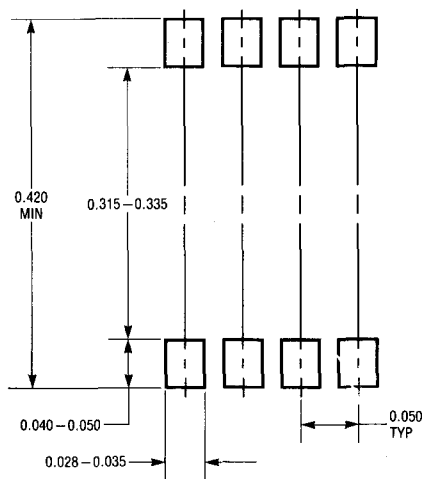


Figure 3. Wave and Reflow Soldering

Lead Finish and Solderability

Lead finish is electroplated, matte-tin, with a low carbon content. Solderability meets the requirements of MIL-STD-883C, Method 2003. Recommended solder pads are given in Figure 3.

Wave and Reflow Soldering

Following are the recommended procedures for soldering surface mount packages to PC boards.

1. Wave Soldering

- Use solder plating boards.
- Dispense adhesive to hold components on board.
- Place components on board.
- Cure adhesive per adhesive manufacturer's specification.
- Foam flux using RMA (Rosin Mildly Activating) flux or an organic acid flux if more aggressive flux is required.
- Wave solder using a dual wave soldering system at 240°C to 260°C for 2 seconds per wave.
- Clean board.

* Note: LTC packages will survive temperatures of 260°C for 10 seconds.

2. Reflow Soldering

- Use solder plating boards.
- Screen solder paste on board.
- Mount components on board.
- Bake for 15–20 minutes at 65°C–90°C.
- Reflow solder paste. The solder paste temperature must be 200°C for at least 30 seconds. LTC recommends vapor phase or infra red reflow systems for best performance.
- Clean boards.

Thermal Information

Table 1 shows the range of junction-to-ambient thermal resistance of devices mounted on a PCB of FR4 material with copper traces, in still air at 25°C. θ_{JA} with a ceramic substrate is about 70% of the FR4 value. Maximum power dissipation may be calculated by the following formula:

$$P_{D\text{ MAX}}[T_A] = \frac{T_{j\text{ MAX}} - T_A}{\theta_{JA}}$$

where $T_{j\text{ MAX}}$ = Maximum operating junction temperature.
 T_A = Desired ambient operating temperature.
 θ_{JA} = Junction to ambient thermal resistance.

SO-8	150 to 200°C/W	SOL-16	85 to 100°C/W
SO-14	100 to 140°C/W	SOL-18	70 to 100°C/W
SO-16	90 to 130°C/W	SOL-20	70 to 90°C/W

Conditions: PCB mount on FR4 material, still air at 25°C, copper trace.

Table 1. Typical Thermal Resistance Values

Product Reliability

Linear Technology Corporation publishes a reliability data pak on a quarterly basis for our complete range of hermetic and plastic devices. The data generated on the SO-8 compares favorably with that generated for dual-in-line packages. The tests that are run to assess package and device reliability are high temperature operating life with electrical bias, temperature and humidity under bias (85/85), autoclave, temperature cycle, and thermal shock. A sample of the data for the S8 (SO-8 small outline plastic DIP) is shown below.

S8 (8 Lead Small Outline Plastic DIP) Reliability Data • October 1986

• Operating Life

DEVICE TYPE	SS	# DEVICE HOURS AT 150°C	# DEVICE HOURS AT 125°C ⁽¹⁾	# DEVICE HOURS AT 55°C ⁽¹⁾	# FAILURES
OP07	200	211.8K	1186.1K	591.9KK	0
LT385-1.2	40	41.9K	234.7K	117.1KK	0
LT1012	46	29.4K	164.6K	82.1KK	0
LTC1044/7660	59	47.4K	265.6K	132.5KK	0
LT1021	45	23.4K	131.0K	65.4KK	0
	390	353.9K	1982.0K	989.0KK	0 ⁽⁴⁾

• 85/85 With Bias

DEVICE TYPE	SS	TOTAL DEVICE HOURS	# FAILURES
OP07	153	234.3K	0
LTC1044C	78	114.2K	0
		348.5K	0

• Autoclave

DEVICE TYPE	SS	TOTAL DEVICE HOURS	# FAILURES
OP07	304	280.4K	0
LTC1044C	103	161.8K	1 ⁽³⁾
LM385B-1.2	85	129.6K	0
LT1012	148	38.0K	1
		589.8K	2

• Temperature Cycle (Air to Air) – 65°C to 150°C

DEVICE TYPE	SS	TOTAL DEVICE CYCLES	# FAILURES
OP07	155	465.0K	0
LTC1044C	96	192.0K	0
		657.0K	0

• Thermal Shock (Liquid to Liquid) – 65°C to 150°C

DEVICE TYPE	SS	TOTAL DEVICE CYCLES	# FAILURES
OP07	156	312.0K	0
LTC1044C	96	91.7K	0
		403.7K	0

Note 1: Assumes $E_g = 1.0\text{eV}$.

Note 2: 1 Fit = 1 failure in 10^9 device hours.

Note 3: Non-functional—Bonding pad corrosion.

Note 4: Failure rate at 55°C 1.2 fits⁽²⁾ to a 60% confidence level.

More current data, by device type, may be obtained by contacting Linear Technology Corporation, Marketing Department.

SURFACE MOUNT PRODUCTS

Tape and Reel Packing

Tape and reel packing is available for all SO and SOL packages (except 18-lead) in accordance with EIA Specification 481-A. Table 2 lists the applicable tape widths, dimensions, and quantities for all LTC small-outline products. Consult factory for tape and reel pricing and minimum order requirements.

PACKAGE	TAPE SIZE	COMPONENT PITCH	HOLE PITCH	REEL DIAMETER	PARTS PER REEL
SO-8	12mm	8mm	4mm	13"	2500
SO-14	16mm	8mm	4mm	13"	2500
SO-16	16mm	8mm	4mm	13"	2500
SOL-16	16mm	12mm	4mm	13"	1000
SOL-18*	—	—	—	—	—
SOL-20	24mm	12mm	4mm	13"	1000

*Unavailable at this time.

Table 2. Tape and Reel Packing Specifications

Plastic Tube Packing

Linear Technology SO and SOL packaged devices are packed in conductive plastic tubes with the dimensions indicated in Figure 4. Unit quantities per tube are as listed in Table 3.

SO-8	100 ea.	SOL-16	50 ea.
SO-14	60 ea.	SOL-18	40 ea.
SO-16	50 ea.	SOL-20	40 ea.
		SOL-24	31 ea.
		SOL-28	27 ea.

Table 3. Devices Per Tube

Linear Technology Corp. packs their SO and SOL products in either conductive plastic tubes or tape and reel, depending on customer preference. Plastic tubes are manufactured to LTC specifications, while tape and reel packing

follows EIA specification 481-A, and is an extra cost item. The following pages describe and detail these packing methods.

PLASTIC TUBE SPECIFICATIONS

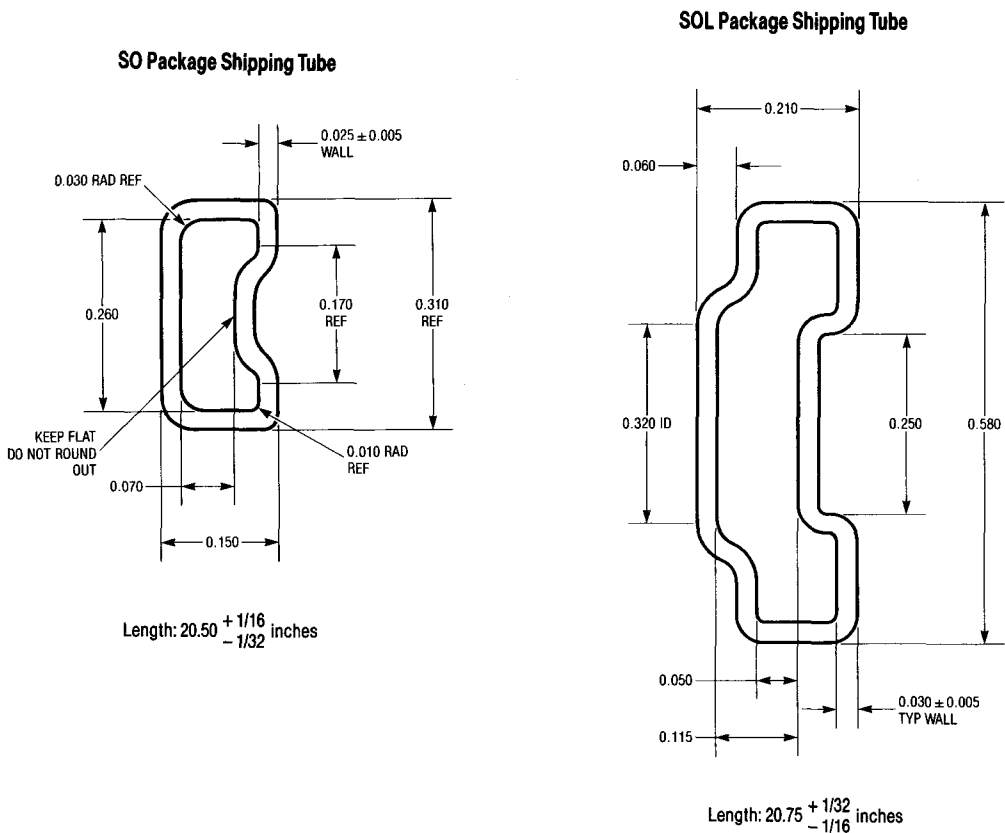


Figure 4.

Note 1: Tolerances: ± 0.010 unless otherwise specified.

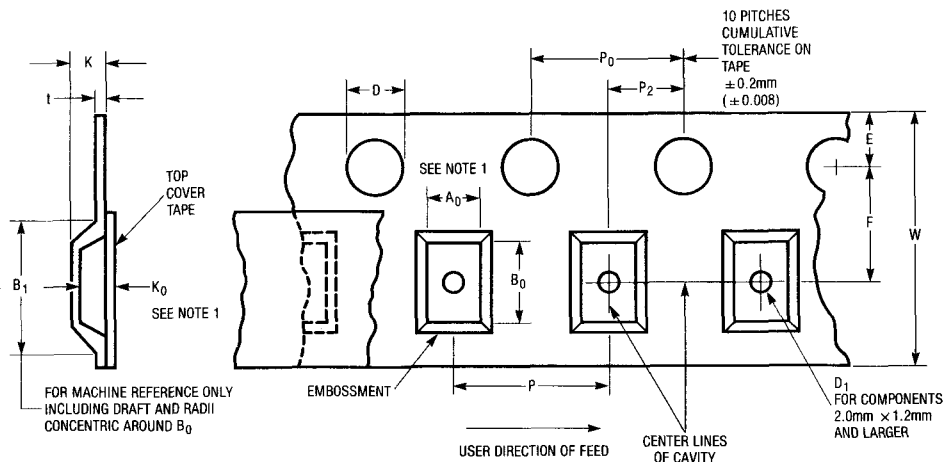
Note 2: Material: anti-static treated rigid transparent PVC or rigid black conductive.

Note 3: Printing: "LTC logo, Linear Technology Corp., Antistatic" on top side of tube.

SURFACE MOUNT PRODUCTS

TAPE AND REEL SPECIFICATIONS

Embossed Carrier Dimensions (12, 16, 24mm Tape Only)



Embossed Tape—Constant Dimensions

Tape Size	D	E	P_0	t(Max.)	$A_0 B_0 K_0$
12, 16, 24mm	1.5 +0.10 -0.0 0.059	1.75 ± 0.10 (0.069 ± 0.004)	4.0 ± 0.10 (0.157 ± 0.004)	0.400 (0.016)	See Note 1

Embossed Tape—Variable Dimensions

Tape Size	B_1 Max.	D_1 Min.	F	K Max.	P_2	R Min.	W	P (SO)	P (SOL)
12mm	8.2 (0.323)	1.5 (0.059)	5.5 ± 0.05 (0.217 ± 0.002)	4.5 (0.177)	2.0 ± 0.05 (0.079 ± 0.002)	30 (1.181)	12.0 ± 0.30 (0.472 ± 0.012)	8.0 ± 0.10 (0.315 ± 0.04)	12.0 ± 0.10 (0.472 ± 0.004)
16mm	12.1 (0.476)		7.5 ± 0.10 (0.295 ± 0.004)	6.5 (0.256)	2.0 ± 0.10 (0.079 ± 0.004)	40 (1.575)	16 ± 0.30 (0.630 ± 0.012)	8.0 ± 0.10 (0.315 ± 0.04)	
24mm	20.1 (0.791)		11.5 ± 0.10 (0.453 ± 0.004)			50 (1.969)	24 ± 0.30 (0.945 ± 0.012)		

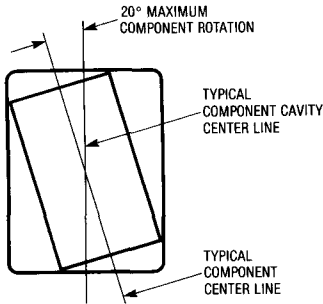
Note 1: $A_0 B_0 K_0$ are determined by component size. The clearance between the component and the cavity must be within 0.05 (0.002) min. to 0.65 (0.026) max. for 12mm tape, 0.05 (0.002) min. to 0.90 (0.035) max. for 16mm tape and 0.05 (0.002) min. to 1.00 (0.039) max. for 24mm tape and larger. The compo-

nent cannot rotate more than 20° within the determined cavity, see Component Rotation.

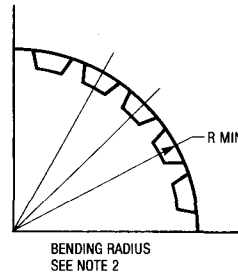
Note 2: Tape and components shall pass around radius "R" without damage.

TAPE AND REEL SPECIFICATIONS

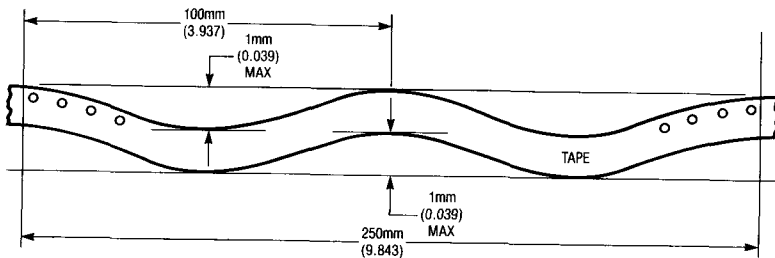
Component Rotation



Bending Radius

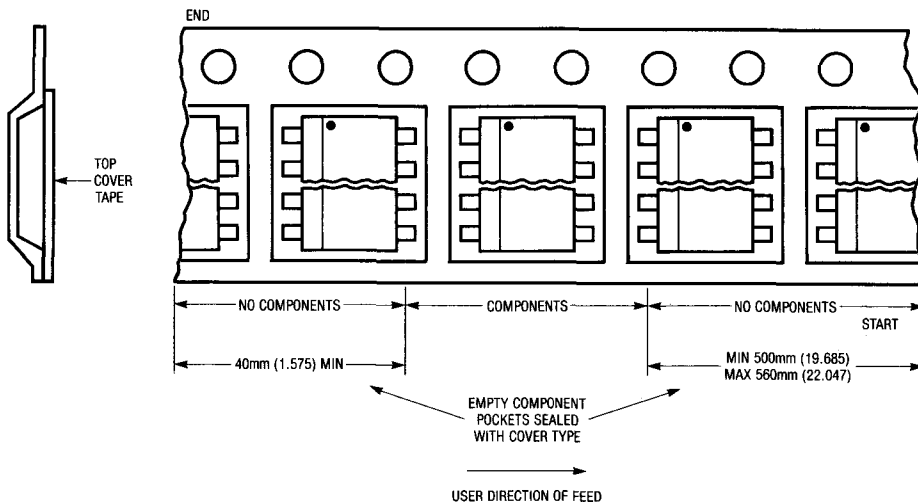


Tape Camber (Top View)



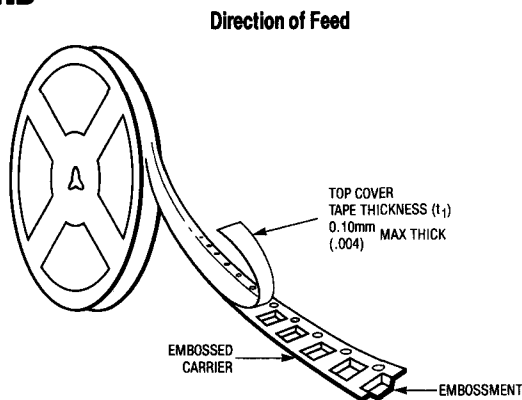
Allowable camber to be 1mm/100mm nonaccumulative over 250mm

Tape Leader (Start/End) Specification

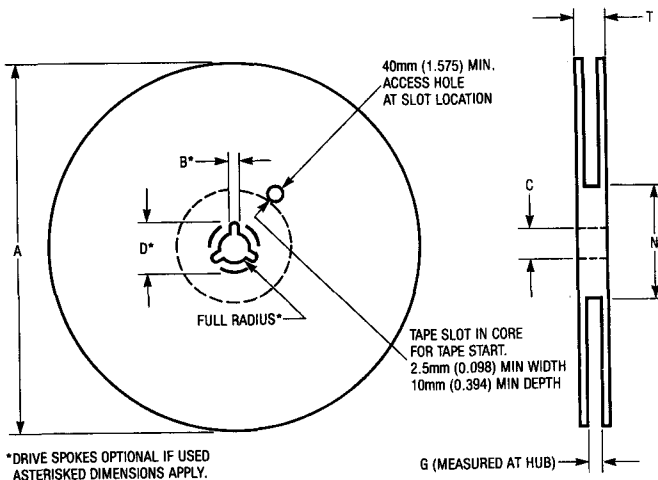


SURFACE MOUNT PRODUCTS

REEL DIMENSIONS



Reel Dimensions



*DRIVE SPOKES OPTIONAL IF USED
ASTERISKED DIMENSIONS APPLY.

Tape Size	A Max.	B Min.	C	D* Min.	N Min.	G	T Max.
12mm	330 (12.992)	1.5 (0.059)	13.0 ± 0.20 (0.512 ± 0.008)	20.2 (0.795)	50 (1.969)	12.4 +2.0 -0.0 (0.488 +0.078 -0.0)	18.4 (0.724)
16mm	360 (14.173)	1.5 (0.059)	13.0 ± 0.20 (0.512 ± 0.008)	20.2 (0.795)	50 (1.969)	16.4 +2.0 -0.0 (0.646 +0.078 -0.0)	22.4 (0.882)
24mm	360 (14.173)	1.5 (0.059)	13.0 ± 0.20 (0.512 ± 0.008)	20.2 (0.795)	50 (1.969)	24.4 +2.0 -0.0 (0.961 +0.078 -0.0)	30.4 (1.197)

*Metric dimensions will govern.
English measurements rounded and for reference only.

SURFACE MOUNT PARTS LIST

LF398S8, Precision Sample and Hold Amplifier	9-113
LM318S8, High Speed Op Amp	2-319
LM334S8, Constant Current Source and Temperature Sensor	3-99
LM385S8-1.2/LM385S8-2.5, Micropower Voltage Reference	3-113
LT1001CS8, Precision Op Amp	2-23
LT1004CS8-1.2/LT1004CS8-2.5, Micropower Voltage References	3-25
LT1006S8, Precision, Single Supply Op Amp	2-53
LT1007CS/LT1037CS, Low Noise, High Speed Precision Op Amps	2-69
LT1009S8, 2.5 Volt Reference	3-31
LT1012S8, Picoamp Input Current, Microvolt Offset, Low Noise Op Amp	2-117
LT1013DS8, Dual Precision Op Amp	2-141
LT1016CS8, Ultra Fast Precision Comparator	6-41
LT1017CS/LT1018CS, Micropower Dual Comparator	6-53
LT1020CS, Micropower Regulator and Comparator	4-45
LT1021DCS8, Precision Reference	3-57
LT1028CS, Ultra-Low Noise Precision High Speed Op Amp	2-177
LT1030CS, Quad Low Power Line Driver	10-9
LT1034CS8-1.2/LT1034CS8-2.5, Micropower Dual Reference	3-81
LT1054CS/LT1054IS, Switched Capacitor Voltage Converter with Regulator	5-35
LT1055S8/LT1056S8, Precision, High Speed, JFET Input Op Amps	2-231
LT1057S/LT1057IS, Dual JFET Input Precision High Speed Op Amps	2-247
LT1080CS/LT1081CS, 5V Powered RS232 Driver/Receiver with Shutdown	10-51
LTC1043CS, Dual Precision Instrumentation Switched-Capacitor Building Block	11-31
LTC1044CS8, Switched Capacitor Voltage Converter	5-21
LTC1052CS, Chopper-Stabilized Op Amp (CSOA™)	2-217
LTC1059CS, High Performance Switched Capacitor Universal Filter	7-11
LTC1060CS, Universal Dual Filter Building Block	7-35
LTC1061CS, High Performance Triple Universal Filter Building Block	7-55
LTC1062CS, 5th Order Low Pass Filter	7-71
OP-07CS8, Precision Op Amp	2-337
SG3524S, Regulating Pulse Width Modulator	5-93

NOTES

INTRODUCTION

Linear Technology Corporation offers a wide variety of precision linear IC's in die form. It is our intent to offer dice electrically tested to levels which can be expected to yield the best possible performance in hybrid circuits. Complicating this task is the fact that many specifications given for our standard packaged products cannot be tested at the wafer level. Further, parameters which are 100% tested at wafer probe testing may shift during the die attach/assembly process.

There is a Dice Products Catalog available that contains ordering information and datasheets for obtaining dice products. Catalogs are available from your local LTC Sales Rep, or from LTC Communications at (800) 637-5545.

GENERAL INFORMATION

Electrical Testing

Dice are 100% tested in wafer form at 25°C to the DC limits shown on the dice data sheet for a given device type. Many LTC packaged products have multiple electrical grades associated with a basic die type. A cross reference appears on each dice data sheet indicating which die product grade should be ordered to optimize candidates to meet the specifications of the desired finished product grade. This information should be used as a guideline only since LTC does not guarantee electrical specifications after assembly. Since electrical testing is done only at 25°C, no absolute guarantee can be made regarding performance at other temperatures. Some LTC products require post-package trimming to overcome certain assembly related parameter shifts. Details on this trimming may be obtained by contacting the factory.

Visual Inspection

Dice are 100% visually inspected in accordance with MIL-STD-883, Method 2010 Condition B.

Chip Dimensions

Chip dimensions are as indicated on individual dice data sheets. Tolerance is ± 1 mil. Chip thickness ranges from

12 mils to 20 mils, depending on product type. Bond pad dimensions are 4.5 x 4.5 mils. minimum.

Topside Passivation

Linear Technology products are passivated with a two layer system: A proprietary deposited oxide gives a crack-free conformal coverage of metal and oxide steps. A plasma nitride overcoat protects the die from ionic contamination and scratches during handling, testing and assembly. Note that LTC uses fuse link and zener zap trimming techniques which require windows in the passivation over the trim points. This passivation system is a major contributor to the extremely high reliability demonstrated throughout millions of device-hours of accelerated testing of LTC devices in plastic and hermetic packages.

Topside Metallization

The metallization is a minimum of 11,000 Å thick unless otherwise specified. The quality of the metallization step coverage is monitored via a weekly SEM inspection per MIL-STD-883, Method 2018.

Backside Metal

Most dice product backsides are coated with an alloyed gold layer. There are some CMOS products with no backside metallization. In addition, some voltage regulators may be specially ordered with a chrome-nickle-silver (Cr-Ni-Ag) backside layer. Contact LTC for details on this type of backside layer or to inquire about availability of LTC products with a particular backside metallization.

Backside Potential

Linear Technology products are junction isolated. For proper operation the backside must be electrically connected to the most negative potential seen by the IC (for bipolar products) or the most positive potential (for CMOS products). This information is also given in the individual dice data sheets.

DICE PRODUCTS

Packaging

Dice are packaged in compartmentalized waffle packs for ease of handling and storage. Each waffle pack contains 100 dice. Special packaging methods are also available by contacting the factory.

Quality Levels of Dice Shipped

Each dice lot is guaranteed to meet the following requirements:

- Internal visual per MIL-STD-883, Method 2010 Condition B: 1.0% AQL Level II.
- Electrical: Due to variations in assembly methods and packaging techniques LTC does not guarantee electrical specifications after assembly. When a determination as to the finished product assembly yield is needed, the lot acceptance testing available at extra cost should be pursued.

Reliability Assurance

In addition to the more conventional reliability audits performed on finished products, LTC has innovated a unique periodic wafer fab reliability audit using a specially designed reliability structure that is stepped into all wafers. The test structure is optimized to accelerate the two primary failure mechanisms in linear circuits, namely mobile positive ions and surface charge-induced inversions. This provides a continuous monitor on the reliability performance of LTC's wafer fab processes and provides immediate feedback to wafer fab typically within one week.

Electrostatic Discharge (ESD) Precautions

Precision linear devices, especially those with very low (pA) input bias current levels and low (<50 microvolts) input offset voltages are susceptible to shifts in electrical performance and ESD damage as a result of improper handling. LTC recommends that ESD precautions, such as grounded conductive work stations, grounded conductive wrist straps and grounded equipment, be taken to prevent ESD damage.

ORDERING INFORMATION

Dice may be ordered by the part number defined in the dice data sheet. Minimum direct dice order, per delivery, is 1000 pieces or \$5,000, whichever is greater. In some cases, tighter parameter selections than indicated on the dice data sheets can be obtained by special order. Please contact the factory for details.

Lot Acceptance Testing

Lot acceptance testing (L.A.T.) based on sample assembly and testing is available at extra cost. Sample sizes and acceptable electrical test limits vary from device to device and must be negotiated at the time of quoting. Contact the factory for details.

- AN1 Understanding and Applying the LT1005 Multifunction Regulator**
 This application note describes the unique operating characteristics of the LT1005 and describes a number of useful applications which take advantage of the regulator's ability to control the output with a logic control signal.
- AN2 Performance Enhancement Techniques for 3-Terminal Regulators**
 This application note describes a number of enhancement circuit techniques used with existing 3-terminal regulators which extend current capability, limit power dissipation, provide high voltage output, operate from 110VAC or 220VAC without the need to switch transformer windings, and many other useful application ideas.
- AN3 Applications for a Switched-Capacitor Instrumentation Building Block**
 This application note describes a wide range of useful applications for the LTC1043 dual precision instrumentation switched-capacitor building block. Some of the applications described are ultra high performance instrumentation amplifier, lock-in amplifier, wide range digitally controlled variable gain amplifier, relative humidity sensor signal conditioner, LVDT signal conditioner, charge pump F to V and V to F converters, 12-bit A to D converter and more.
- AN4 Applications for a New Power Buffer**
 The LT1010 150 μ A power buffer is described in a number of useful applications such as boosted op amp, a feed-forward, wide-band DC stabilized buffer, a video line driver amplifier, a fast sample-hold with hold step compensation, an overload protected motor speed controller, and a piezoelectric fan servo.
- AN5 Thermal Techniques in Measurement and Control Circuitry**
 6 applications utilizing thermally based circuits are detailed. Included are a 50MHz RMS to DC converter, an anemometer, a liquid flowmeter and others. A general discussion of thermodynamic considerations involved in circuitry is also presented.
- AN6 Applications of New Precision Op Amps**
 Application considerations and circuits for the LT1001 and LT1002 single and dual precision amplifiers are illustrated in a number of circuits, including strain gauge signal conditioners, linearized platinum RTD circuits, an ultra precision dead zone circuit for motor servos and other examples.
- AN7 Some Techniques for Direct Digitization of Transducer Outputs**
 Analog-to-digital conversion circuits which directly digitize low level transducer outputs, without DC preamplification, are presented. Covered are circuits which operate with thermocouples, strain gauges, humidity sensors, level transducers and other sensors.
- AN8 Power Conditioning Techniques for Batteries**
 A variety of approaches for power conditioning batteries is given. Switching and linear regulators and converters are shown, with attention to efficiency and low power operation. 14 circuits are presented with performance data.
- AN9 Application Considerations and Circuits for a New Chopper-Stabilized Op Amp**
 A discussion of circuit, layout and construction considerations for low level DC circuits includes error analysis of solder, wire and connector junctions. Applications include sub-microvolt instrumentation and isolation amplifiers, stabilized buffers and comparators and precision data converters.
- AN11 Designing Linear Circuits for 5V Operation**
 This note covers the considerations for designing precision linear circuits which must operate from a single 5V supply. Applications include various transducer signal conditioners, instrumentation amplifiers, controllers and isolated data converters.
- AN12 Circuit Techniques for Clock Sources**
 Circuits for clock sources are presented. Special attention is given to crystal-based designs including TXCOs and VXCOs.
- AN13 High Speed Comparator Techniques**
 The AN13 is an extensive discussion of the causes and cures of problems in very high speed comparator circuits. A separate applications section presents circuits, including a 0.025% accurate 1Hz-30MHz V to F converter, a 200ns 0.01% sample-hold and a 10MHz fiber optic receiver. Five appendices covering related topics complete this note.
- AN14 Designs for High Frequency Voltage-To-Frequency Converters**
 A variety of high performance V to F circuits is presented. Included are a 1Hz to 100MHz design, a quartz stabilized type and a 0.0007% linear unit. Other circuits feature 1.5V operation, sine wave output and non-linear transfer functions. A separate section examines the trade-offs and advantages of various approaches to V to F conversion.
- AN15 Circuitry for Single Cell Operation**
 1.5V powered circuits for complex linear functions are detailed. Designs include a V to F converter, a 10 bit A-D, sample-hold amplifiers, a switching regulator and other circuits. Also included is a section on component considerations for 1.5V powered linear circuits.
- AN16 Unique IC Buffer Enhances Op Amp Designs, Tames Fast Amplifiers**
 This note describes some of the unique IC design techniques incorporated into a fast, monolithic power buffer, the LT1010. Also, some application ideas are described such as capacitive load driving, boosting fast op amp output current and power supply circuits.
- AN17 Considerations for Successive Approximation A - D Converters**
 A tutorial on SAR type A-D converters, this note contains detailed information on several 12-bit circuits. Comparator, clocking, and pre-amplifier designs are discussed. A final circuit gives a 12-bit conversion in 1.8 μ s. Appended sections explain the basic SAR technique and explore DAC considerations.
- AN18 Power Gain Stages for Monolithic Amplifiers**
 This note presents output stage circuits which provide power gain for monolithic amplifiers. The circuits feature voltage gain, current gain, or both. Eleven designs are shown, and performance is summarized. A generalized method for frequency compensation appears in a separate section.

APPLICATION NOTES

AN19 LT1070 Design Manual

This design manual is an extensive discussion of all standard switching configurations for the LT1070; including buck, boost, flyback, forward, inverting and "Cuk". The manual includes comprehensive information on the LT1070, the external components used with it, and complete formulas for calculating component values.

AN20 Applications for a DC Accurate Low-Pass Switched-Capacitor Filter

Discusses the principles of operation of the LTC1062 and helpful hints for its application. Various application circuits are explained in detail with focus on how to cascade two LTC1062's and how to obtain notches. Noise and distortion performance are fully illustrated.

AN21 Composite Amplifiers

Applications often require an amplifier that has extremely high performance in several areas. For example, high speed and DC precision are often needed. If a single device cannot simultaneously achieve the desired characteristics, a composite amplifier made up of two (or more) devices can be configured to do the job. AN21 shows examples of composite approaches in designs combining speed, precision, low noise and high power.

AN22 A Monolithic IC for 100MHz RMS-DC Conversion

AN22 details the theoretical and application aspects of the LT1088 thermal RMS-DC converter. The basic theory behind thermal RMS-DC conversion is discussed and design details of the LT1088 are presented. Circuitry for RMS-DC converters, wideband input buffers and heater protection is shown.

AN23 Micropower Circuits for Signal Conditioning

Low power operation of electronic apparatus has become increasingly desirable. AN23 describes a variety of low power circuits for transducer signal conditioning. Also included are designs for data converters and switching regulators. Three appended sections discuss guidelines for micropower design, strobed power operation and effects of test equipment on micropower circuits.

AN24 Unique Applications for the LTC1062 Lowpass Filter

Highlights the LTC1062 as a lowpass filter in a phase lock loop. Describes how the loop's bandwidth can be increased and the VCO output jitter reduced when the LTC1062 is the loop filter. Compares it with a passive RC loop filter.

Also discussed is the use of LTC1062 as simple bandpass and bandstop filter.

AN25 Switching Regulators for Poets

Subtitled "A Gentle Guide for the Trepidatious", this is a tutorial on switching regulator design. The text assumes no switching regulator design experience, contains no equations, and requires no inductor construction to build the circuits described.

Designs detailed include flyback, isolated telecom, off-line, and others. Appended sections cover component considerations, measurement techniques and steps involved in developing a working circuit.

AN26

A collection of interface applications between various microprocessors/controllers and the LTC1090 family of data acquisition systems. The note is divided into sections specific to each interface. The following sections are available:

Number	A/D	Microprocessor/ Microcontroller
AN26A	LTC1090	8051
AN26B	LTC1090	68HC05
AN26C	LTC1090	63705
AN26D	LTC1090	COP820
AN26E	LTC1090	TMS7742
AN26F	LTC1090	COP402N
AN26G	LTC1091	8051
AN26H	LTC1091	68HC05
AN26I	LTC1091	COP820
AN26J	LTC1091	TMS7742
AN26K	LTC1091	COP402N
AN26L	LTC1091	HD63705VO
AN26M	LTC1090	TMS320C25
AN26N	LTC1091/92	TMS320C25
AN26O	LTC1090	Z-80
AN26P	LTC1090	HD64180
AN26Q	LTC1091	HD64180
AN26R	LTC1094	TMS320C25

These interface notes demonstrate the ease with which the LTC1090 family can be interfaced to microprocessors/controllers having either parallel or serial ports. A complete hardware and software description of the interface is included.

AN27A A Simple Method of Designing Multiple Order All Pole Bandpass Filters by Cascading 2nd Order Sections

Presents two methods of designing high quality Switched Capacitor bandpass filters. Both methods are intended to vastly simplify the mathematics involved in filter design by using tabular methods. The text assumes no filter design experience but allows high quality filters to be implemented by techniques not presented before in the literature. The designs are implemented by numerous examples using devices from LTC's Switched Capacitor filter family: LTC1060, LTC1061, and LTC1064. Butterworth and Chebyshev bandpass filters are discussed.

AN28 Thermocouple Measurement

Considerations for thermocouple based temperature measurement are discussed. A tutorial on temperature sensors summarizes performance of various types, establishing a perspective on thermocouples. Thermocouples are then focused on. Included are sections covering cold-junction compensation, amplifier selection, differential/isolation techniques, protection, and linearization. Complete schematics are given for all circuits. Processor based linearization is also presented with the necessary software detailed.

AN29 Some Thoughts on DC-DC Converters

This note examines a wide range of DC-DC converter applications. Single inductor, transformer, and switched capacitor converter designs are shown. Special topics like low noise, high efficiency, low quiescent current, high voltage, and wide-input voltage range converters are covered. Appended sections explain some fundamental properties of different types of converters.

AN30 Switching Regulator Circuit Collection

Switching regulators are of universal interest. Linear Technology has made a major effort to address this topic. A catalog of circuits has been compiled so that a design engineer can swiftly determine which converter type is best. This catalog serves as a visual index to be browsed through for a specific or general interest.

AN31 Linear Circuits for Digital Systems

Subtitled "Some Affable Analogs for Digital Devotees," discusses a number of analog circuits useful in predominantly digital systems. Vpp generators for flash memories receive extensive treatment. Other examples include a current loop transmitter, dropout detectors, power management circuits, and clocks.

AN32 High Efficiency Linear Regulators

Presents circuit techniques permitting high efficiency to be obtained with linear regulation. Particular attention is given to the problem of maintaining high efficiency with widely varying inputs, outputs and loading. Appendix sections review component characteristics and measurement methods.

AN33 Converting Light to Digits: LTC1099 Half Flash 8-Bit A/D Converter Digitizes Photodiode Array

This application note describes a Linear Technology "Half Flash" A/D converter, the LTC1099, being connected to a 256 element line scan photodiode array. This technology adapts itself to hand held (i.e. low power) bar code readers, as well as high resolution automated machine inspection applications.

AN34 LTC1099 Enables PC Based Data Acquisition Board to Operate DC-20kHz

A complete design for a data acquisition card for the IBM PC is detailed in this application note. Additionally, C language code is provided to allow sampling of data at speeds of more than 20kHz. The speed limitation is strictly based on the execution speed of the "C" data acquisition loop. A "Turbo" XT can acquire data at speeds greater than 20kHz. Machines with 80286 and 80386 processors can go faster than 20kHz. The computer that was used as a test bed in this application was an XT running at 4.77MHz and therefore all system timing and acquisition time measurements are based on that the 4.77MHz clock speed.

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